GA-M52L-S3

Revision:1.0

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27	FRONT PANEL POWER SEQUENCE
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29	PWM ISL6312
30	ITE 8716GB/ SPI BIOS
31	DDRII POWER

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M52L-S3 | Rev: 1.0

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Model Name:GA-M52L-S3 *Revision:1.0*

Component value change history

P-Code: U96058-0

Date	Change Item	Reason
2007.06.05	0.1 E_BOM release PCB:0.1	New BOM for MCP65V.
2007.06.13	0.2 E_BOM release PCB:0.2	Change chip to MCP61D for no MCP65V in MP
2007.07.06	1.0A P_BOM release PCB:1.0	Change PCB REV. to 1.0 Remove BC179 ADD AM2 TYCO socket & add packing BOM
2007.07.23	1.0A P_BOM release PCB:1.0	Add second source ---> W83310 & BAT54A & .22uF cap

Circuit or PCB layout change for next version

Date	Change Item	Reason
2007.06.04	0.1 Gerber Out	Modify from M52S-S3P, change to MCP65V chip
2007.06.12	0.2 Gerber Out	Modify from M52L-S3, change to MCP61D chip
		Add 2.2 ohm for noise.

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M52L-S3 | Rev: 1.0

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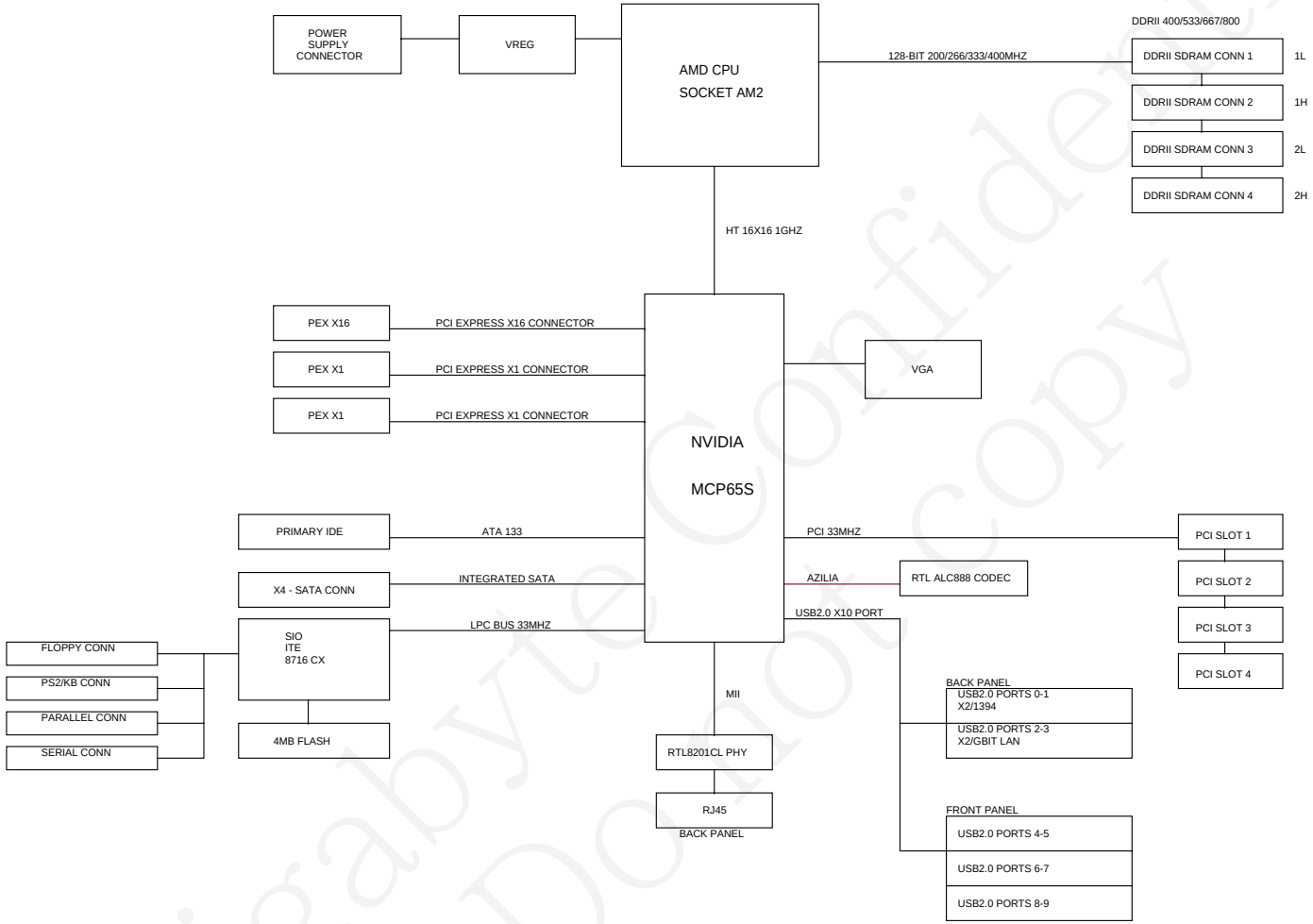
BLOCK DIAGRAM



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Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-M52L-S3	Rev: 1.0
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
VCC12_HT R3 49.9/4/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6 1	TP78
GND R4 49.9/4/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6 1	TP79
<11> L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2 L0_CTLOUT_H0	<11> L0_CTLOUT_H0 <11>
<11> L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3 L0_CTLOUT_L0	<11> L0_CTLOUT_L0 <11>
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

SOCKET_M2

M2/[12KRC-04K807-42R]

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Title: CPU HYPER TRANSPORT

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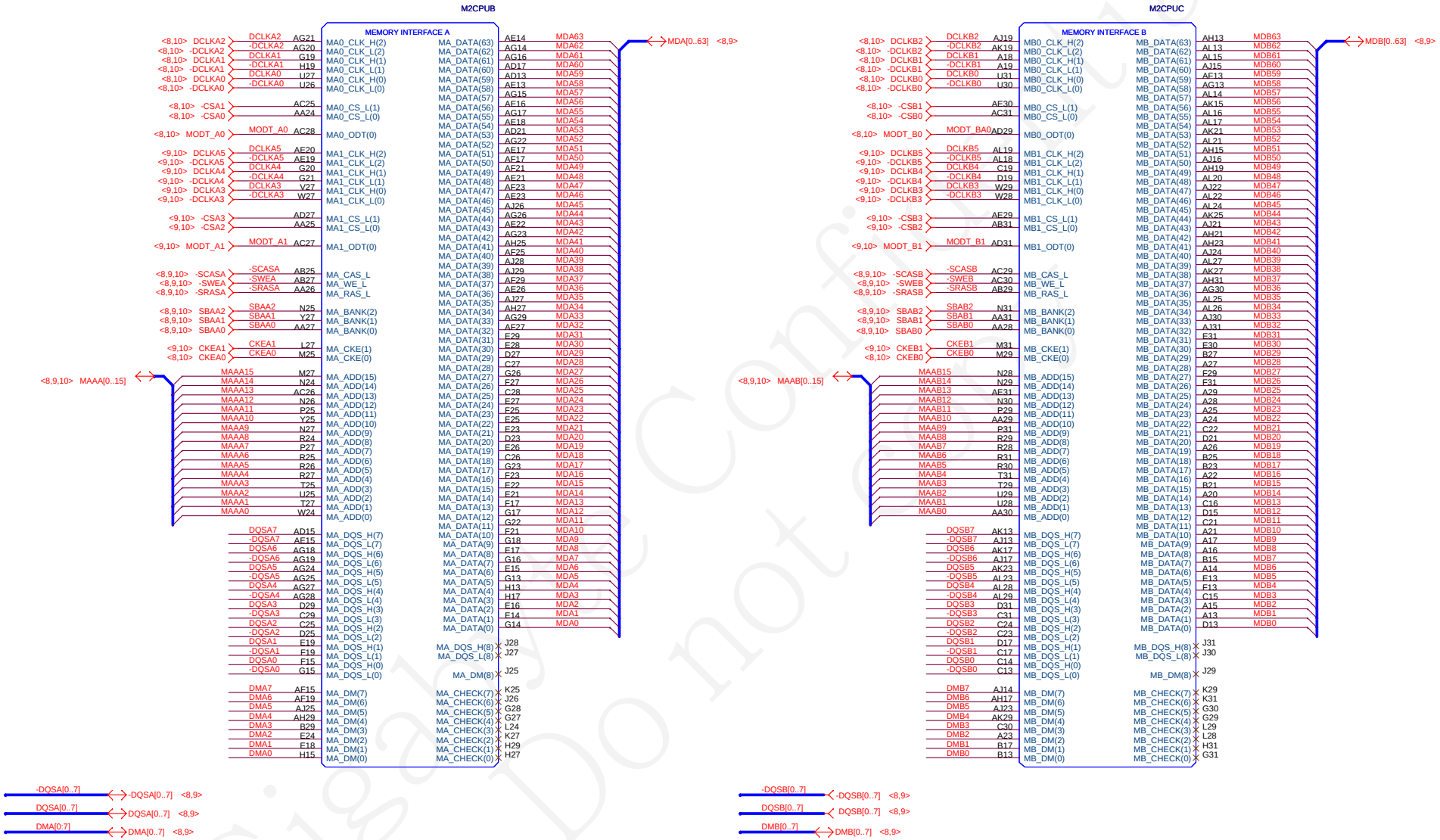

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Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-M52L-S3	Rev: 1.0
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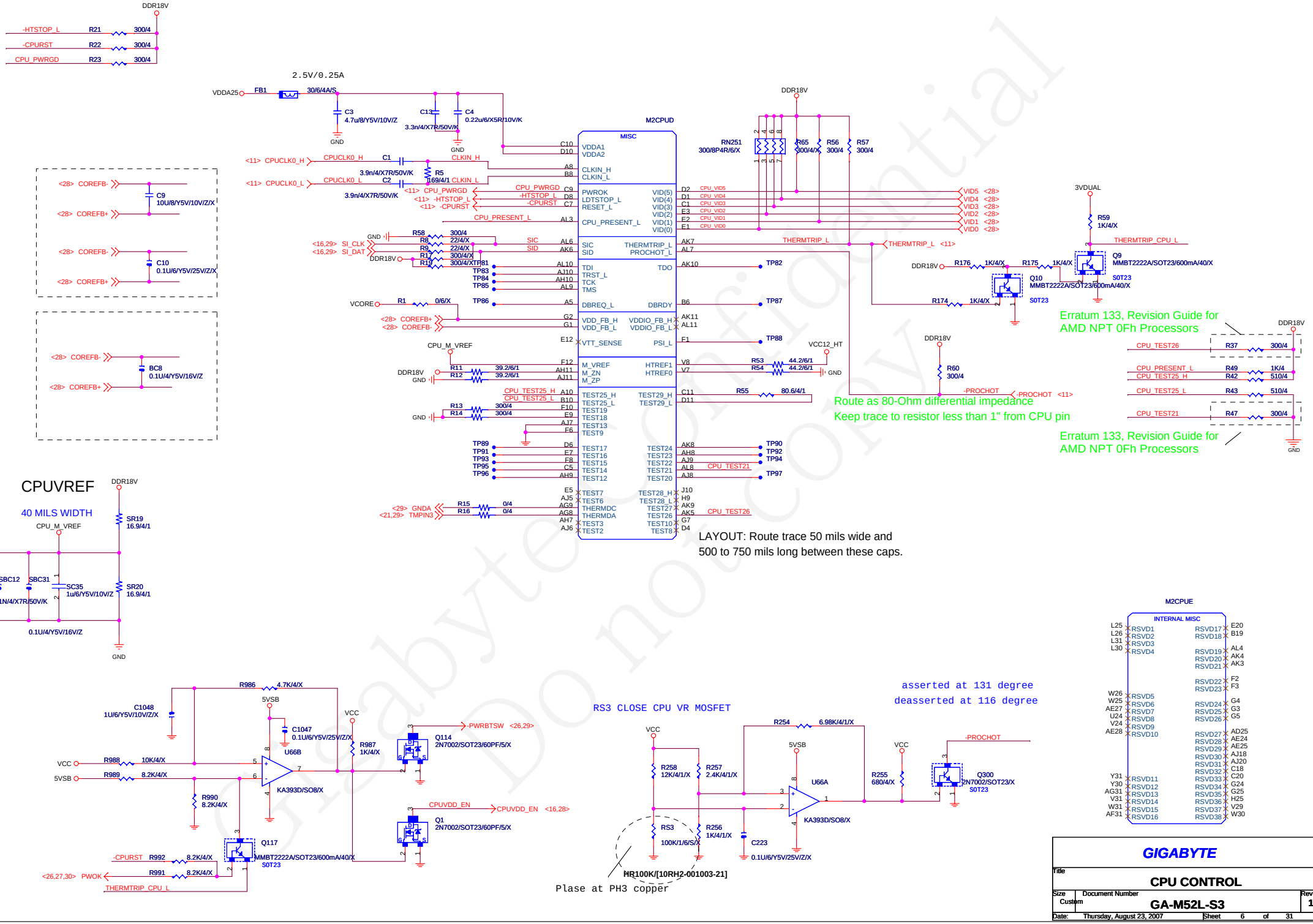
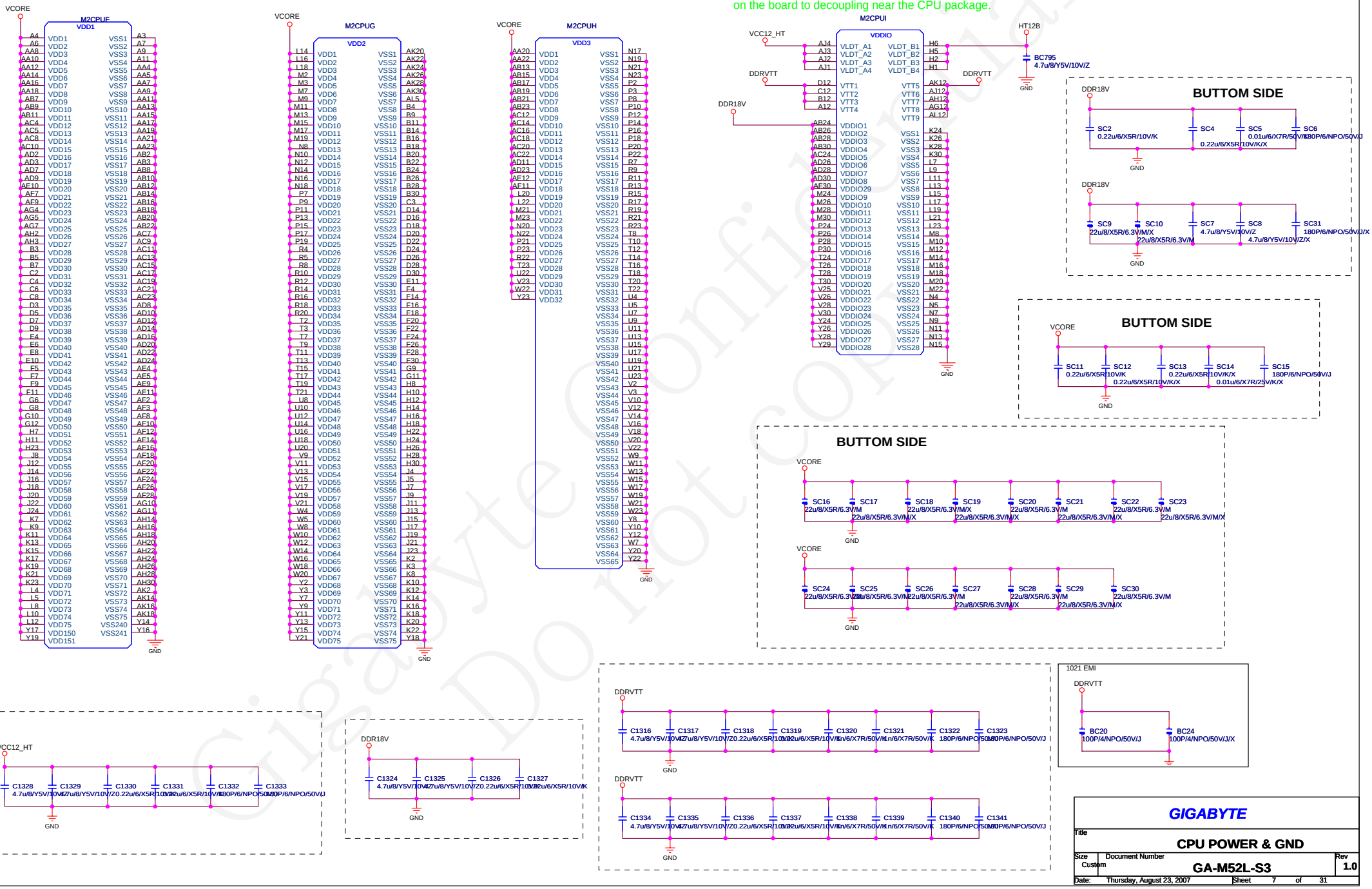


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Title	CPU POWER & GND		
Size: Custom	Document Number: GA-M52L-S3		Rev: 1.0
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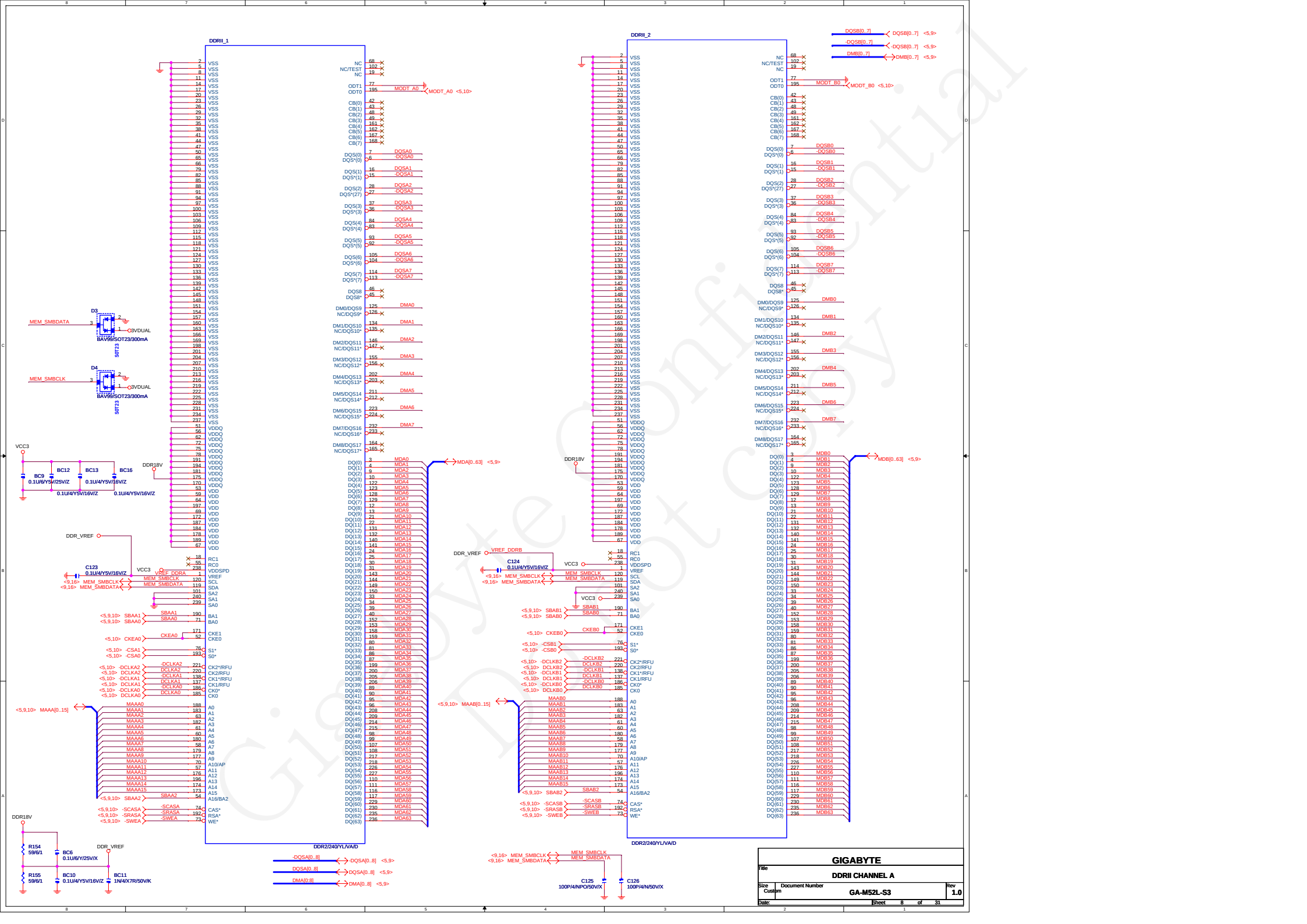
DDRII_1
DDRII_2
DDR2/240/YL/VA/D
DDR18V
VCC3
DDR_VREF
VREF_DDRA
VREF_DDRB
MEM_SMBDATA
MEM_SMBCLK
D3
D4
BAV99/SOT23/300mA
SOT23
3VDUAL
BC9 0.1U/6/Y5/25V/Z
BC12 0.1U/4/Y5V/16V/Z
BC13 0.1U/4/Y5V/16V/Z
BC16 0.1U/4/Y5V/16V/Z
C123 0.1U/4/Y5V/16V/Z
C124 0.1U/4/Y5V/16V/Z
C125 100P/4/NPO/50V/X
C126 100P/4/N/50V/X
R154 59/6/1
R155 59/6/1
BC6 0.1U/6/Y/25V/X
BC10 0.1U/4/Y5V/16V/Z
BC11 1N/4/X7R/50V/K
MODT_A0
MODT_B0
DQSB[0..7]
-DQSB[0..7]
DMB[0..7]
MDB[0..63]
MAAA[0..15]
MAAB[0..15]
-DQSA[0..8]
DQSA[0..8]
DMA[0..8]
GIGABYTE
DDRII CHANNEL A
GA-M52L-S3
1.0
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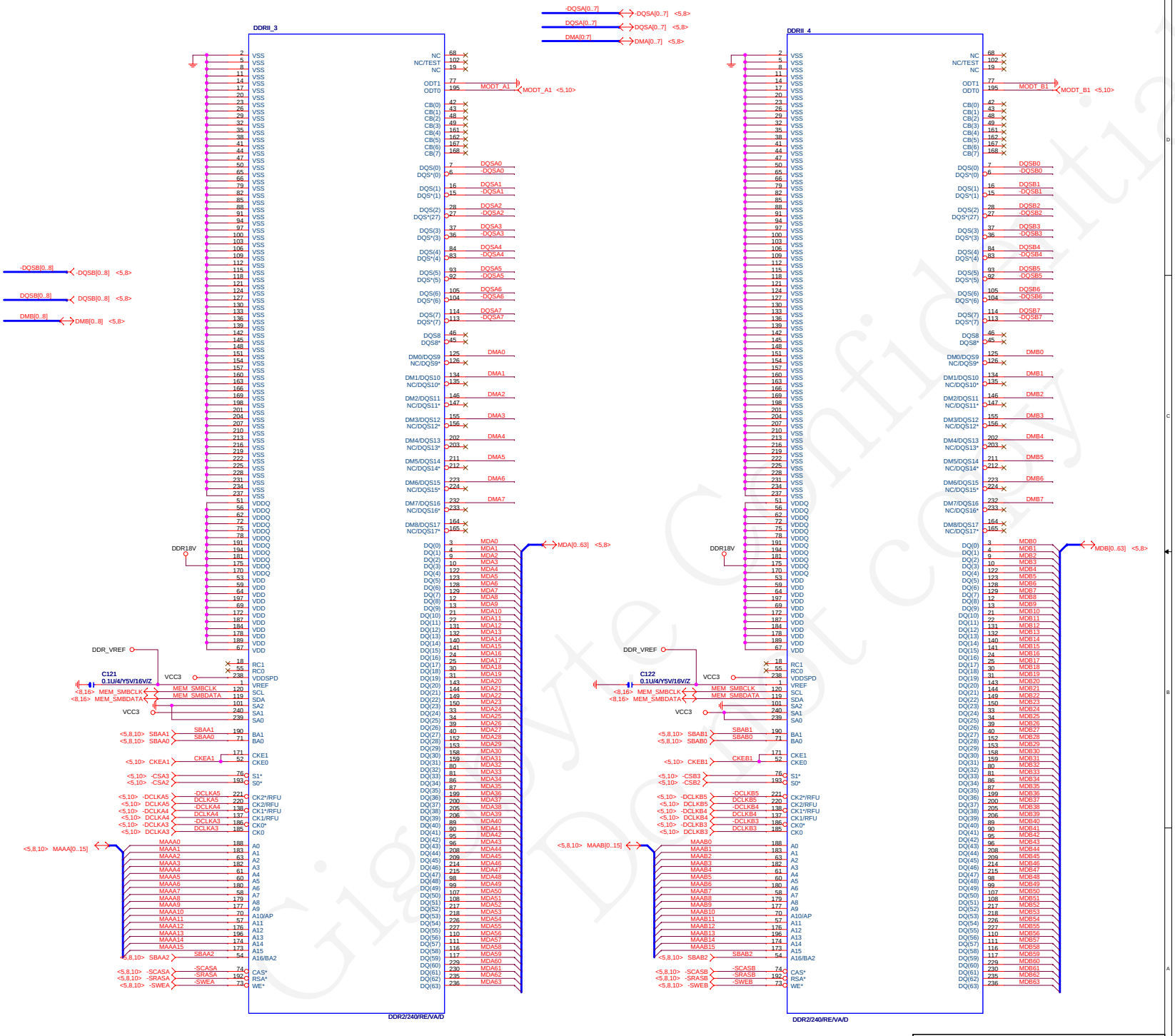

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Title	DDRII CHANNEL B	
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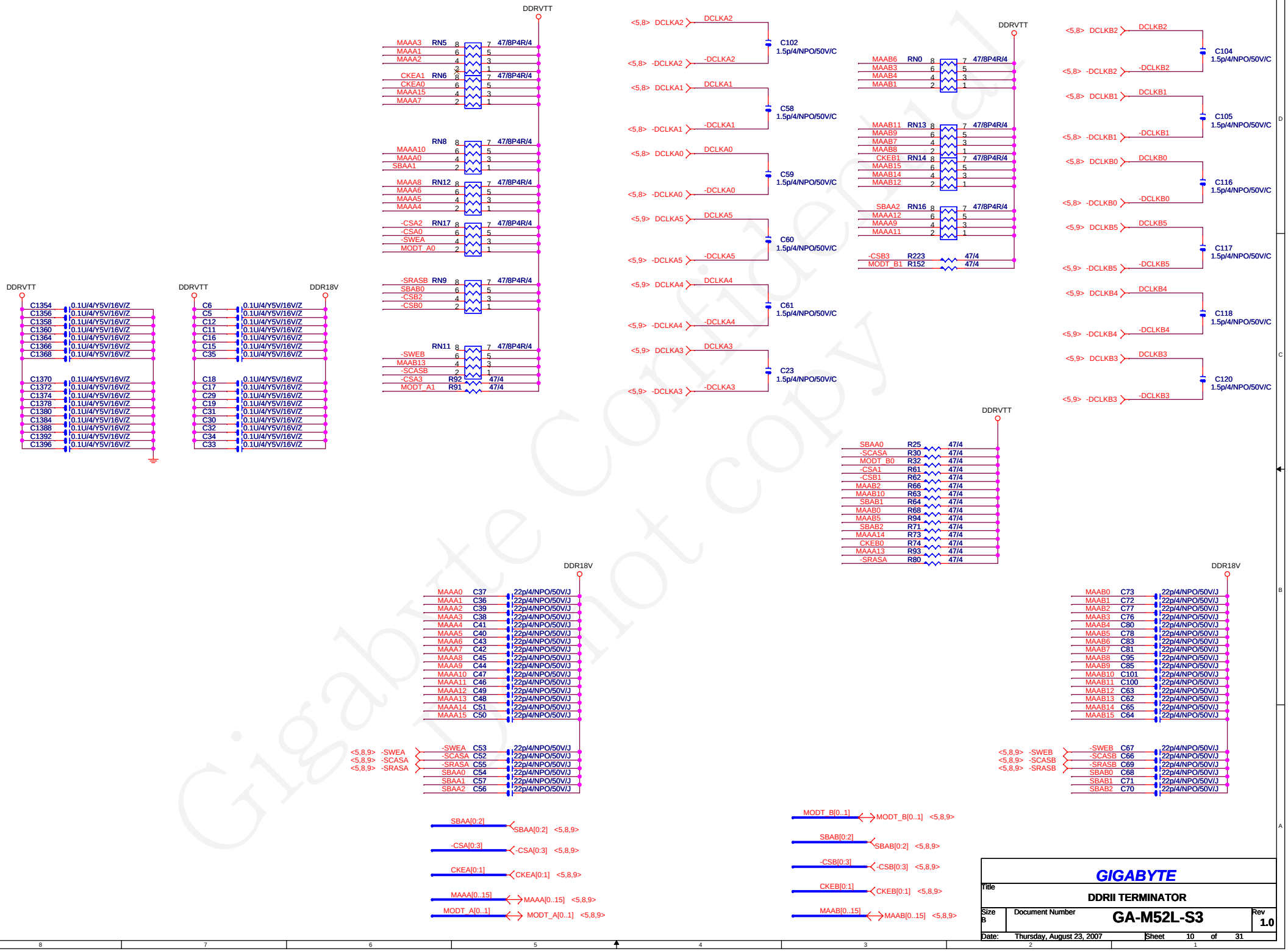
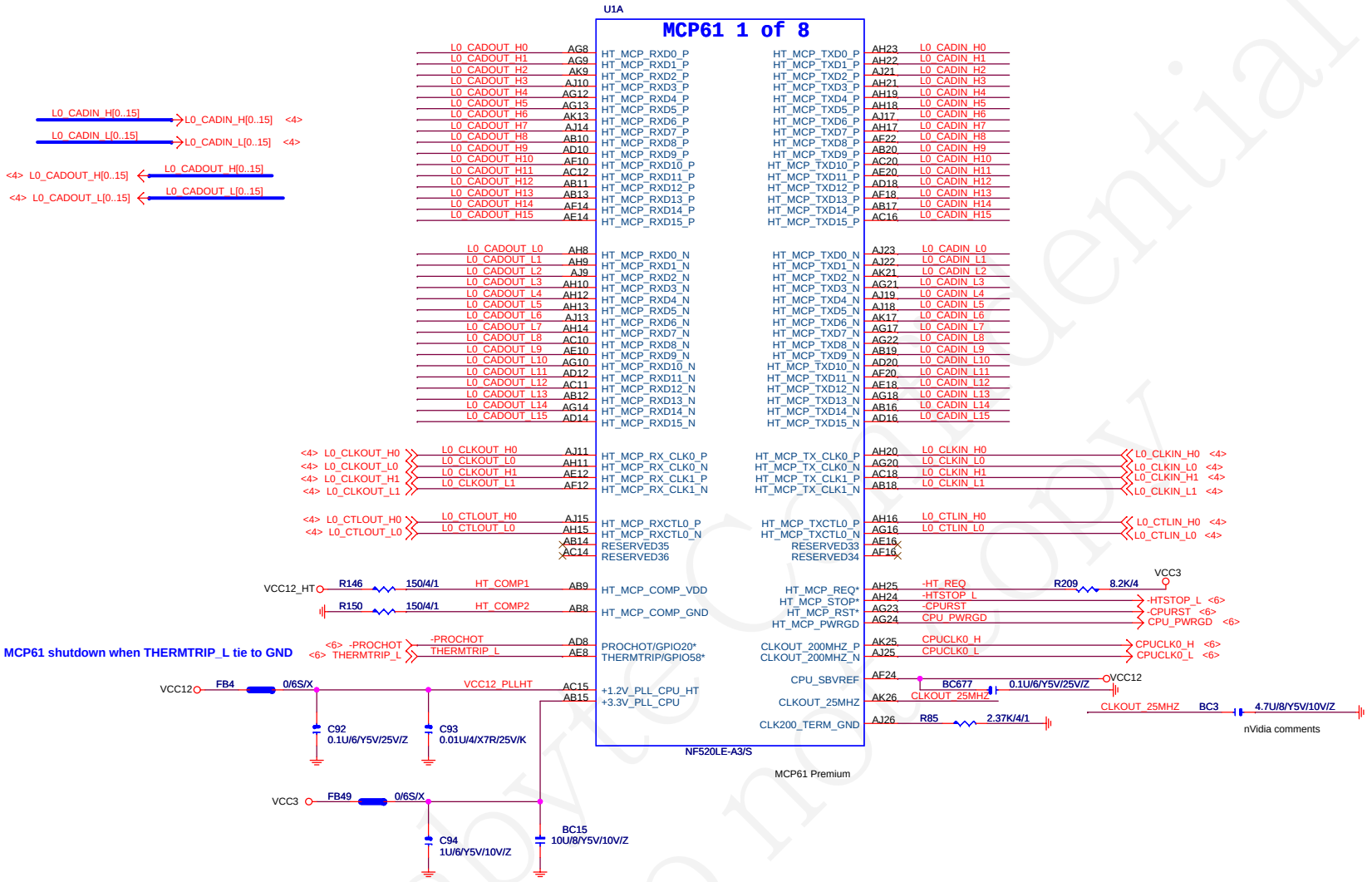
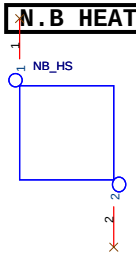
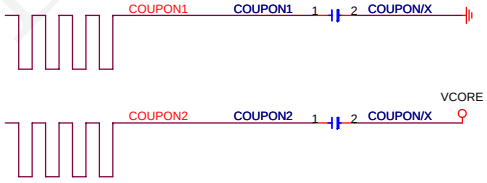




N.B HEATSINK



BGASINK_NB/[12SP2-01A002-51R_12SP2-01A002-52R_12SP2-01A002-53R]



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Title	MCP61D-HOST	
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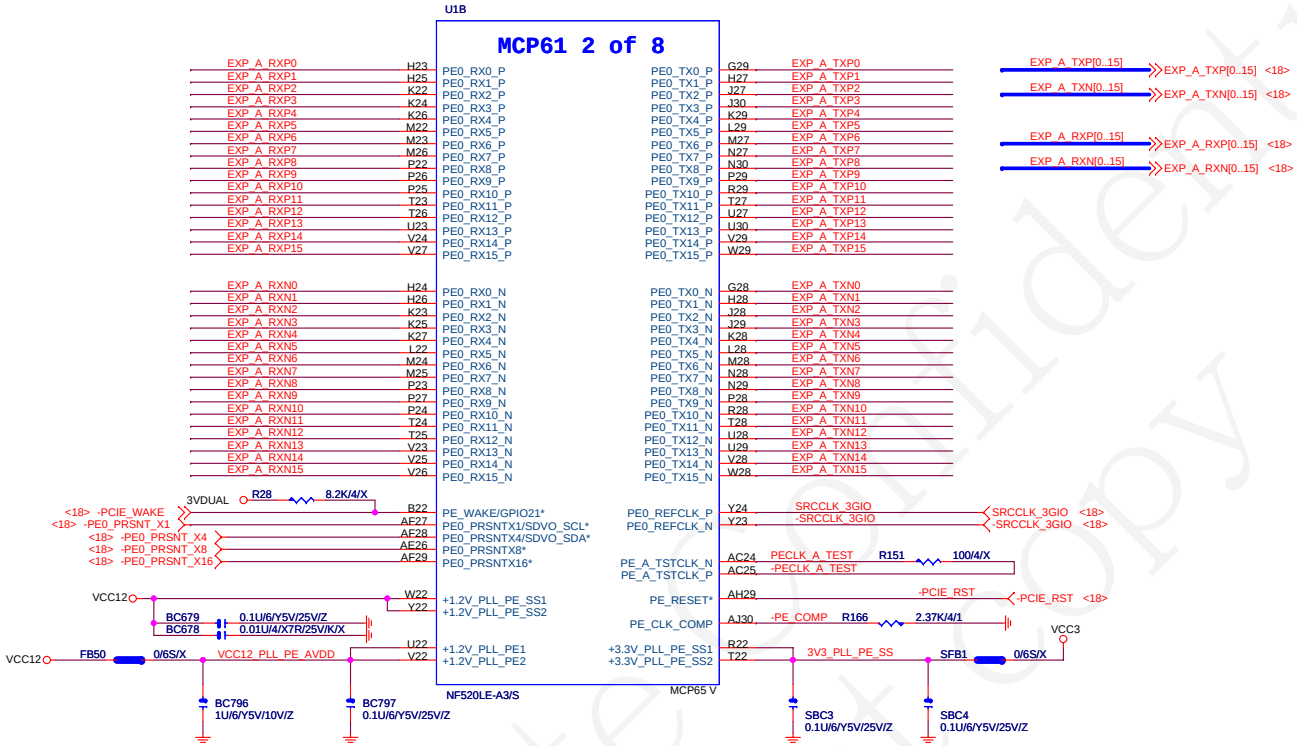

GIGABYTE		
Title: MCP61D-PCI_E		
Size: Custom	Document Number: GA-M52L-S3	Rev: 1.0
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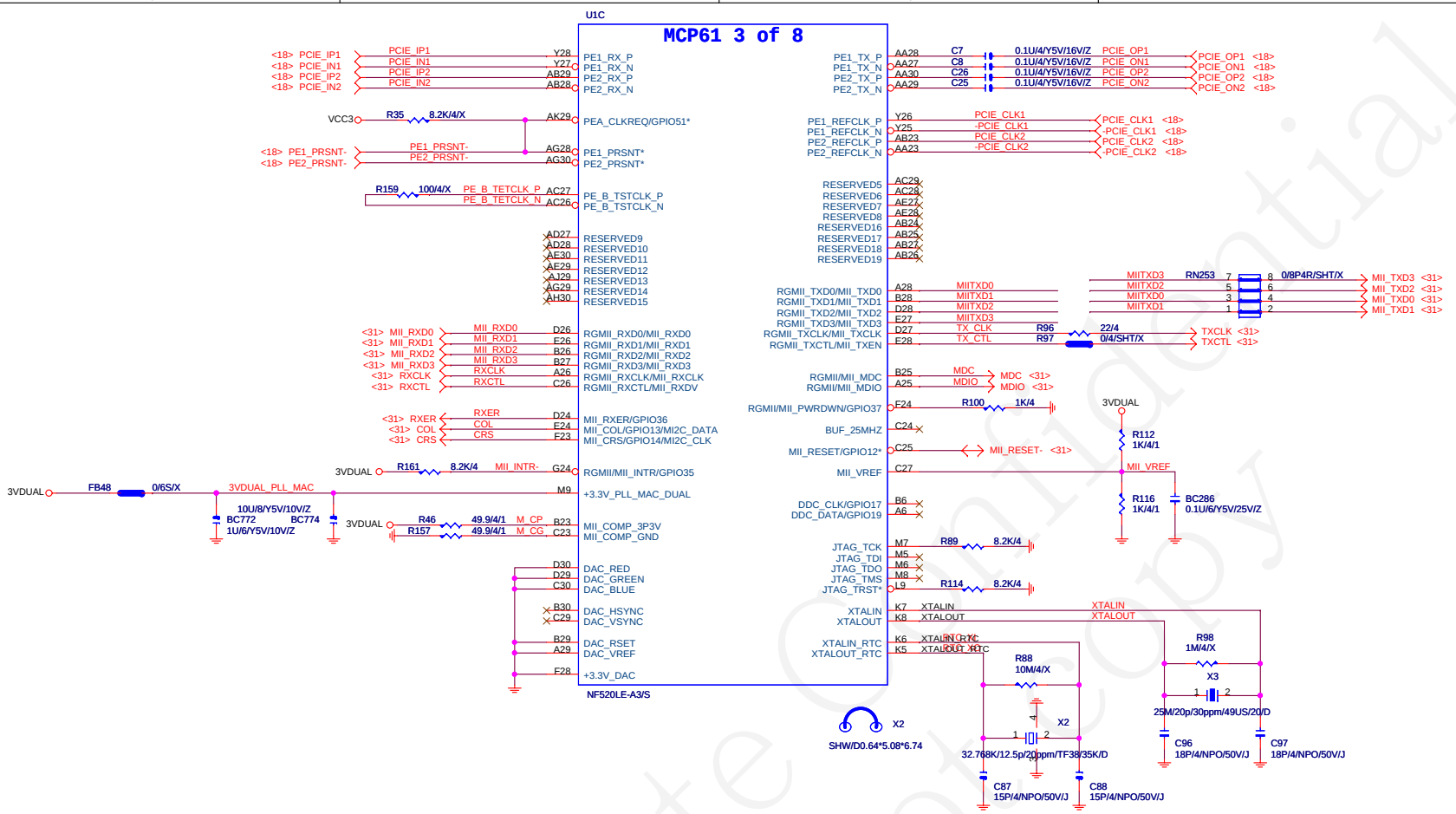

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Title	MCP61D-DAC, RGMII	
Size: Custom	Document Number: GA-M52L-S3	Rev: 1.0
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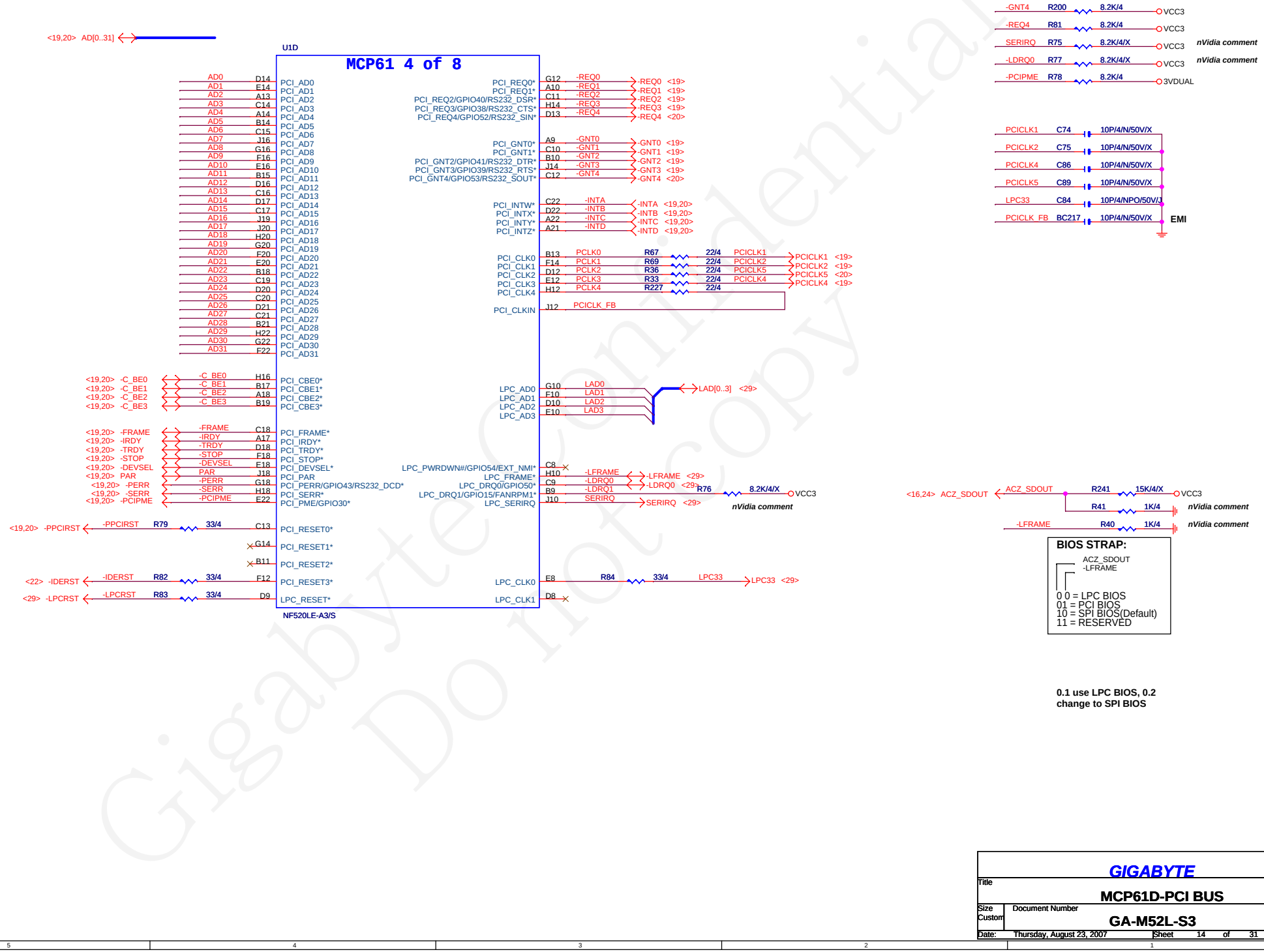

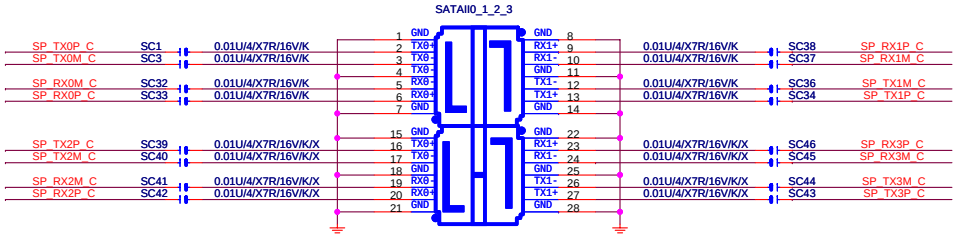

SATA2/7/YL/H/P/VA/D/2/B/GBT=>2 SATA PORT
770-44-28SY00 =>4 SATA PORT

U1E

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SATA_A0_TX_P / SATA_A0_TX_N — SP_TX0P_C (V2), SP_TX0M_C (V1)
SATA_A0_RX_N / SATA_A0_RX_P — SP_RX0M_C (W3), SP_RX0P_C (W2)
SATA_A1_TX_P / SATA_A1_TX_N — SP_TX1P_C (Y8), SP_TX1M_C (Y7)
SATA_A1_RX_N / SATA_A1_RX_P — SP_RX1M_C (Y5), SP_RX1P_C (Y6)
SATA_B0_TX_P / SATA_B0_TX_N — SP_TX2P_C (Y4), SP_TX2M_C (Y3)
SATA_B0_RX_N / SATA_B0_RX_P — SP_RX2M_C (AA4), SP_RX2P_C (AA3)
SATA_B1_TX_P / SATA_B1_TX_N — SP_TX3P_C (AA2), SP_TX3M_C (AA1)
SATA_B1_RX_N / SATA_B1_RX_P — SP_RX3M_C (AB1), SP_RX3P_C (AB2)

SATA B port is NC for MCP61D

RESERVED20 (AC3), RESERVED21 (AC2), RESERVED23 (AD4), RESERVED22 (AD3), RESERVED24 (AE4), RESERVED25 (AE3), RESERVED27 (AE1), RESERVED26 (AE2)

IDE_DATA_P0 (AJ3) PDD0
IDE_DATA_P1 (AJ2) PDD1
IDE_DATA_P2 (AH3) PDD2
IDE_DATA_P3 (AH1) PDD3
IDE_DATA_P4 (AG2) PDD4
IDE_DATA_P5 (AF2) PDD5
IDE_DATA_P6 (AF4) PDD6
IDE_DATA_P7 (AE6) PDD7
IDE_DATA_P8 (AE5) PDD8
IDE_DATA_P9 (AF5) PDD9
IDE_DATA_P10 (AF3) PDD10
IDE_DATA_P11 (AG1) PDD11
IDE_DATA_P12 (AG3) PDD12
IDE_DATA_P13 (AH2) PDD13
IDE_DATA_P14 (AJ1) PDD14
IDE_DATA_P15 (AK2) PDD15

PDD[0..15] ↔ PDD[0..15] <22>

IDE_ADDR_P0 (AG6) PDA0
IDE_ADDR_P1 (AJ5) PDA1
IDE_ADDR_P2 (AH6) PDA2

PDA[0..2] ↔ PDA[0..2] <22>

IDE_CS1_P* (AK6) -PCS1 ↔ -PCS1 <22>
IDE_CS3_P* (AJ6) -PCS3 ↔ -PCS3 <22>
IDE_DACK_P* (AG5) -PDDACK ↔ -PDDACK <22>
IDE_IOW_P* (AH4) -PDIOW ↔ -PDIOW <22>
IDE_INTR_P (AH5) IRQ14 ↔ IRQ14 <22>
IDE_DREQ_P (AK3) PDDREQ ↔ PDDREQ <22>
IDE_IOR_P* (AJ4) -PDIOR ↔ -PDIOR <22>
IDE_RDY_P (AK4) PIORDY ↔ PIORDY <22>
CABLE_DET_P/GPIO63 (AF6) P66DET ↔ P66DET <22>

IDE_COMP_3P3 (AD5) — IDE_COMP_3P3V — R50 121/4/1 — VCC3
IDE_COMP_GND (AD6) — IDE_COMP_GND — R51 121/4/1

SATA_LED/GPIO57* (A5) -SATA_LED ↔ -SATA_LED <26>

SATA_TSTCLK_P (AA6) SPTSTCLK — R242 100/4/X
SATA_TSTCLK_N (AB6) -SPTSTCLK
nVidia comment

SATA_TERMP (AB5) — SP_TERMP — R253 2.49K/4/1

Y9 +1.2V_PLL_SP_VDD
U13 +1.2V_PLL_SP_SS
U12 +3.3V_PLL_SP_SS
V12 +3.3V_PLL_LEG
M12 +3.3V_PLL_DISP

NF520LE-A3/S

VCC12 — FB41 0/6S/X — VCC12_PLL_SP_VDD
10U/8/Y5V/10V/Z
BC686
BC685 0.1U/6/Y5V/25V/Z
VCC12 — BC680 0.1U/6/Y5V/25V/Z

VCC3 — FB10 0/6S/X — VCC3_PLL_SP_SS
BC321 0.01U/4/X7R/25V/K/X
BC322 0.1U/6/Y5V/25V/Z
BC323 0.1U/6/Y5V/25V/Z

VCC3_PLL_SP_SS
SBC1 0.1U/4/Y5V/16V/Z/X
SBC2 0.1U/4/Y5V/16V/Z

PCI LOADING

VCC3
EC1 1000U/D/6.3V/8C/30m

GIGABYTE		
Title	MCP61D-SATA IDE	
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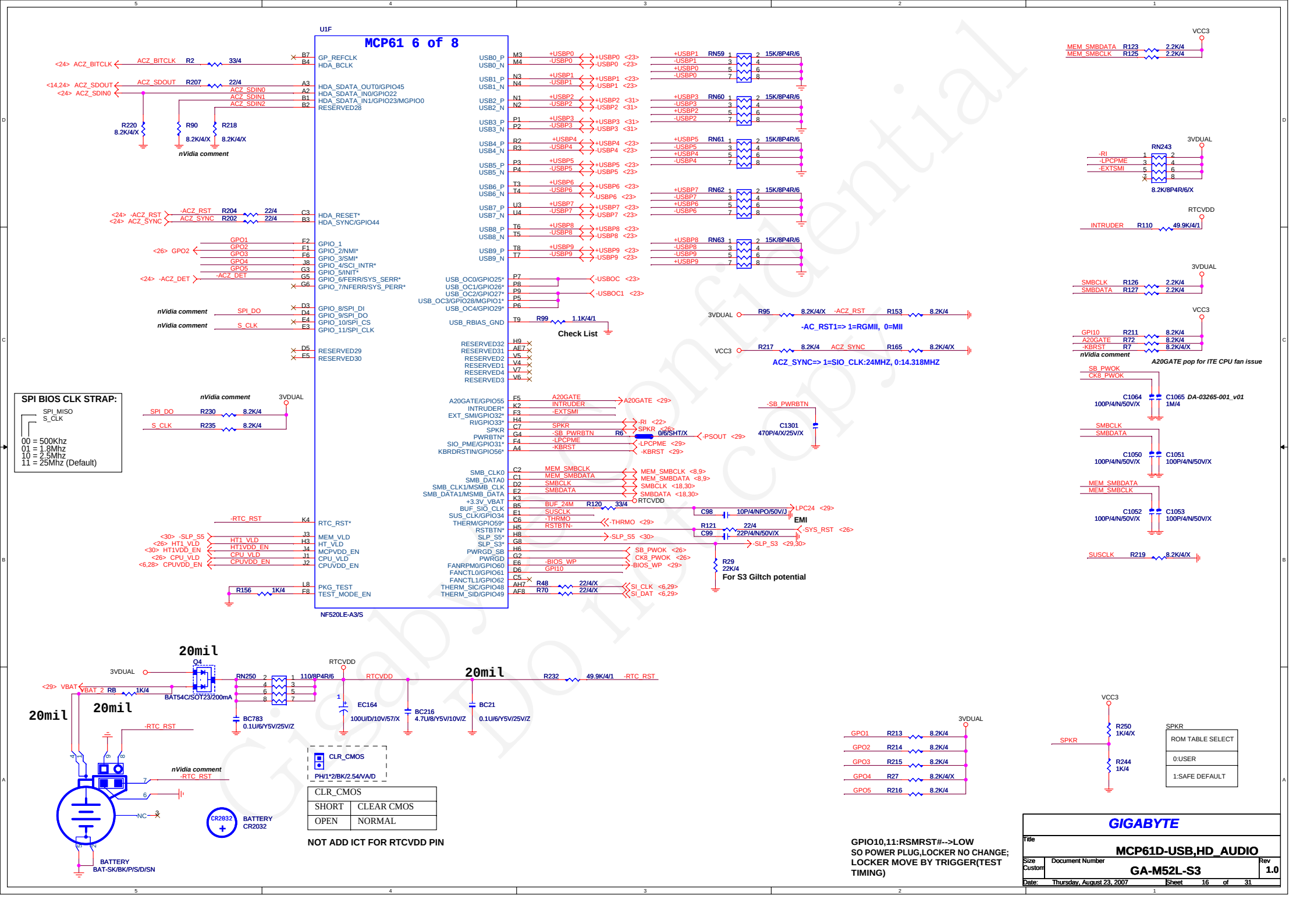
U1F
MCP61 6 of 8
NF520LE-A3/S
SPI BIOS CLK STRAP:
SPI_MISO
S_CLK
00 = 500Khz
01 = 1.8Mhz
10 = 2.5Mhz
11 = 25Mhz (Default)
Check List
-AC_RST1=> 1=RGMII, 0=MII
ACZ_SYNC=> 1=SIO_CLK:24MHZ, 0:14.318MHZ
A20GATE pop for ITE CPU fan issue
For S3 Giltch potential
EMI
20mil
BATTERY
BAT-SK/BK/P/S/D/SN
CR2032
BATTERY
CR2032
CLR_CMOS
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT
CLEAR CMOS
OPEN
NORMAL
NOT ADD ICT FOR RTCVDD PIN
GPIO10,11:RSMRST#-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST
TIMING)
SPKR
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
GIGABYTE
MCP61D-USB,HD_AUDIO
GA-M52L-S3
1.0
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DA-03265-001_v01
Gigabyte Confidential
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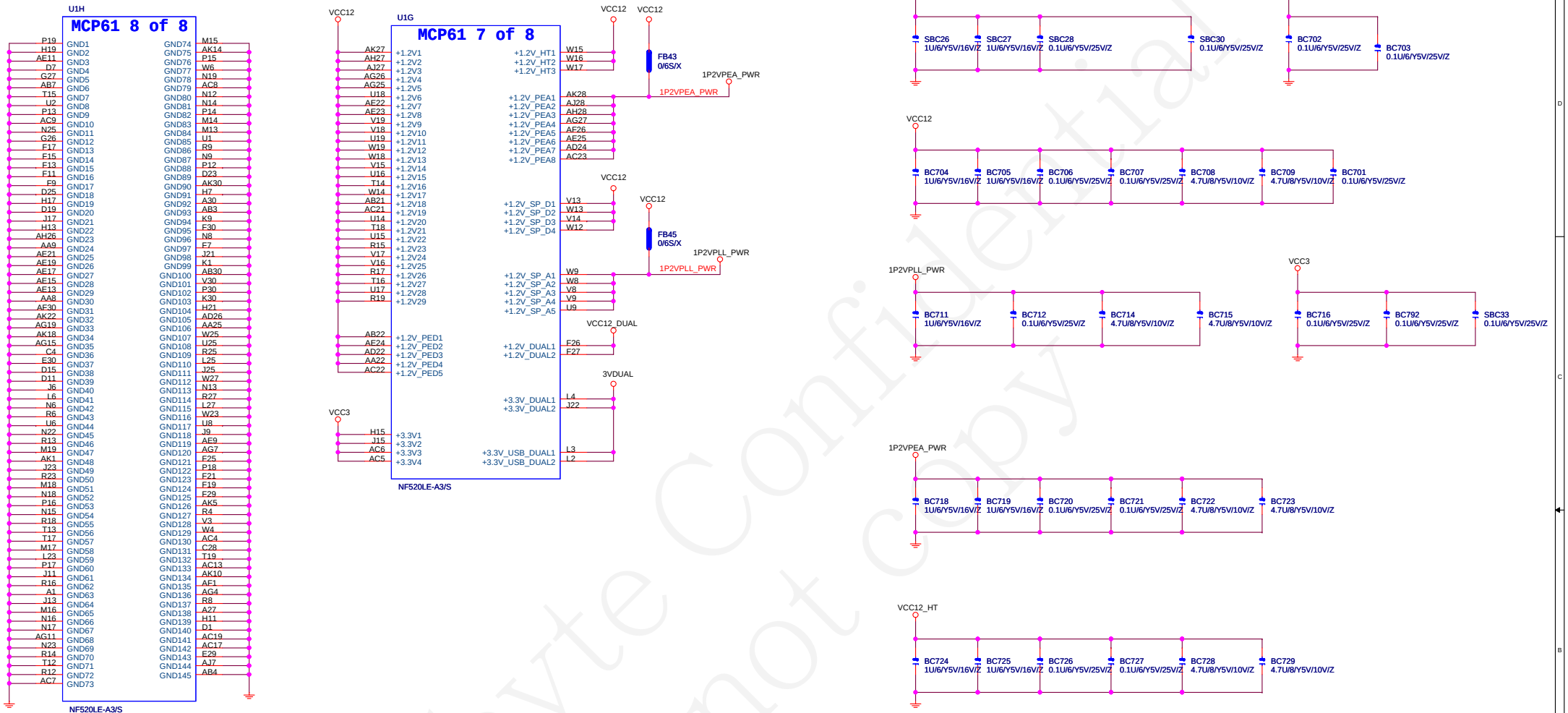

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Title	MCP61D-PWR,GND	
Size: Custom	Document Number: GA-M52L-S3	Rev: 1.0
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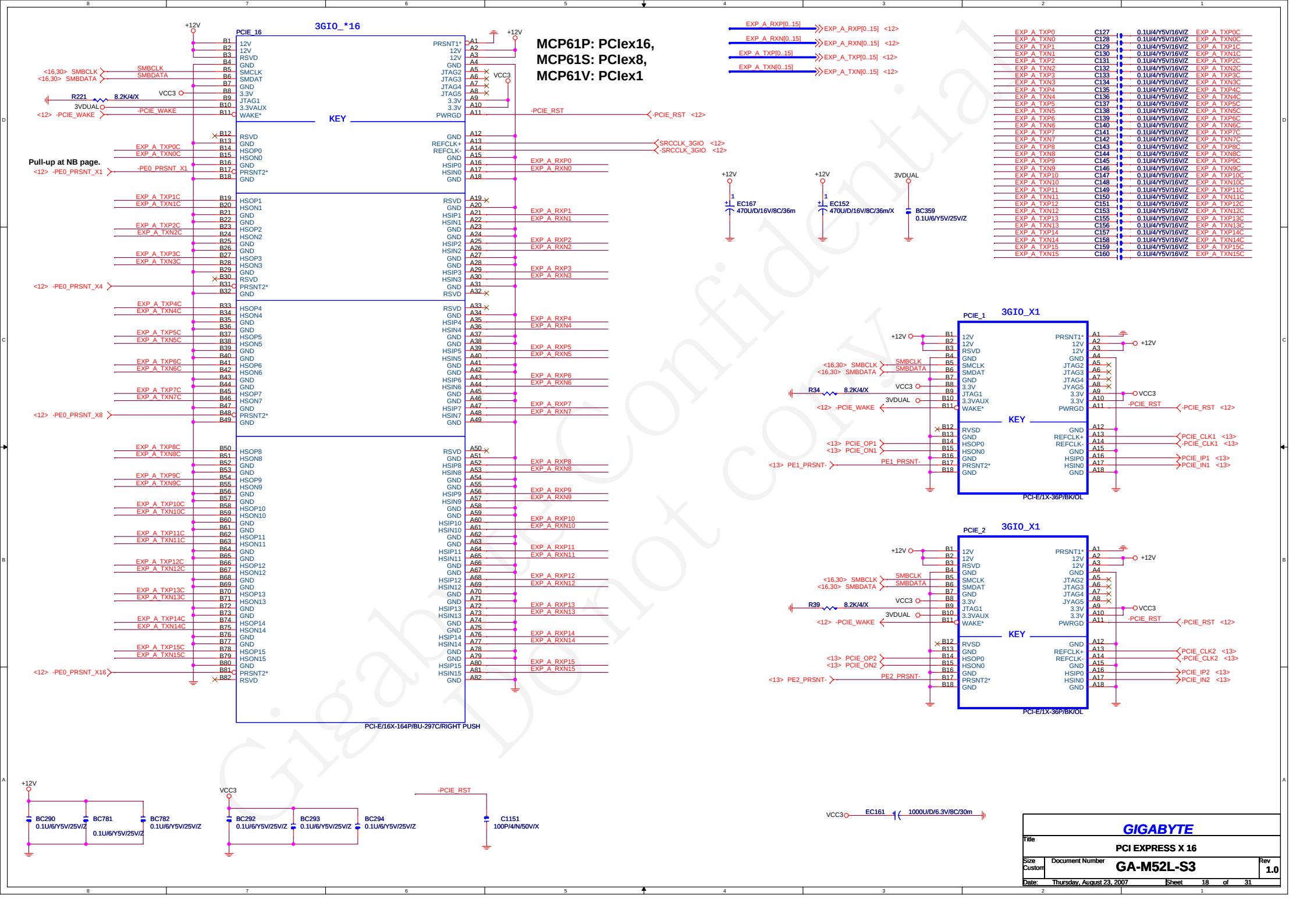
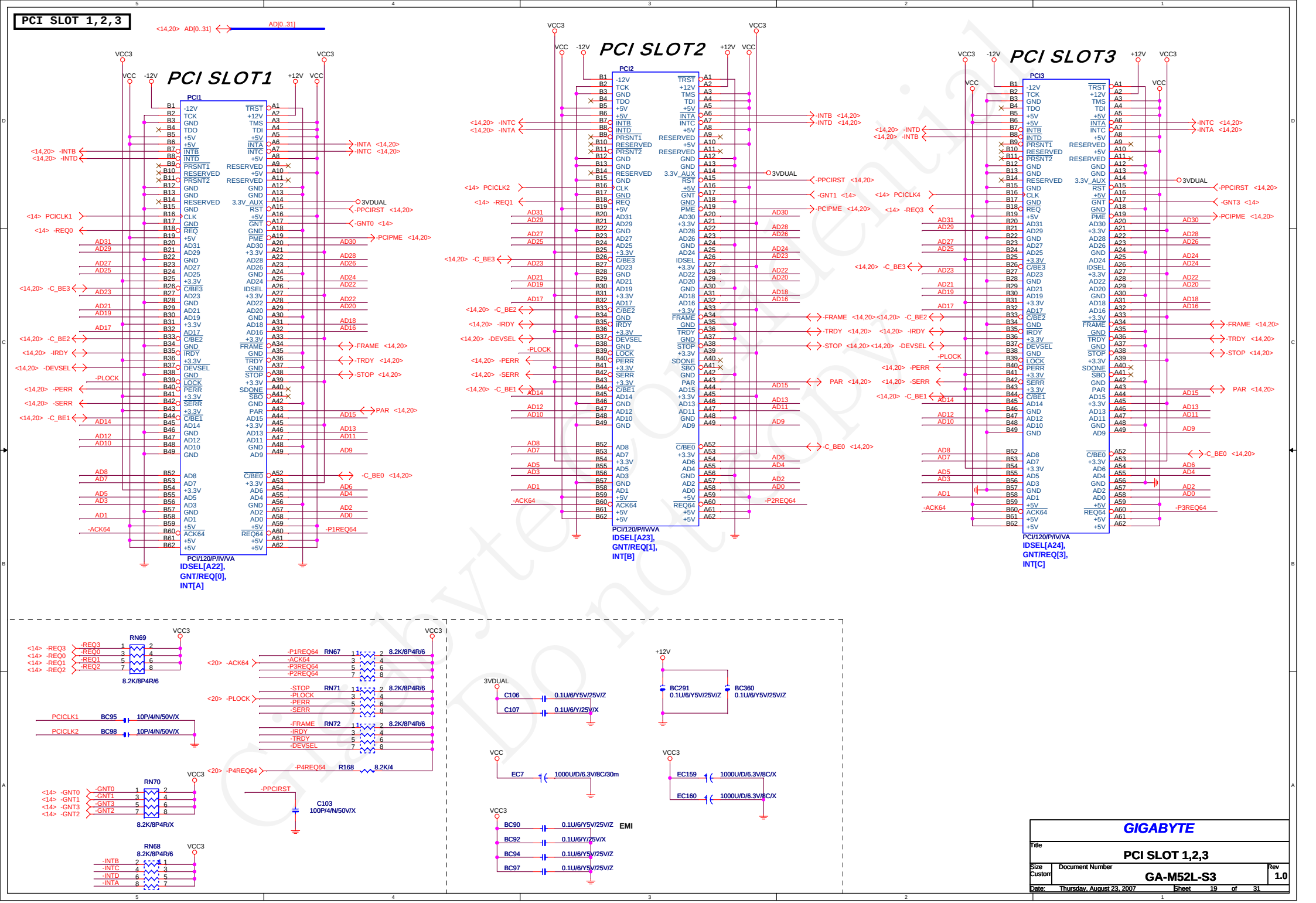


PCI SLOT 1,2,3



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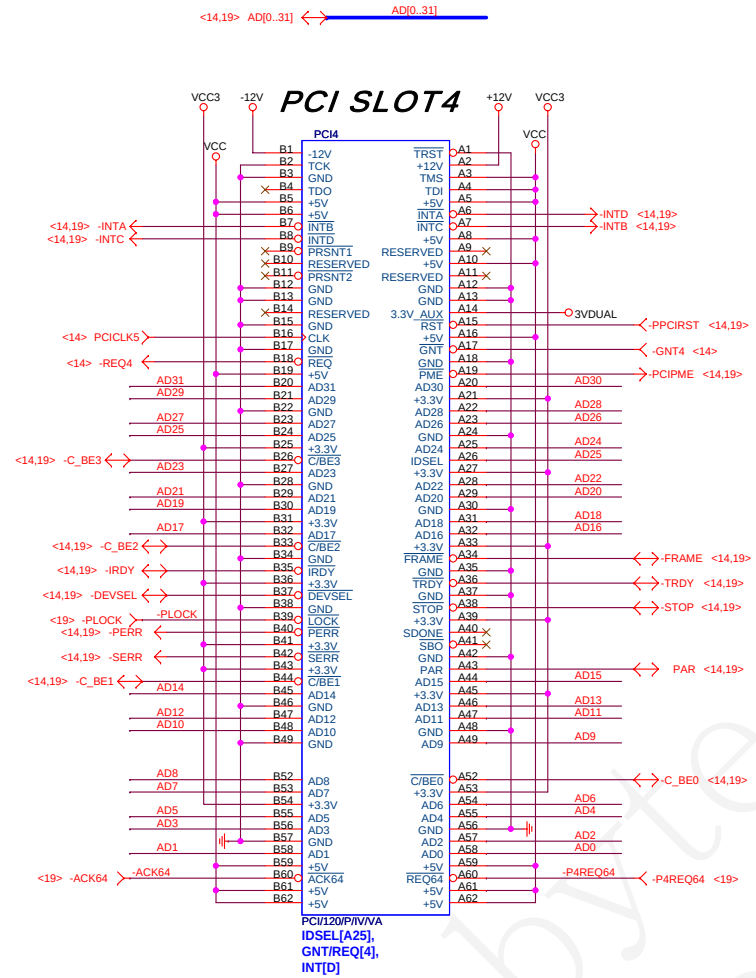

GIGABYTE		
Title: PCI SLOT 4		
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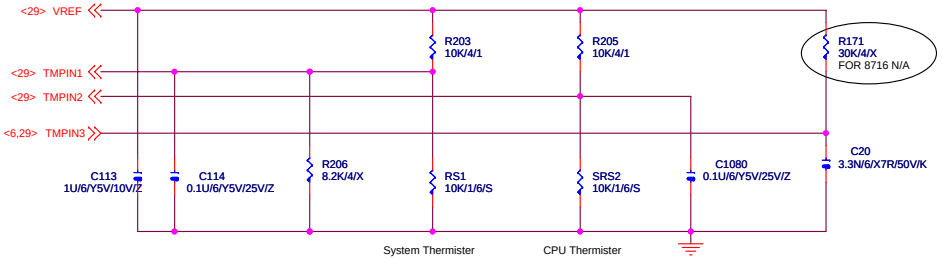
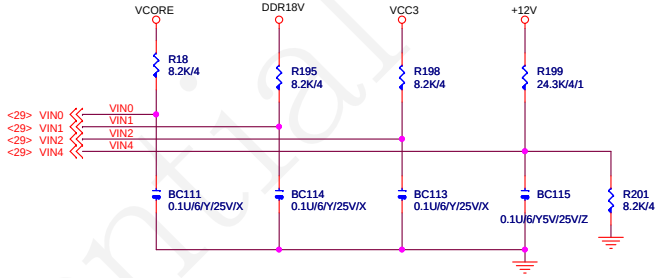
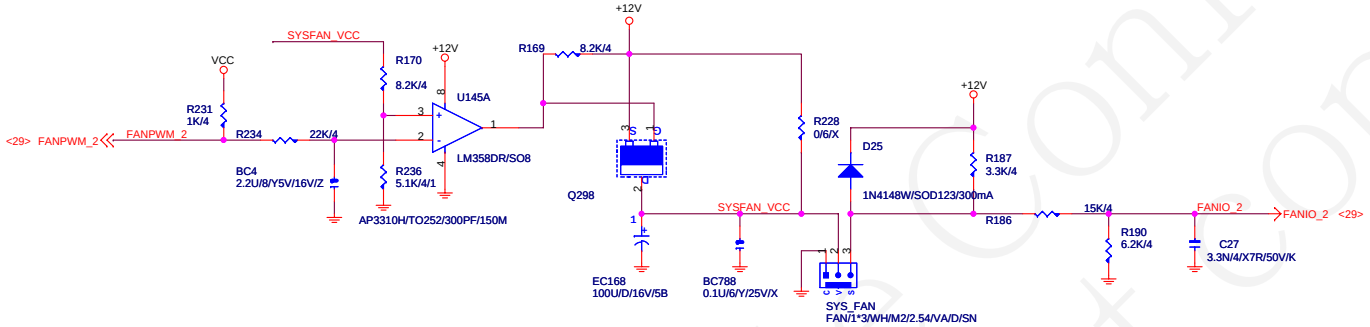
Hardware Monitor circuits

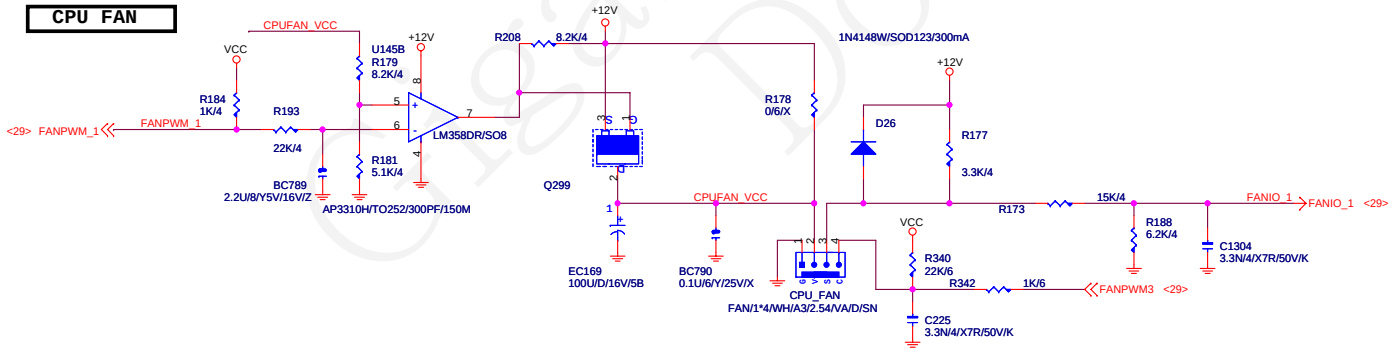




SYSTEM FAN



CPU FAN



GIGABYTE

Title	FAN/HWMO
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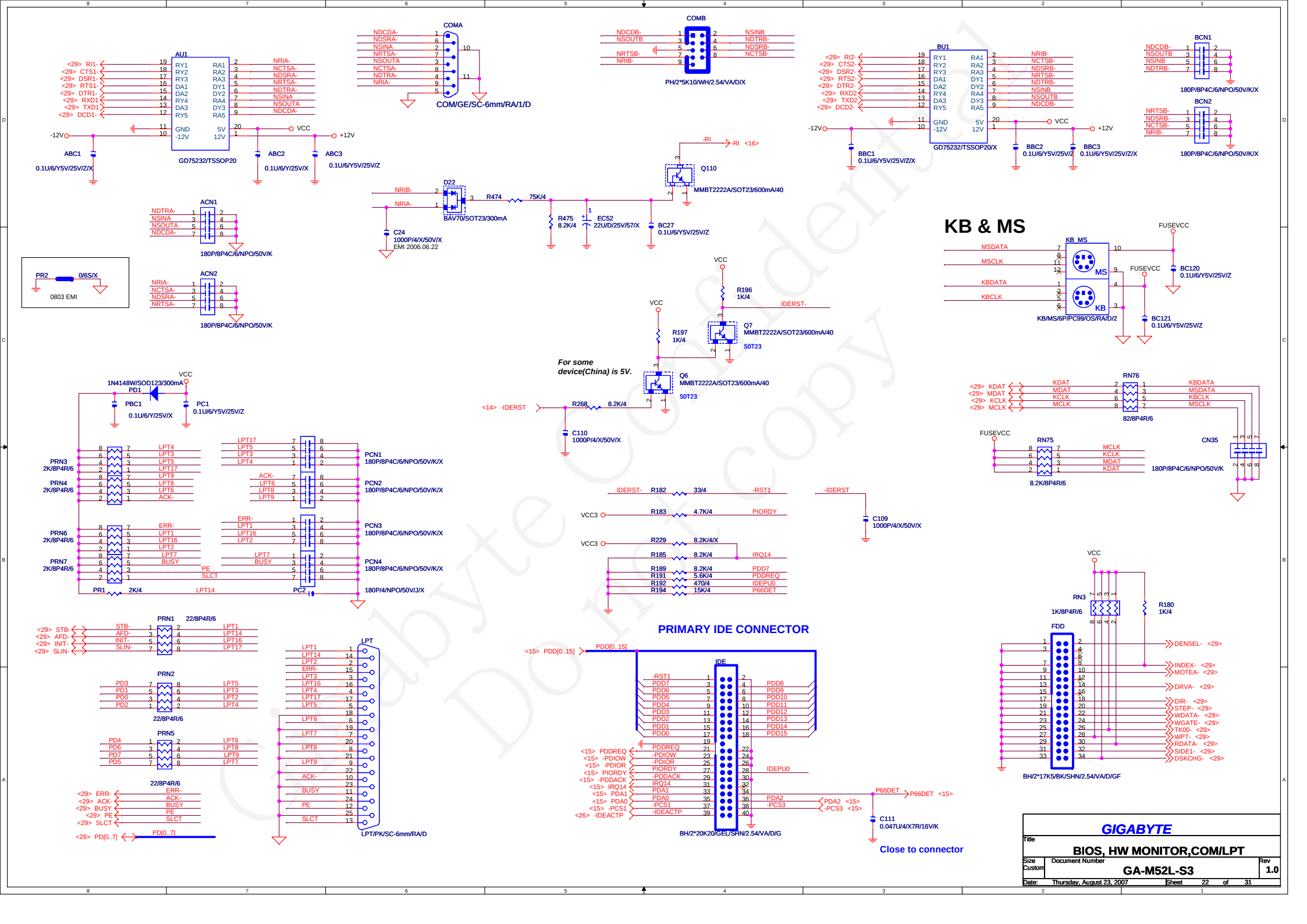

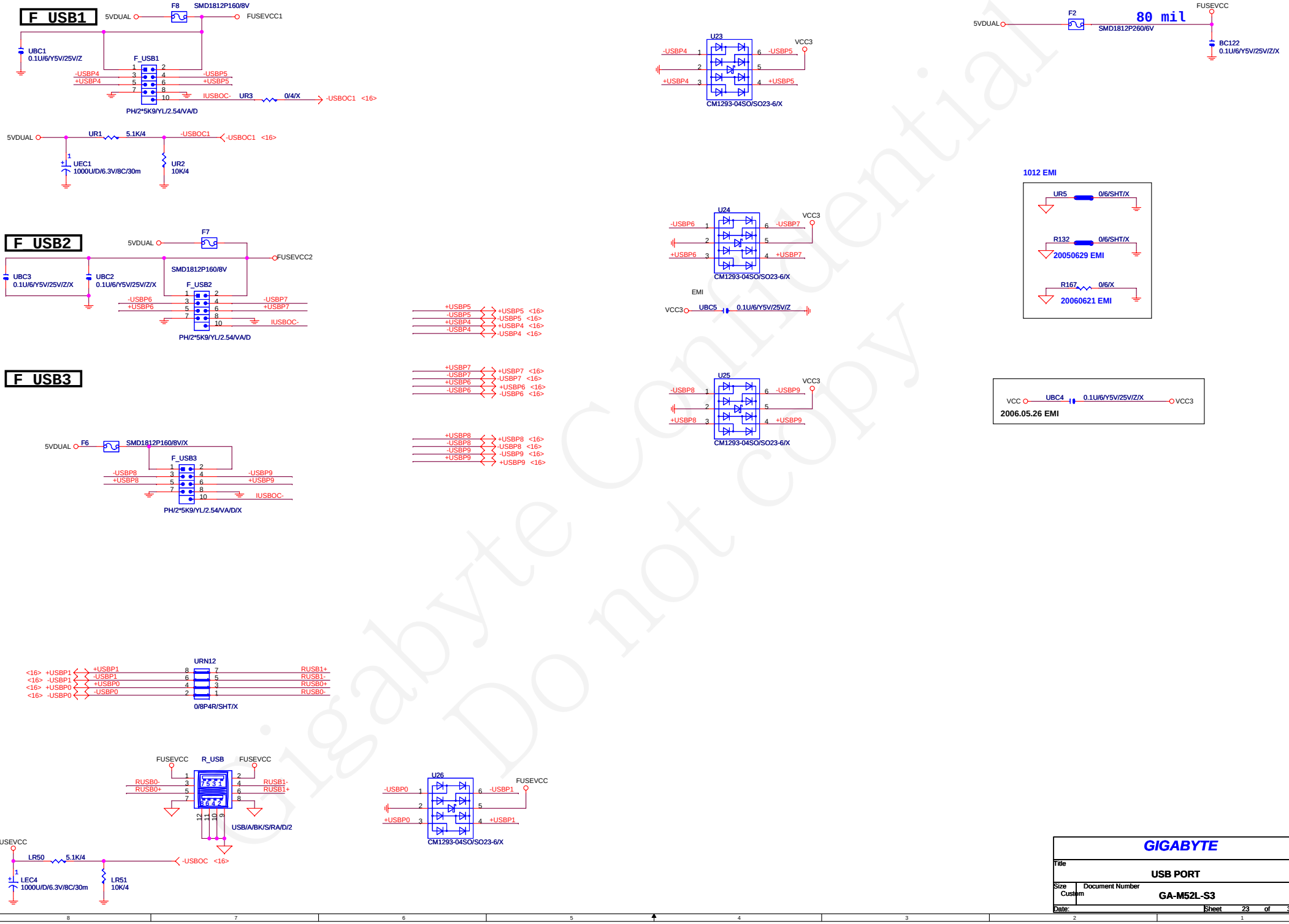

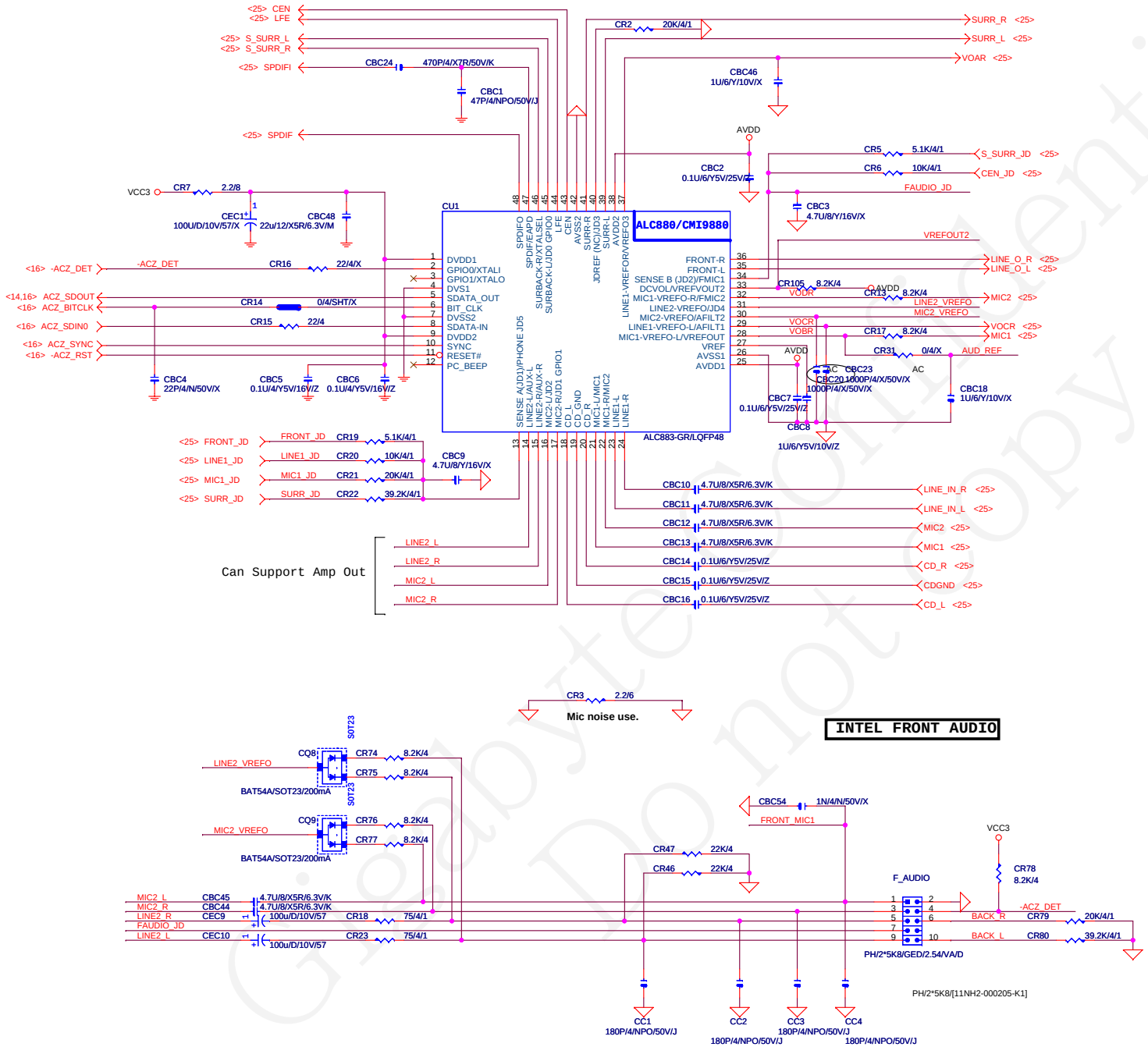

GIGABYTE			
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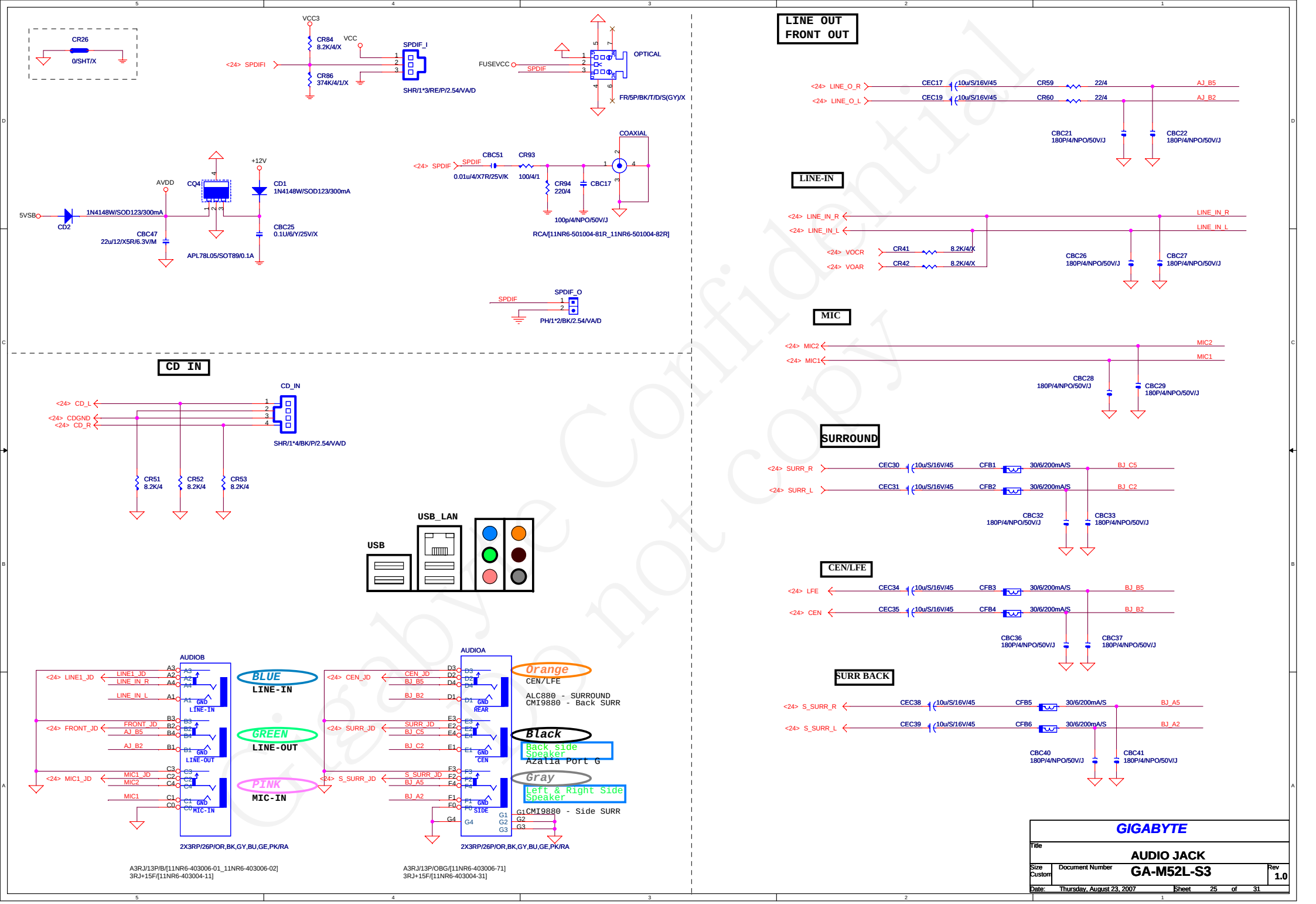

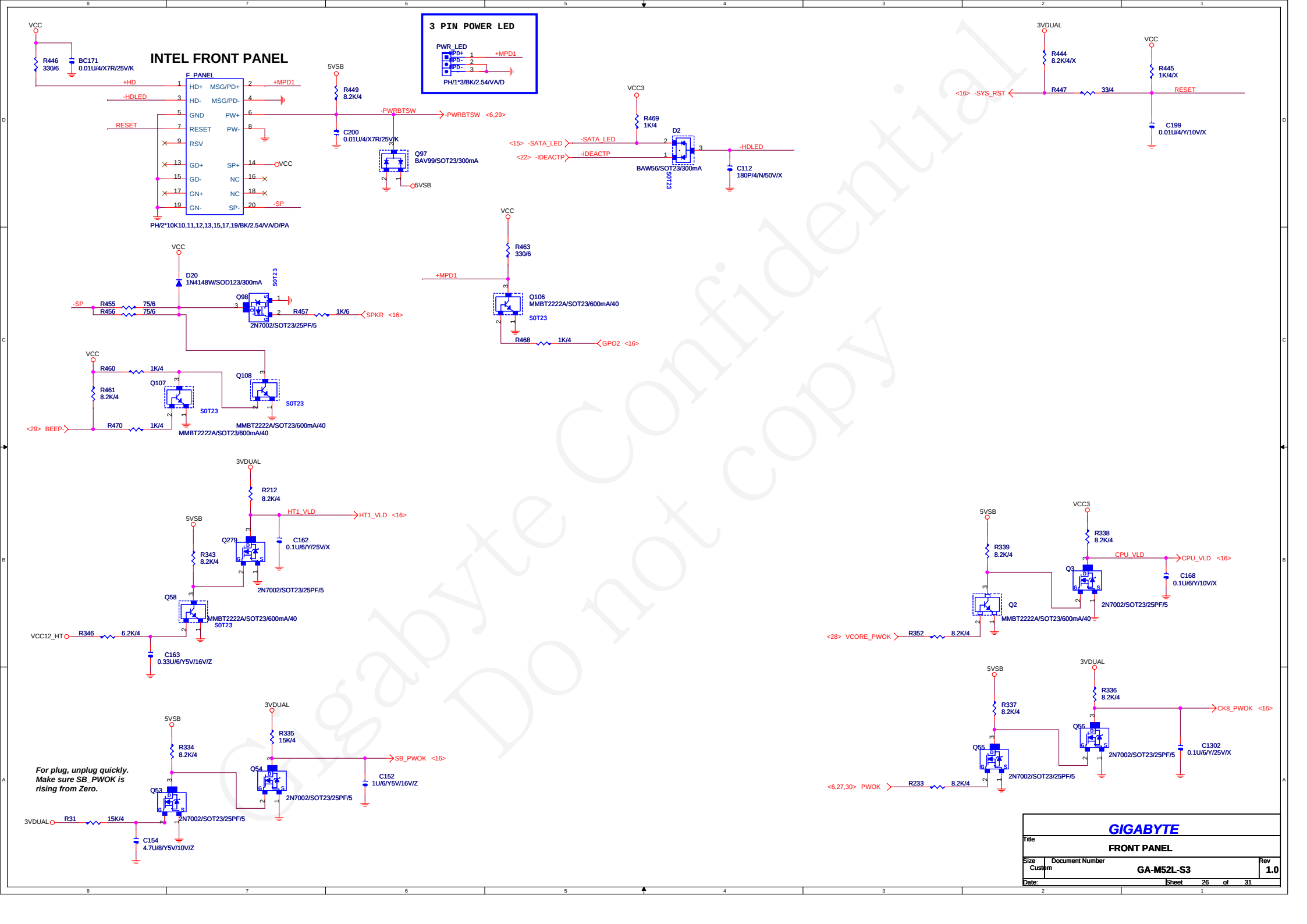
INTEL FRONT PANEL
3 PIN POWER LED
PWR_LED
PH/1*3/BK/2.54/VA/D
F_PANEL
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D/PA
HD+ MSG/PD+
HD- MSG/PD-
GND PW+
RESET PW-
RSV
GD+ SP+
GD- NC
GN+ NC
GN- SP-
+HD
-HDLED
RESET
+MPD1
VCC
-SP
R446 330/6
BC171 0.01U/4/X7R/25V/K
R449 8.2K/4
C200 0.01U/4/X7R/25V/K
Q97 BAV99/SOT23/300mA
-PWRBTSW
-PWRBTSW <6,29>
5VSB
R469 1K/4
D2
BAW56/SOT23/300mA
C112 180P/4/N/50V/X
-SATA_LED
-IDEACTP
<15> -SATA_LED
<22> -IDEACTP
-HDLED
VCC3
R444 8.2K/4/X
R445 1K/4/X
R447 33/4
C199 0.01U/4/Y/10V/X
<16> -SYS_RST
RESET
3VDUAL
D20 1N4148W/SOD123/300mA
Q98 2N7002/SOT23/25PF/5
R455 75/6
R456 75/6
R457 1K/6
SPKR <16>
R463 330/6
Q106 MMBT2222A/SOT23/600mA/40
R468 1K/4
GPO2 <16>
R460 1K/4
R461 8.2K/4
R470 1K/4
Q107
Q108
MMBT2222A/SOT23/600mA/40
<29> BEEP-
R212 8.2K/4
HT1_VLD
HT1_VLD <16>
Q279 2N7002/SOT23/25PF/5
C162 0.1U/6/Y/25V/X
R343 8.2K/4
Q58 MMBT2222A/SOT23/600mA/40
VCC12_HT
R346 6.2K/4
C163 0.33U/6/Y5V/16V/Z
R339 8.2K/4
R338 8.2K/4
CPU_VLD
CPU_VLD <16>
Q3 2N7002/SOT23/25PF/5
C168 0.1U/6/Y/10V/X
Q2 MMBT2222A/SOT23/600mA/40
<28> VCORE_PWOK
R352 8.2K/4
R334 8.2K/4
R335 15K/4
SB_PWOK
SB_PWOK <16>
Q54 2N7002/SOT23/25PF/5
C152 1U/6/Y5V/16V/Z
Q53 2N7002/SOT23/25PF/5
R31 15K/4
C154 4.7U/8/Y5V/10V/Z
For plug, unplug quickly.
Make sure SB_PWOK is
rising from Zero.
R337 8.2K/4
R336 8.2K/4
CK8_PWOK
CK8_PWOK <16>
Q56 2N7002/SOT23/25PF/5
C1302 0.1U/6/Y/25V/X
Q55 2N7002/SOT23/25PF/5
<6,27,30> PWOK
R233 8.2K/4
GIGABYTE
Title
FRONT PANEL
Size Custom
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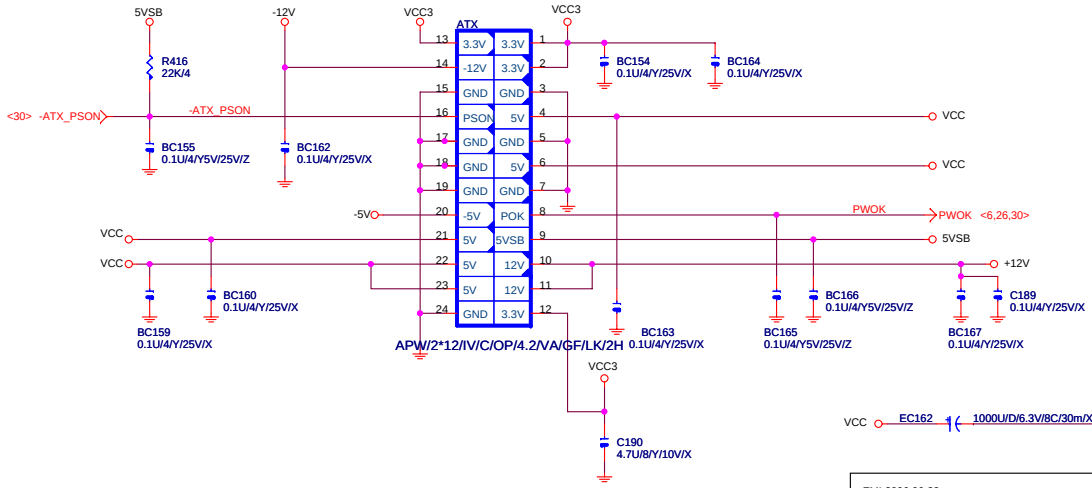
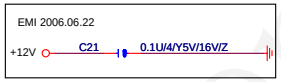
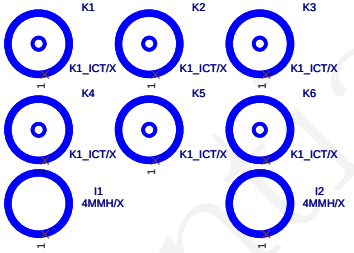
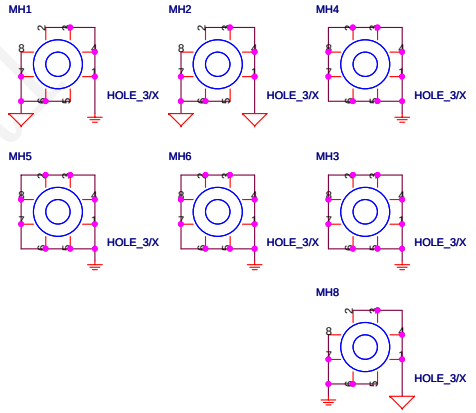
Do not copy

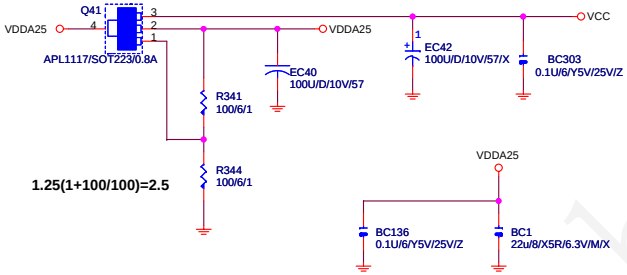
ATX POWER CONNECTOR

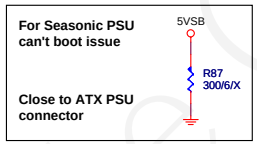


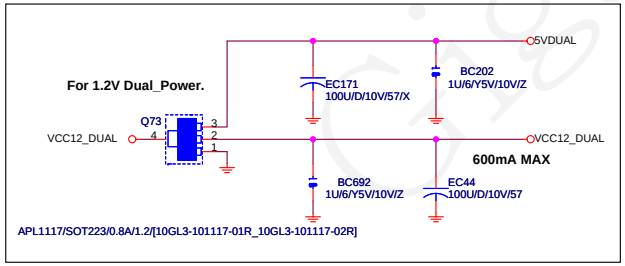


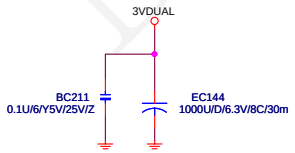












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Title	Misc. PWR & ATX CONN	
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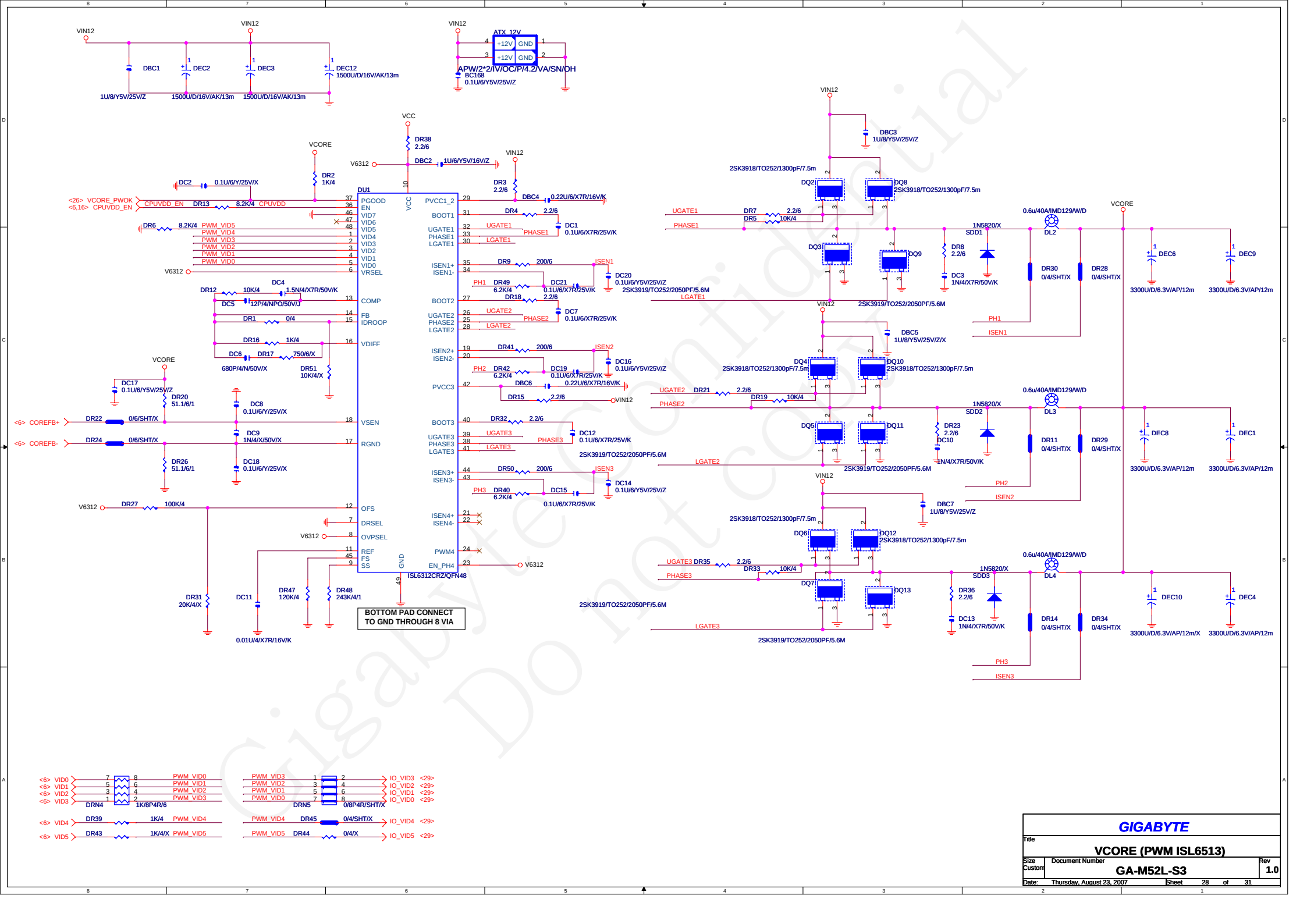

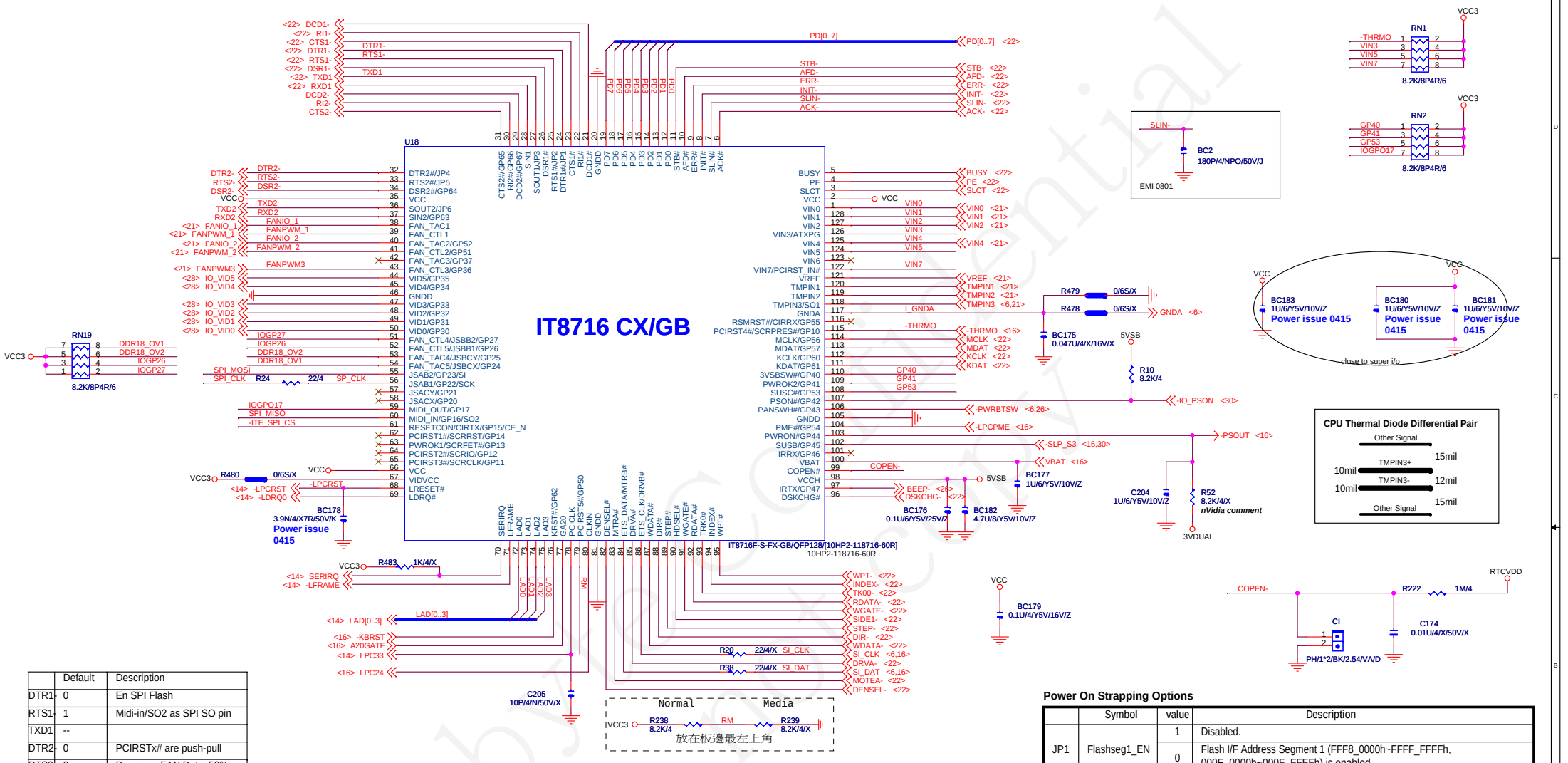

	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

IT8712 H/W Strap

ON: EN SPI

DTR1- R240 680/4

RTS1- R243 680/4/X VCC

TXD1 R245 680/4/X

R246 8.2K/4/X VCC

DTR2- R247 680/4

R248 8.2K/4/X VCC

RTS2- R249 680/4

TXD2 R251 680/4

75232 internal P.U.

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title	ITE 8712 LPC IO	
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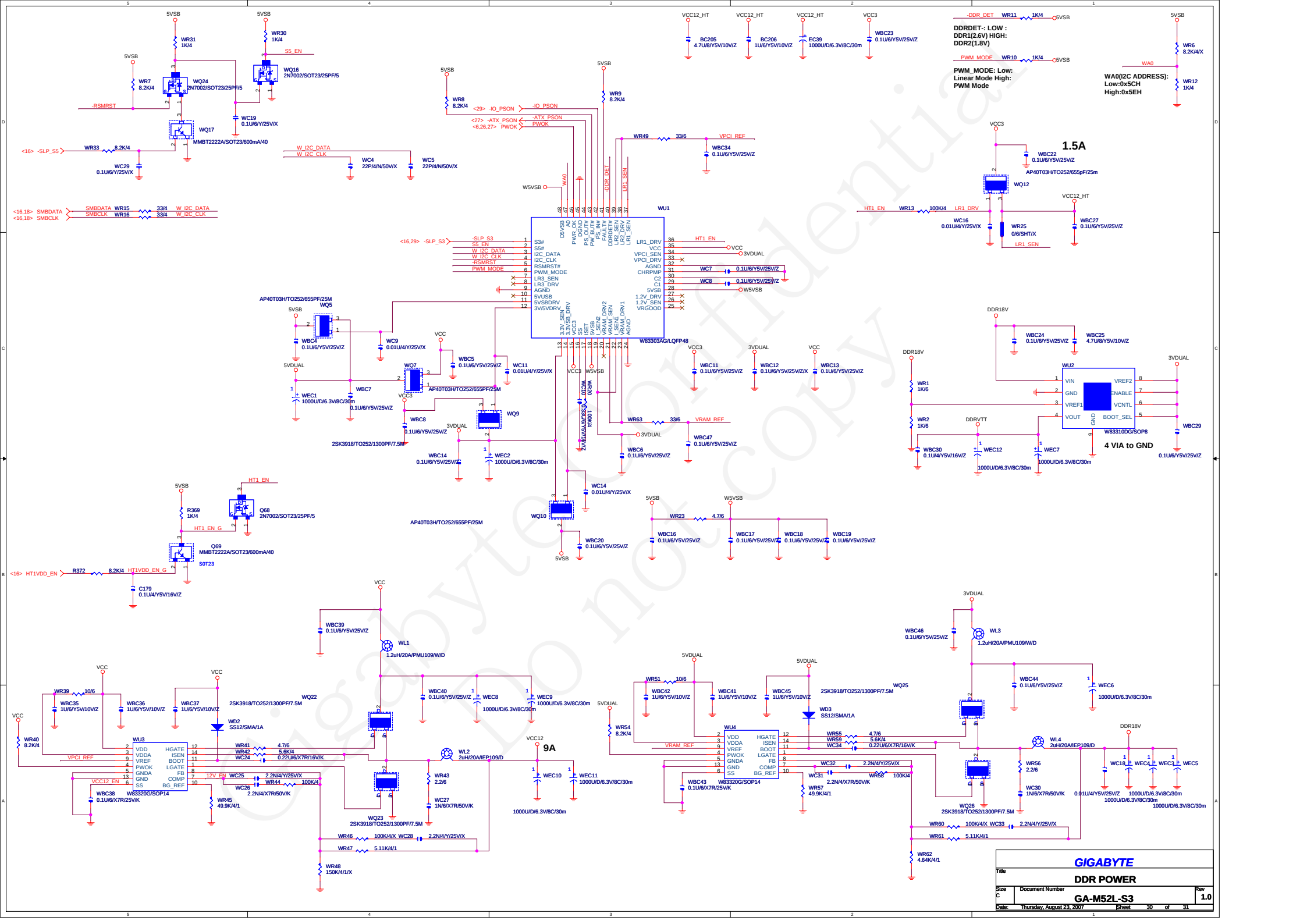
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
4 VIA to GND
W83303AG/LQFP48
W83310DG/SOP8
W83320G/SOP14
AP40T03H/TO252/655PF/25M
2SK3918/TO252/1300PF/7.5M
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25PF/5
SS12/SMA/1A
1.2uH/20A/PMU109/W/D
2uH/20A/IEP109/D
9A
GIGABYTE
DDR POWER
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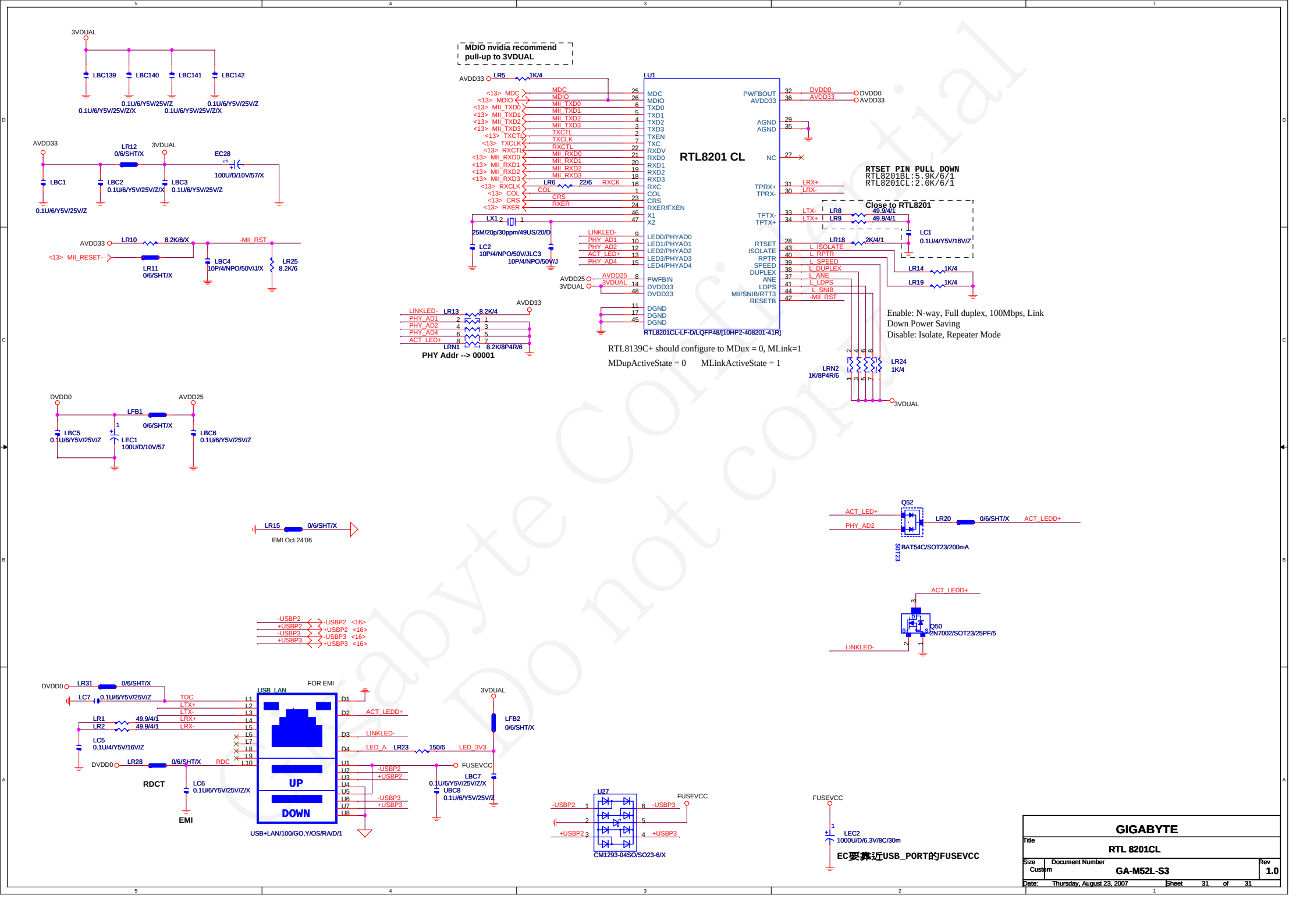

GIGABYTE		
Title: RTL 8201CL		
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