GA-M51GM-S2G

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38	TI TSB43AB23 1394a

Revision:1.2

GIGABYTE

Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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Model Name:GA-M51GM-S2G

Component value change history

Version: 1.2

P-Code: A94231-0

Date	Change Item	Reason
2006.02.23	0.1 New BOM Release.	
2006.03.20	0.2 BOM Release.	
2006.04.11	1.0A BOM Release.	
2006.04.25	1.0A BOM Release.	Modify from 9MM51GMS2R-00-10A
2006.05.02	1.0B BOM Release.	change CPU_FAN & SYS_FAN smart fan 分壓組值
2006.05.08	1.0B BOM Release.	Add second source
2006.06.07	1.1A BOM Release.	Modify DVI I2C PU ,74LVC08A change to SOIC
2006.06.12	1.2A BOM Release.	Modify VDDA25 & U12 LM358 cost down
2006.06.28	1.2A BOM Release.	轉 P-BOM
2006.09.07	1.2A BOM Release.	修 鵟]材

Circuit or PCB layout change for next version

Date	Change Item	Reason
2006.02.21	0.1 Gerber Out	
2006.03.17	0.2 Gerber Out	無] OSP 製程
2006.04.10	1.0 Gerber Out	
2006.04.24	1.0 Gerber Out	Modify from GA-M51GM-S2 1.0
2006.06.06	1.1 Gerber Out	Modify DVI I2C PU ,74LVC08A change to SOIC
2006.06.09	1.2 Gerber Out	Modify VDDA25 & U12 LM358 cost down

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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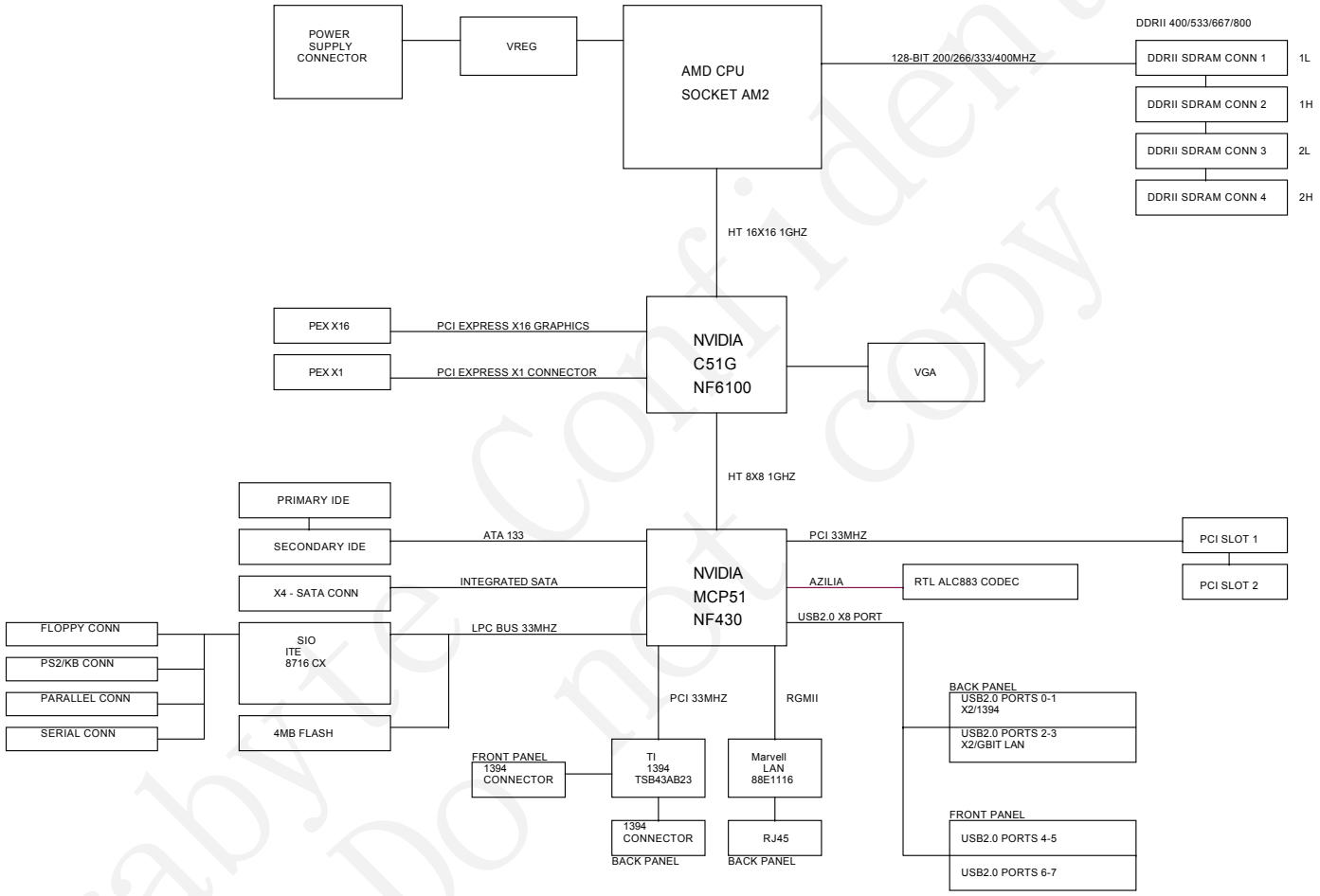
BLOCK DIAGRAM



GIGABYTE		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
Date: Thursday, September 07, 2006	Sheet 3 of 38	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] 11
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 11
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] 11
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] 11
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 11
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 11
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] 11
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] 11

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

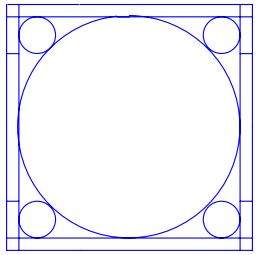
VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
VCC12_HT R3 49.9/4/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1 TP78
GND R4 49.9/4/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1 TP79
11 L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0 11
11 L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0 11
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

SOCKET_M2
M2/[12KRC-04K807-21R]



GIGABYTE

Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
Custom	GA-M51GM-S2G	1.2

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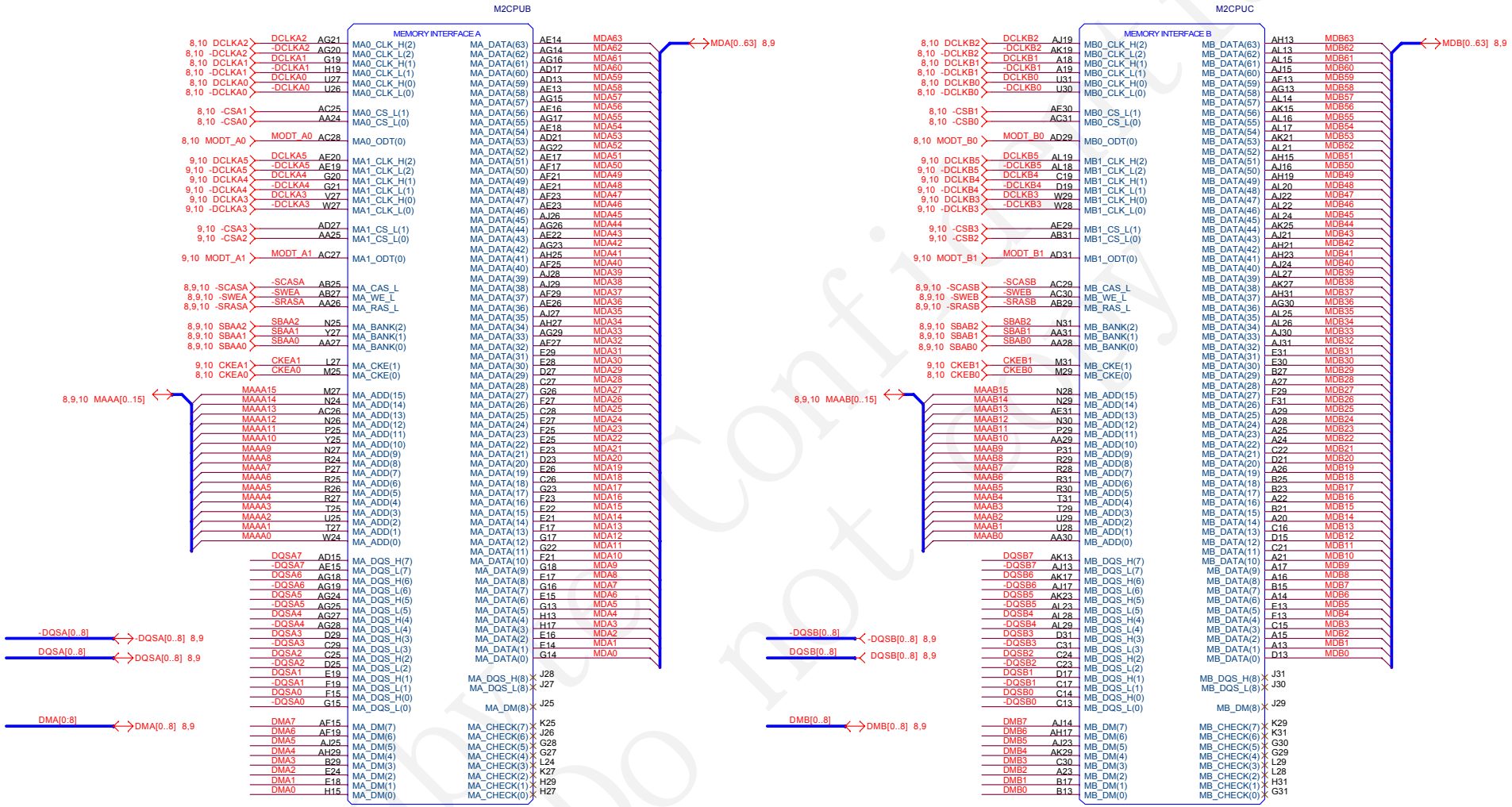
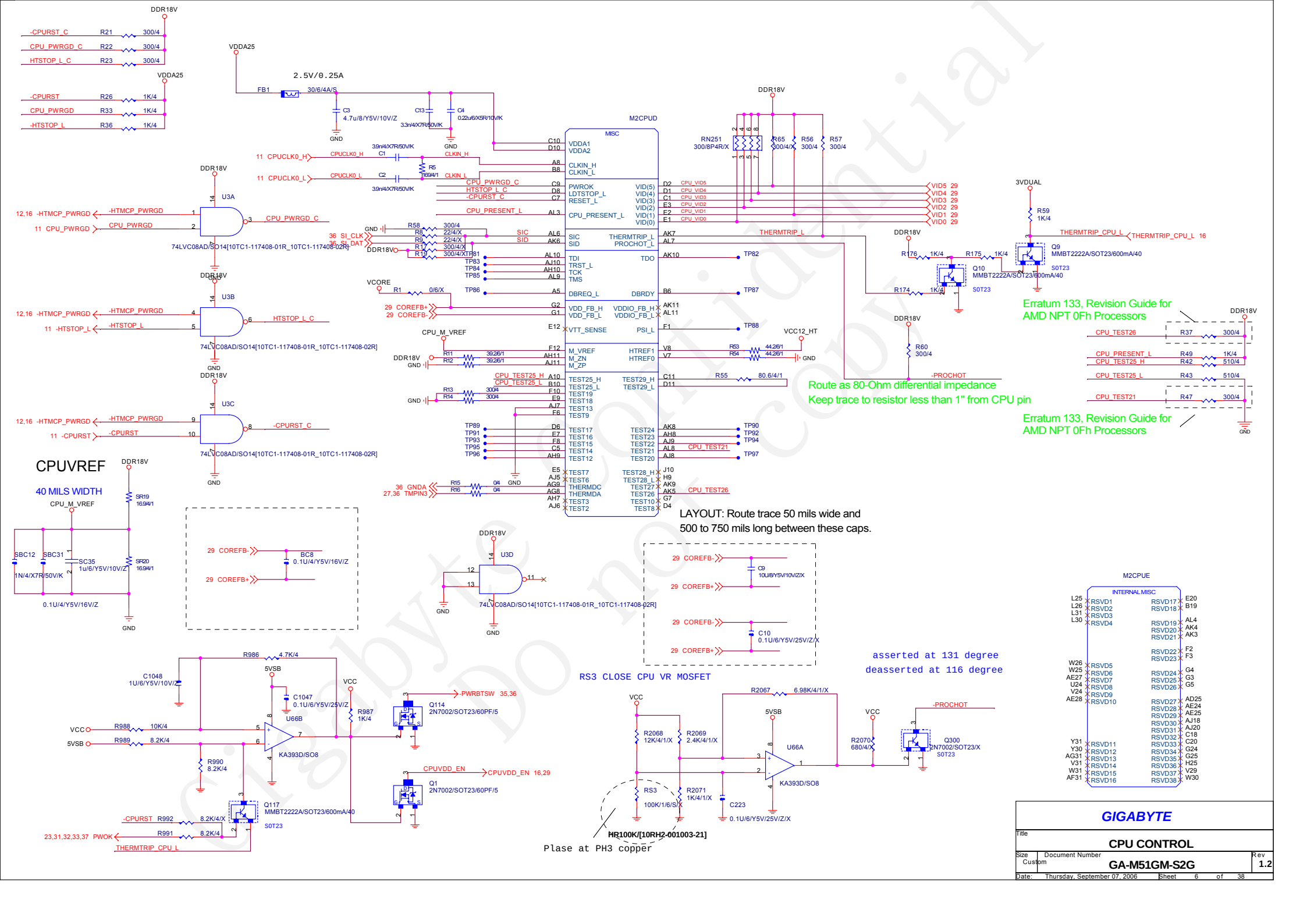


GIGABYTE

Title: **CPU DDRII MEMORY**

Size	Document Number	Rev
Custom	GA-M51GM-S2G	1.2

Date: Thursday, September 07, 2006 Sheet 5 of 38



GIGABYTE

Title	CPU CONTROL	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
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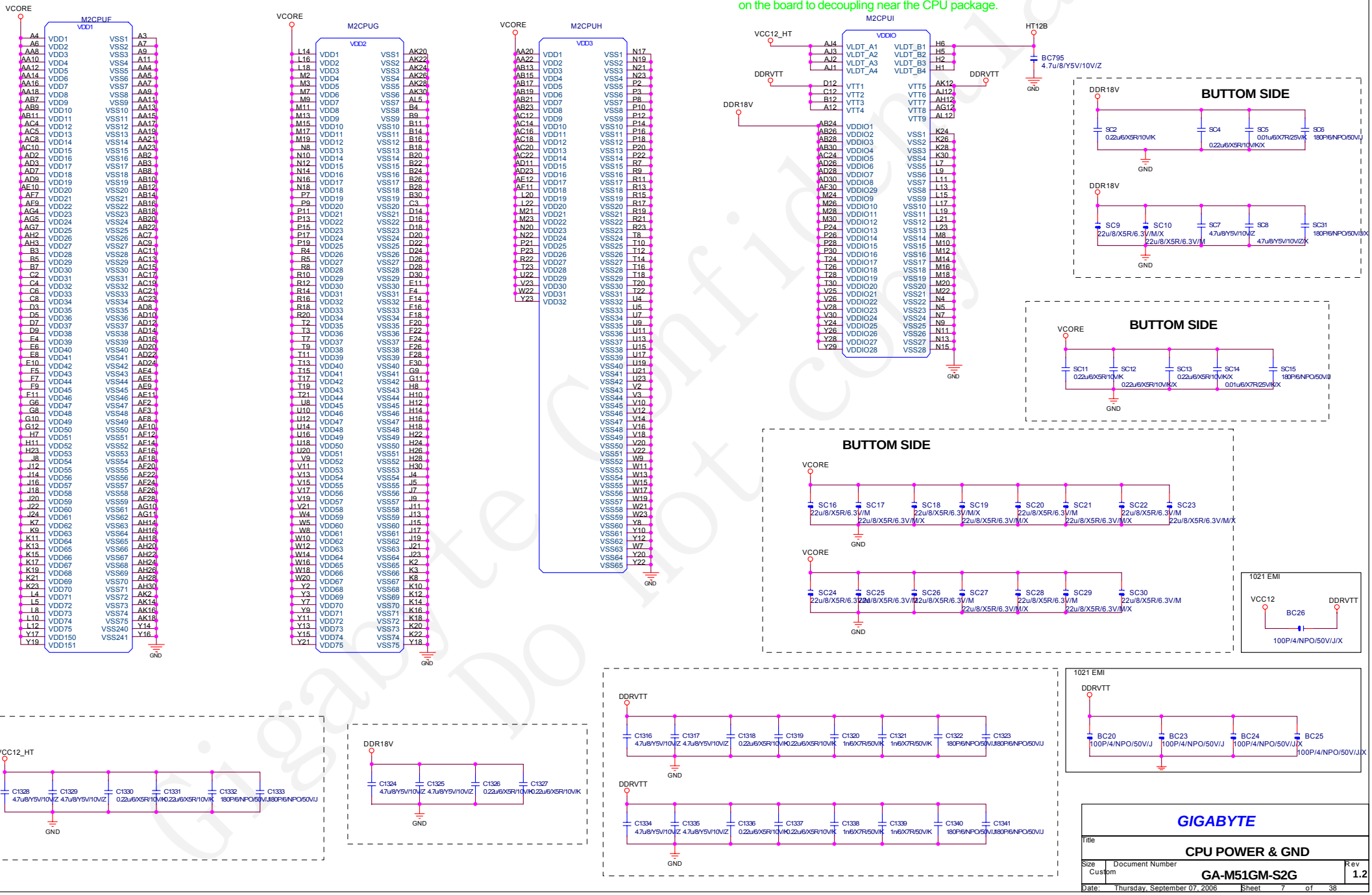
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

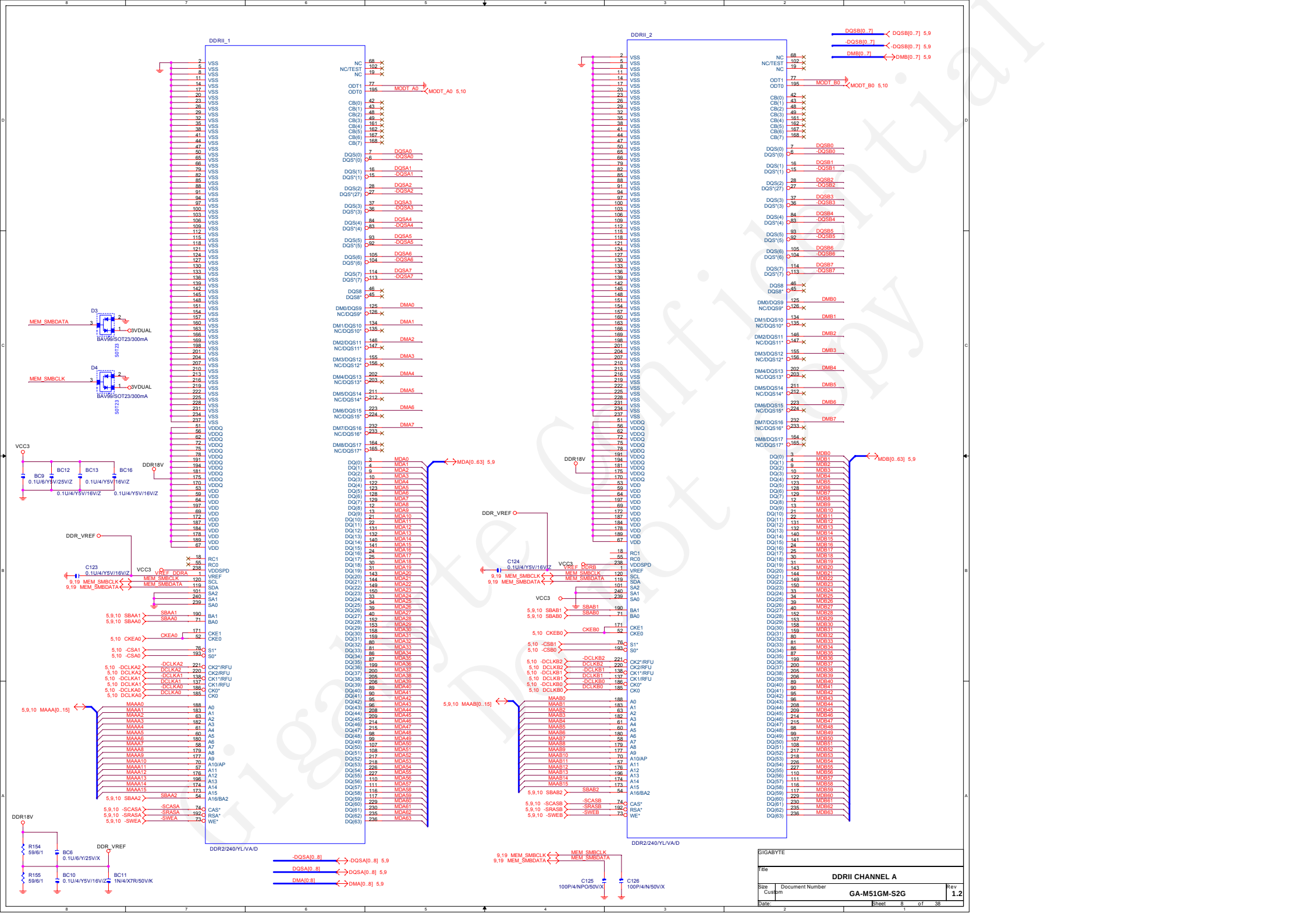


GIGABYTE

Title: **CPU POWER & GND**

Size	Document Number	Rev
Custom	GA-M51GM-S2G	1.2

Date: Thursday, September 07, 2006 Sheet 7 of 38


DDRII_1
DDRII_2
DDR2/240/YL/VA/D
DDR2/240/YL/VA/D
MODT_A0 5,10
MODT_B0 5,10
MDA[0..63] 5,9
MDB[0..63] 5,9
DQSB[0..7] 5,9
DMB[0..7] 5,9
DQSA[0..8] 5,9
DMA[0..8] 5,9
MEM_SMBDATA
MEM_SMBCLK
BAV99/SOT23/300mA
3VDUAL
VCC3
DDR18V
DDR_VREF
GIGABYTE
DDRII CHANNEL A
GA-M51GM-S2G
Rev 1.2
Sheet 8 of 38
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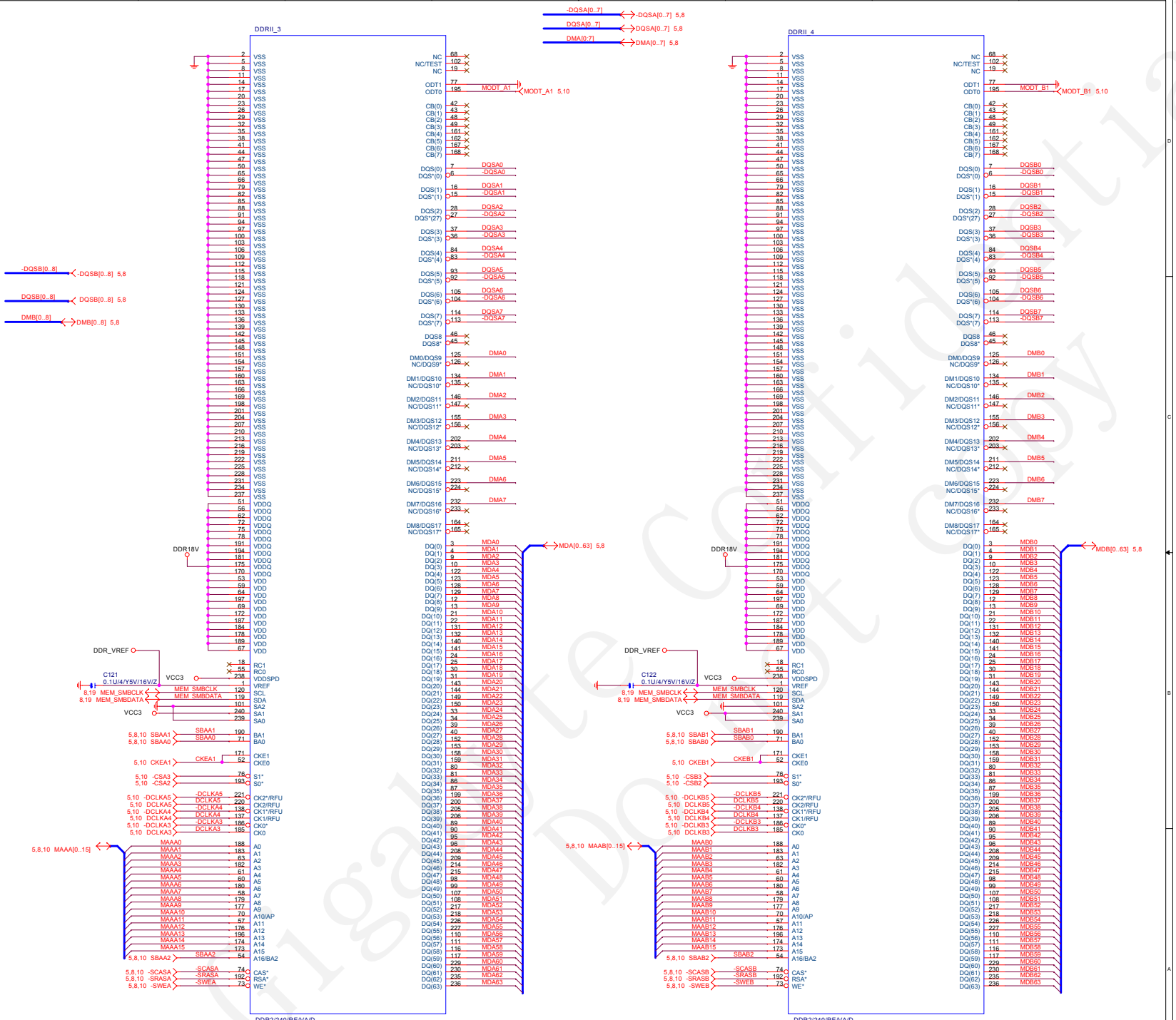

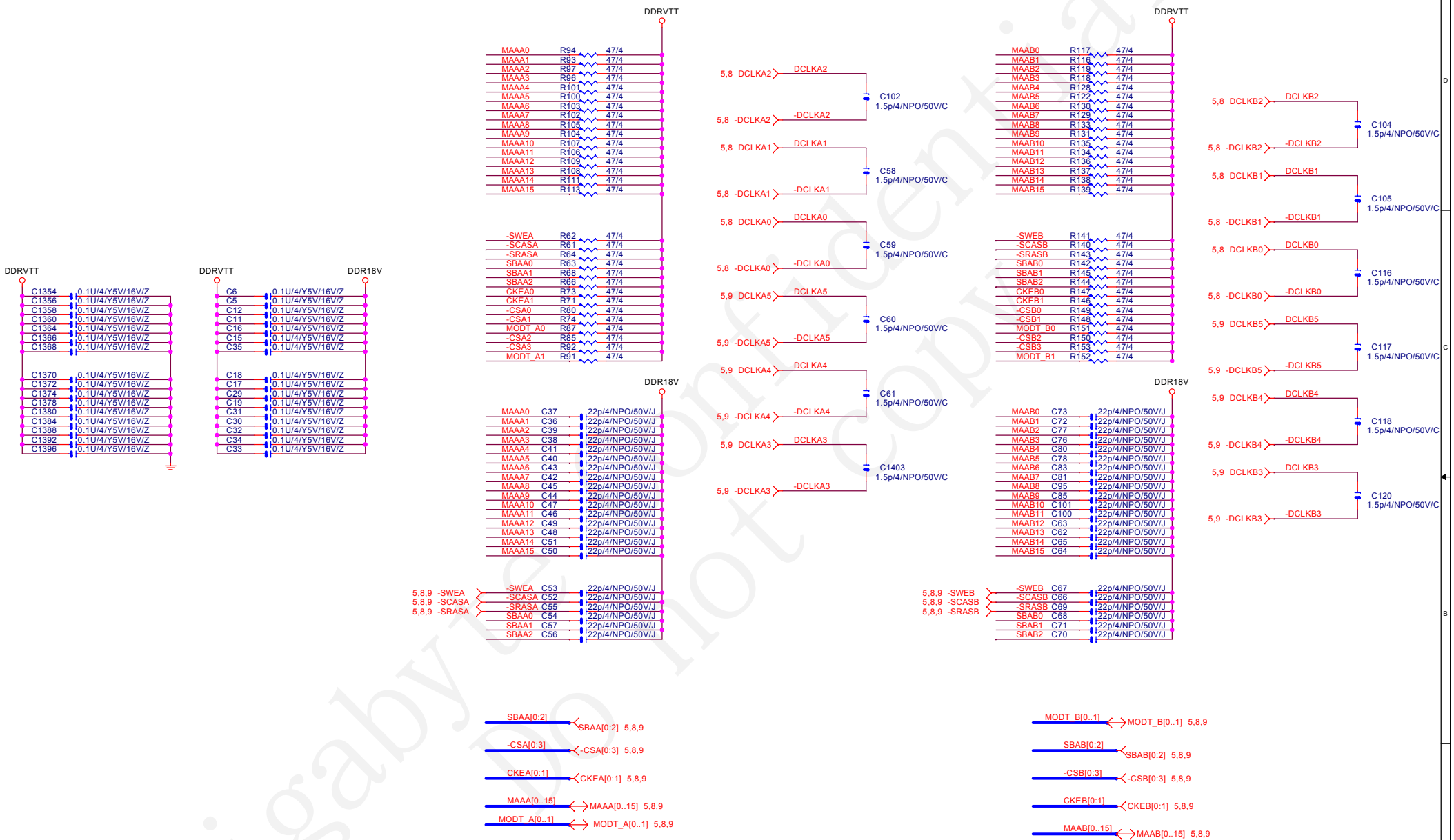

GIGABYTE

Title: DDRII TERMINATOR

Size: B | Document Number: GA-M51GM-S2G | Rev: 1.2

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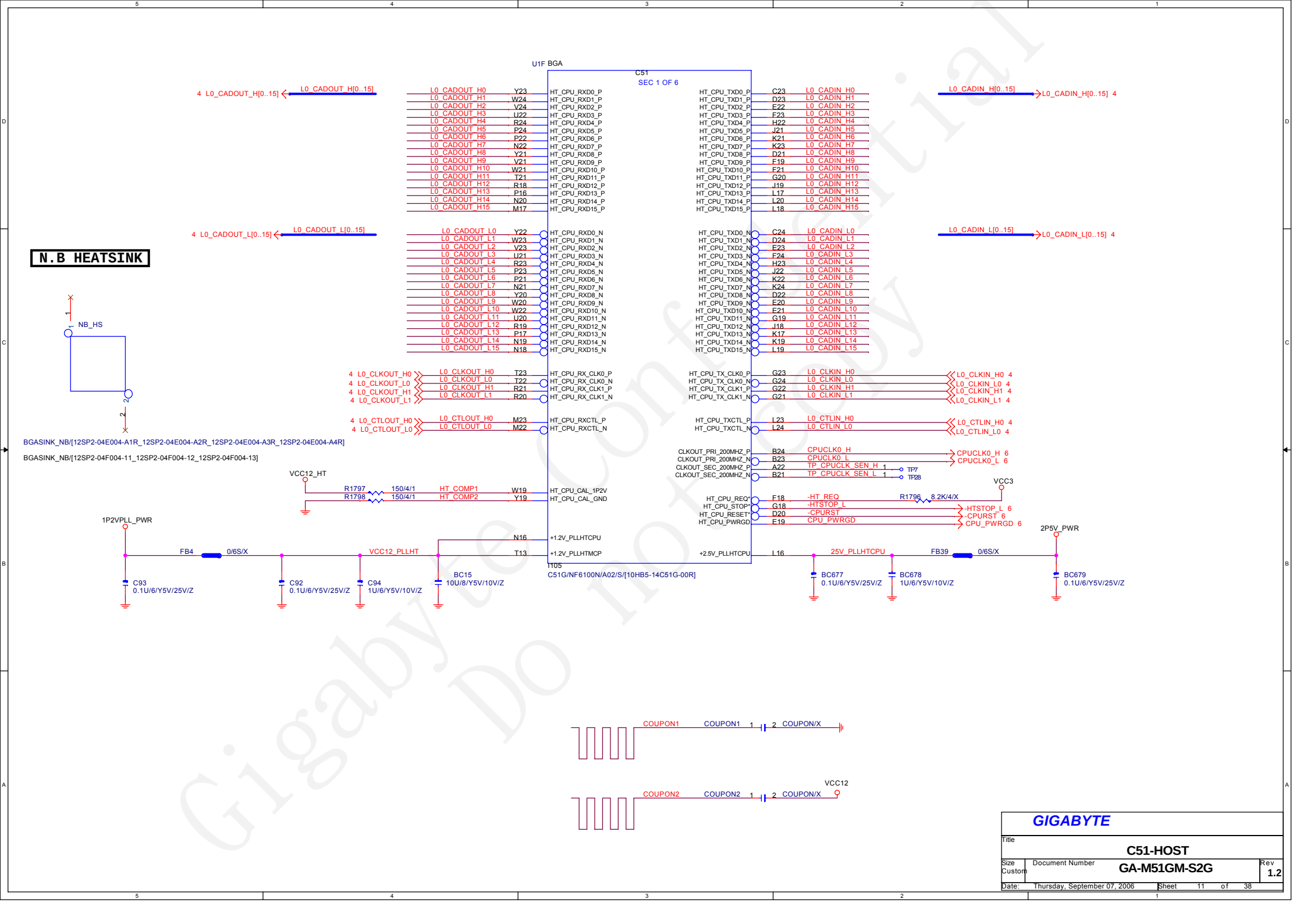
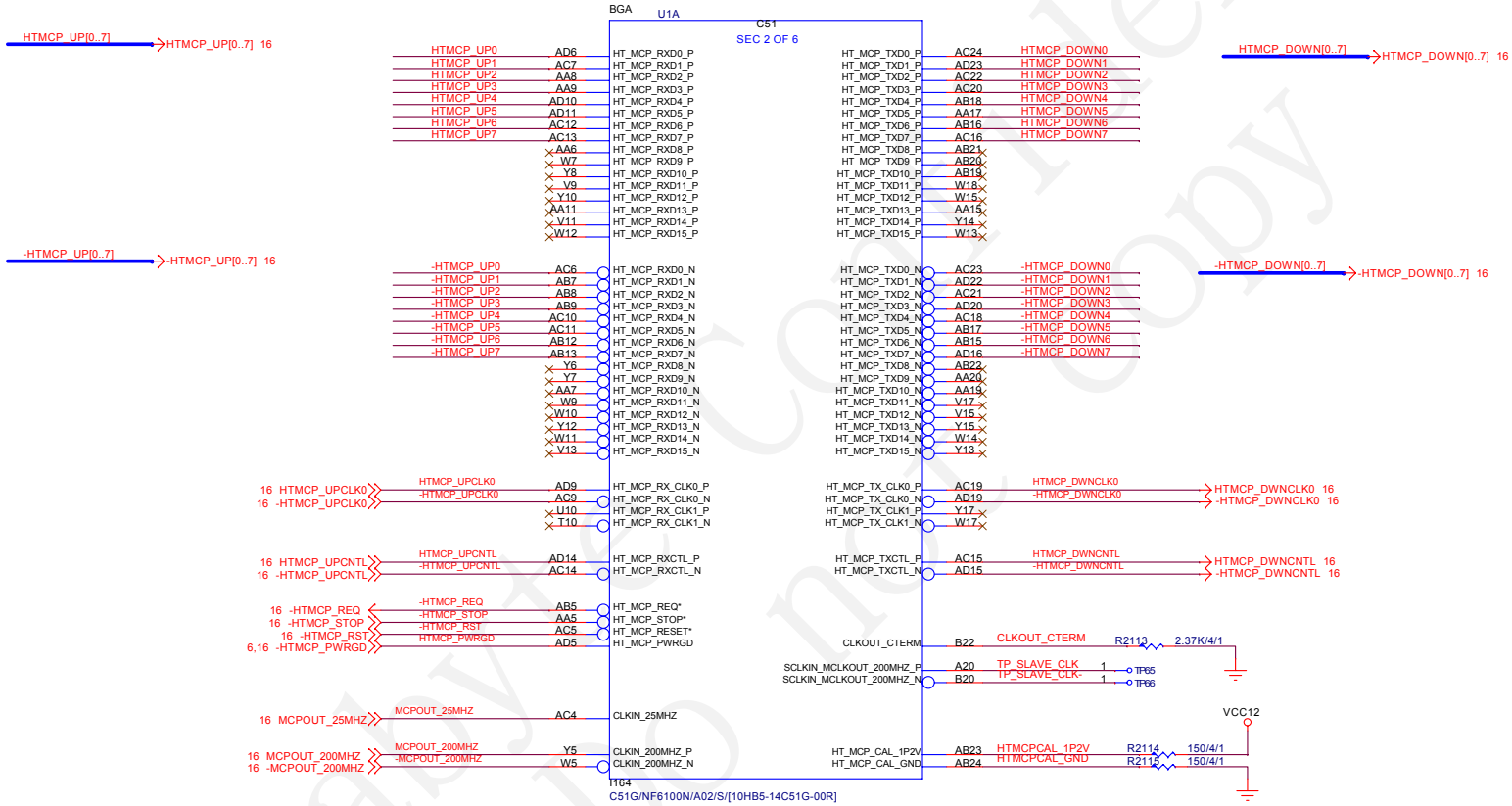


GIGABYTE		
Title	C51-HOST	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
Date: Thursday, September 07, 2006	Sheet 11 of 38	

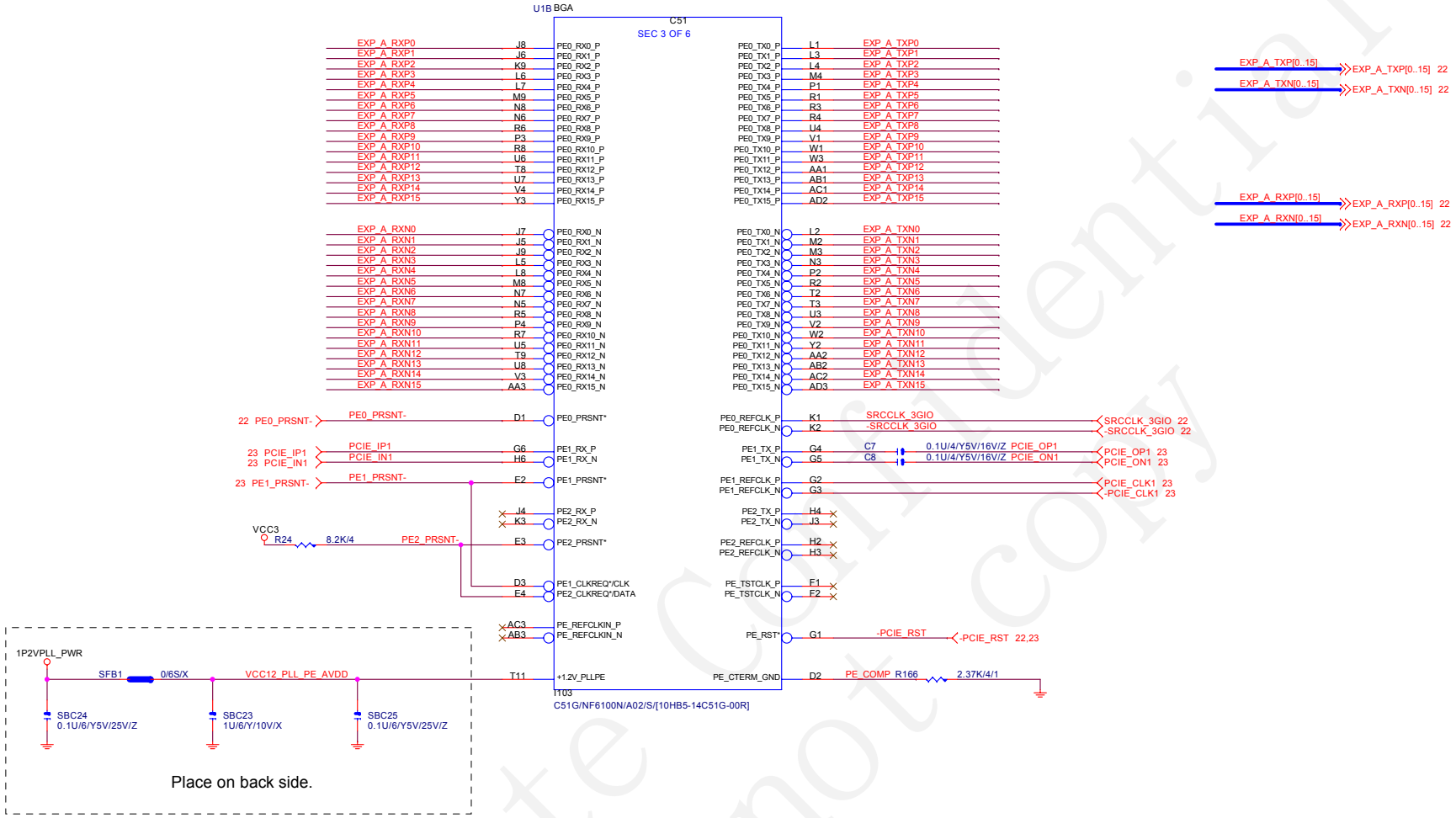


GIGABYTE

Title: C51-HT BUS

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

Date: Thursday, September 07, 2006 | Sheet 12 of 38

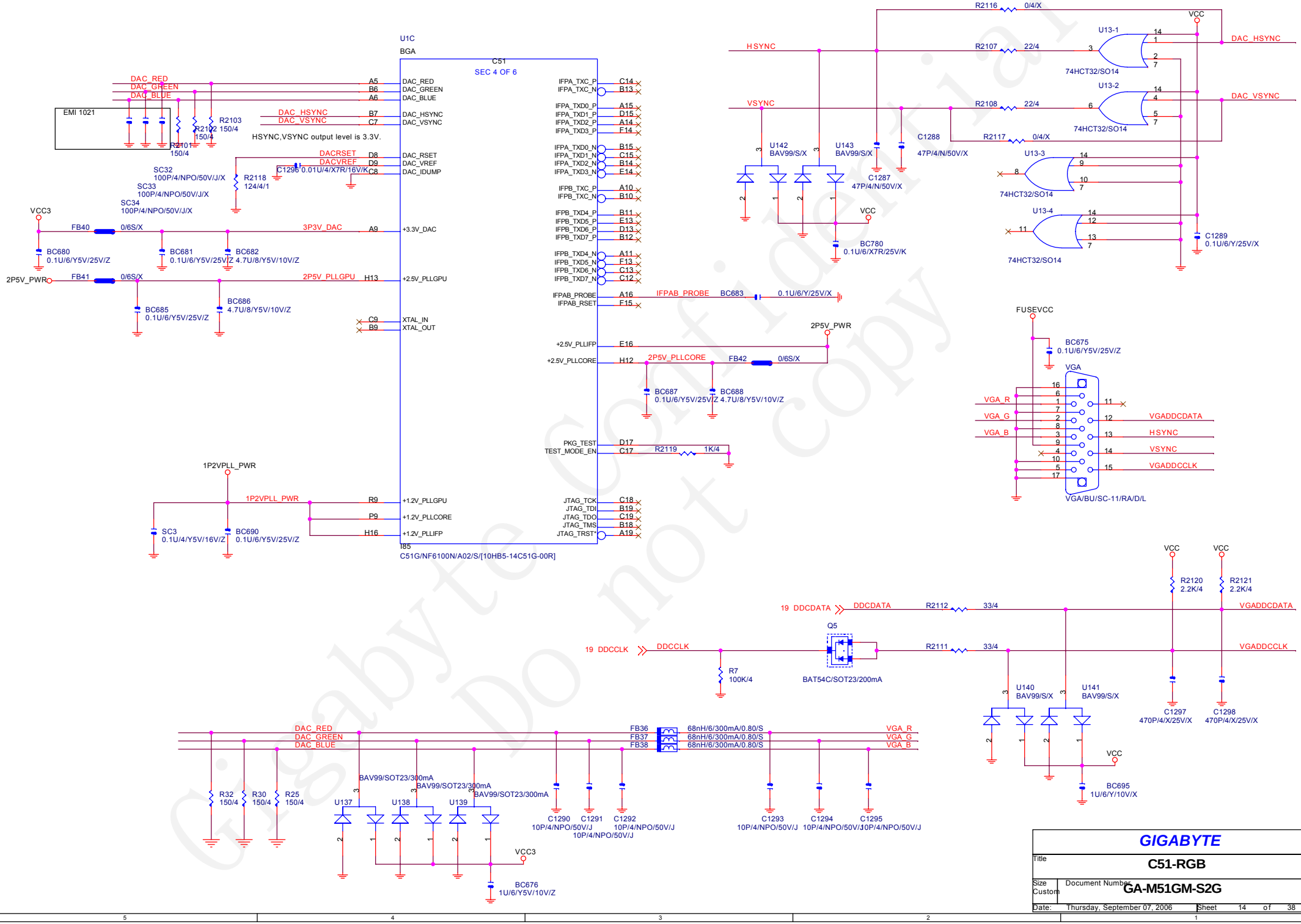


GIGABYTE

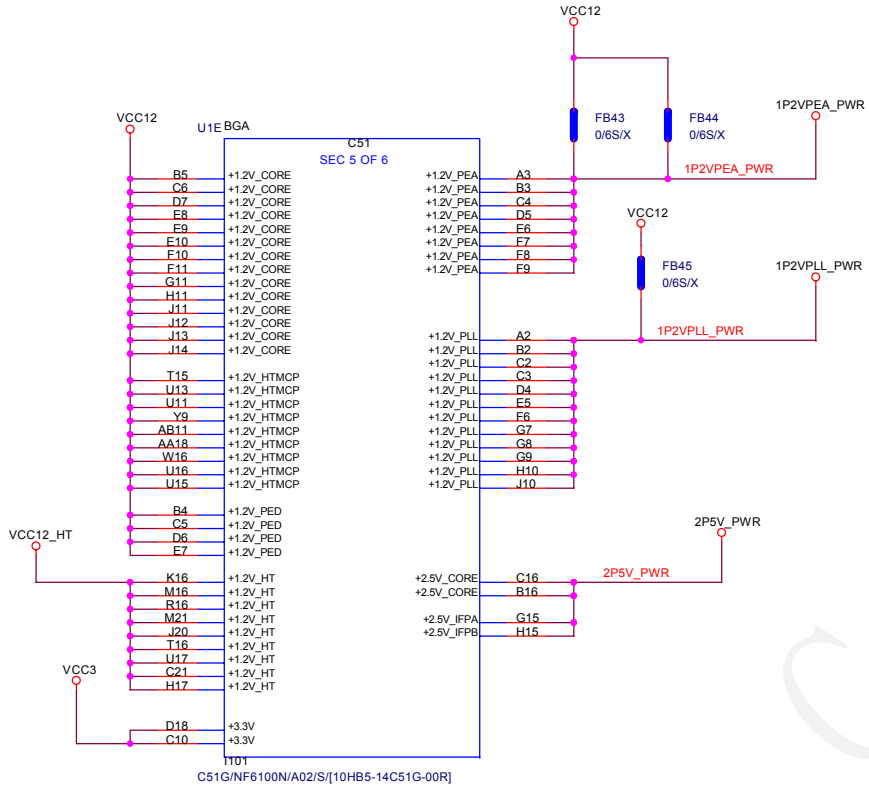
Title: C51-PCI EXPRESS

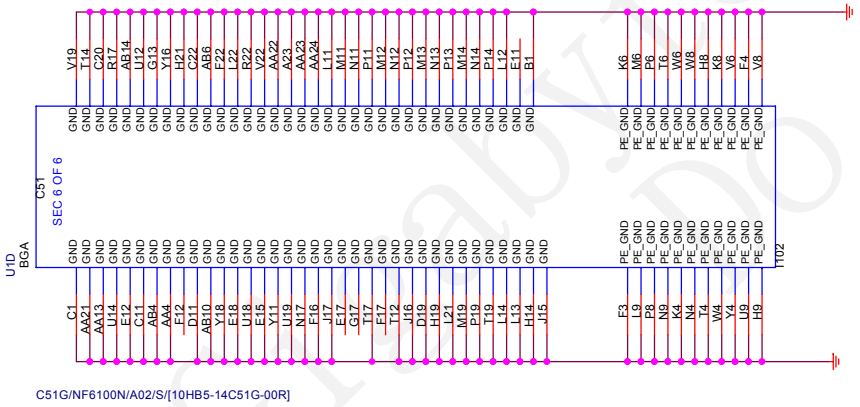
Size	Document Number	Rev
Custom	GA-M51GM-S2G	1.2

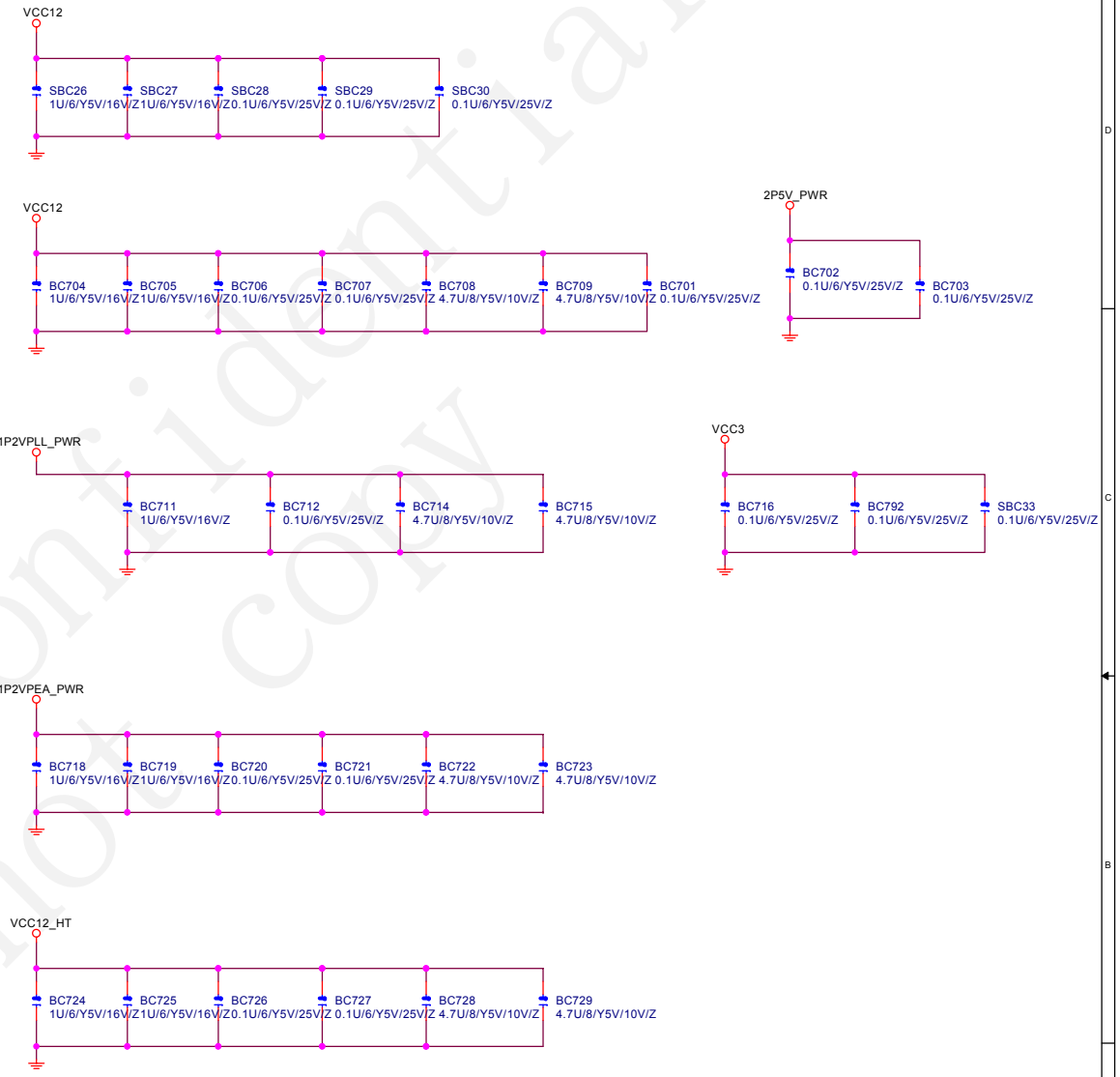
Date: Thursday, September 07, 2006 Sheet 13 of 38



GIGABYTE		
Title	C51-RGB	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
Date: Thursday, September 07, 2006	Sheet 14 of 38	







GIGABYTE

Title: C51-PWR/GND

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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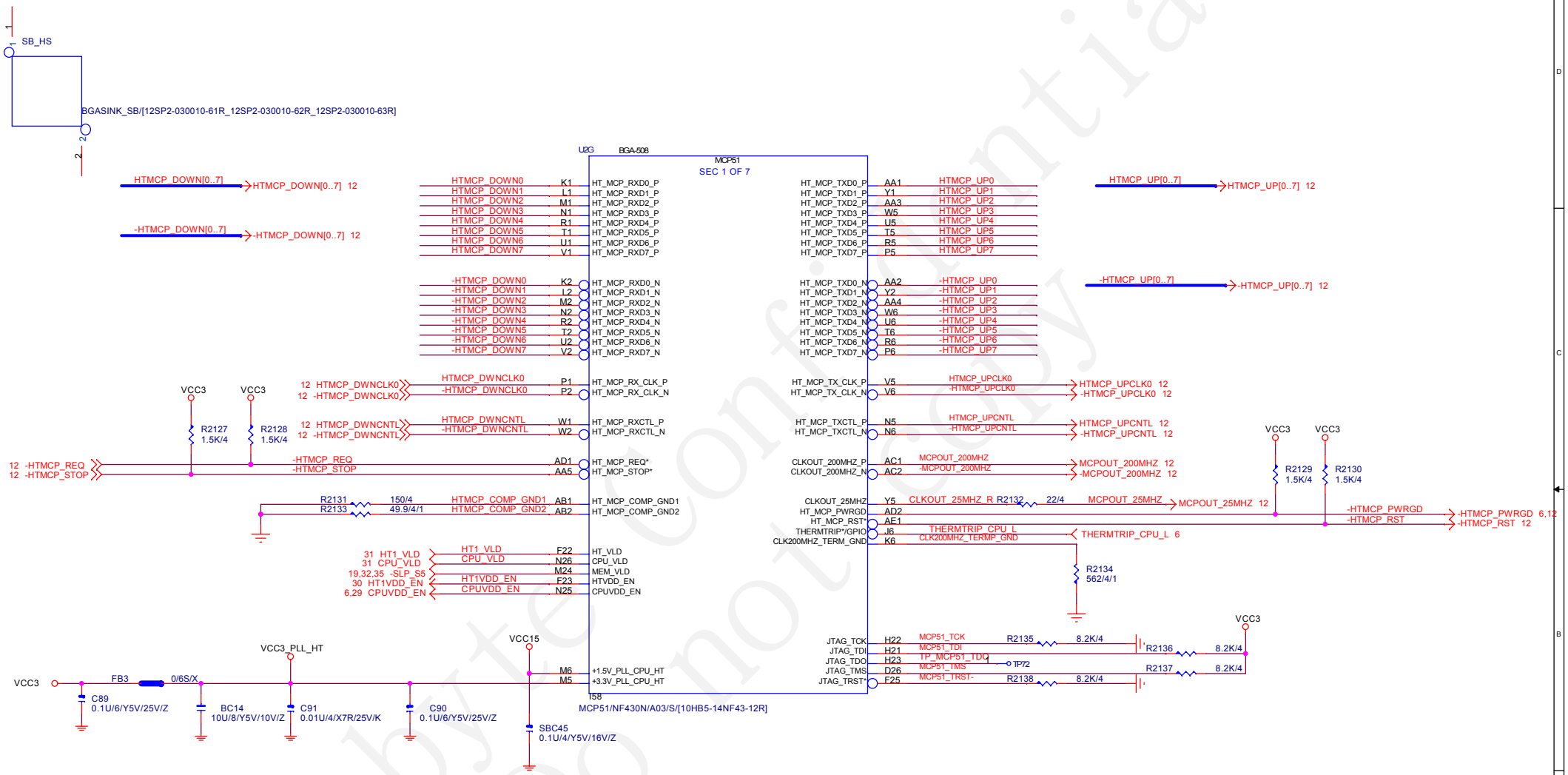
S.B FANSINK



GIGABYTE

Title: MCP51-HT BUS

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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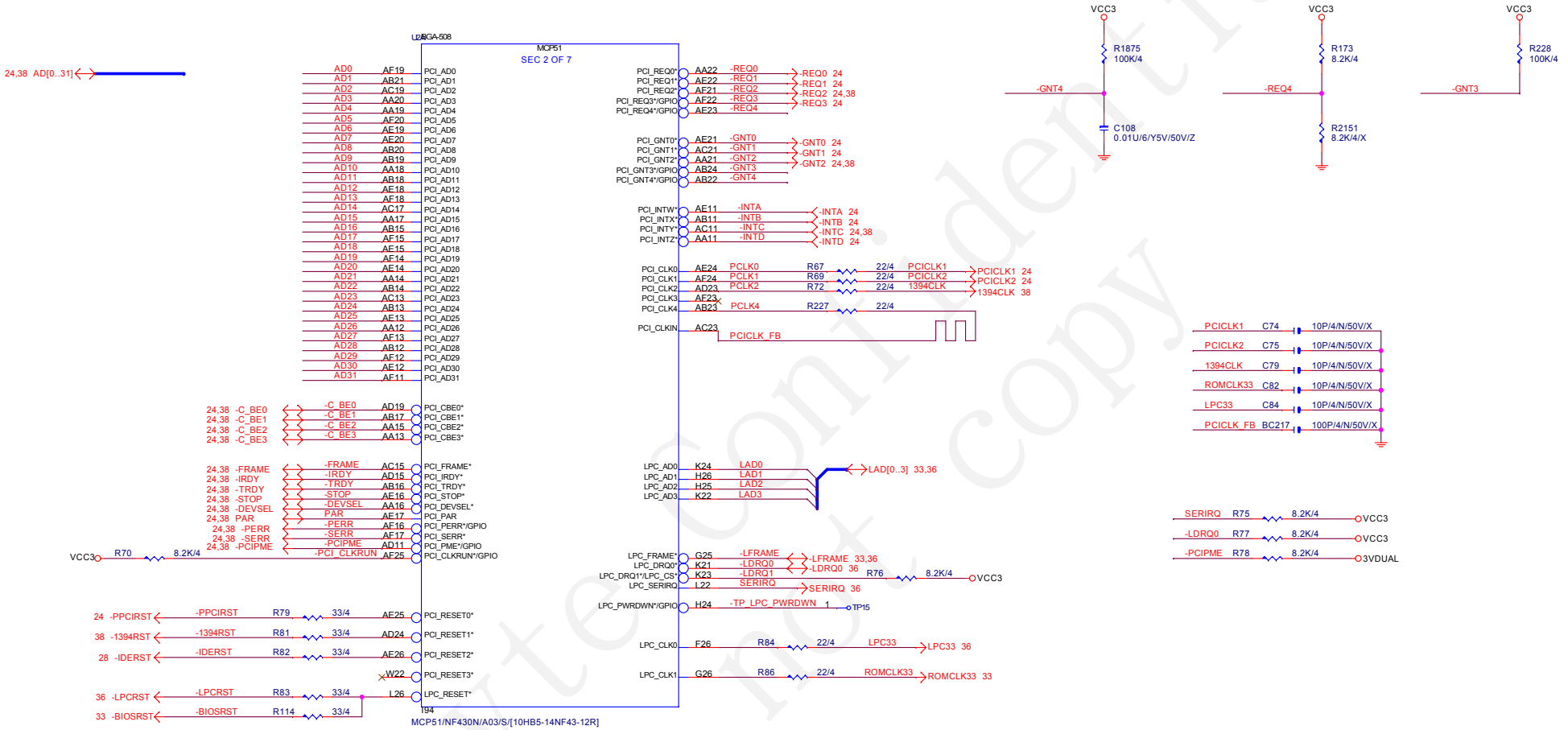
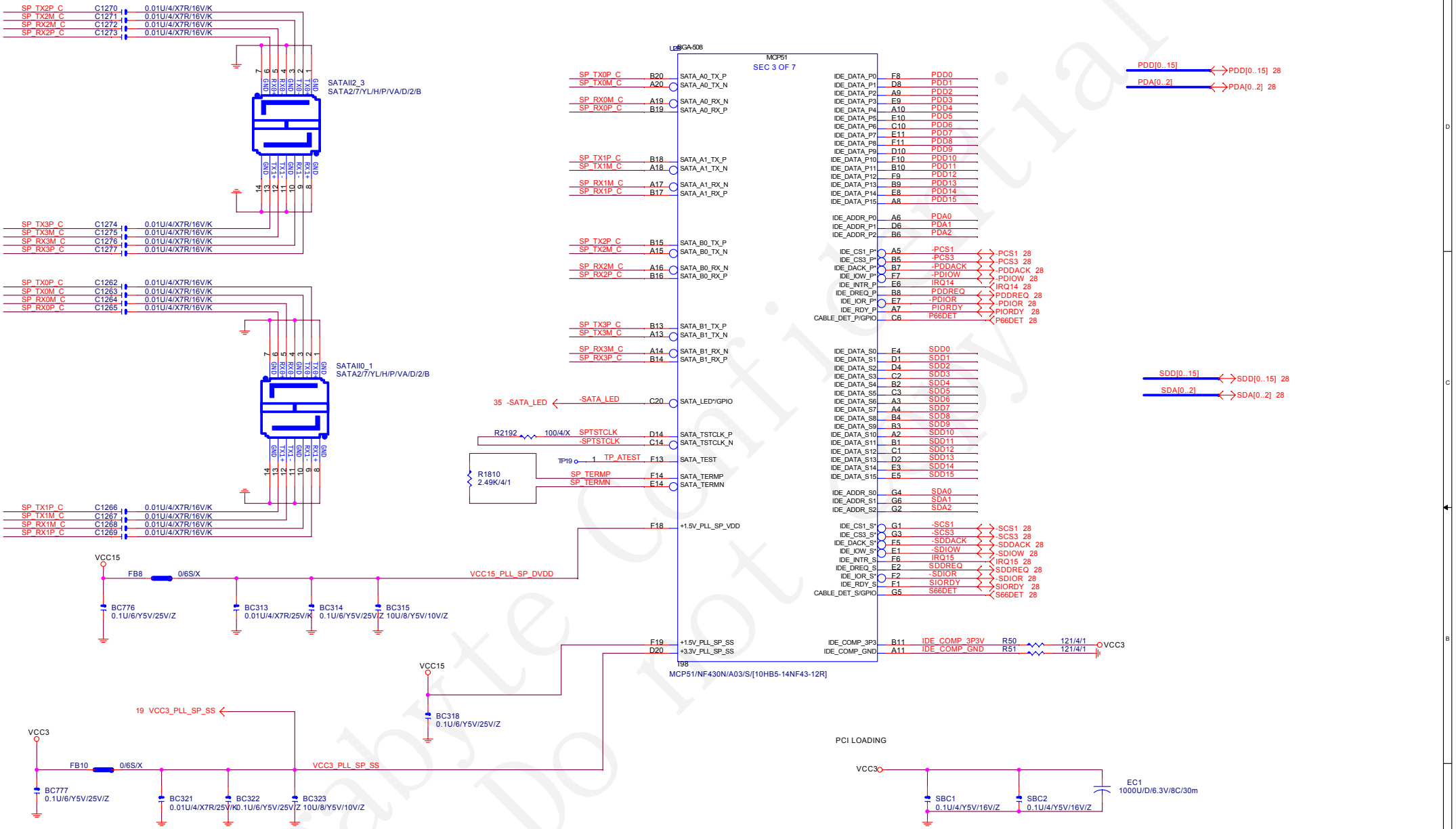


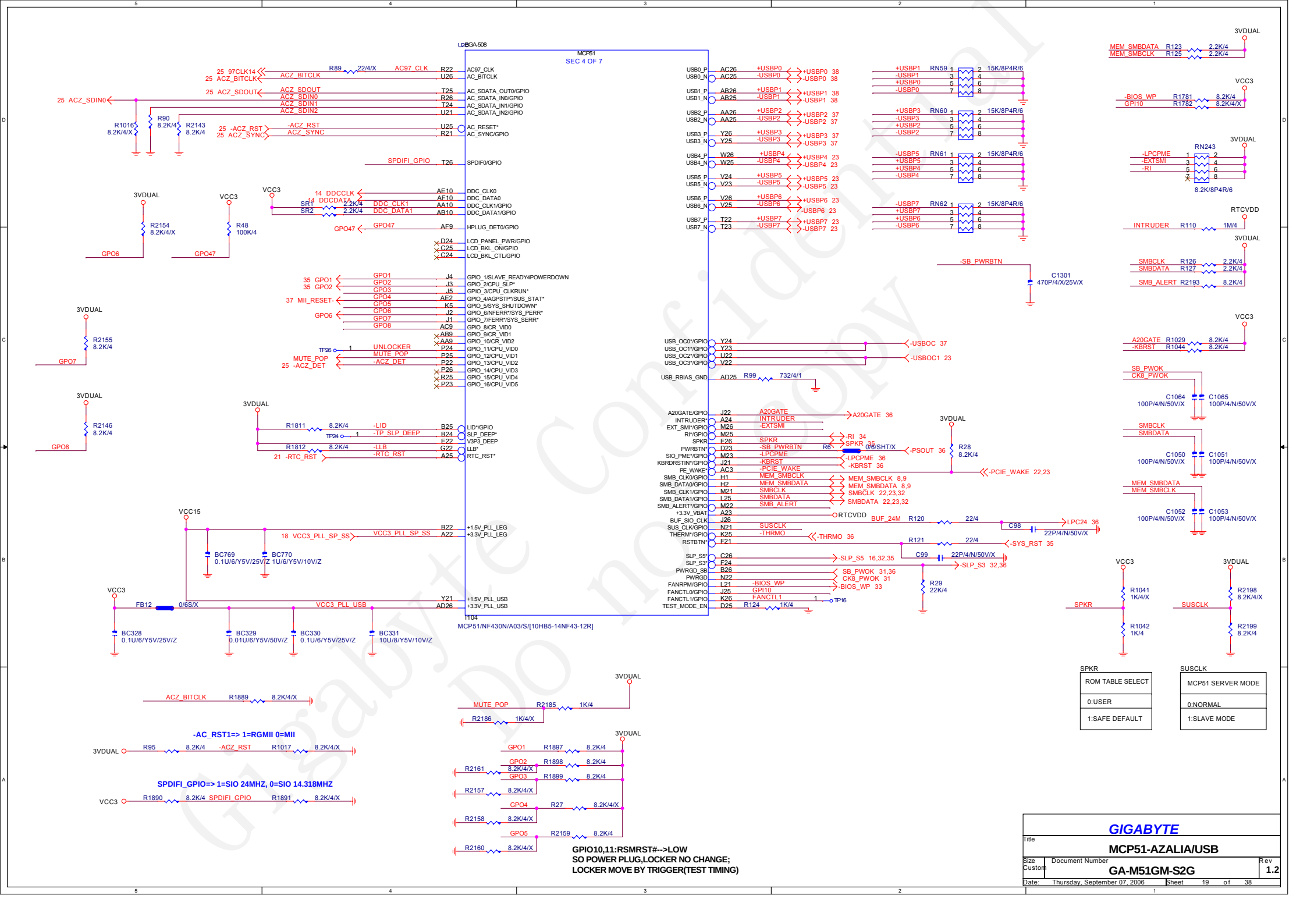
GIGABYTE

Title: MCP51-PCI BUS

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

Date: Thursday, September 07, 2006 | Sheet 17 of 38




MCP51
SEC 4 OF 7
MCP51/NF430N/A03/S/[10HB5-14NF43-12R]
GPIO10,11:RSMRST#-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST TIMING)
-AC_RST1=> 1=RGMII 0=MII
SPDIFI_GPIO=> 1=SIO 24MHZ, 0=SIO 14.318MHZ
SPKR
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
SUSCLK
MCP51 SERVER MODE
0:NORMAL
1:SLAVE MODE
GIGABYTE
MCP51-AZALIA/USB
GA-M51GM-S2G
1.2
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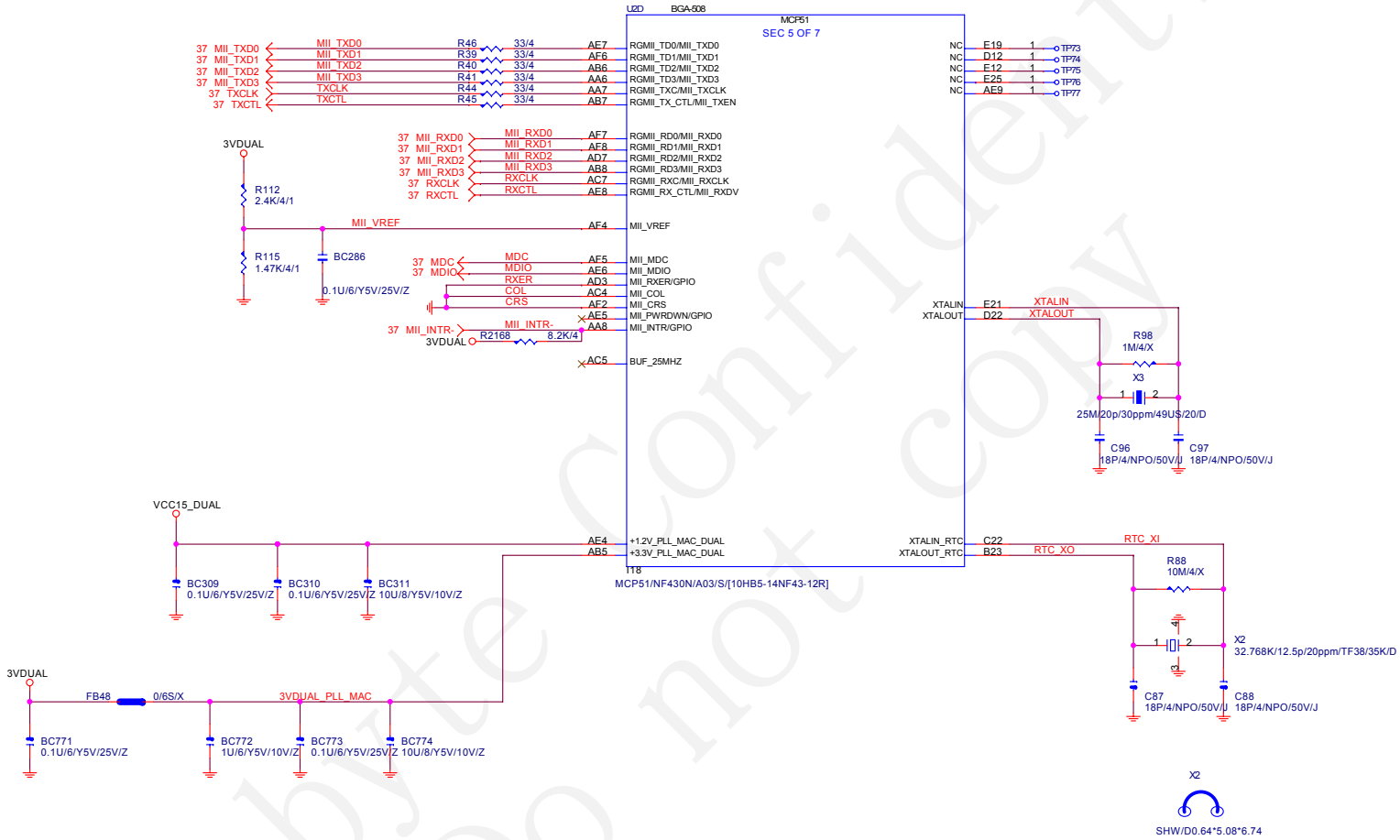

GIGABYTE

Title: MCP51-RGMII

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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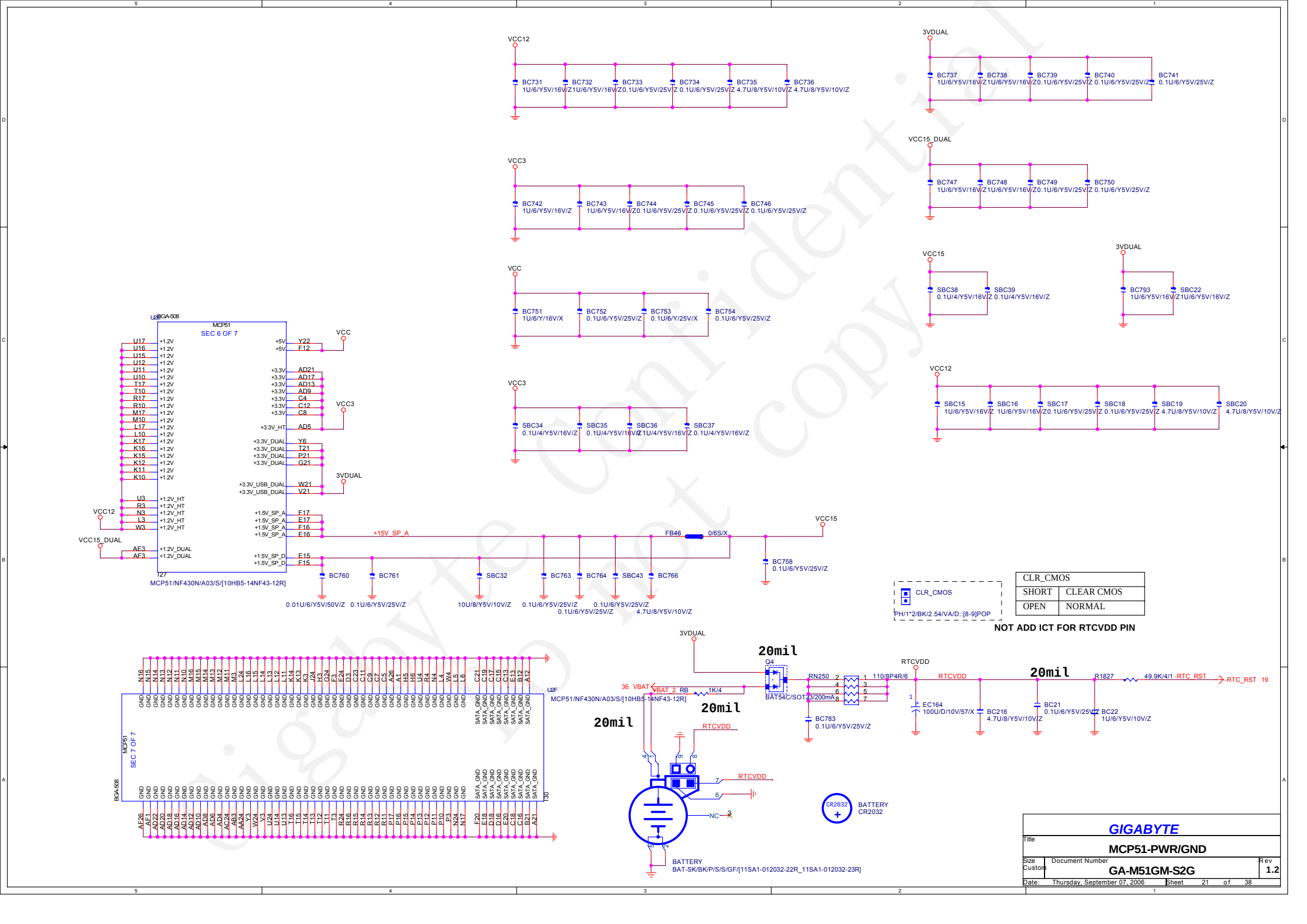

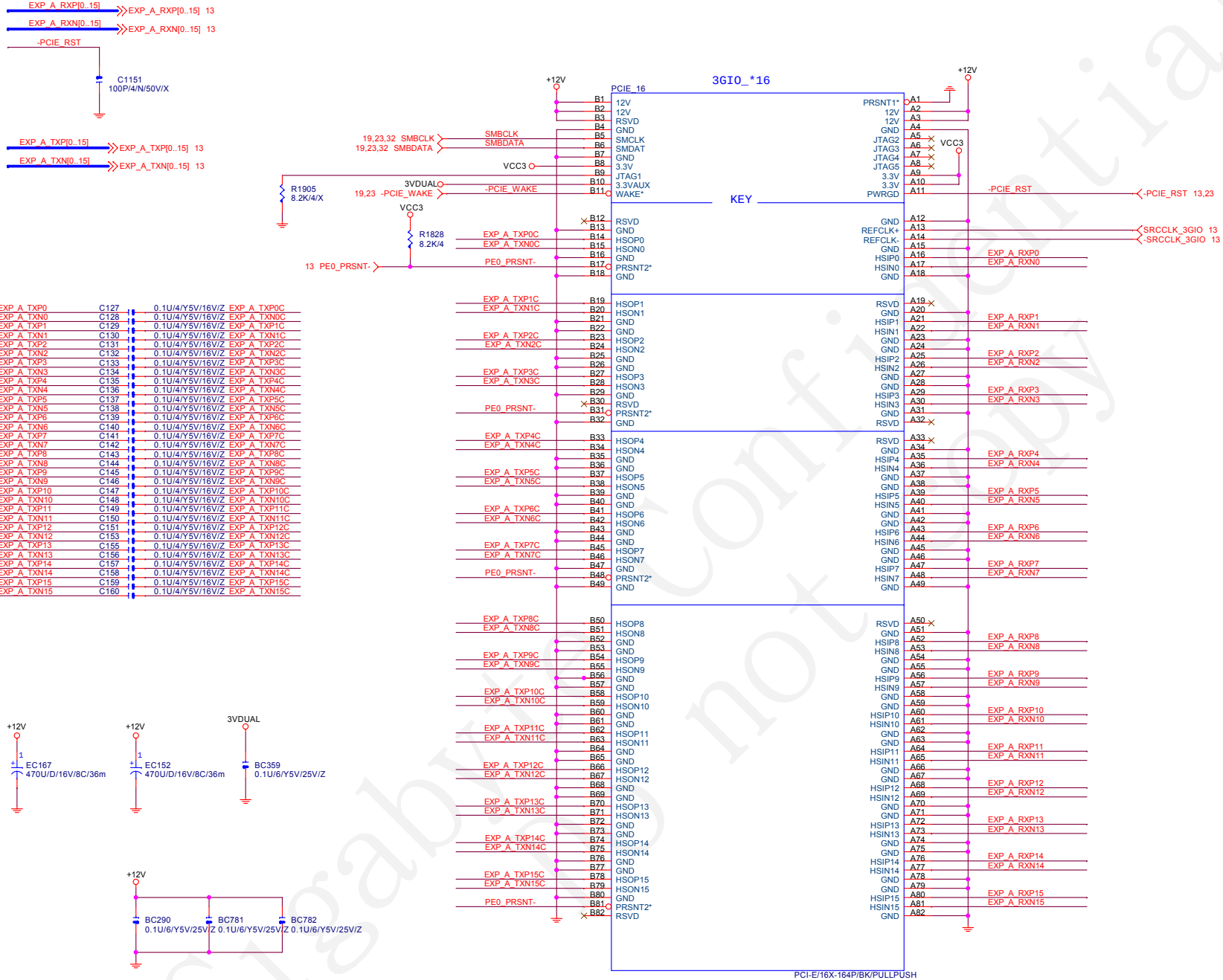

GIGABYTE

Title: PCI EXPRESS X 16

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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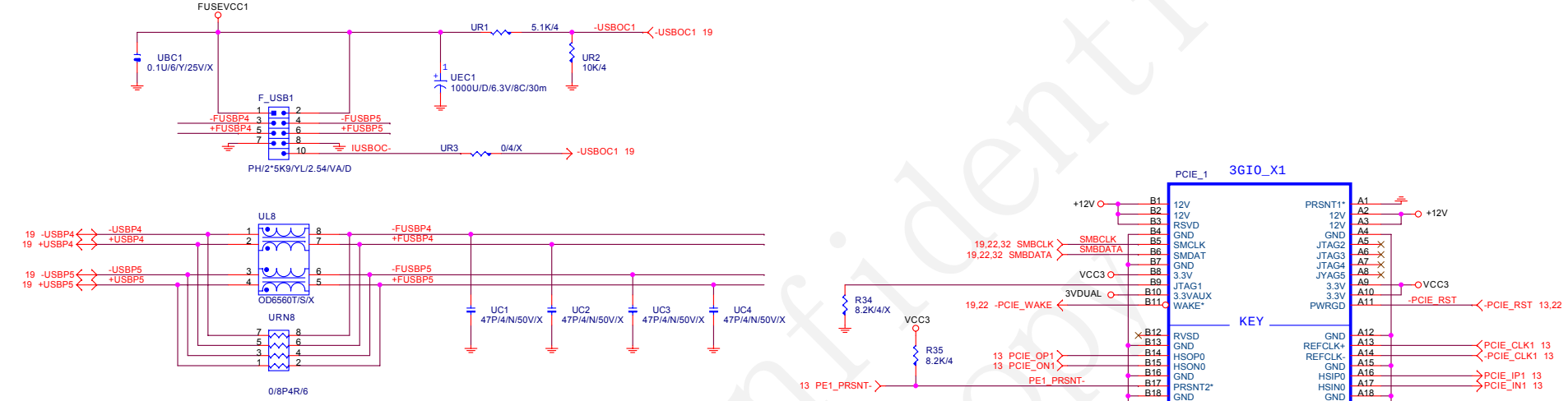
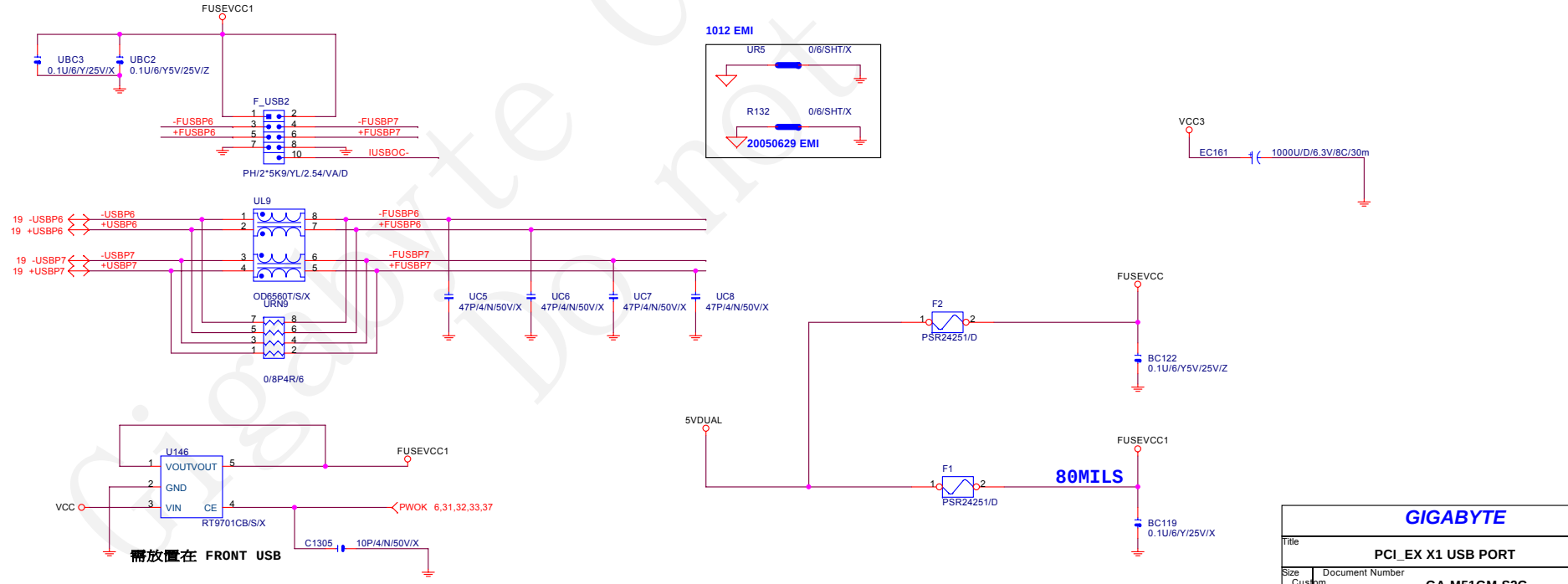
FRONT SIDE USB1



FRONT SIDE USB2



GIGABYTE

Title: PCI_EX X1 USB PORT

Size: Custom | Document Number: GA-M51GM-S2G | Rev: 1.2

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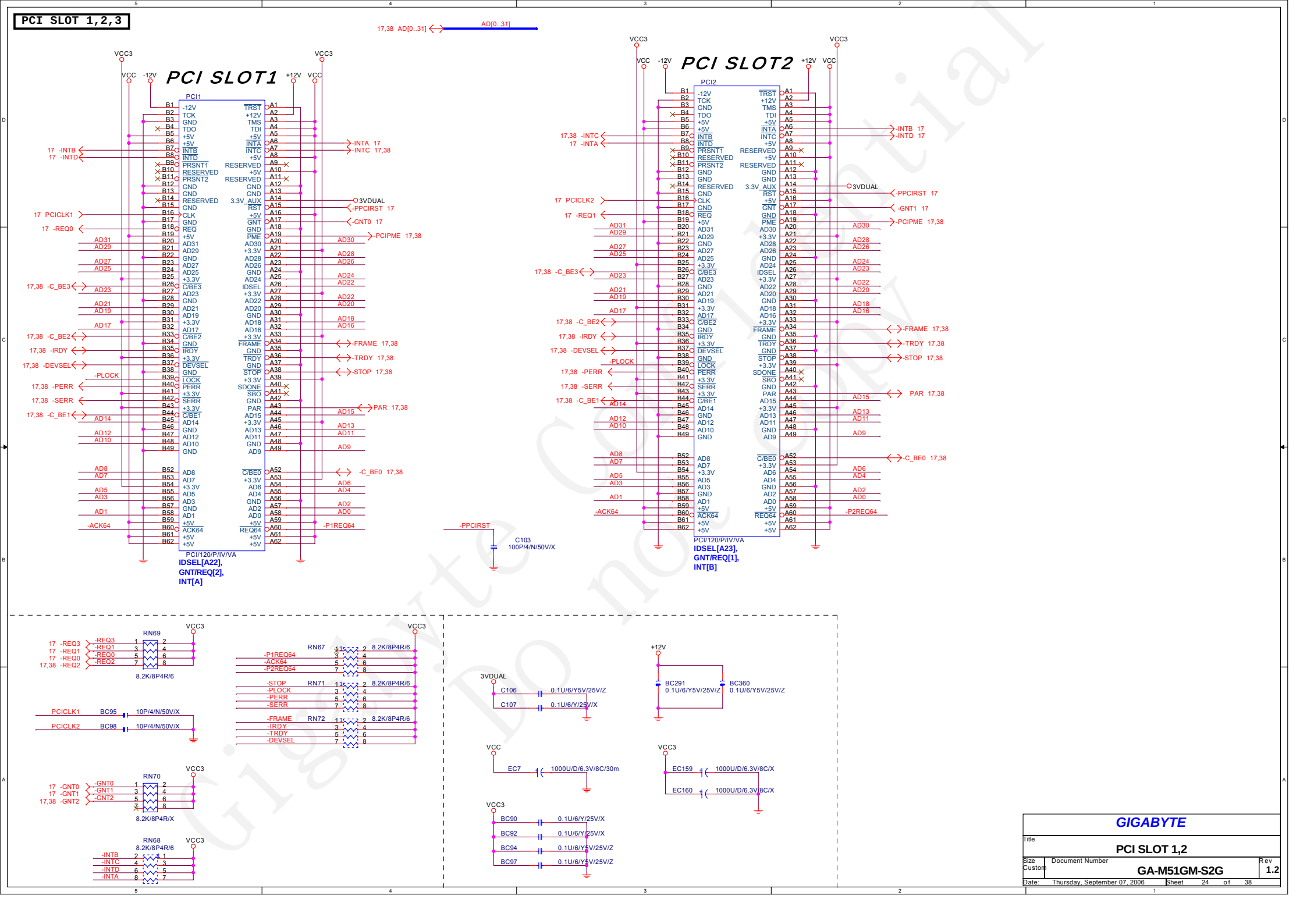
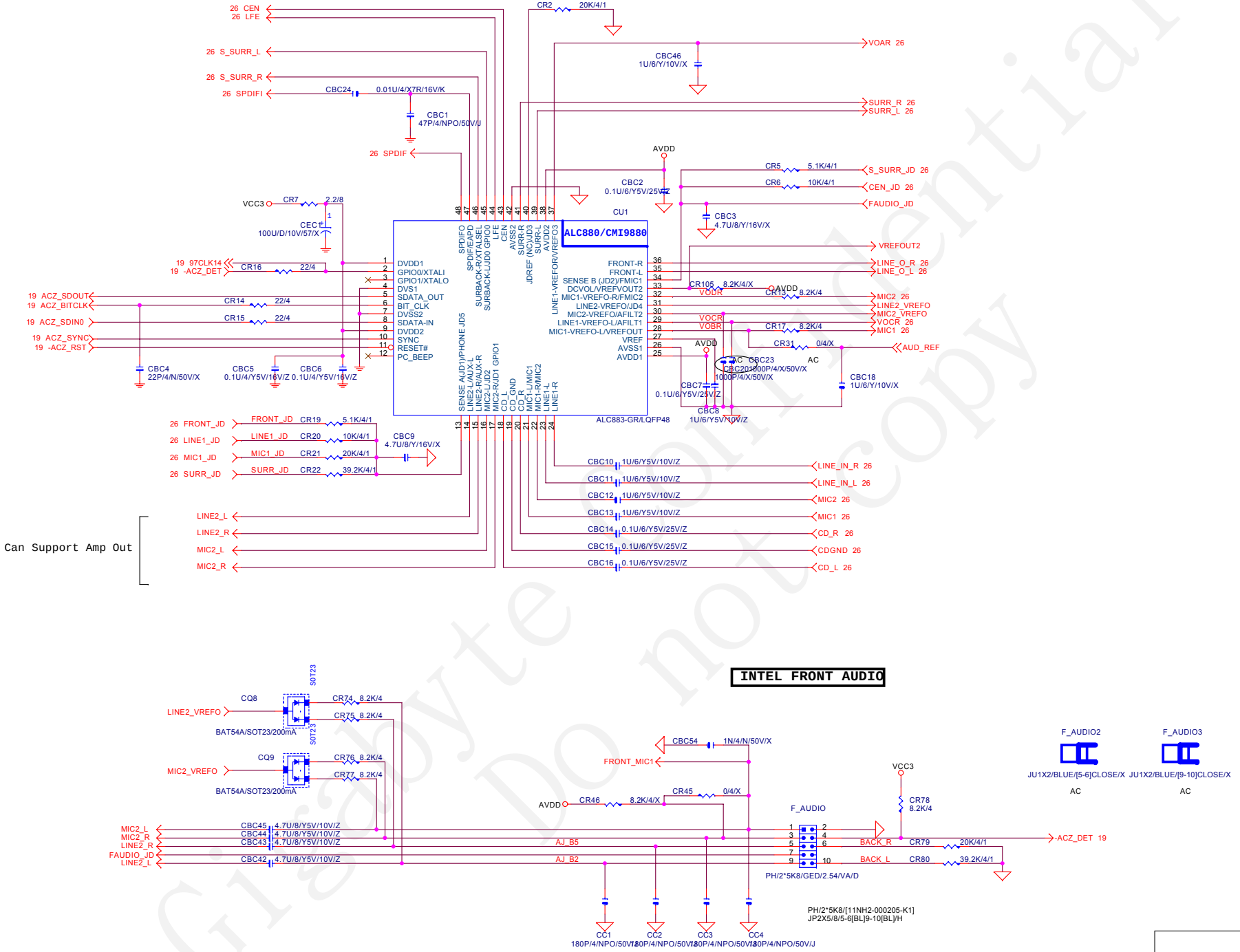
PCI SLOT 1,2,3



GIGABYTE

Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
Date: Thursday, September 07, 2006	Sheet 24 of 38	



GIGABYTE			
Title	ALC883		
Size: Custom	Document Number: GA-M51GM-S2G		Rev: 1.2
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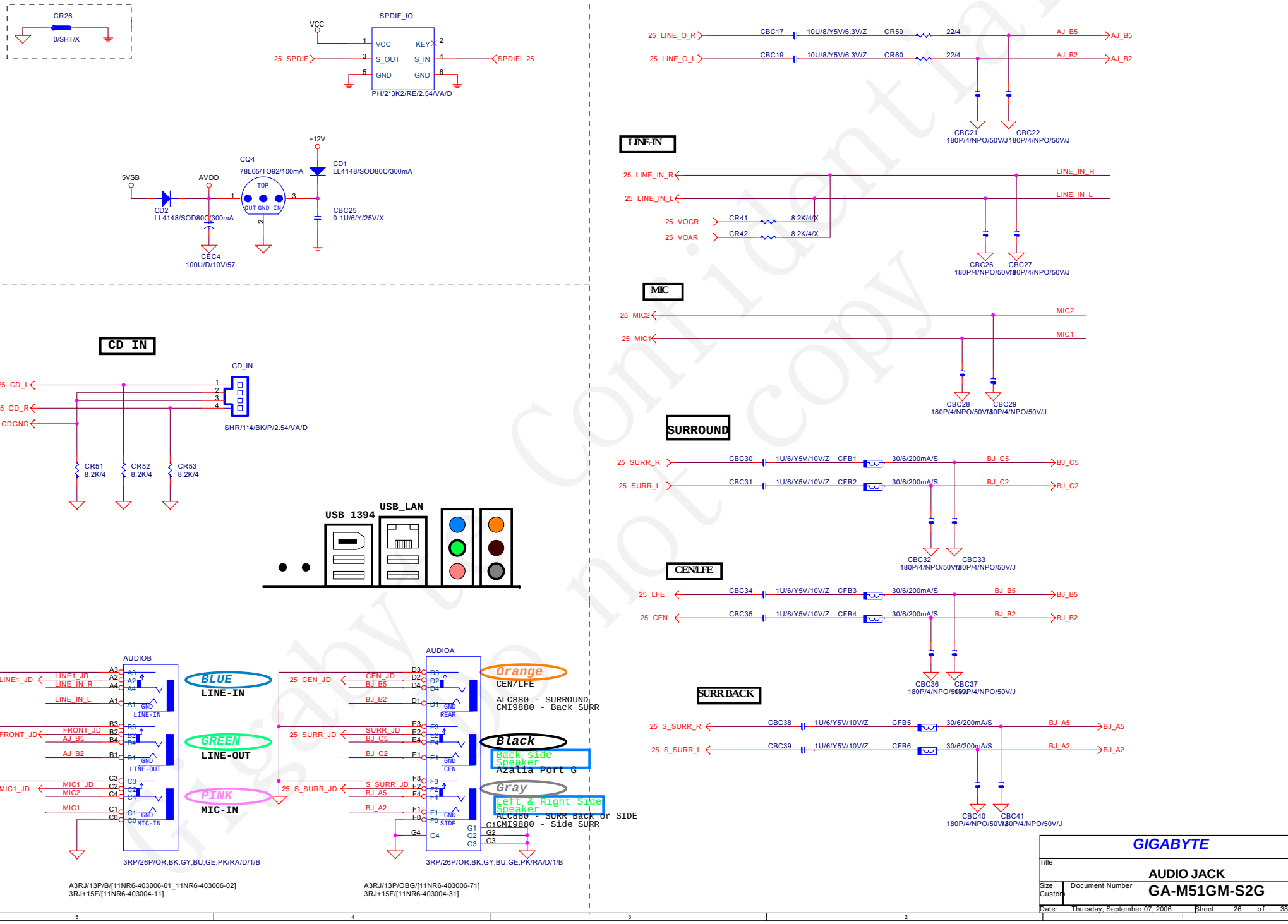
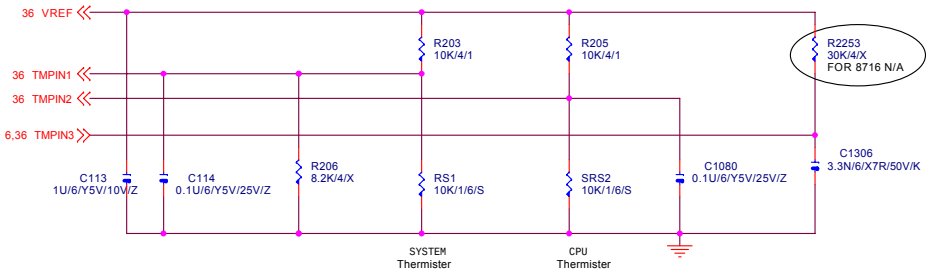
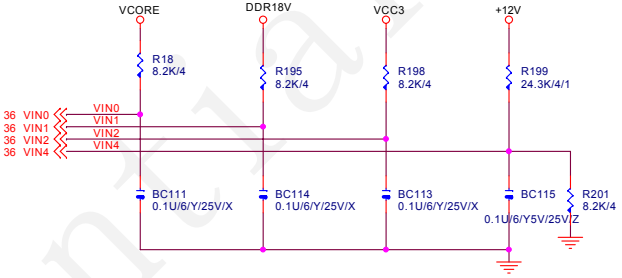
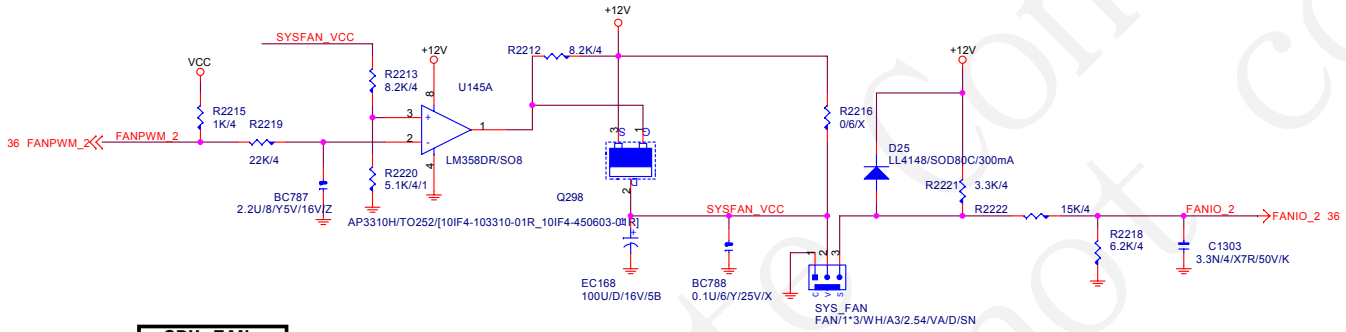


Hardware Monitor circuits

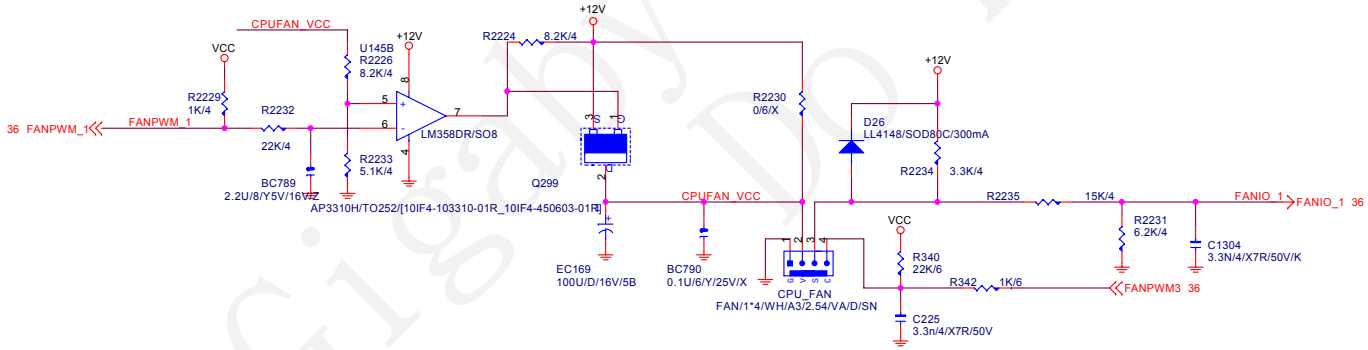




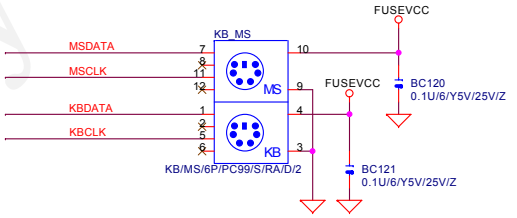
SYSTEM FAN

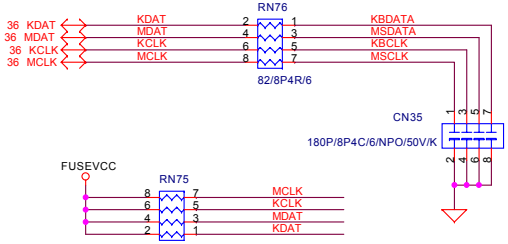


CPU FAN



KB & MS





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Title: FAN/HWMO KB/MS

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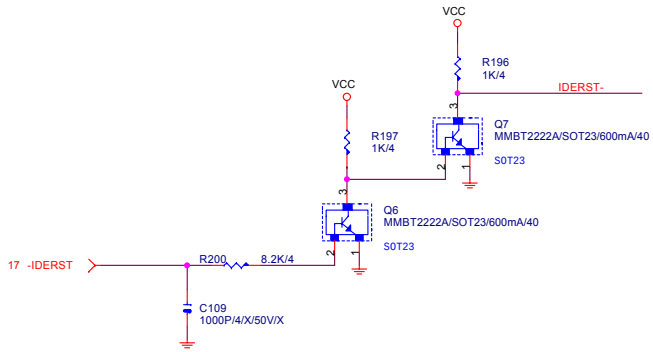
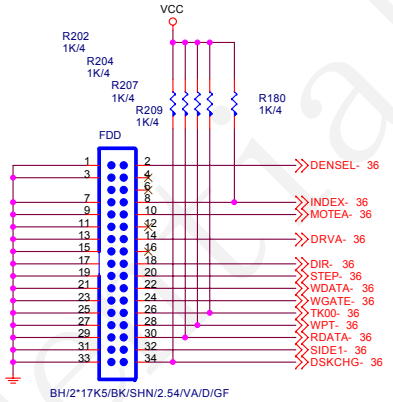
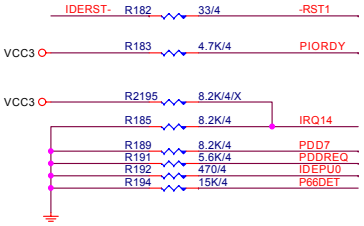
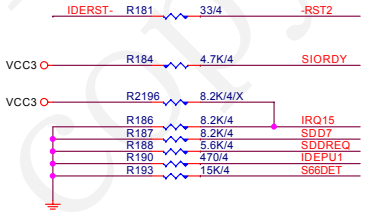
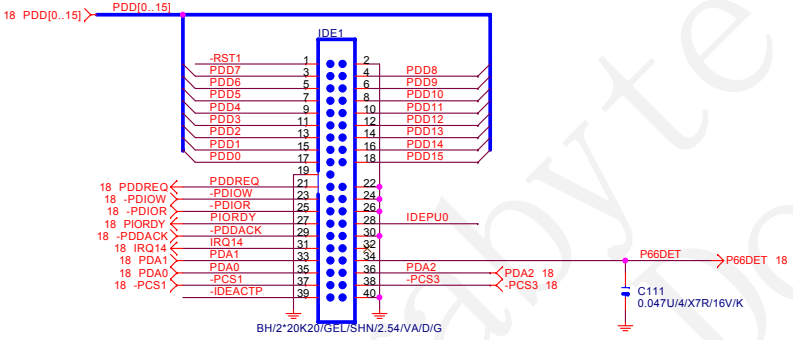




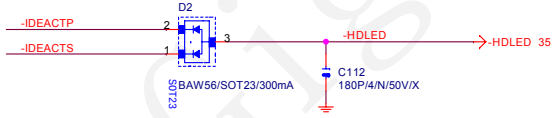




PRIMARY IDE CONNECTOR



Close to connector



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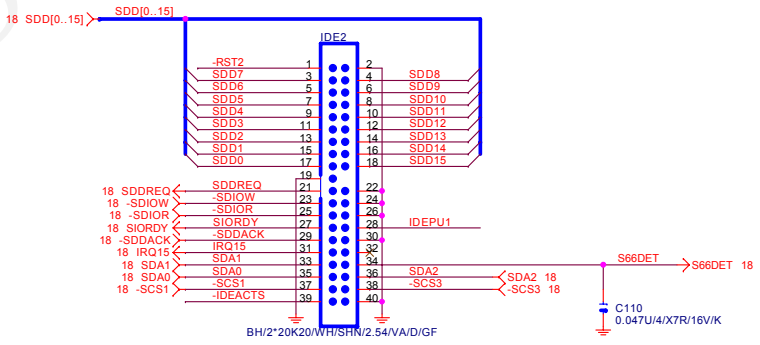

Close to connector

GIGABYTE

Title	IDE CONNECTOR	
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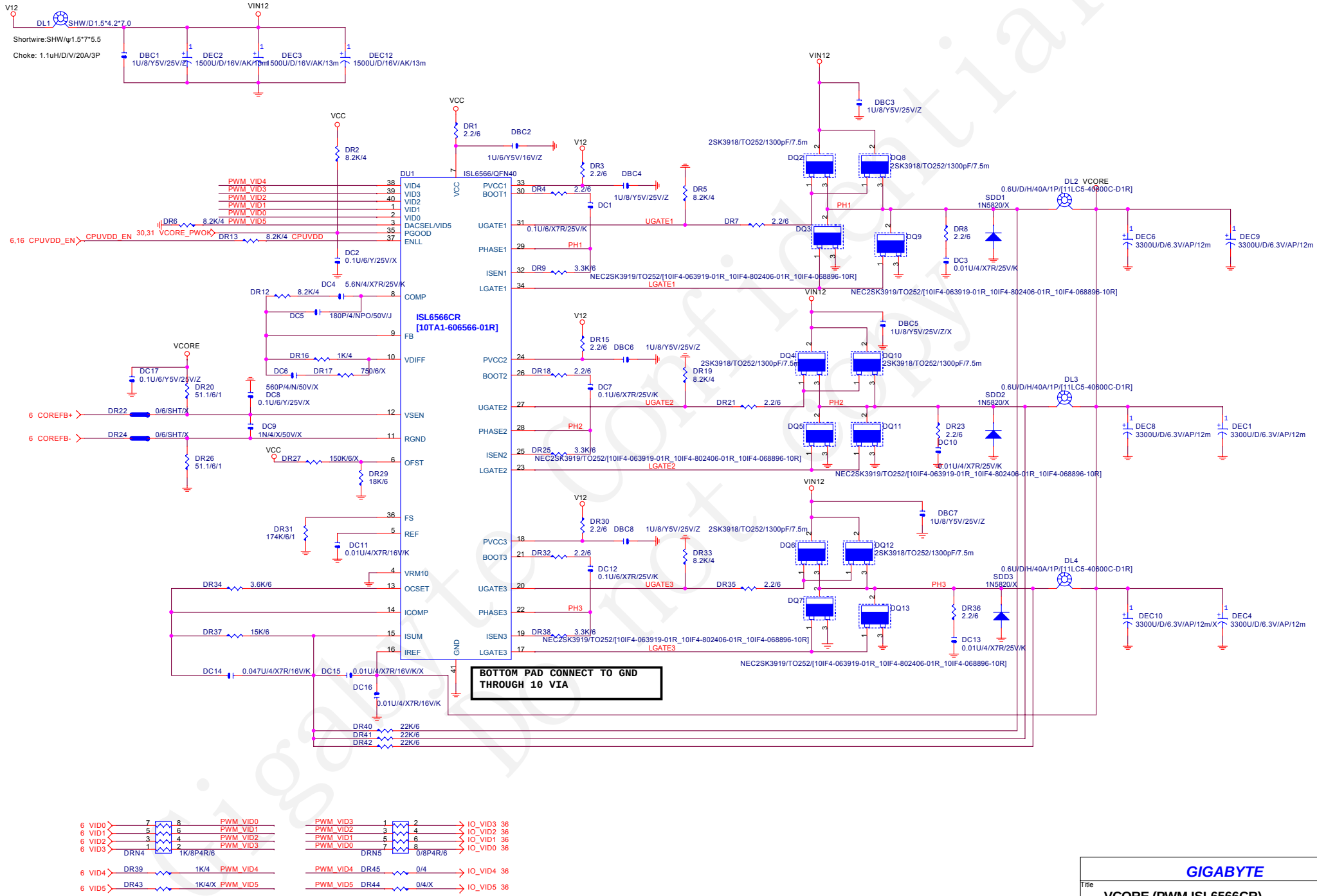
ISL6566CR
[10TA1-606566-01R]
ISL6566/QFN40
BOTTOM PAD CONNECT TO GND
THROUGH 10 VIA
NEC2SK3919/TO252/[10IF4-063919-01R_10IF4-802406-01R_10IF4-068896-10R]
2SK3918/TO252/1300pF/7.5m
GIGABYTE
VCORE (PWM ISL6566CR)
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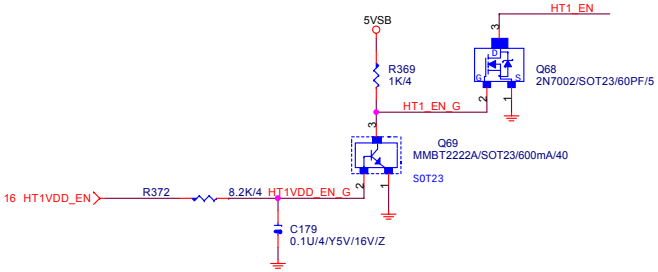

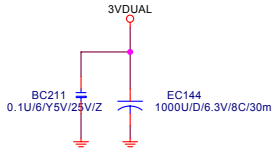

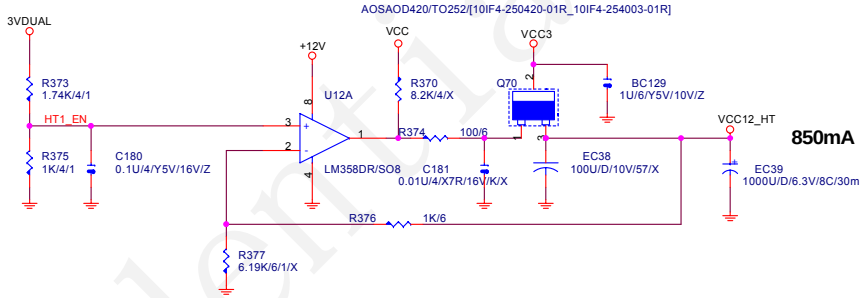

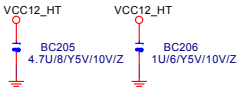

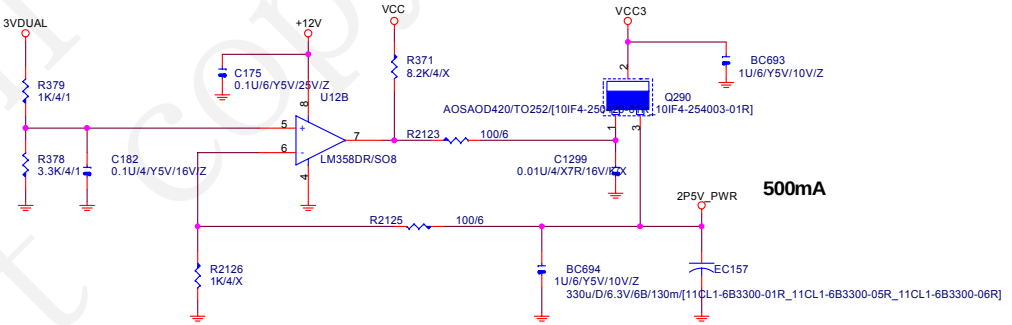

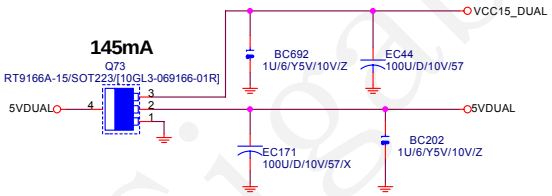

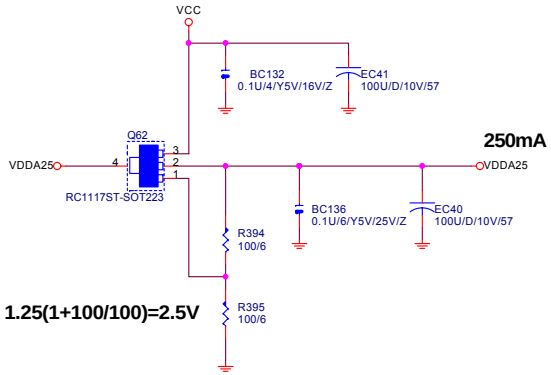

Title	VCC12HT,VDDA25 POWER	
Size	Document Number GA-M51GM-S2G	Rev 1.2
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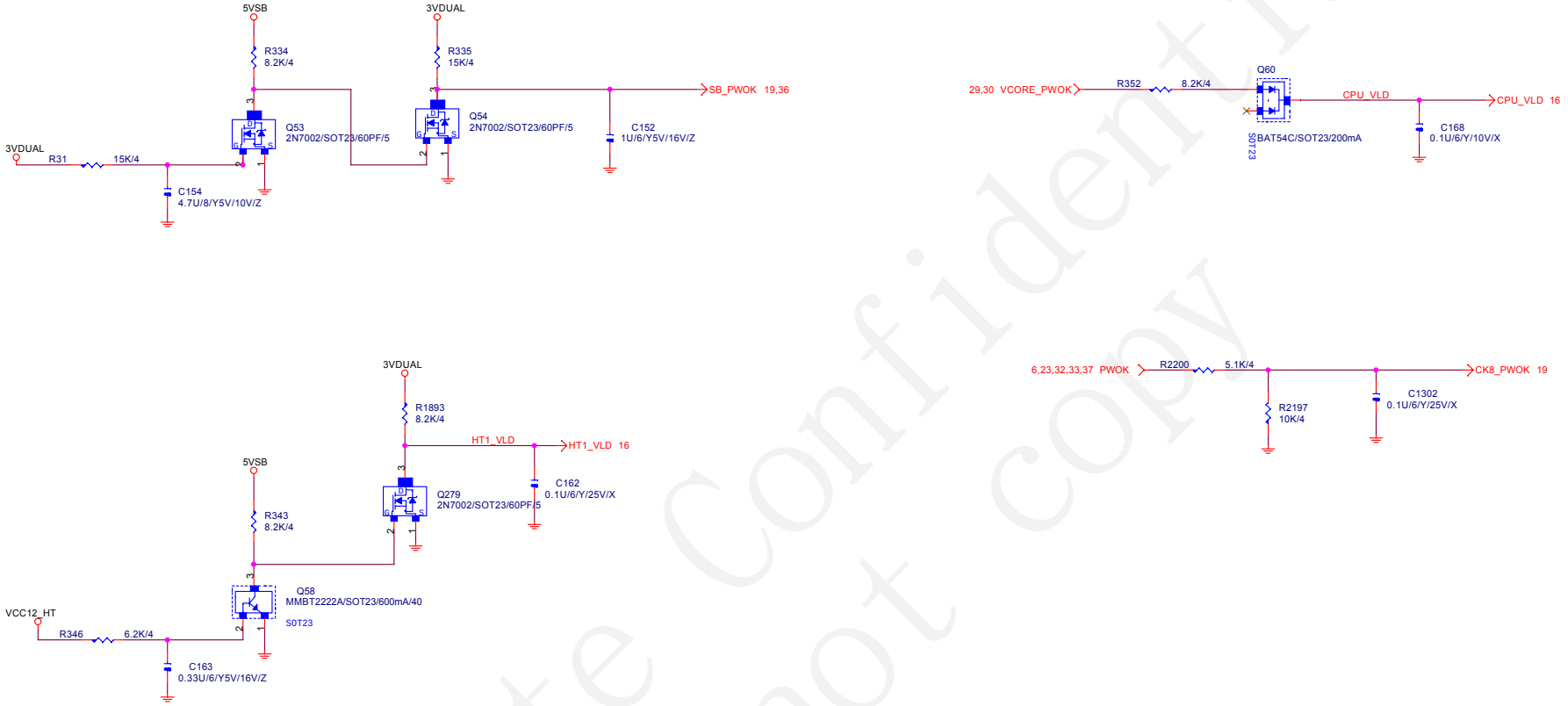

Title	POWER SEQUENCE	
Size	Document Number GA-M51GM-S2G	Rev 1.2
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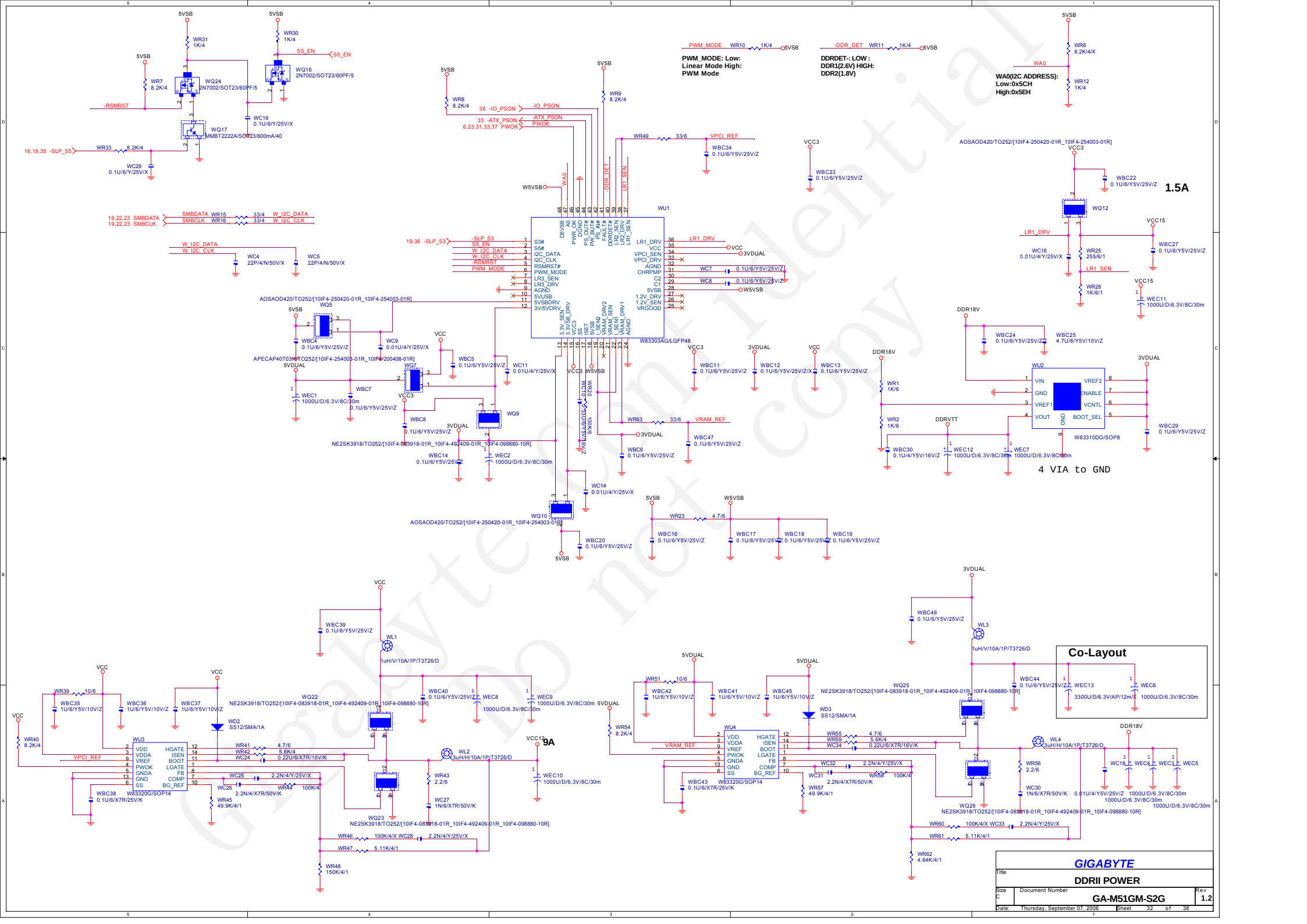
PWM_MODE: Low:
Linear Mode High:
PWM Mode
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
4 VIA to GND
9A
Co-Layout
W83303AG/LQFP48
W83310DG/SOP8
W83320G/SOP14
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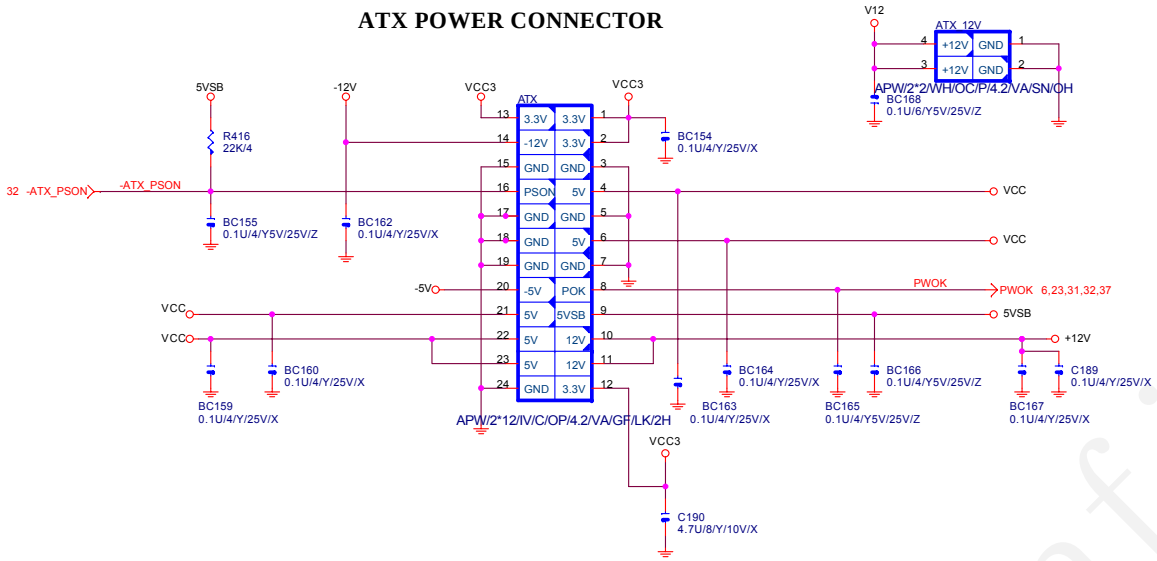
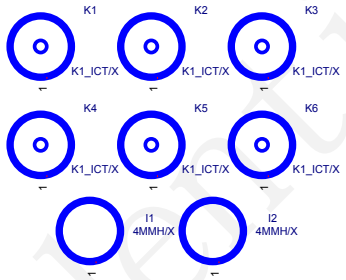
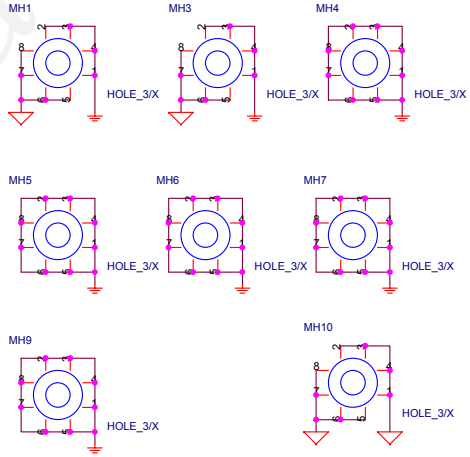
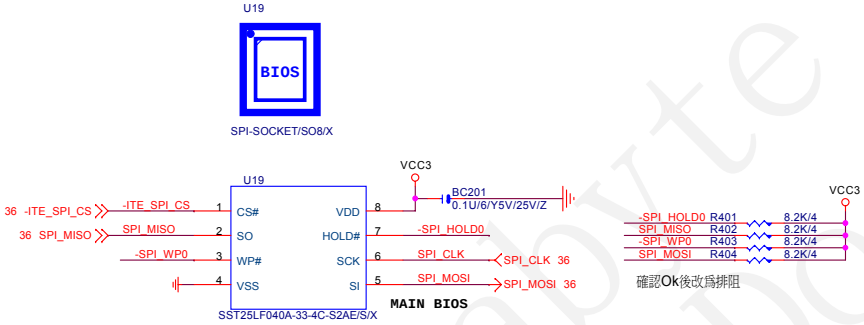
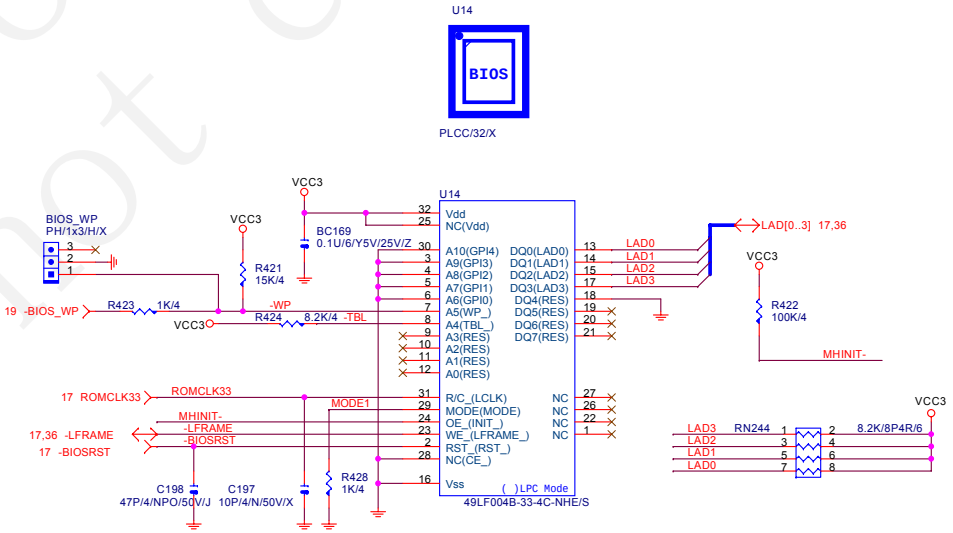
ATX POWER CONNECTOR











GIGABYTE

Title	ATX CONN & BIOS	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
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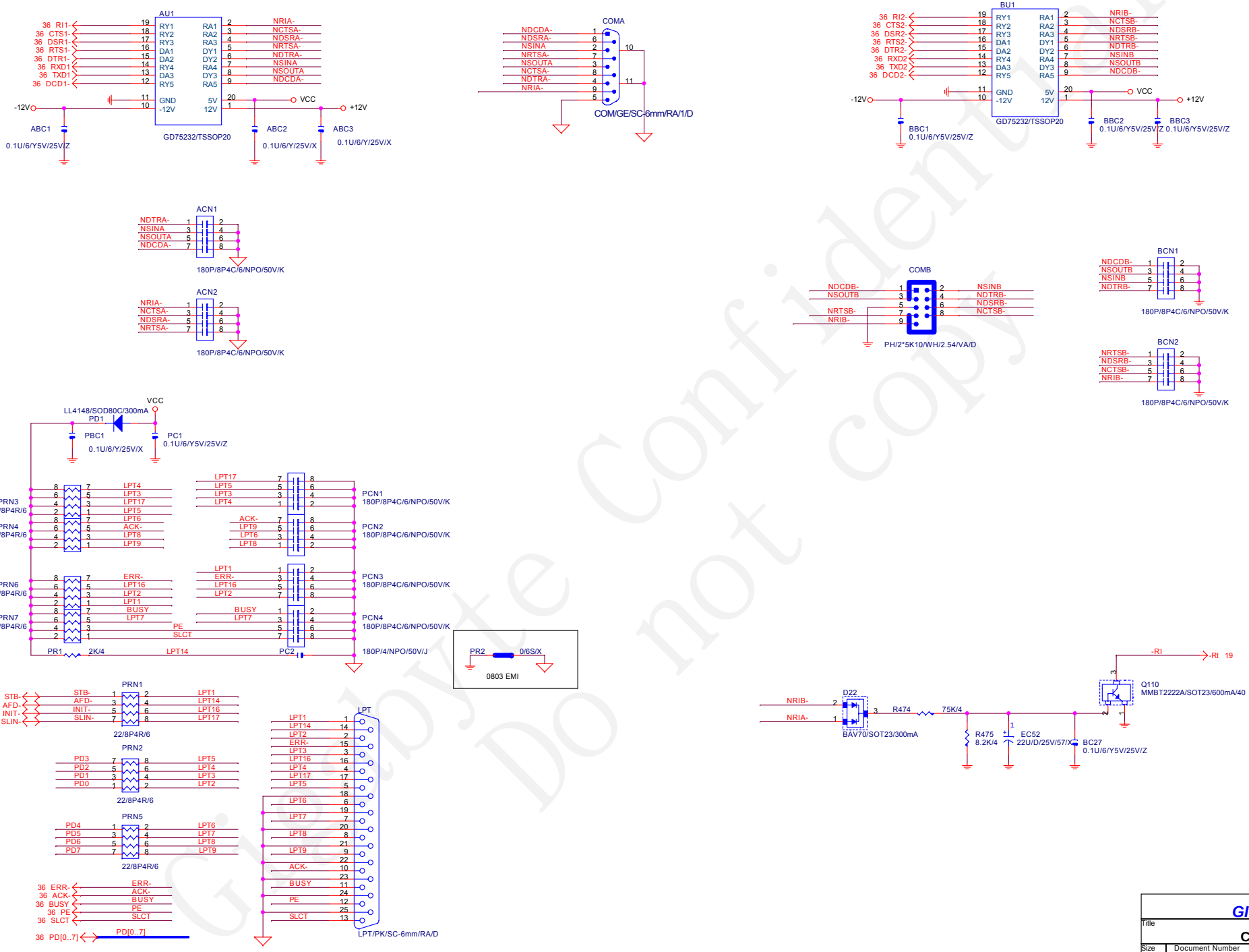

GIGABYTE		
Title	COM/LPT	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
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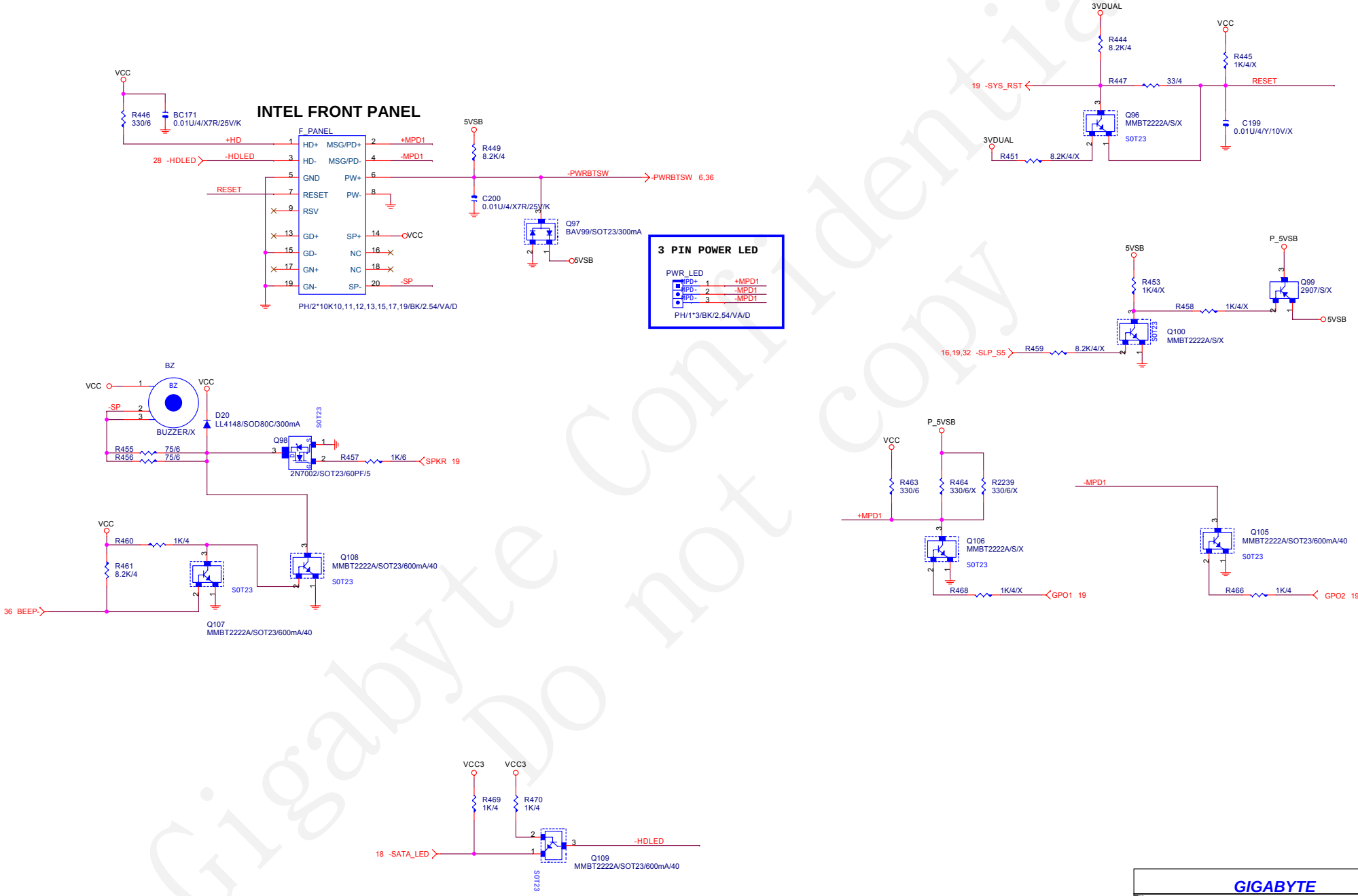

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Title	PANEL & BUZZER	
Size: Custom	Document Number: GA-M51GM-S2G	Rev: 1.2
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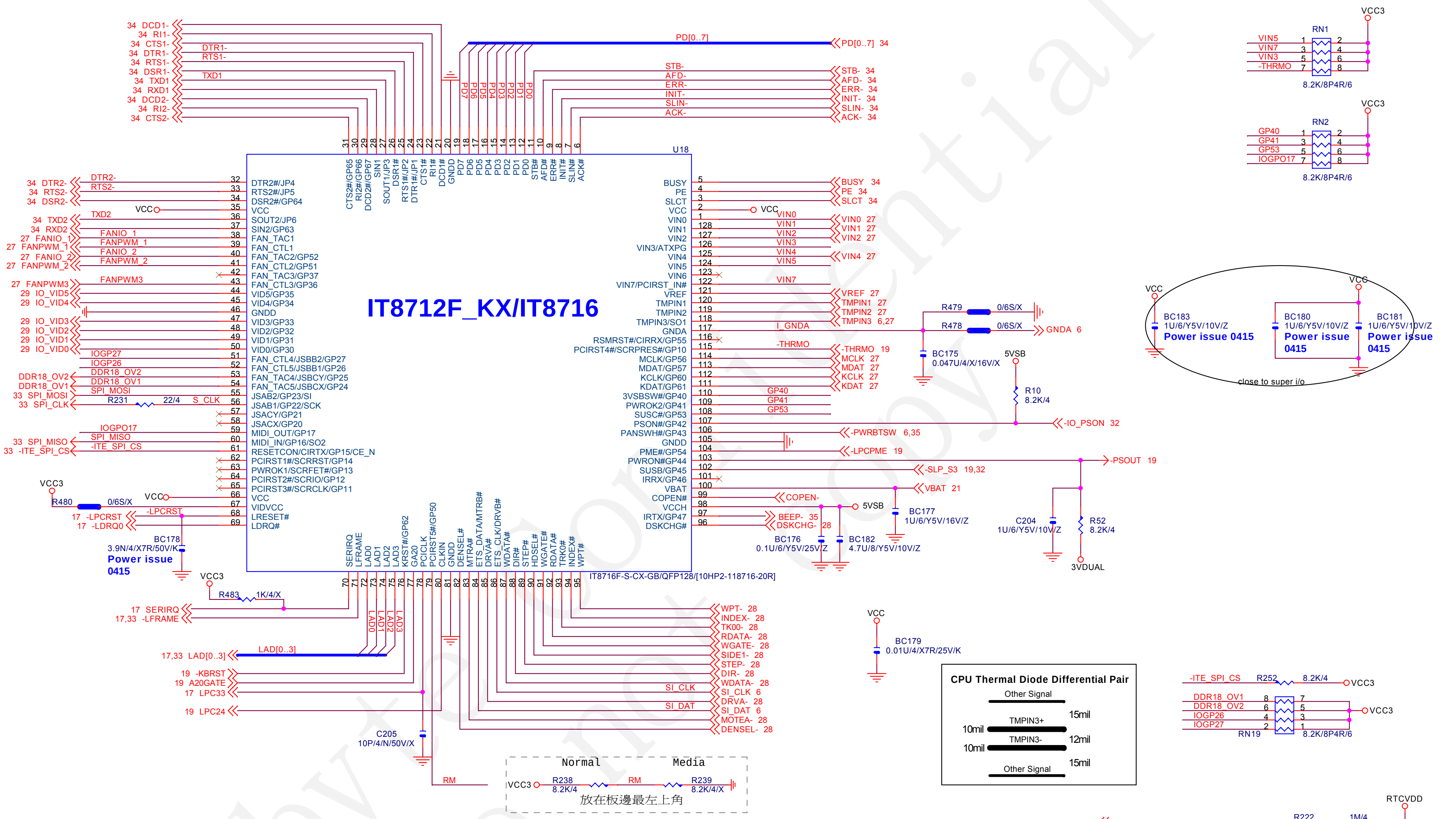
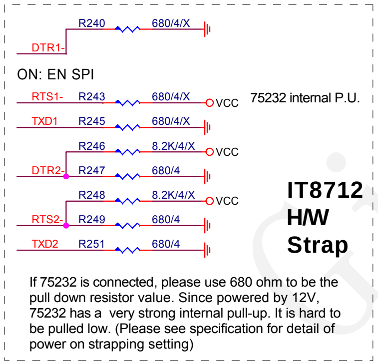




	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

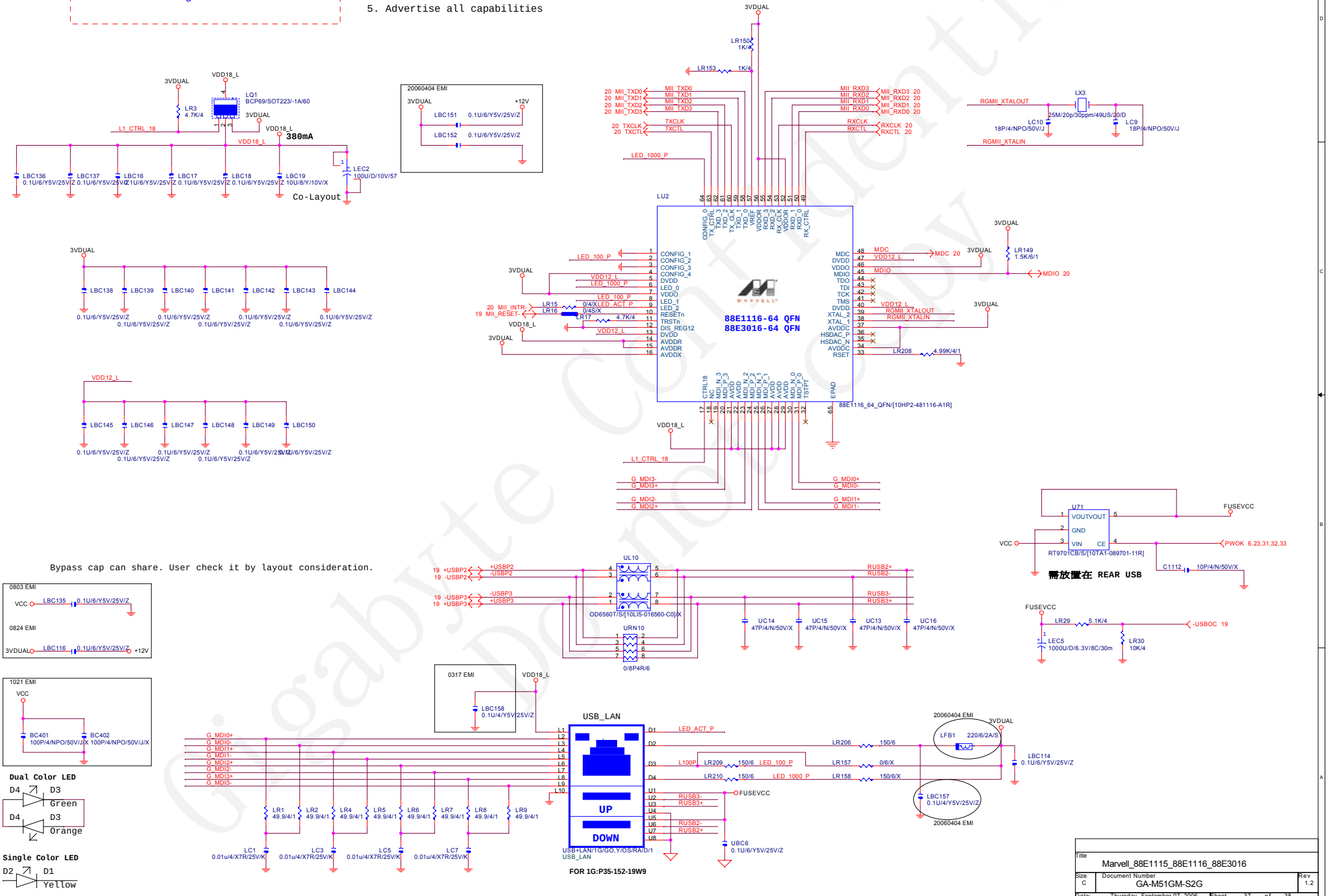
Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

Hardware Configuration: See config _0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



Title	Marvell_88E1115_88E1116_88E3016		
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