

GIGABYTE GA-8PENXP Schematics

Revision 2.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR4,5 CHANNEL B
13	DDR TERMINATION
14	AGP PRO
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	DUAL BIOS
19	CY28405/ICS95203 CLOCK GEN
20	PCI1,2
21	PCI3,4
22	PCI5
23	CODEC
24	AUDIO JACK
25	COM_LPT

SHEET TITLE

26	IDE
27	H/W, FAN
28	KB_PS2, GAME PORT
29	FPANEL
30	USB CONN
31	DDRVTT, DDR25V, 5VDUAL, VDDQ, VCCVID, 3VDUAL
32	VCORE POWER
33	DUAL POWER-1
34	DUAL POWER-2
35	CSA KENAI II+ KINNERITH-1
36	CSA KENAI II+ KINNERITH-2
37	CSA KENAI II+ KINNERITH-3
38	PROMISE PDC20276/ITE8212-1
39	PROMISE PDC20276/ITE8212-2
40	ITE 8712GX
41	ATX , OTHER POWER
42	TI 1394
43	SILICON IMAGE SIL3112 (S-ATA)
44	DDR3,6 CHANNEL B
45	TEST POINT

COMPONENT SIDE
(1 oz. Copper)
VCC SIDE
(1 oz. Copper)
GND SIDE
(1 oz. Copper)
SOLDER SIDE
(1 oz. Copper)

GIGABYTE CORP.

TitleCOVER SHEET

SizeCustomDocument NumberGA-8PENXPRev2.0

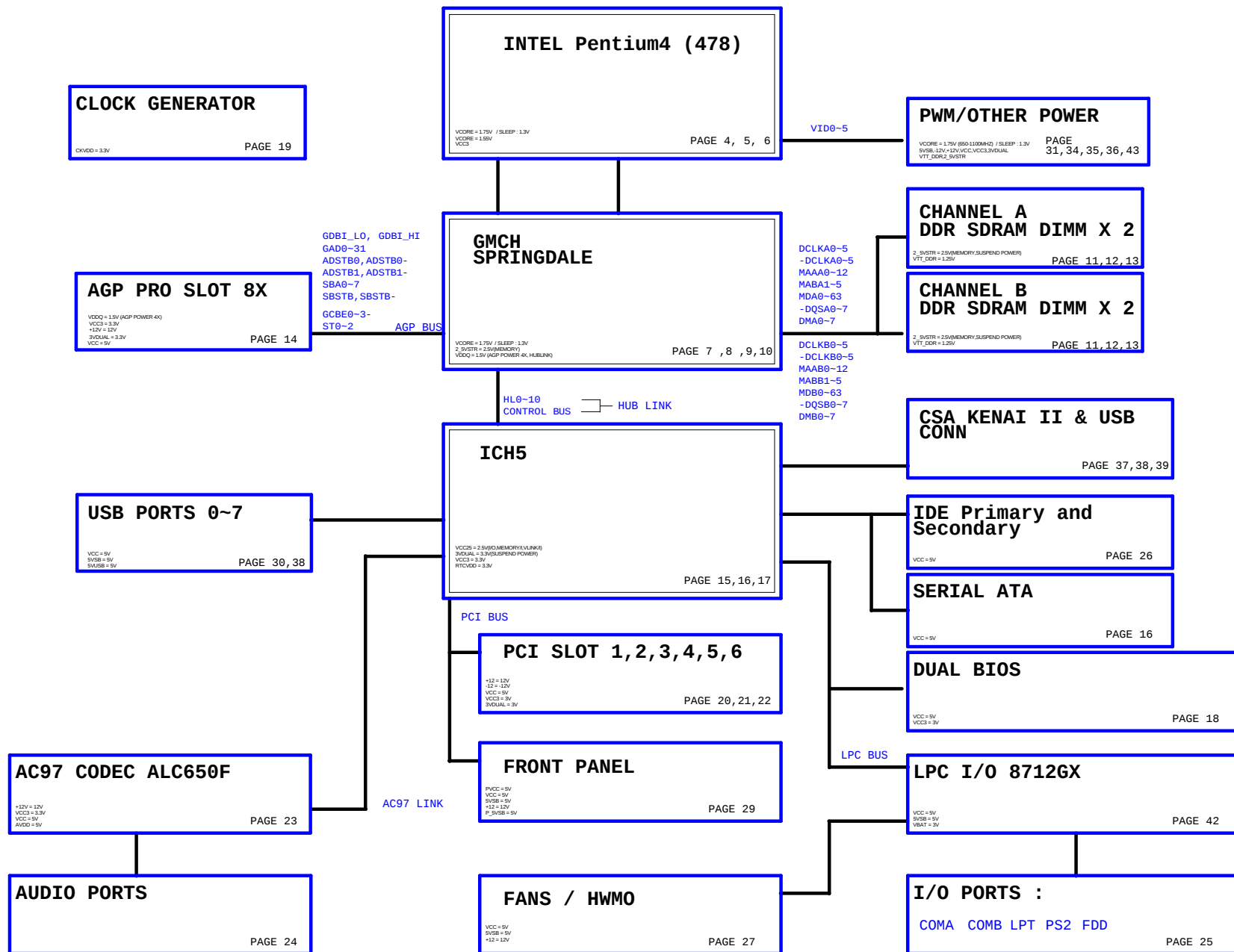
Date:Sheet1 of 45

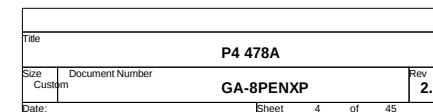
Model Name: GA-8PENXP

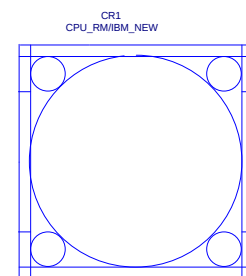
Component history

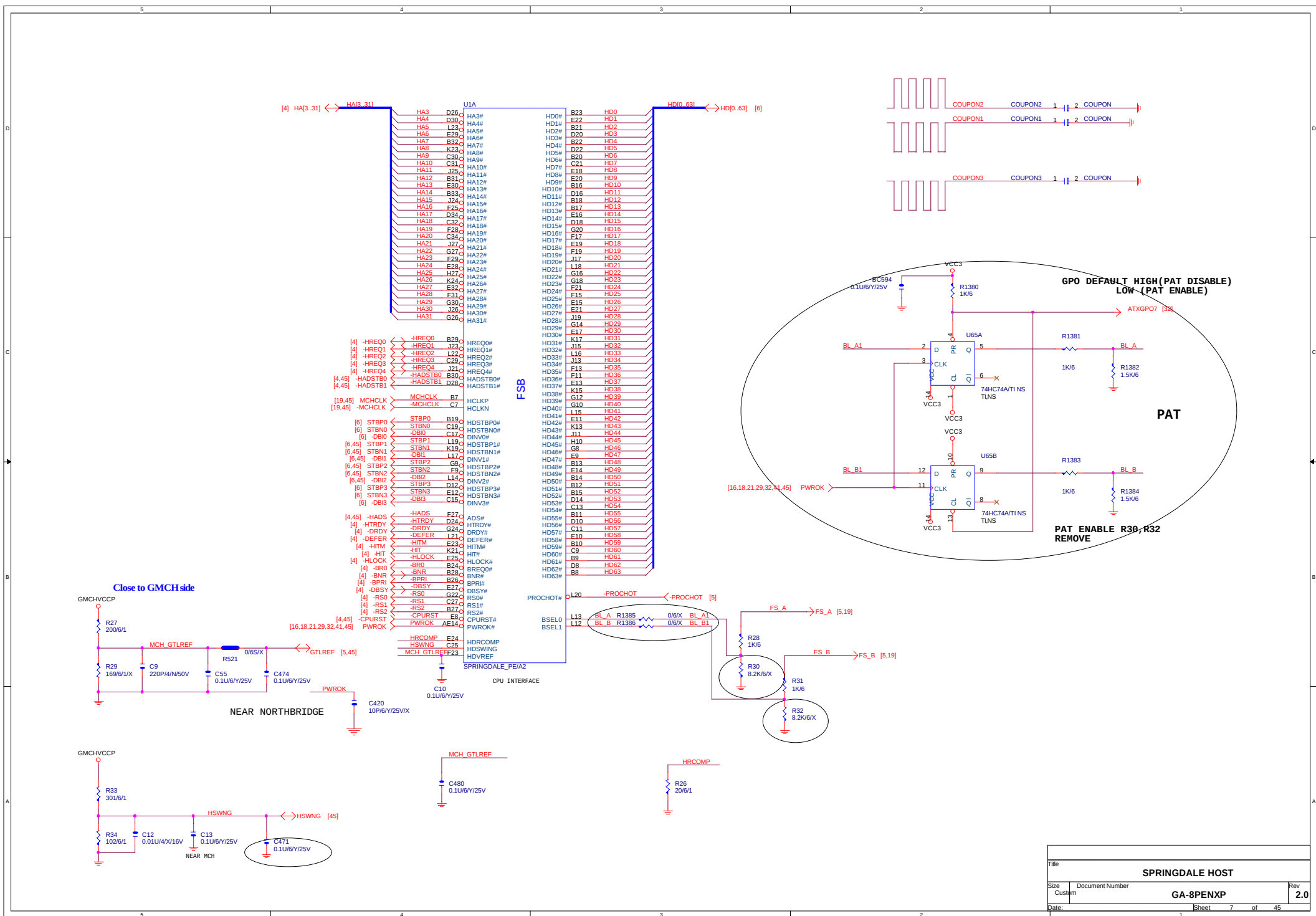
2.0A版修改下列項目					
	PCB TURN 2.0 CLOCK GEN CHANGE TO ICS952635 CODEC CHANGE TO 658 REMOVE R1143,ADD R1144 8.2K				
2.0B版修改下列項目					
	UPDATE ALC658 " C" RESISTOR CHANGE ATXP6 TO ITE8206				
2.0B版 ECN 修改下列項目					
	CPU 電容 COST DOWN , PAT ISSUE UPDATE				
2.0B版 ECN 修改下列項目					
08/12	8212 CX & ICH5 RESET ISSUE				
2.0C版 修改下列項目					
08/29	DUAL BIOS RESET ISSUE & PRESCOTT SOLUTION				

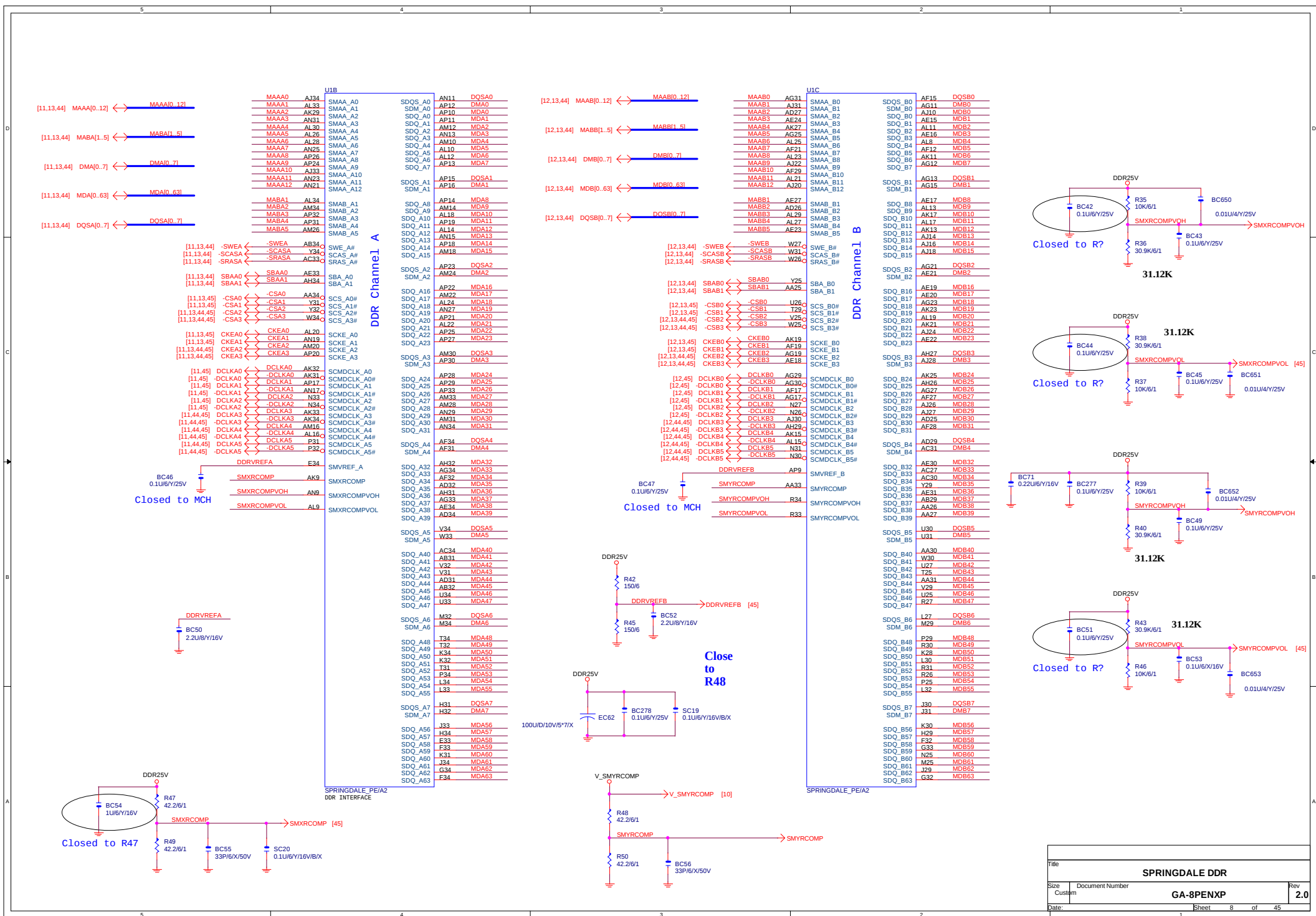
BLOCK DIAGRAM











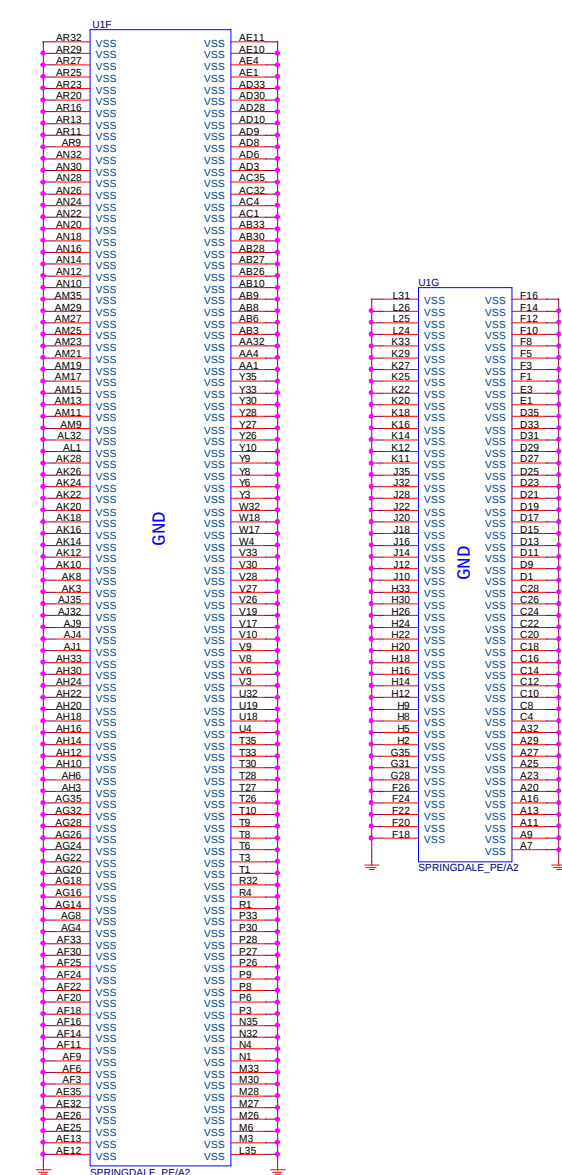
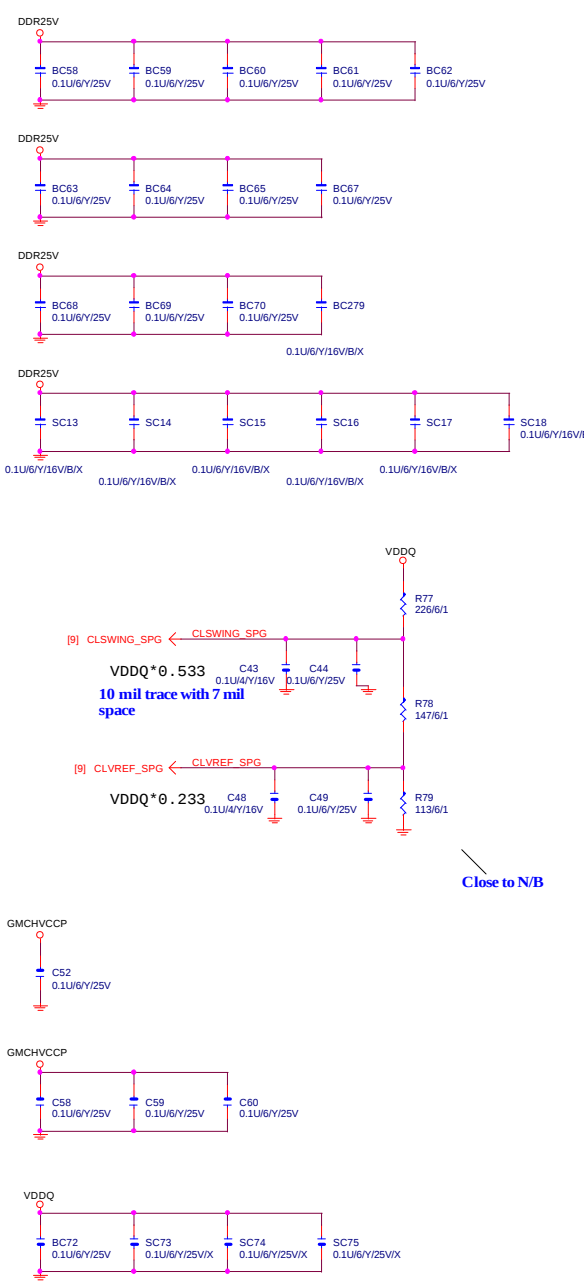
[14] GAD[0..31] <-> GAD[0..31]
[14] SBA[0..7] <-> SBA[0..7]
[15,45] HL[0..10] <-> HL[0..10]

U10
[14] -GCBEO <-> -GCBEO Y7
[14] -GCBE1 <-> -GCBE1 W5
[14] -GCBE2 <-> -GCBE2 AA3
[14] -GCBE3 <-> -GCBE3 U2
[14,45] -GFRAME <-> -GFRAME U6
[19,45] GMCH3V66 <-> GMCH3V66 U4
[14] -GDEVSEL <-> -GDEVSEL AB4
[14] -GIRDY <-> -GIRDY V11
[14] -GTRDY <-> -GTRDY AB5
[14] -GSTOP <-> -GSTOP W11
[14] GPAR <-> GPAR AB2
[14] -GREQ <-> -GREQ N6
[14] -GGNT <-> -GGNT M7

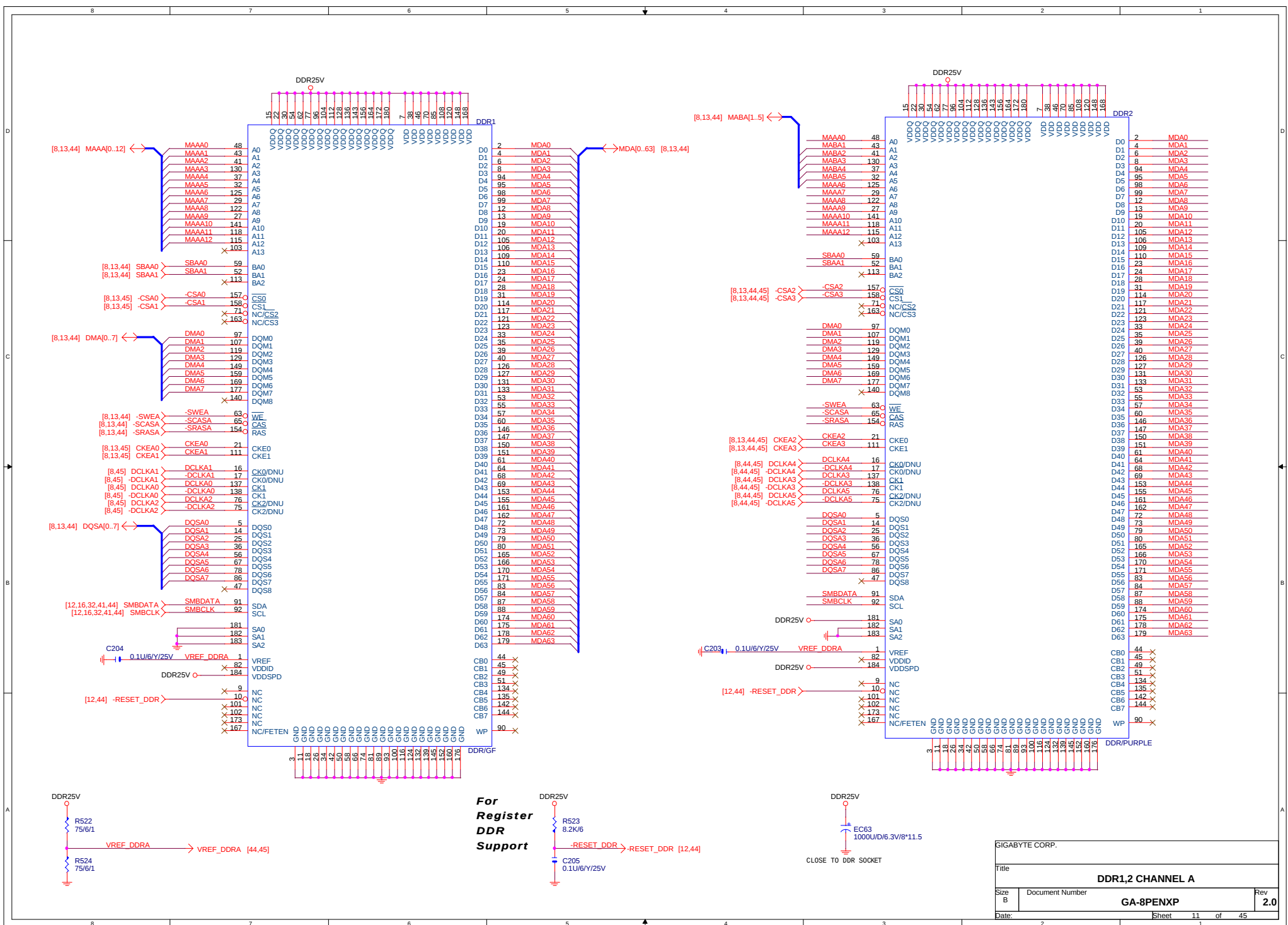
[14,45] GSWING <-> GSWING AC2
[14,45] MCH_AGPREF <-> MCH_AGPREF AC3
[14] -RBF <-> -RBF R10
[14] -WBF <-> -WBF R9
[14] -PIPE <-> -PIPE M4
[14] GDBI_LO <-> GDBI_LO M5
[14] ST0 <-> ST0 N3
[14] ST1 <-> ST1 N5
[14] ST2 <-> ST2 N2

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HL_VREF_MCH AE2
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Title			
SPRINGDALE PWR			
Size	Document Number		Rev
Custom	GA-8PENXP		2.0
Date	1	Sheet 10 of 45	

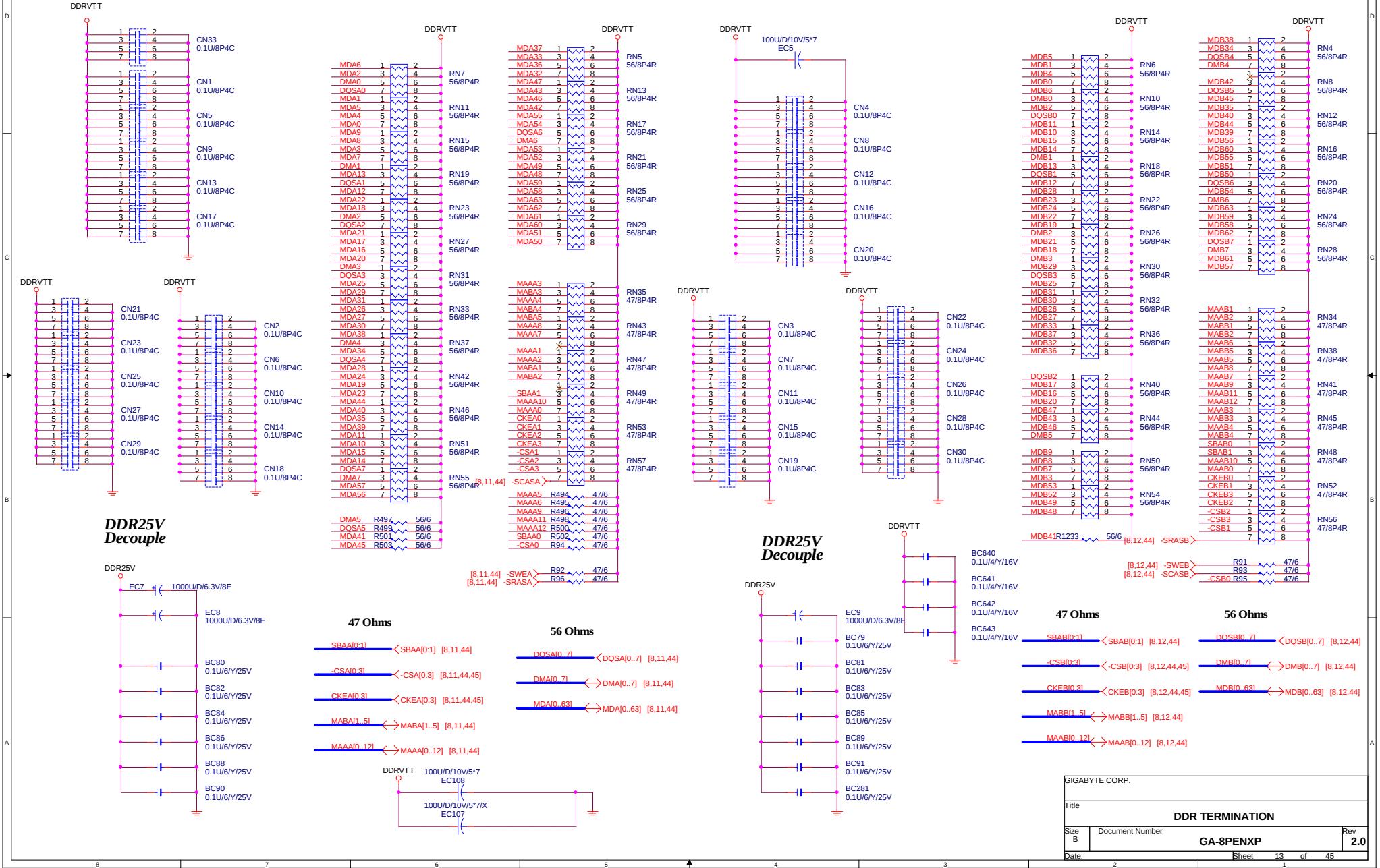


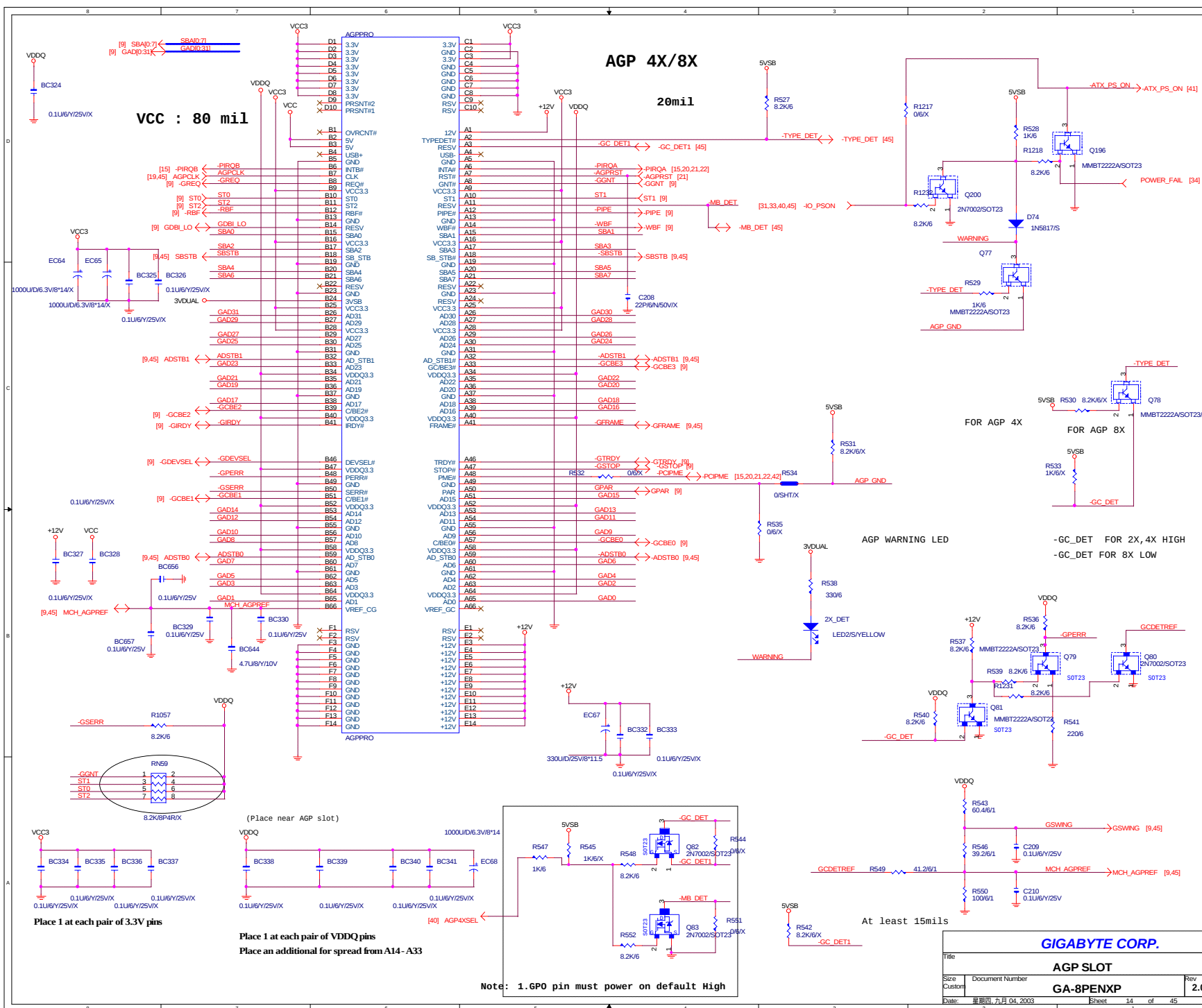
DDRVTT Decouple

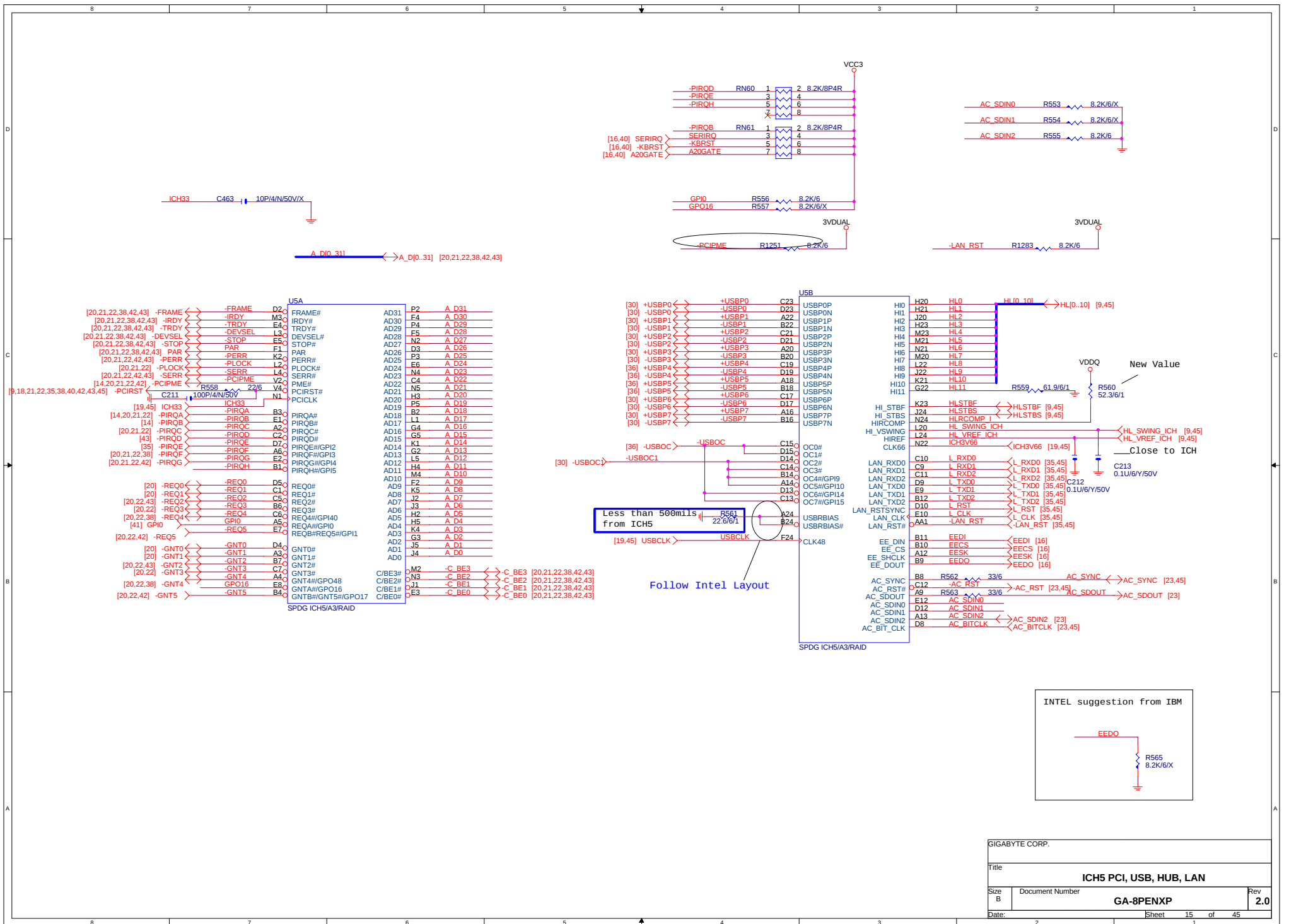
DDR TERMINATION CHANNEL A

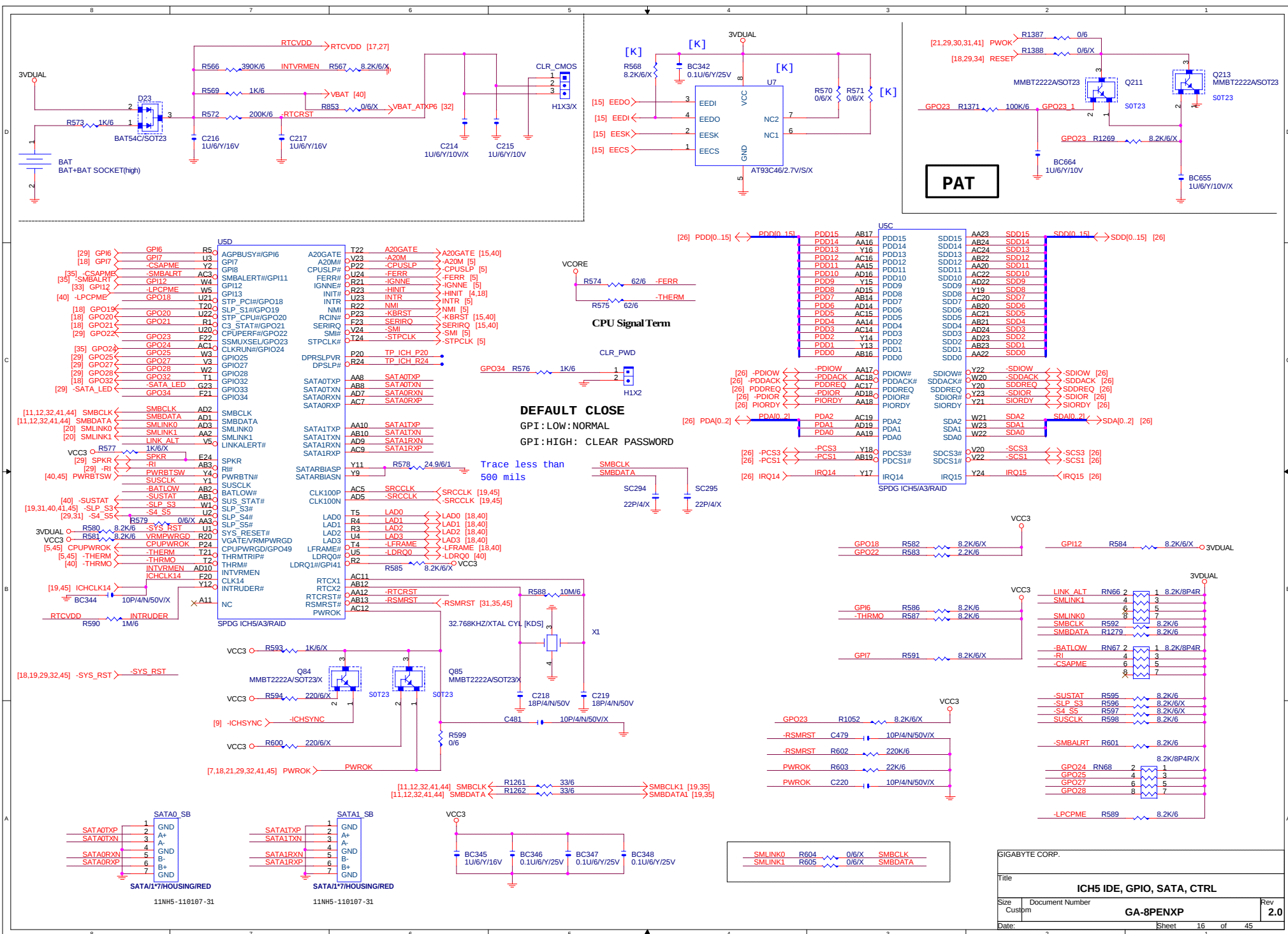
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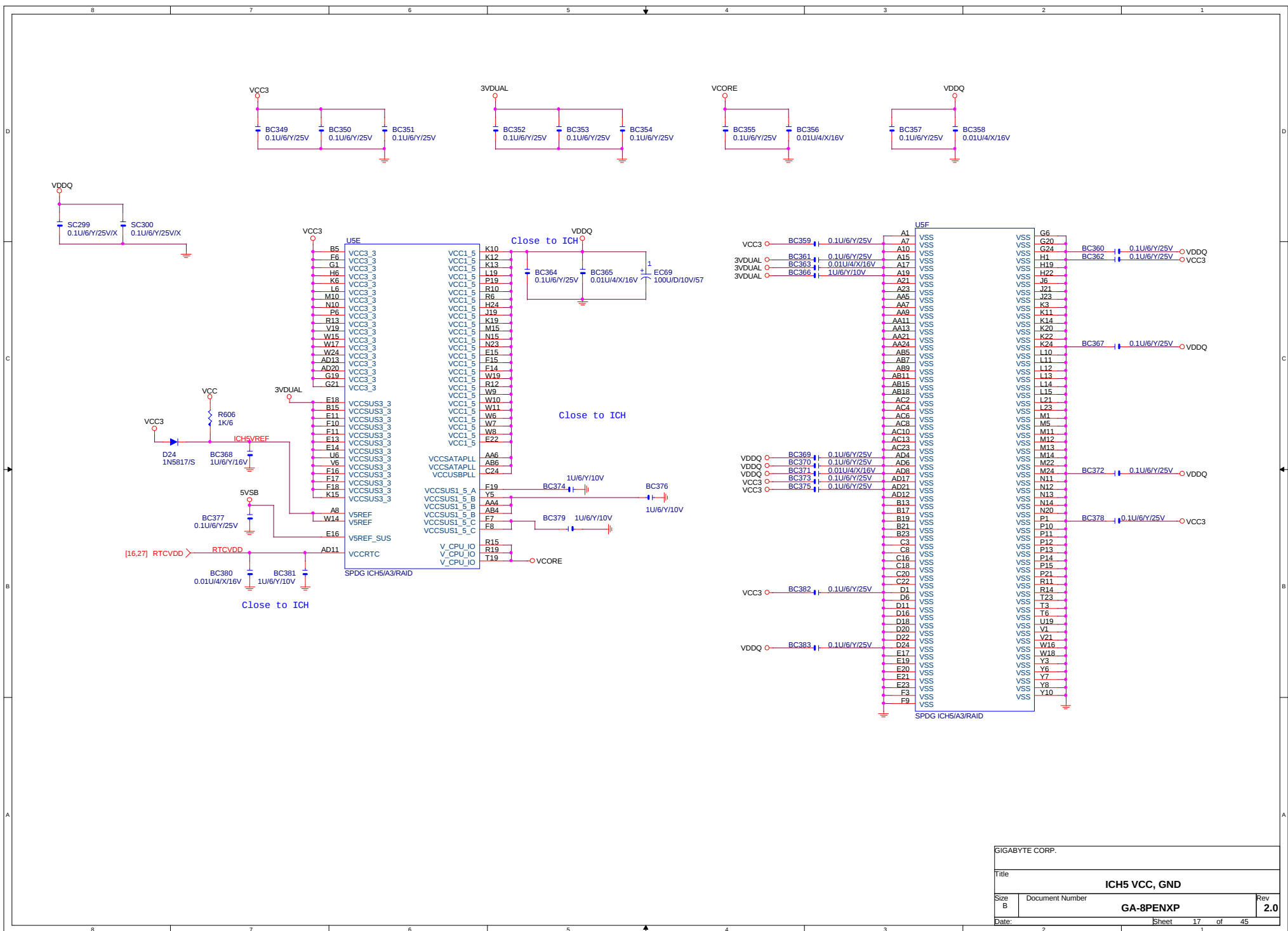
CHANNEL B

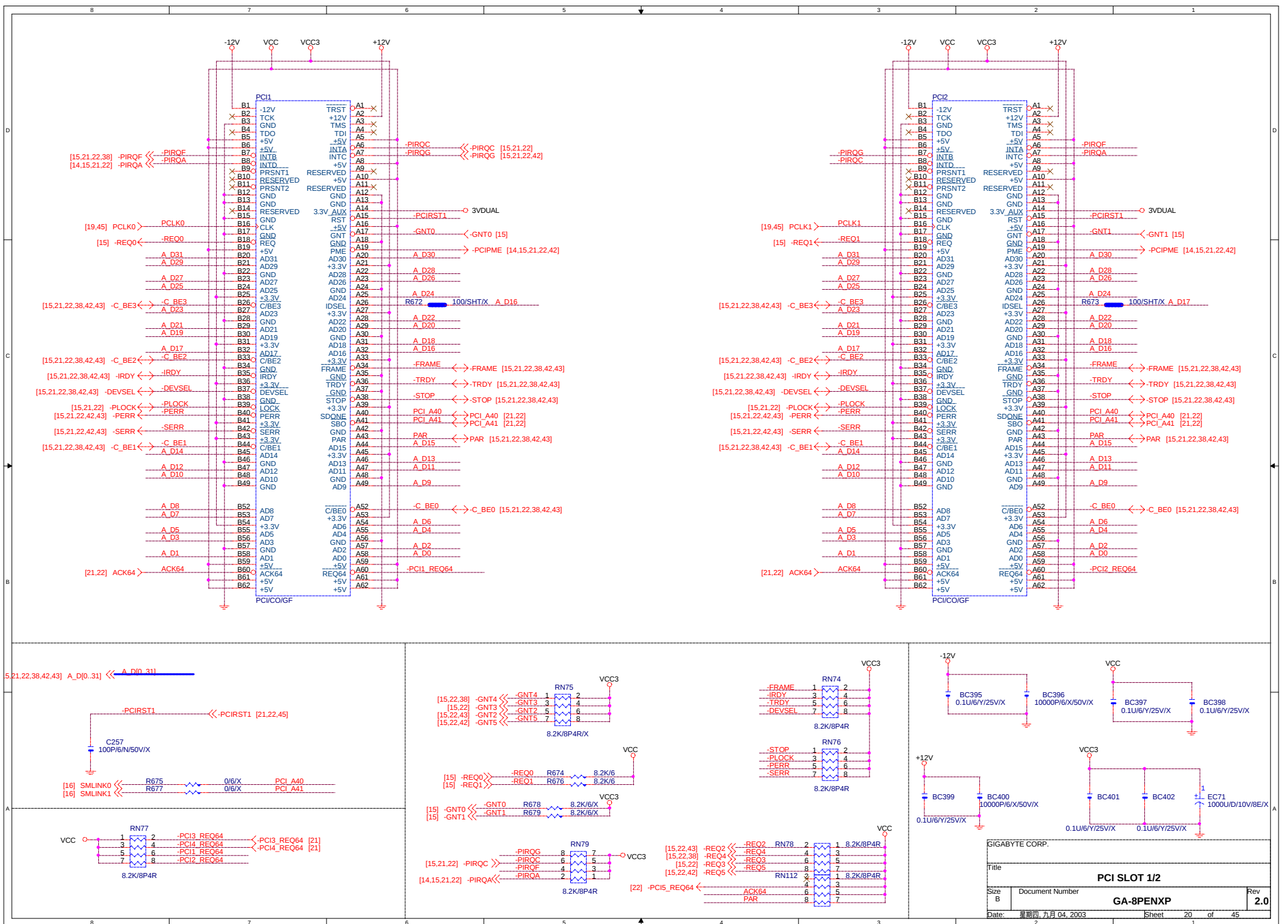


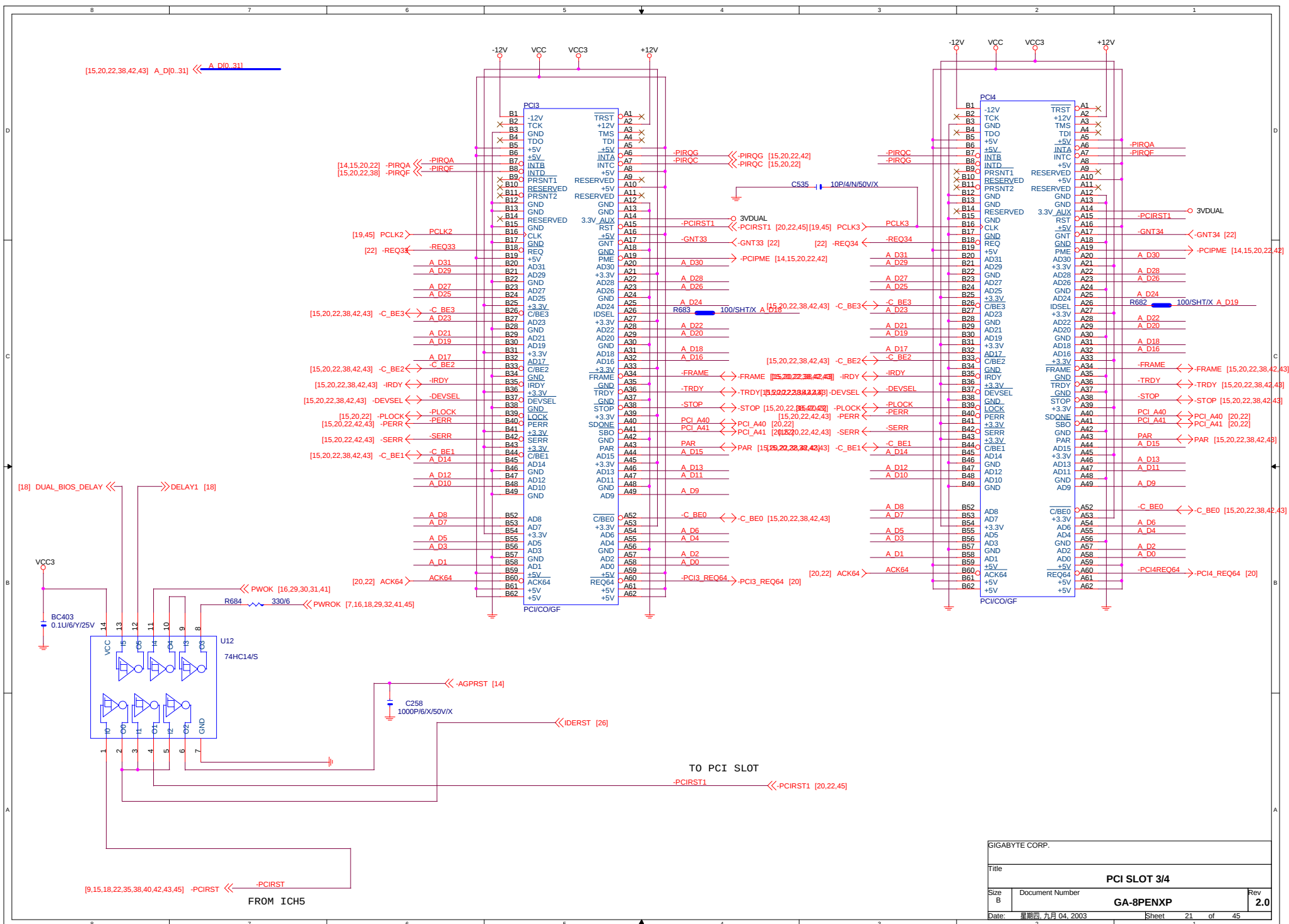


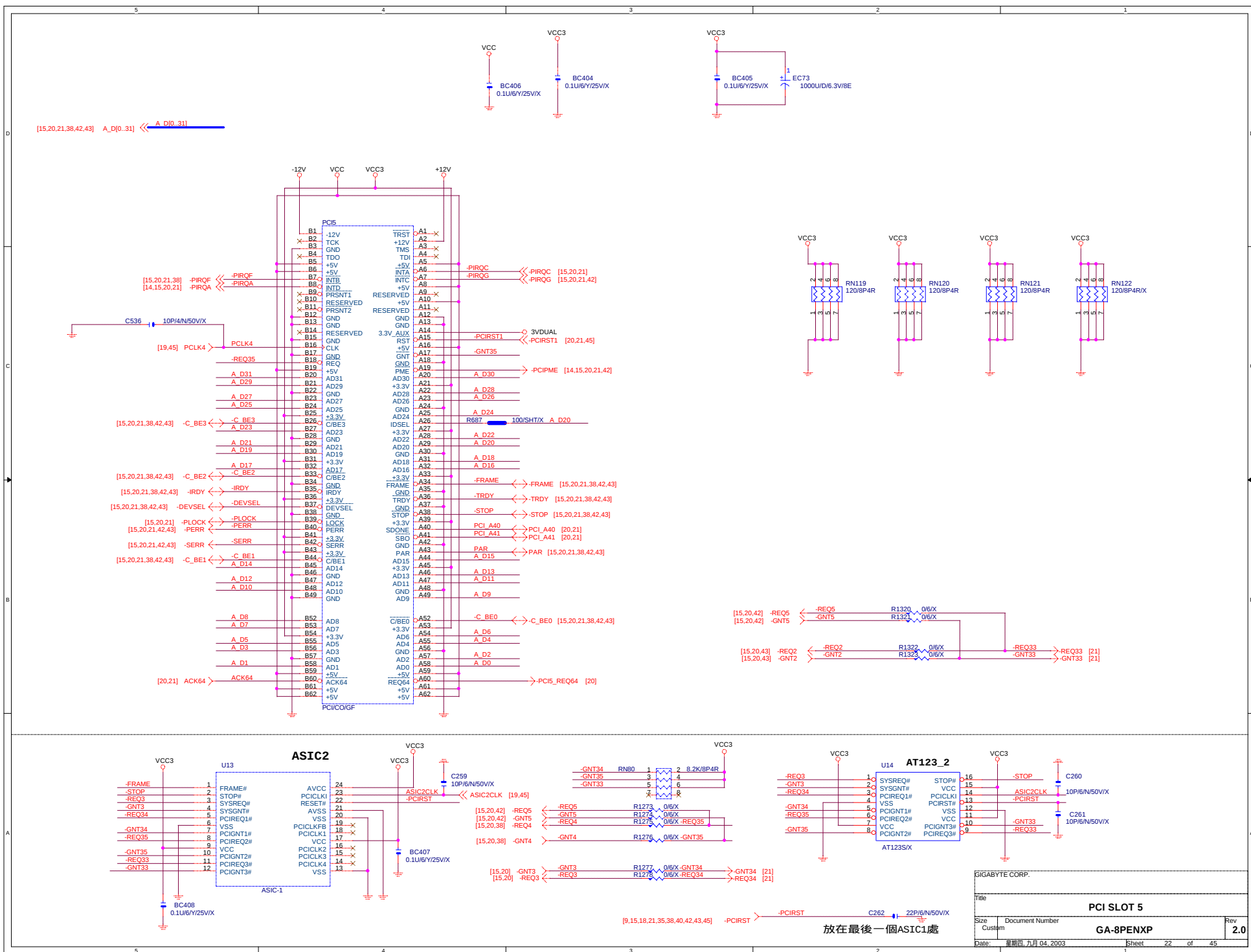




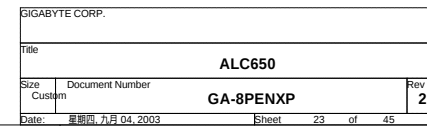




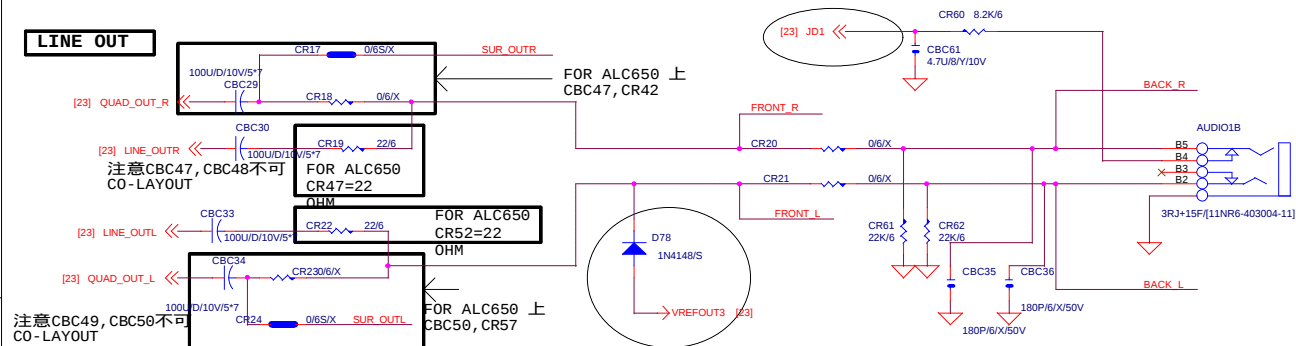




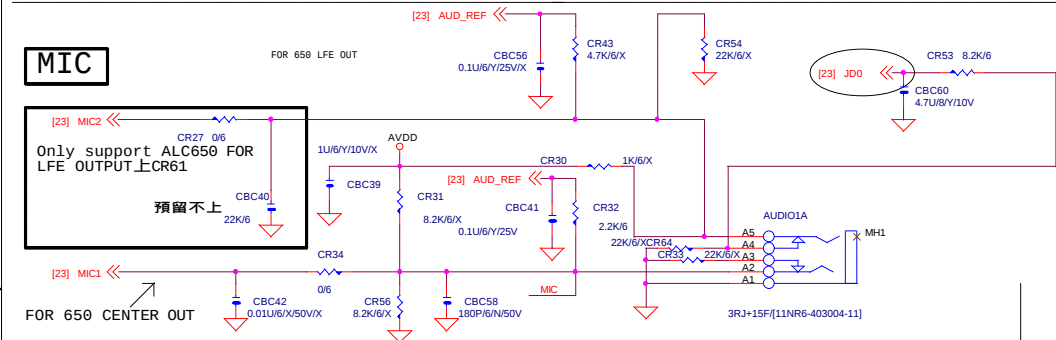
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ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2	
ALC655 Rev C	1000pf	1000pf	1uf	X	
ALC658	X	X	JD4	X	
ALC650	1000pf	1000pf	1uf	1uf	



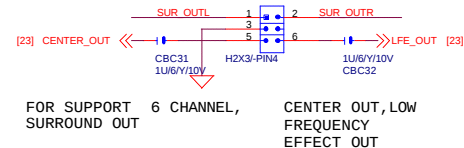
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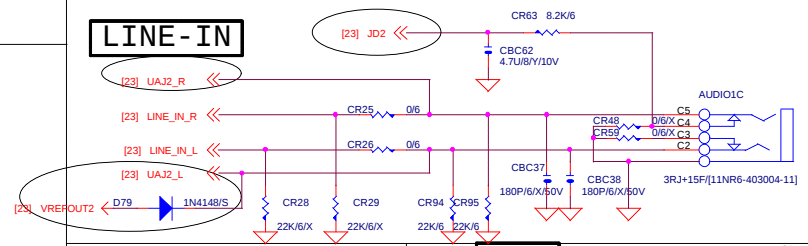
MIC



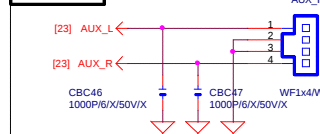
SUR_CEN



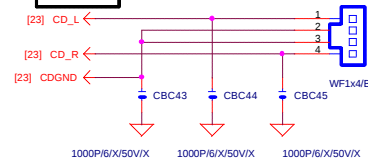
LINE-IN



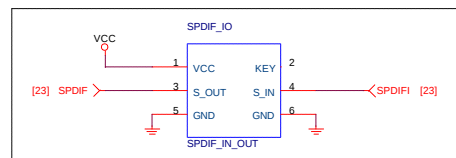
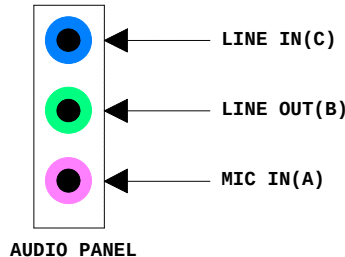
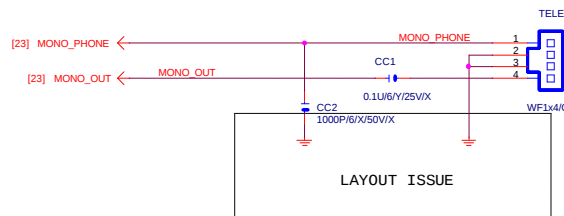
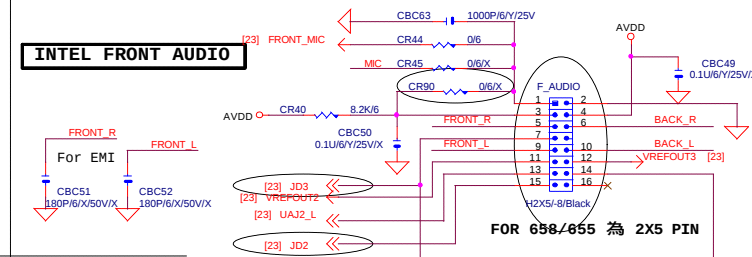
AUX IN DEFAULT NO POP



CD IN

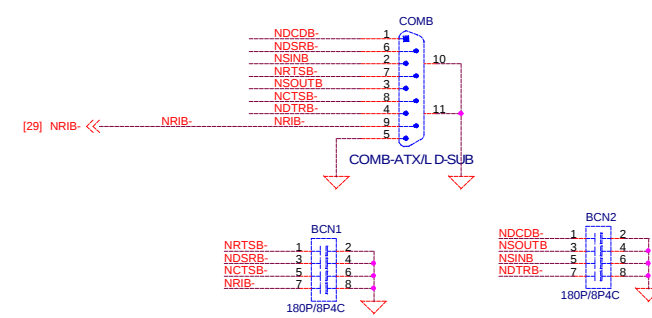
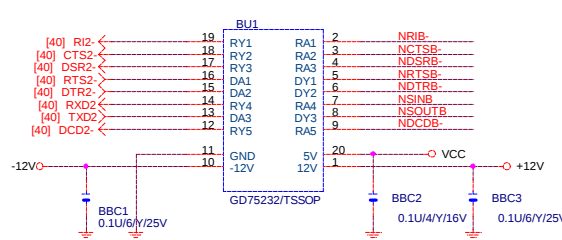
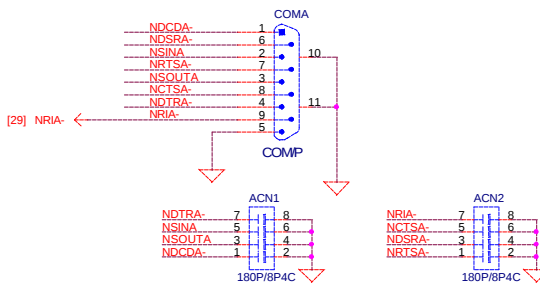
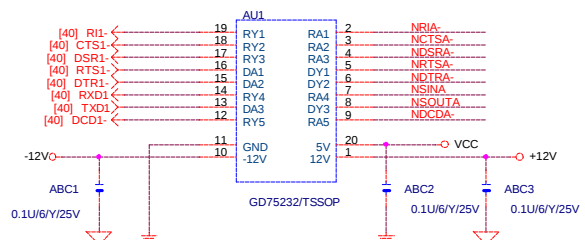


INTEL FRONT AUDIO

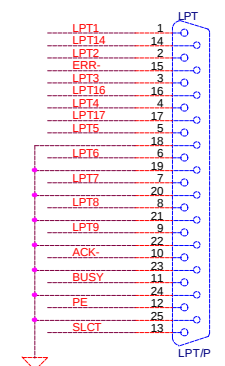
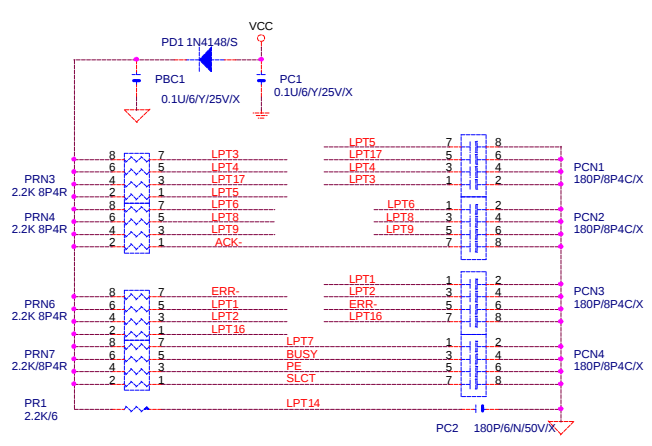
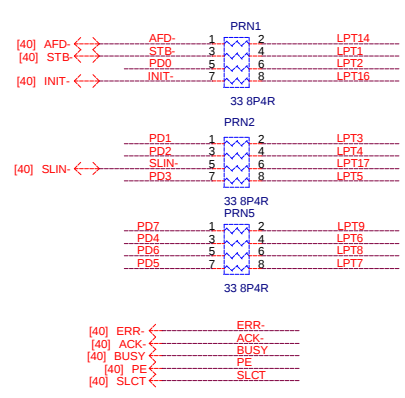


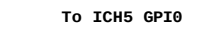
GIGABYTE CORP.

Title			
AUDIO OUTPUT, GAME PORT			
Size	Document Number	Rev	
Custom	GA-8PENXP	2.0	
Date	星期四, 九月 04, 2003	Sheet	24 of 45

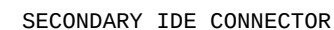


[40] PD[0..7] ↔ PD[0..7]



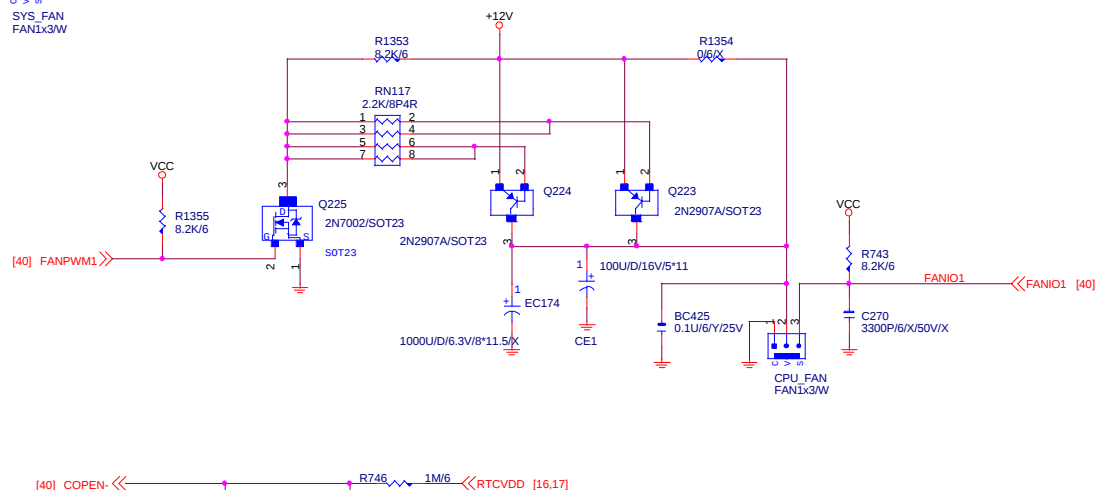
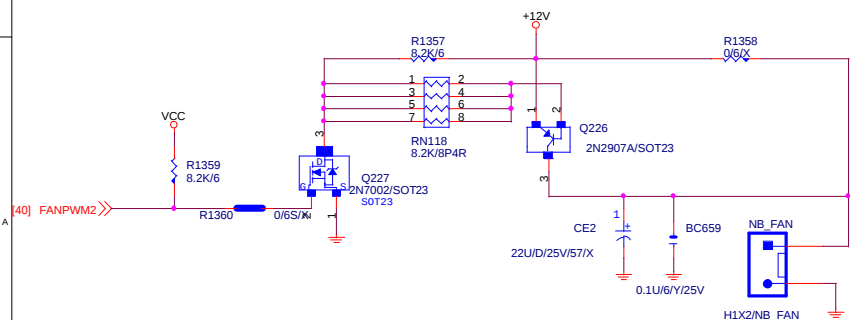
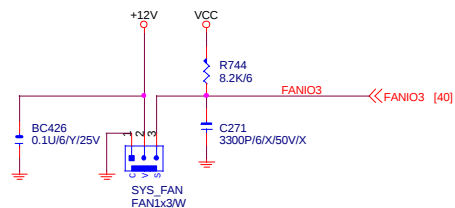
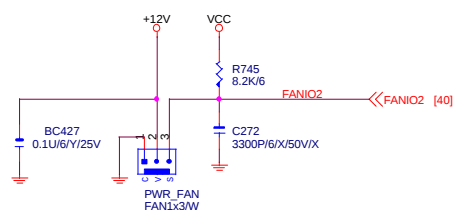
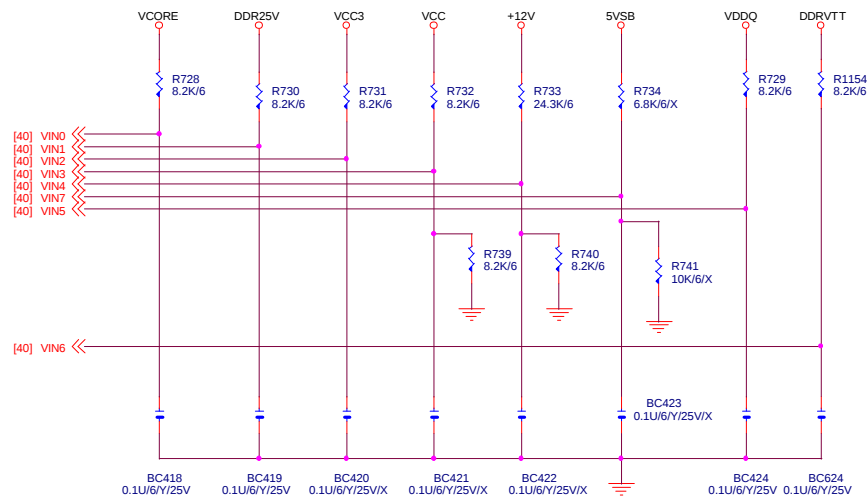
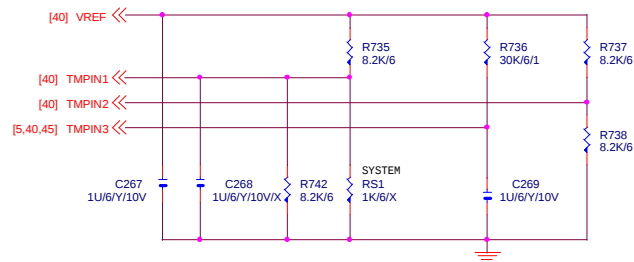


Close to
connector

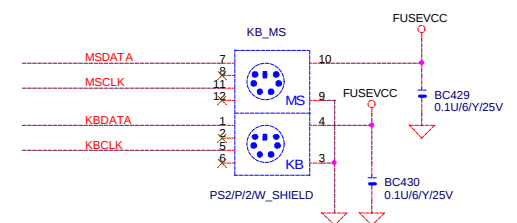
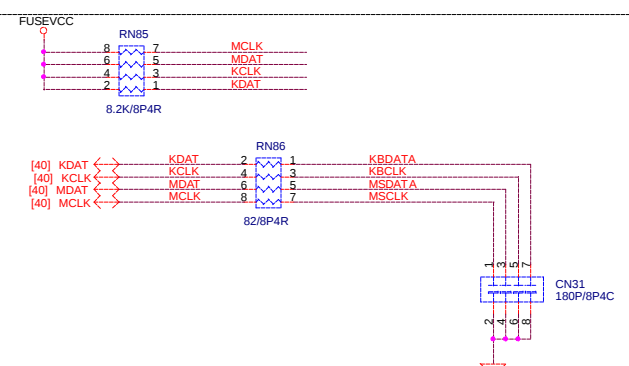
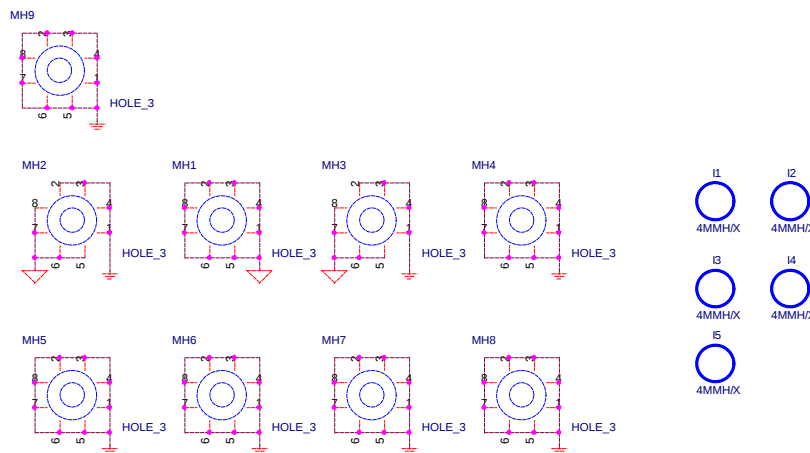
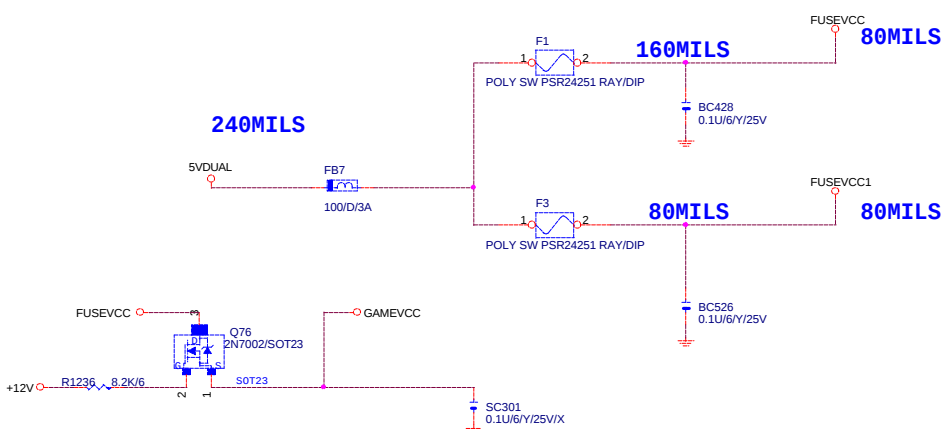


**Close to
connector**

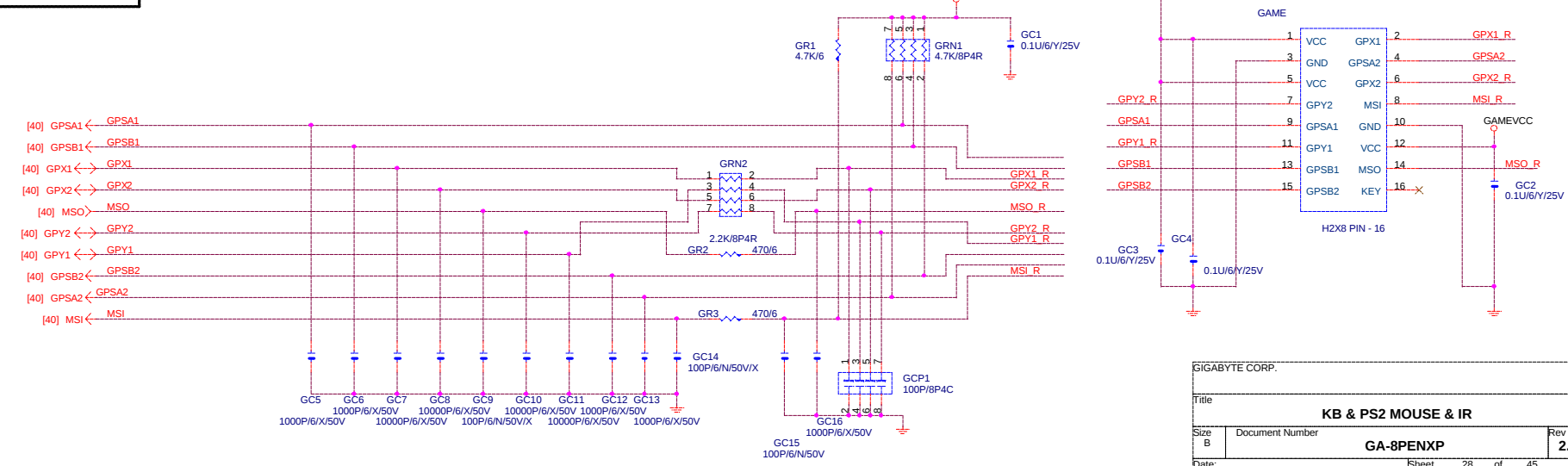
Hardware Monitor circuits



GIGABYTE CORP.			
Title		FAN/HWMO	
Size	Document Number	Rev	
B	GA-8PENXP	2.0	
Date:	量版图, 九月 04, 2003	Sheet	27 of 45



GAME_PORT



INTEL FRONT PANEL

Pad trace same as pad width [16,18,34] RESET

3 PIN POWER LED

PWR_LED 1X3
 +MPD 1 +MPD
 -MPD 2 -MPD
 -MPD 3 -MPD
 P_LED_1X3

DIMM LED

GIGABYTE CORP.

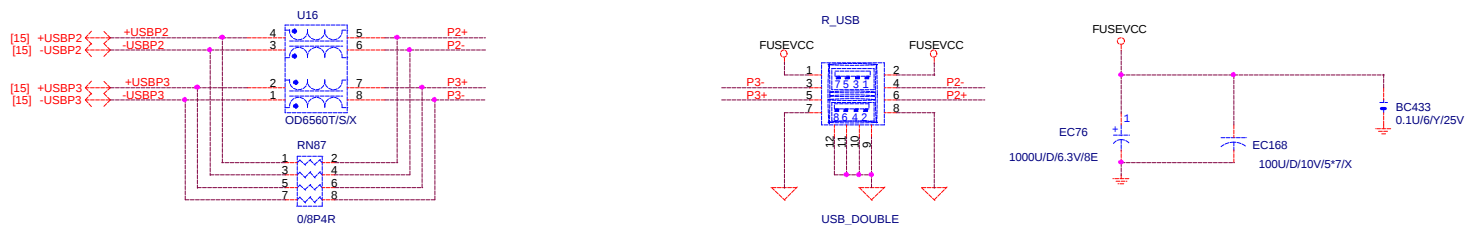
Title
PANEL & STR LED & RI

Size B Document Number
GA-8PENXP

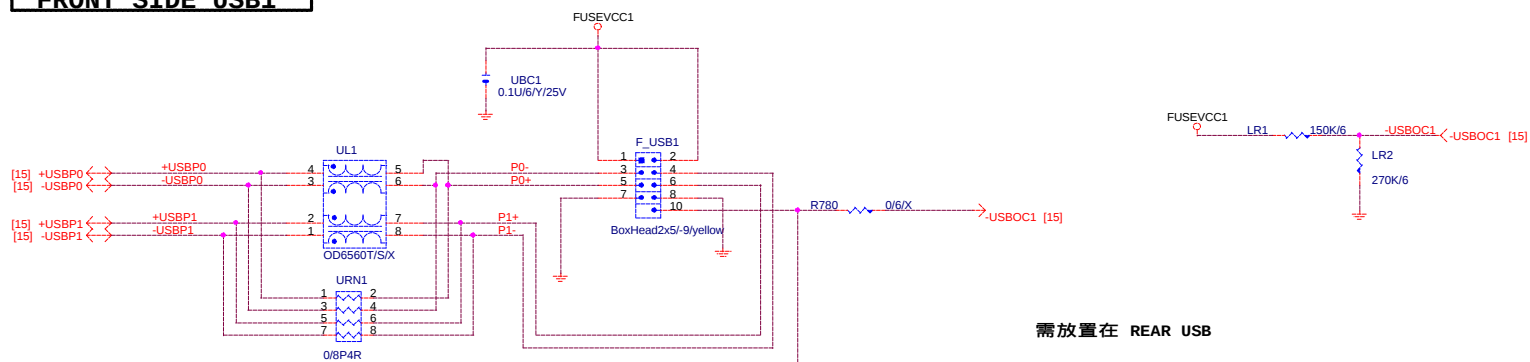
Rev
2.0

Date: Sheet 29 of 45

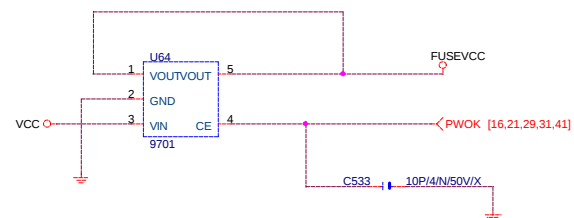
REAR USB



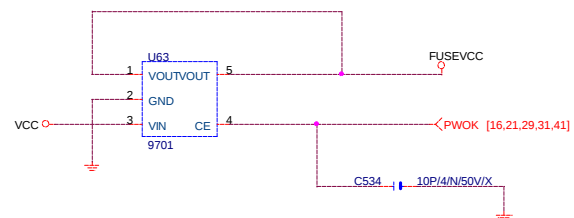
FRONT SIDE USB1



需放置在 REAR USB



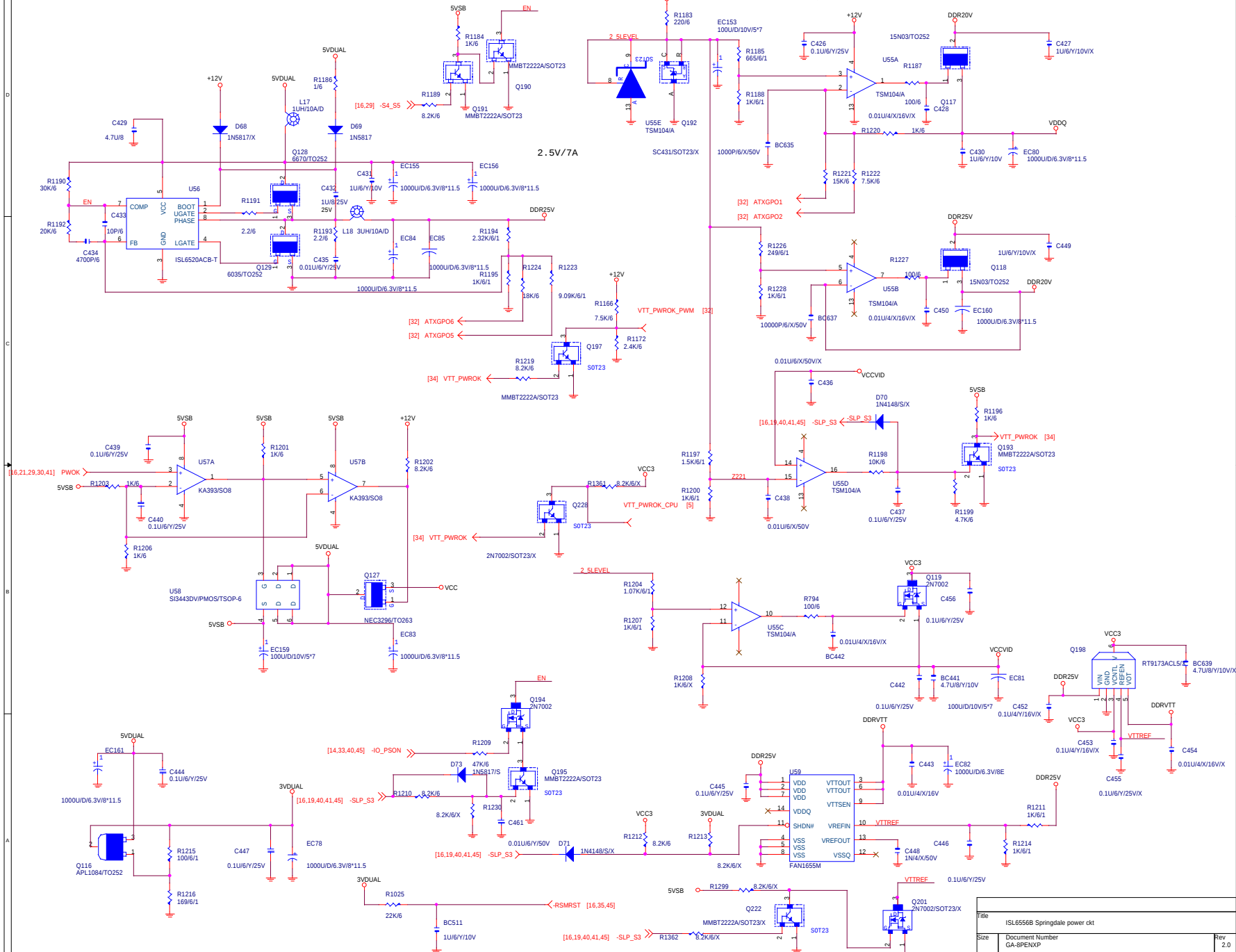
需放置在 REAR USB



GIGABYTE CORP.		
Title		
ICH USB PORT		
Size	Document Number	Rev
B	GA-8PENXP	2.0
Date:	Sheet	30 of 45
	2	1

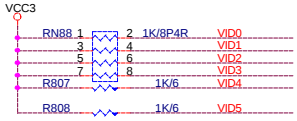
DDR25V FOR DDR DIMM & NB

VDDQ FOR AGP 4X/8X



Title			
ISL6556B Springdale power ckt			
Size	Document Number	Rev	
	GA-8PENXP	2.0	
Date:	星期二, 九月 04, 2003	Sheet	31 of 45

CPU Voltage ID output



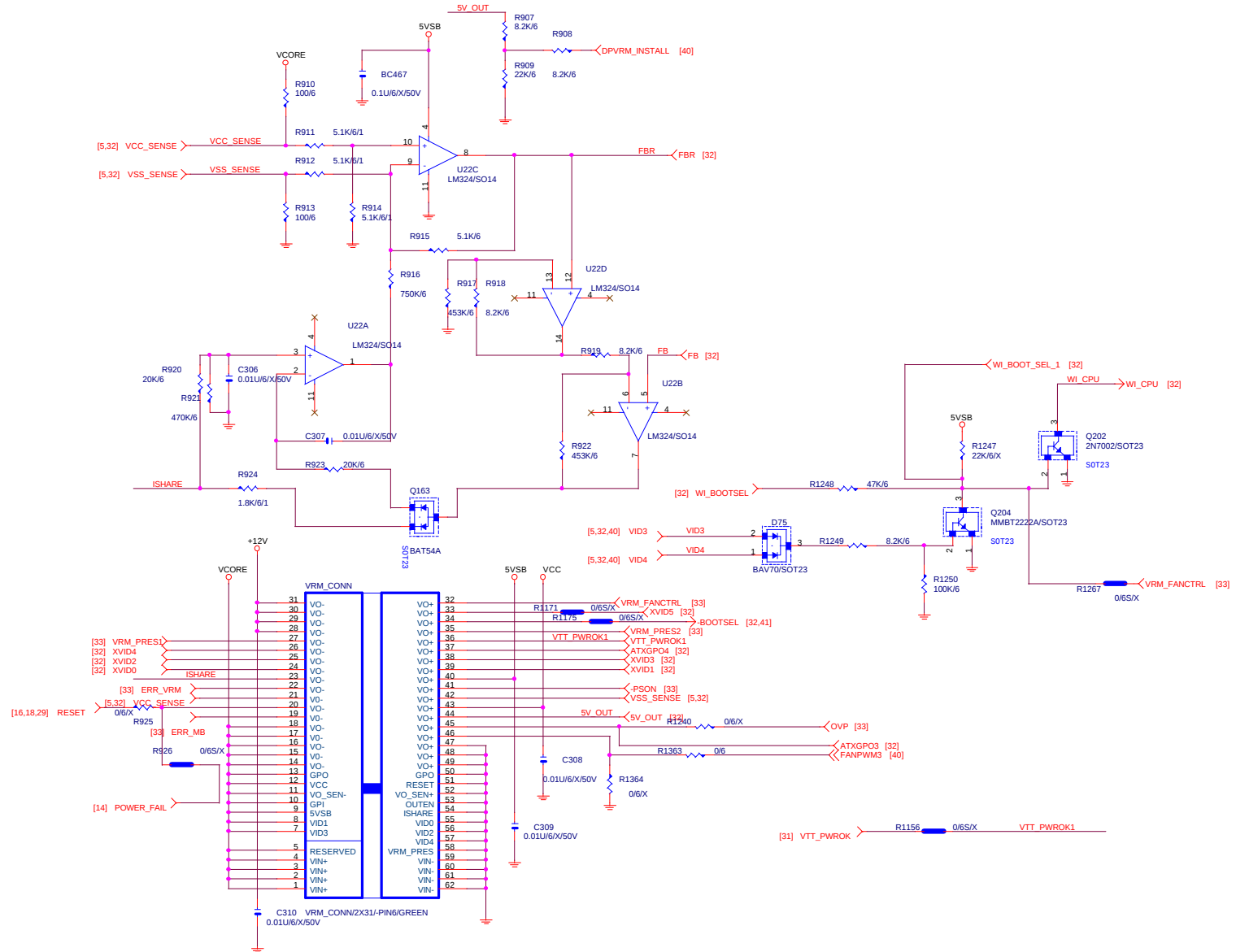
Near PWM

Near PWM

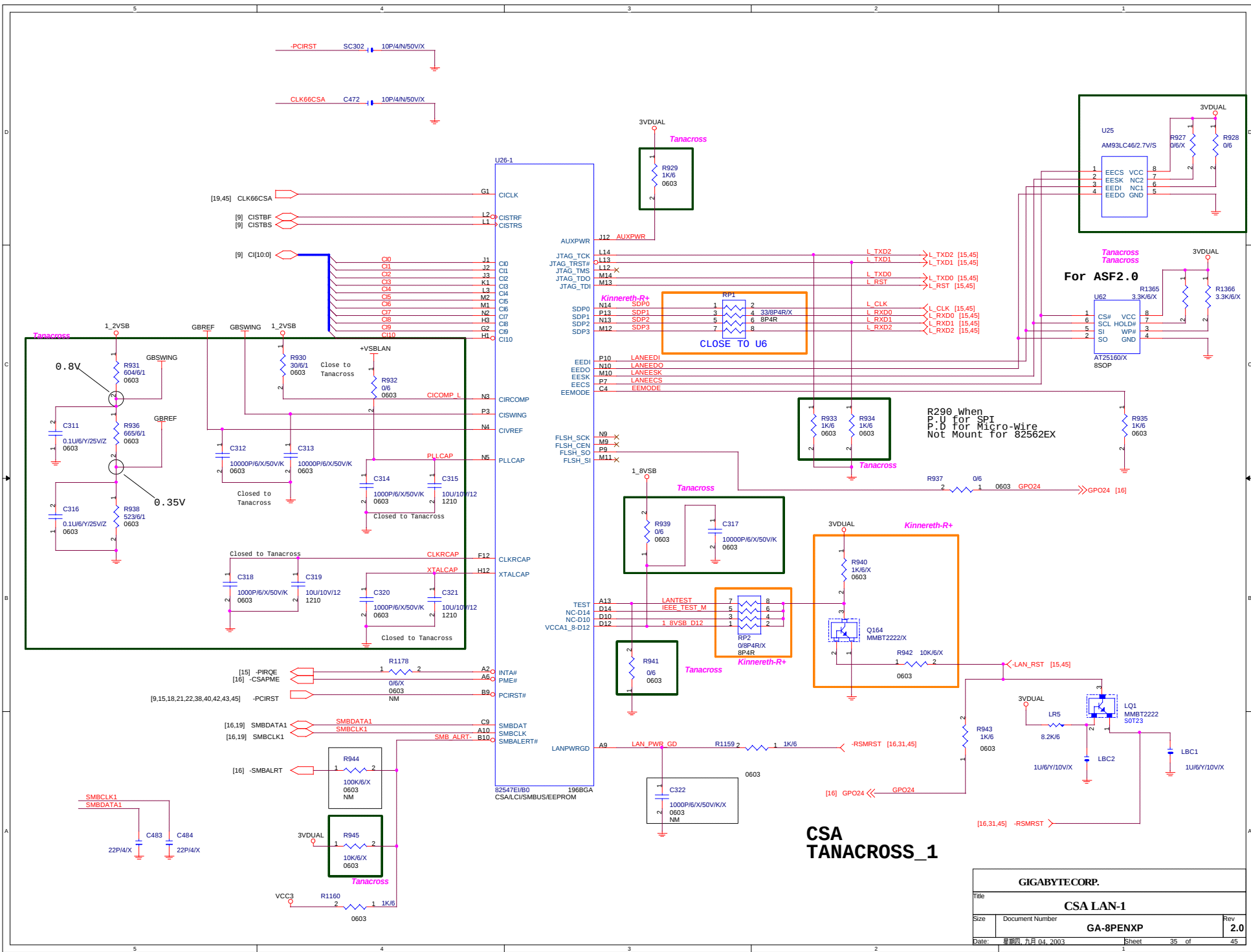
Near PWM

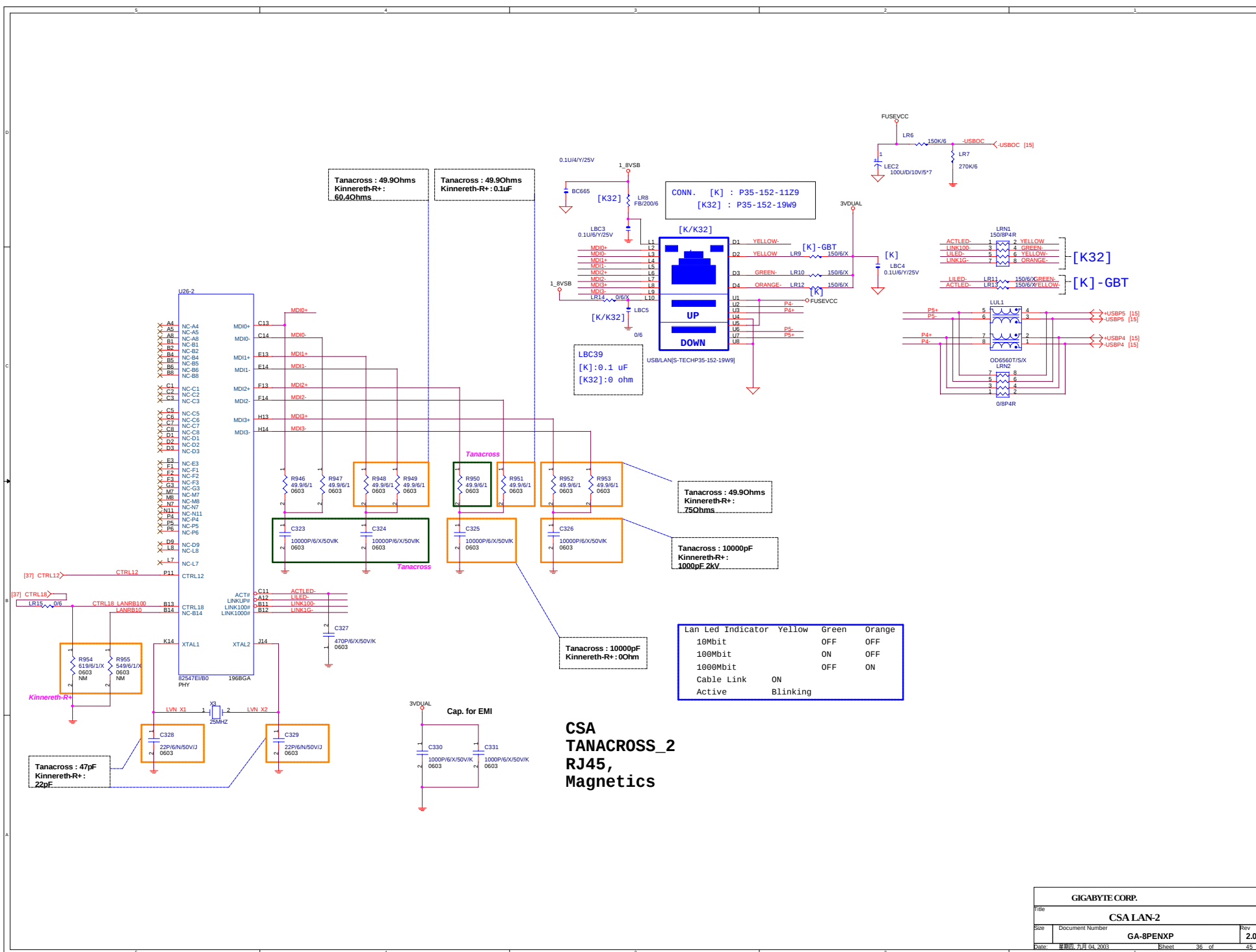
GIGABYTE CORP.			
Title			
Vcore PWM HIP6302CB & DRIVER HIP6602CB			
Size	Document Number	GA-8PENXP	Rev
Custom			2.0
Date:		Sheet	32 of 45
		2	1

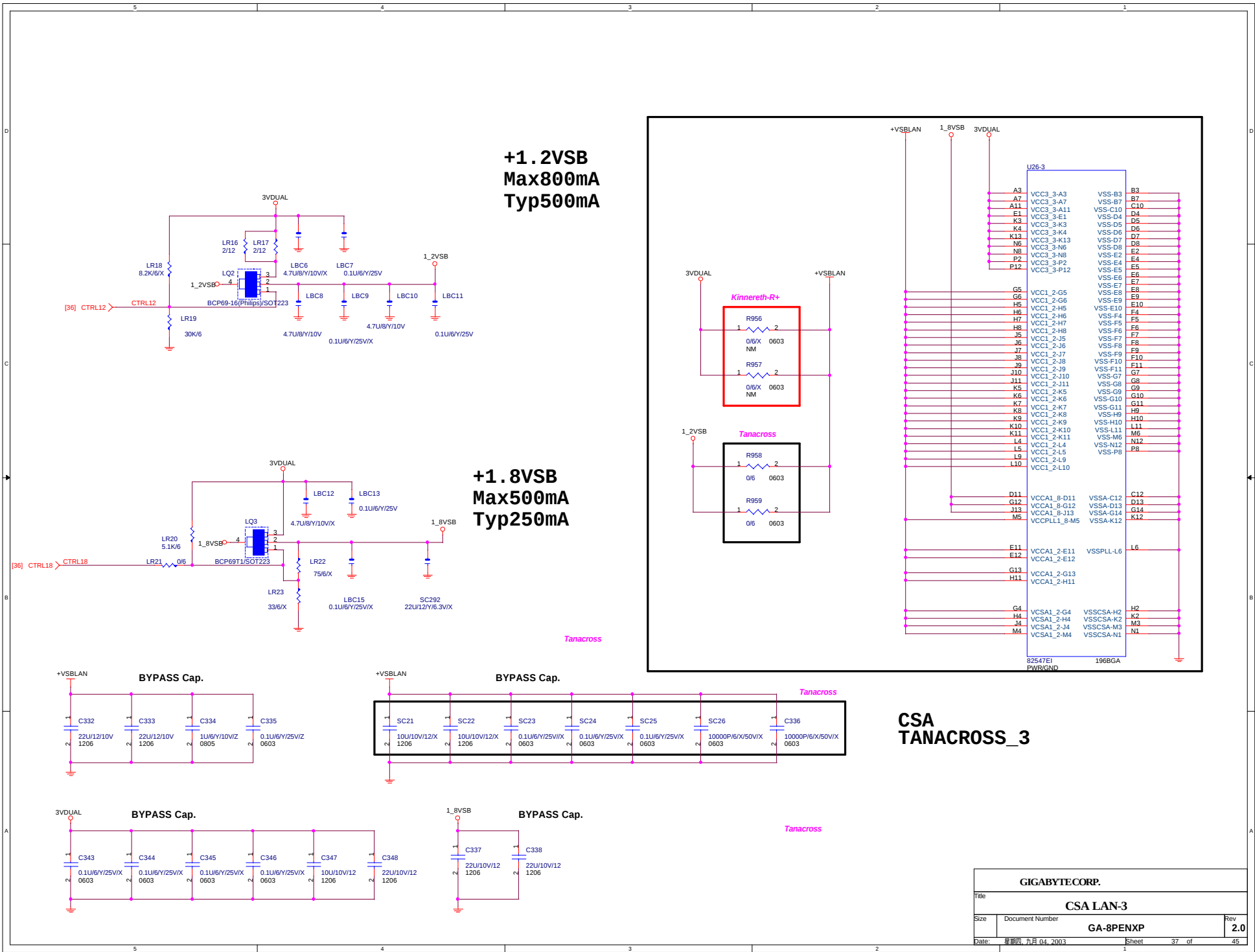
DUAL POWER

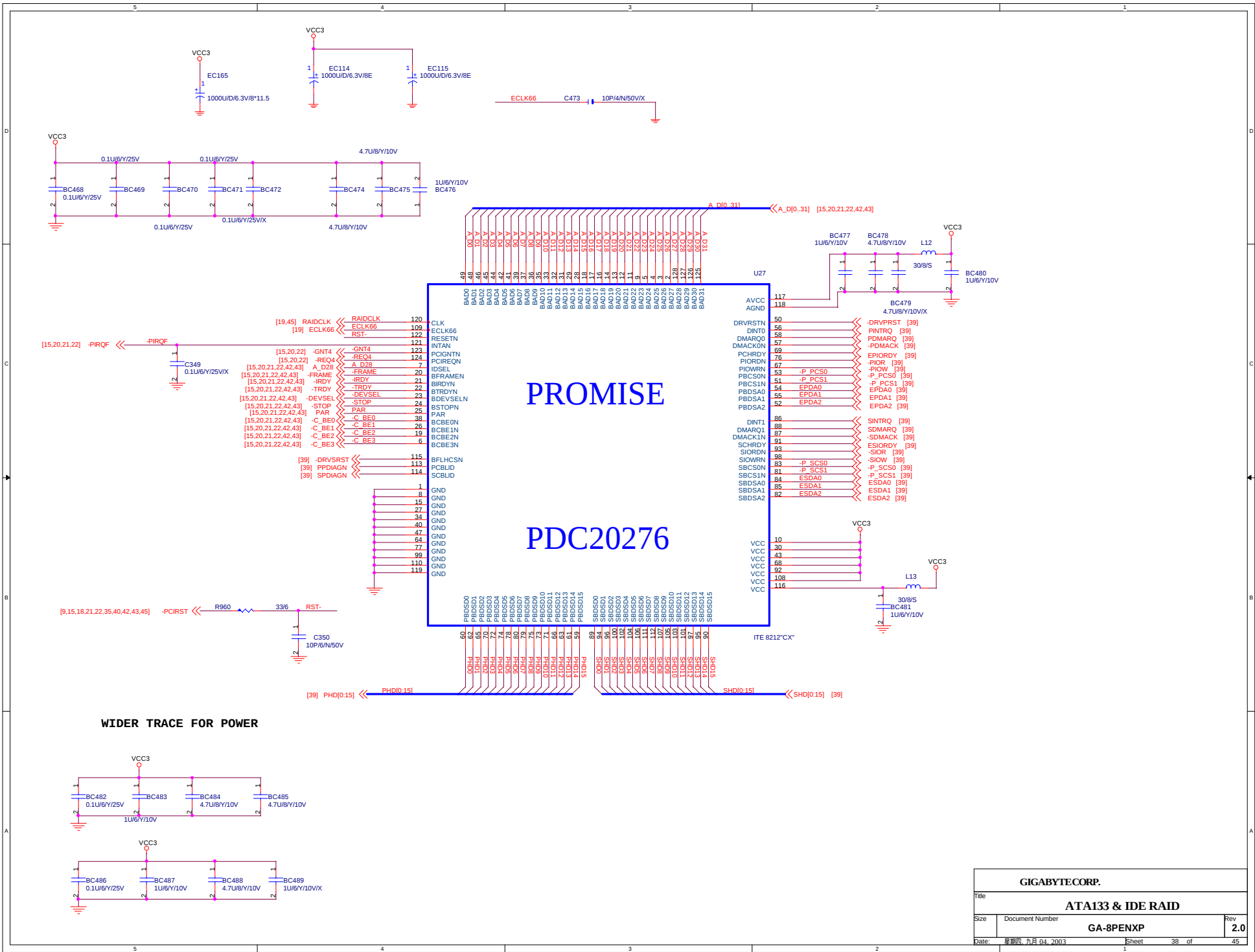


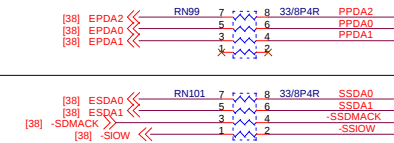
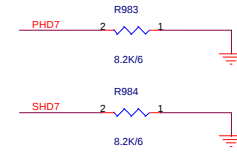
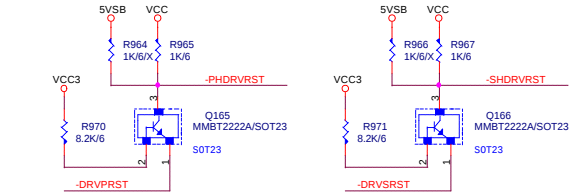
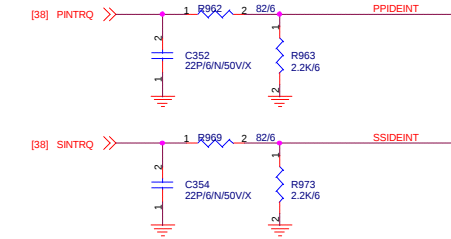
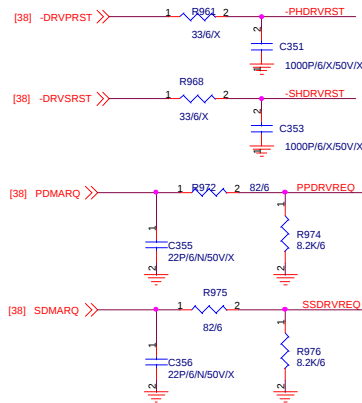
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Title			
Vcore PWM HIP6301+6601			
Size	Document Number	Rev	
Custom	GA-8PENXP	2.0	
Date:	星期四, 九月 04, 2003	Sheet	34 of 45



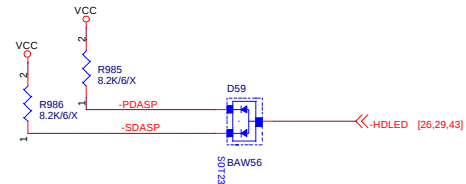
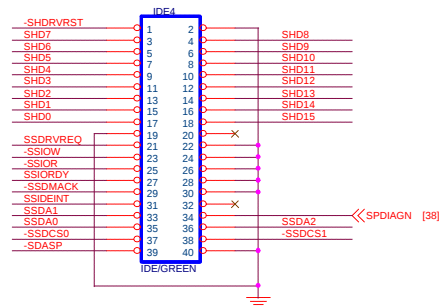
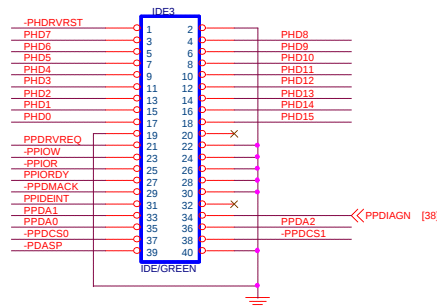
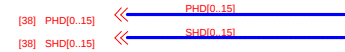




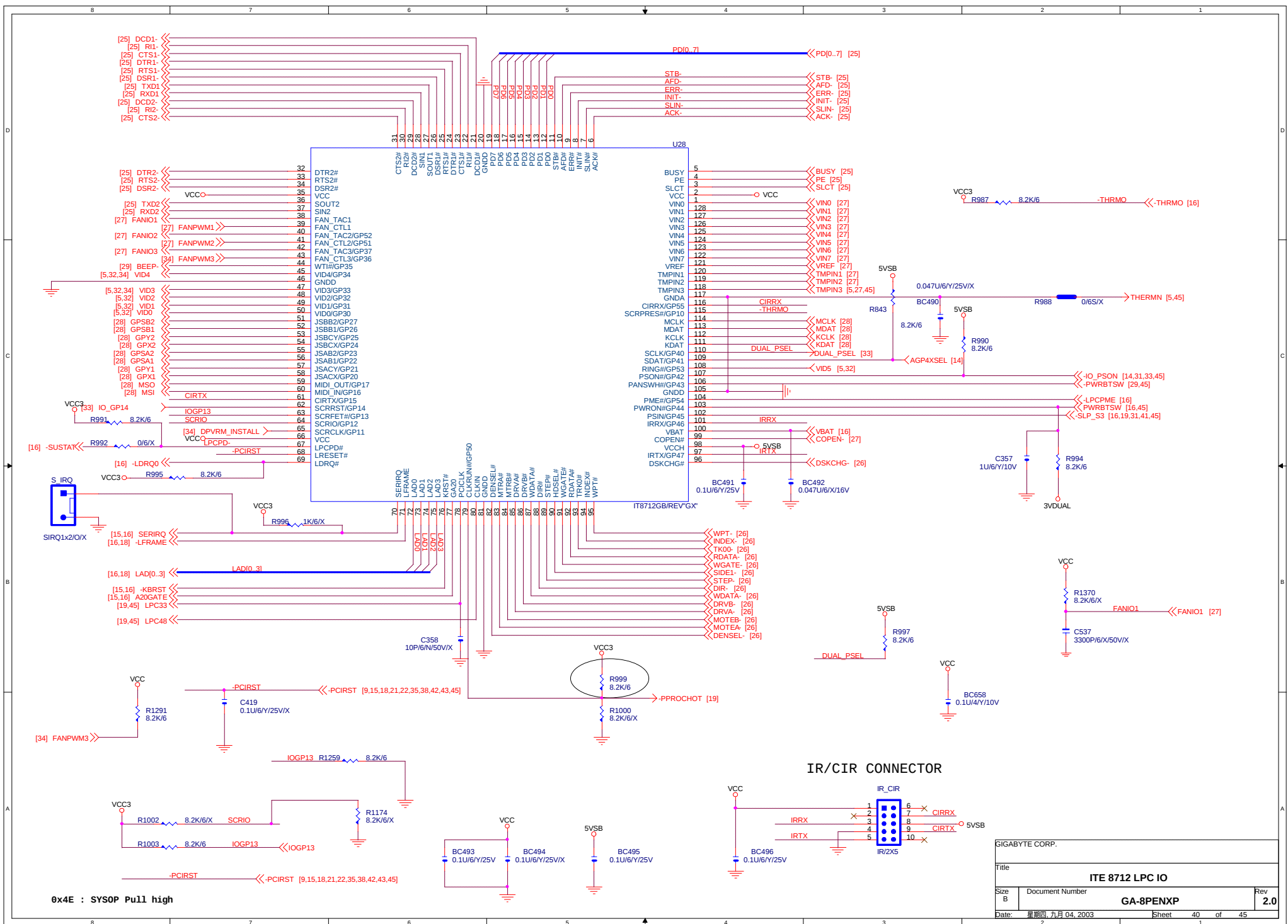




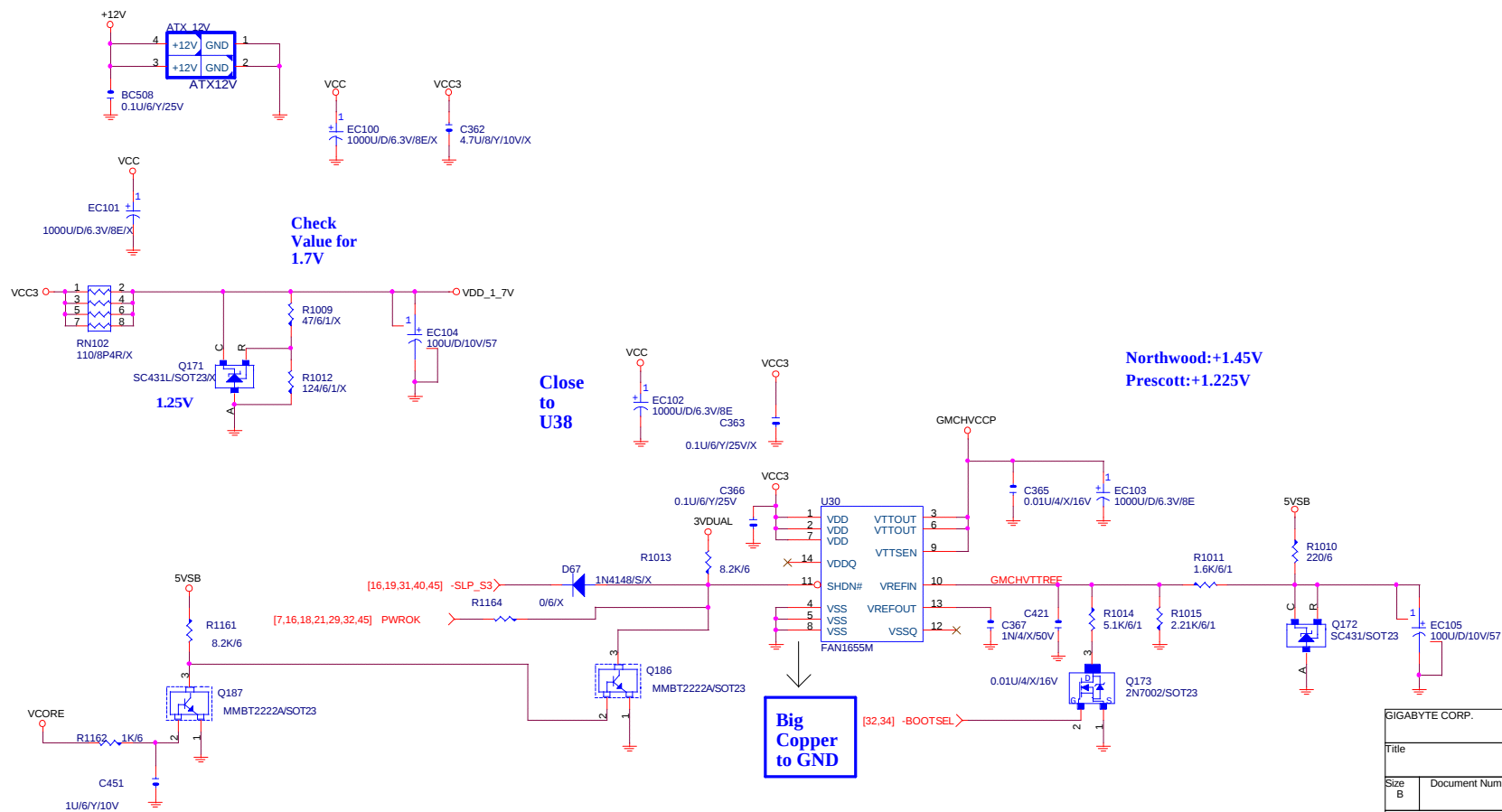
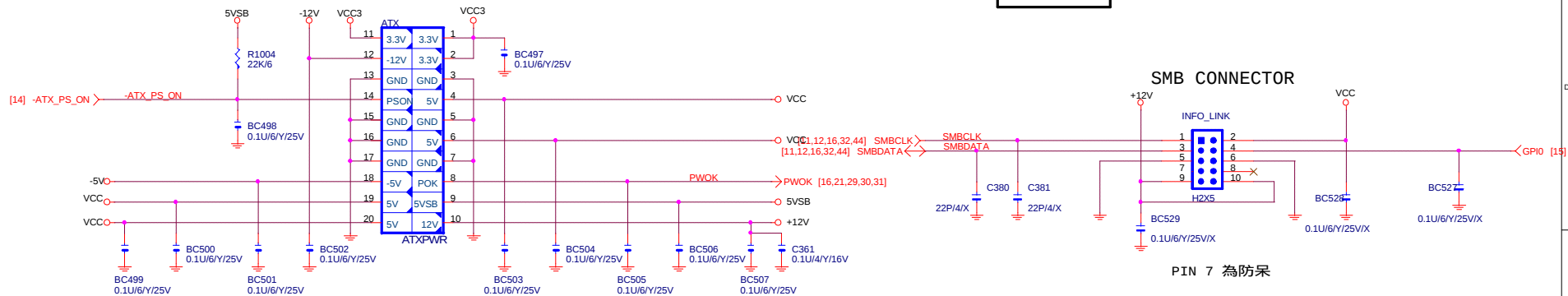
SWAP



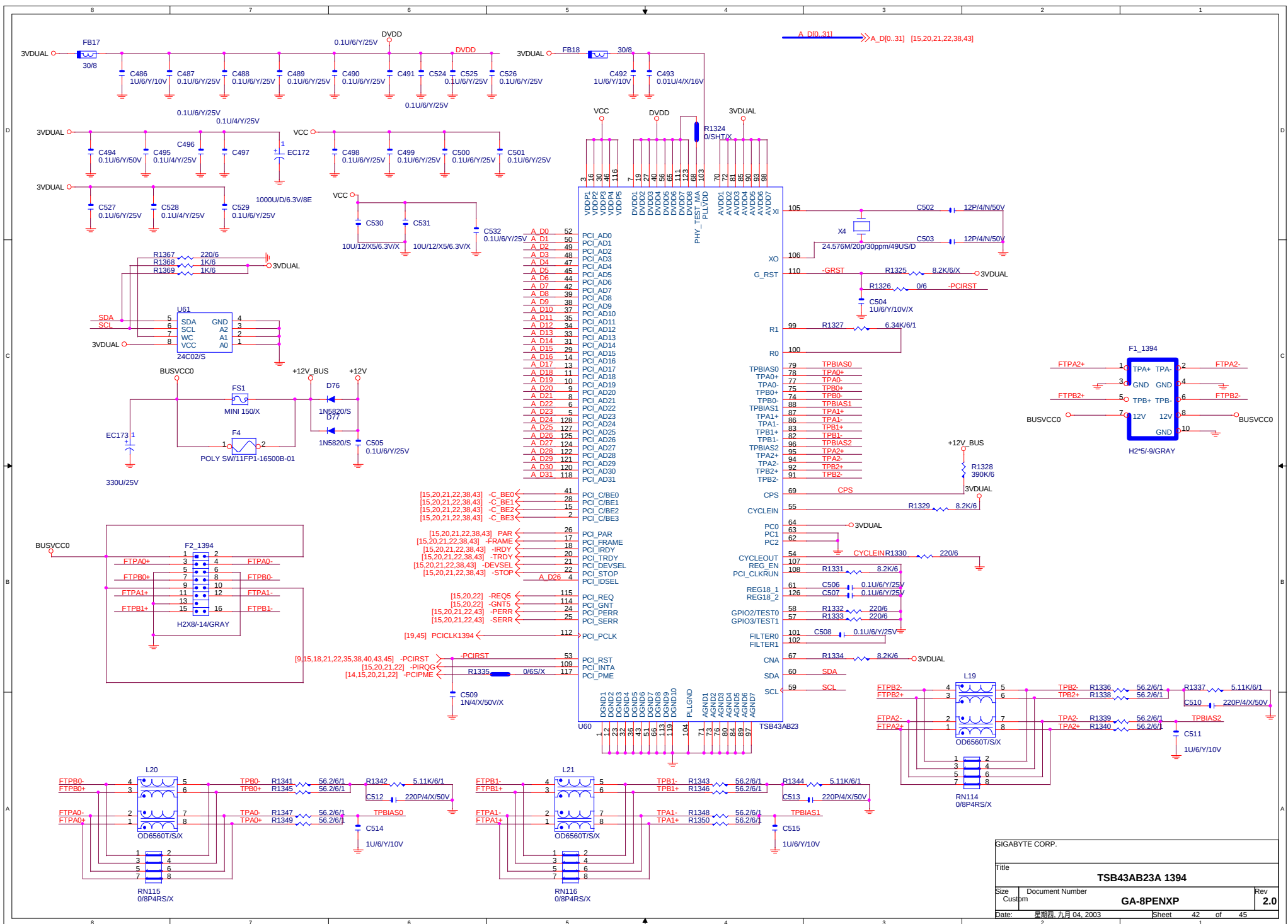
GIGABYTECORP.			
Title			
ATA133 & IDE RAID			
Size	Document Number	GA-8PENXP	Rev 2.0
Date:	星期四, 九月 04, 2003	Sheet 39 of 45	

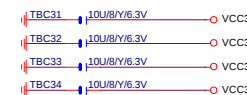
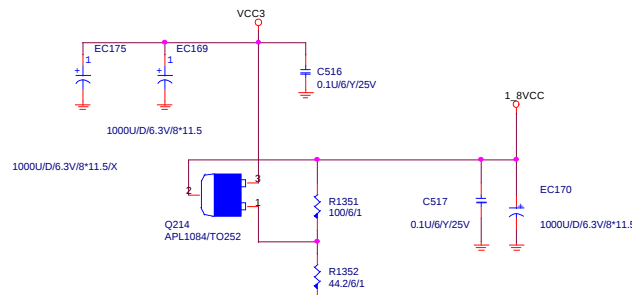
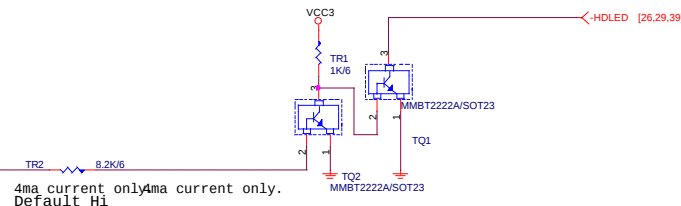
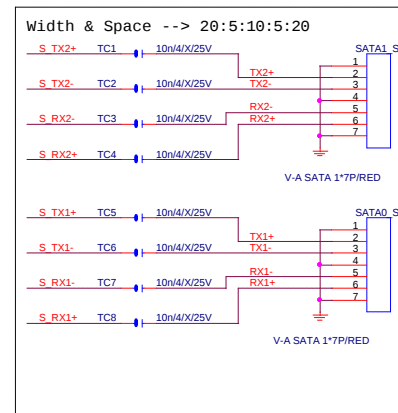
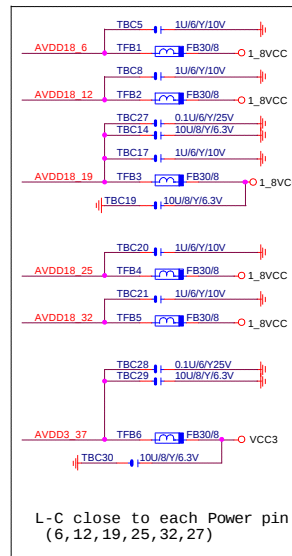
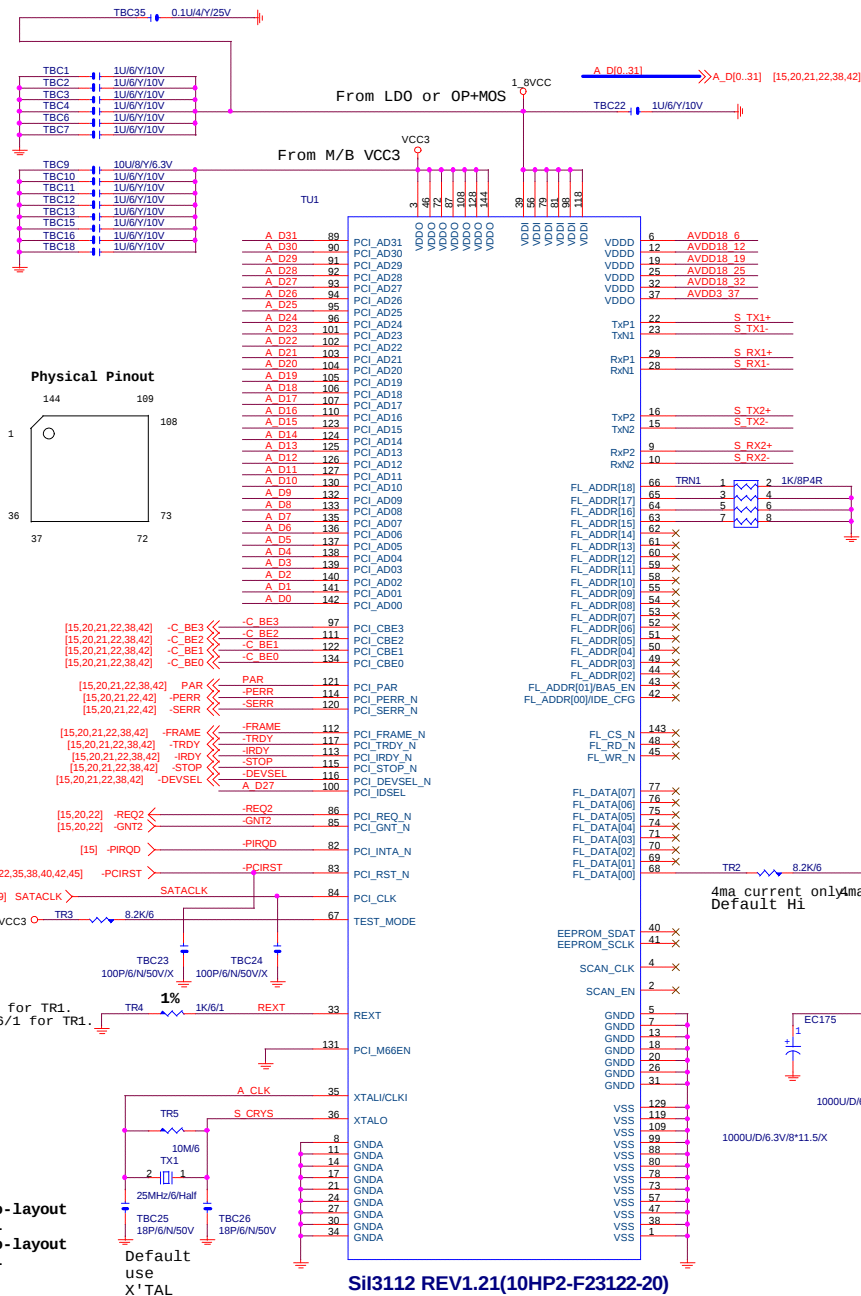


ATX POWER CONNECTOR



GIGABYTE CORP.				
Title Misc. PWR & ATX CONN.				
Size B	Document Number GA-8PENXP			Rev 2.0
Date:		Sheet	41	of 45





1. TX+/- & RX+/- 儘可能Reference GND, 換層時須在其Via hole旁5mil處左右各打一個GND Via.
1. TX+/- & RX+/- 兩旁最好能包地。

GIGABYTE			
Silicon Image SiI3112(S-ATA)			
Title	Document Number	Rev	2.0
Size	Custom	GA-8PENXP	
Date	星期四, 九月 04, 2003	Sheet	43 of 45

CPURST_0

GTUREF_0

CPUCLK

-CPUCLK

CPUPWROK_0

DB11_1 → -DB11 [6,7]
 -DB12_1 → -DB12 [6,7]
 VCOREPLL → VCOREPLL
 VCCA → VCCA [5]
 VSSA → VSSA [5]
 VCORE_0 → VCORE

AGPCLK	→	AGPCLK [14,19]
-PCIRST_1	→	-PCIRST [9,15,18,21,22,35,40,42,43]
-ADSTB0	→	-ADSTB0 [9,14]
ADSTB0	→	ADSTB0 [9,14]
-ADSTB1	→	-ADSTB1 [9,14]
ADSTB1	→	ADSTB1 [9,14]
-SBSTB	→	-SBSTB [9,14]
SBSTB	→	SBSTB [9,14]
MCH_AGPREF_1	→	MCH_AGPREF [9,14]
VCC3_1	→	VCC3
VDDQ_1	→	VDDQ
VCC_0	→	VCC
-TYPE_DET	→	-TYPE_DET [14]
-GC_DET1	→	-GC_DET1 [14]
-MB_DET	→	-MB_DET [14]
-GFRAME	→	-GFRAME [9,14]

CPURST_1 ↔ -CPURST [4,7]
 -HADS_0 ↔ -HADS [4,7]
 -HADSTB0_1 ↔ -HADSTB0 [4,7]
 -HADSTB1_1 ↔ -HADSTB1 [4,7]
 GTLREF_1 ↔ GTLREF [5,7]
 MCHCLK_1 ↔ MCHCLK [7,19]
 -MCHCLK ↔ -MCHCLK [7,19]

Timing diagram for the 74VHC04-100. The diagram shows five digital signals over time:

- DBI1_0**: Input signal for DBI1, period 100ns.
- DBI2_0**: Input signal for DBI2, period 100ns.
- HSWNG**: Input signal for HSWNG, period 7ns.
- PWROK_0**: Input signal for PWROK, period 7.16, 18, 21, 29, 32, and 41ns.
- DBI1 [6,7]**: Output signal for DBI1, period 6.7ns.
- DBI2 [6,7]**: Output signal for DBI2, period 6.7ns.
- HSWNG [7]**: Output signal for HSWNG, period 7ns.
- PWROK [7,16,18,21,29,32,41]**: Output signal for PWROK, period 7.16, 18, 21, 29, 32, and 41ns.

GMCH3V66 [9,19]
 GSWING_0 [9,14]
 MCH_AGPREF_0 [9,14]

 1 VDDQ
 GMCHVCCP
 1 GMCHVCCP
 DDR25V_0
 1 DDR25V
 VCC3_0
 1 VCC3
 VCORE_1
 1 VCORE

● DCLKA0	↔	DCLKA0 [8.11]
● -DCLKA0	↔	-DCLKA0 [8.11]
● DCLKA1	↔	DCLKA1 [8.11]
● -DCLKA1	↔	-DCLKA1 [8.11]
● DCLKA2	↔	DCLKA2 [8.11]
● -DCLKA2	↔	-DCLKA2 [8.11]
● DCLKA3	↔	DCLKA3 [8.11.44]
● -DCLKA3	↔	-DCLKA3 [8.11.44]
● DCLKA4	↔	DCLKA4 [8.11.44]
● -DCLKA4	↔	-DCLKA4 [8.11.44]
● DCLKA5	↔	DCLKA5 [8.11.44]
● -DCLKA5	↔	-DCLKA5 [8.11.44]
● DCLKB0	↔	DCLKB0 [8.12]
● -DCLKB0	↔	-DCLKB0 [8.12]
● DCLKB1	↔	DCLKB1 [8.12]
● -DCLKB1	↔	-DCLKB1 [8.12]
● DCLKB2	↔	DCLKB2 [8.12]

 DCLKB5 [8,12,44]
 -DCLKB5 [8,12,44]
 CKEA0 [8,11,13]
 CKEA1 [8,11,13]

VREF_DDRA [11,44]
VREF_DDRB [12,44]
DDR25V_DDR1
DDR25V_DDR4
DDR25V

Figure 10 illustrates the pinmux configuration for the i.MX8M Mini. The diagram shows the following connections:

- ICH33** (Pin 1) connects to **ICH33 [15,19]**.
- PCHIST_2** (Pin 1) connects to **-PCHIST [9,15,18,21,22,36,38,40,42,43]**.
- USBCLK** (Pin 1) connects to **USBCLK [15,19]**.
- ICH3V66** (Pin 1) connects to **ICH3V66 [15,19]**.
- HL_VREF_ICH** (Pin 1) connects to **HL_VREF_ICH [9,15]**.
- HL_SWING_ICH** (Pin 1) connects to **HL_SWING_ICH [9,15]**.
- ICHCLK14** (Pin 1) connects to **ICHCLK14 [16,19]**.
- CPUPWROK_1** (Pin 1) connects to **CPUPWROK [5,16]**.
- THERM** (Pin 1) connects to **-THERM [5,16]**.
- SYS_RST** (Pin 1) connects to **-SYS_RST [16,18,19,29,32]**.
- SRCCLK** (Pin 1) connects to **SRCCLK [16,19]**.
- SRCCLK** (Pin 1) connects to **-SRCCLK [16,19]**.
- RSMRST** (Pin 1) connects to **-RSMRST [16,31,35]**.
- PWROK** (Pin 1) connects to **PWROK [7,16,18,21,29,32,41]**.
- VDDQ_2** (Pin 1) connects to **VDDQ**.
- VCC3_2** (Pin 1) connects to **VCC3**.
- 3VDUAL_0** (Pin 1) connects to **3VDUAL**.

5VSB_ICH5

FWH33 [18,19]
-PCIRST_3 [9,15,18,21,22,35,38,40,42,43]

CKVDD

1 CKVDD

The diagram shows a signal labeled CKVDD. It starts at a low level (0) and transitions to a high level (1) at a specific point in time. The transition is marked with a red circle and the number 1.

ASIC2CLK

1

ASIC2CLK [19,22]

PCICLK1394

PCICLK1394 [19,42]

RAIDCLK 1 RAIDCLK [19:38]

PCIRST1_0	→	PCIRST1 [20,21,22]
PCIRST1_1	→	PCIRST1 [20,21,22]
PCIRST1_2	→	PCIRST1 [20,21,22]
PCILK0	→	PCLK0 [19,20]
PCILK1	→	PCLK1 [19,20]
PCILK2	→	PCLK2 [19,21]
PCILK3	→	PCLK3 [19,21]
PCILK4	→	PCLK4 [19,22]

-PCIRST1_3
1
-PCIRST1 [20,21,22]

-PCIRST1_4
1
-PCIRST1 [20,21,22]

-PCIRST1_5
1
-PCIRST1 [20,21,22]

Diagram illustrating the gene structure of *PIRIST_8* and its orthologous genes. The diagram shows the gene structure of *PIRIST_8* with 8 exons (blue circles) and 7 introns (red lines with arrows). Below it, the orthologous genes are shown: *LPC33*, *LPC48*, *TMPIN3*, *THERMIN*, and *VCC3_5*. The orthologous genes are shown with their exon-intron structure and the corresponding gene name and coordinates in brackets.

Gene	Coordinates
<i>PIRIST_8</i>	-
<i>LPC33</i>	[9,15,18,21,22,35,38,40,42,43]
<i>LPC48</i>	[19,40]
<i>TMPIN3</i>	[5,27,40]
<i>THERMIN</i>	[5,40]
<i>VCC3_5</i>	-

Figure 10: Pin connections for the P10410 module. The diagram shows a vertical list of pins on the left, each with a red double-headed arrow pointing to its corresponding pin name and value on the right. The pins are: PCIRST_4 (PCIRST [9,15,18,21,22,35,38,40,42,43]), CLK66C6SA (CLK66C6SA [19,35]), -LAN_RST (-LAN_RST [15,35]), L_RXD2 (L_RXD2 [15,35]), L_RXD1 (L_RXD1 [15,35]), L_RXD0 (L_RXD0 [15,35]), L_CLK (L_CLK [15,35]), L_TXD2 (L_TXD2 [15,35]), L_TXD1 (L_TXD1 [15,35]), L_TXD0 (L_TXD0 [15,35]), and L_RST (L_RST [15,35]).

HLSTB-1
HLSTBS
HL0
HL5
HL10

Timing diagram for the AC interface. The diagram shows the relationship between the signals and their corresponding pins [19,23].

- 97CLK14 (Pin 19) is connected to 97CLK14 [19,23].
- AC_BITCLK (Pin 20) is connected to AC_BITCLK [15,23].
- AC_RST (Pin 21) is connected to -AC_RST [15,23].
- AC_SYNC (Pin 22) is connected to AC_SYNC [15,23].
- AVDD (Pin 23) is connected to AVDD.
- VCC3_7 (Pin 24) is connected to VCC3.

Title				
TEST POINT				
Size Custom	Document Number GA-8PENXP			Rev 2.1
Date	File name	Alt.	Ref.	Alt.