

GA-8PE800-L Schematics

Revision 1.1

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[illegible]

GIGABYTE			
COVER SHEET			
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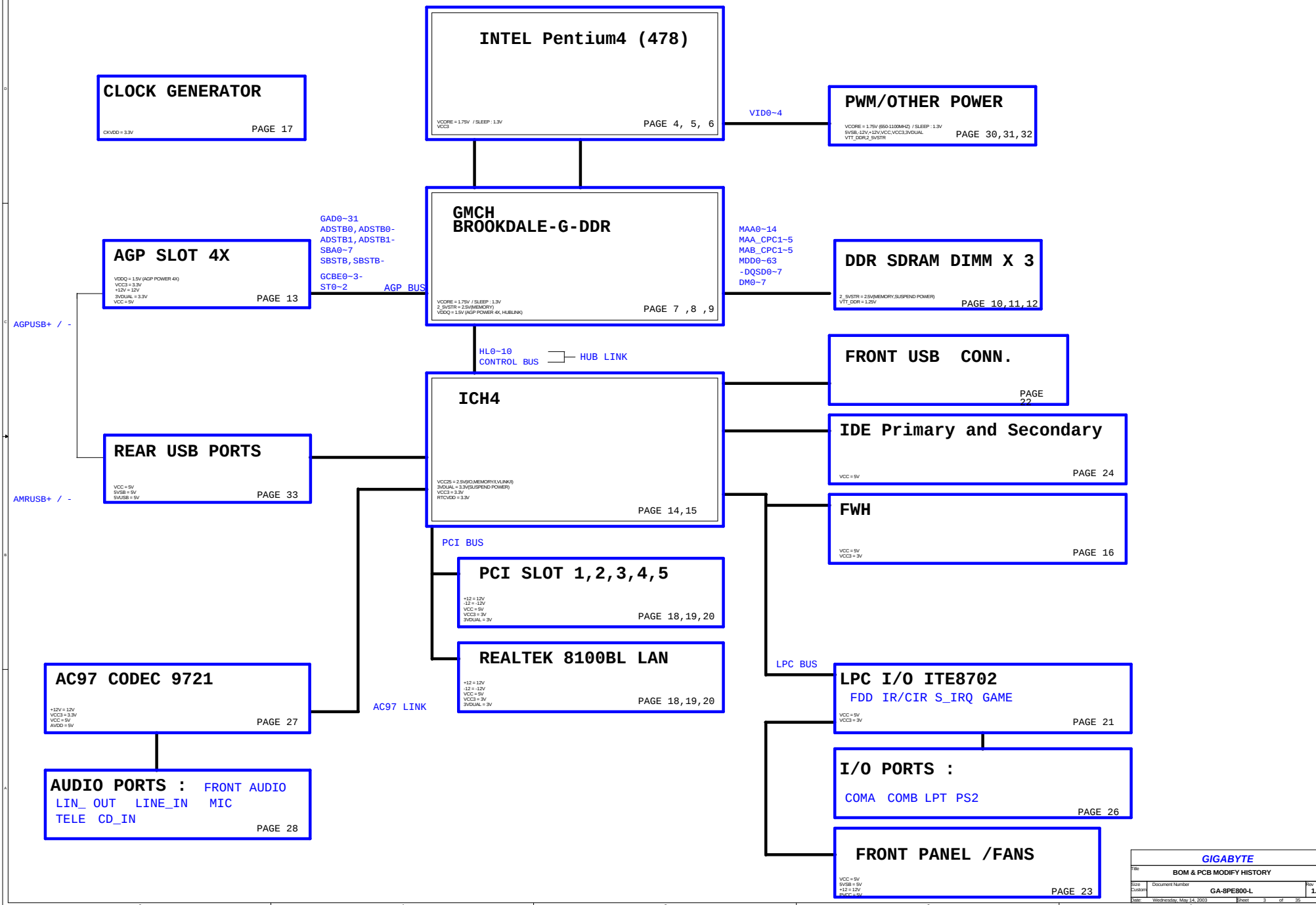
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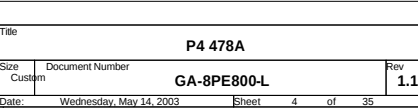
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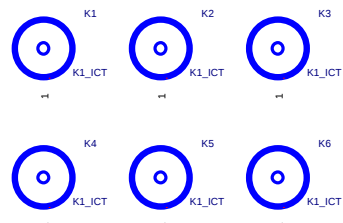
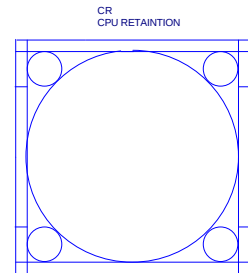
Circuit or PCB layout change for next version

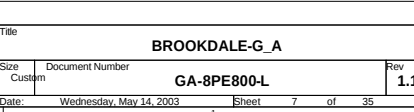
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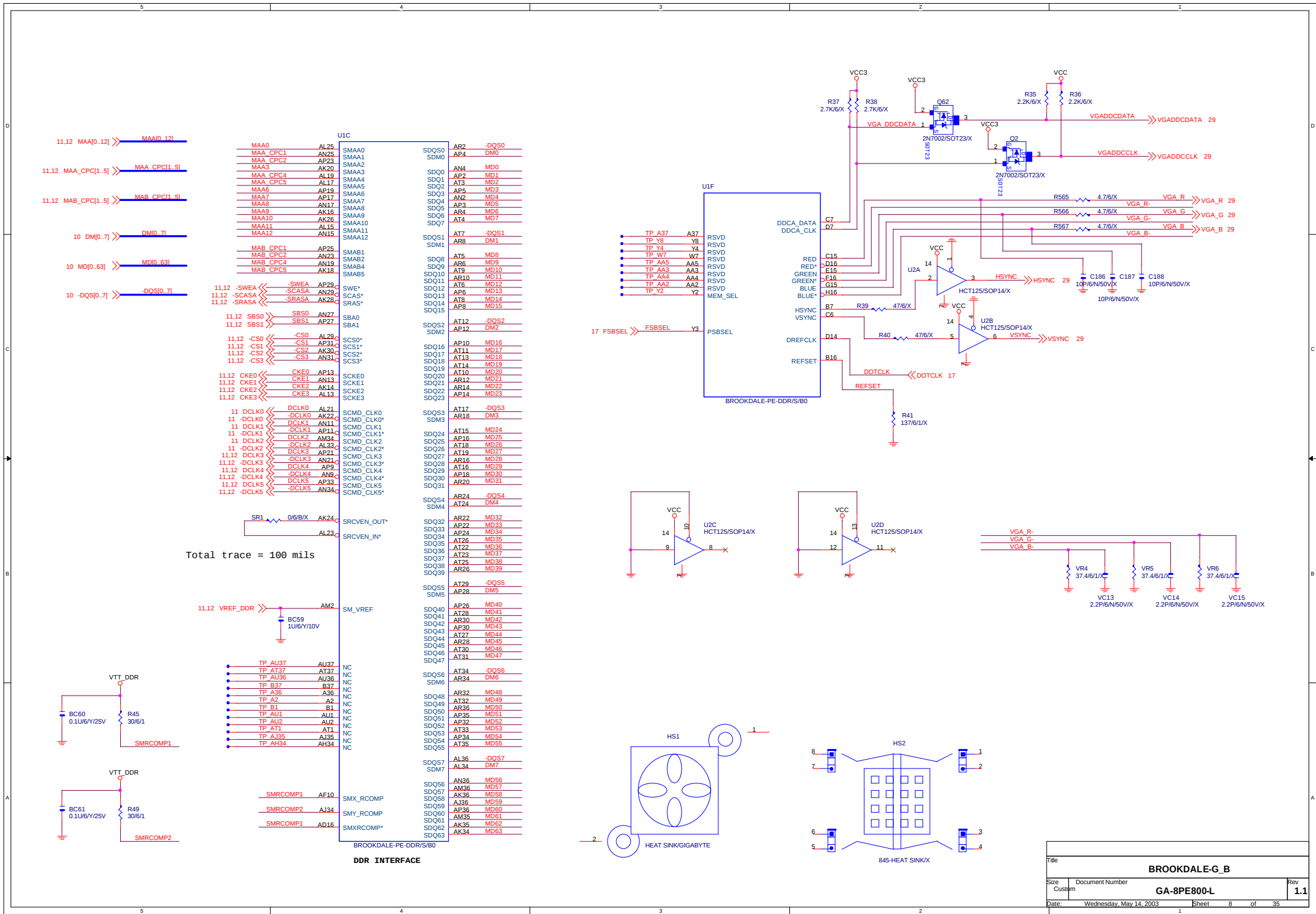
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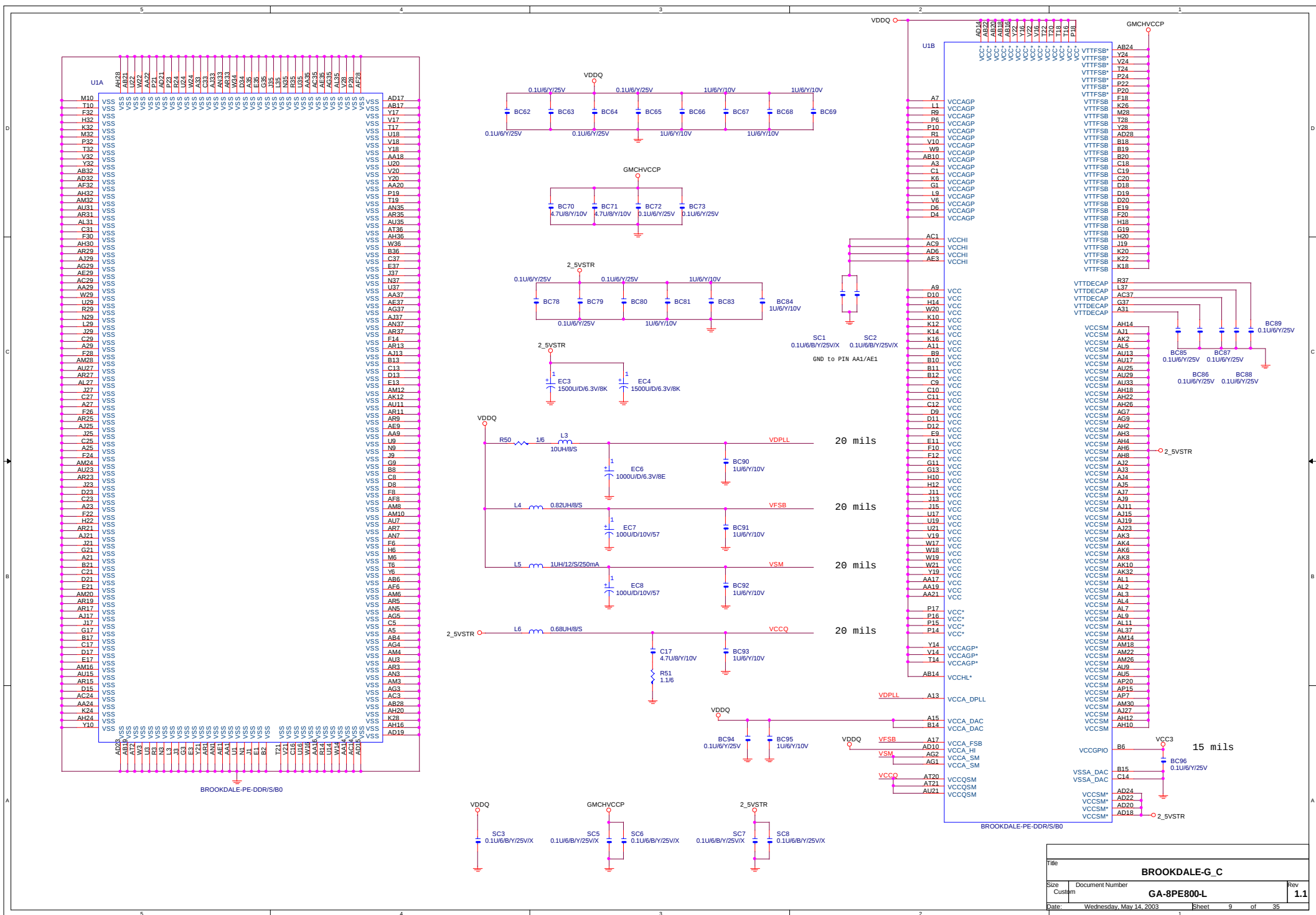


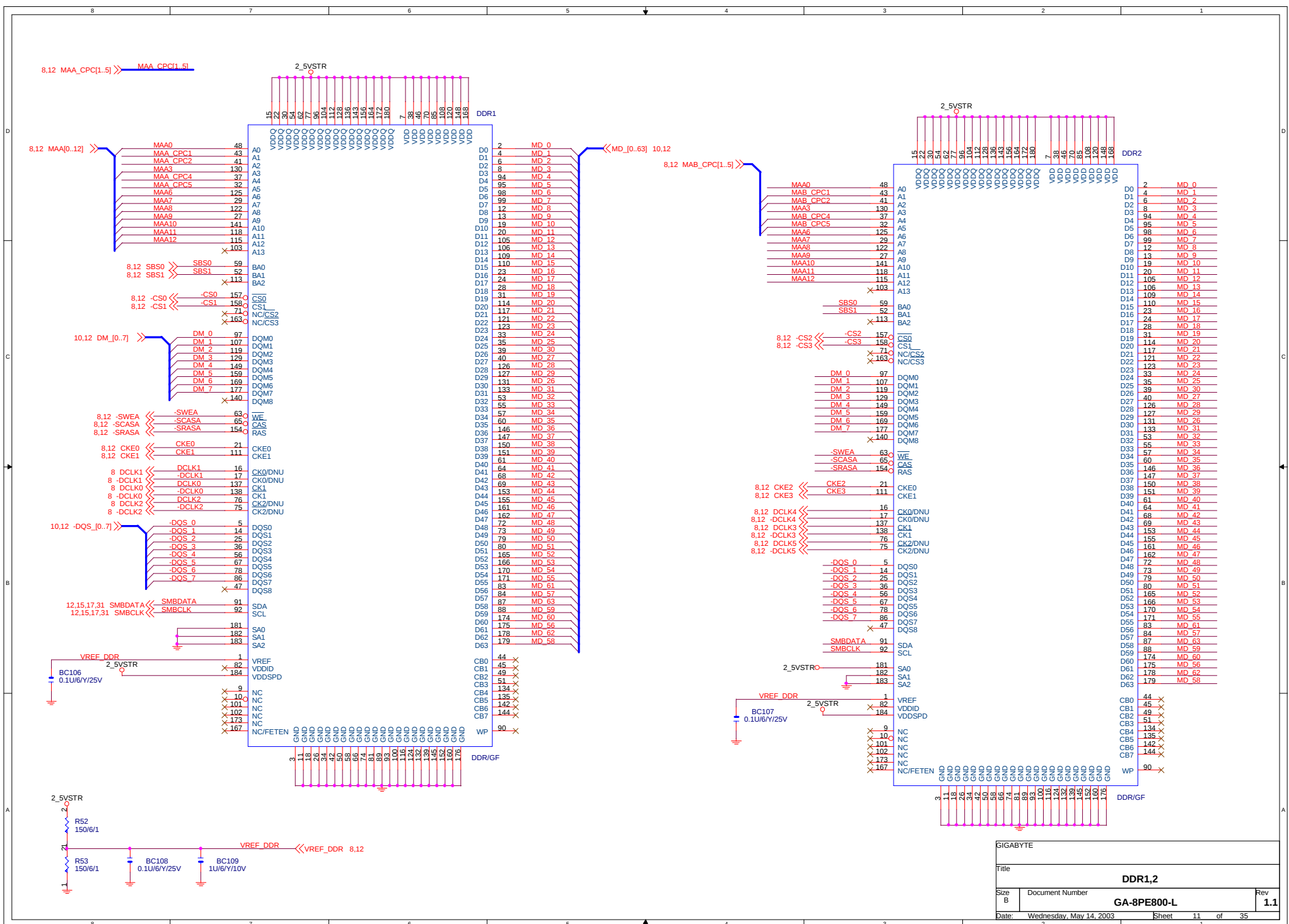


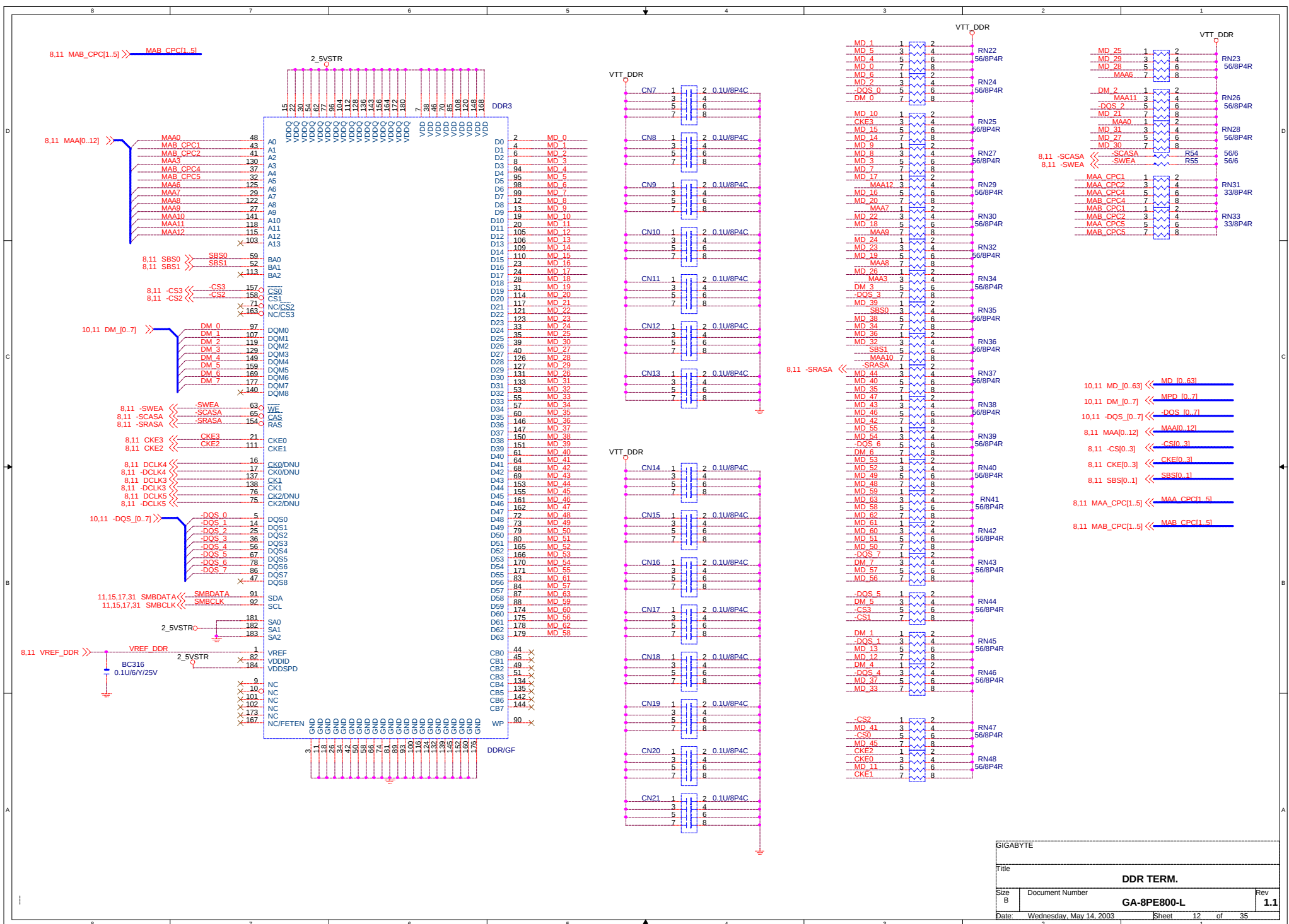




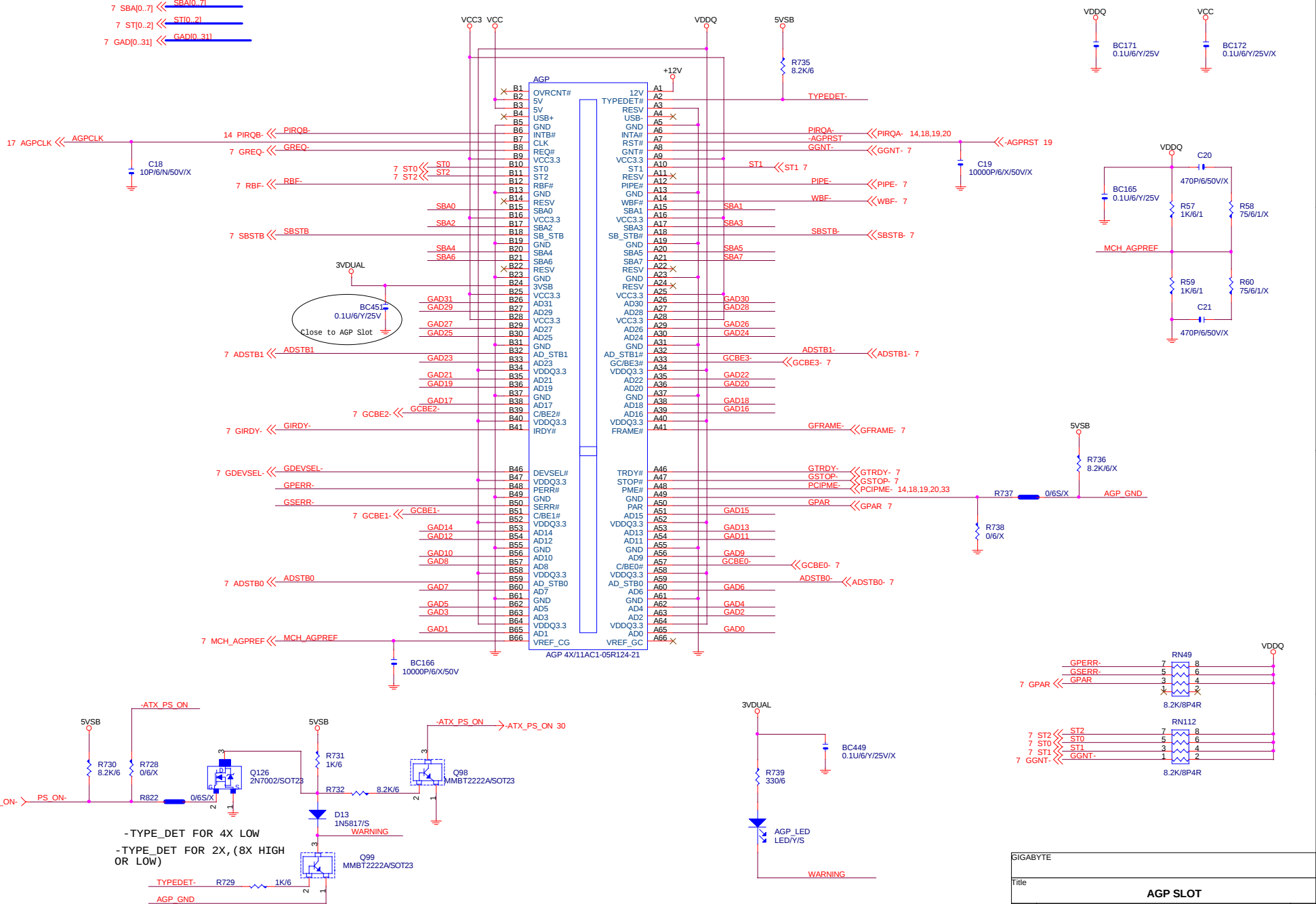








7 SBA[0..7] << SBA[0..7]
 7 ST[0..2] << ST[0..2]
 7 GAD[0..31] << GAD[0..31]

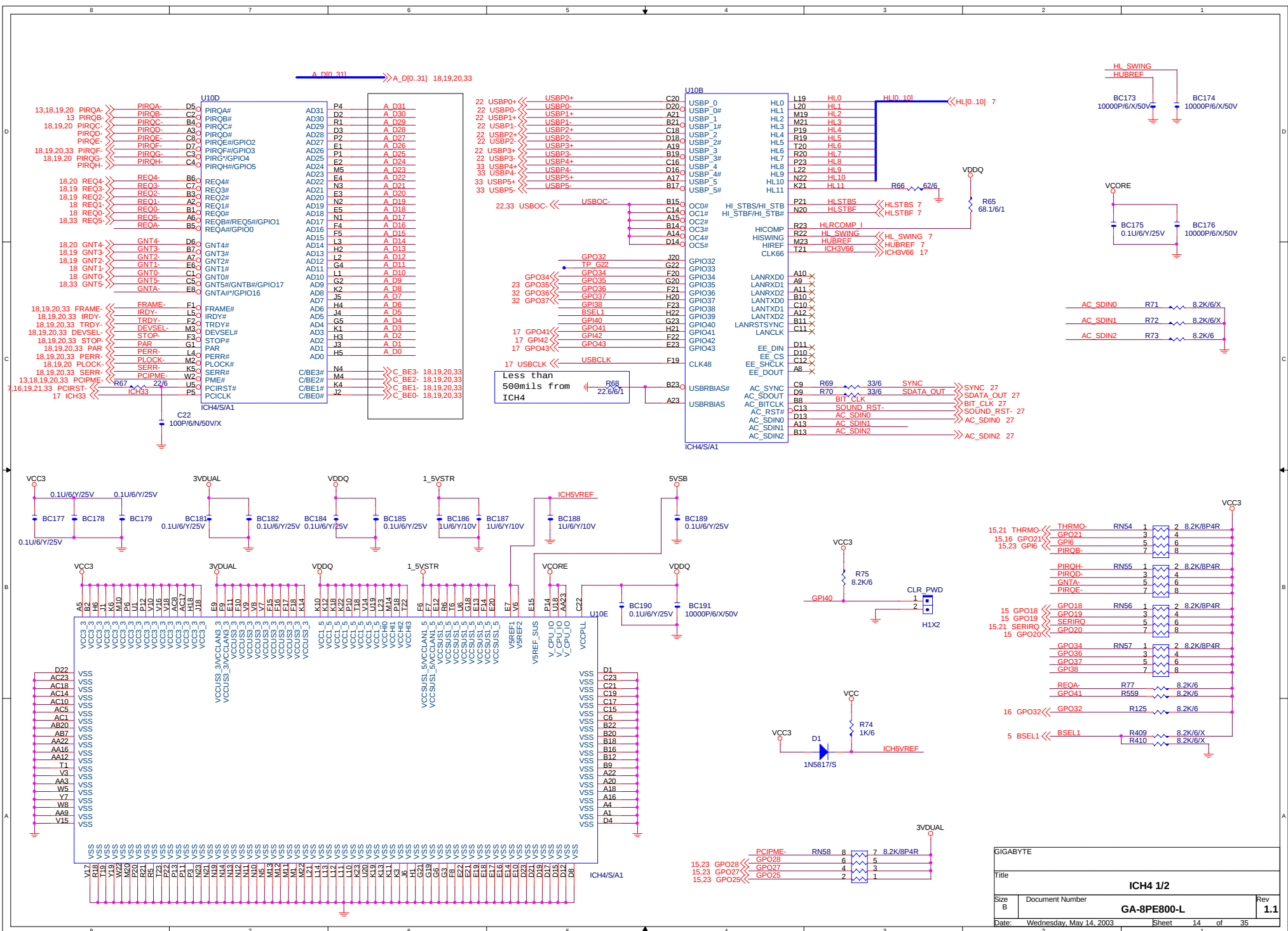


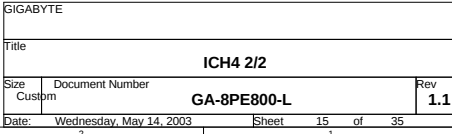
-TYPE_DET FOR 4X LOW
 -TYPE_DET FOR 2X, (8X HIGH OR LOW)

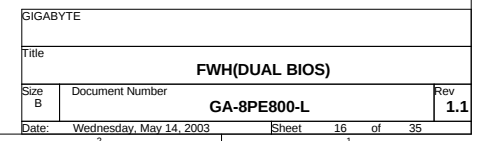
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 AGP_GND

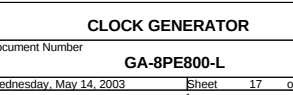
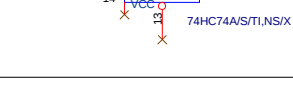
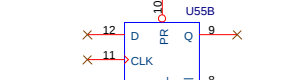
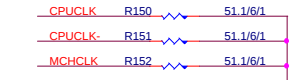
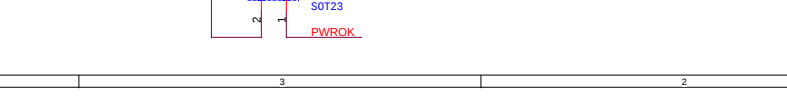
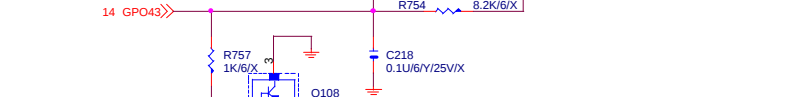
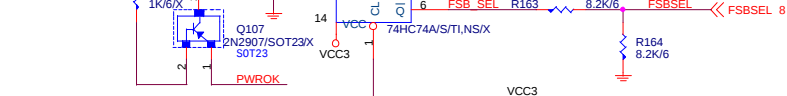
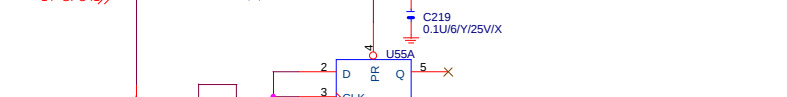
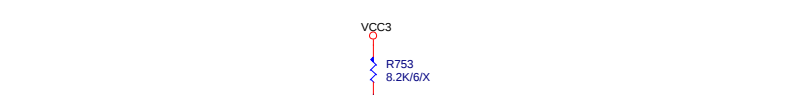
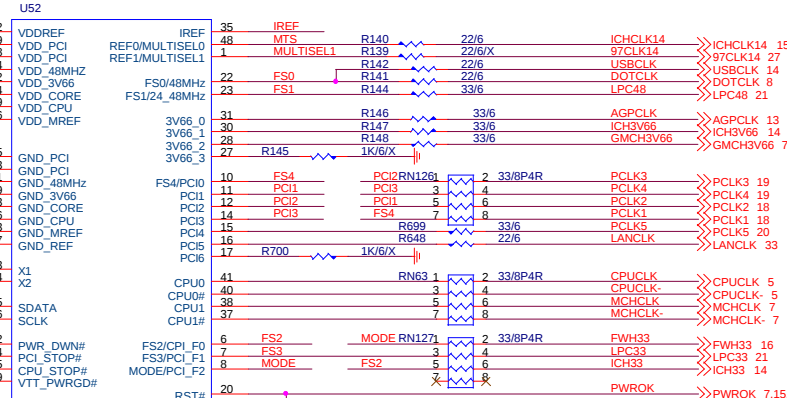
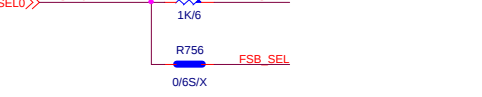
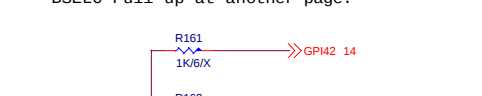
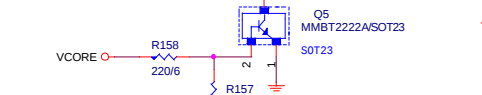
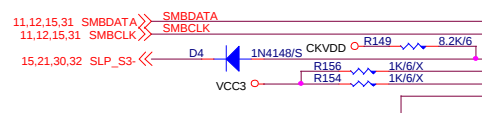
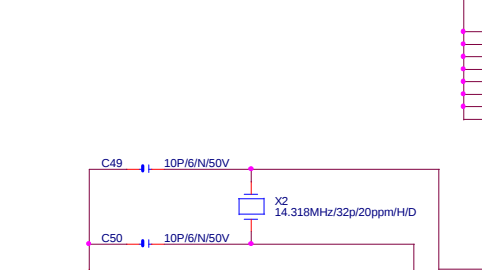
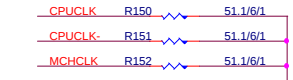
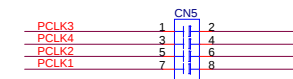
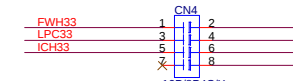
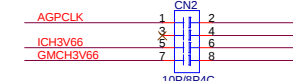
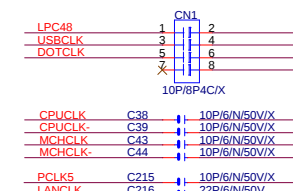
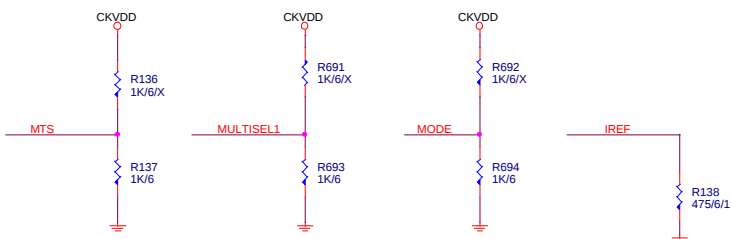
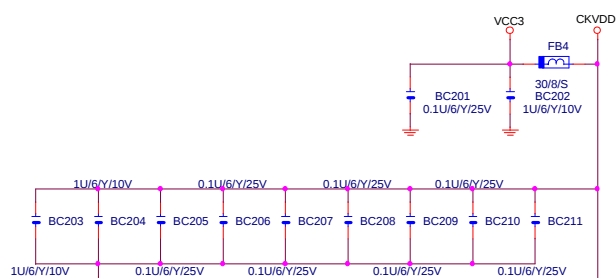
Layout 時整組線路均需靠近 AGP SLOT

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AGP SLOT			
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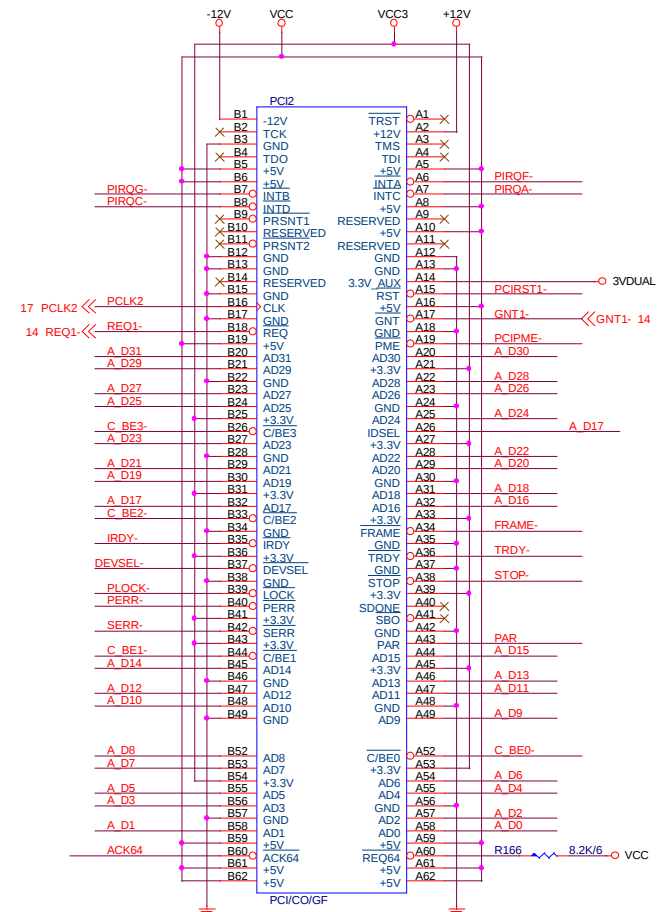
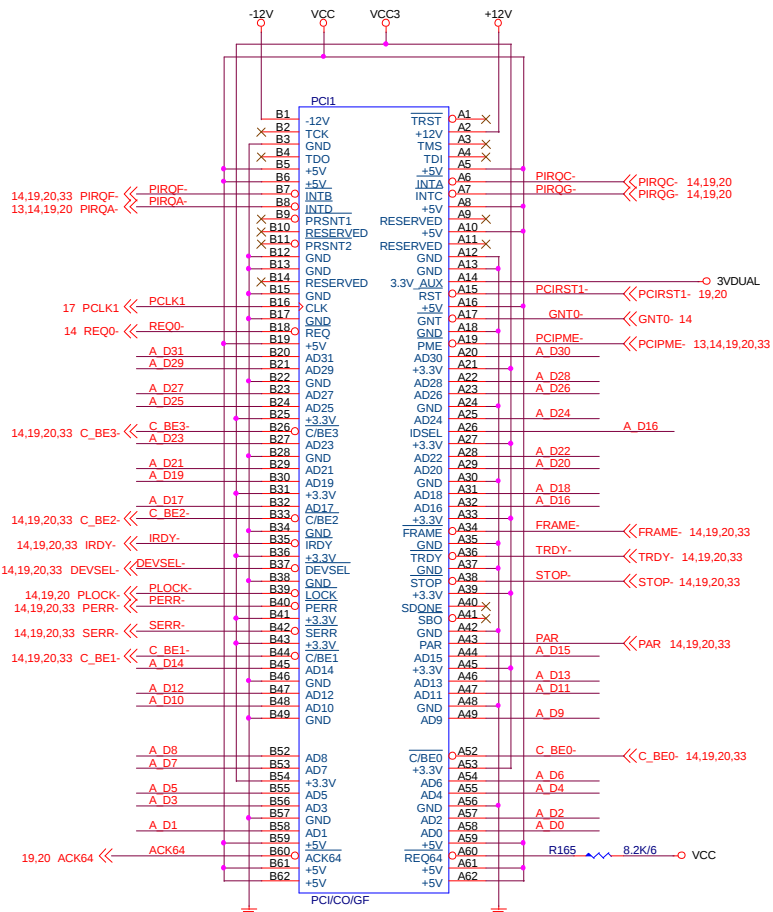






BSEL0 Pull-up at another page.

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CLOCK GENERATOR			
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14,19,20,33 A_D[0..31] << A D0_31

14,19 GNT3 << GNT3- 1
14,19 GNT2 << GNT2- 2
14,20 GNT4 << GNT4- 3
14,33 GNT5 << GNT5- 4

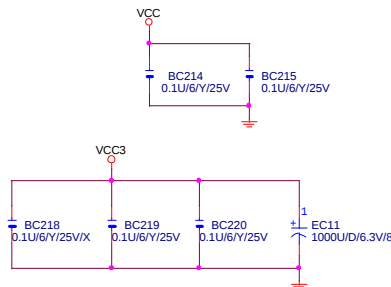
14 GNT0 << GNT0- R167 8.2K/6/X
13,14,19,20 PIRQA << PIRQA- R168 8.2K/6
14 GNT1 << GNT1- R169 8.2K/6/X

14,19,20 PIRQC << PIRQC- RN65 8.2K/8P4R/X
14 REQ0 << REQ0- RN66 8.2K/8P4R
14 REQ1 << REQ1- RN67 8.2K/8P4R

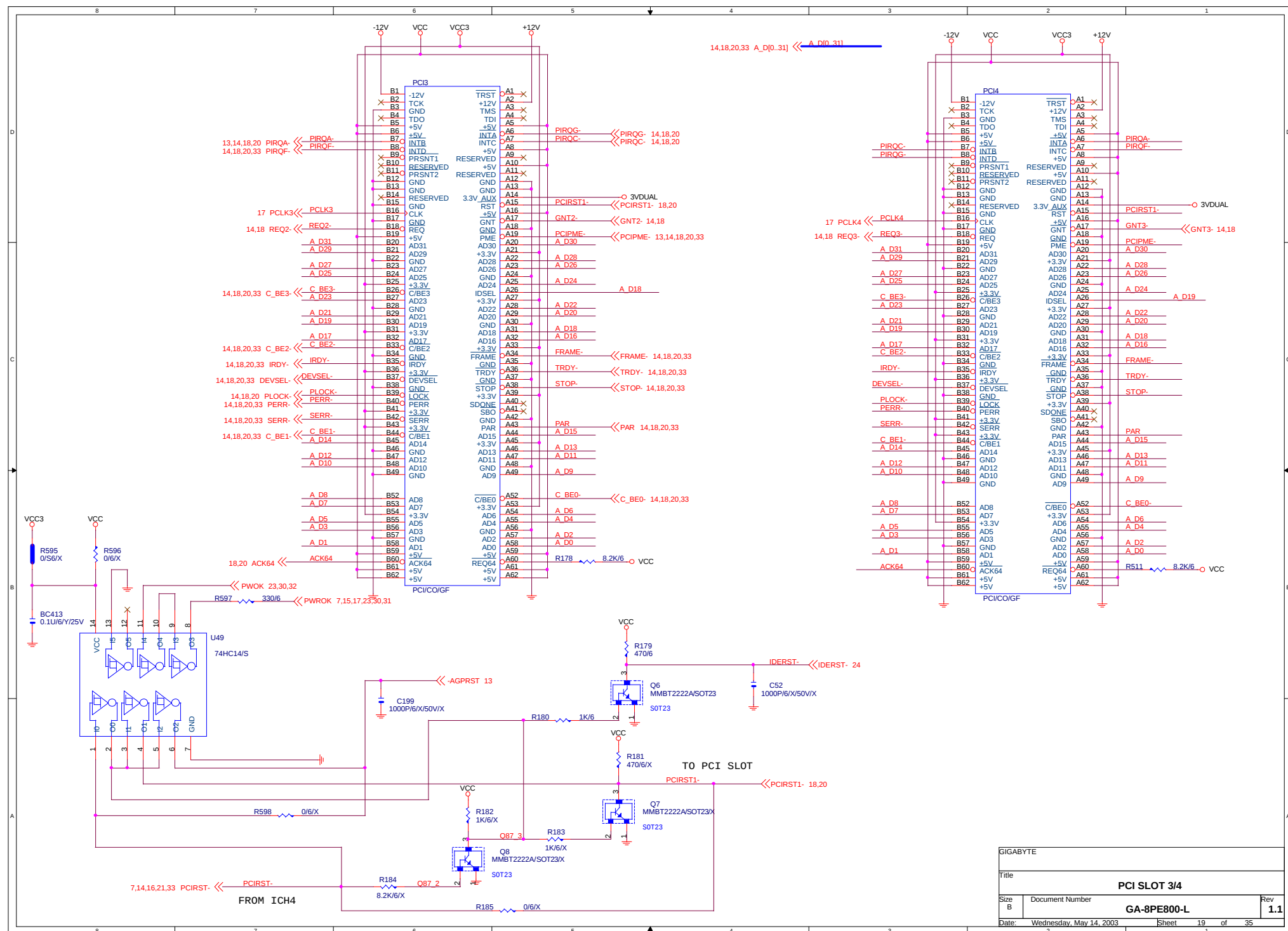
FRAME << FRAME- RN64 8.2K/8P4R
IRDY << IRDY- RN65 8.2K/8P4R
TRDY << TRDY- RN66 8.2K/8P4R
DEVSEL << DEVSEL- RN67 8.2K/8P4R

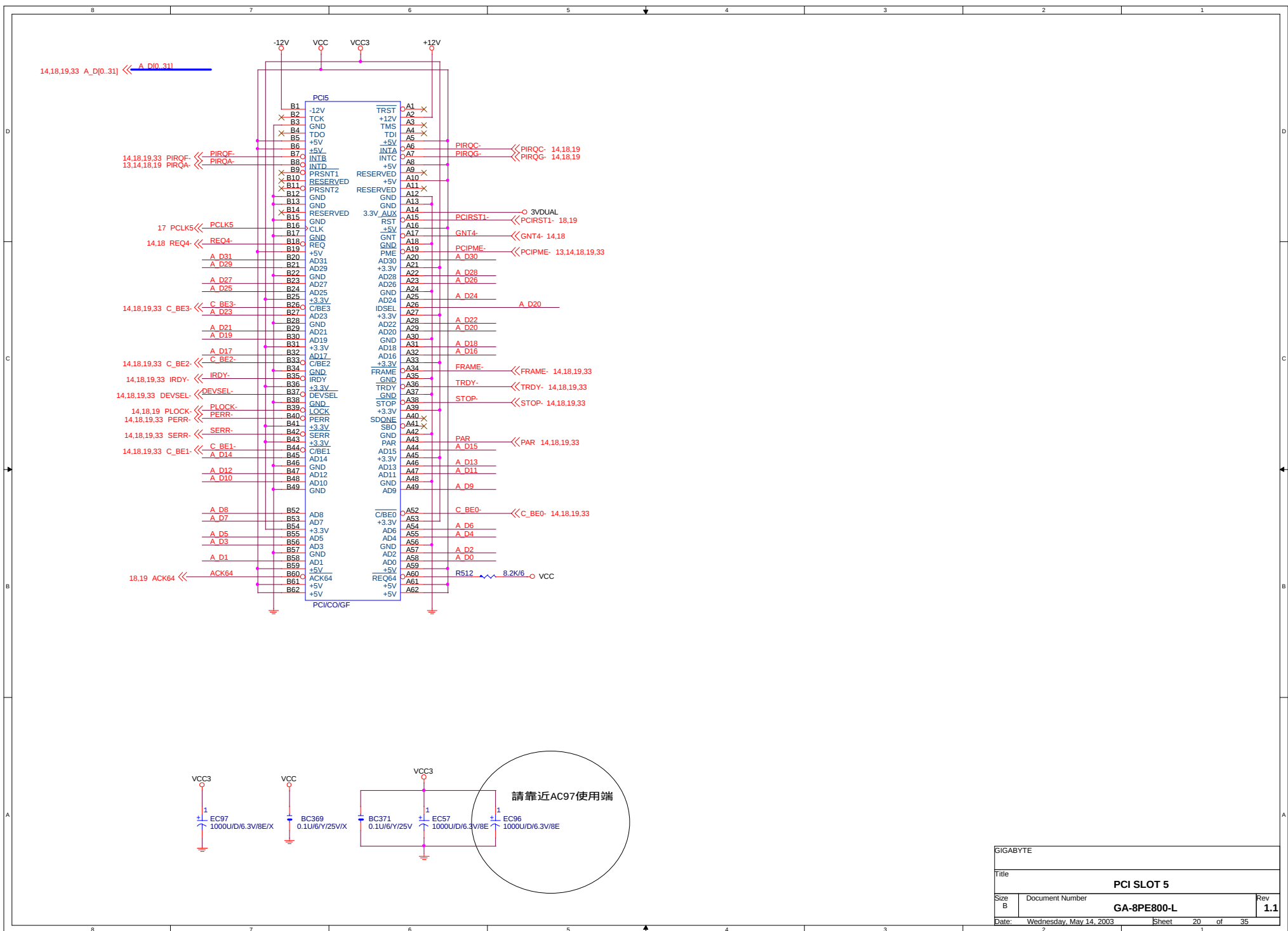
STOP << STOP- RN68 8.2K/8P4R
PLOCK << PLOCK- RN69 8.2K/8P4R
PERR << PERR- RN70 8.2K/8P4R
SERR << SERR- RN71 8.2K/8P4R

14,19 REQ3 << REQ3- RN111 8.2K/8P4R
14,33 REQ5 << REQ5- RN112 8.2K/8P4R
14,20 REQ4 << REQ4- RN113 8.2K/8P4R
14,19 REQ2 << REQ2- RN114 8.2K/8P4R
PAR << PAR- R176 8.2K/6
ACK64 << ACK64- R177 8.2K/6

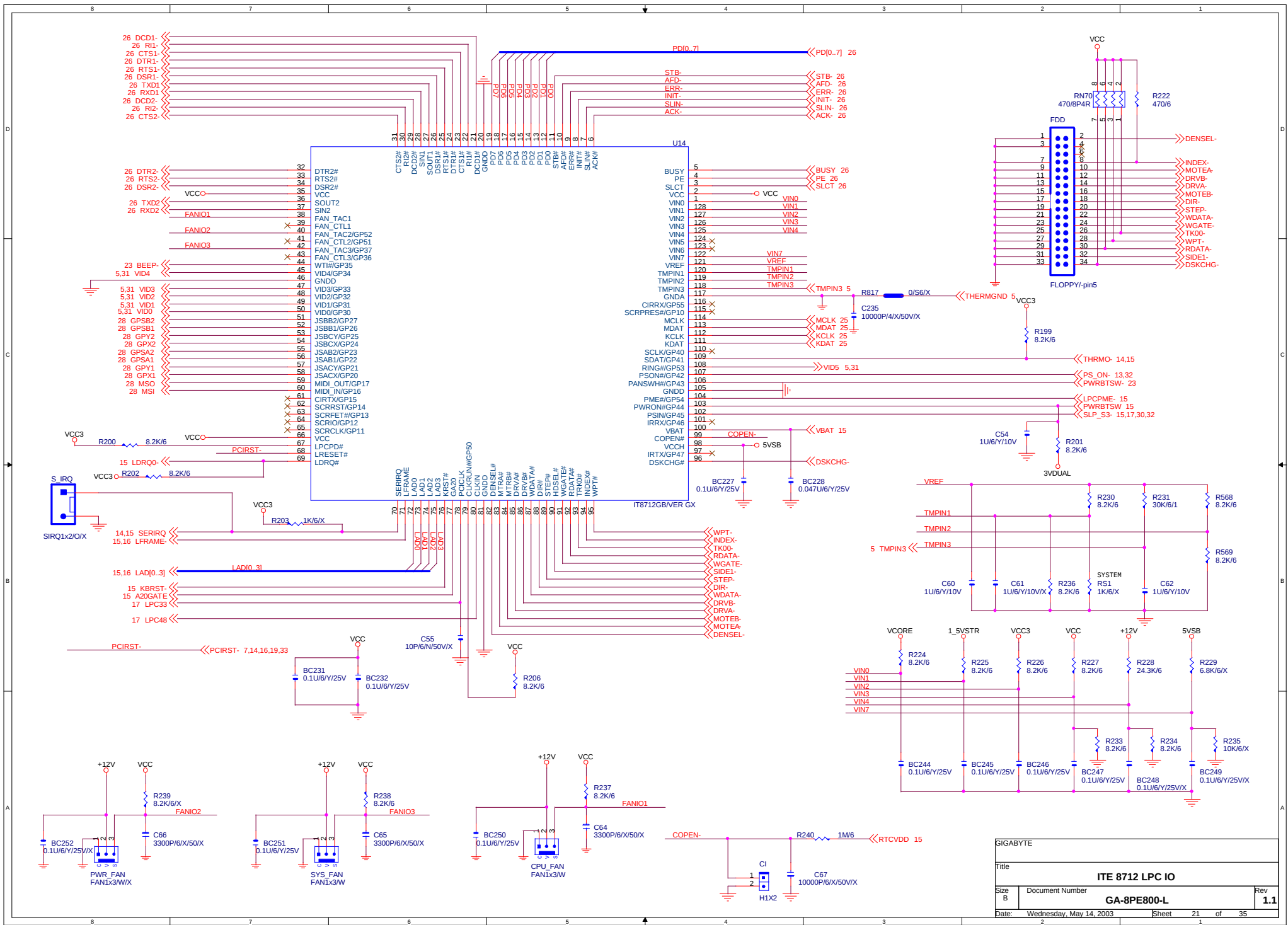


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PCI SLOT 5			
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ITE 8712 LPC IO			
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ICH4 USB2.0

The diagram illustrates the internal circuitry for two USB2.0 ports, L13 and L14, on the ICH4 USB2.0 controller. Both ports share a common FUSEVCC supply and are protected by fuses BC253 and BC254.

Port L13:

- Inputs:** 14 USBP0+, 14 USBP0-, 14 USBP1+, 14 USBP1-.
- Components:** L13 (inductor), OD6560T/S/X (diode), RN117 (resistor), 0/8P4R (connector).
- Outputs:** FUSB0+, FUSB0-, FUSB1+, FUSB1-.
- Internal Connections:** FUSB0+ and FUSB1+ are connected to the positive pins of the 0/8P4R connector. FUSB0- and FUSB1- are connected to the negative pins of the 0/8P4R connector.
- Grounding:** FUSB0- and FUSB1- are also connected to ground.
- Other Components:** BC253 (0.1U/6/Y/25V) fuse, EC12 (100U/D/10V/57) capacitor, H2*5/-9/YELLOW (connector).

Port L14:

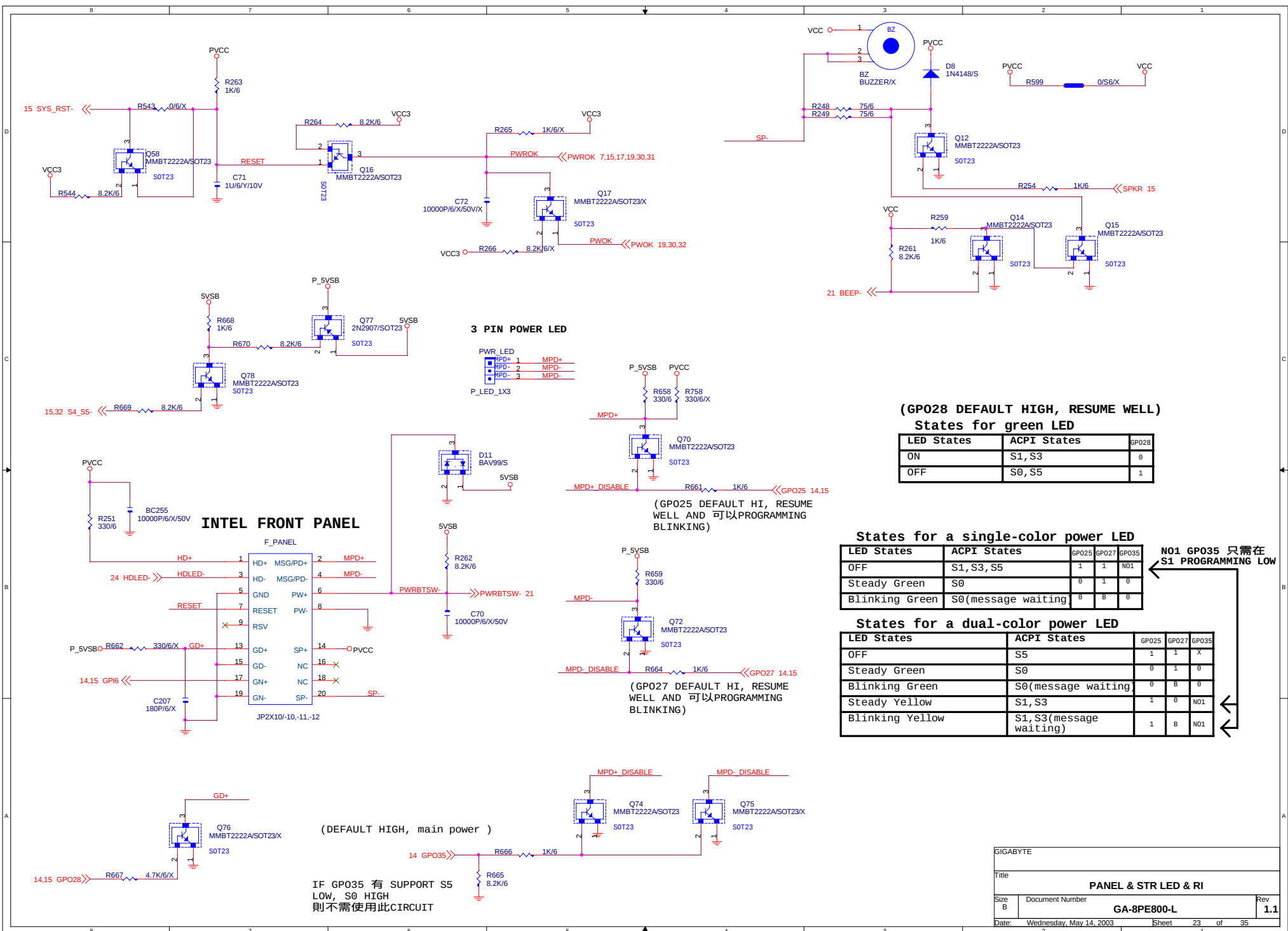
- Inputs:** 14 USBP2+, 14 USBP2-, 14 USBP3+, 14 USBP3-.
- Components:** L14 (inductor), OD6560T/S/X (diode), RN118 (resistor), 0/8P4R (connector).
- Outputs:** FUSB2+, FUSB2-, FUSB3+, FUSB3-.
- Internal Connections:** FUSB2+ and FUSB3+ are connected to the positive pins of the 0/8P4R connector. FUSB2- and FUSB3- are connected to the negative pins of the 0/8P4R connector.
- Grounding:** FUSB2- and FUSB3- are also connected to ground.
- Other Components:** BC254 (0.1U/6/Y/25V) fuse, H2*5/-9/YELLOW (connector).

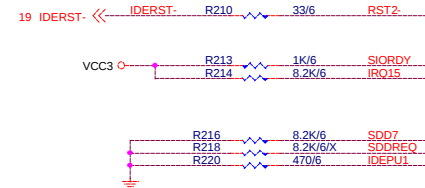
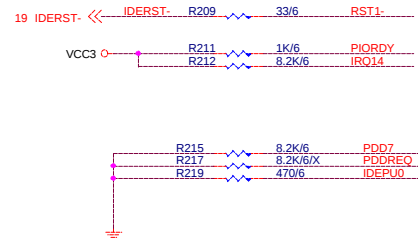
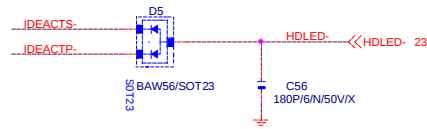
Common Connections:

- FUSEVCC:** Supply voltage for the fuses.
- IUSB0C-:** Common ground connection for the first port.
- IUSB0C-:** Common ground connection for the second port.
- R603:** Resistor connected to the IUSB0C- line.
- USB0C-:** Common ground connection for the second port.
- USB0C- 14,33:** Common ground connection for the second port.

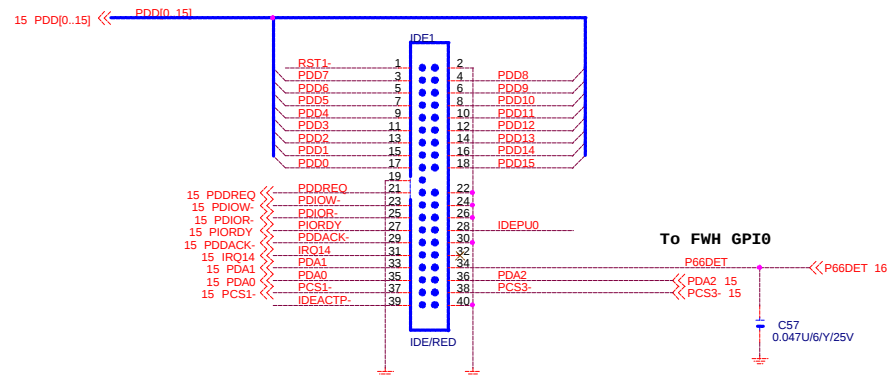
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ICH USB+LAN PORT			
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ICH USB+LAN PORT			
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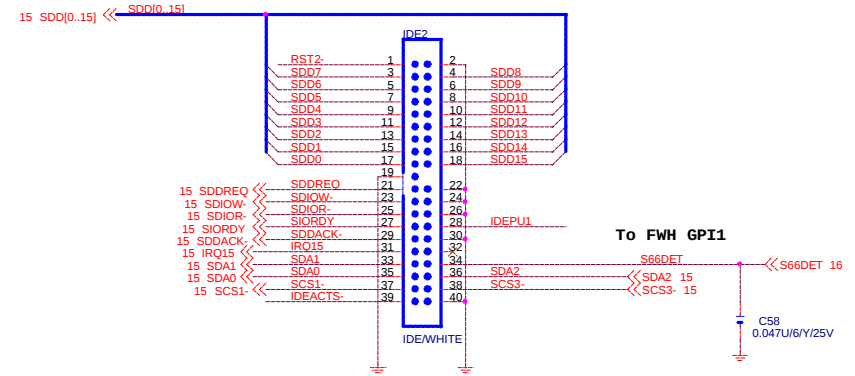




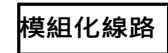
PRIMARY IDE CONNECTOR

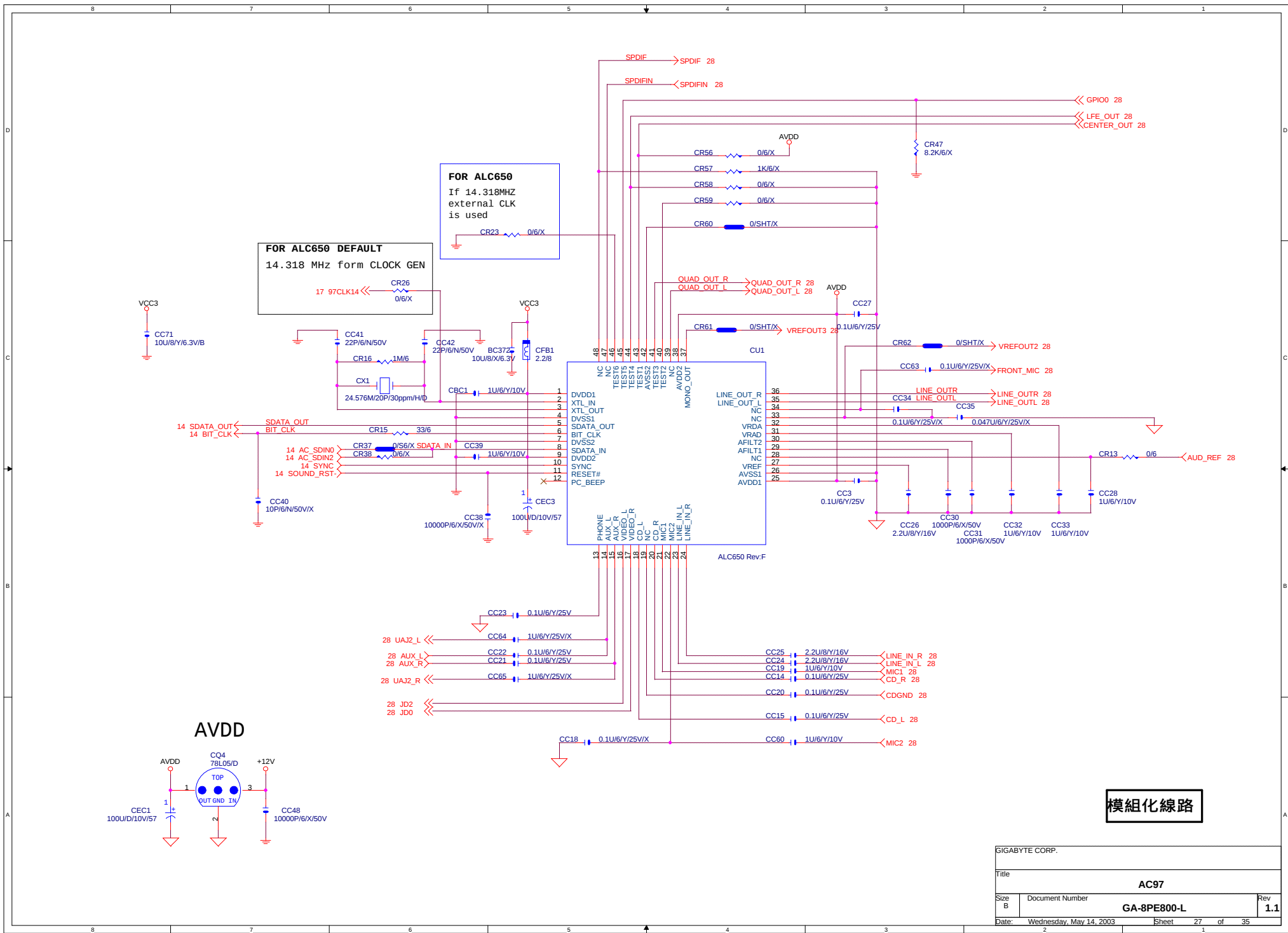


SECONDARY IDE CONNECTOR



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IDE CONNECTOR			
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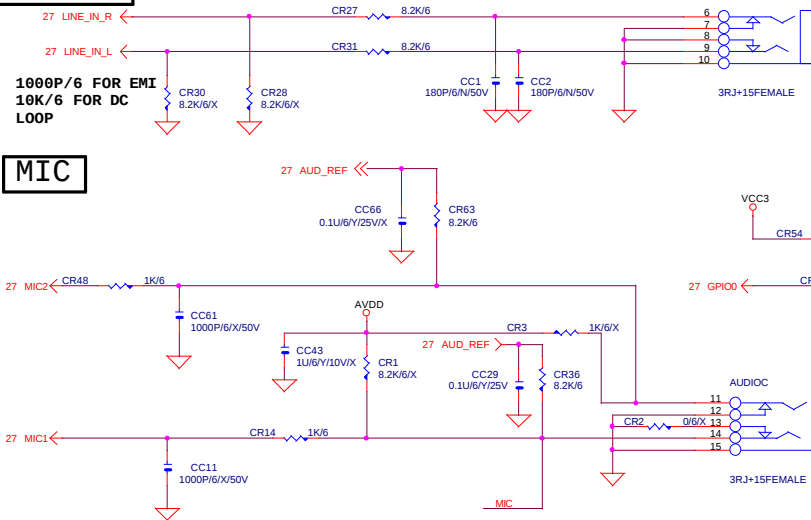




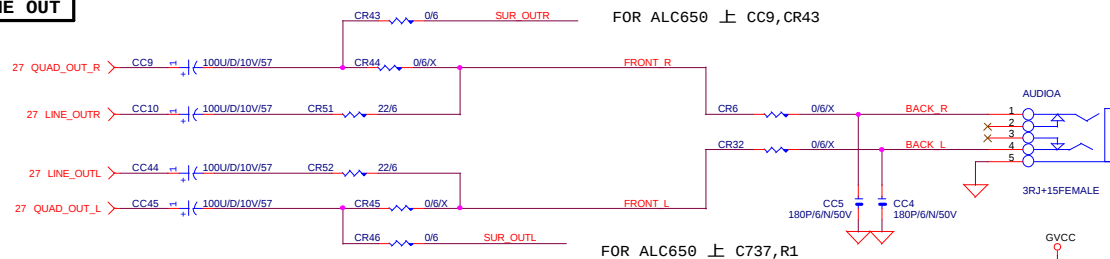
模組化線路

GIGABYTE CORP.			
Title			
AC97			
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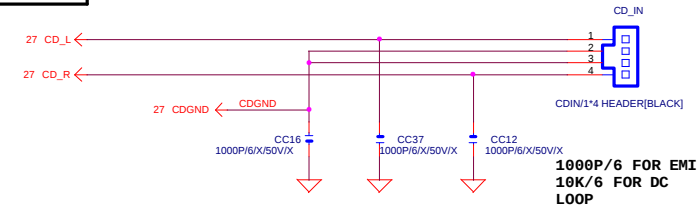
LINE-IN



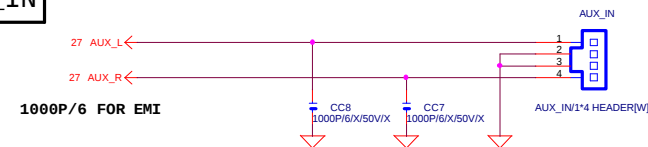
LINE OUT



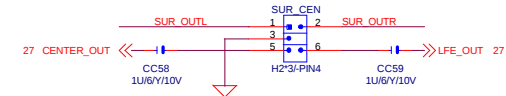
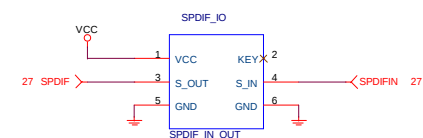
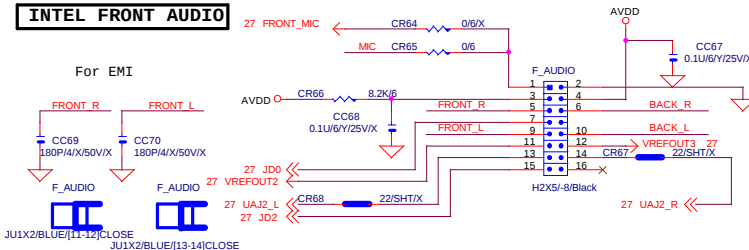
CDIN



AUX_IN



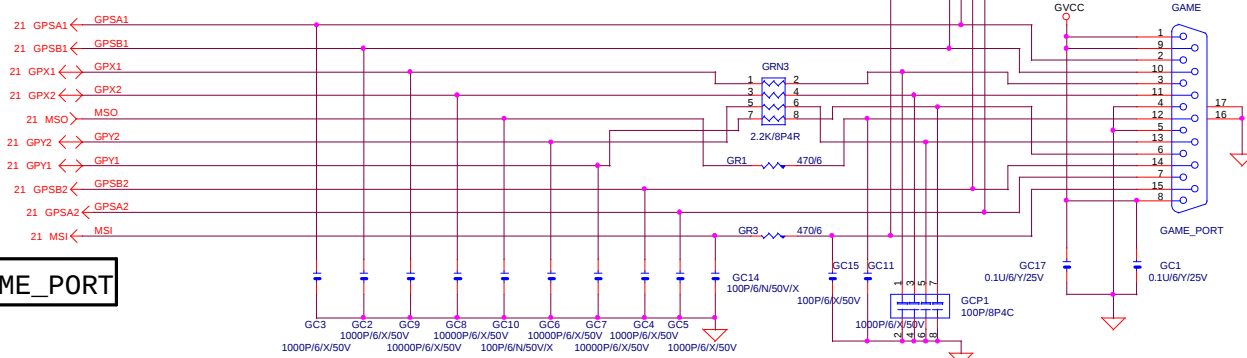
INTEL FRONT AUDIO



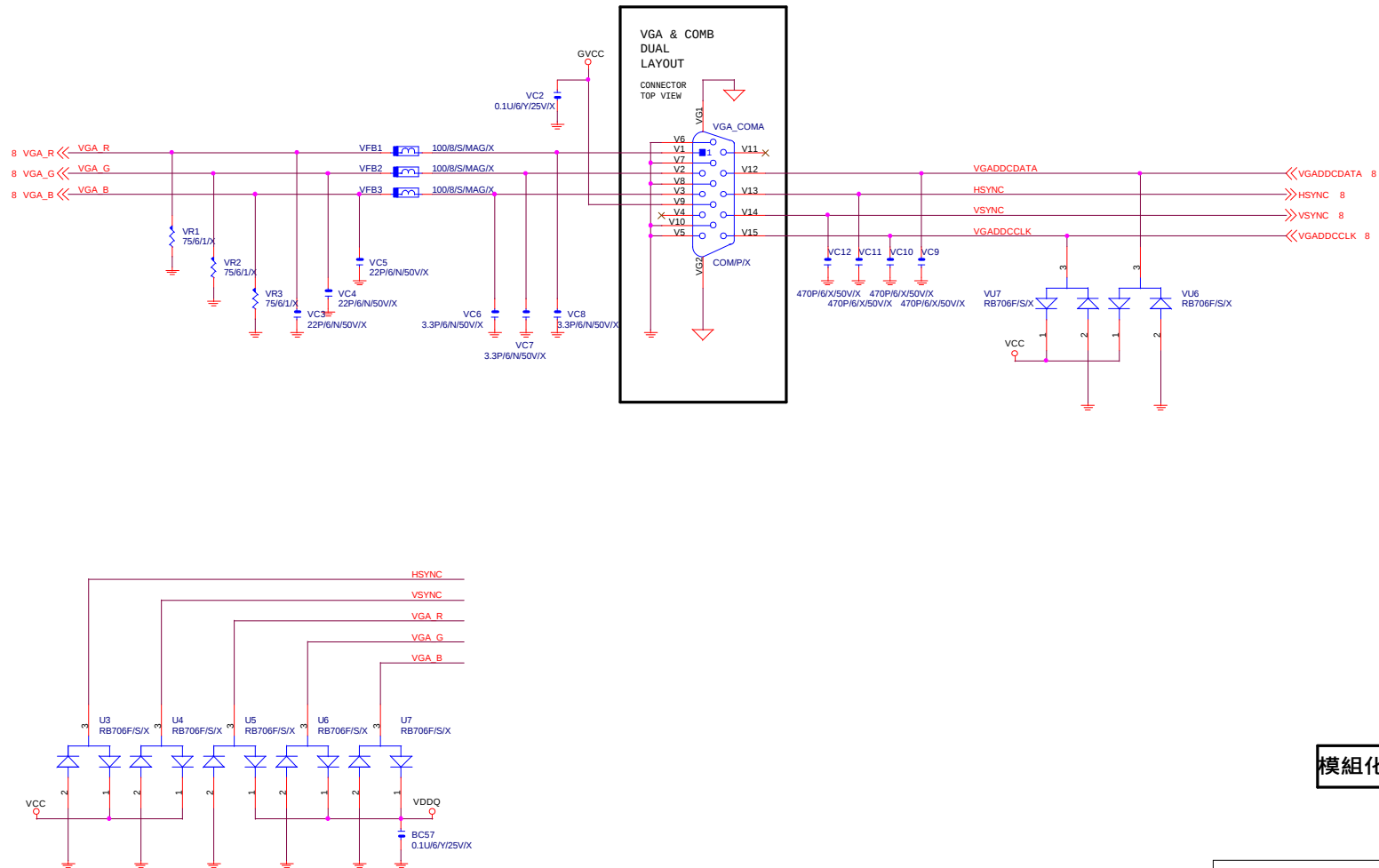
FOR SUPPORT 6 CHANNEL, SURROUND OUT
CENTER OUT, LOW FREQUENCY EFFECT OUT

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GAME_PORT

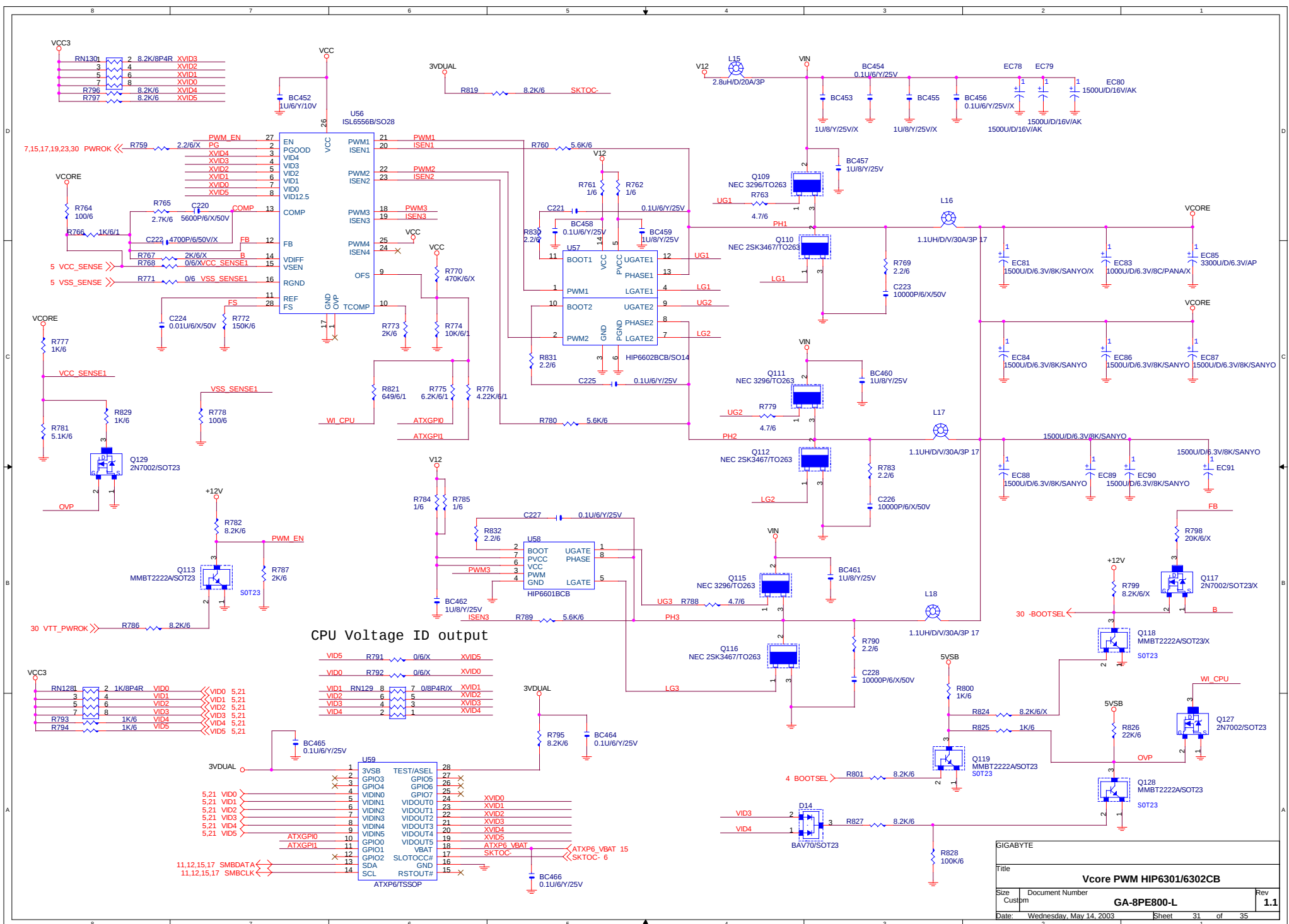


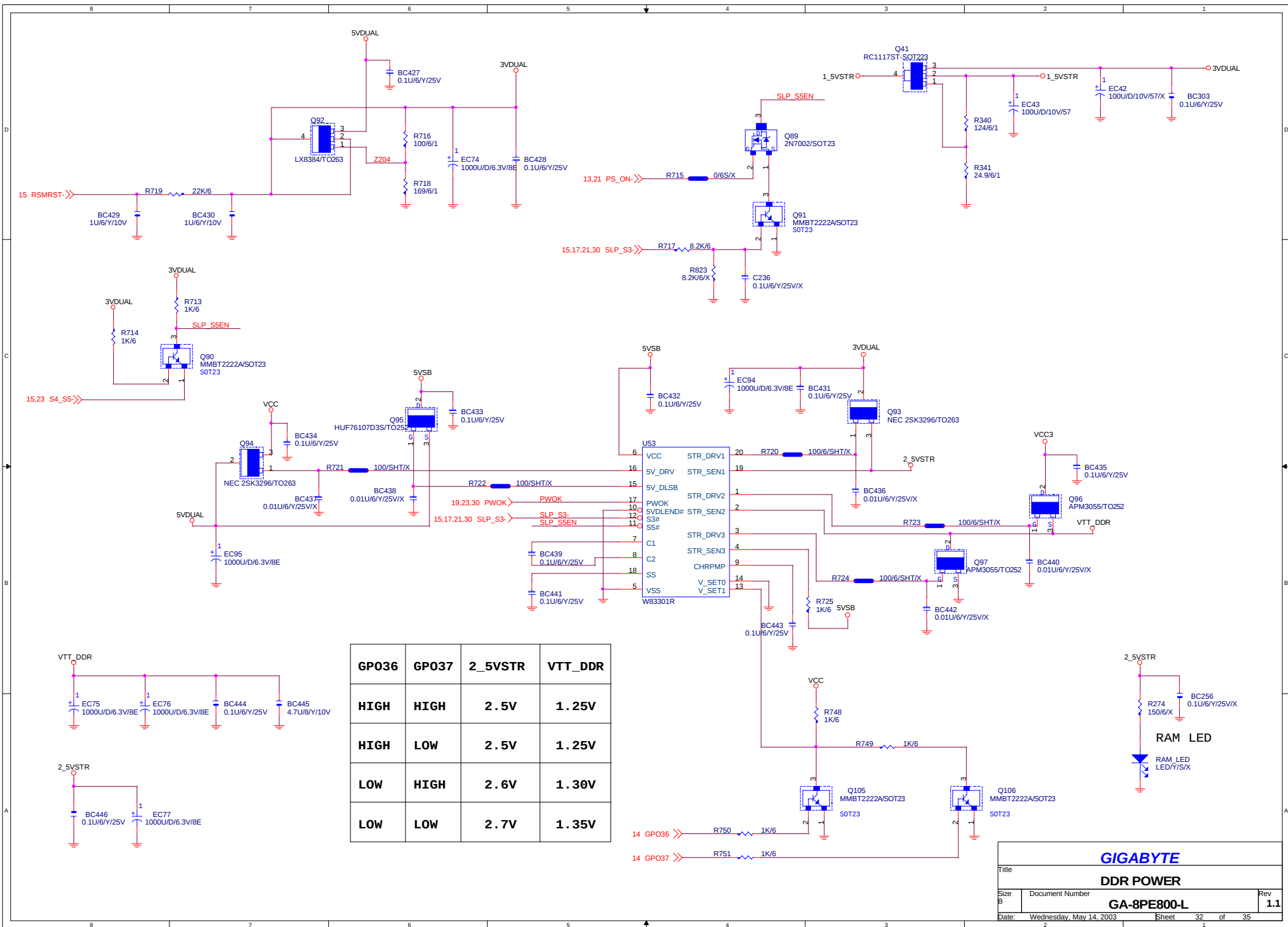
GIGABYTE CORP.			
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PHONE JACK, GAME PORT			
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VGA CONNECTOR			
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POWER DECOUPLING CAP.

The diagram shows two power rails, 3VDD and AVDD33, each with five decoupling capacitors. The 3VDD rail is connected to 3VDDUAL and has capacitors LBC1 through LBC6, each labeled 0.1U/6V/25V. The AVDD33 rail is connected to AVDD33 and has capacitors LBC9 through LBC12, each labeled 0.1U/6V/25V. A component FB5, labeled 30R/5, is connected between the 3VDD and AVDD33 rails.

LAN EEPROM

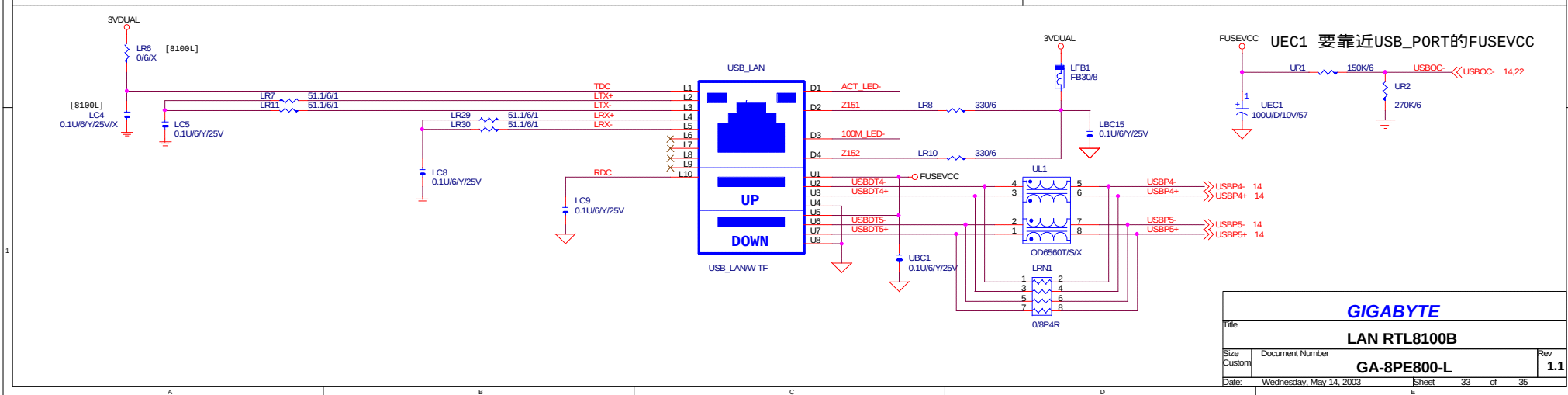
Circuit diagram showing the LAN EEPROM (93C46) connected to a 3V DUAL supply. The chip is labeled L112 and 93C46. The connections are as follows:

- Pin 1: L_EECS
- Pin 2: L_EESK
- Pin 3: L_EEDI
- Pin 4: L_EEDO
- Pin 5: GND
- Pin 6: NC
- Pin 7: NC
- Pin 8: VCC

A 3V DUAL supply is connected to pin 8. A 0.1uF/25V capacitor is connected between pin 8 and pin 5. The chip is also labeled LBC14.

8100/8100B NOTE:

- Pin 65 pull-down (5.6K for 8100B)
- Pin 65 pull-down (1.8K for 8100)
- R502 remove pull-down (1.8K for 8100B)
- R502:0/6 pull-down (1.8K for 8100)



GIGABYTE GA-8PE667 PCI ROUNTING LIST *Revision : 0.1*

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT	
PCI SLOT1	16	C, F, G, A	PCLK1	REQ0 -	GNT0 -	
PCI SLOT2	17	F, G, A, C	PCLK2	REQ1 -	GNT1 -	
PCI SLOT3	18	G, A, C, F	PCLK3	REQ2 -	GNT2 -	
PCI SLOT4	19	A, C, F, G	PCLK4	REQ3 -	GNT3 -	
PCI SLOT5	20	C, F, G, A	PCLK5	REQ4 -	GNT4 -	
LAN	21	F	LANCLK	REQ5 -	GNT5 -	

GIGABYTE		
Title		
PCI ROUNT LIST		
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GIGABYTE GA-8PE667 GPIO LIST

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SHEET TITLE

GPI		
GPI0/REQA-		PULL DOWN 15K, detect IDE1 connector type.
GPI1/REQ5-		PULL DOWN 15K, detect IDE2 connector type.
GPI2/PIRQE-		PULL 8.2K TO VCC3
GPI3/PIRQF-		PULL 8.2K TO VCC3
GPI4/PIRQG-		PULL 8.2K TO VCC3
GPI5/PIRQH-		PULL 8.2K TO VCC3
GPI6		PULL 8.2K TO VCC3 (GREEN_BUTTON)
GPI7		NOT IMPLEMENTED
GPI8		PULL 8.2K TO 3VDUAL, LPC PME.
GPI9	NA	NOT IMPLEMENTED
GPI10	NA	NOT IMPLEMENTED
GPI11		PULL 4.7K TO 3VDUAL (SMBALERT)
GPI12		PULL DOWN 10K.
GPI13		PULL DOWN 10K, CNR_PRIMARY
GPI14	NA	NOT IMPLEMENTED
GPI15	NA	NOT IMPLEMENTED

SHEET TITLE

GPO		
GP016		PULL 8.2K TO VCC3
GP017		PULL 8.2K TO VCC3 (GNT5-)
GP018		PULL 8.2K TO VCC3
GP019		PULL 8.2K TO VCC3
GP020		PULL 8.2K TO VCC3
GP021		PULL 8.2K TO VCC3
GP022		PULL 8.2K TO VCC3
GP023		PULL 8.2K TO VCC3
GP024		PULL 1K TO 3VDUAL (TOP BLOCK)
GP025		PULL 4.7K TO 3VDUAL, POWER LED CONTROL.
GP026		NOT IMPLEMENTED
GP027		PULL 8.2K TO 3VDUAL, POWER LED CONTROL.
GP028		PULL 8.2K TO 3VDUAL, GREEN LED.
GP032		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GP035		PULL DOWN 10K, POWER LED CONTROL.