8INXP 6 layer Schematics

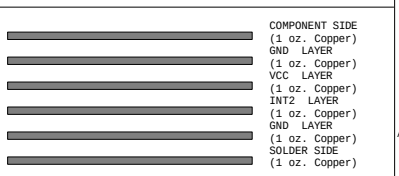
Revision 1.01

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_NORTHWOOD_478
7-10	MCH(GRANITE BAY) HOST; DDR; AGP,HUB LINK
11-13	ICH4
14	CLOCK GENERATOR (ICS950223)
15-17	DDR SDRAM DIMMS 1-4,TERMINATOR
18	AGP SLOT
19,20	PCI SLOT 1,2,3,4,5
21	IDE,FRONT USB,PCIRST#
22	LPCIO_IT8712
23	DUAL BIOS
24	COM,PRT,FDD,KB/MS,IR
25	AC97(ALC650)
26	AUDIO JACK,GAME PORT
27	FAN, H/W MONITOR
28	PANEL,STR LED,FANS ,CPU GN
29	VCORE PHASE PWM HIP 6301 + 6601
30	DDR POWER,3VDUAL,VDDQ DC POWER
31	ATX CONN, DC POWER
32	KINNERETH R / KENAI 32

SHEET	TITLE
33	SERIAL ATA
34	PROMISE 20276-1
35	PROMISE 20276-1
36	DUAL POWER
37	BOM & PCB MODIFY HISTORY (2)
38	BOM & PCB MODIFY HISTORY (3)

ICH4 GPIO	FUNCTION	I/O	DEFAULT	HIGH	LOW	POWER PLANE
GPIO39	VRM FAN CTL	O	H	ENABLE	DISABLE	MAIN
GPIO41	GREEN LED	O	H	DISABLE	ENABLE	RESUME
GPIO7	DUAL BIOS	I	H	MAIN BIOS	BACKUP BIOS	MAIN
GPIO6	GREEN BTN	I	H	NORMAL	GREEN	MAIN
GPIO13	CNR PRIMARY DOWN	I	L	PRIMARY	SECONDARY	MAIN
GPIO19	DUAL BIOS	O	H	DEFAULT	MAIN BIOS	MAIN
GPIO20	DUAL BIOS	O	H	DEFAULT	BACKUP BIOS	MAIN
GPIO21	4 OR 6 CHANNEL	O	H	4 CHANNEL	6 CHANNEL	MAIN
GPIO24	LAN ENABLE	O	H	ENABLE	DISABLE	RESUME
GPIO25	POWER LED	O	H	PAGE 28	PAGE 28	RESUME
GPIO27	POWER LED	O	H	PAGE 28	PAGE 28	RESUME
GPIO28	DDR O.V.	O	H	DISABLE	ENABLE	RESUME
GPIO32	BIOS W.P.	O	H	PAGE 30	PAGE 30	MAIN
GPIO34	CPU O.V.	O	H	VID VOLTAGE	OVER VOLTAGE	MAIN
GPIO35	POWER LED	O	H	PAGE 28	PAGE 28	MAIN
GPIO36	AGP O.V.	O	H	PAGE 30	PAGE 30	MAIN
GPIO37	AGP O.V.	O	H	PAGE 30	PAGE 30	MAIN
GPIO38	DUAL POWER EN	O	H	DISABLE	ENABLE	MAIN
GPIO43	CLR PASSWORD	I	L	CLEAR	NORMAL	MAIN
ITE GPIO	FUNCTION	I/O	DEFAULT	HIGH	LOW	POWER PLANE
GP40	DDR O.V.	O	H	PAGE 30	PAGE 30	RESUME
GP53	DUAL POWER SEL	O	H	DISABLE	ENABLE	RESUME

PCB Size: 305*244 mm



GIGABYTE

Title: **COVER SHEET**

Size: Custom | Document Number: **GA-8INXP** | Rev: **1.01**

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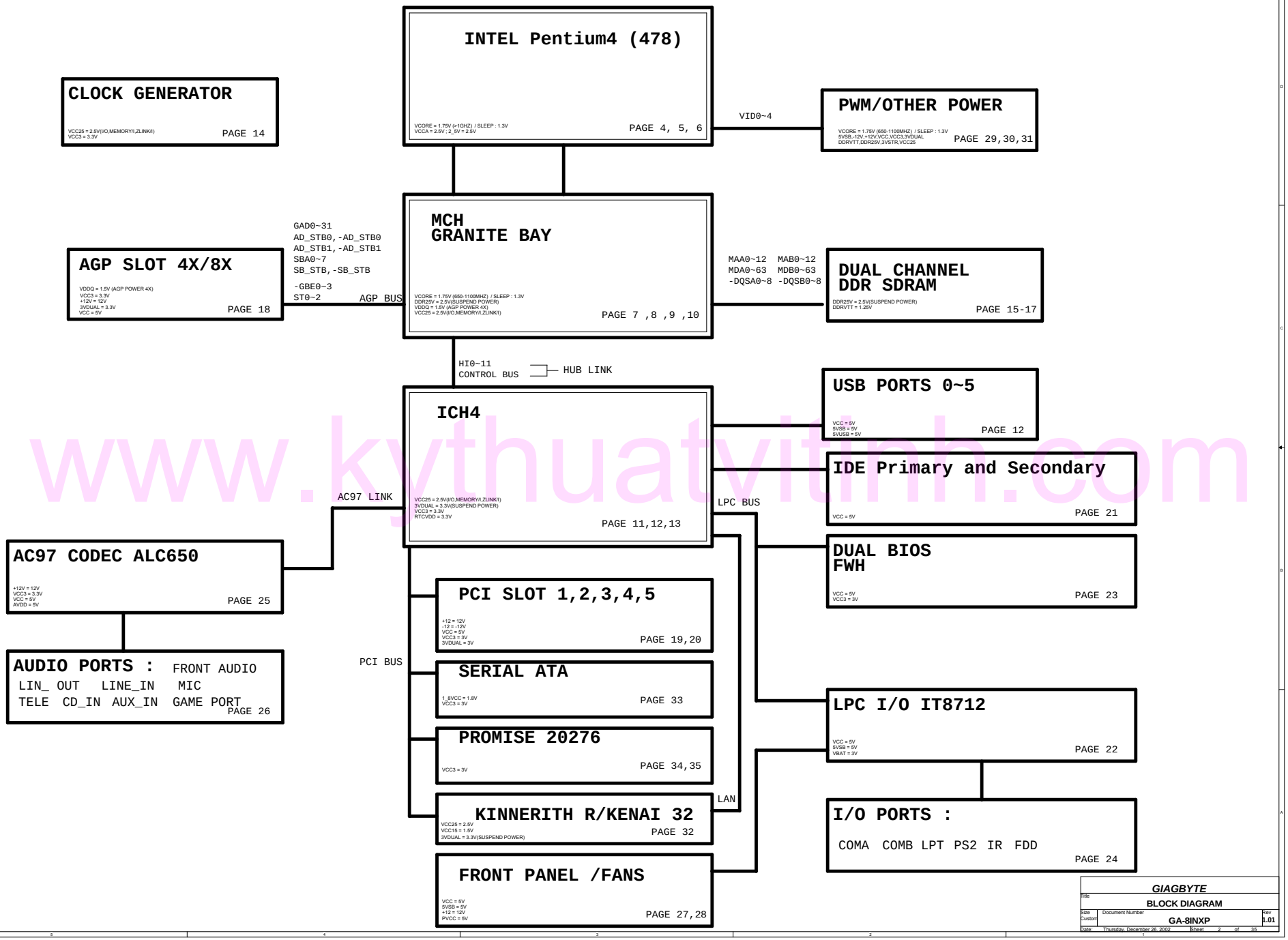
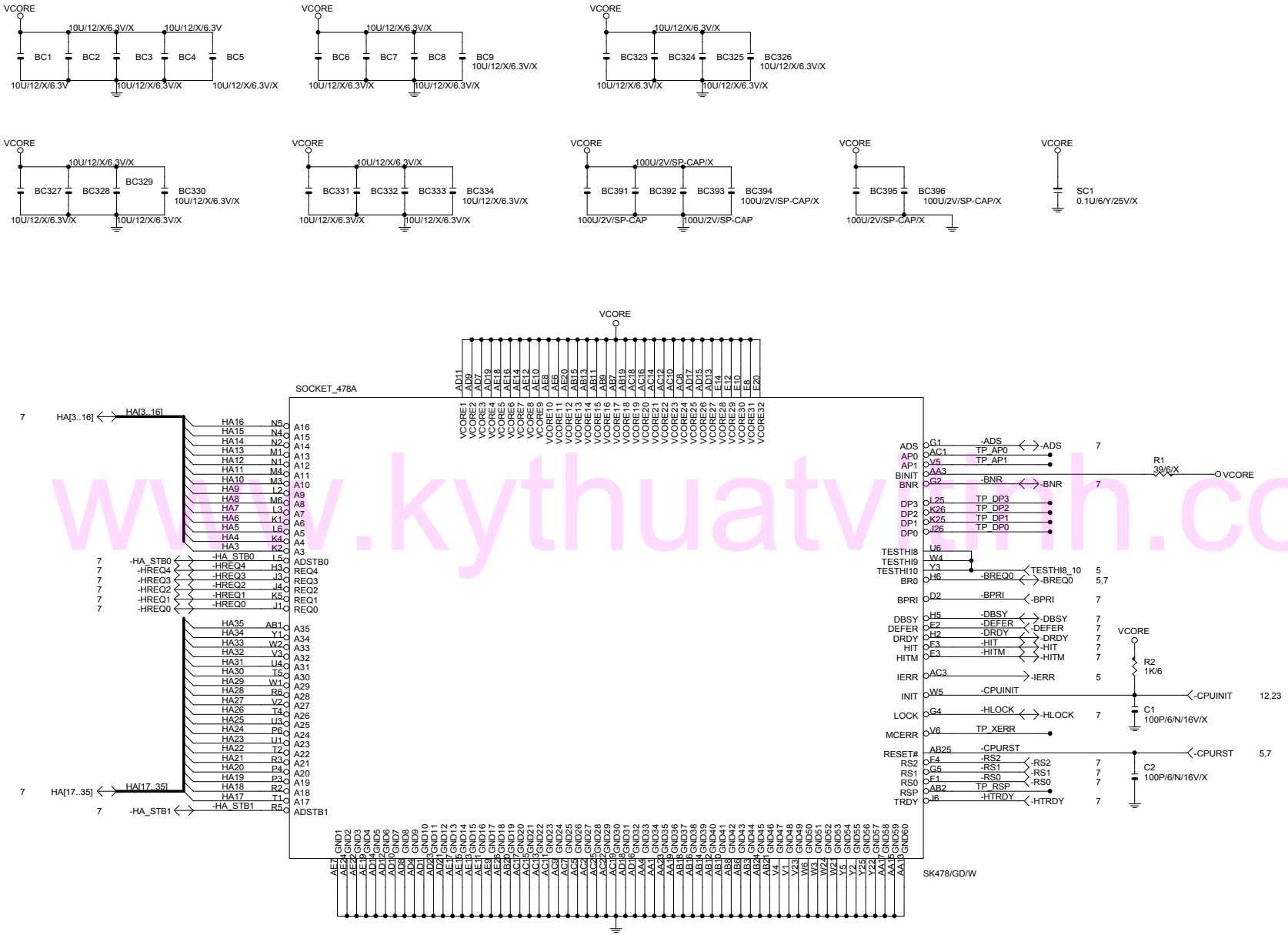
8INXP BLOCK DIAGRAM





GIGABYTE			
Title	NORTHWOOD 1/3		
Size B	Document Number GA-8INXP		Rev 1.01
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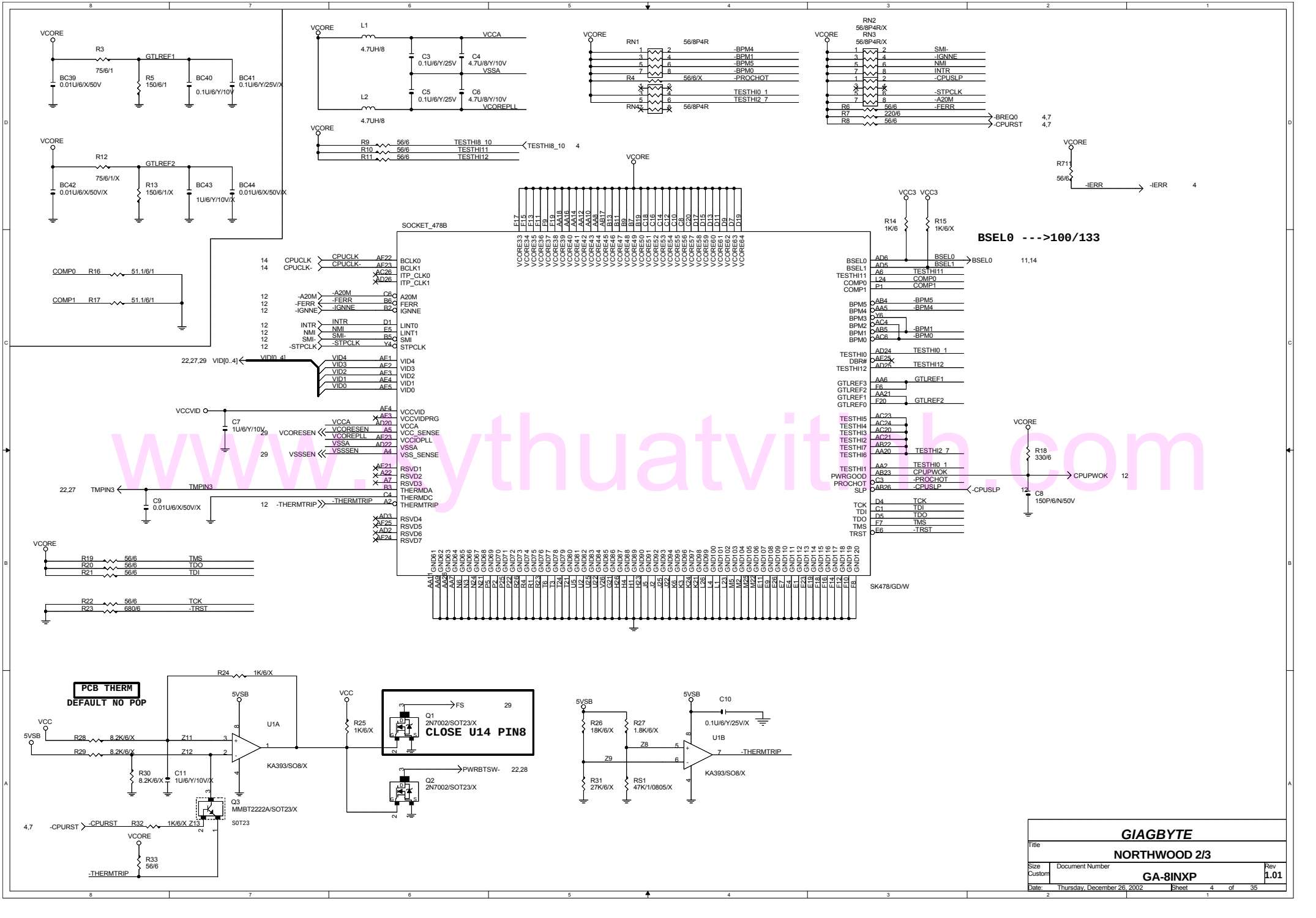
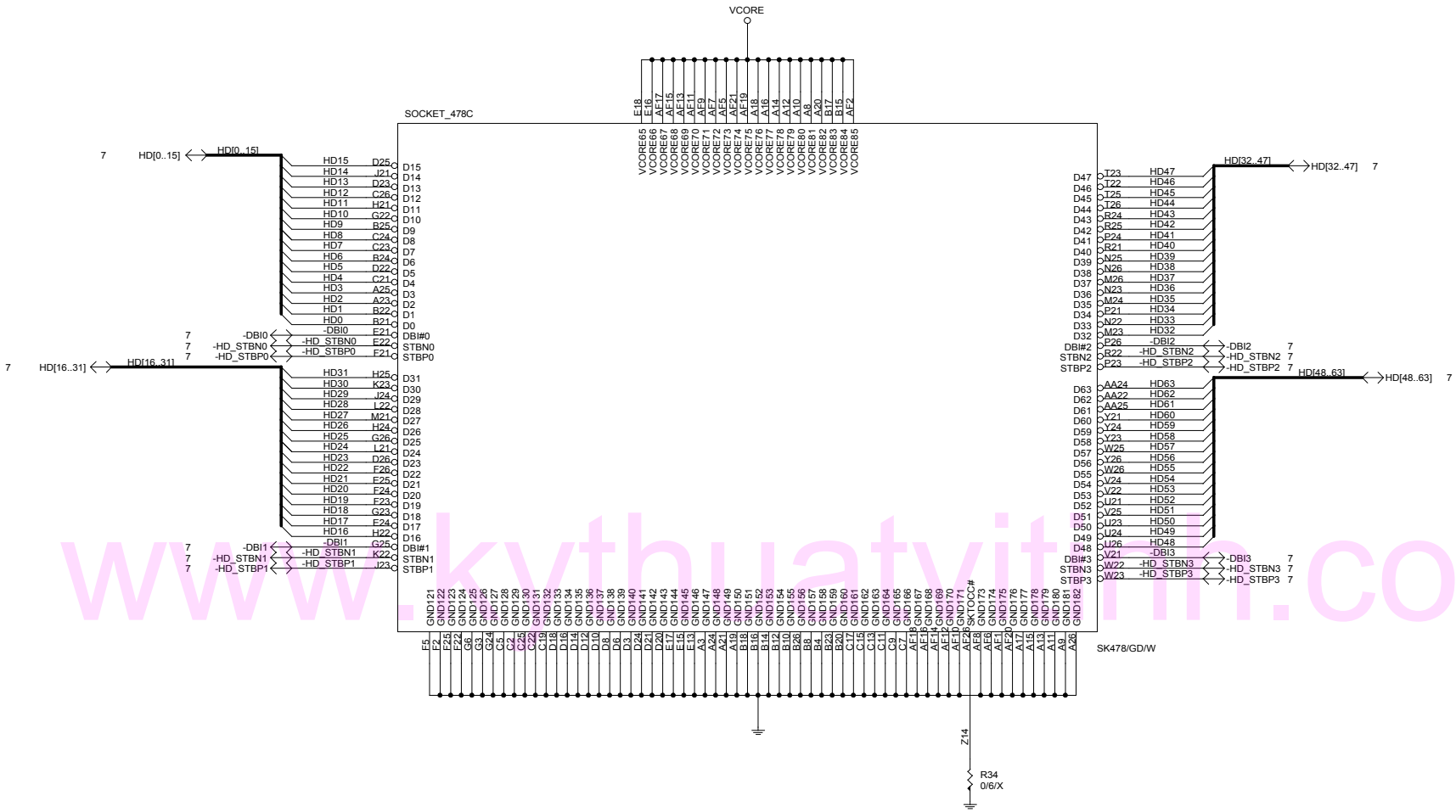
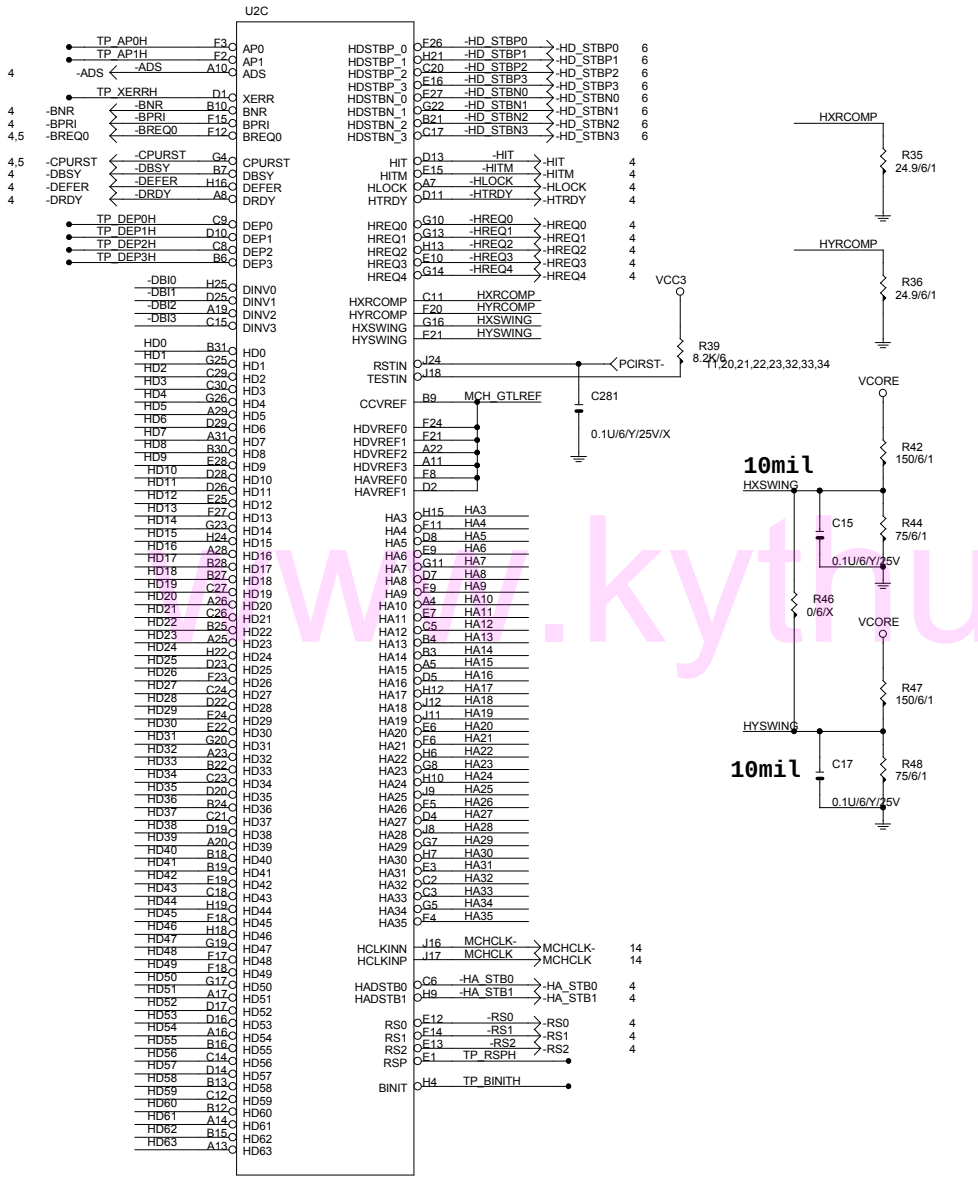


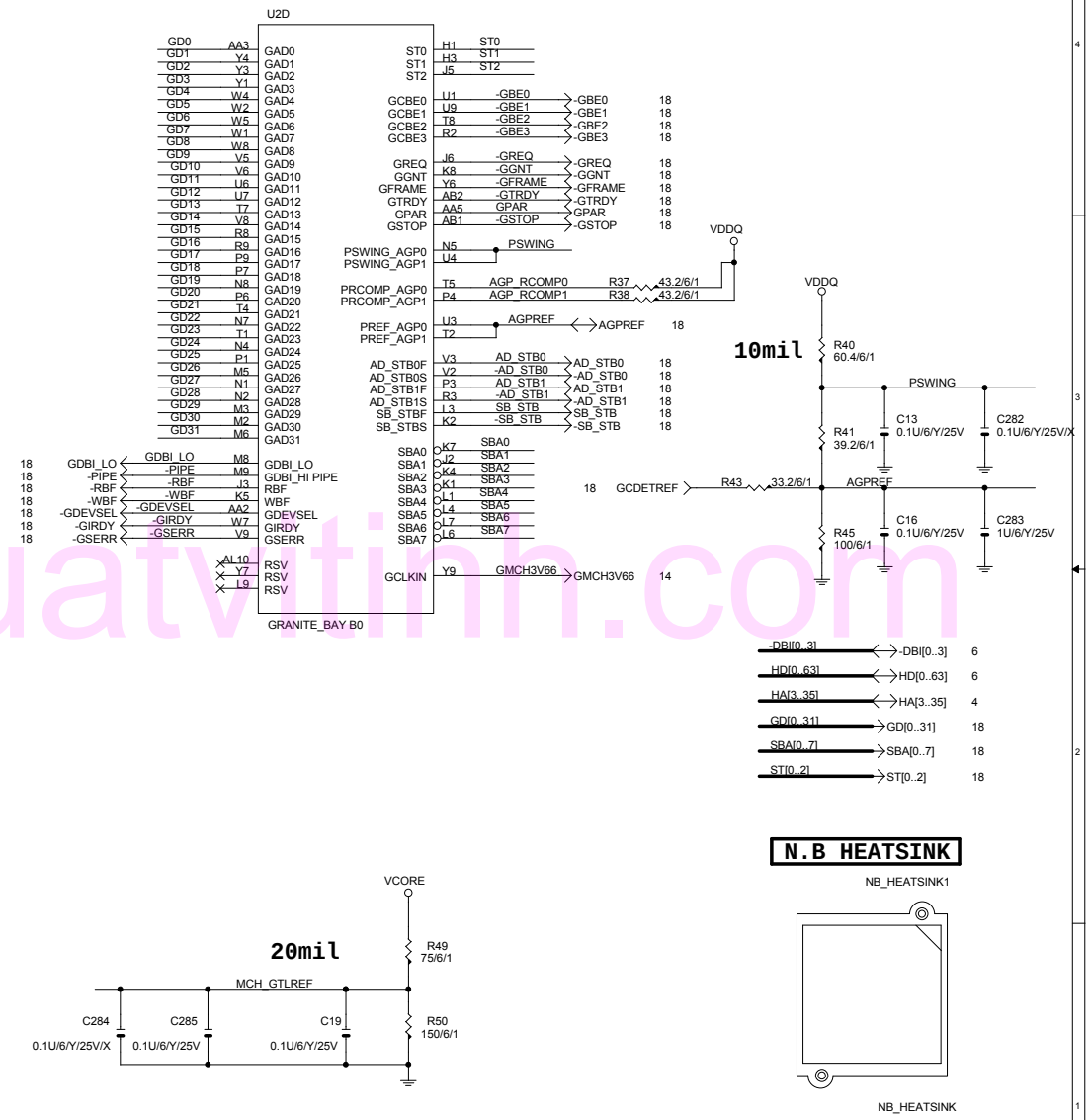


GIGABYTE		
Title	NORTHWOOD 3/3	
Size B	Document Number GA-8INXP	Rev 1.01
Date: Thursday, December 26, 2002	Sheet 5 of 35	

HOST



AGP



N.B HEATSINK

Title	GRANITE (HOST/AGP)
Size: Custom	Document Number: GA-8INXP
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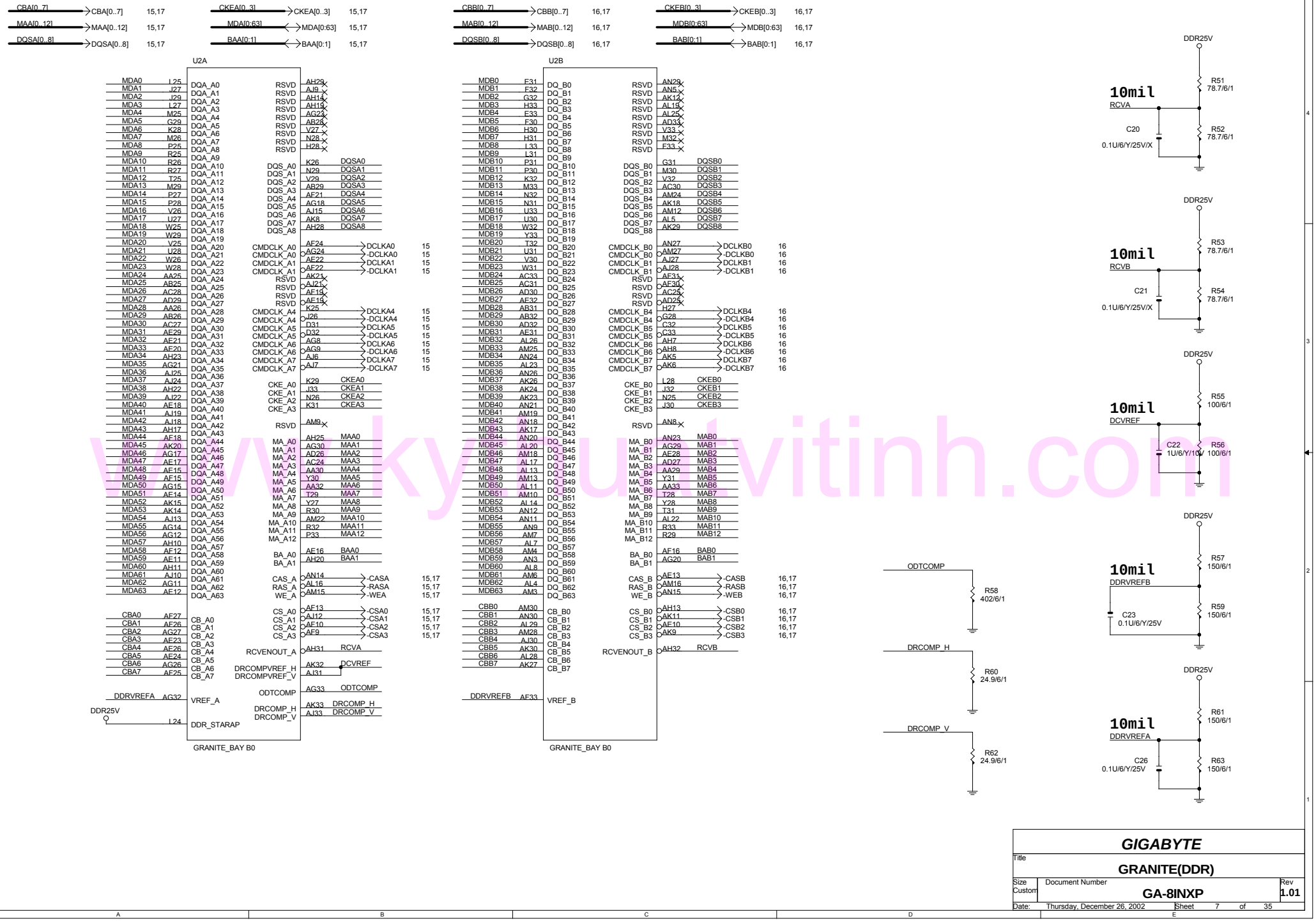
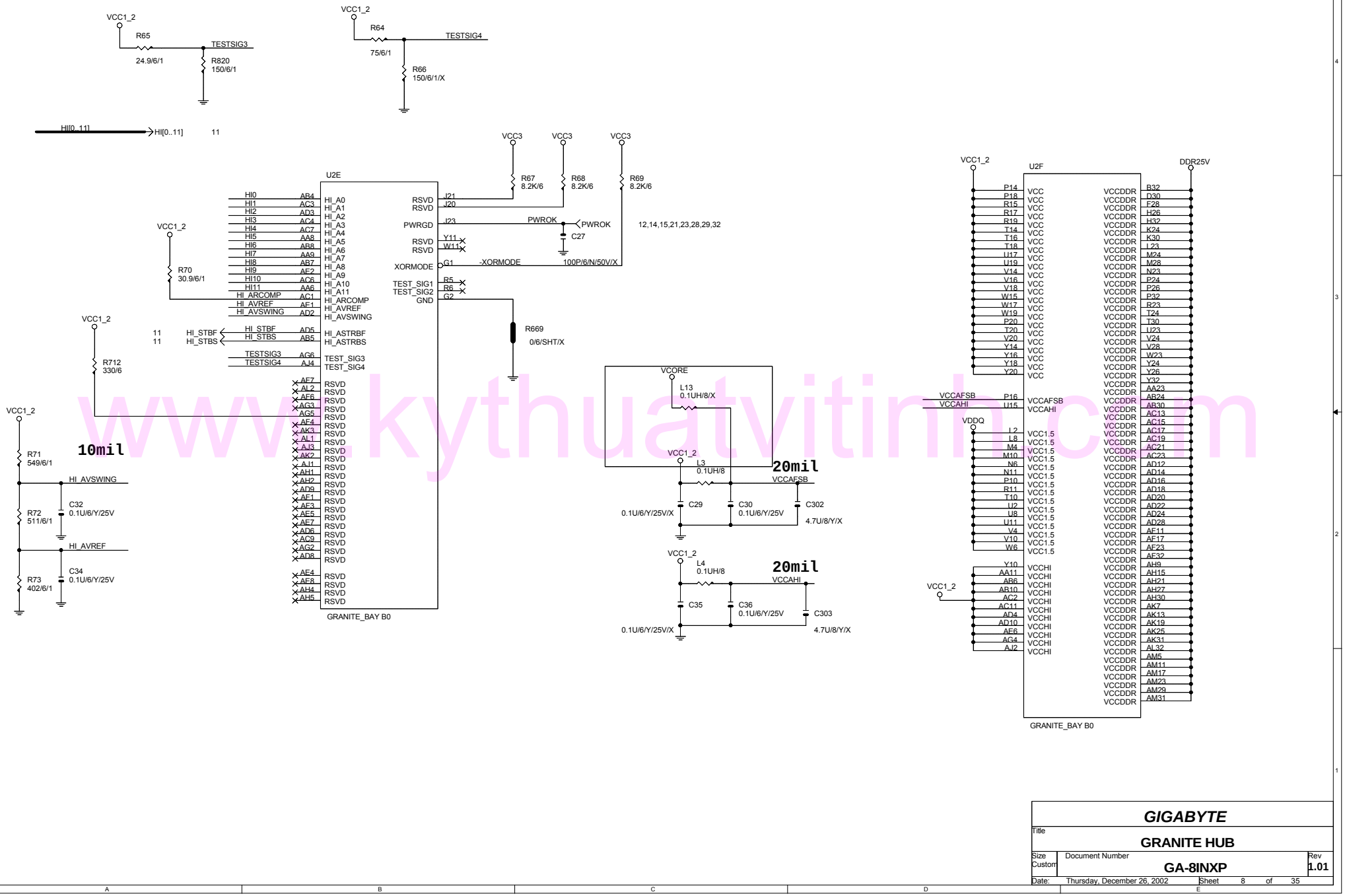
GIGABYTE





GIGABYTE		
Title: GRANITE HUB		
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
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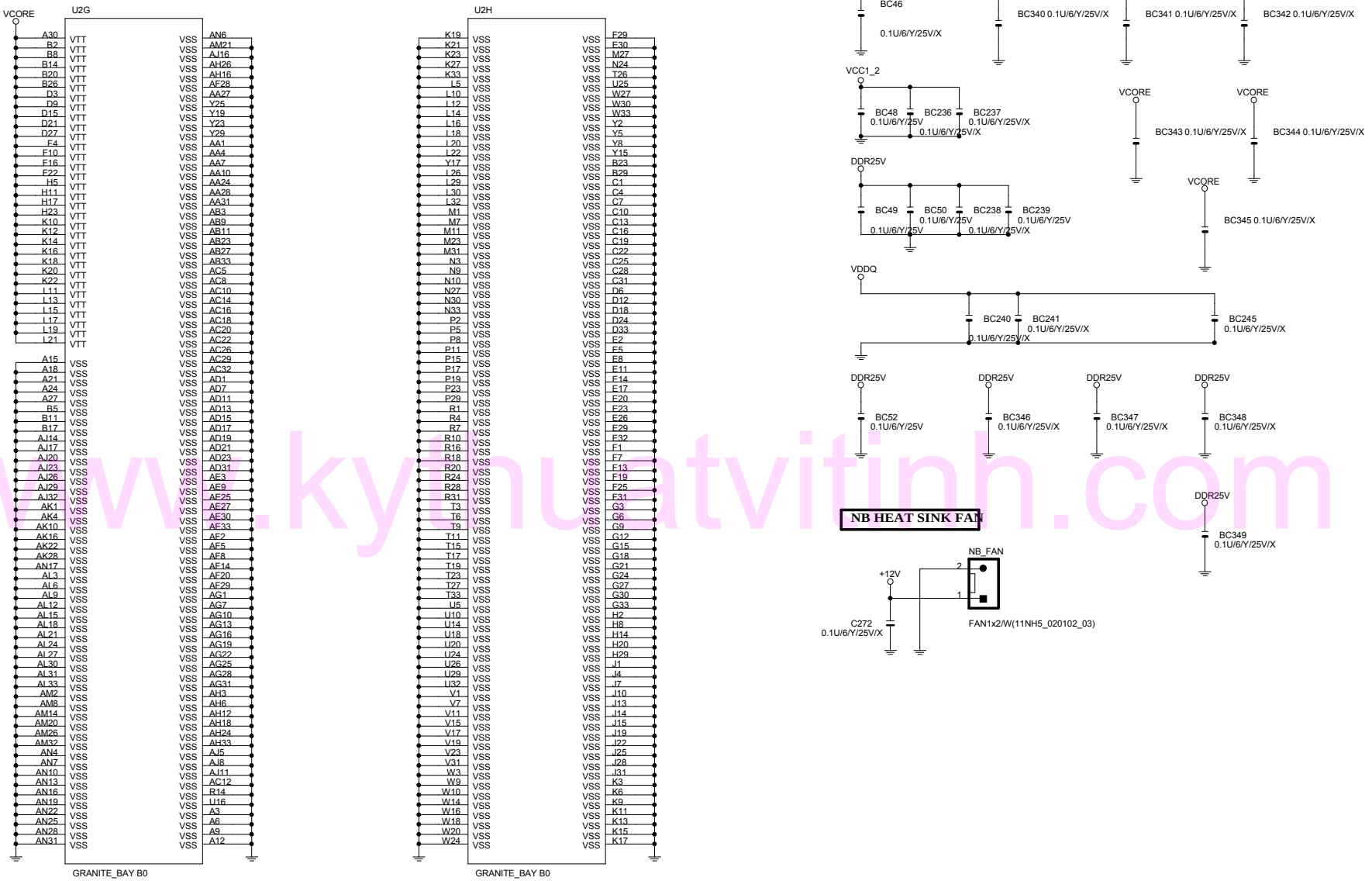

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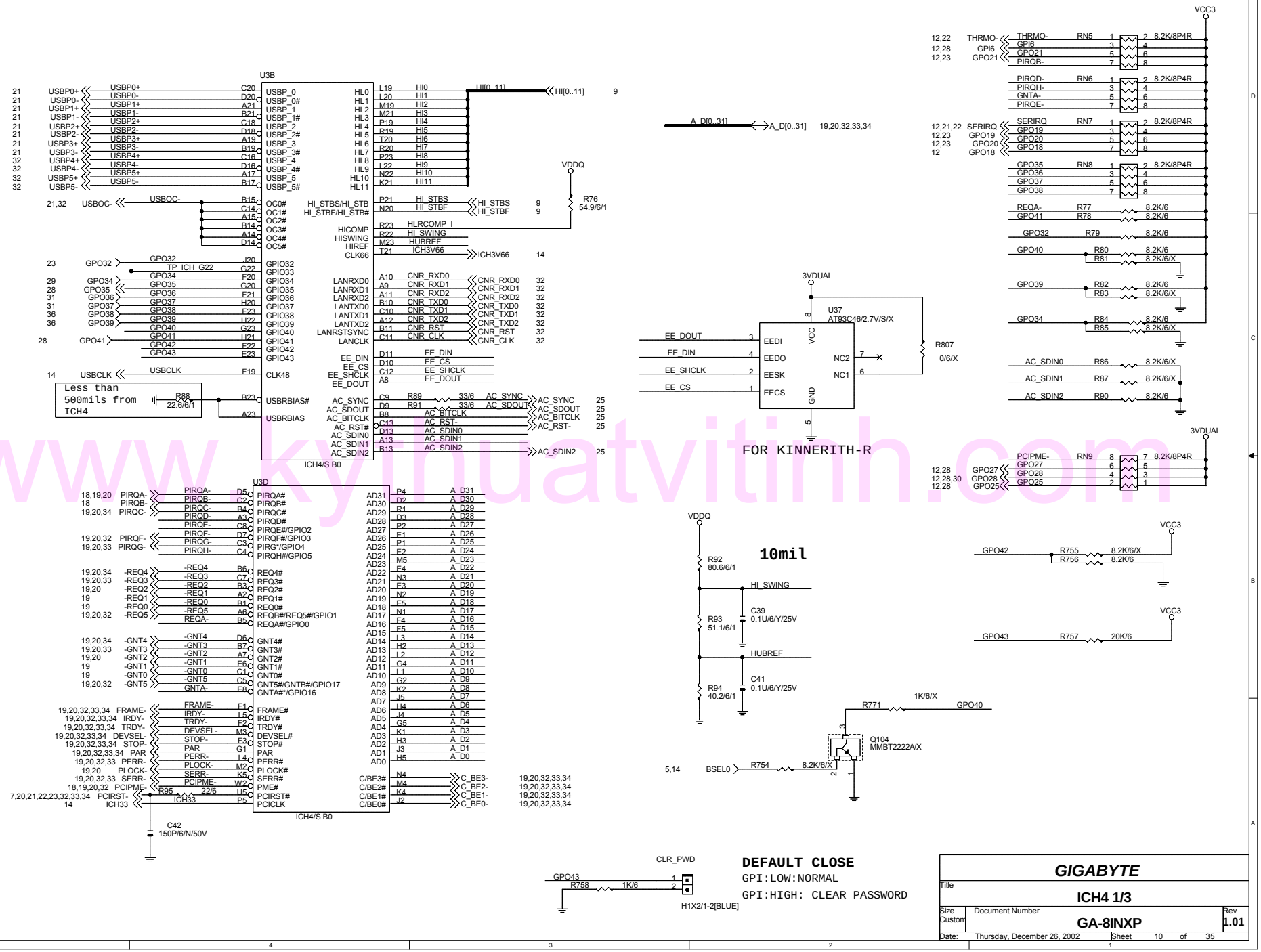
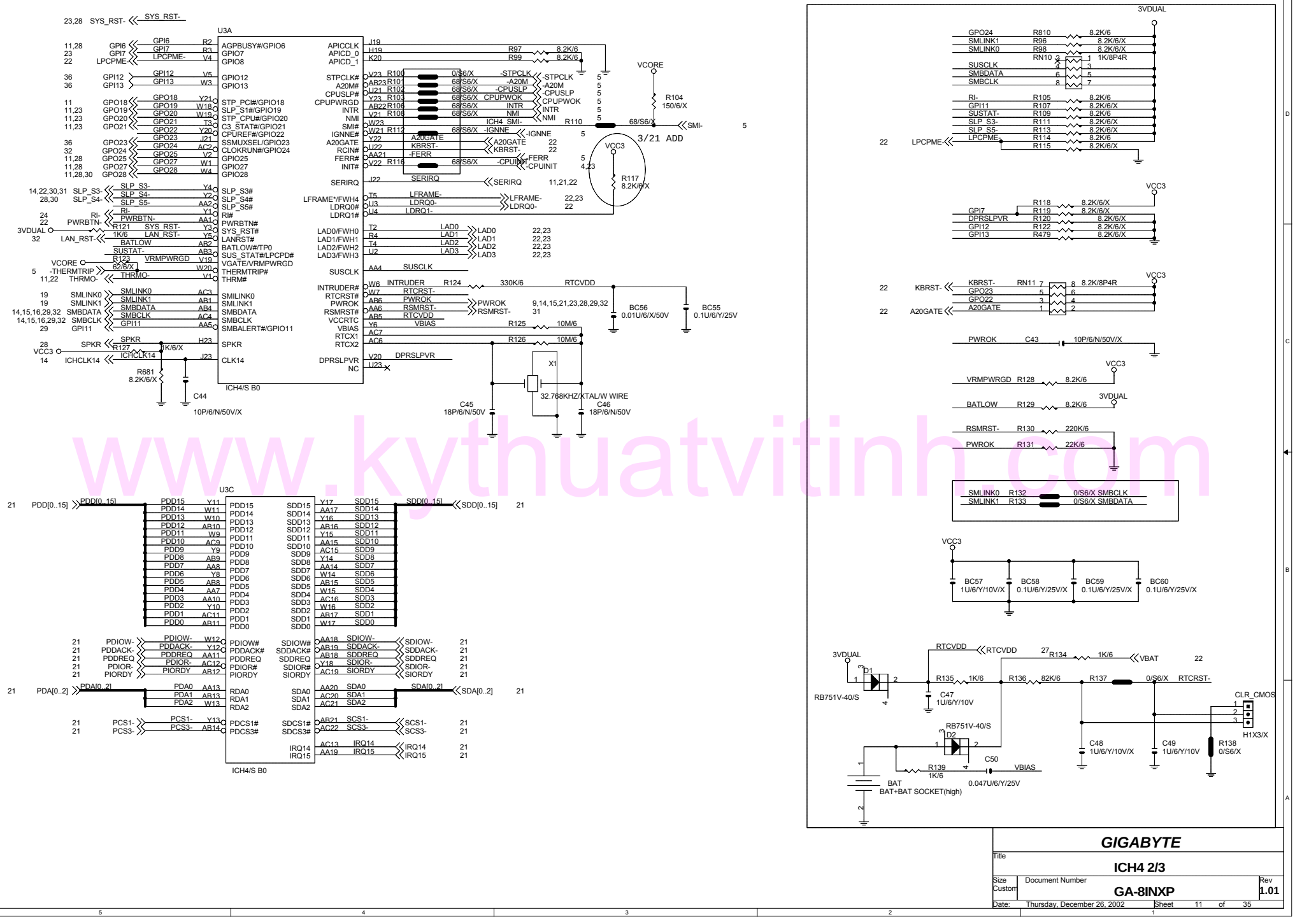
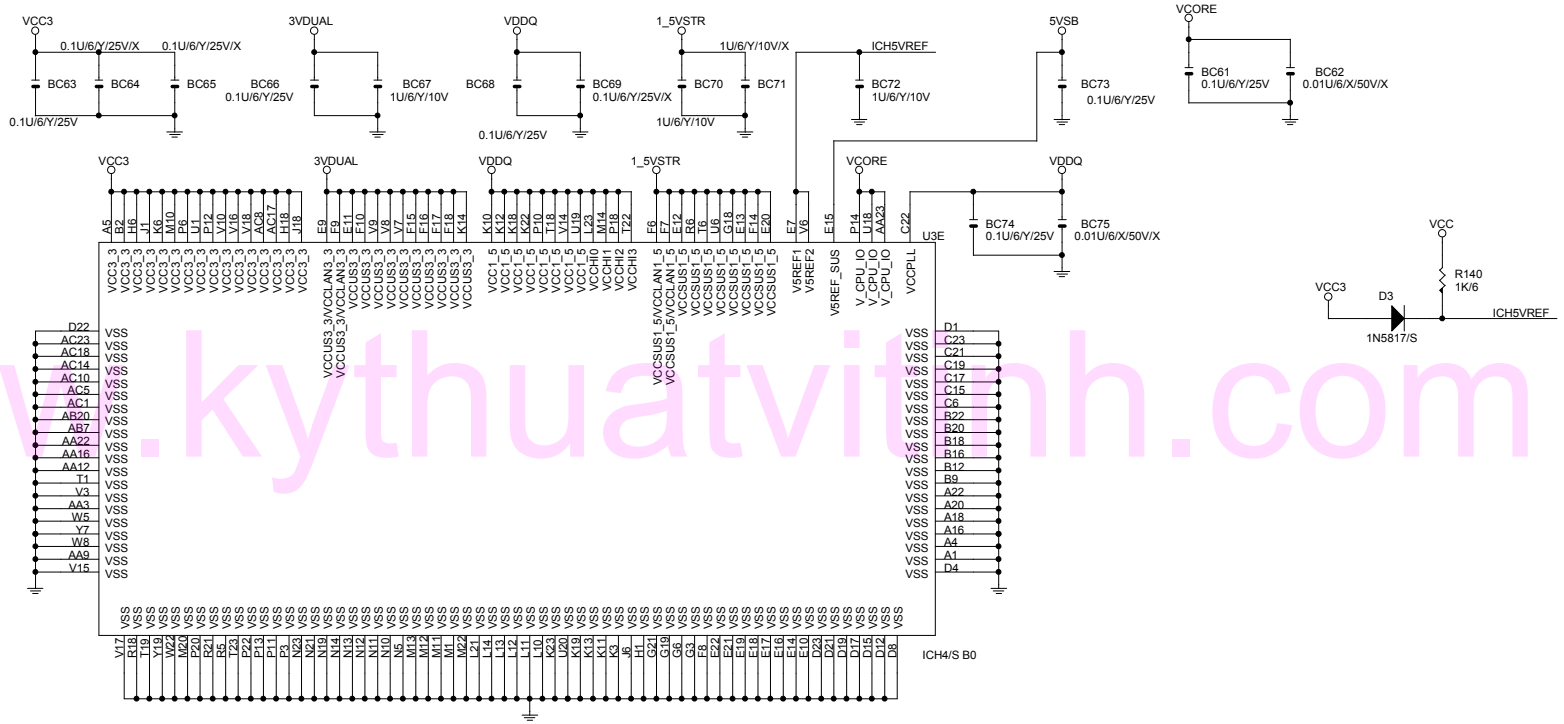
Title	GRANITE(PWR)	
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
Date: Thursday, December 26, 2002	Sheet 9 of 35	







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Title	ICH4 3/3	
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
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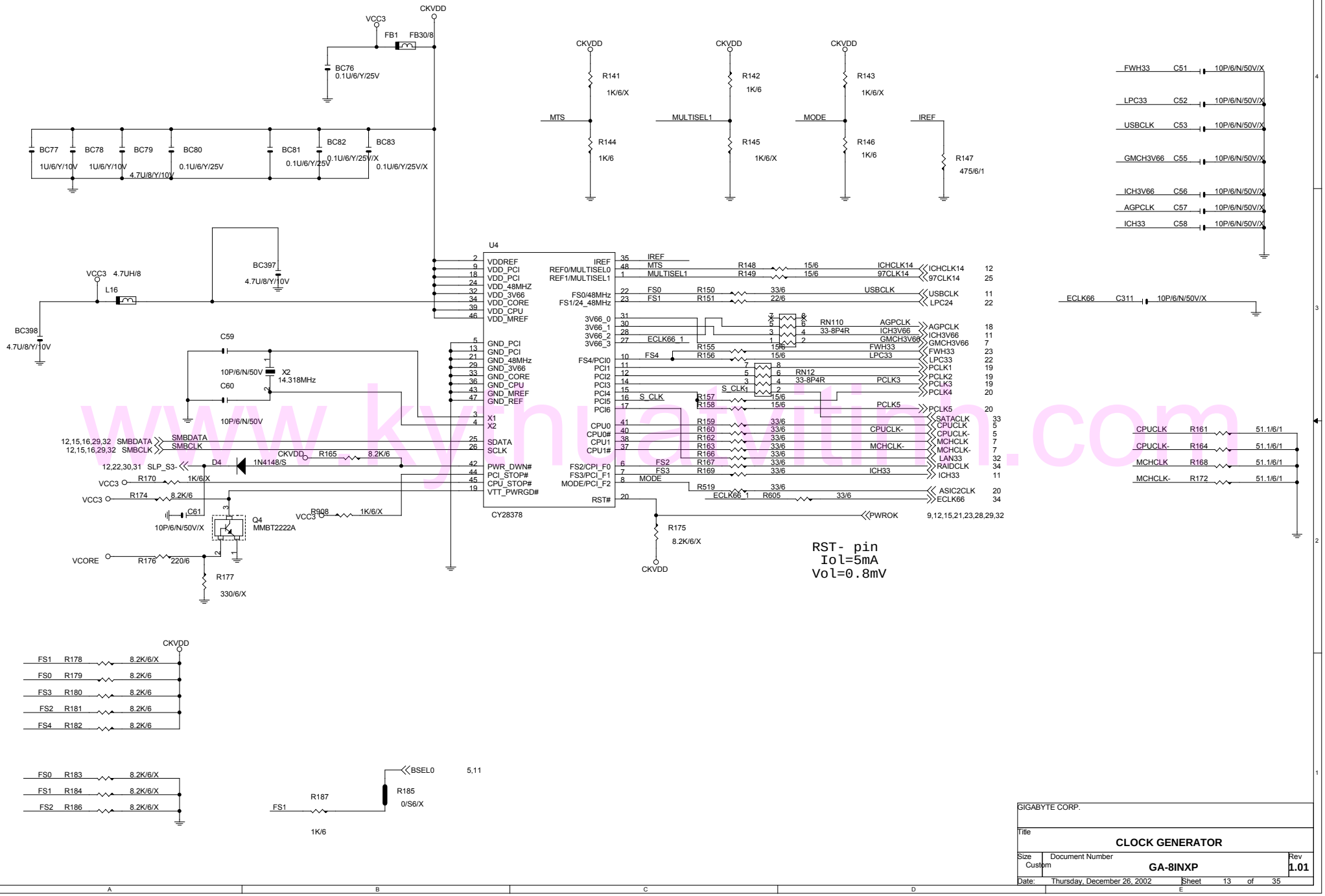
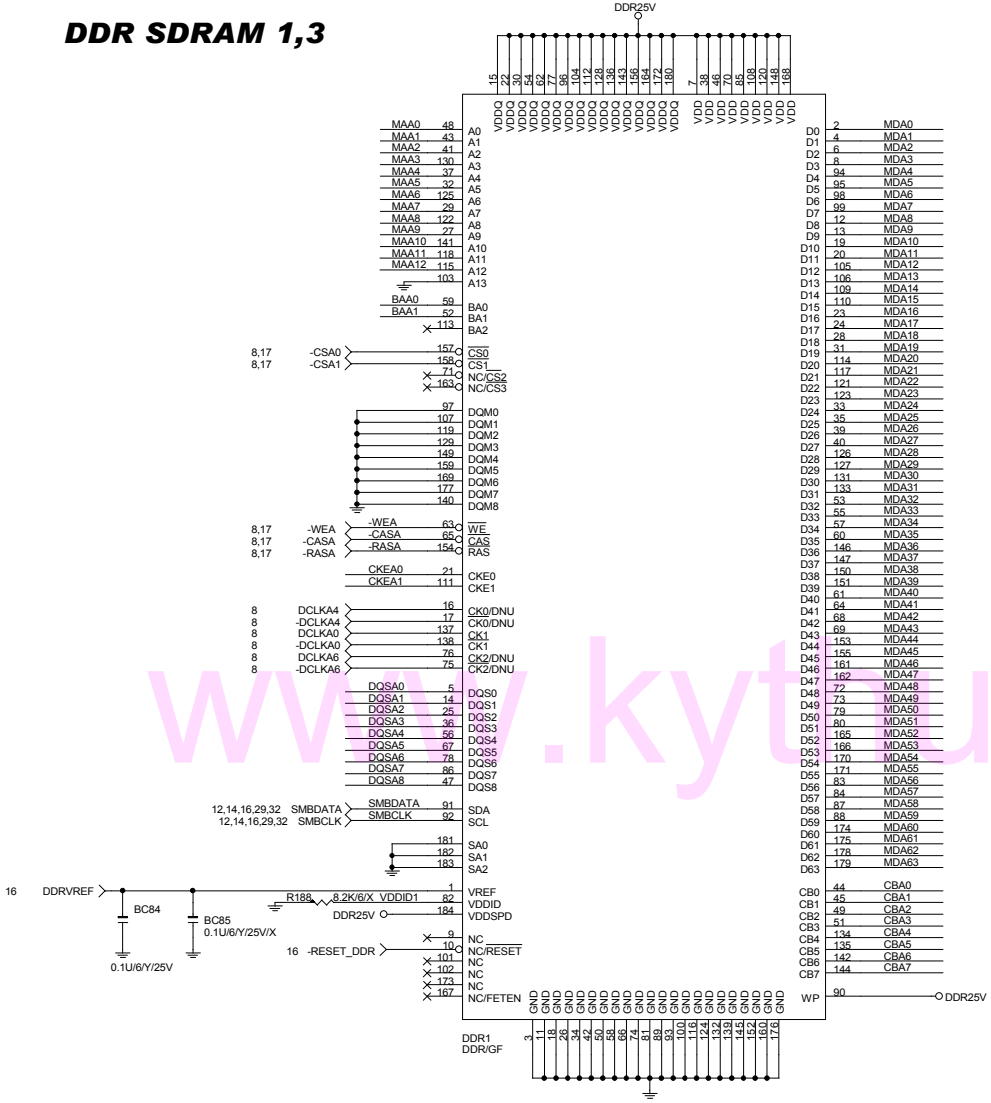
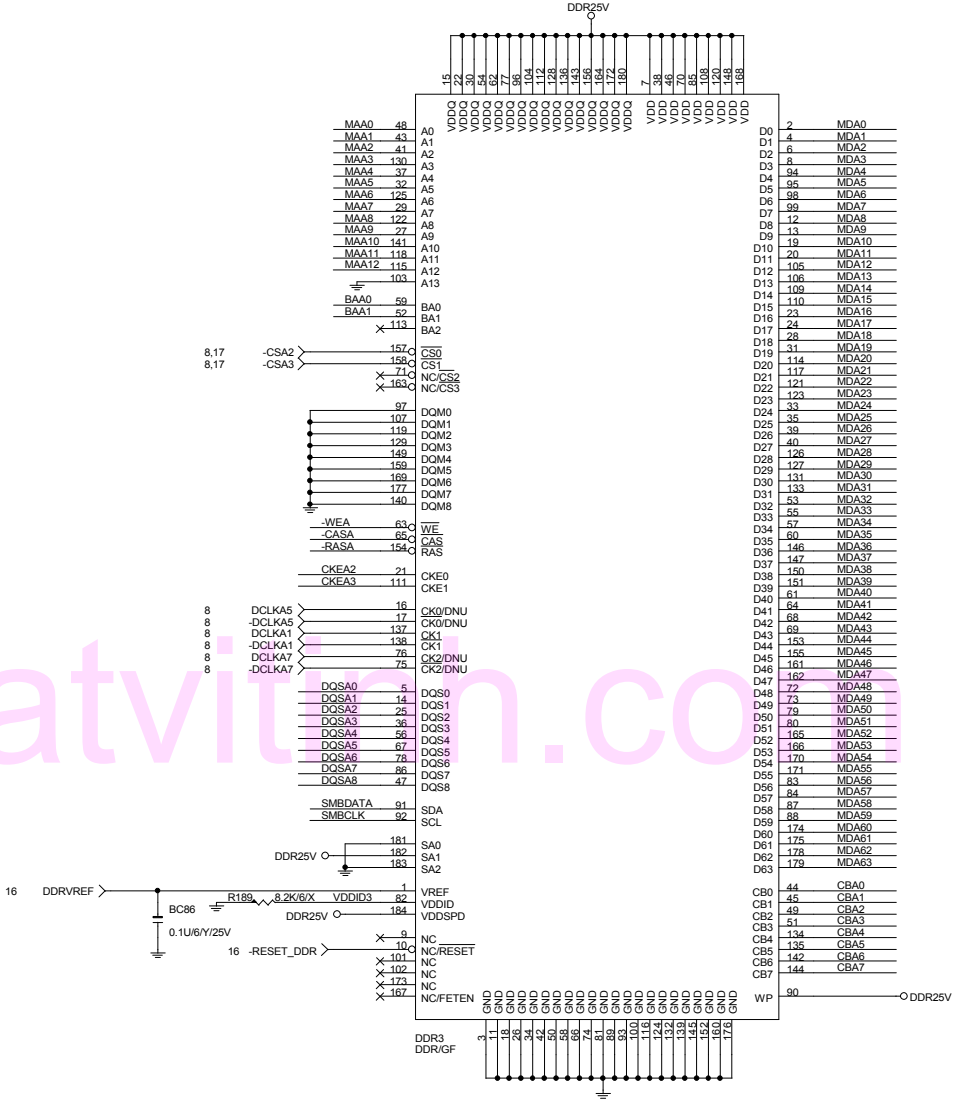


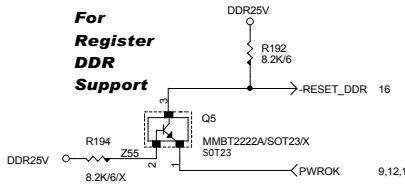
GIGABYTE CORP.		
Title: CLOCK GENERATOR		
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
Date: Thursday, December 26, 2002	Sheet 13 of 35	

DDR SDRAM 1,3





For Register DDR Support



GIGABYTE		
Title	DDR UNBUFFERED 1,3	
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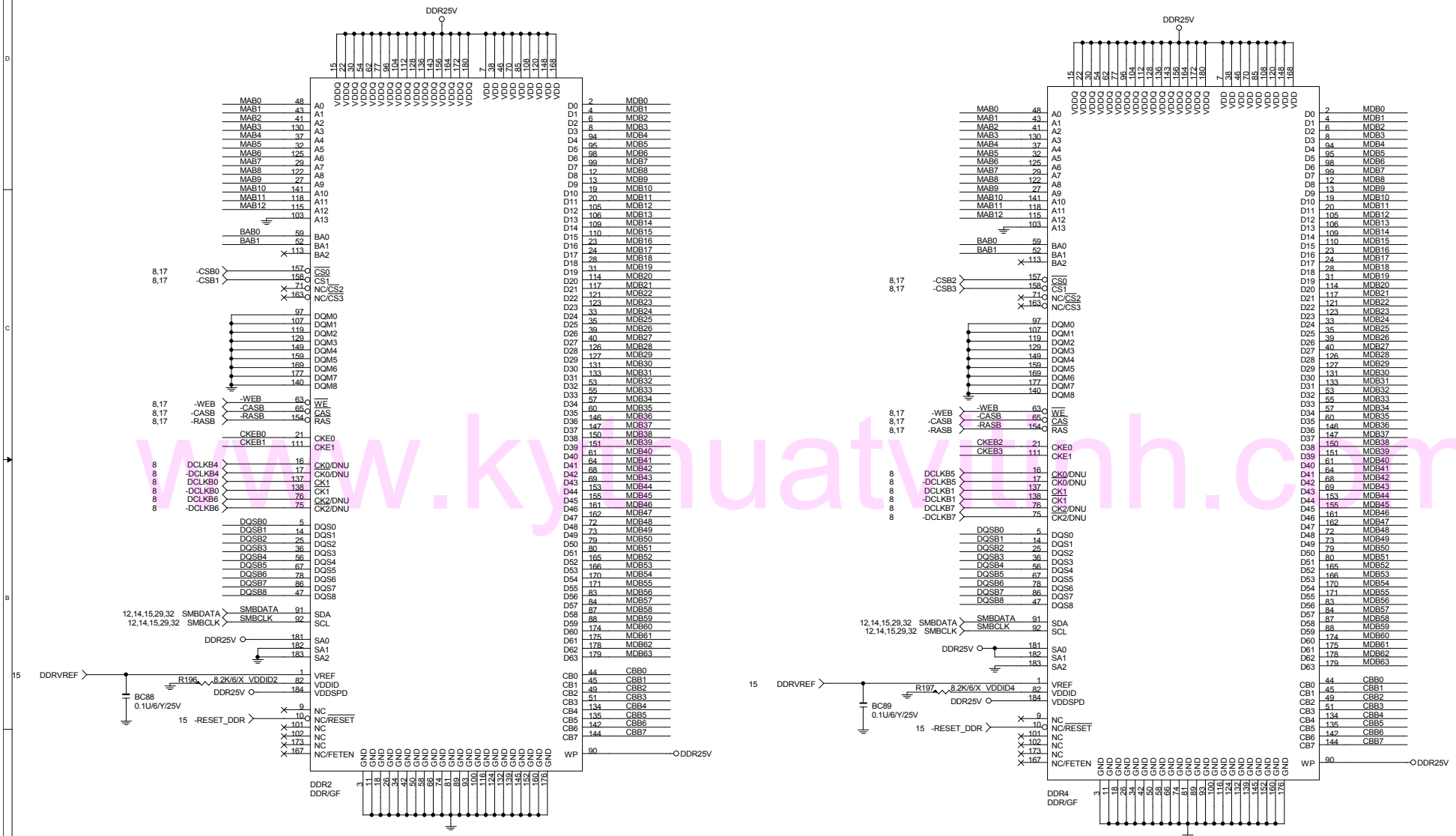
DDR SDRAM 2,4



GIGABYTE		
Title	DDR UNBUFFERED 2,4	
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
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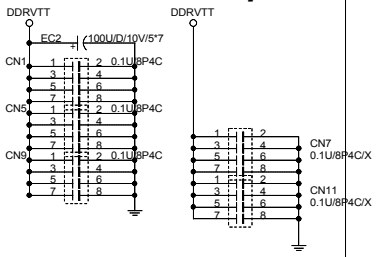
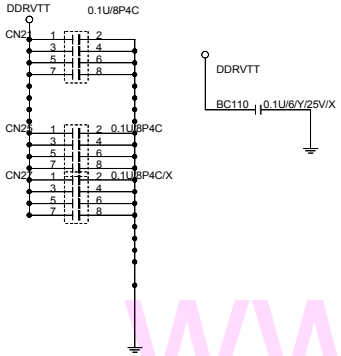
DDRVTT Decouple

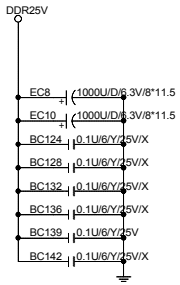


每兩個排容之間放一個0603電容
0.1U排容只上10個即可



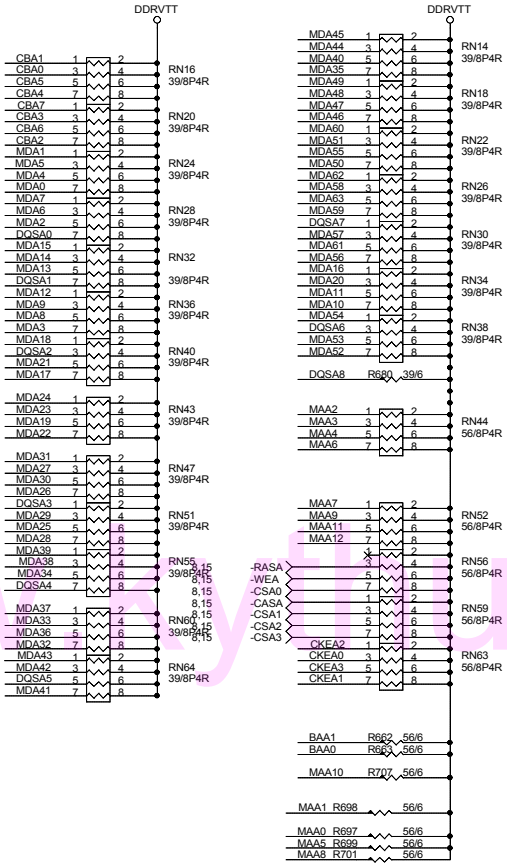
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling coapcitor for each two R-packs)

DDR25V Decouple



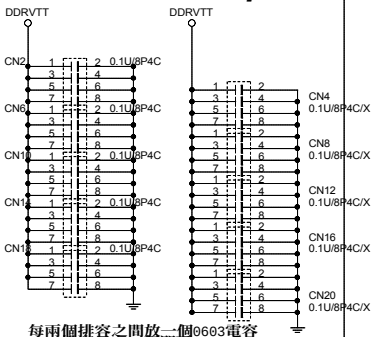
DDR TERMINATION

CHANNEL A

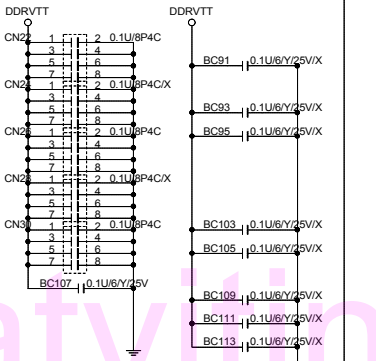


CBA[0..7] → CBA[0..7] 8,15
MAA[0..12] → MAA[0..12] 8,15
DQSA[0..8] → DQSA[0..8] 8,15
CKEA[0..3] → CKEA[0..3] 8,15
MDA[0:63] ↔ MDA[0:63] 8,15
BAA[0:1] ↔ BAA[0:1] 8,15

DDRVTT Decouple

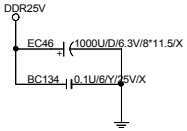


每兩個排容之間放一個0603電容
0.1U排容只上10個即可

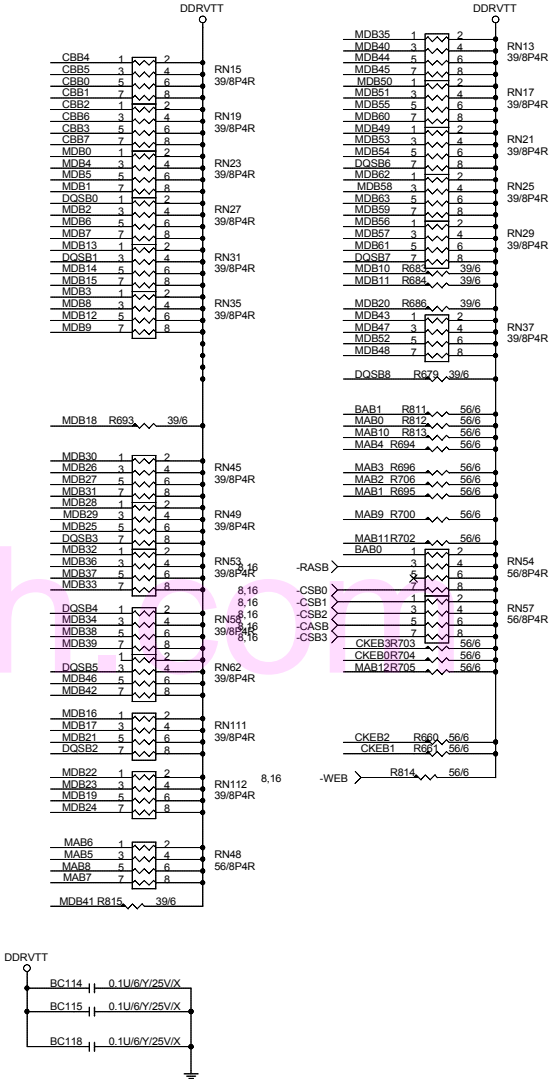


NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling coapcitor for each two R-packs)

DDR25V Decouple



CHANNEL B



DDRVTT

CBB[0..7] → CBB[0..7] 8,16
MAB[0..12] → MAB[0..12] 8,16
DQSB[0..8] → DQSB[0..8] 8,16
CKEB[0..3] → CKEB[0..3] 8,16
MDB[0:63] ↔ MDB[0:63] 8,16
BAB[0:1] ↔ BAB[0:1] 8,16

GIGABYTE			
Title: DDR TERM.			
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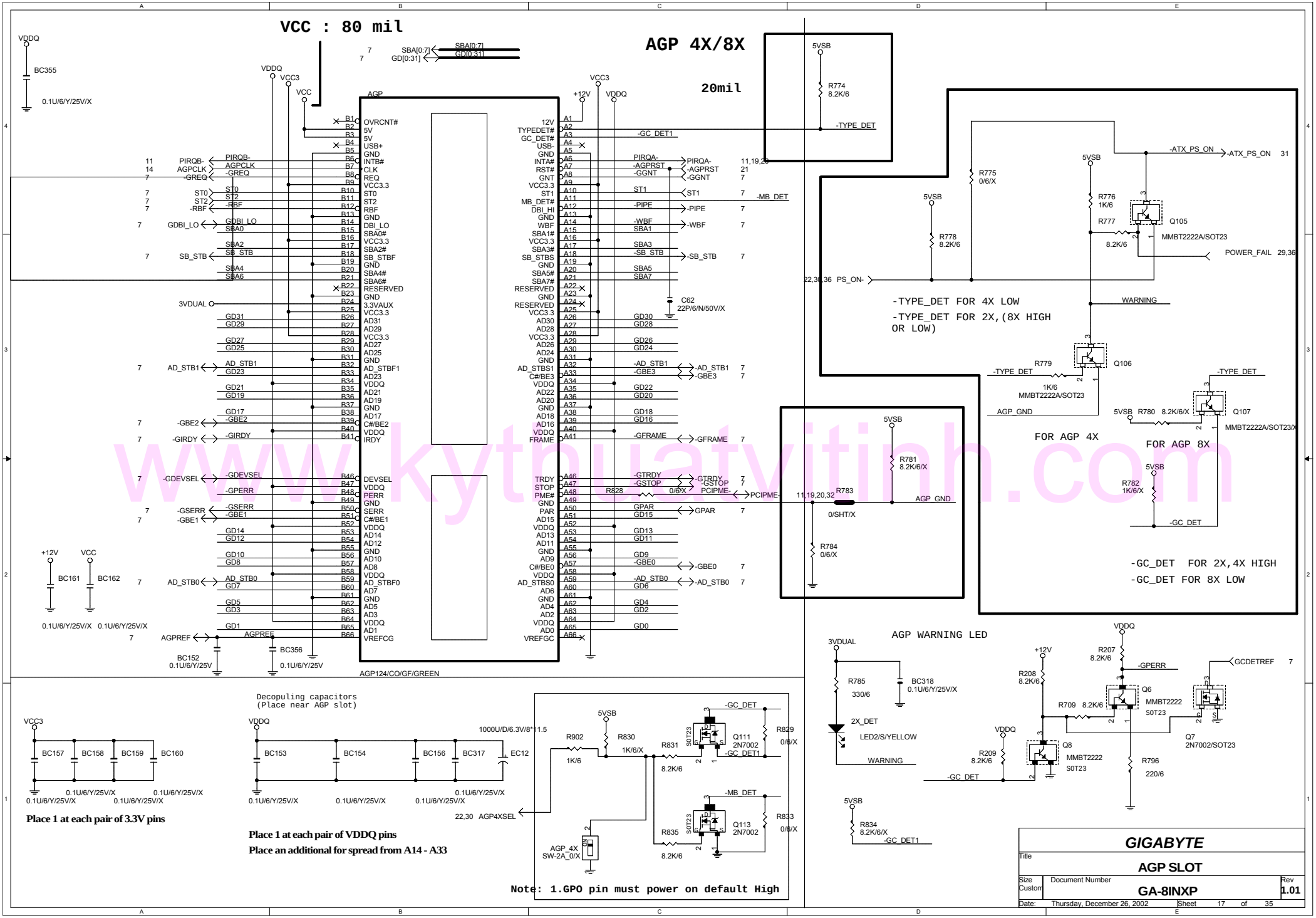

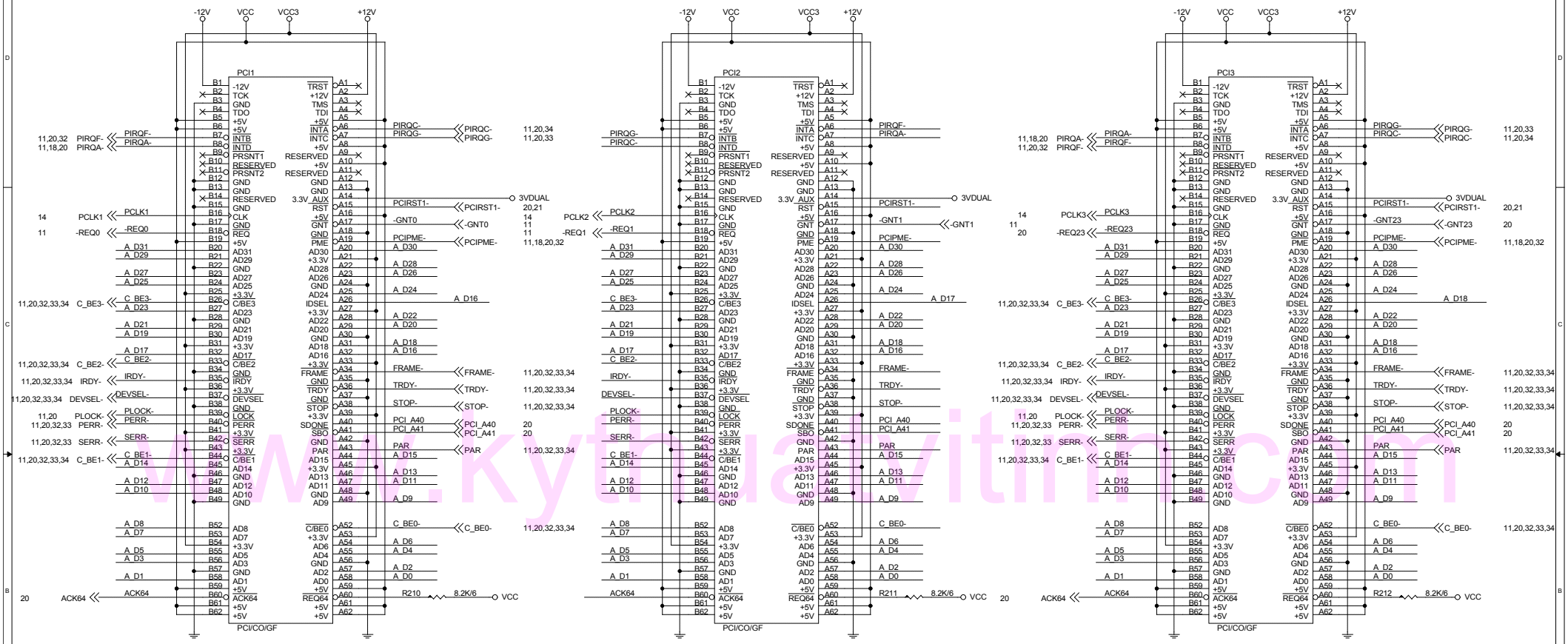

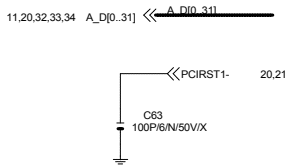

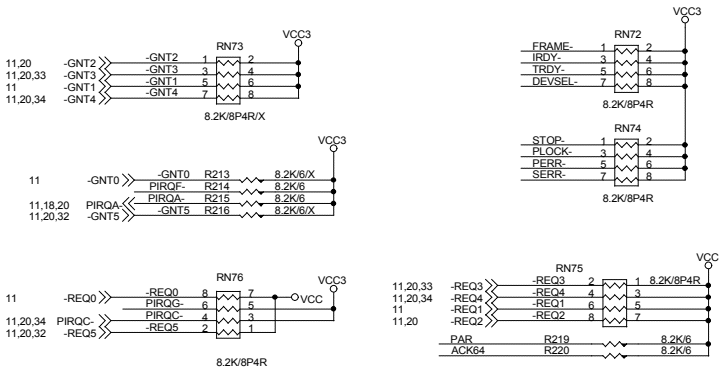

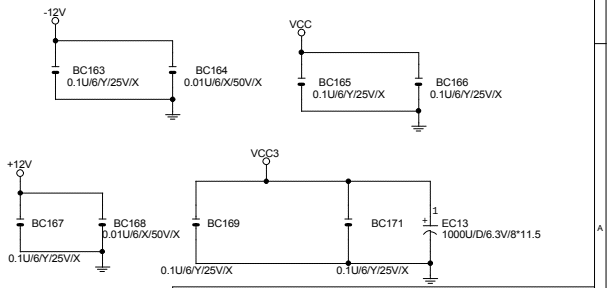

GIGABYTE

Title: **PCI SLOT 1/2**

Size	Document Number	Rev
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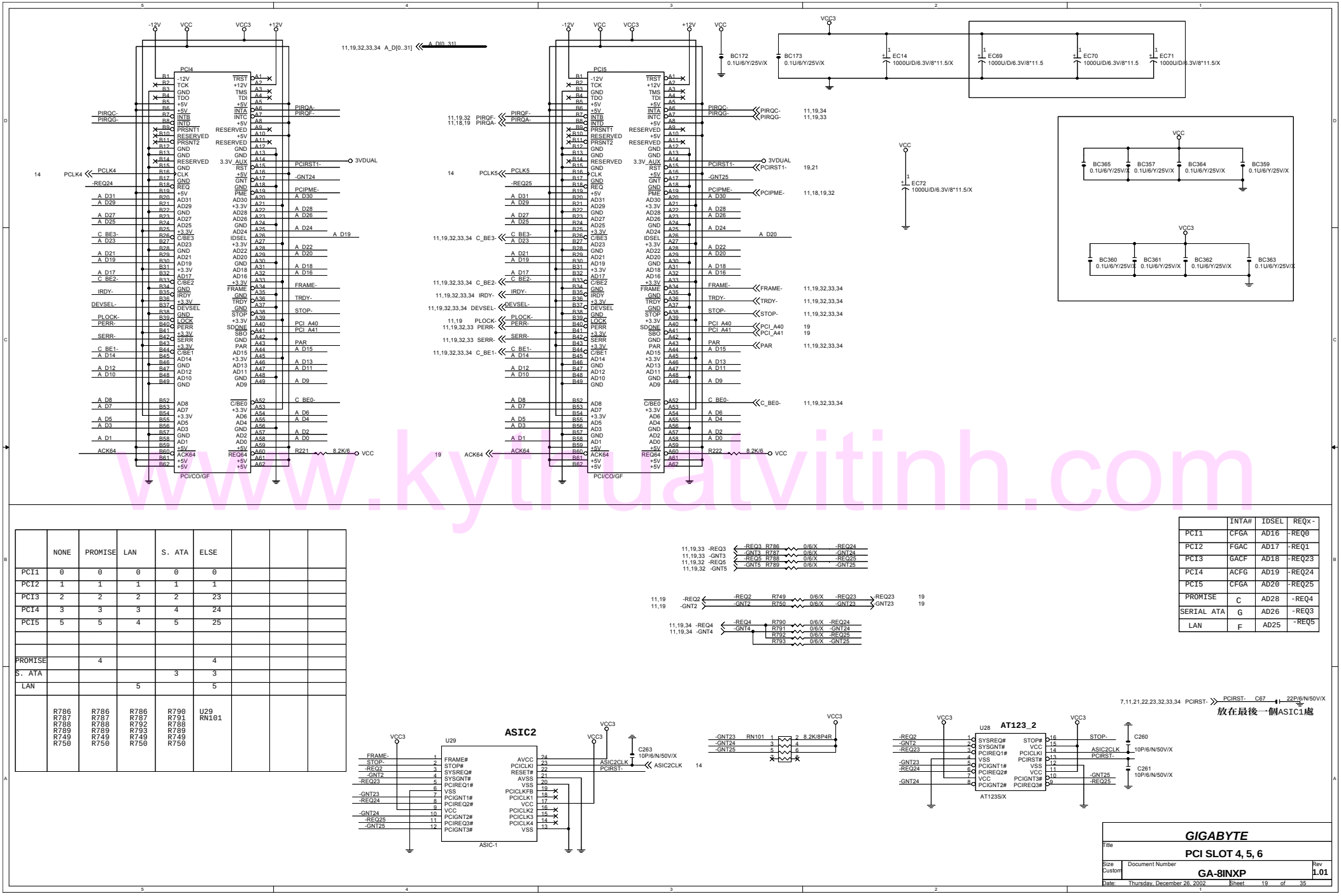

	NONE	PROMISE	LAN	S. ATA	ELSE			
PCI1	0	0	0	0	0			
PCI2	1	1	1	1	1			
PCI3	2	2	2	2	23			
PCI4	3	3	3	4	24			
PCI5	5	5	4	5	25			
PROMISE		4			4			
S. ATA				3	3			
LAN			5		5			
	R786 R787 R788 R789 R749 R750	R786 R787 R788 R789 R749 R750	R786 R787 R792 R793 R749 R750	R790 R791 R788 R789 R749 R750	U29 RN101			

	INTA#	IDSEL	REQx-
PCI1	CFGA	AD16	-REQ0
PCI2	FGAC	AD17	-REQ1
PCI3	GACF	AD18	-REQ23
PCI4	ACFG	AD19	-REQ24
PCI5	CFGA	AD20	-REQ25
PROMISE	C	AD28	-REQ4
SERIAL ATA	G	AD26	-REQ3
LAN	F	AD25	-REQ5

Title	PCI SLOT 4, 5, 6
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PRIMARY IDE

IDERST1- R228 33/6 RST1-

VCC3 R230 1K/6 PIORDY
R231 8.2K/6 IRQ14

R236 8.2K/6 PDD7
R238 5.6K/6/X PDDREQ
R240 470/6 IDEPU0

IDEACTS- D5 1N4148/S HDLED- HDLED- 28,33,35
IDEACTP- D6 1N4148/S
C68 180P/6/N/50V/X

SECONDARY IDE

IDERST2- R229 33/6 RST2-

VCC3 R232 1K/6 SIORDY
R233 8.2K/6 IRQ15

R237 8.2K/6 SDD7
R239 5.6K/6/X SDDREQ
R241 470/6 IDEPU1

VCC VCC3
R234 0/6/X
R235 0/6/SHT/X
BC175
0.1U/6/Y/25V/X

U7 74HC14
PCIRST- Z64 R242 0/6/X PCIRST1-
R243 0/6/X -AGPRST
VCC GND
DUAL_BIOS_DELAY DELAY1 PWOK
R244 330/6
9,12,14,15,23,28,29,32 PWROK

PWOK PWOK 30,31
-AGPRST -AGPRST 18
PCIRST1- PCIRST1- 19,20
PCIRST- PCIRST- 7,11,20,22,23,32,33,34
DUAL_BIOS_DELAY DUAL_BIOS_DELAY 23
DELAY1 DELAY1 23

PRIMARY IDE CONNECTOR

12 PDD[0..15] IDE1 IDE/RED

RST1-	1	2	
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
	19		
PDDREQ	21	22	
PDIOW-	23	24	
PDIOR-	25	26	
PIORDY	27	28	IDEPU0
PDDACK-	29	30	
IRQ14	31	32	
PDA1	33	34	P66DET
PDA0	35	36	PDA2
PCS1-	37	38	PCS3-
IDEACTP-	39	40	

12 PDDREQ 12 PDIOW- 12 PDIOR- 12 PIORDY 12 PDDACK- 12 IRQ14 12 PDA1 12 PDA0 12 PCS1-

To FWH GPI0

P66DET P66DET 23
12 12
C69 0.047U/6/Y/25V

SECONDARY IDE CONNECTOR

12 SDD[0..15] IDE2 IDE/WHITE

RST2-	1	2	
SDD7	3	4	SDD8
SDD6	5	6	SDD9
SDD5	7	8	SDD10
SDD4	9	10	SDD11
SDD3	11	12	SDD12
SDD2	13	14	SDD13
SDD1	15	16	SDD14
SDD0	17	18	SDD15
	19		
SDDREQ	21	22	
SDIOW-	23	24	
SDIOR-	25	26	
SIORDY	27	28	IDEPU1
SDDACK-	29	30	
IRQ15	31	32	
SDA1	33	34	S66DET
SDA0	35	36	SDA2
SCS1-	37	38	SCS3-
IDEACTS-	39	40	

12 SDDREQ 12 SDIOW- 12 SDIOR- 12 SIORDY 12 SDDACK- 12 IRQ15 12 SDA1 12 SDA0 12 SCS1-

To FWH GPI1

S66DET S66DET 23
12 12
C70 0.047U/6/Y/25V

SIRQ

S_IRQ
11,12,22 SERIRQ SERIRQ
SIRQ1x2/Orange/X

FRONT SIDE USB1

FUSEVCC
UBC1 0.1U/6/Y/25V
UL1 OD6560T/S/X
F_USB1 BoxHead2x5/-9/yellow
URN1 0/8P4R

11 USBP2+ USBP2+ 11 USBP2-
11 USBP3+ USBP3+ 11 USBP3-
P2- P2+ P3+ P3-
R247 0/6/X USBOC- 11,32

IDE RESET

VCC 5VSB
R245 1K/6
R816 1K/6/X
Z64 R246 8.2K/6 Q9 MMBT2222A/SOT23 IDERST1-
5VSB R817 0/6
R818 1K/6/X
R819 8.2K/6/X Q110 MMBT2222A/SOT23/X IDERST2-

SUPPORT POWER OFF PLAY CD

FRONT SIDE USB2

FUSEVCC
UBC2 0.1U/6/Y/25V
UEC1 1000U/D/6.3V/8*11.5
UL2 OD6560T/S/X
F_USB2 BoxHead2x5/-9/yellow
URN2 0/8P4R

11 USBP0+ USBP0+ 11 USBP0-
11 USBP1+ USBP1+ 11 USBP1-
P0- P0+ P1+ P1-
R248 0/6/X USBOC- 11,32

VCC C280 VCC3
0.1U/6/Y/25V
摆在跨切割層旁

FUSEVCC,GAMEVCC

5VDUAL 220mil FB2 FB100/DIP
60mil KF1 POLY SW PSR24251 RAY/DIP 2.5A/16V
FUSEVCC 60mil GQ1 2N7002/SOT23
+12V 20mil GAMEVCC GR1 1K/6

GIGABYTE			
Title	IDE, USB		
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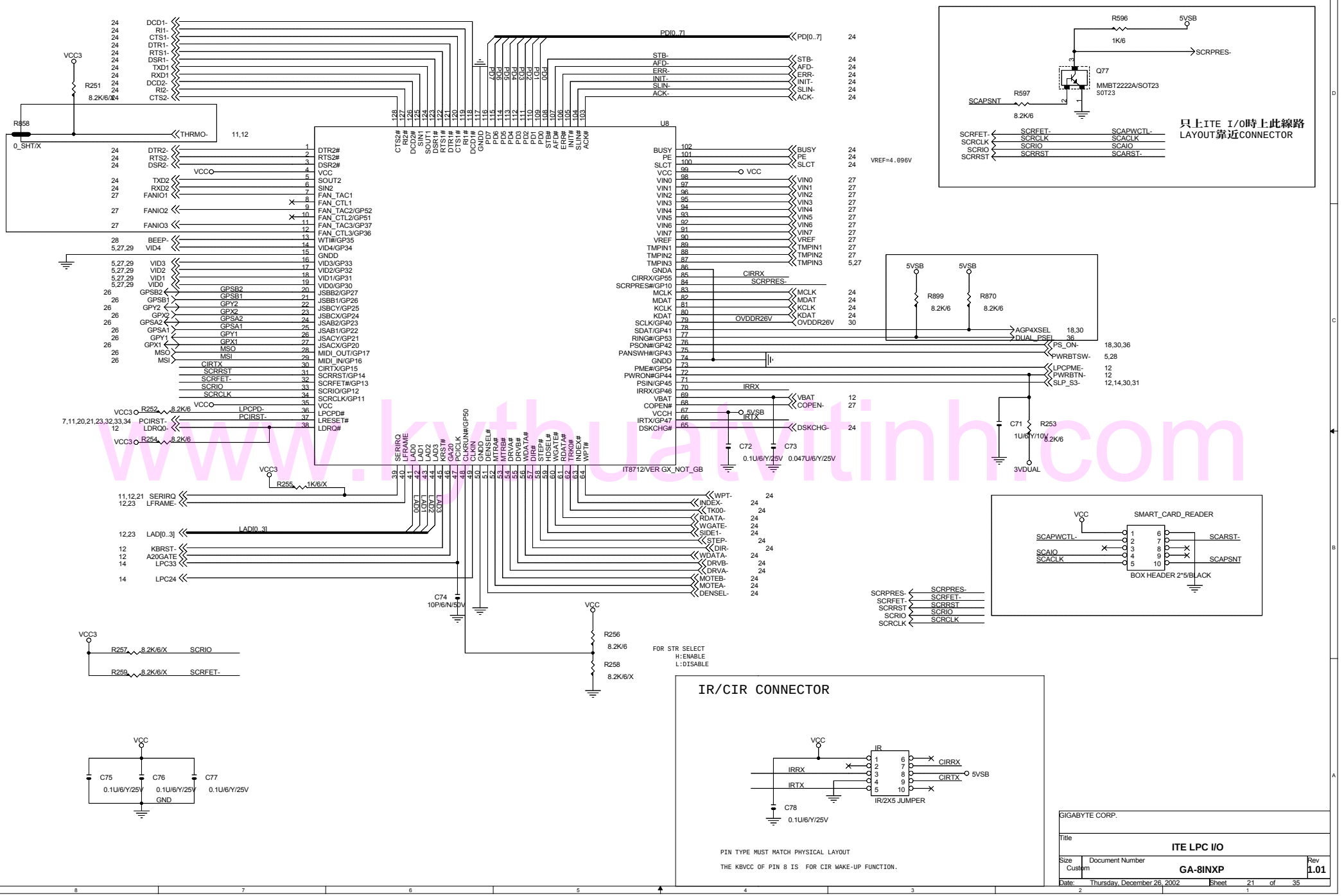

GIGABYTE CORP.			
Title: ITE LPC I/O			
Size: Custom	Document Number: GA-8INXP		Rev: 1.01
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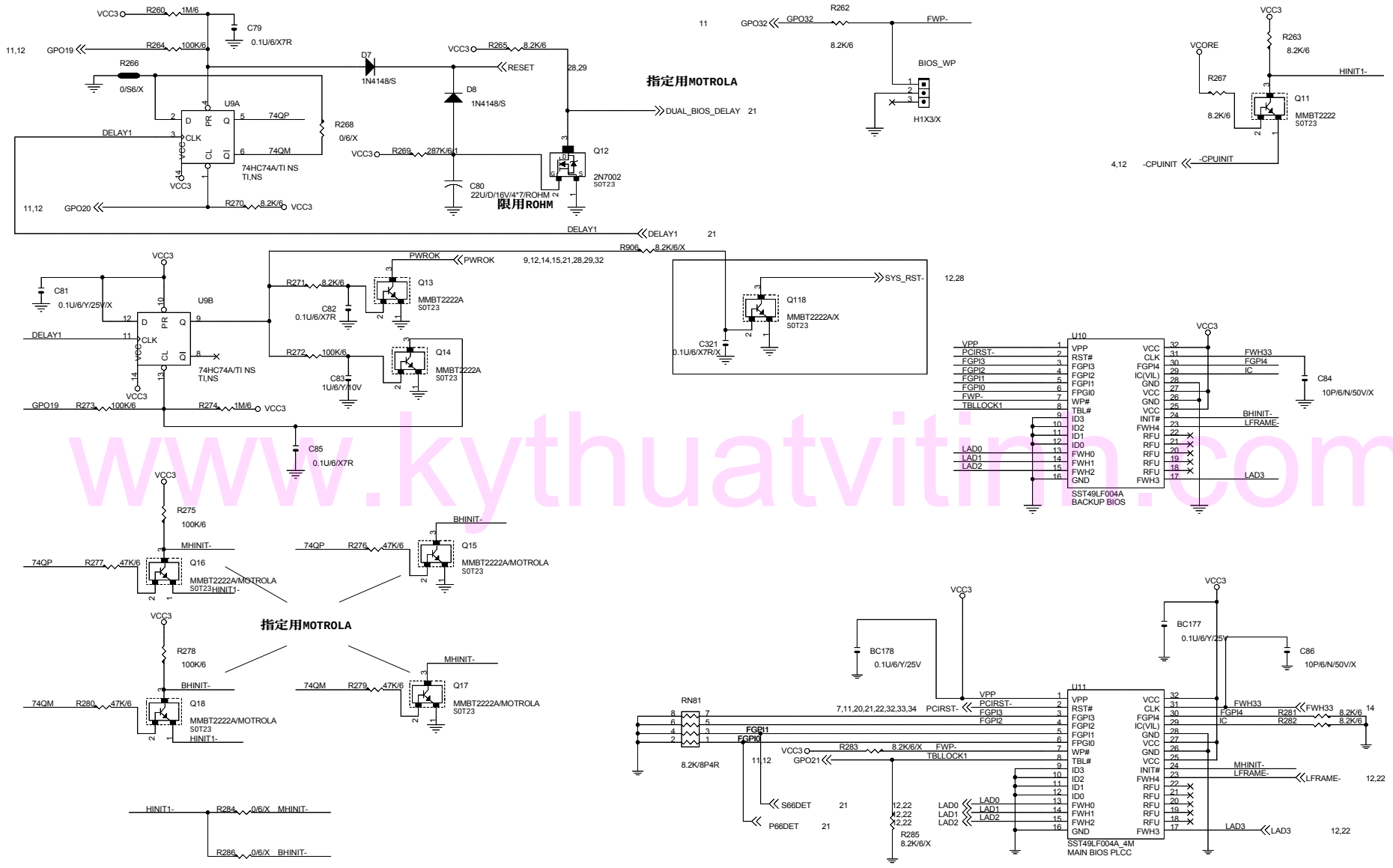

ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title: FWH		
Size: Custom	Document Number: GA-8INXP	Rev: 1.01
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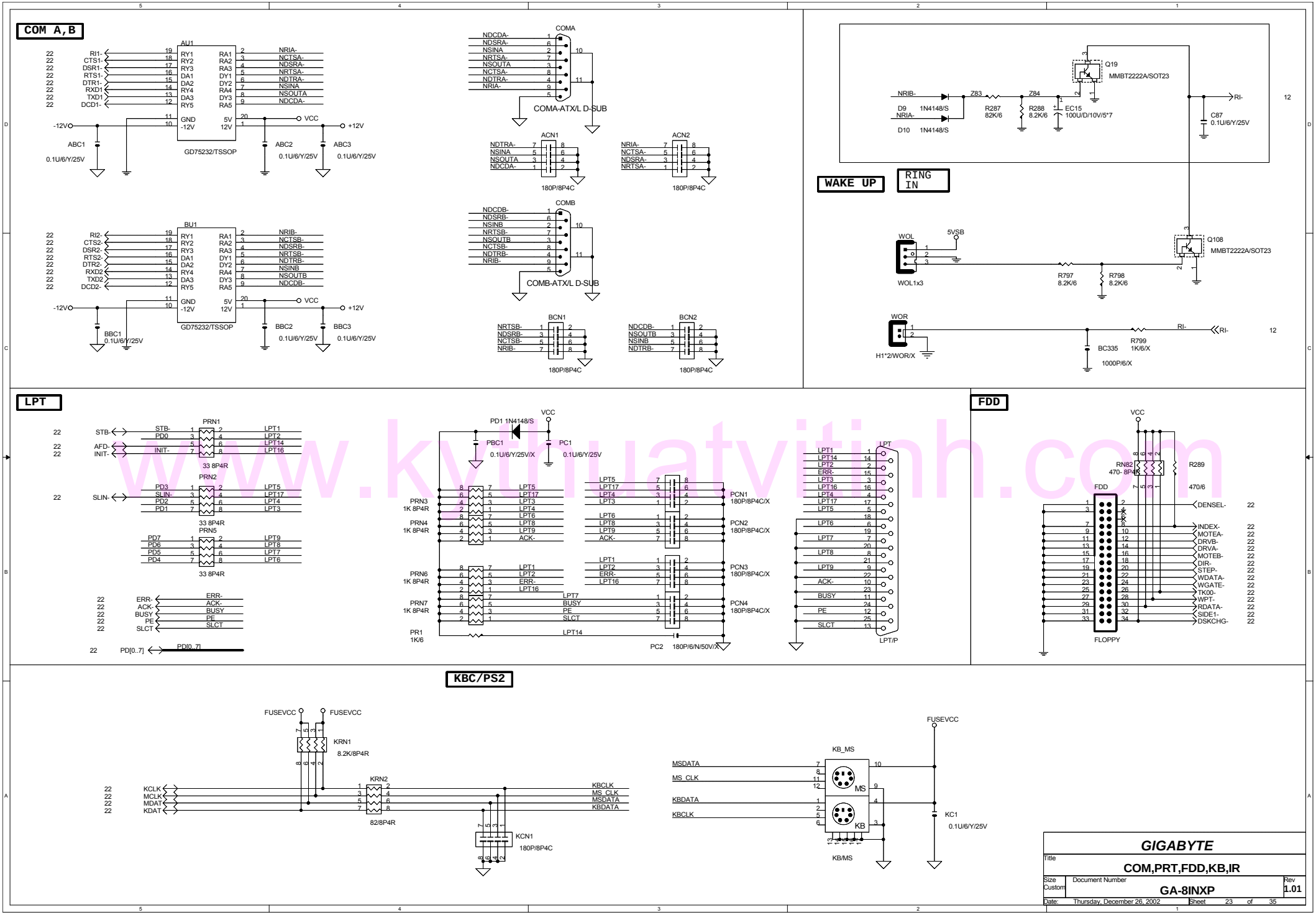
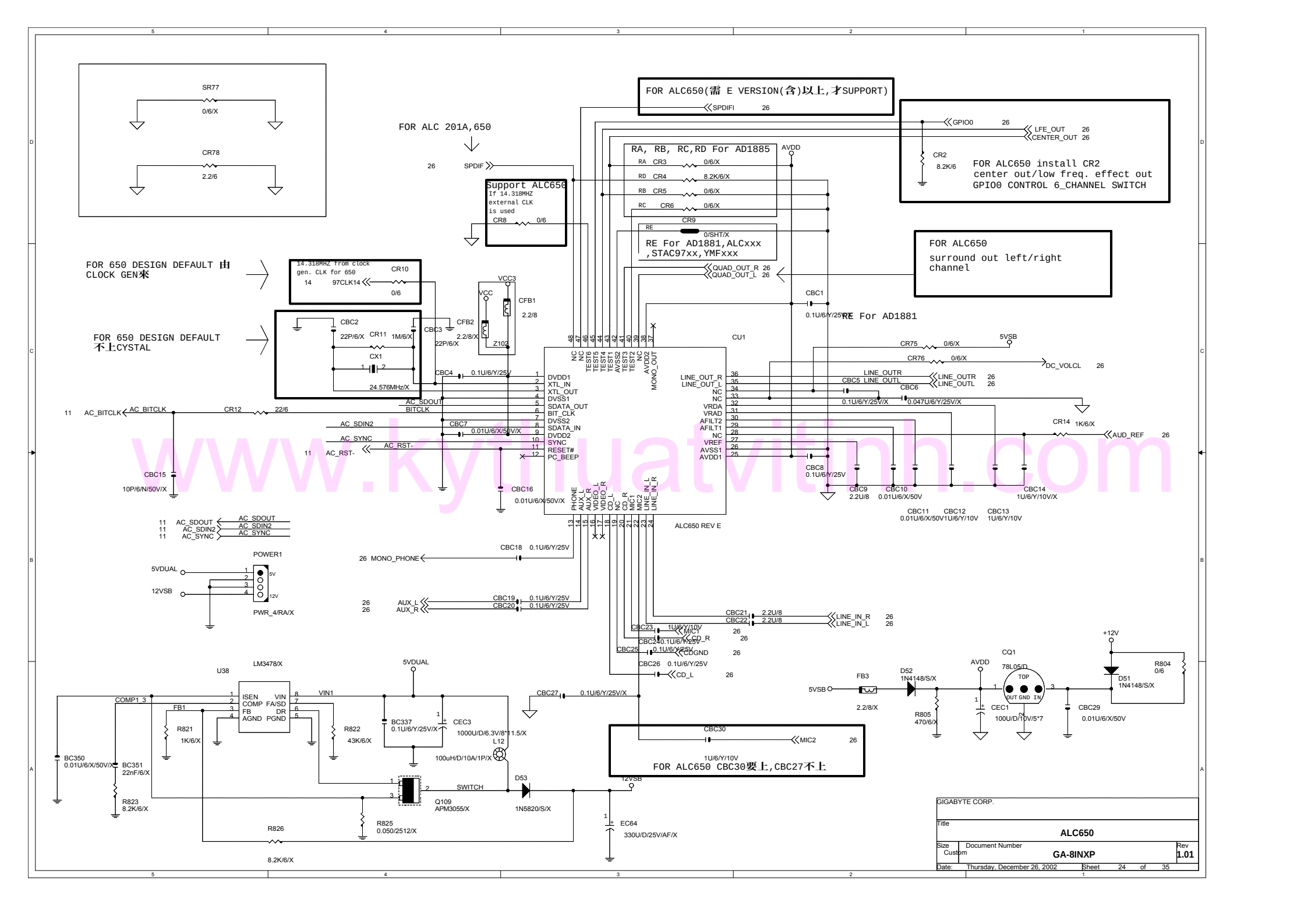
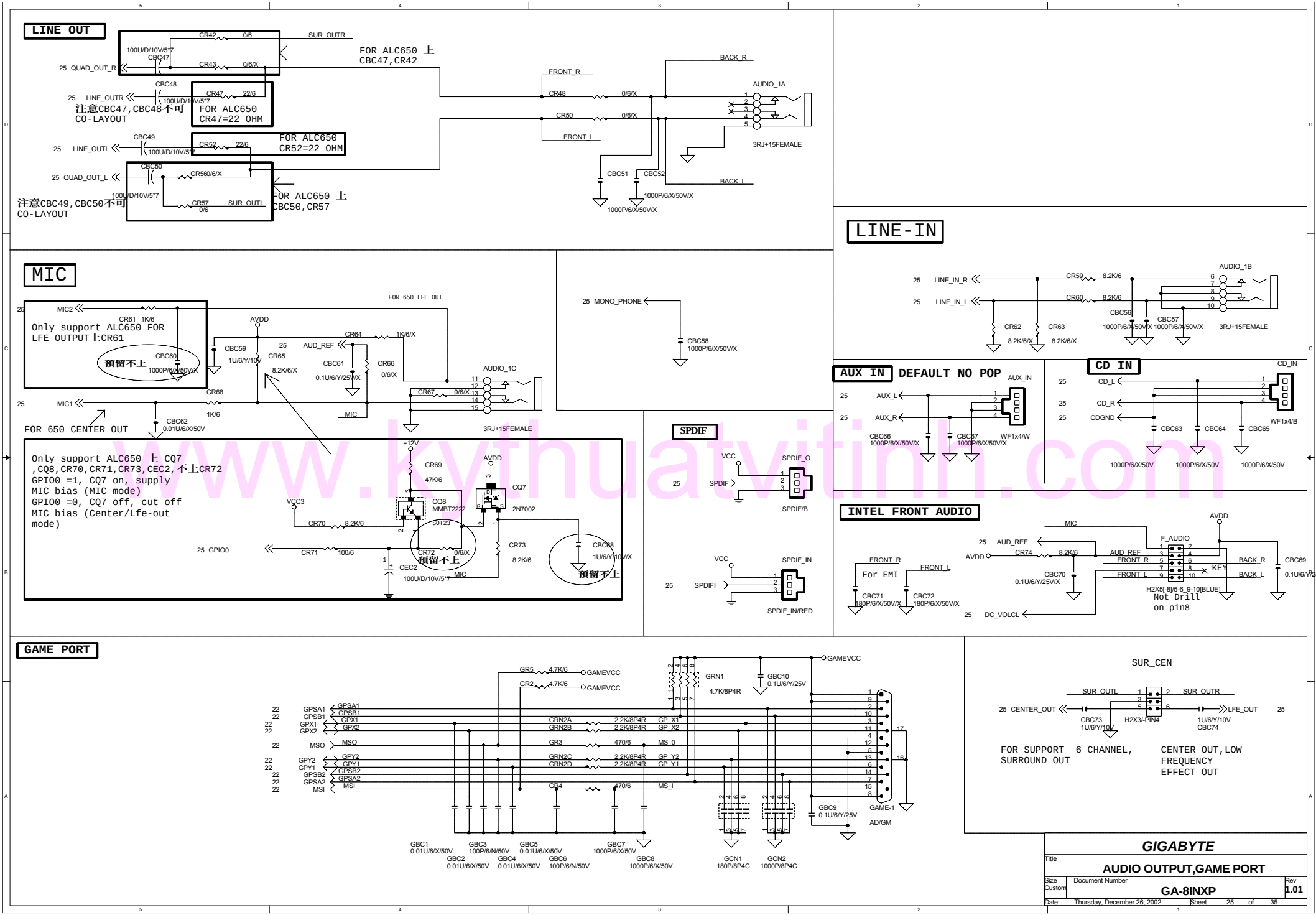
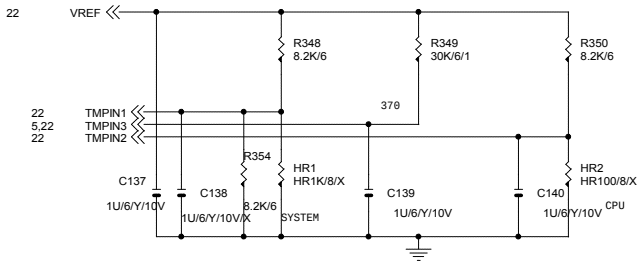
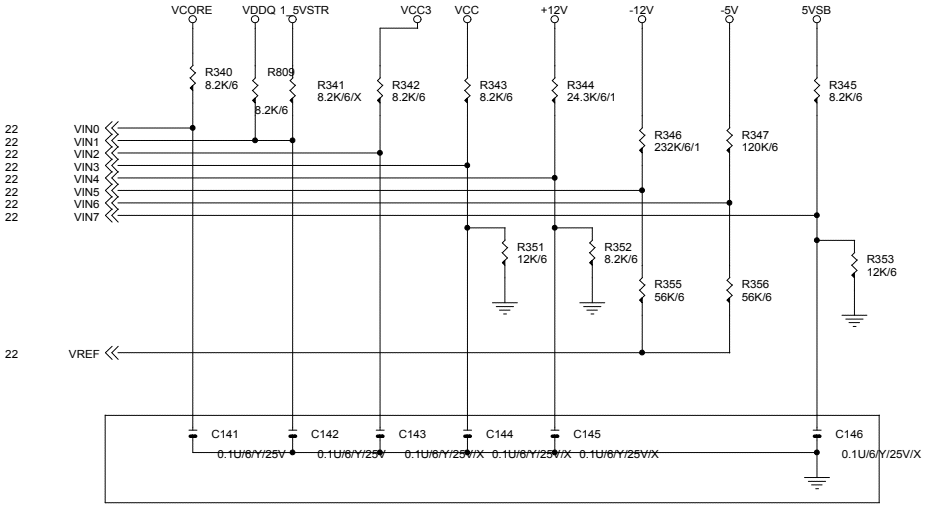




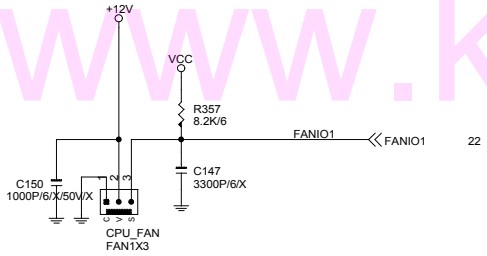


Hardware Monitor circuits

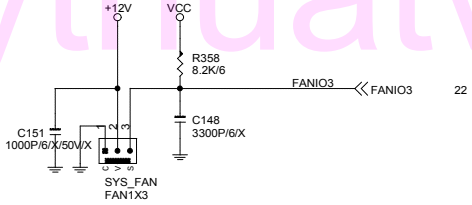




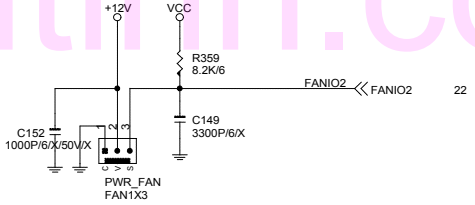
CPU FAN
+12V -->40 mils



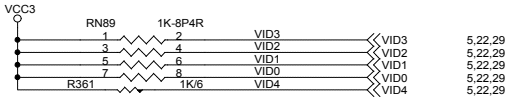
SYSTEM FAN
+12V -->40 mils



POWER FAN
+12V -->40 mils



CPU Voltage ID output



GIGABYE CORP.	
Title	HAREWARE MONITOR
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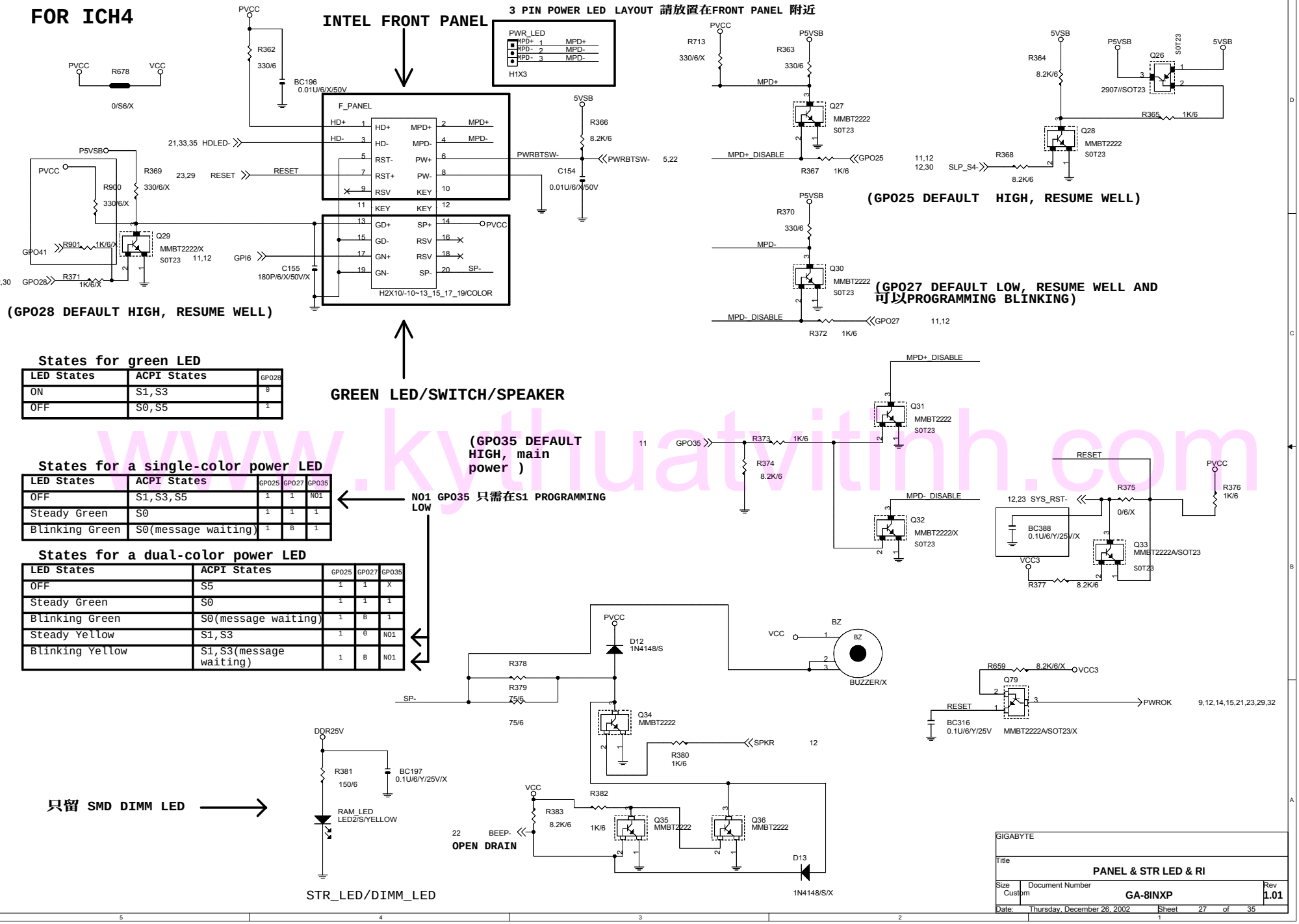
FOR ICH4



States for green LED

LED States	ACPI States	GPO28
ON	S1,S3	0
OFF	S0,S5	1

States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1

States for a dual-color power LED

LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

GIGABYTE	
Title	PANEL & STR LED & RI
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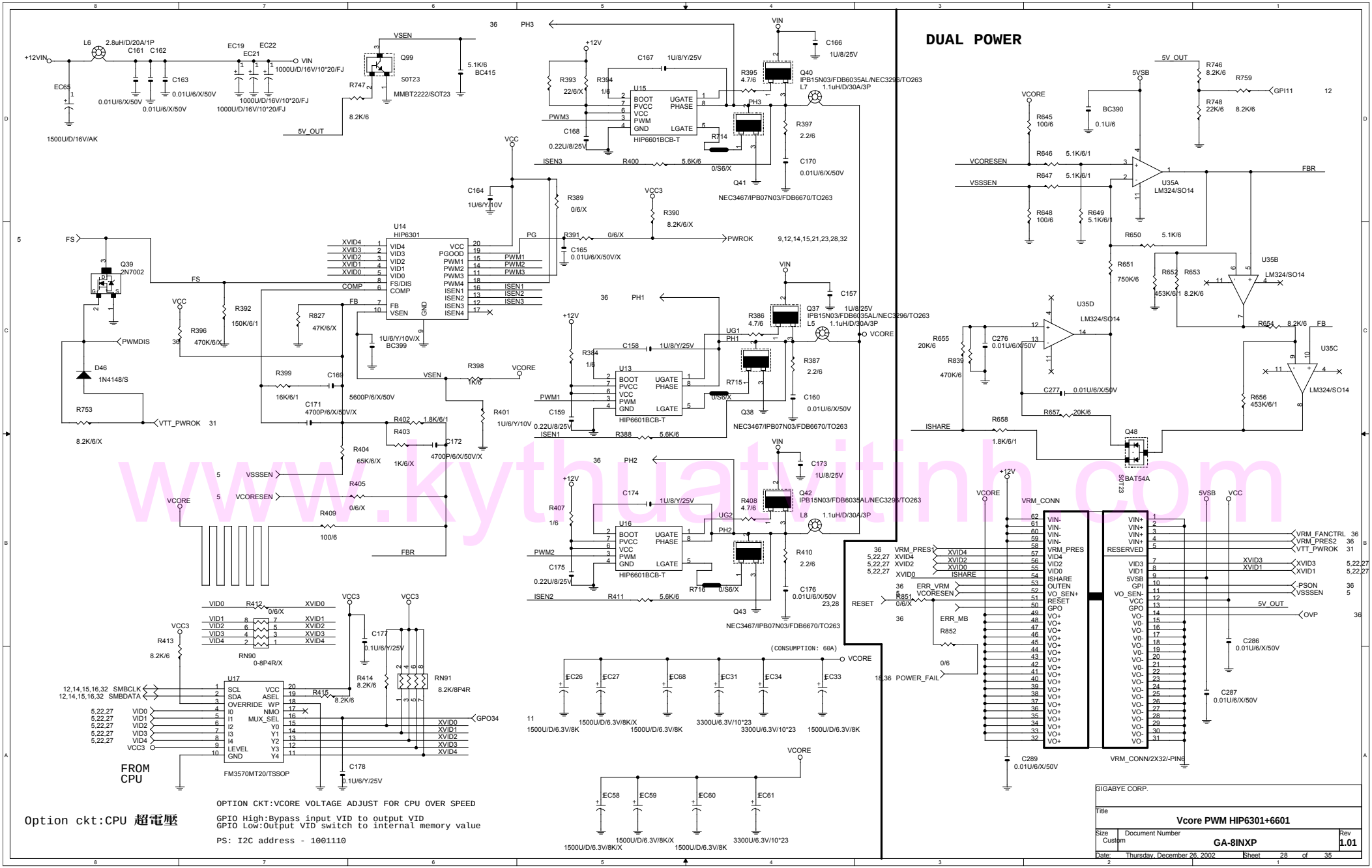
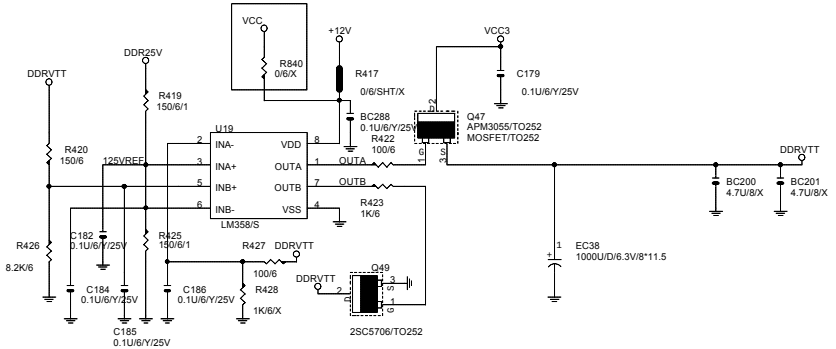
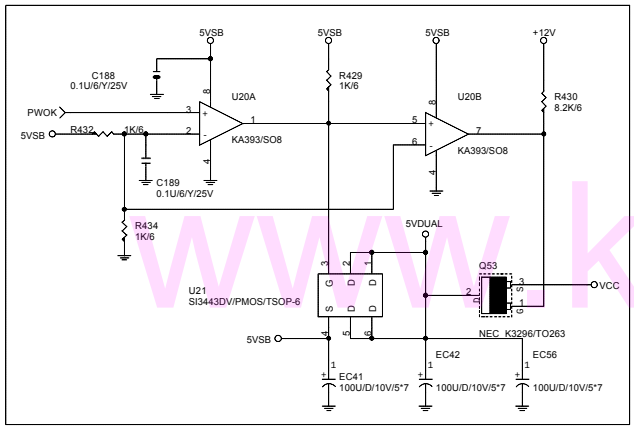
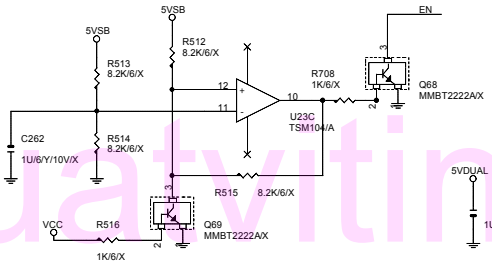
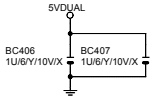


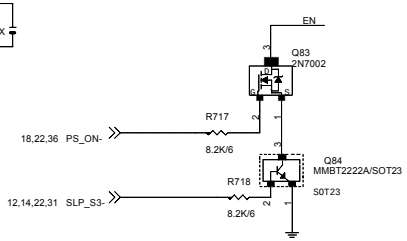
1.25V DDRVTT LINEAR SOLUTION



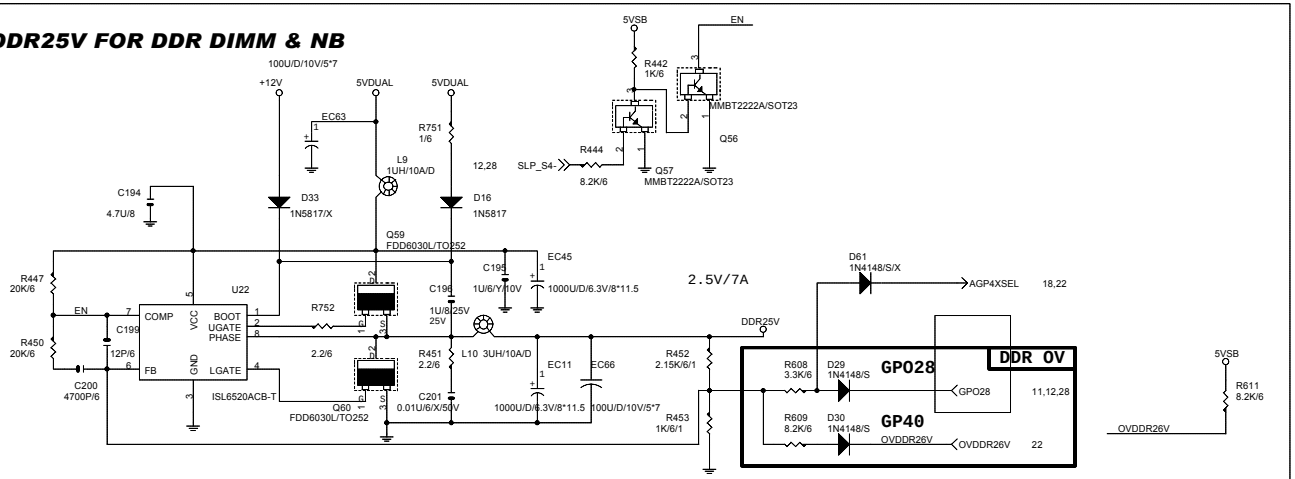








DDR25V FOR DDR DIMM & NB



GP40:GP028		
2.5V :	H	H
2.6V :	L	H
2.7V :	H	L
2.78V:	L	L

GIGABYTE		
Title	DDR POWER	
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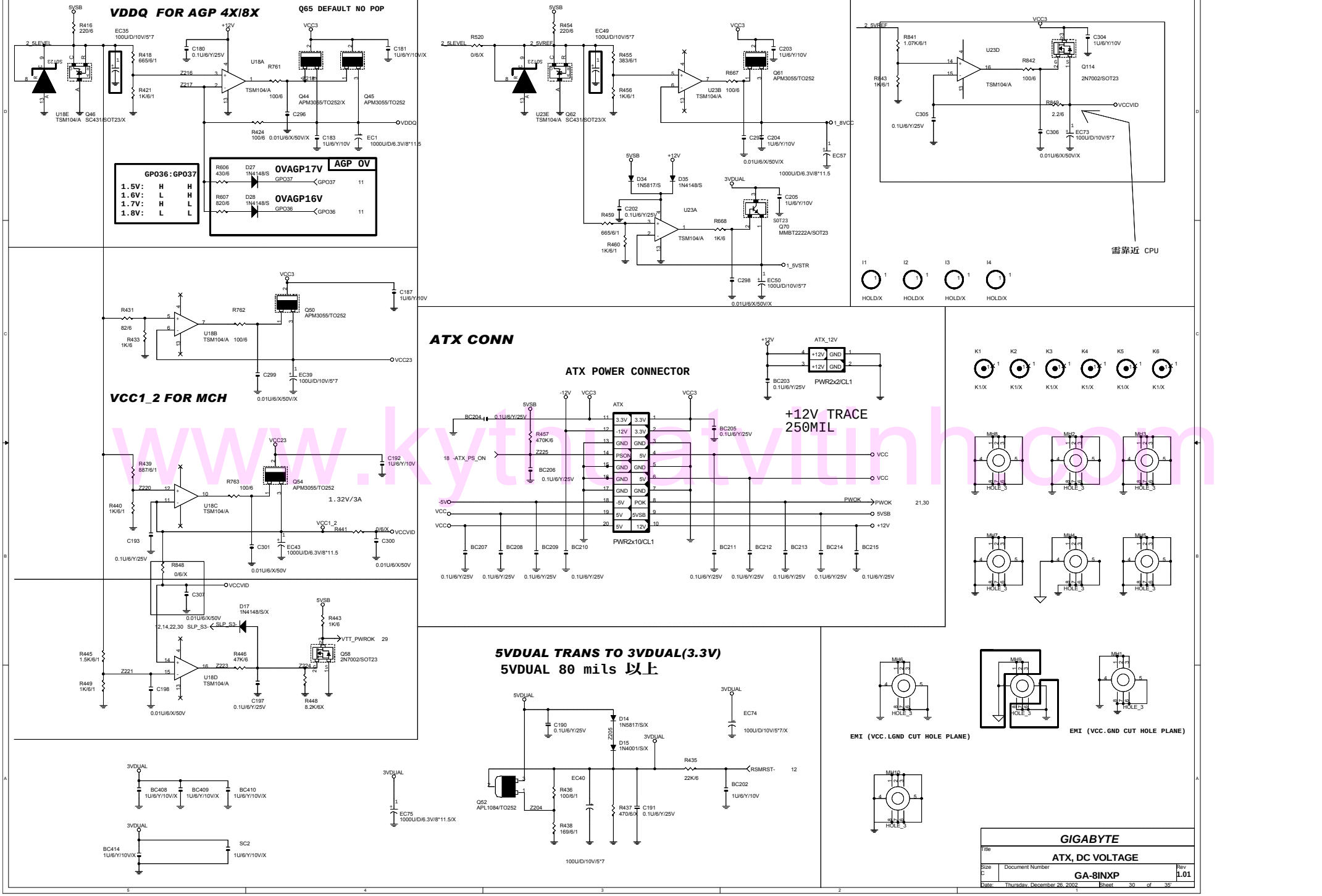

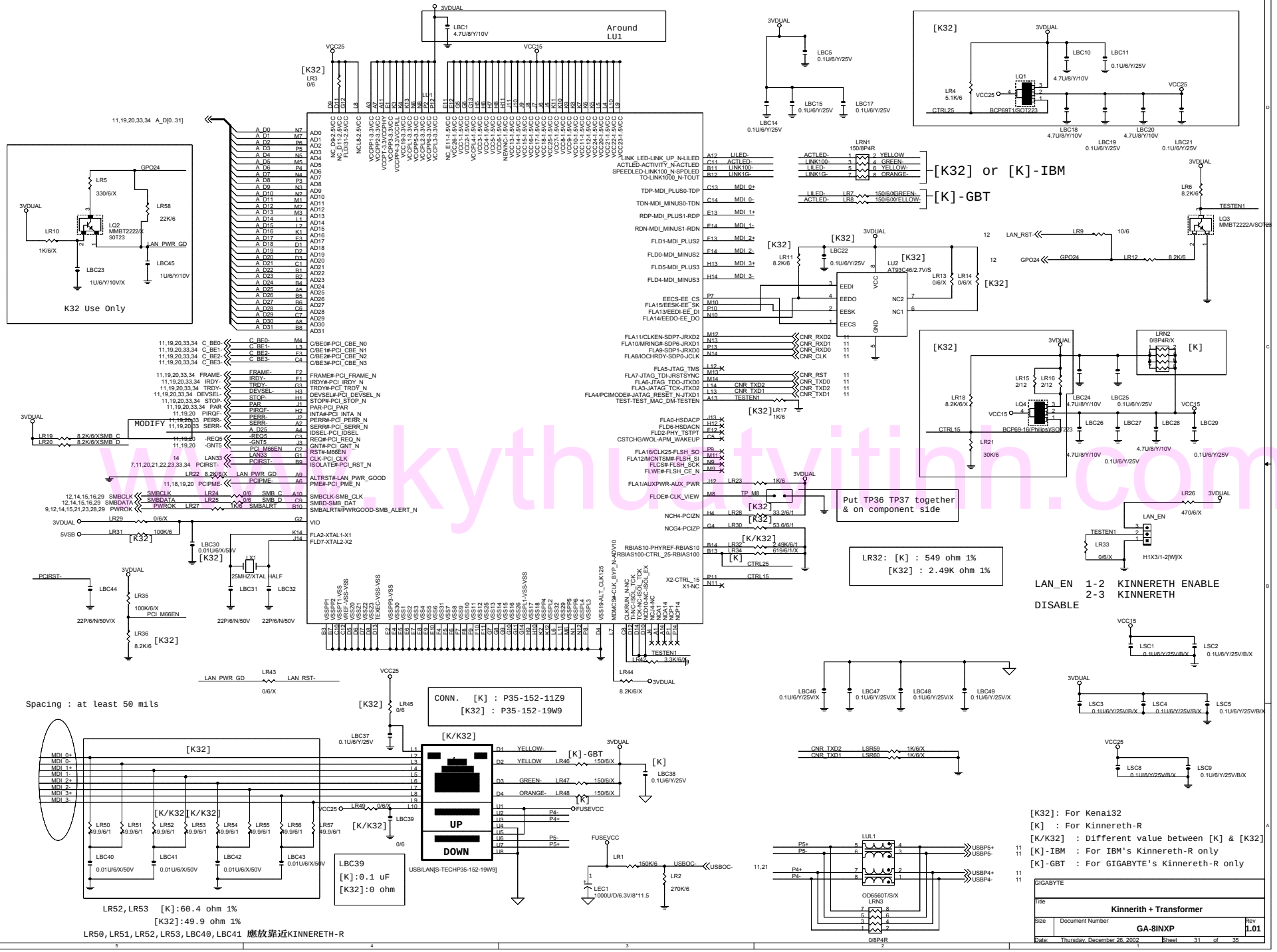

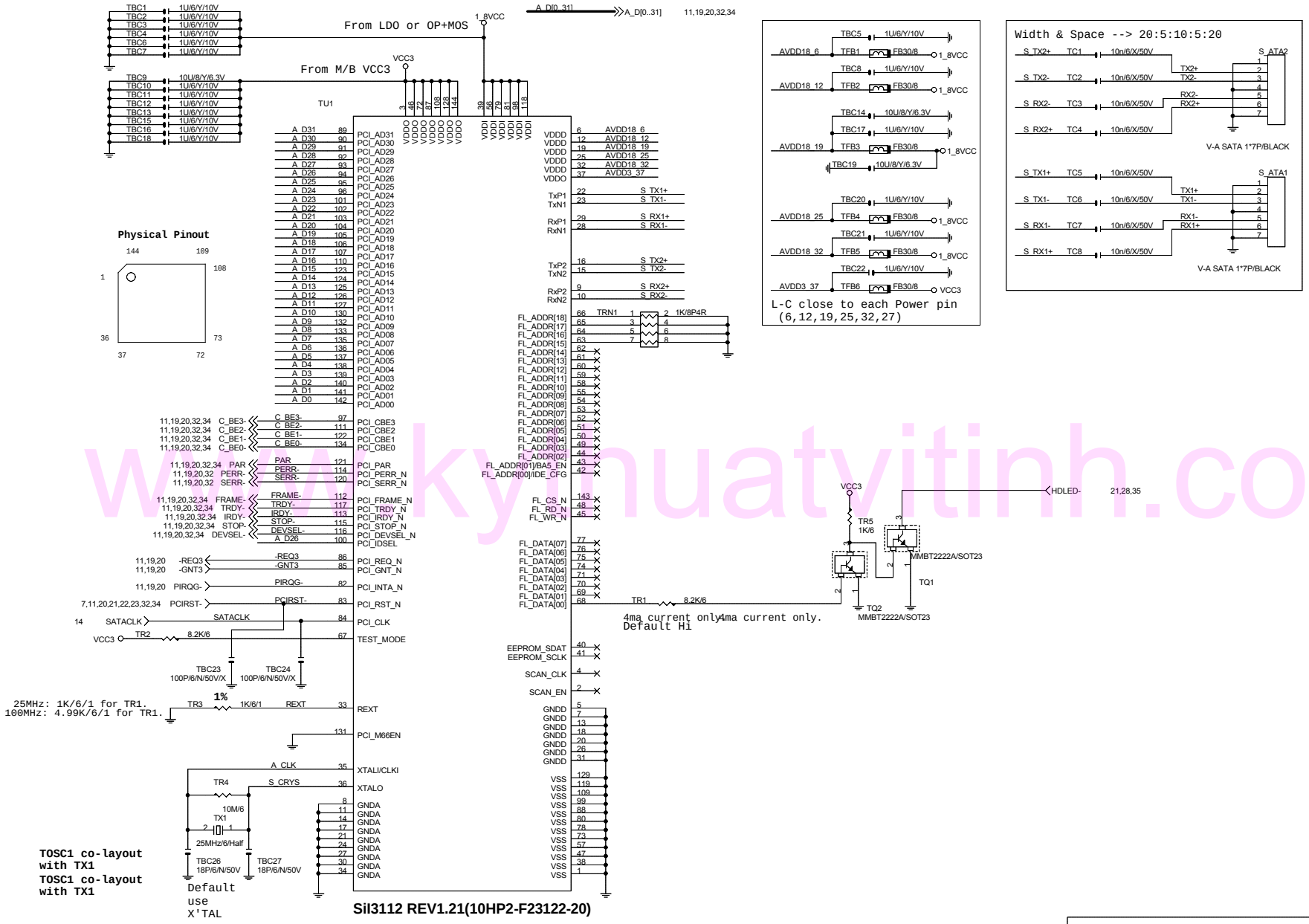

1. TX+/- & RX+/- 儘可能Reference GND, 換層時須在其Via hole旁5mil處左右各打一個GND Via。
1. TX+/- & RX+/-兩旁最好能包地。

GIGABYTE		
Title: Silicon Image Sil3112(S-ATA)		
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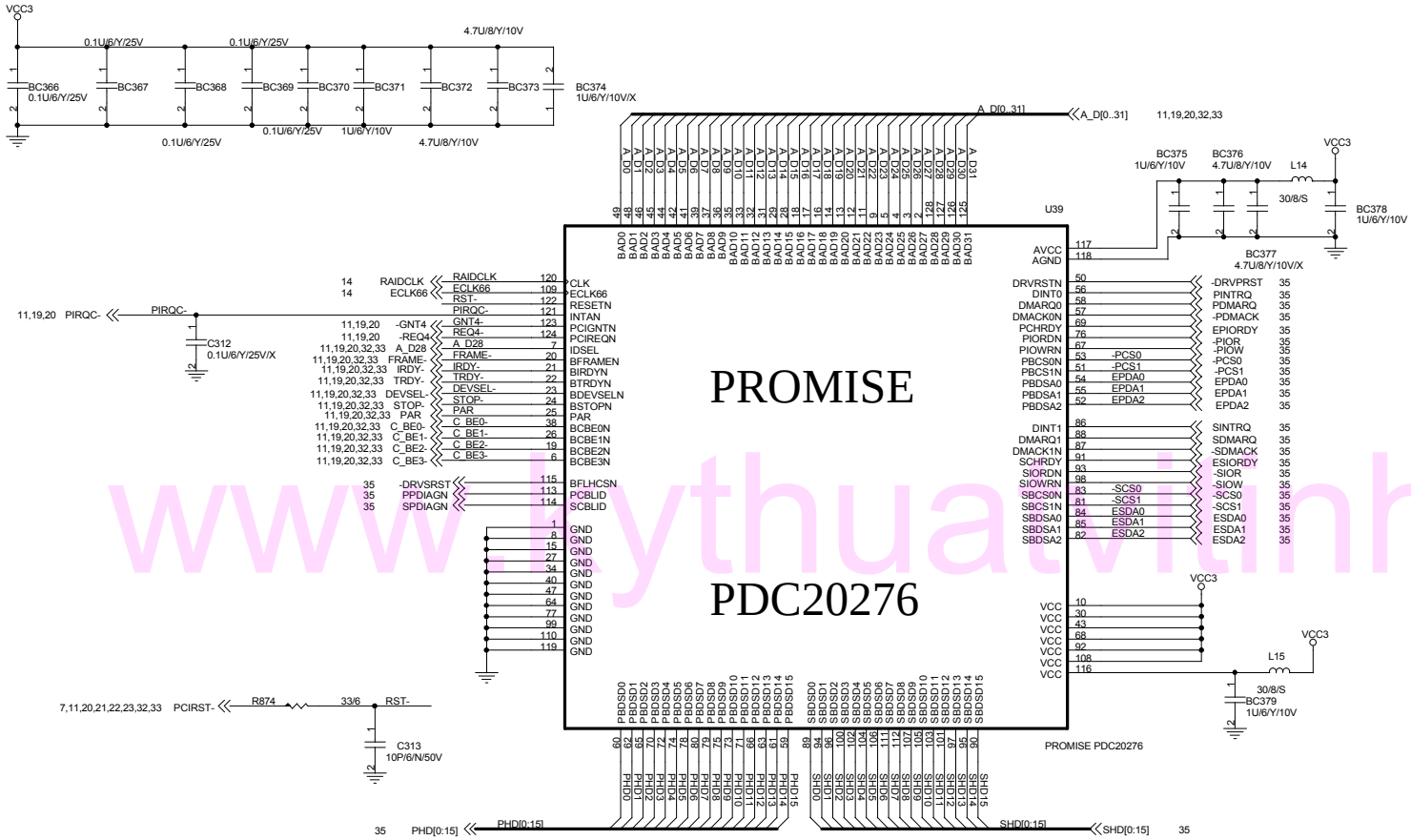
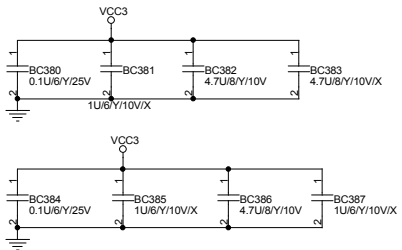


WIDER TRACE FOR POWER



GIGABYTE TECHNOLOGY CORPORATION	
Title	ATA133 & IDE RAID
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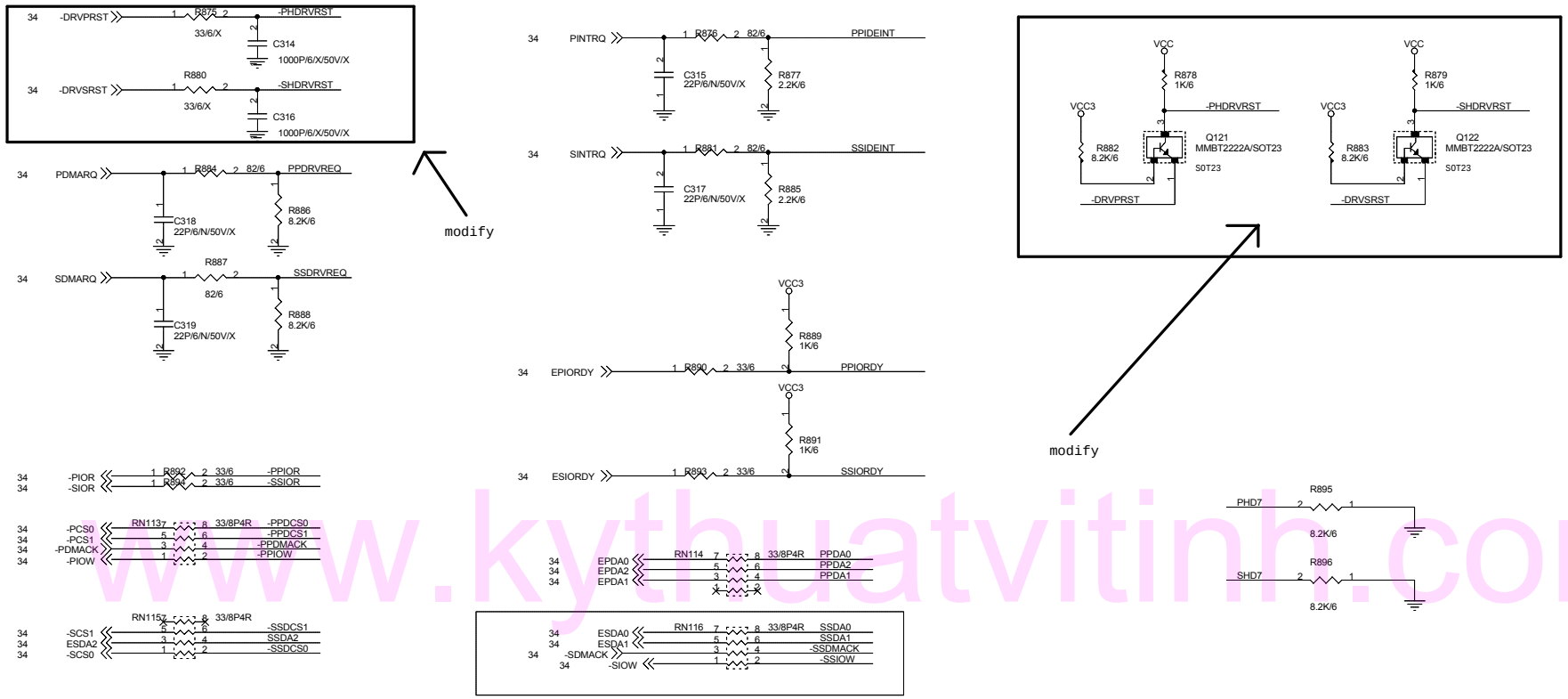

附件三

GIGABYTE TECHNOLOGY CORPORATION		
Title: ATA133 & IDE RAID		
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