D45/D46 Block Diagram

Project code: 91.4J001.001--D45
91.4K001.001--D46
PCB P/N : 07248
REVISION : SA

CLK GEN.
ICS9LPRS365YGLFT-GP
3
RTM875T-606-VD-GRT

Mobile CPU
Penryn
4, 5

G7921
20

HOST BUS 667/800/1066MHz@1.05V

DDR2 socket
12,13
800/667MHz

DDR2 socket
12,13
800/667MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CNTIG.00U
6,7,8,9,10,11

PCI-EG

ATI
M82M
VRAMx4 256MB
41~47

LVDS WXGA/SXGA+ 15"LCD 14
RGB CRT CRT 13
S-Video S-Video 13

X4 DMI 400MHz
C-Link0

Headphone Out
MIC In
29 INT.MIC
29 INT.SPKR

Codec
ALC269
29

AZALIA

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH9M.00U
16,17,18,19

PCI-E/USB 2.0 New card 25 G577 25

PCI-E USB Cardreader JMICRO380 26 MS/MS Pro/ MMC/SD 4 in 1 26
1394

PCI-E LAN TRL8111C 23 TXFM 24 RJ45 24

PCI-E /USB 2.0 Mini Card Kedron a/b/g/n 25

PCI-E /USB 2.0 Mini Card UMTS(3G) 25

LPC BUS

RJ11
MODEM MDC Card
22

SATA
SATA
SATA
USB0
USB

BlueTooth 22

KBC
Winbond
WPC773
28

SPI I/F

BIOS
4M byte
28

LPC
DEBUG CONN.
27

HDD 21
CDROM 21
eSATA /USB 22
USB 3 Port 22
CAMERA 14
Touch Pad 27
INT. KB 27

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 34

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC TPS51124 36

INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D8V_S3(10A)

RT9026 35

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

G9131 35

3D3V_S0	2D5V_S0 (300mA)

APL5912 35

1D8V_S3	1D5V_S0

NB DC/DC ISL6263A 37

INPUTS	OUTPUTS
DCBATOUT	GFX_CORE

CHARGER BQ24745 38

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6266A 33

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: BLOCK DIAGRAM
Size: D45/D46 Rev: PD
Date: Sheet 1 of 47

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

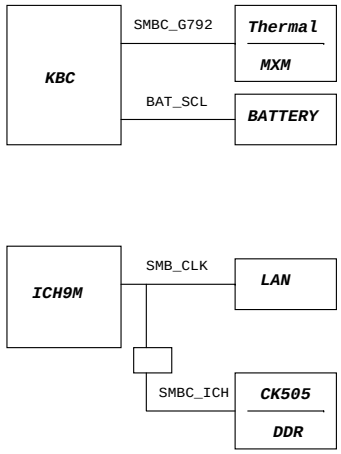
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	Combo(ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

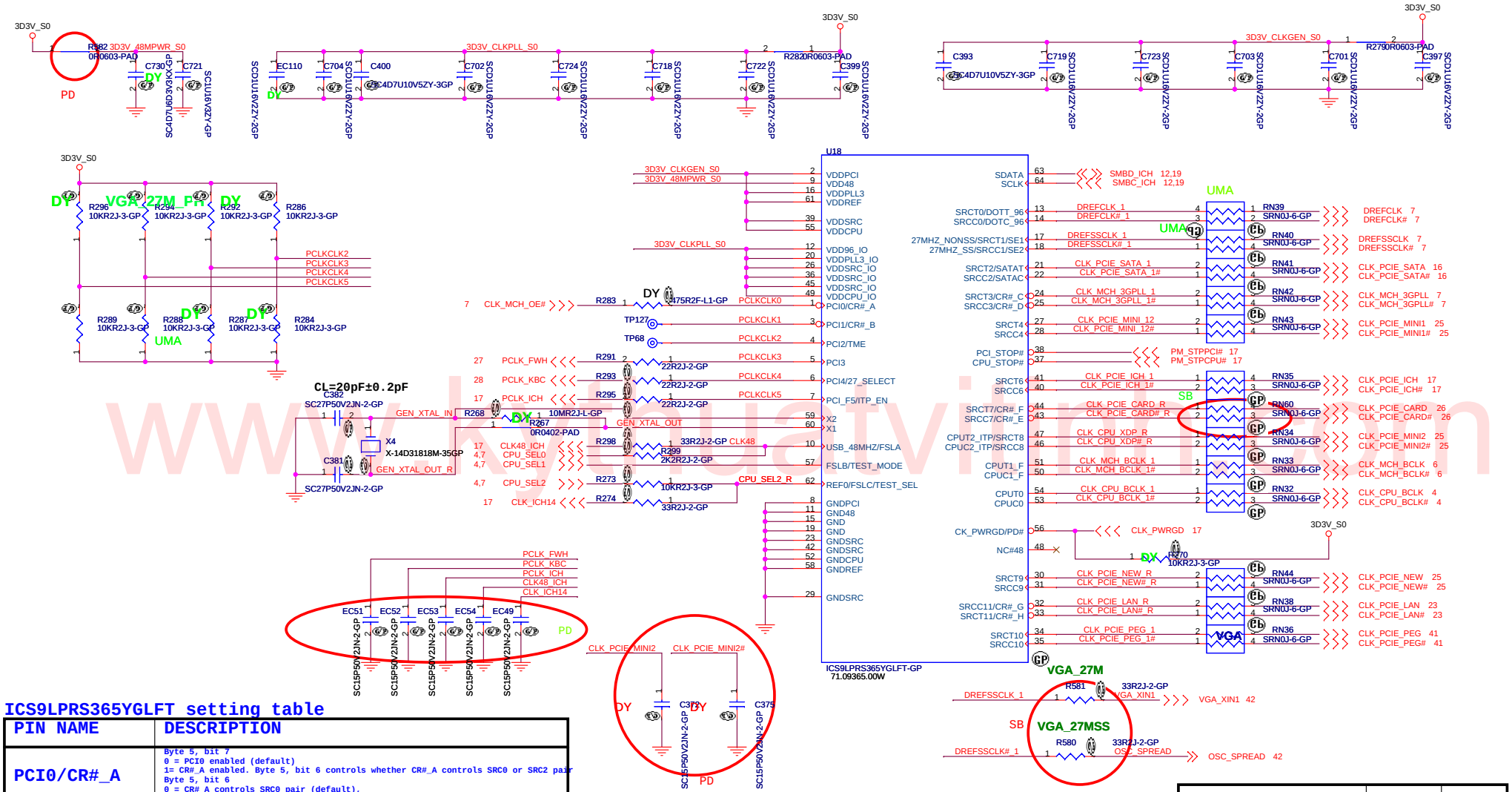
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size	Document Number	Rev
	D45/D46	PD

Date: Friday, March 14, 2008 Sheet 2 of 47



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

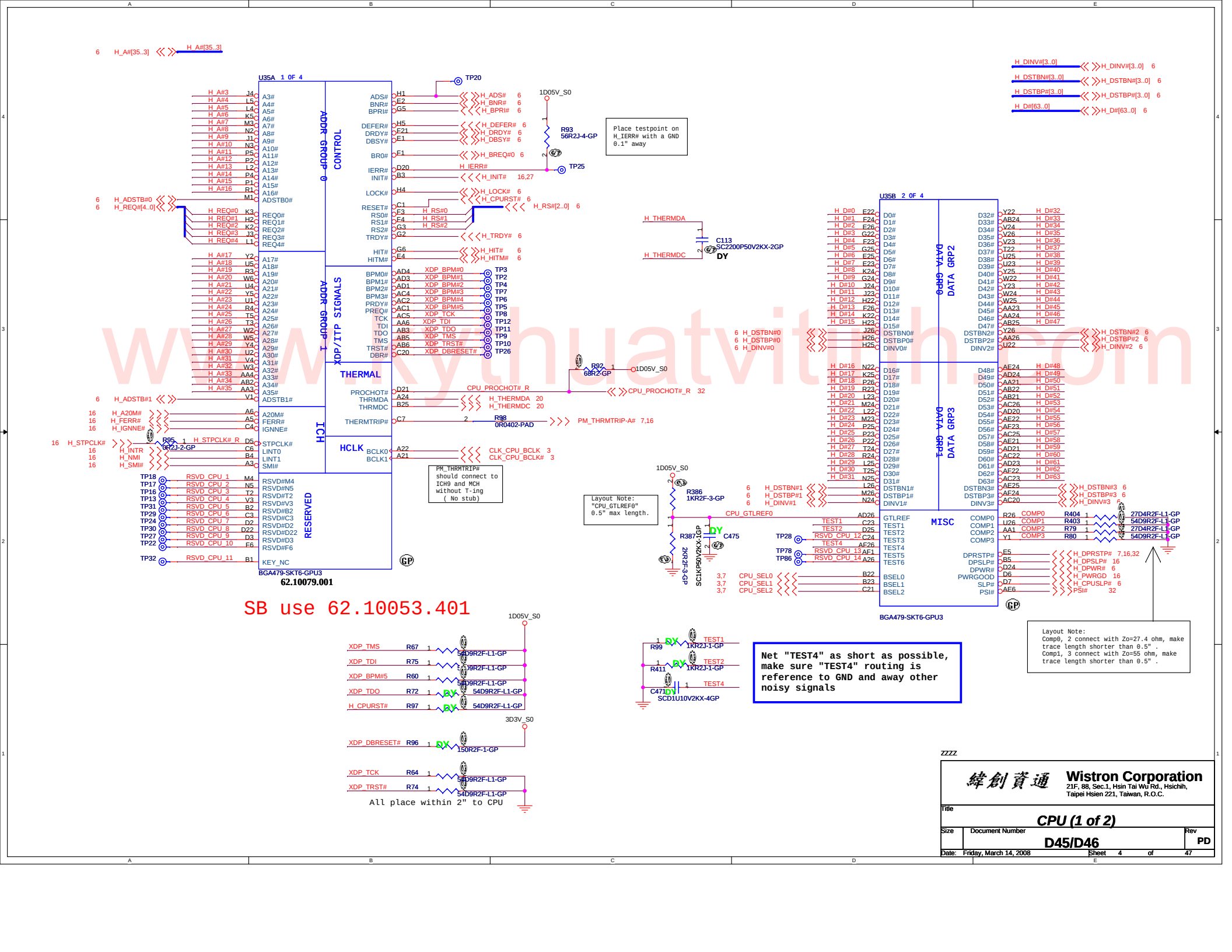
UMA

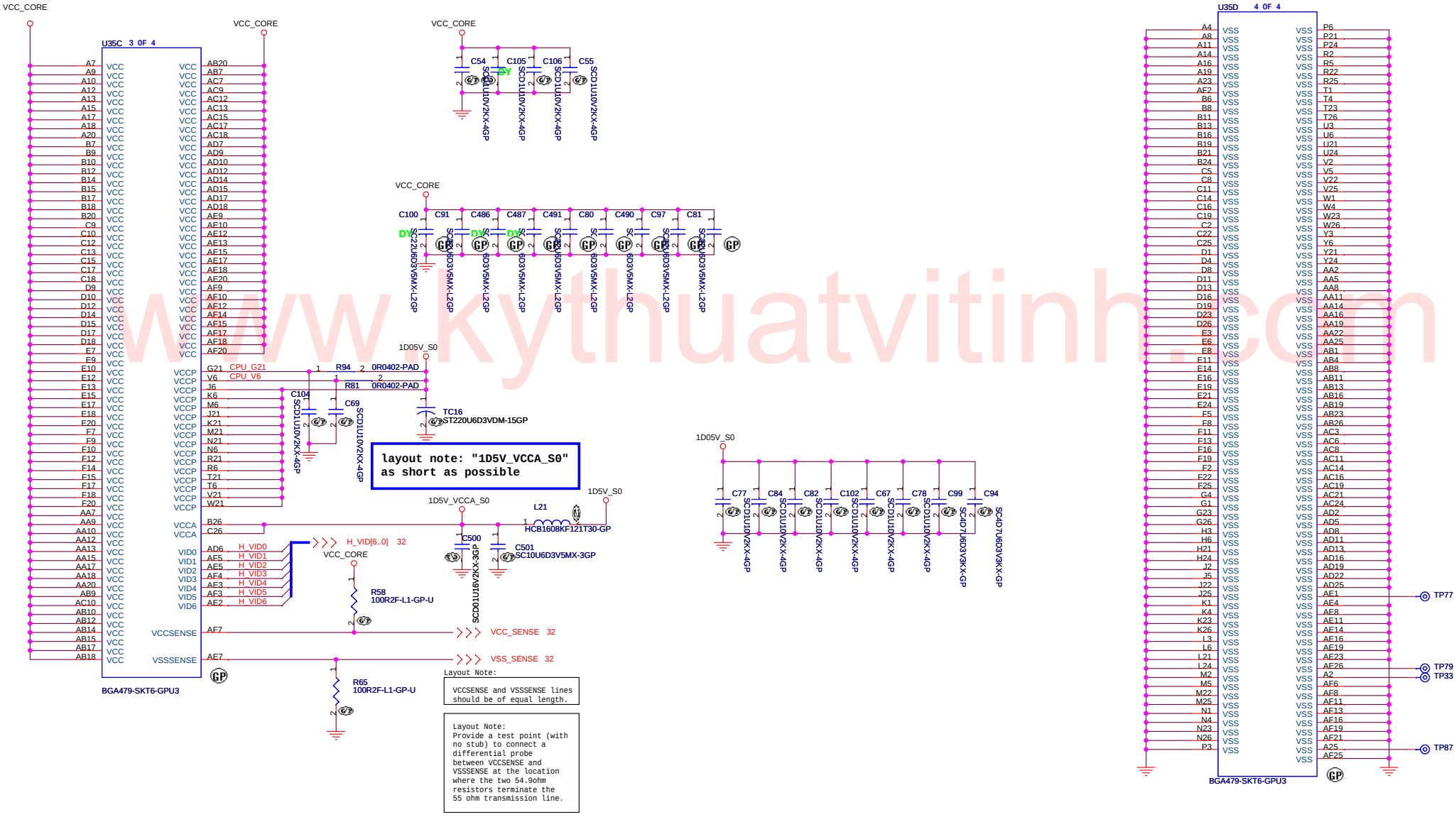
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

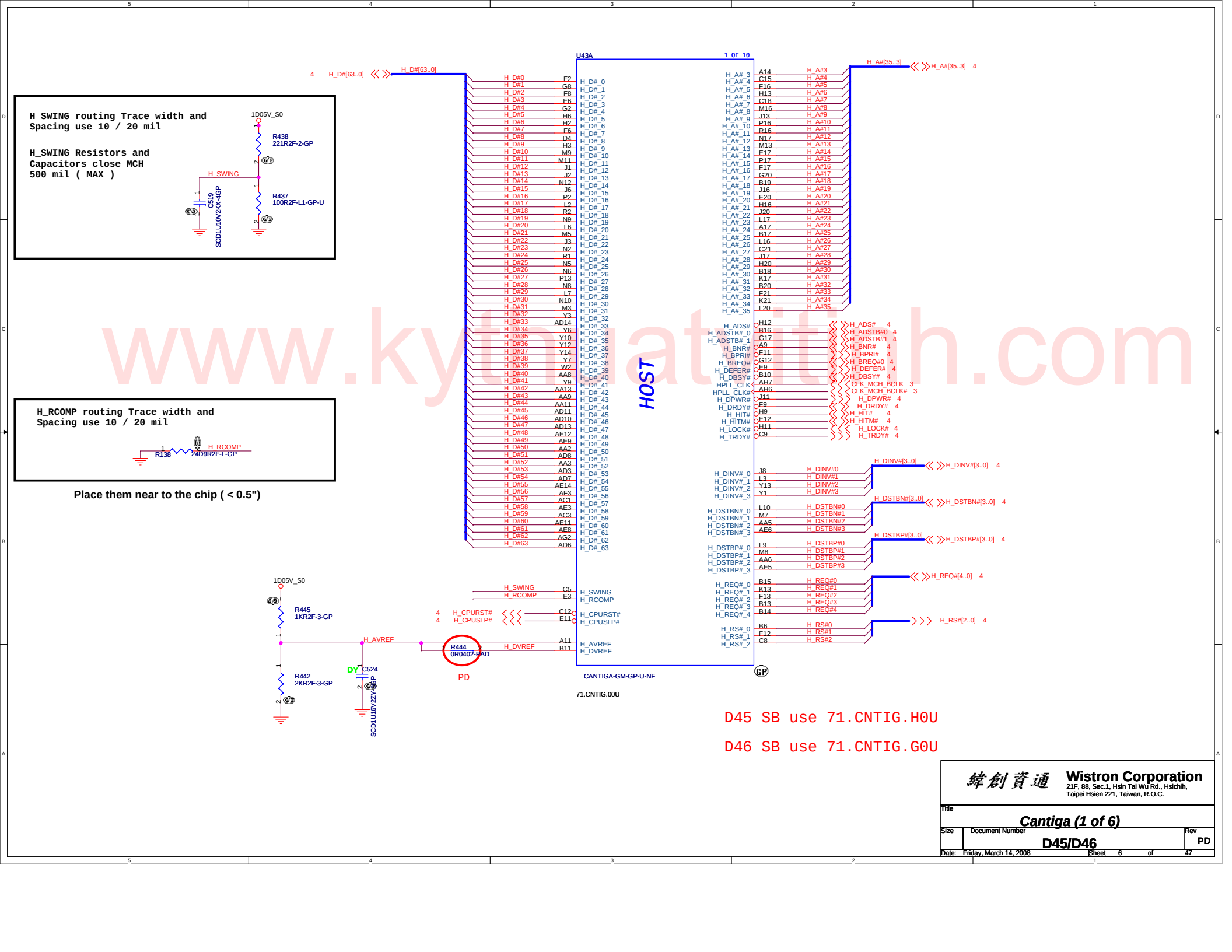
Size | Document Number: D45/D46 | Rev: PD

Date: Tuesday, March 18, 2008 | Sheet 3 of 47

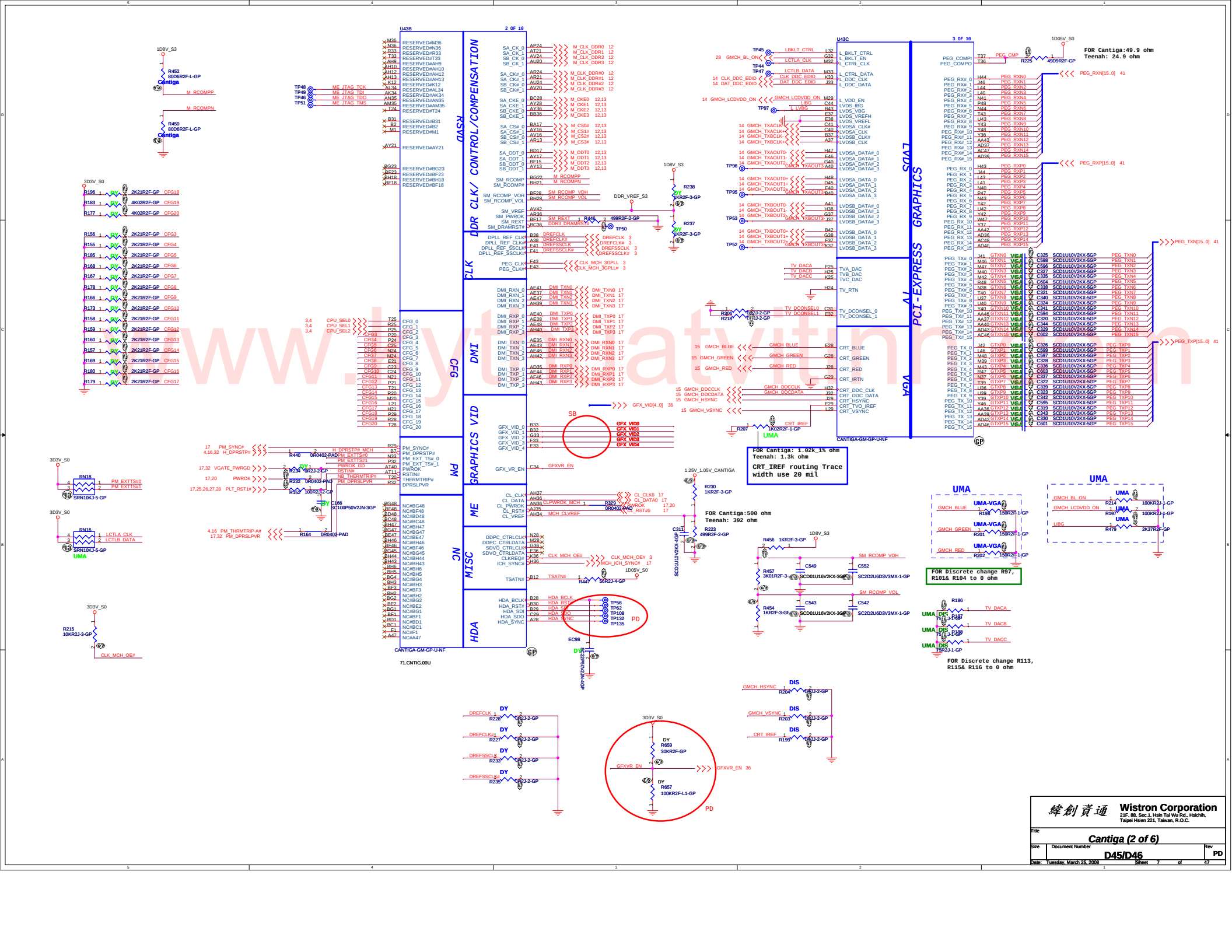


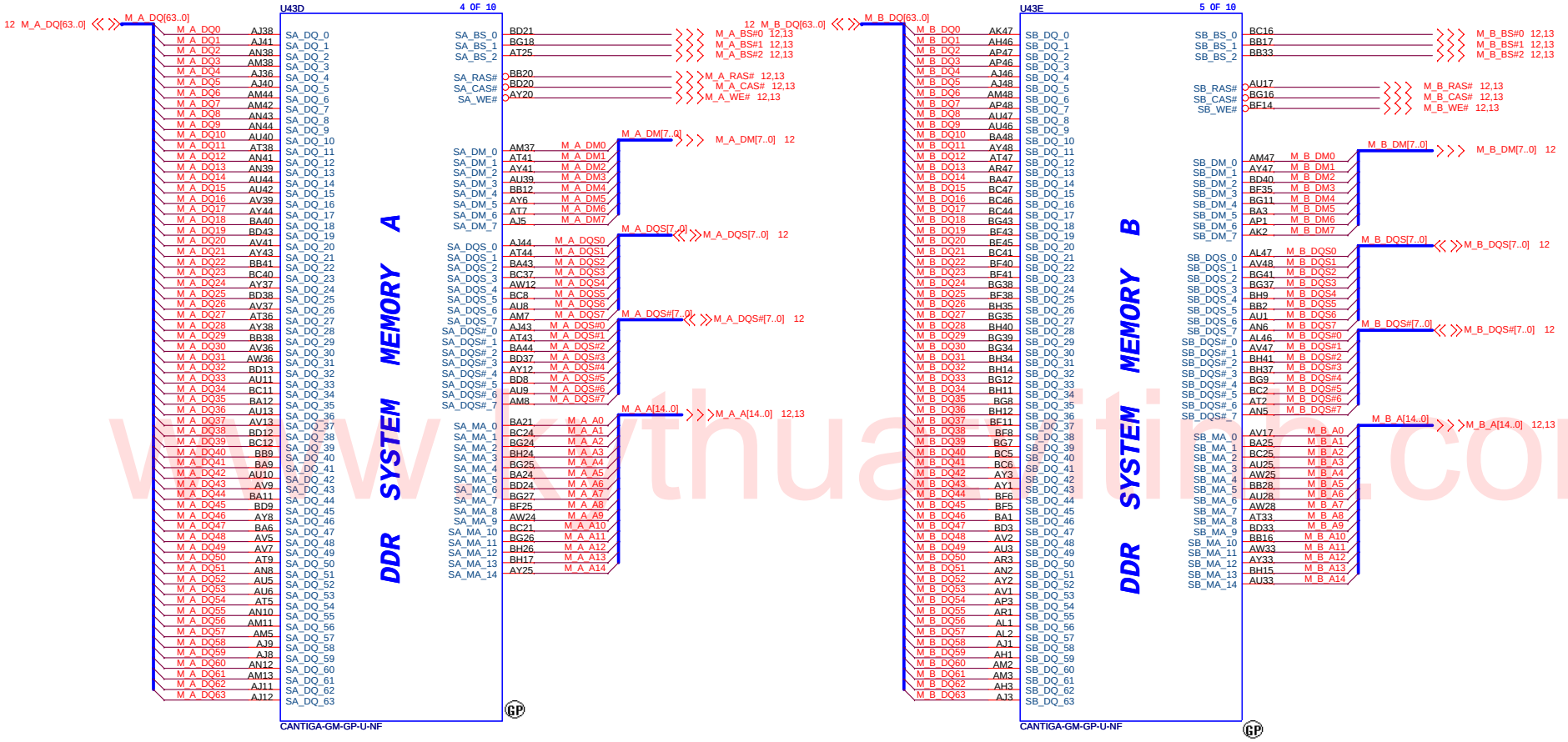


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (2 of 2)	
Size	Document Number: D45/D46
Rev: PD	
Date: Friday, March 14, 2008	Sheet 5 of 47

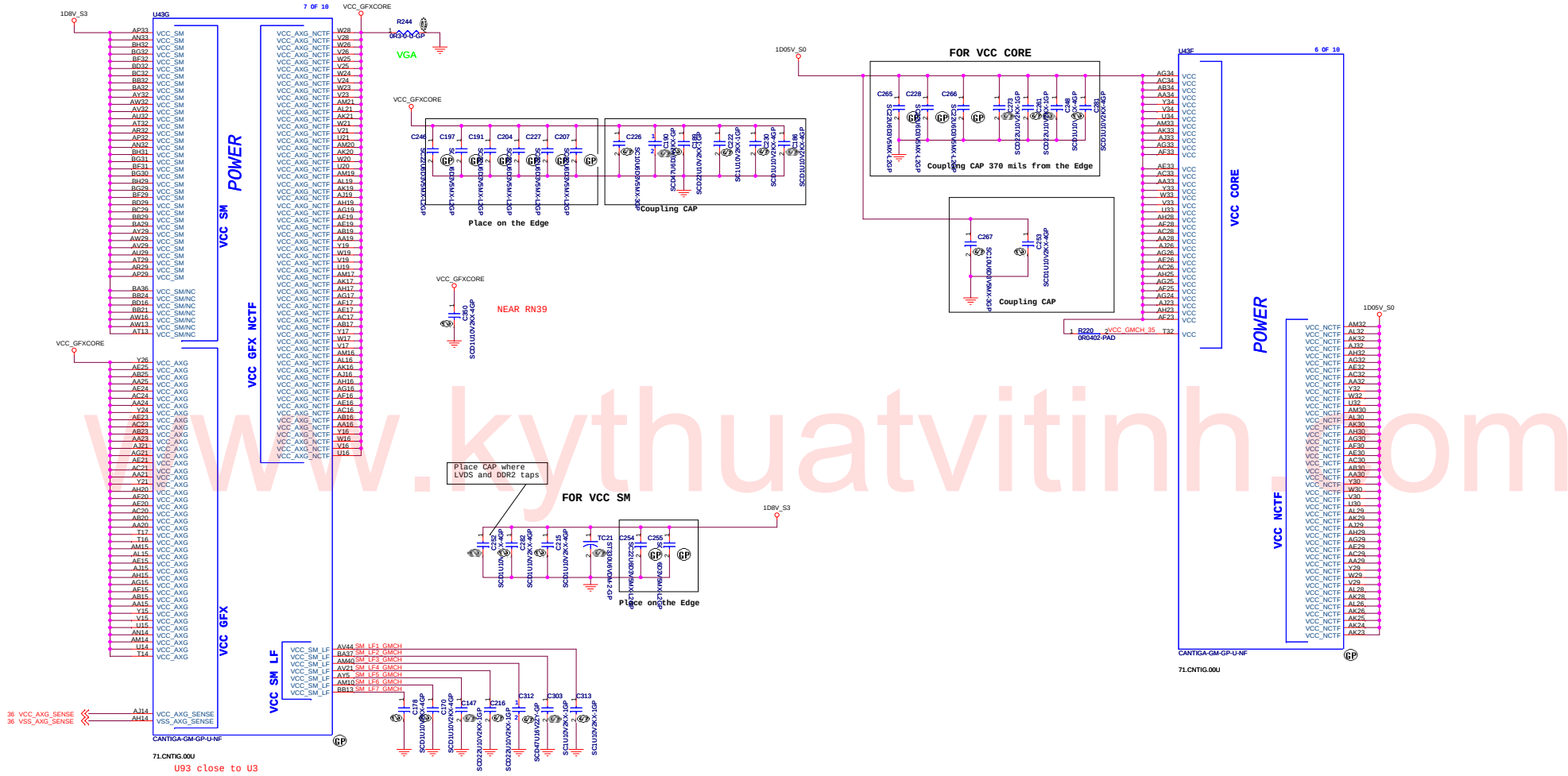


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Cantiga (1 of 6)
Size	Document Number: D45/D46
Rev	PD
Date: Friday, March 14, 2008	Sheet 6 of 47

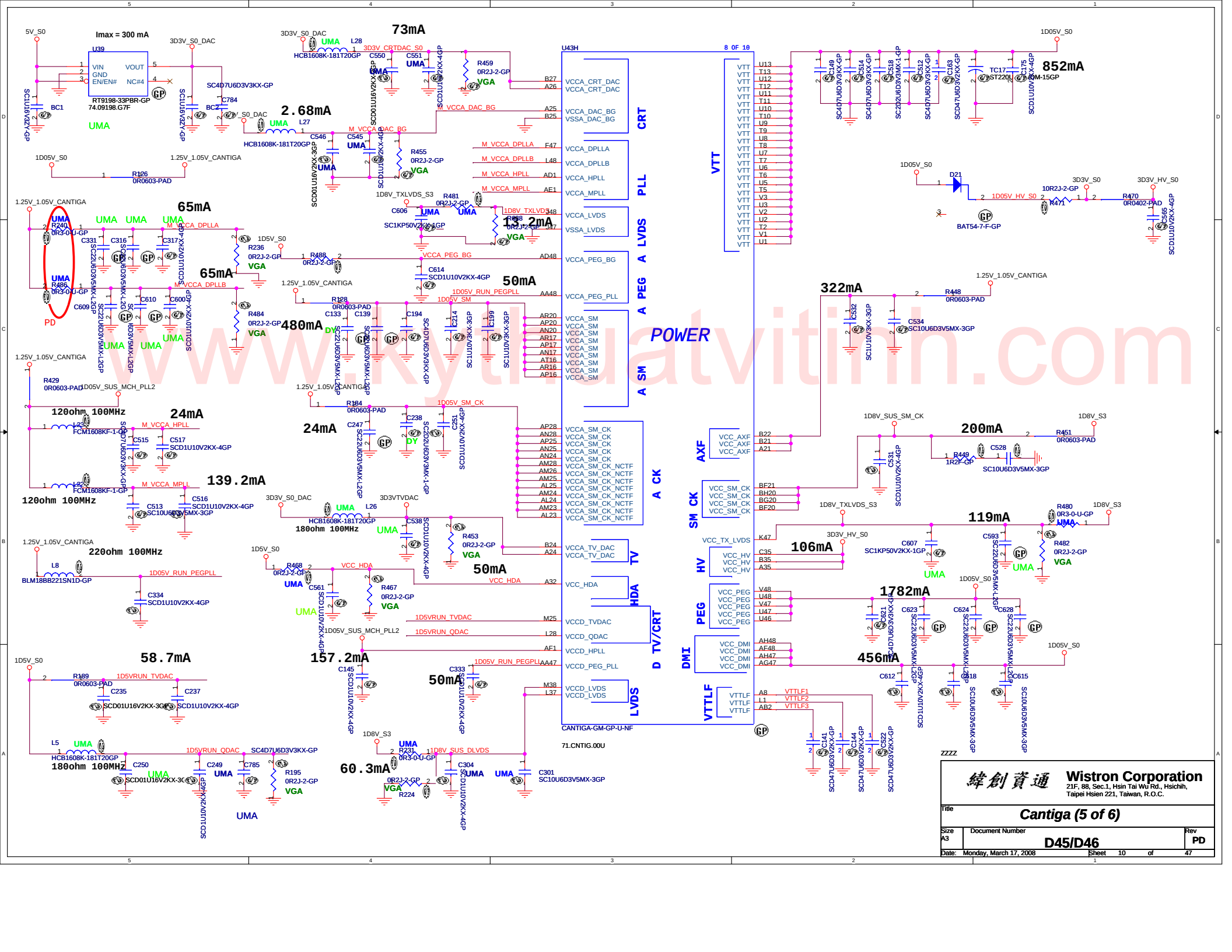

U43B
2 OF 10
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
HDA
U43C
3 OF 10
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
FOR Cantiga:49.9 ohm
Teenah: 24.9 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Discrete change R97,
R101& R104 to 0 ohm
FOR Discrete change R113,
R115& R116 to 0 ohm
UMA
PD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga (2 of 6)
D45/D46
Tuesday, March 25, 2008
Sheet 7 of 47

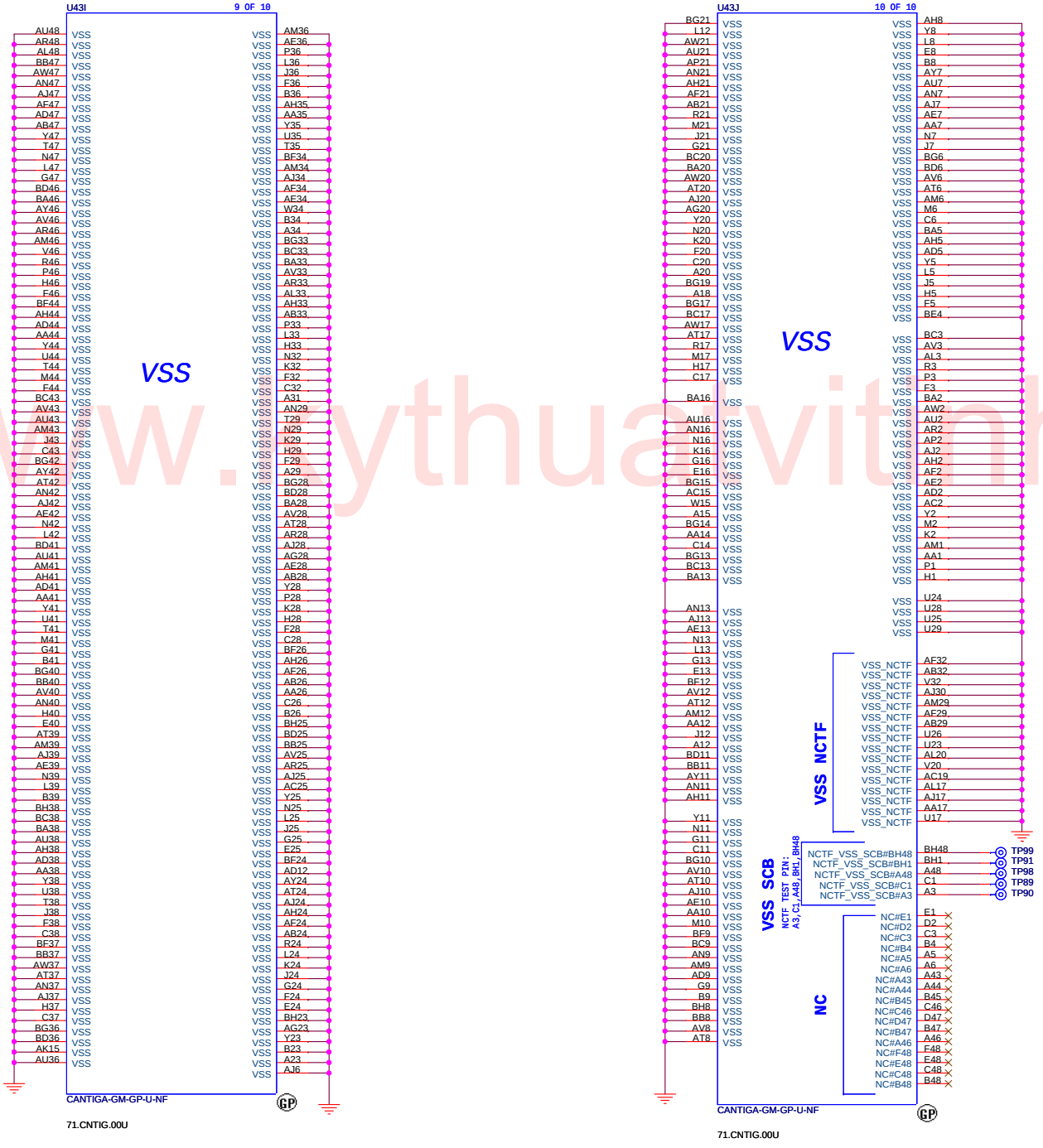


緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Cantiga (3 of 6)	
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 8 of 47	



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Cantiga (4 of 6)	
Size	Document Number: D45/D46	Rev: PD
Date: Monday, March 24, 2008	Sheet 9 of 47	


POWER
73mA
2.68mA
65mA
65mA
480mA
50mA
24mA
139.2mA
50mA
157.2mA
50mA
58.7mA
60.3mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
Imax = 300 mA
RT9198-33PBR-GP
74.09198.G7F
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga (5 of 6)
D45/D46
PD
Monday, March 17, 2008
Sheet 10 of 47



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga (6 of 6)***

Size | Document Number: **D45/D46** | Rev: **PD**

Date: Friday, March 14, 2008 | Sheet 11 of 47

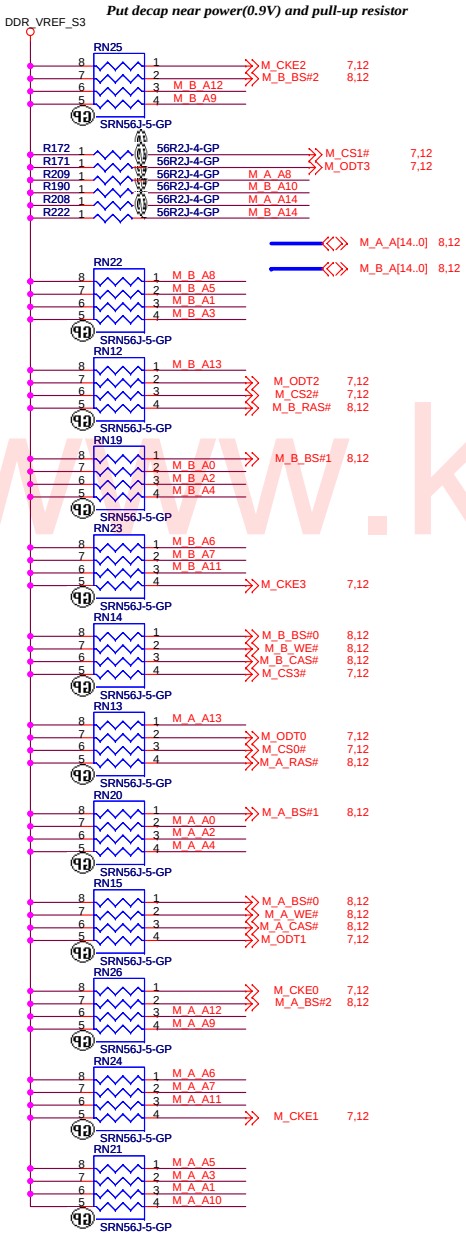
DDR SOCKET

D45 46 use 62.10017.631

緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR2 Socket
Size	Document Number: D45/D46
Rev	PD
Date: Friday, March 14, 2008	Sheet 12 of 47

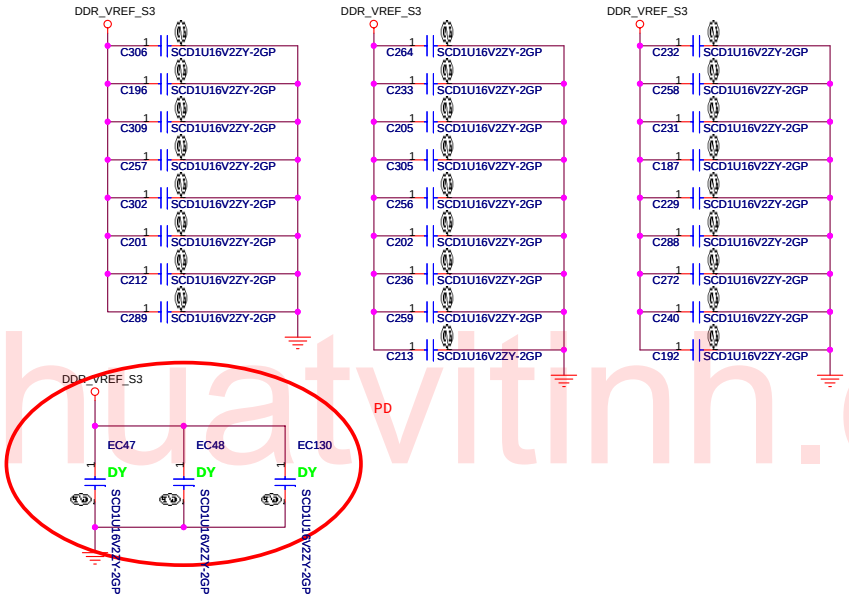
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

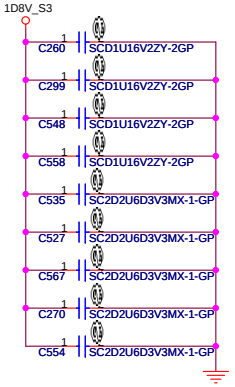


Decoupling Capacitor

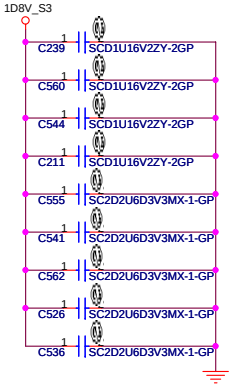
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



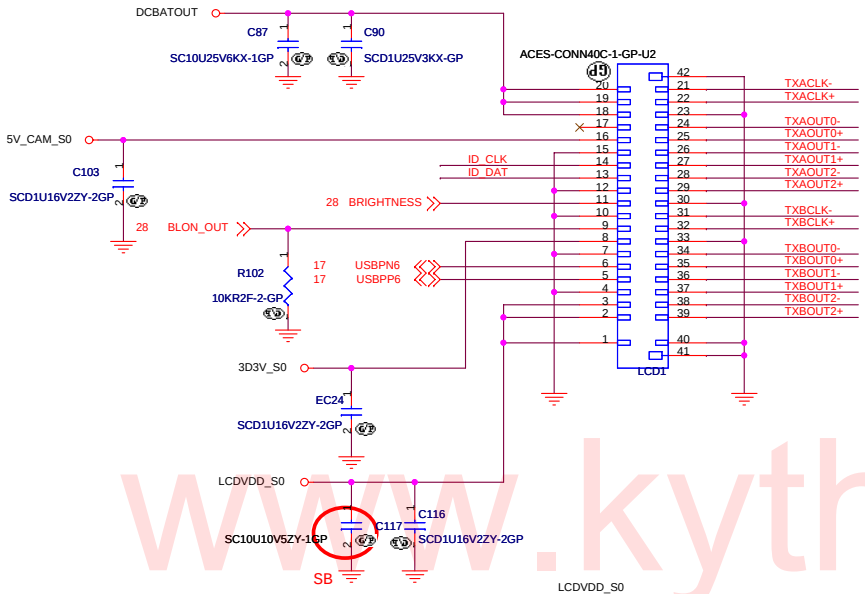
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

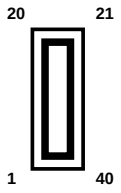
Size	Document Number	Rev
	D45/D46	PD

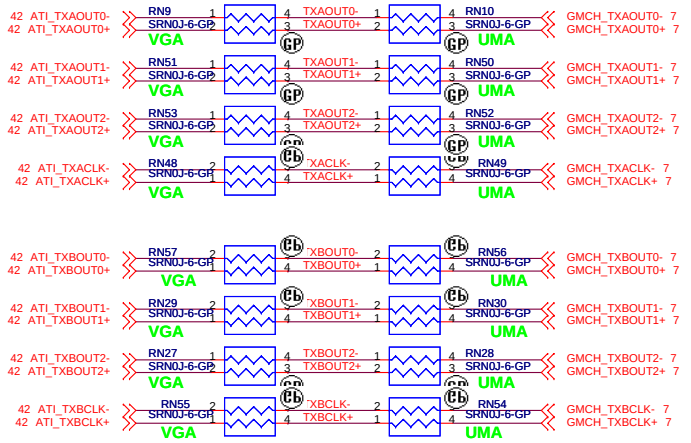
Date: Wednesday, March 19, 2008 Sheet 13 of 47

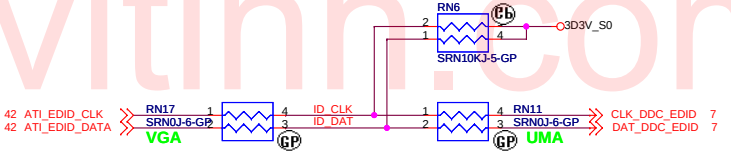
LCD CONNECTOR

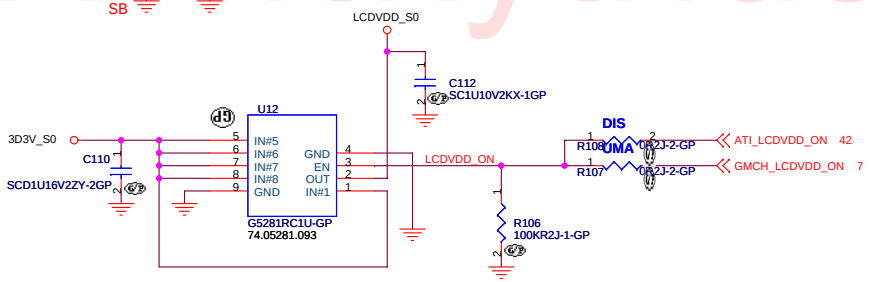


TOP VIEW

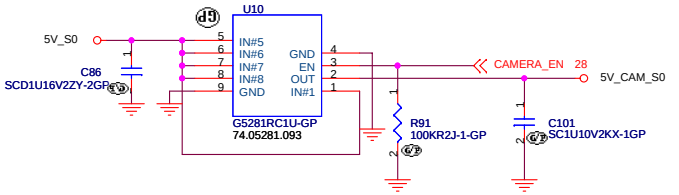


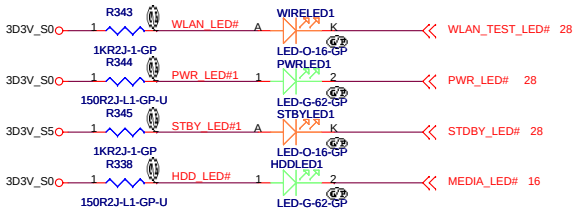


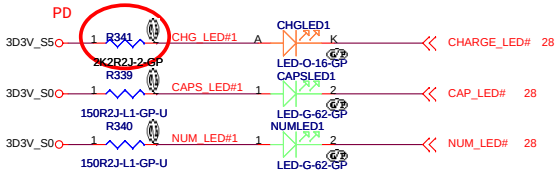




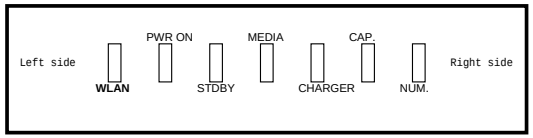
WEBCAM POWER







LED Location and Sequence (The edge of PCB,Top view)



zzzz

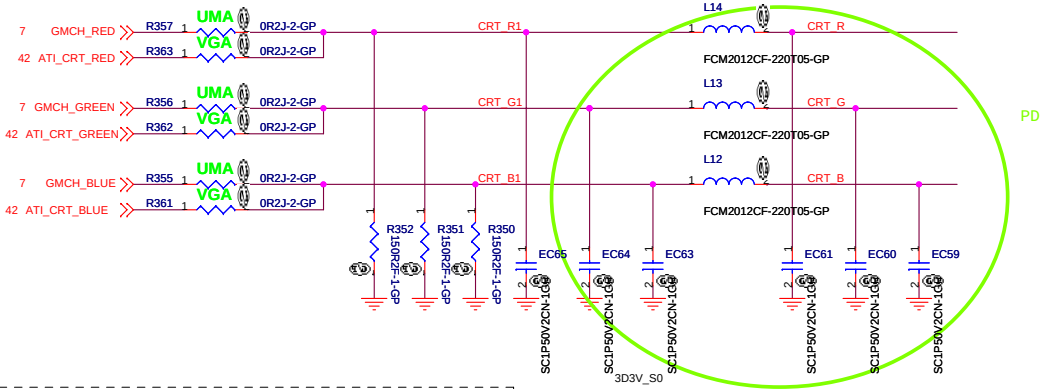
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD CONN / LED / WEBCAM
Size A3 / Document Number	D45/D46
Rev	PD
Date: Friday, March 14, 2008	Sheet 14 of 47

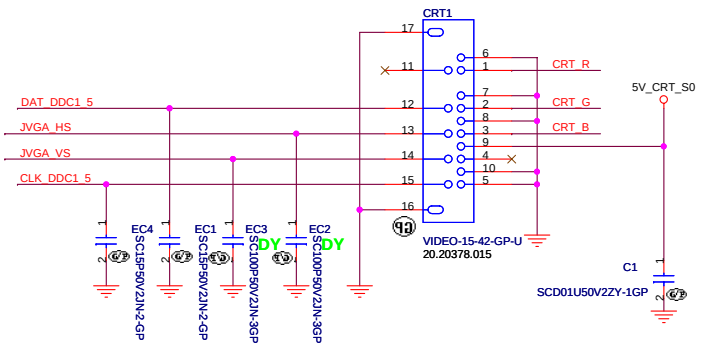
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

PD use 22 ohm 68.00215.211

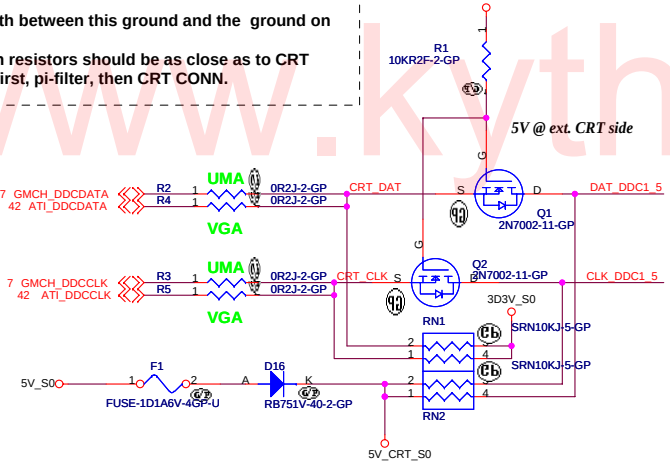
CRT I/F & CONNECTOR



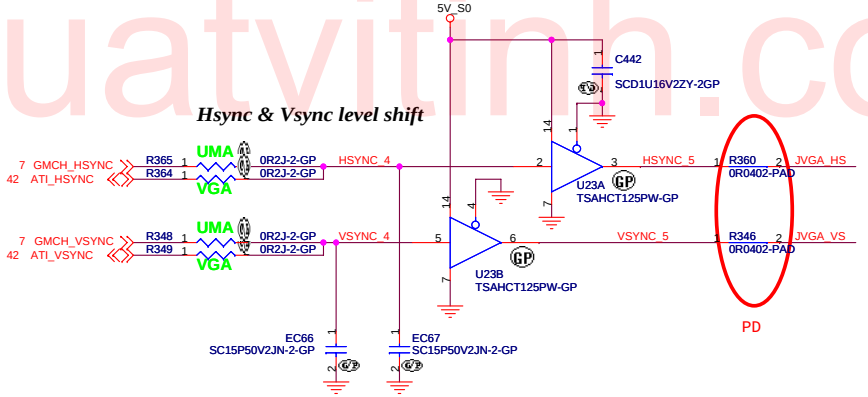


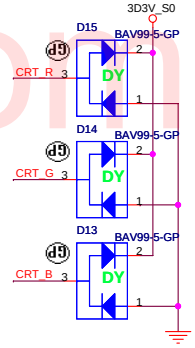
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V @ ext. CRT side

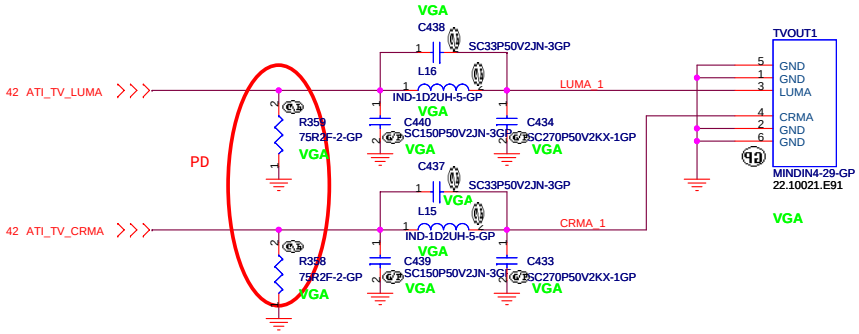


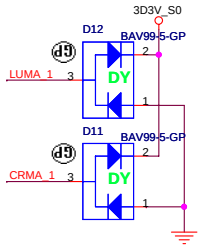
Hsync & Vsync level shift



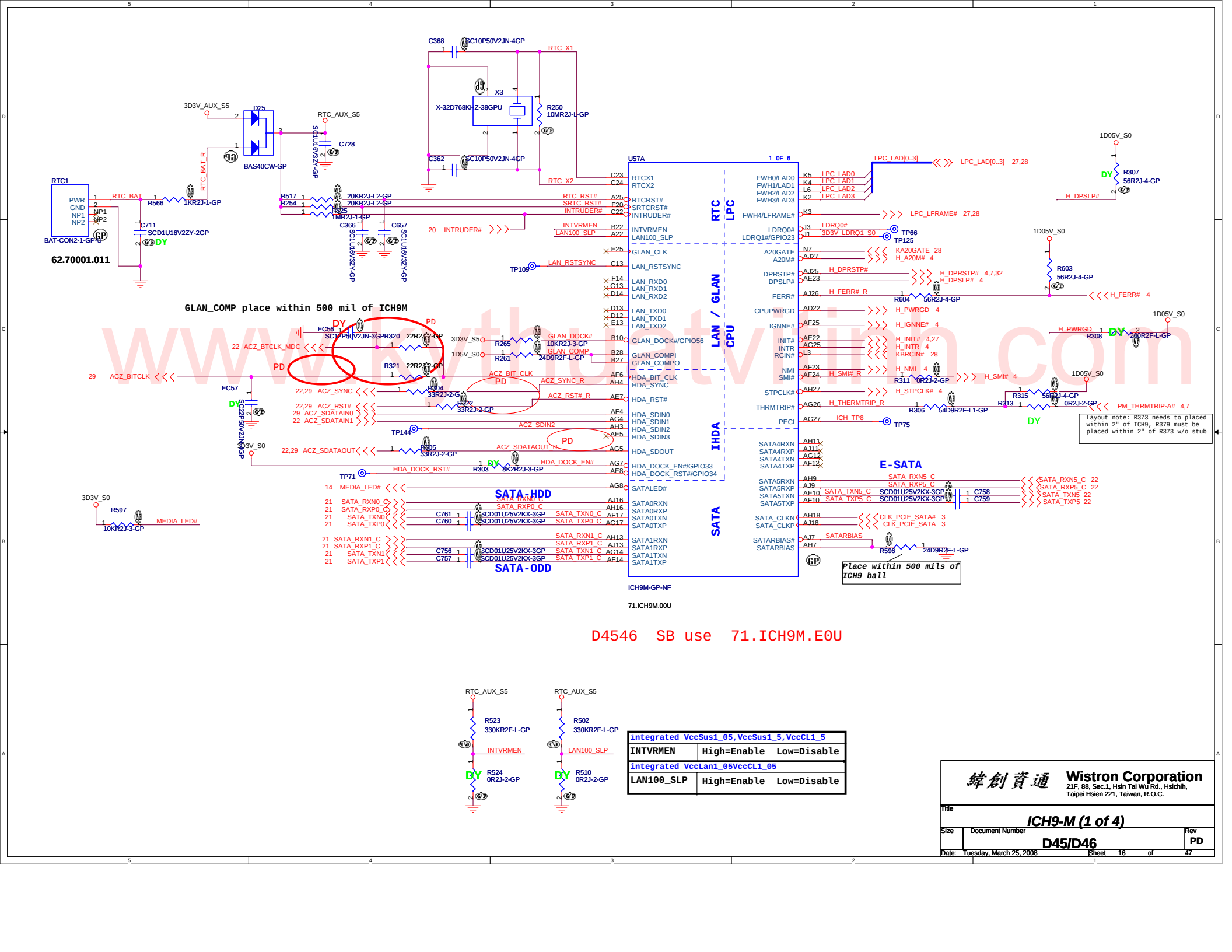


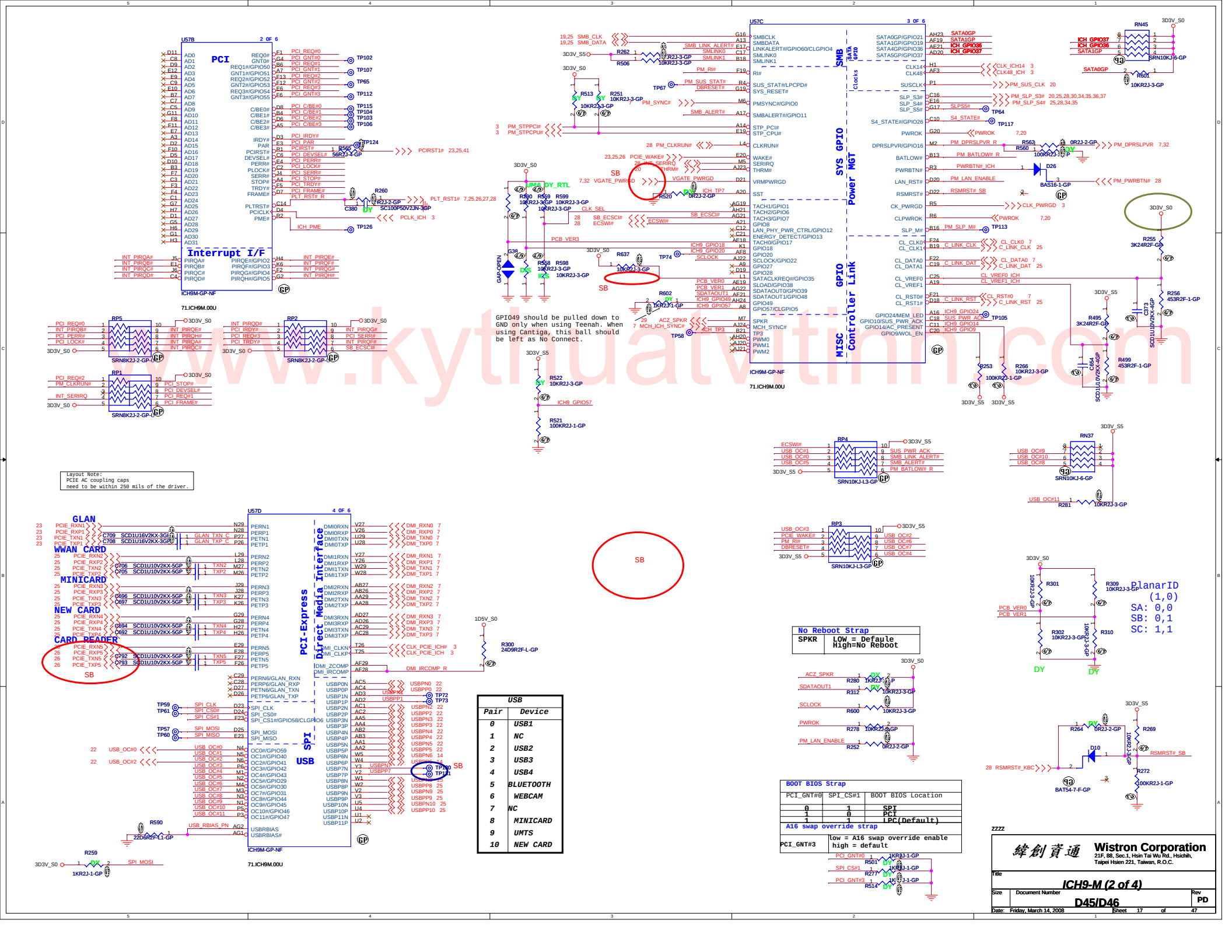
TV CONN

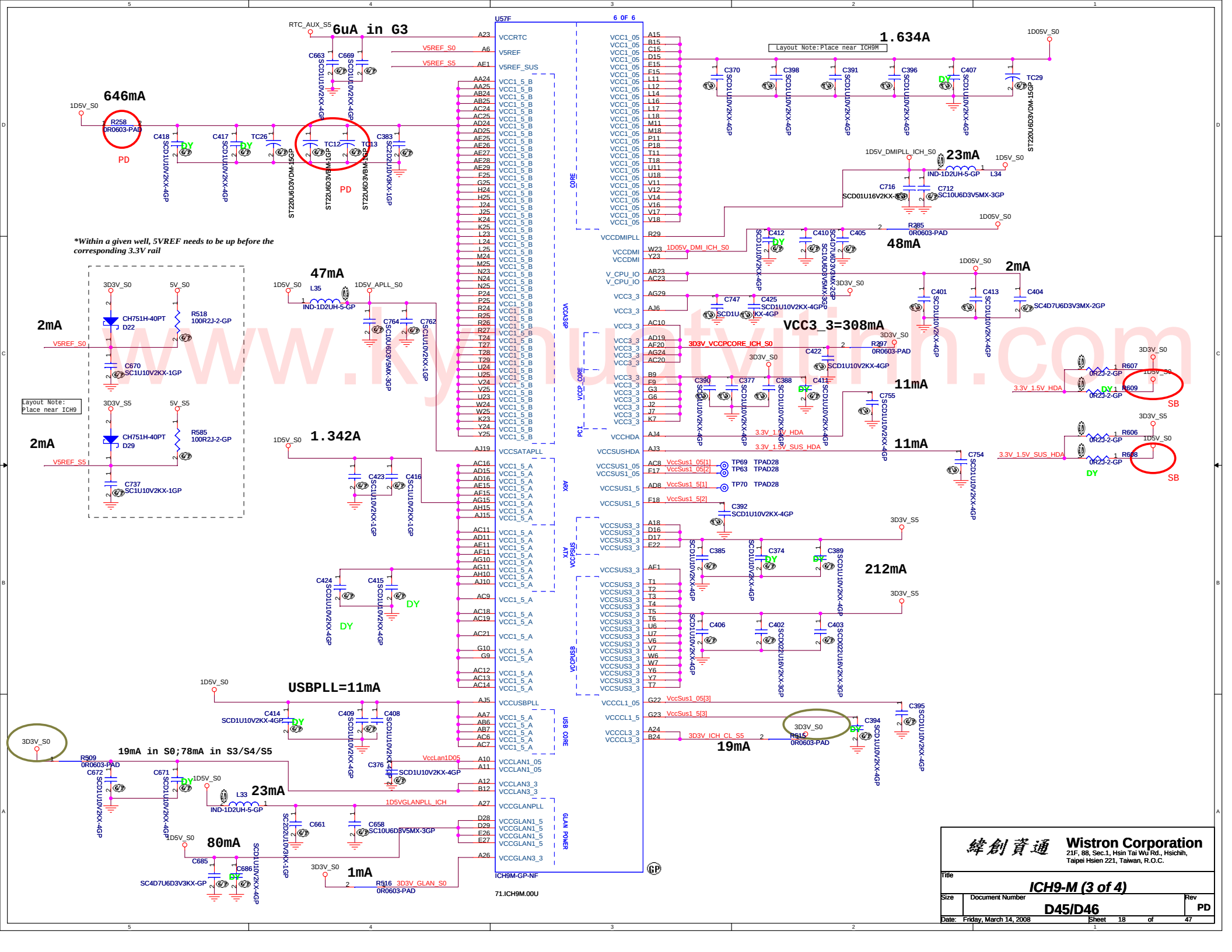


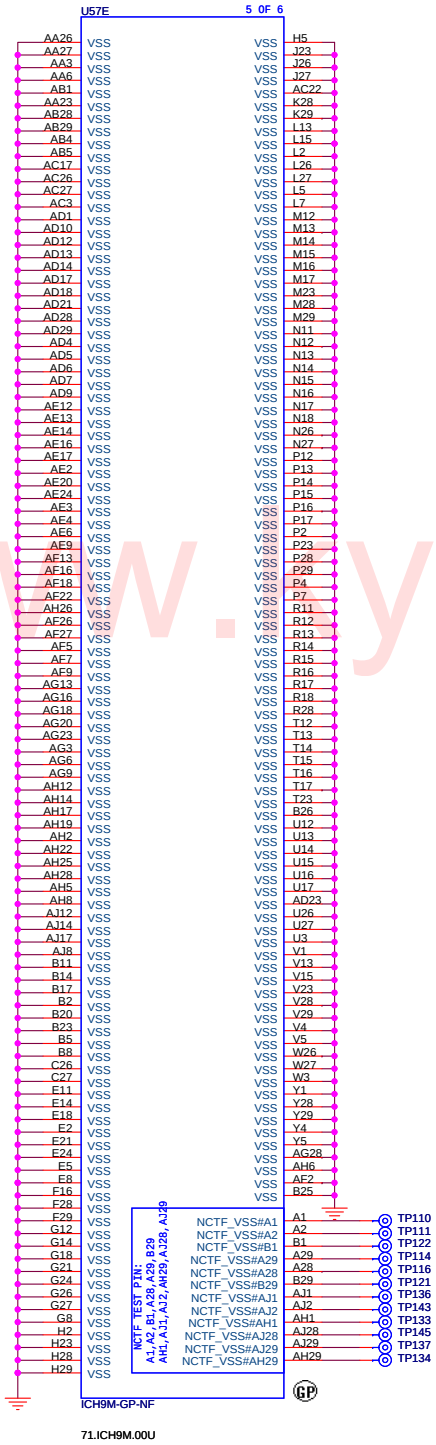


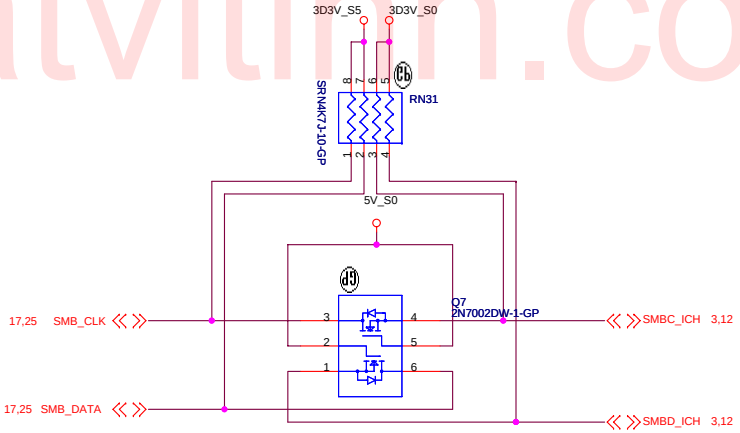
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT/TV Connector***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Tuesday, March 18, 2008	Sheet 15 of 47	


GLAN_COMP place within 500 mil of ICH9M
SATA-HDD
SATA-ODD
E-SATA
U57A
1 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
D4546 SB use 71.ICH9M.E0U
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
Place within 500 mils of ICH9 ball
62.70001.011
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
D45/D46
PD
Date: Tuesday, March 25, 2008
Sheet 16 of 47




6uA in G3
646mA
1.634A
23mA
48mA
2mA
47mA
1.342A
VCC3_3=308mA
11mA
11mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U57F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
D45/D46
PD
Friday, March 14, 2008
Sheet 18 of 47



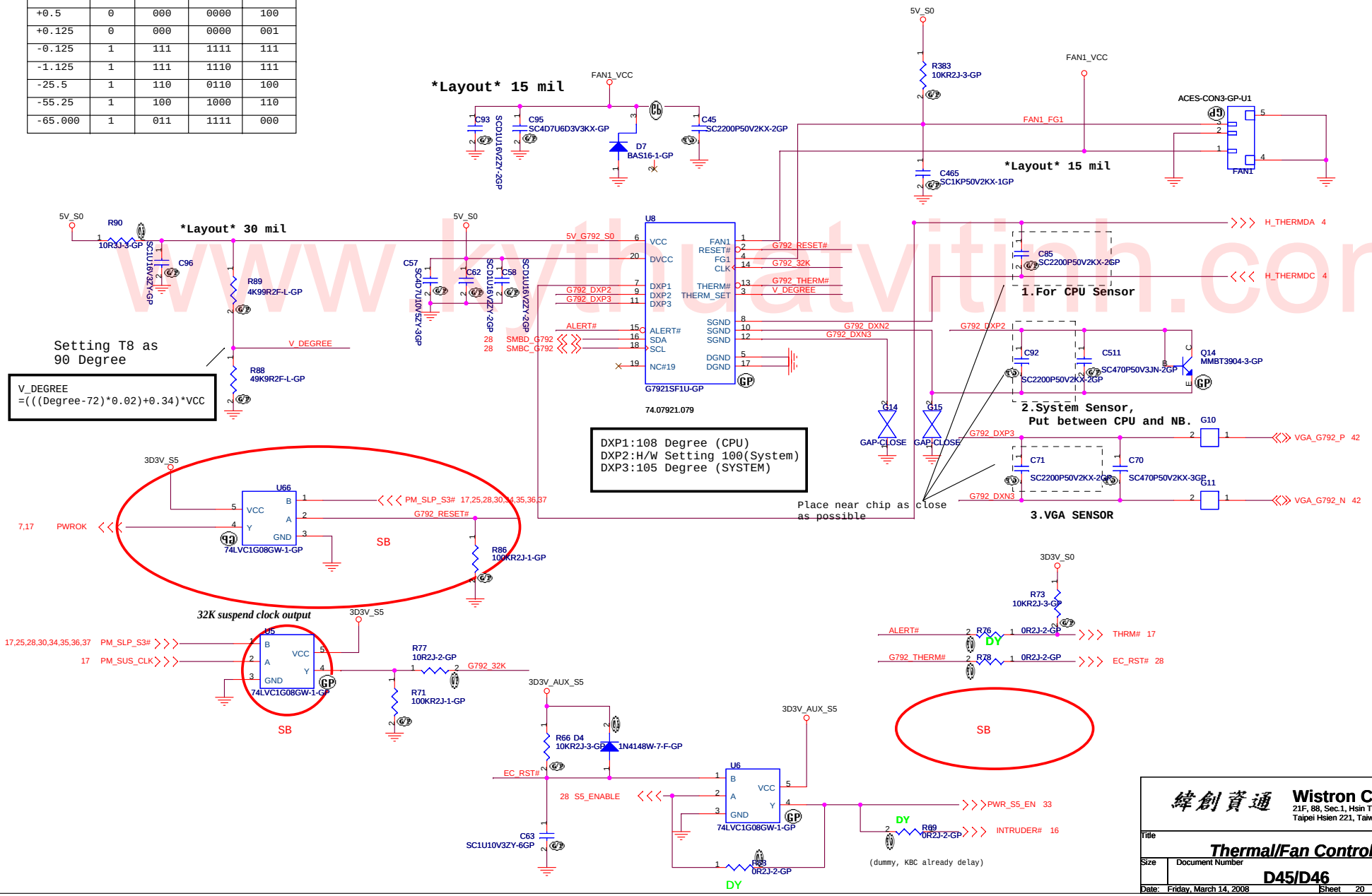


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

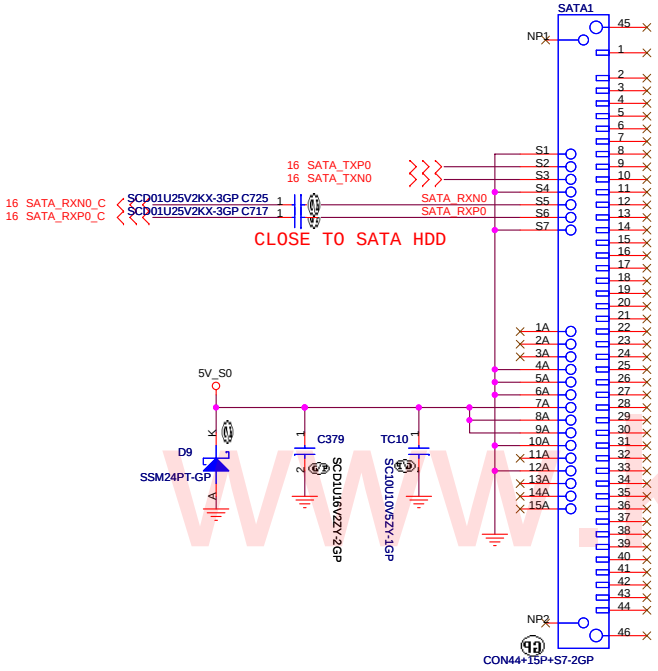
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ICH9-M (4 of 4)		
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 19 of 47	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



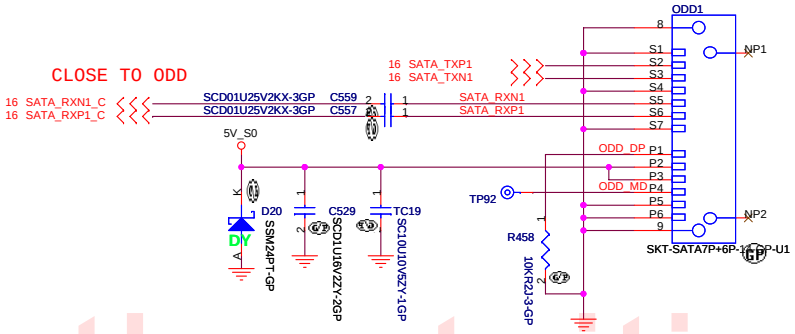
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Thermal/Fan Controllor	
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 20 of 47	

SATA HD Connector

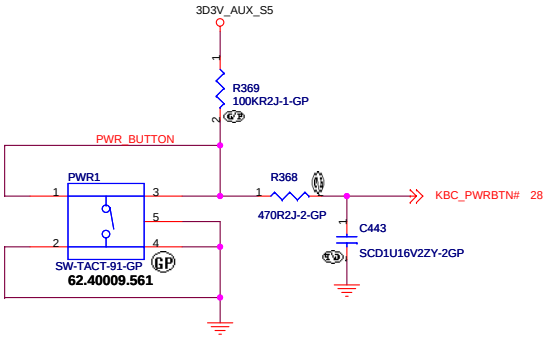


20.F0885.001

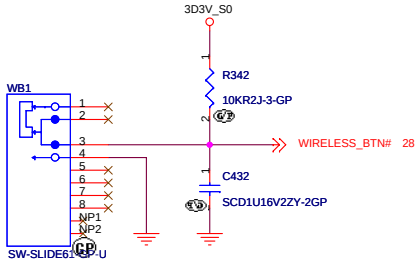
ODD Connector



LAUNCH BUTTON



WIRELESS BUTTON

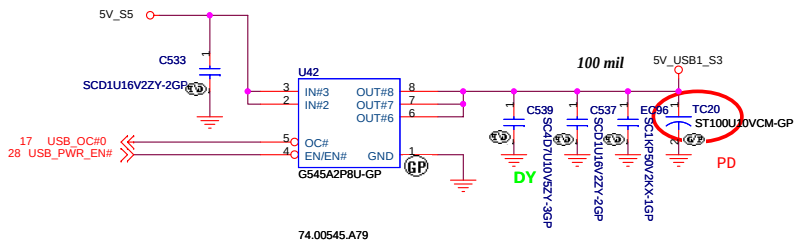


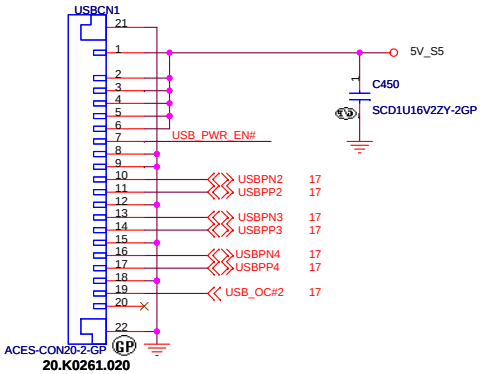
62.40018.351

ZZZZ

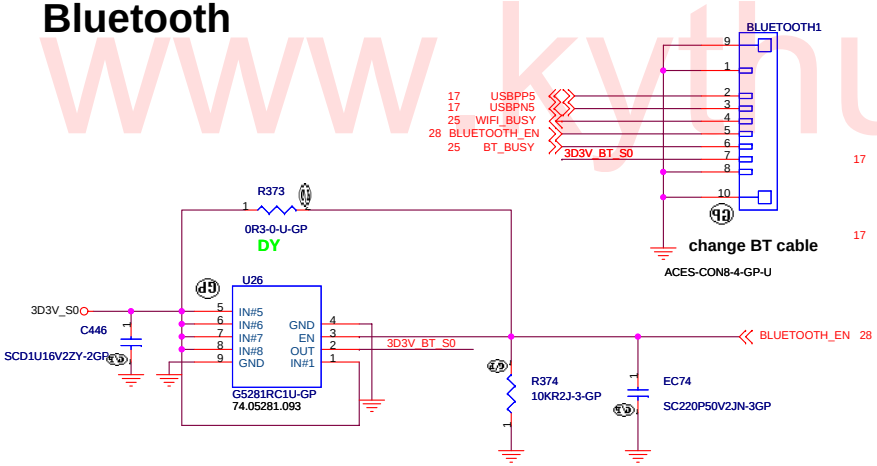
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD / CDROM / LAUNCH	
Size	Document Number D45/D46	Rev PD
Date: Friday, March 14, 2008	Sheet 21 of 47	

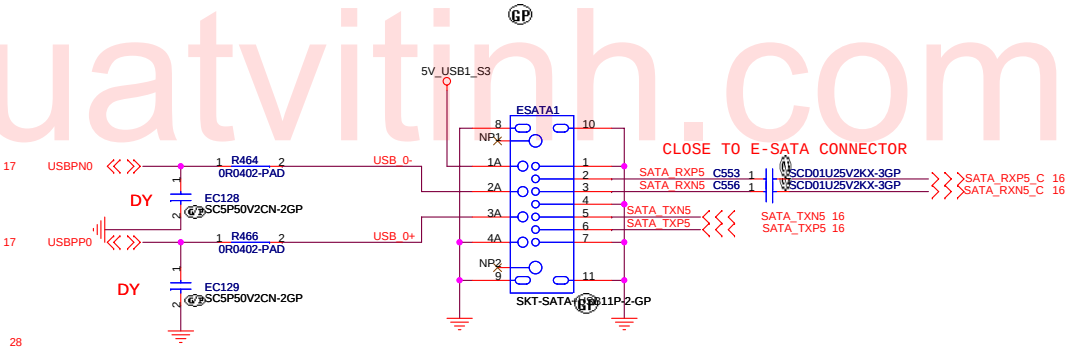
USB BOARD CONN





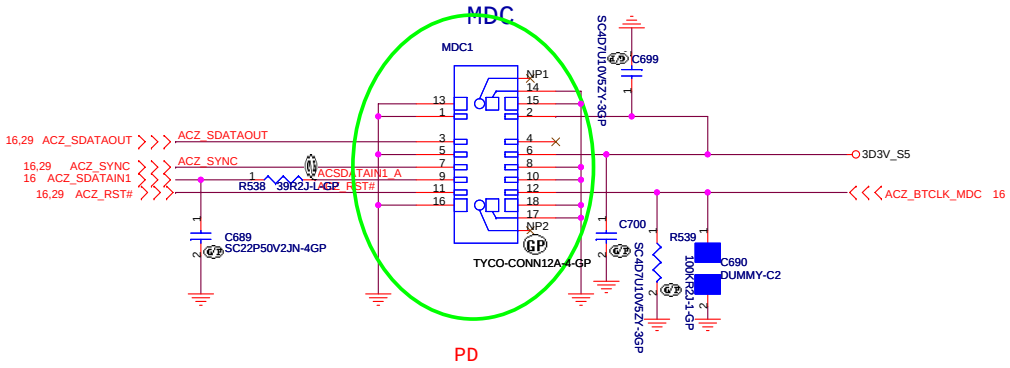
Bluetooth





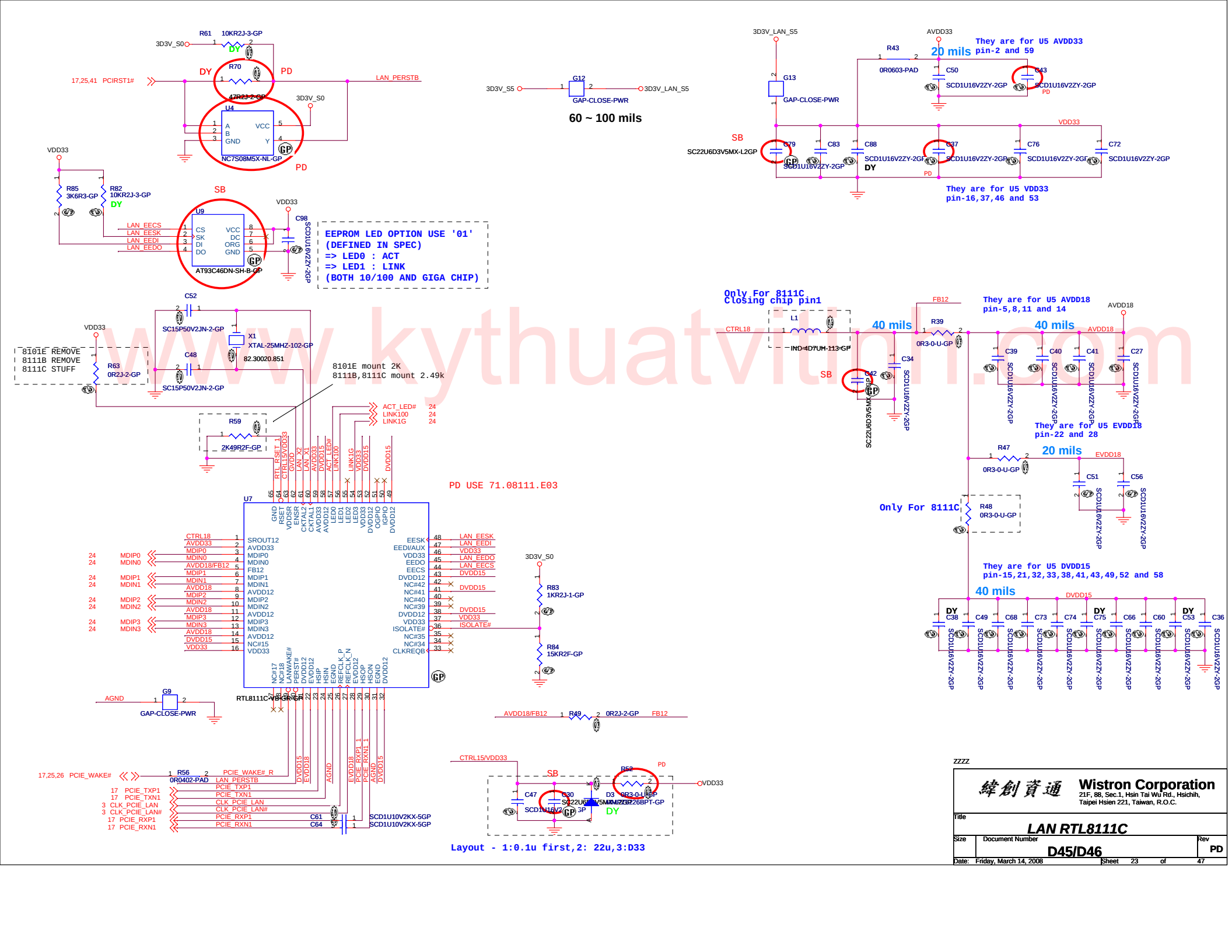
PD USE 22.10218.Z71

eSATA/USB

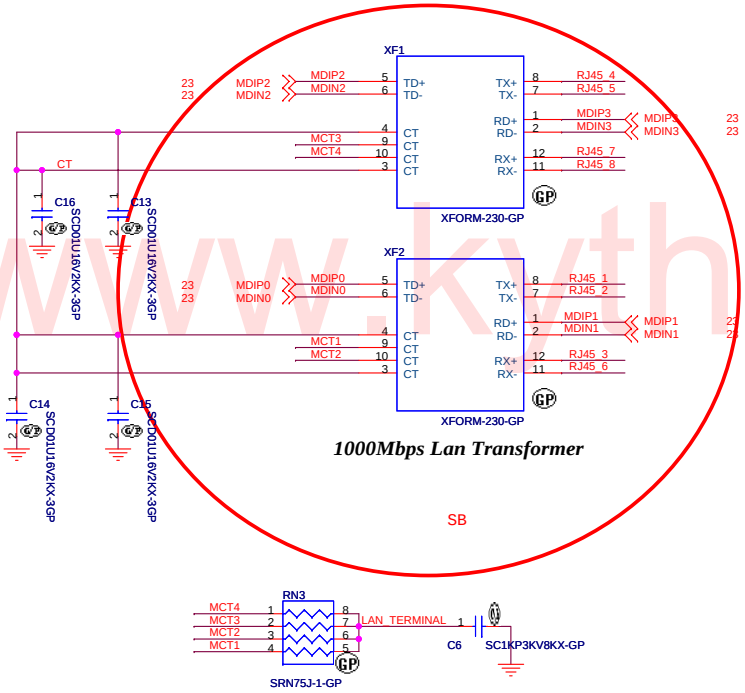


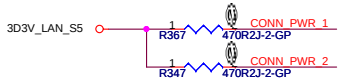
ZZZZ

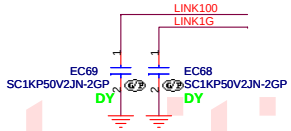
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB / MDC / BLUETOOTH**	
Size	Document Number **D45/D46**	Rev **PD**
Date: Friday, March 14, 2008	Sheet 22 of 47	

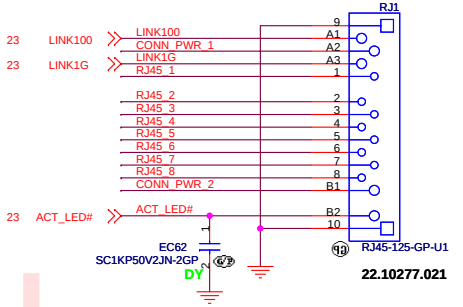


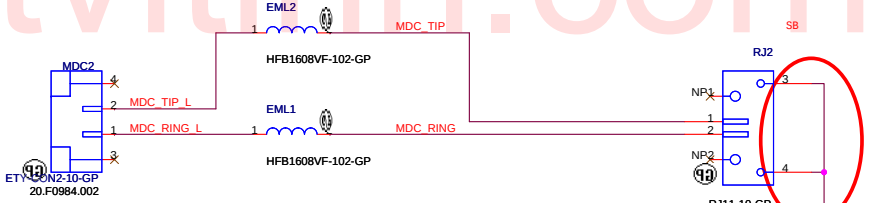
Lan Conn











1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

ZZZZ

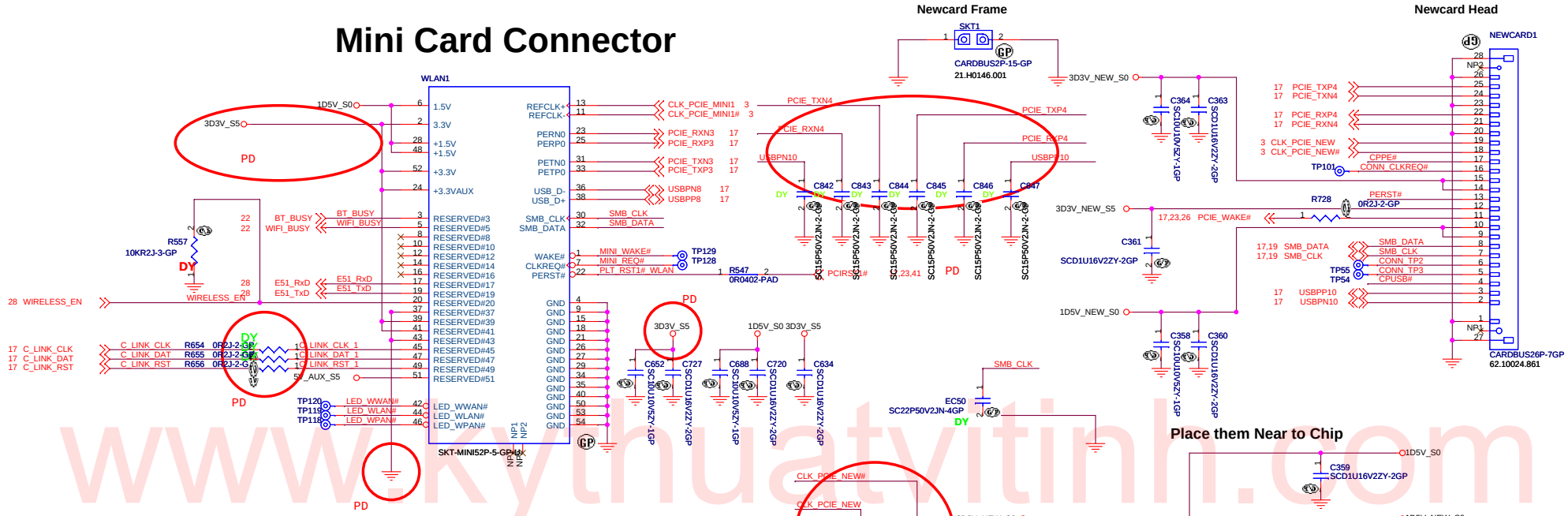
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size | Document Number: **D45/D46** | Rev: **PD**

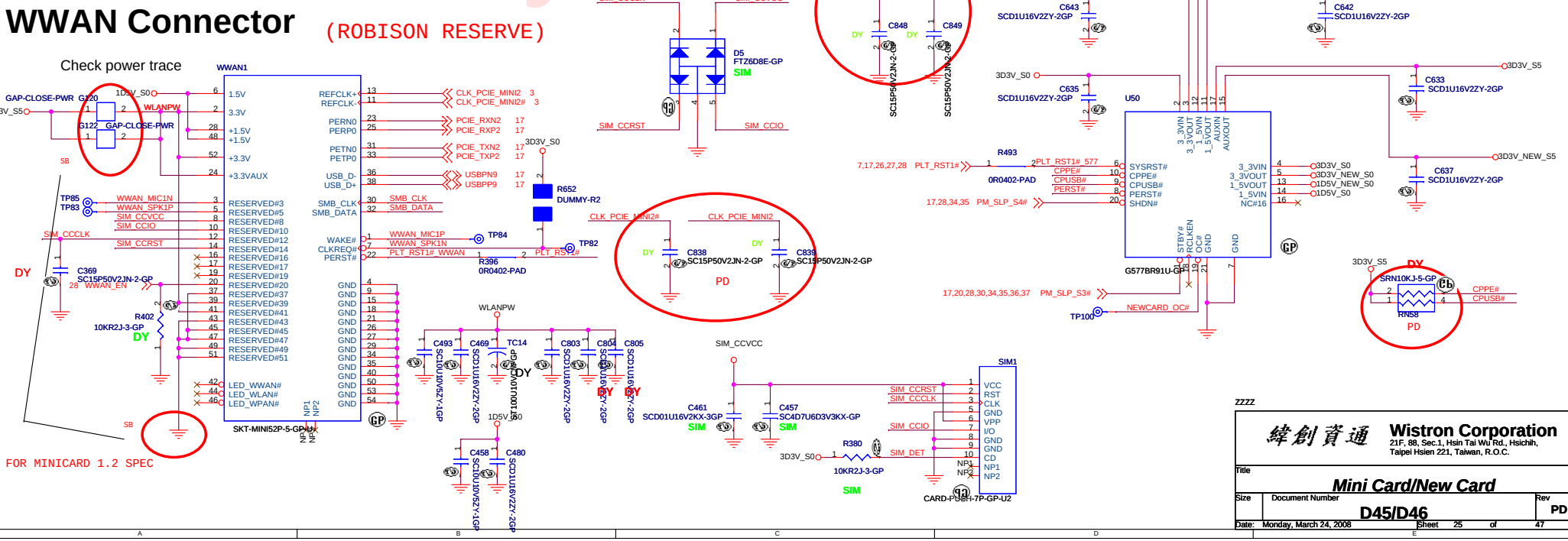
Date: Friday, March 14, 2008 | Sheet 24 of 47

Mini Card Connector

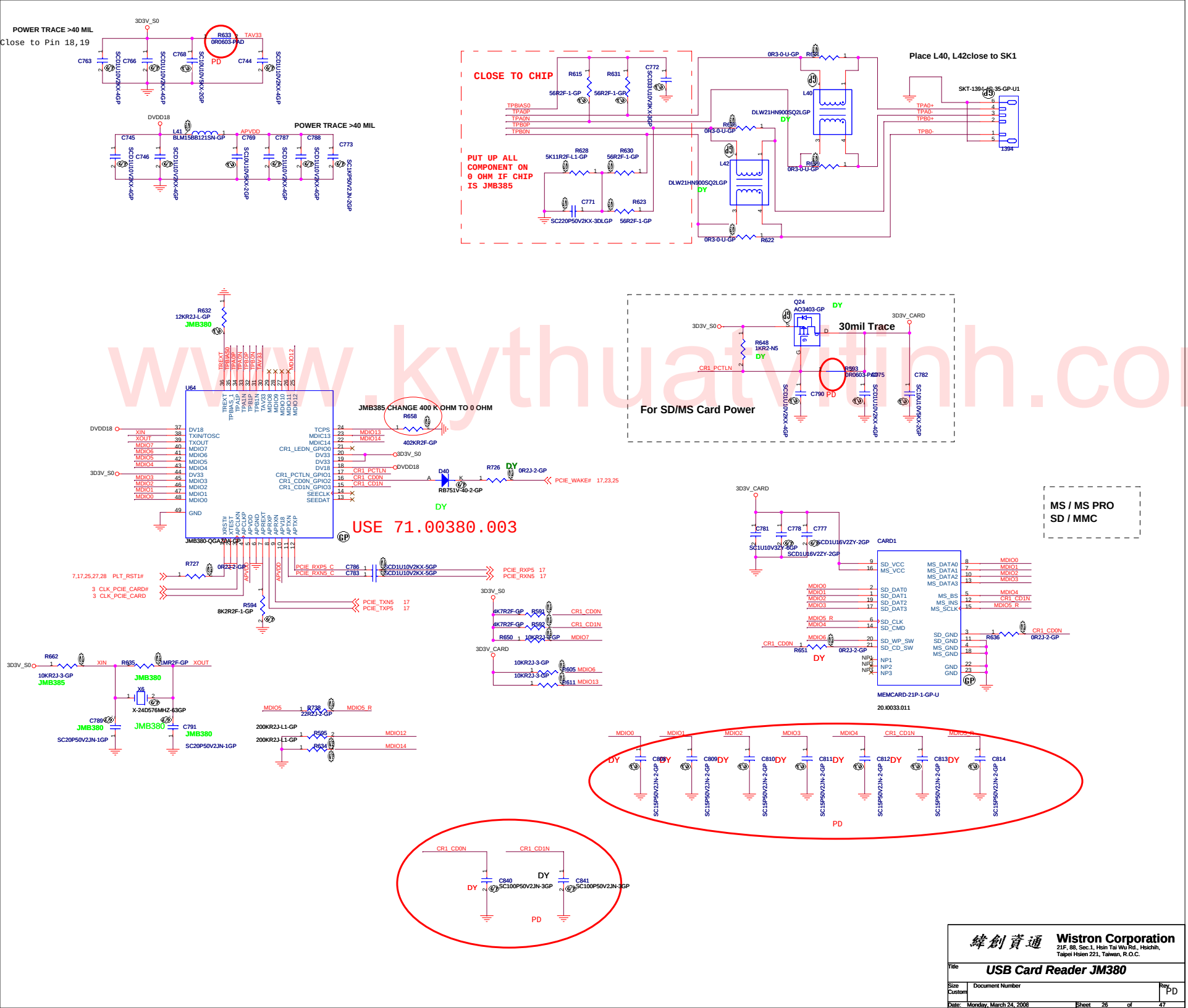


WWAN Connector

(ROBISON RESERVE)

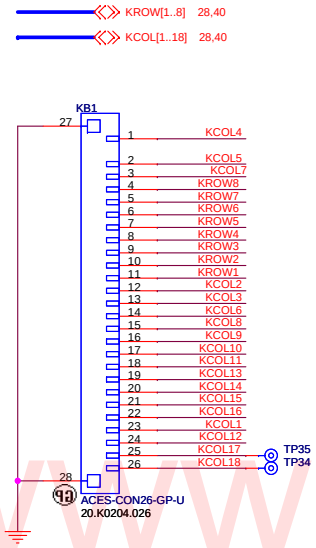


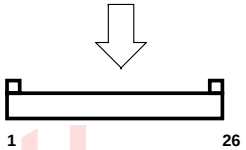
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Mini Card/New Card	
Size	Document Number	Rev
	D45/D46	PD
Date: Monday, March 24, 2008	Sheet 25 of 47	



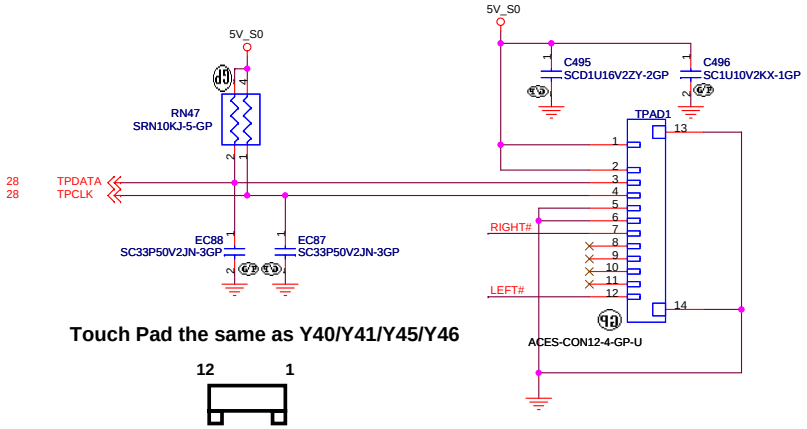
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	USB Card Reader JM380
Size: Custom	Document Number: — Rev: PD
Date: Monday, March 24, 2008	Sheet 26 of 47

Internal KeyBoard Connector



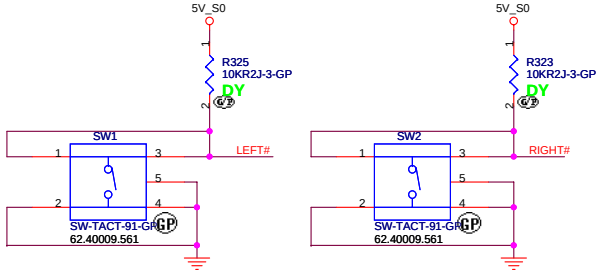


TouchPad Connector

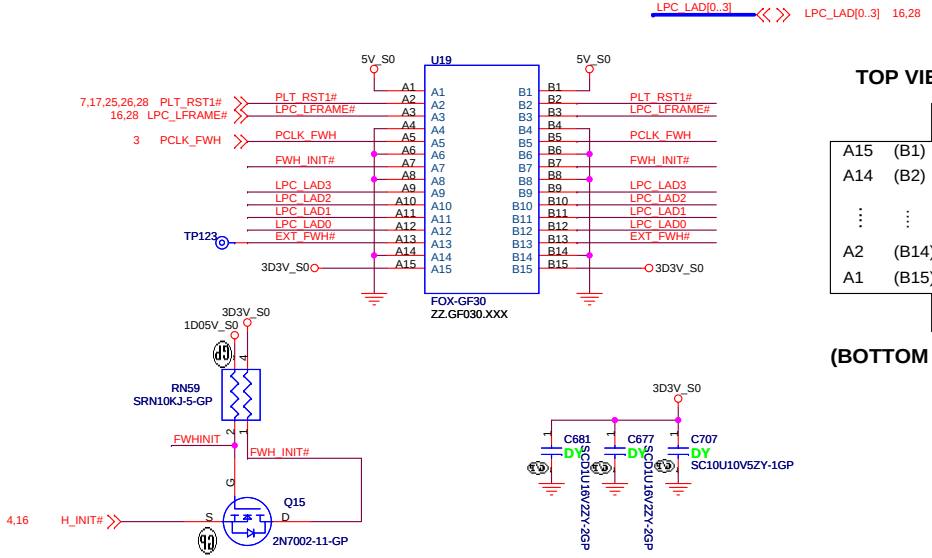


Touch Pad the same as Y40/Y41/Y45/Y46

15" TOUCHPAD BUTTON SWITCH



GOLDEN FINGER FOR DEBUG BOARD

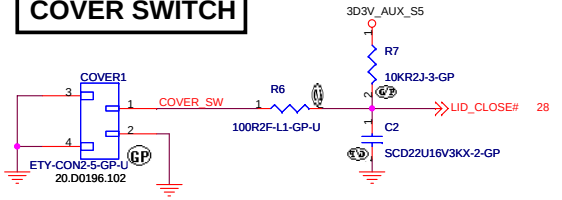


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

COVER SWITCH



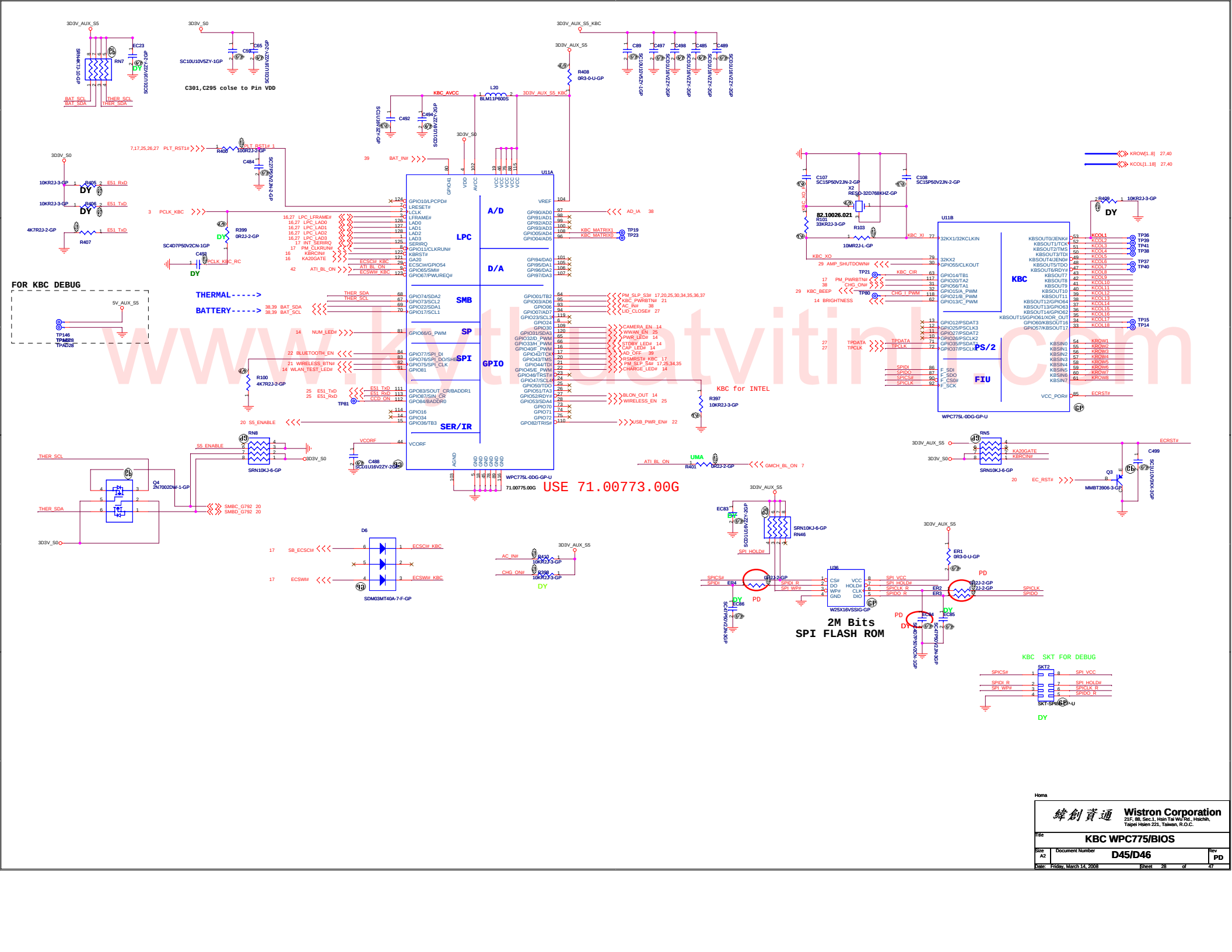
zzzz

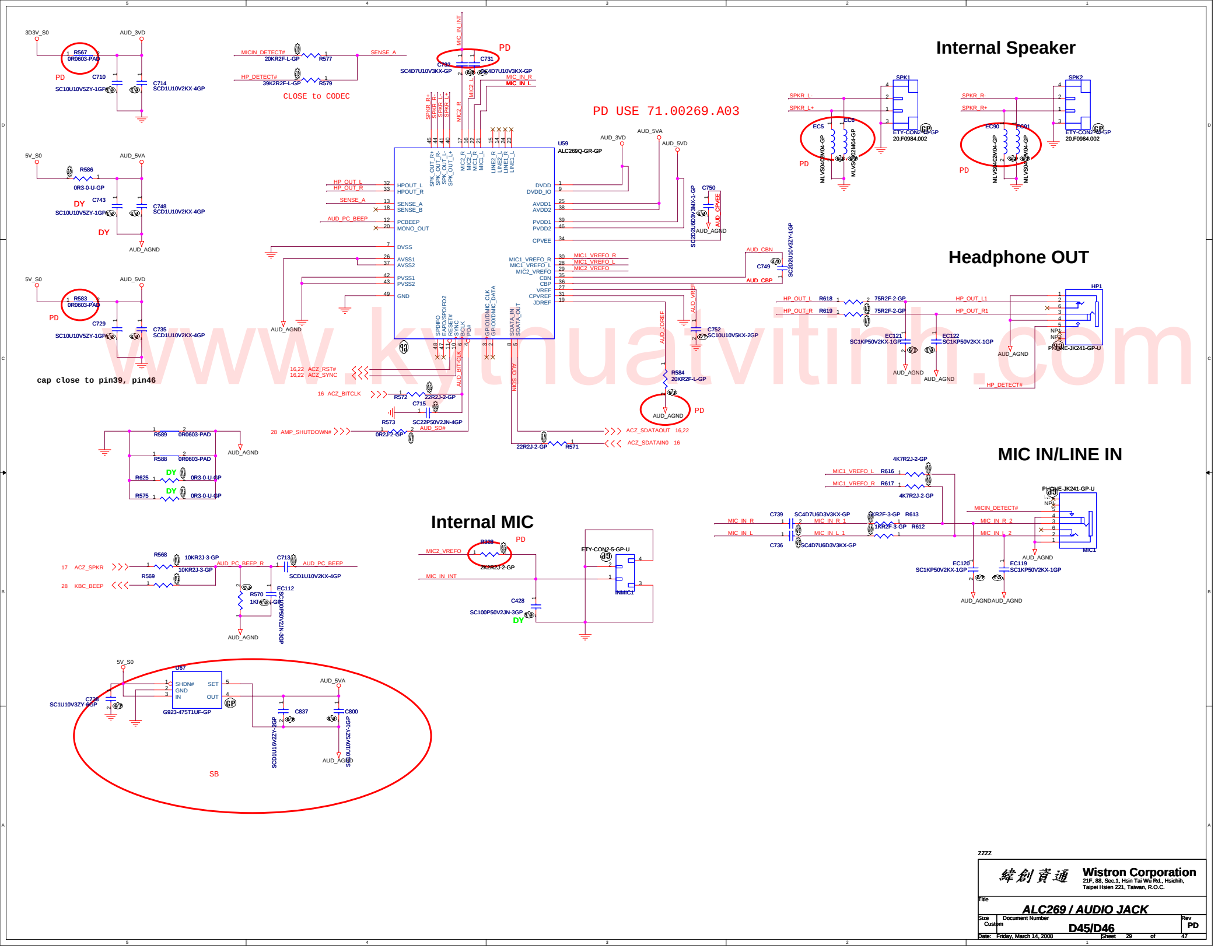
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***KeyBoard/TPAD/Debug***

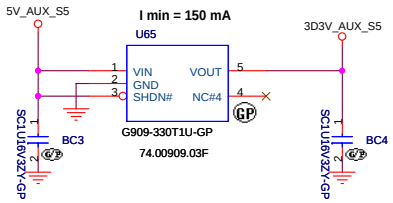
Size	Document Number	Rev
Custom	D45/D46	PD

Date: Tuesday, March 25, 2008 Sheet 27 of 47

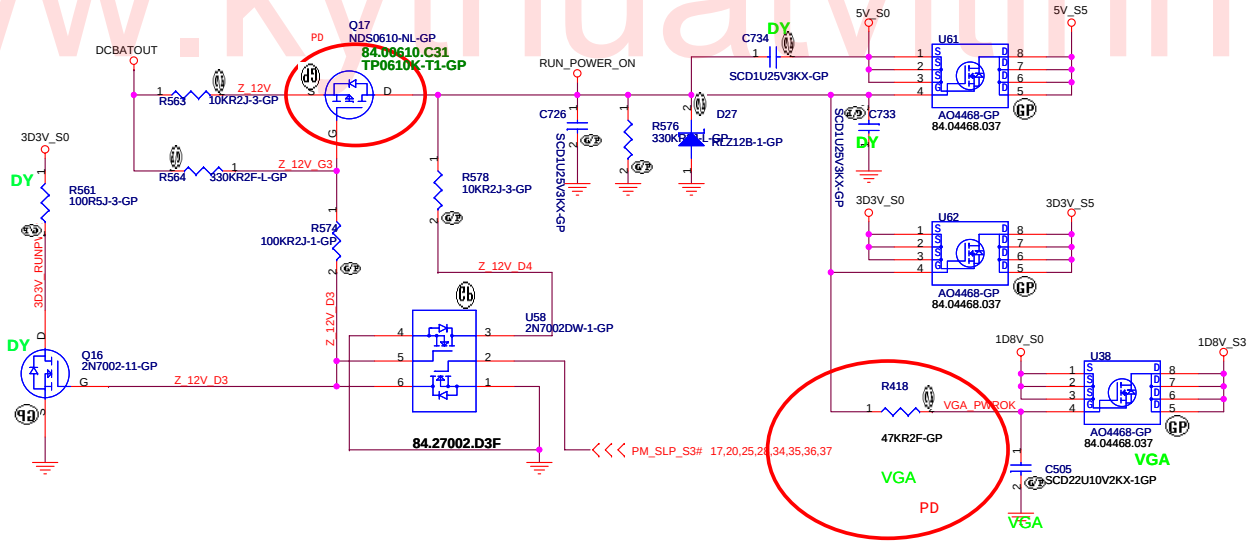

C301,C295 colse to Pin VDD
U11A
WPC775L-0DG-GP-U
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
FOR KBC DEBUG
KBC for INTEL
USE 71.00775.00G
KBC
PS/2
FIU
UMA
2M Bits
SPI FLASH ROM
KBC SKT FOR DEBUG
Wistron Corporation
KBC WPC775/BIOS
D45/D46
PD
Friday, March 14, 2008


Internal Speaker
Headphone OUT
MIC IN/LINE IN
Internal MIC
PD USE 71.00269.A03
CLOSE to CODEC
cap close to pin39, pin46
U59
ALC269Q-GR-GP
SPK1
SPK2
HP1
MIC1
U67
G923-475T1UF-GP
SB
www.kythuatvitinh.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ALC269 / AUDIO JACK
D45/D46
Date: Friday, March 14, 2008
Sheet 29 of 47

Aux Power 3D3V_AUX_S5

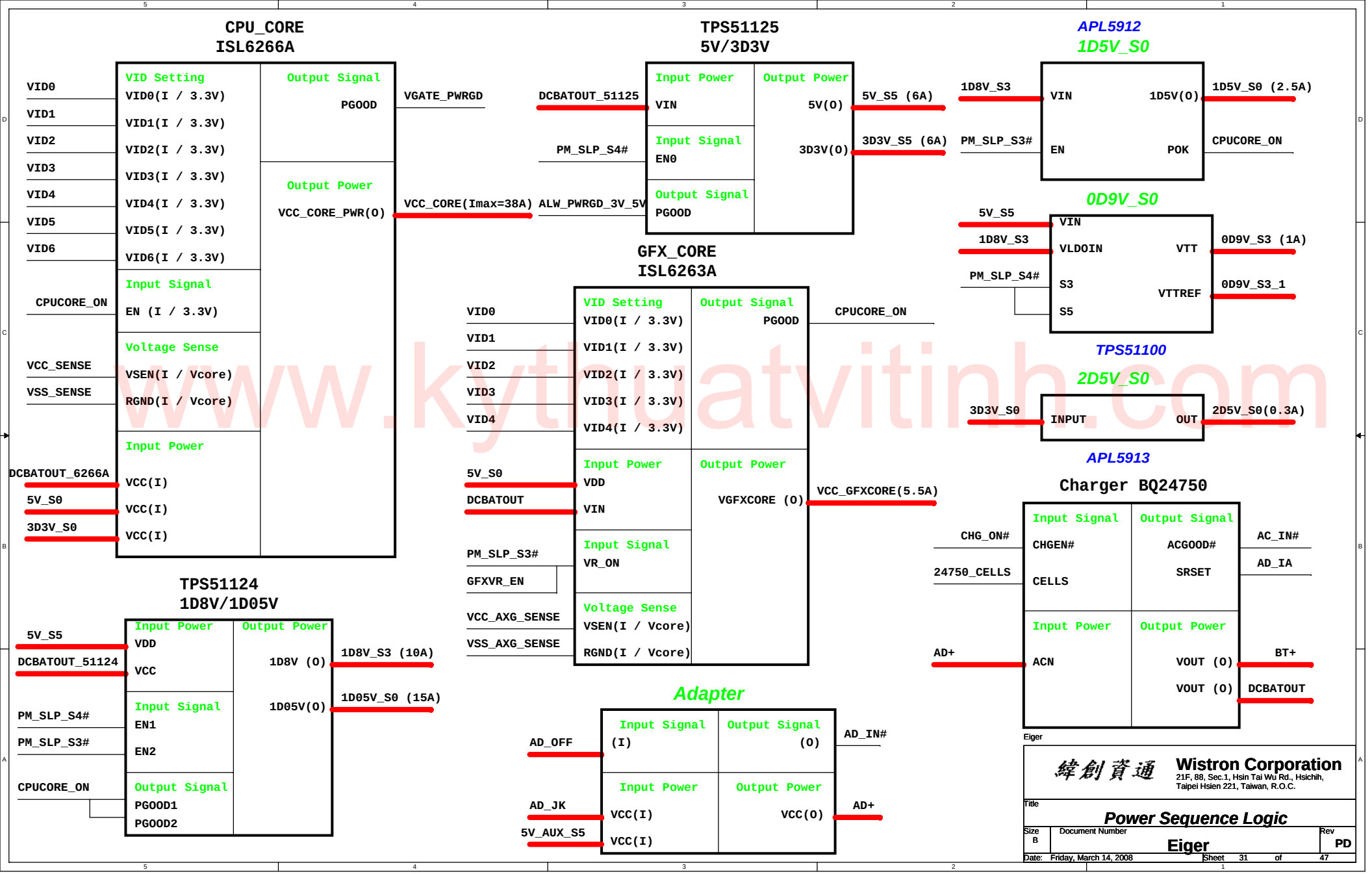


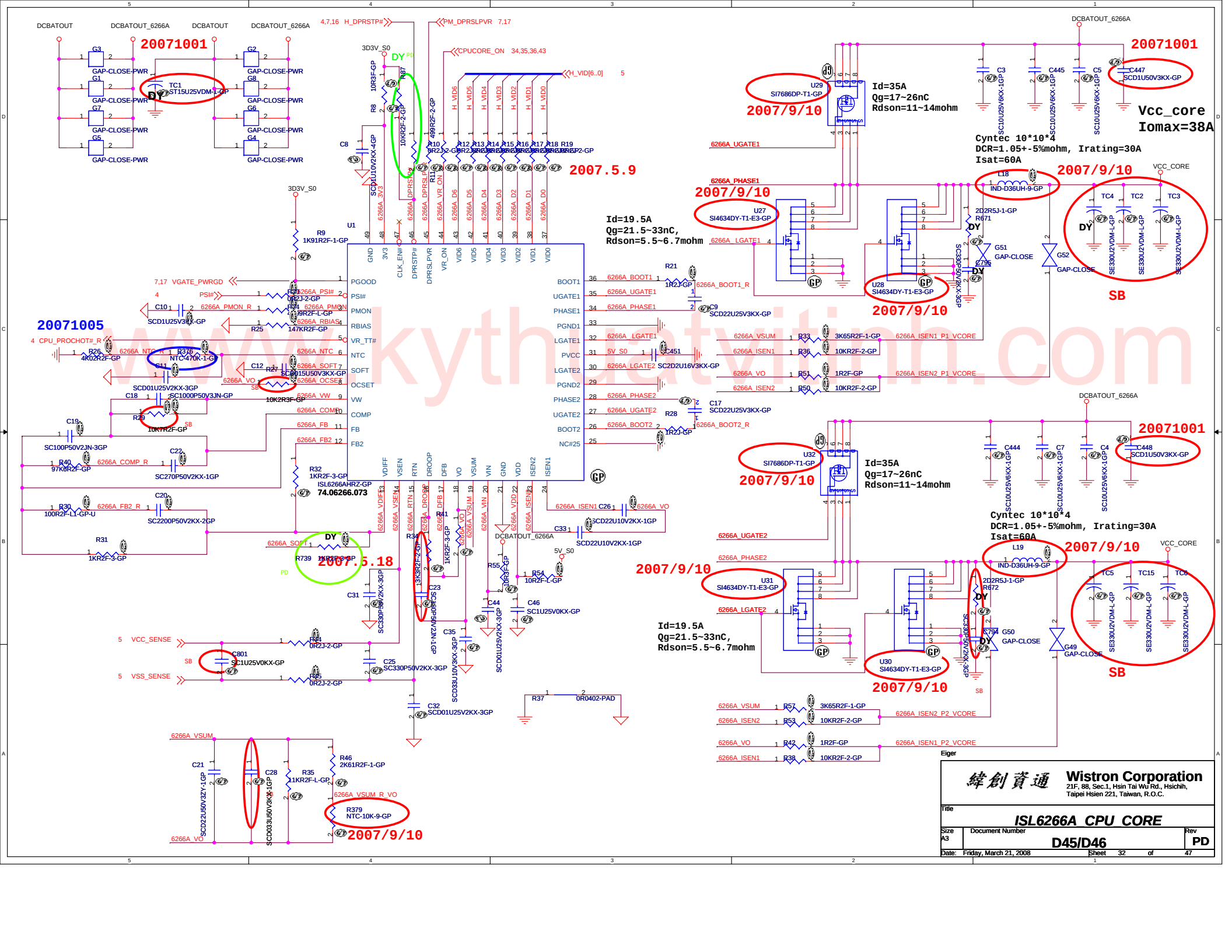
Run Power

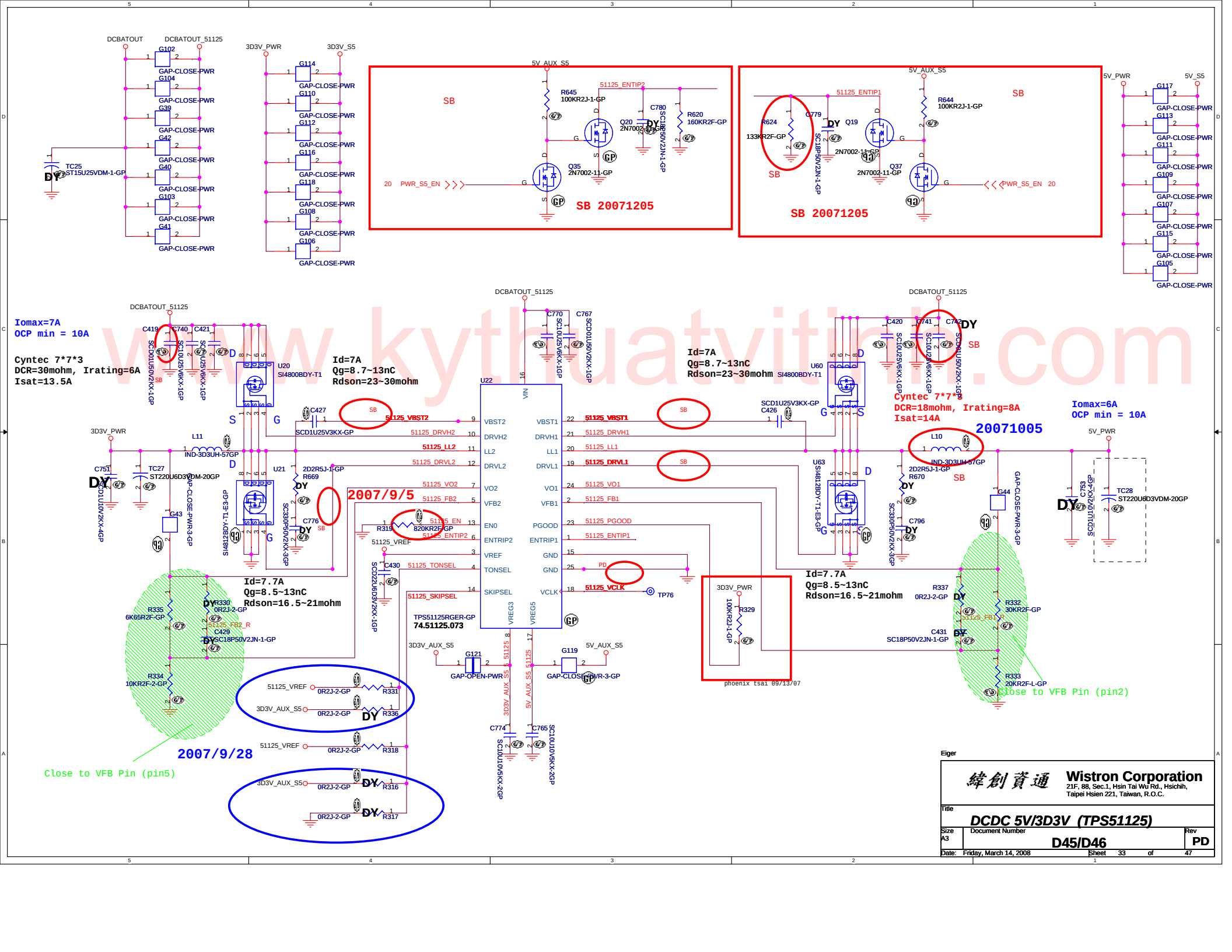


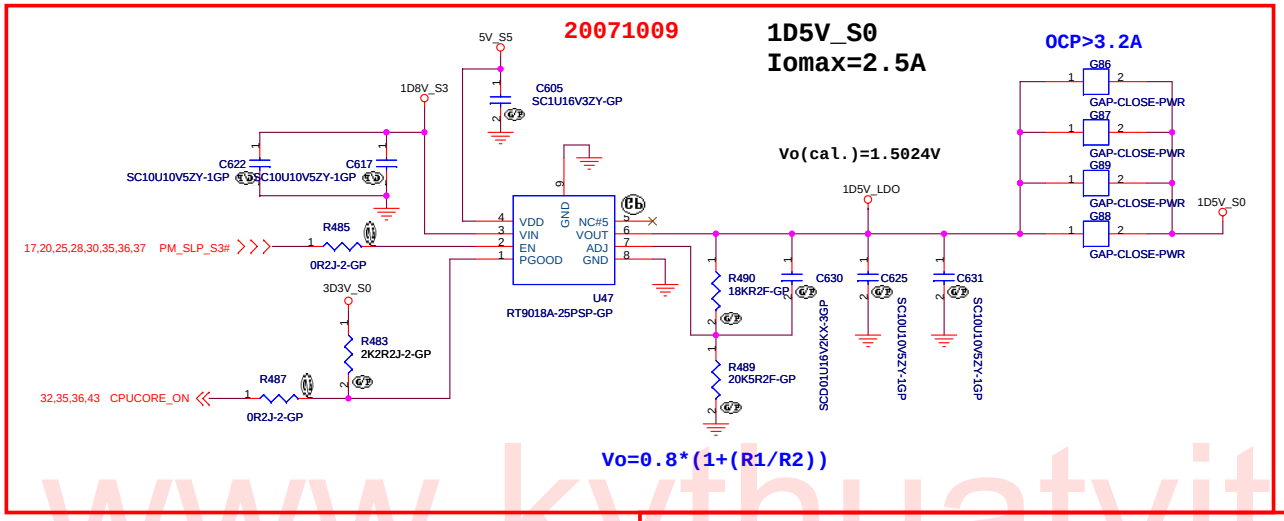
zzzz

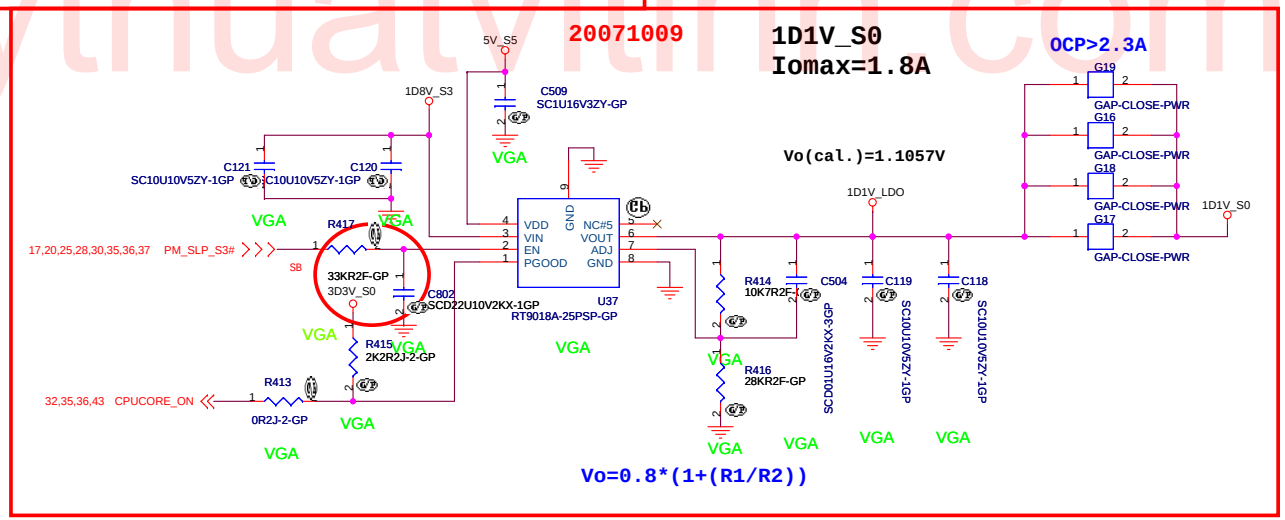
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RUN POWER and 3D3V_AUX_S5*		
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 30 of 47	

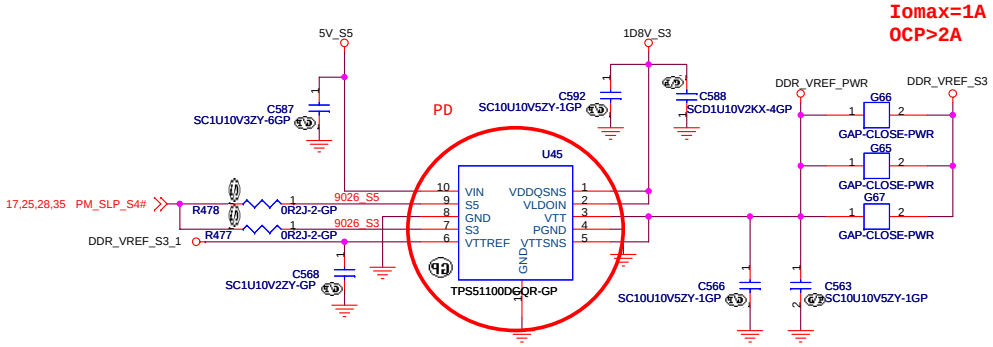



DCBATOUT
DCBATOUT_6266A
20071001
GAP-CLOSE-PWR
TC1
ST15U25VDM-1-GP
DY
3D3V_S0
H_DPRSTP#
PM_DPRSLPVR
CPUCORE_ON
H_VID[6..0]
2007.5.9
U1
ISL6266AHRZ-GP
74.06266.073
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
20071005
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
2007/9/10
U29
SI7686DP-T1-GP
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
U27
SI4634DY-T1-E3-GP
U28
SI4634DY-T1-E3-GP
U32
SI7686DP-T1-GP
U31
SI4634DY-T1-E3-GP
U30
SI4634DY-T1-E3-GP
SB
2007.5.18
VCC_SENSE
VSS_SENSE
Eiger
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number
D45/D46
Rev PD
Date: Friday, March 21, 2008
Sheet 32 of 47


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
SB
SB 20071205
Iomax=7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Cyntec 7*7*
DCR=18mohm, Irating=8A
Isat=14A
Iomax=6A
OCP min = 10A
20071005
2007/9/5
2007/9/28
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
phoenix tsai 09/13/07
Eiger
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
D45/D46
PD
Friday, March 14, 2008
33
47







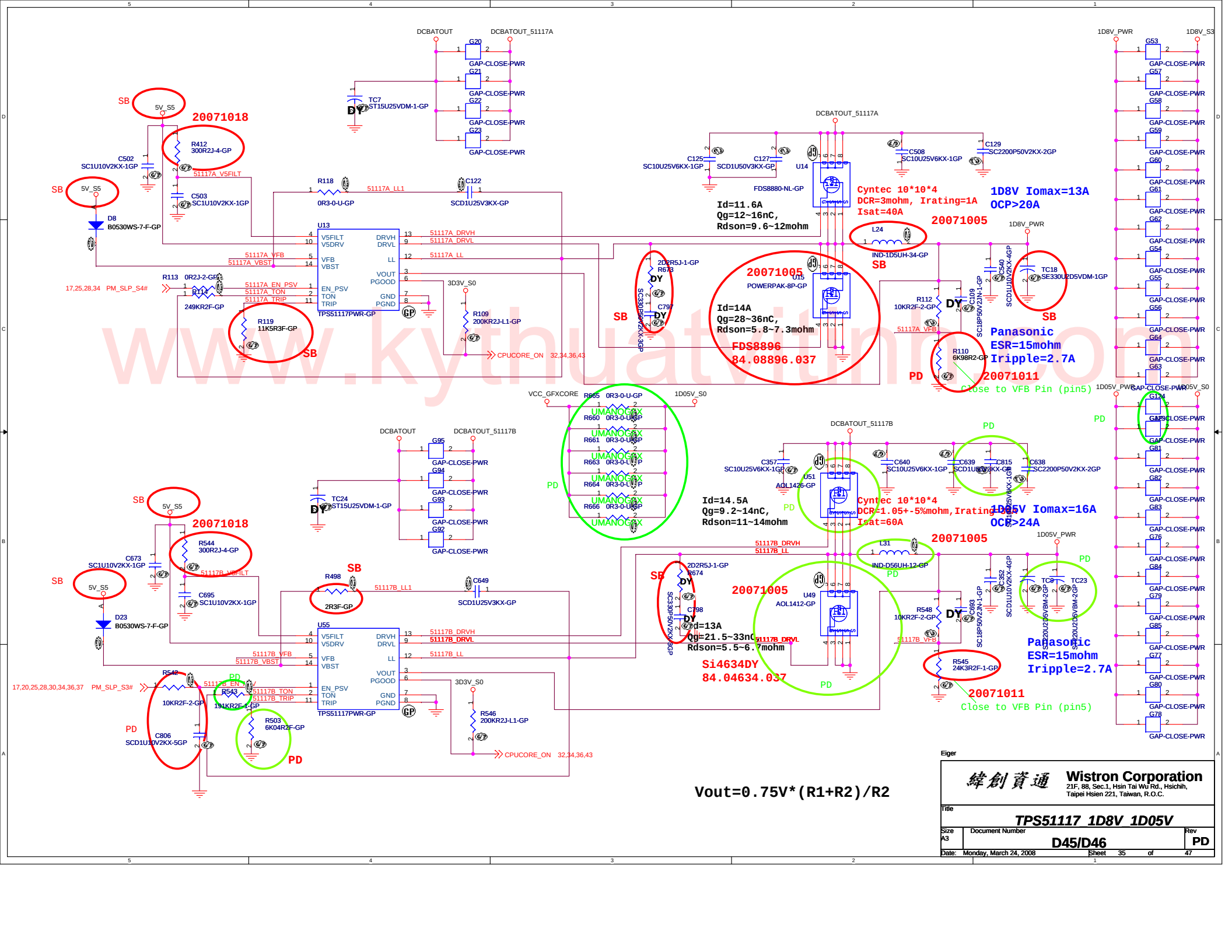
Eiger

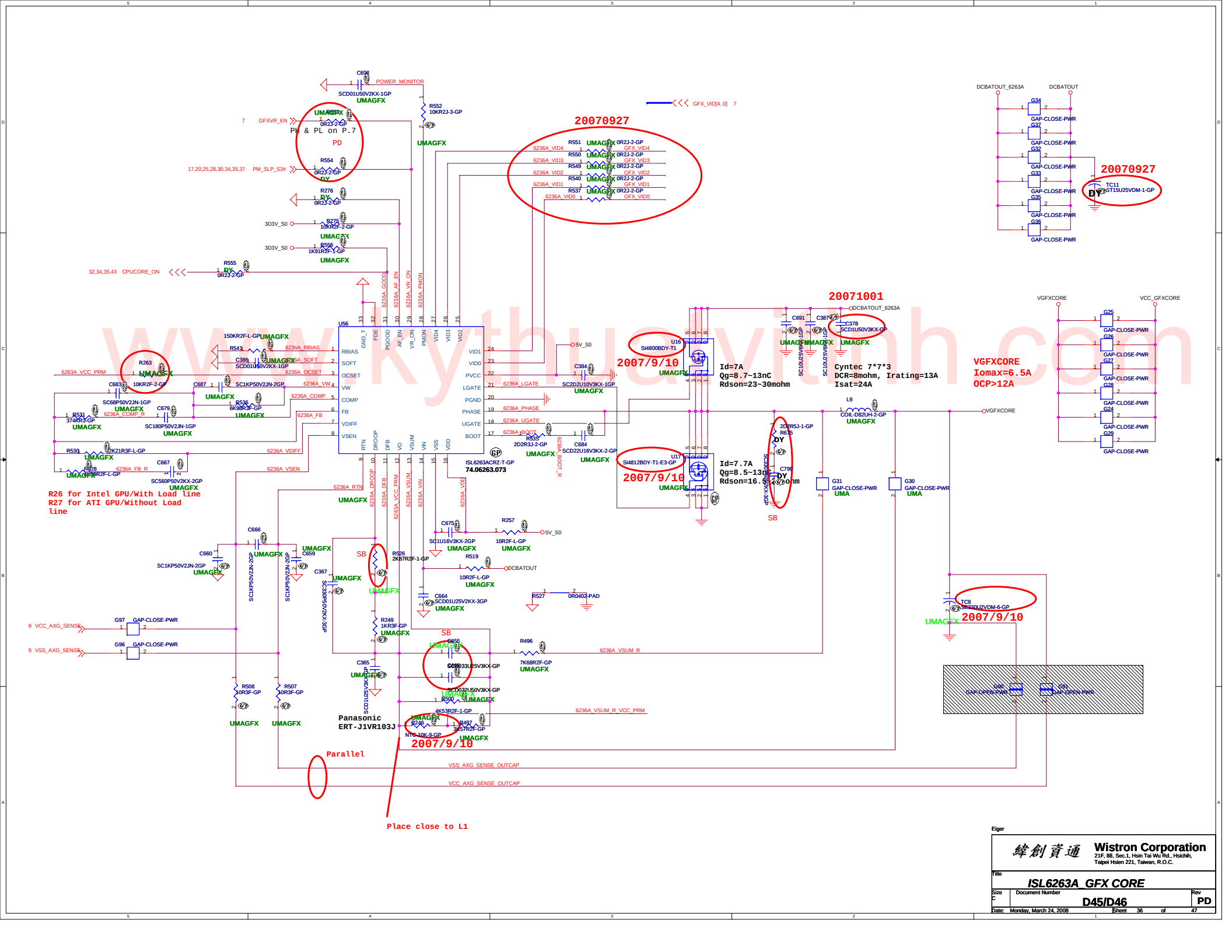
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

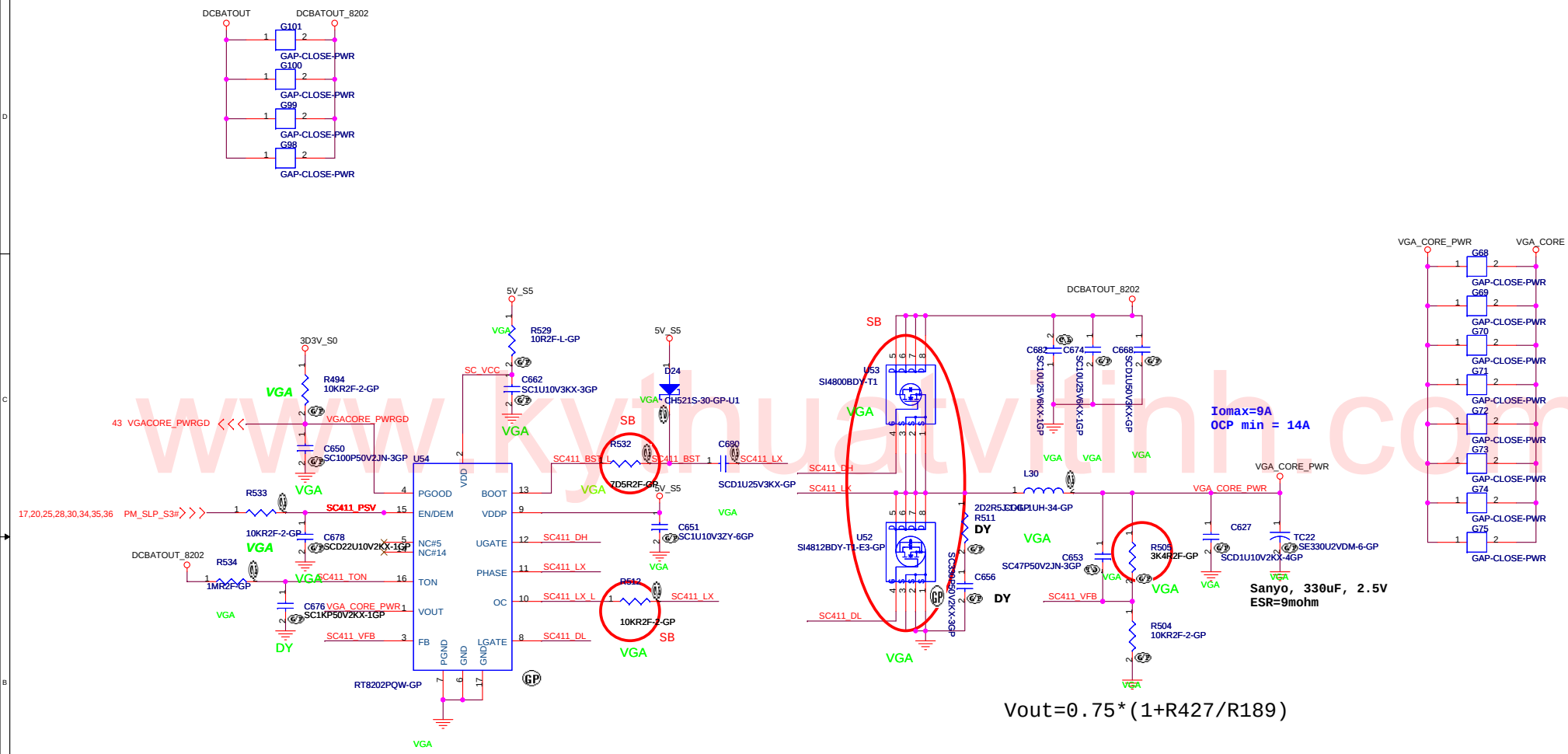
Title: **1D5V & 0D9V**

Size: A3 | Document Number: **D45/D46** | Rev: **PD**

Date: Friday, March 14, 2008 | Sheet 34 of 47




20070927
20071001
2007/9/10
2007/9/10
2007/9/10
U56
ISL6263ACRZ-T-GP
74.06263.073
U16
SI4800BDY-T1
U17
SI4812BDY-T1-E3-GP
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~20mohm
VGFXCORE
Iomax=6.5A
OCP>12A
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L1
SB
PD
DY
UMAGFX
UMA
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
Eiger
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
D45/D46
PD
Monday, March 24, 2008
36
47



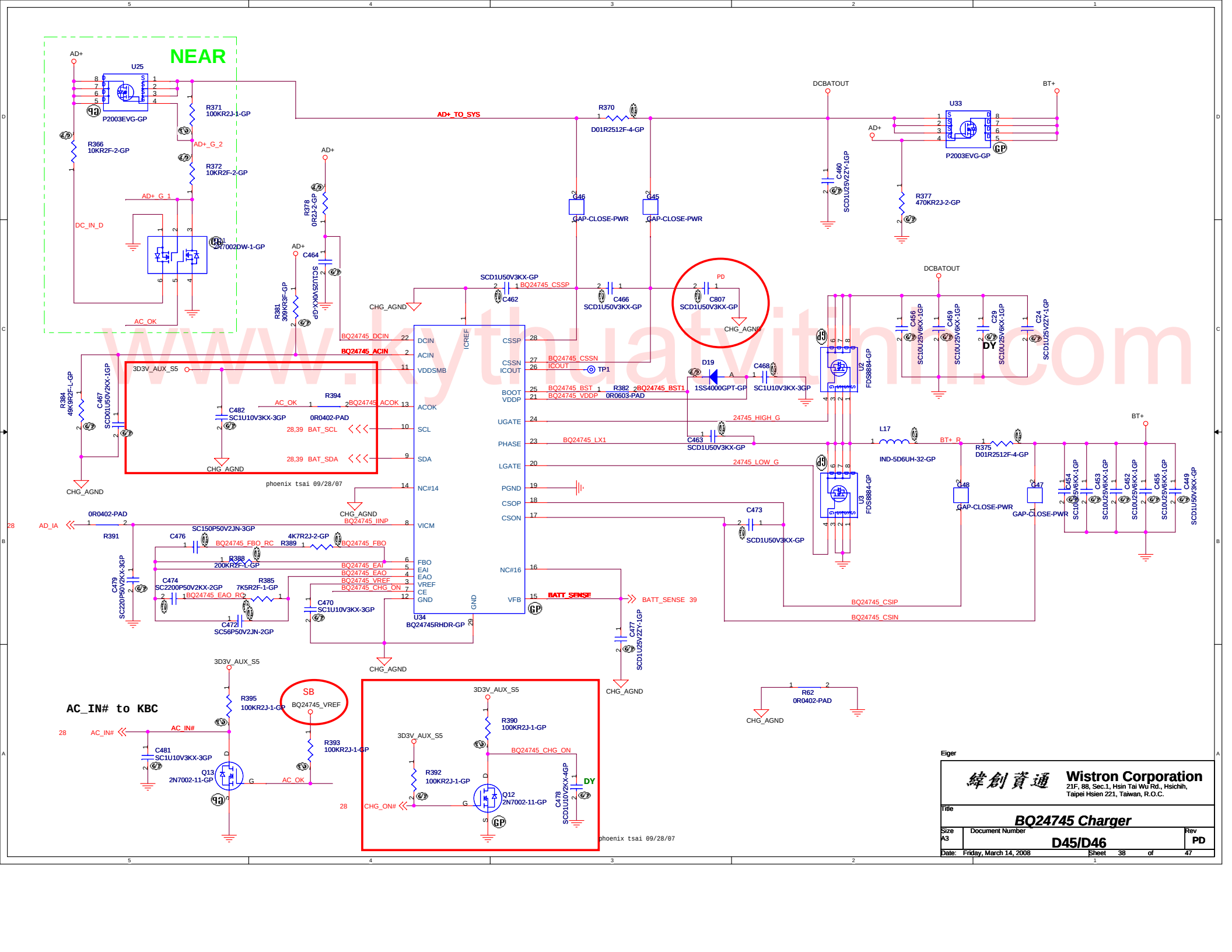
Eiger

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

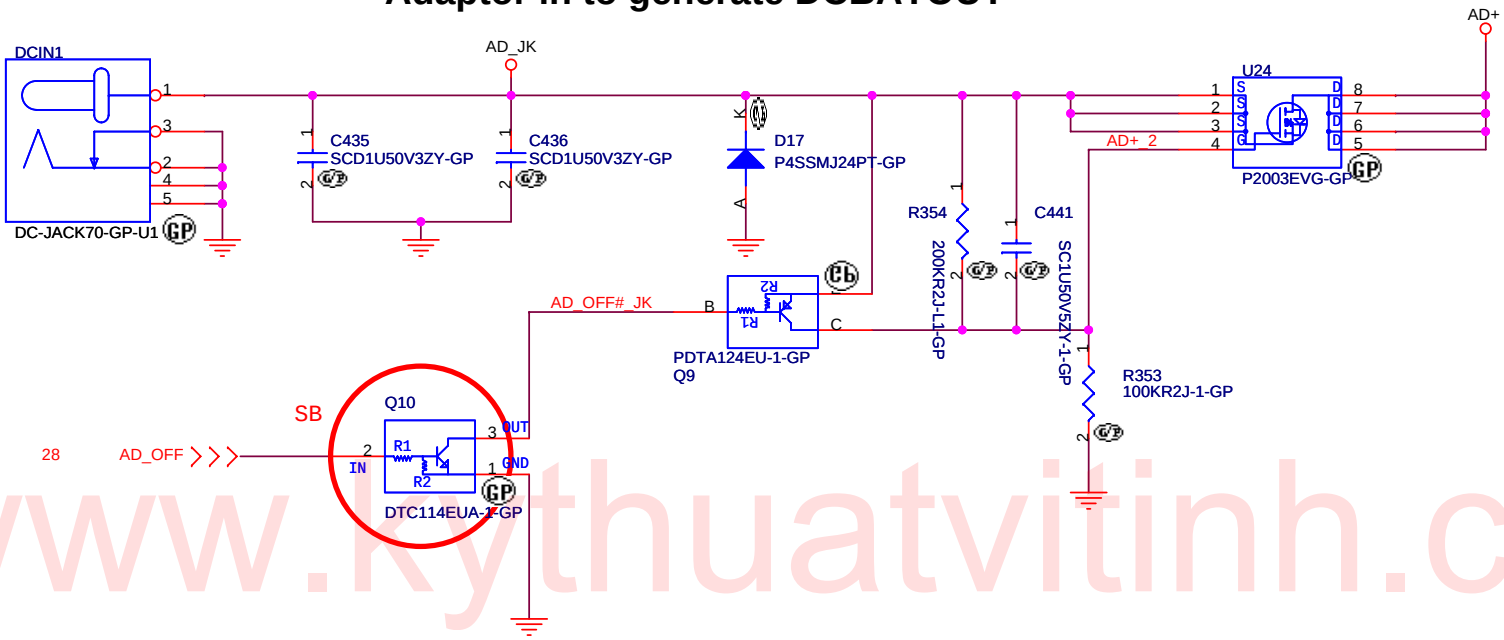
Title: VGA_CORE_S0 (UMA)

Size: A3 | Document Number: D45/D46 | Rev: PD

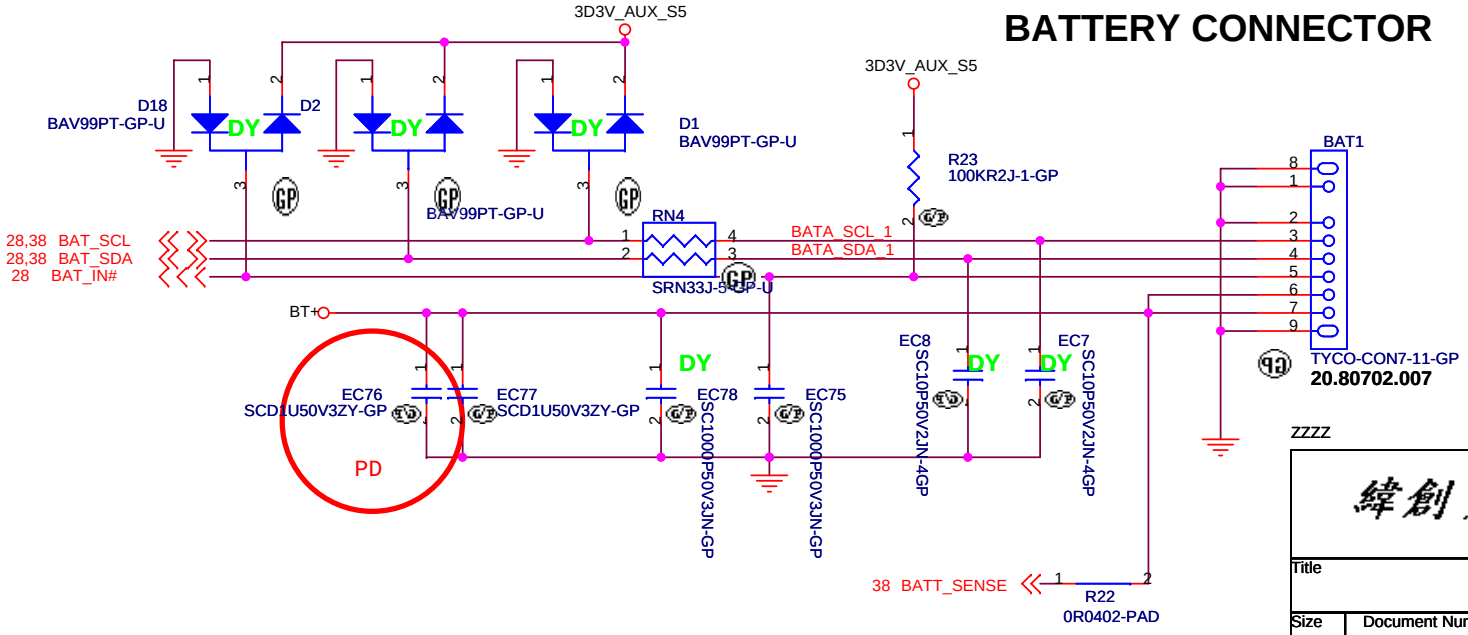
Date: Friday, March 14, 2008 | Sheet 37 of 47



Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

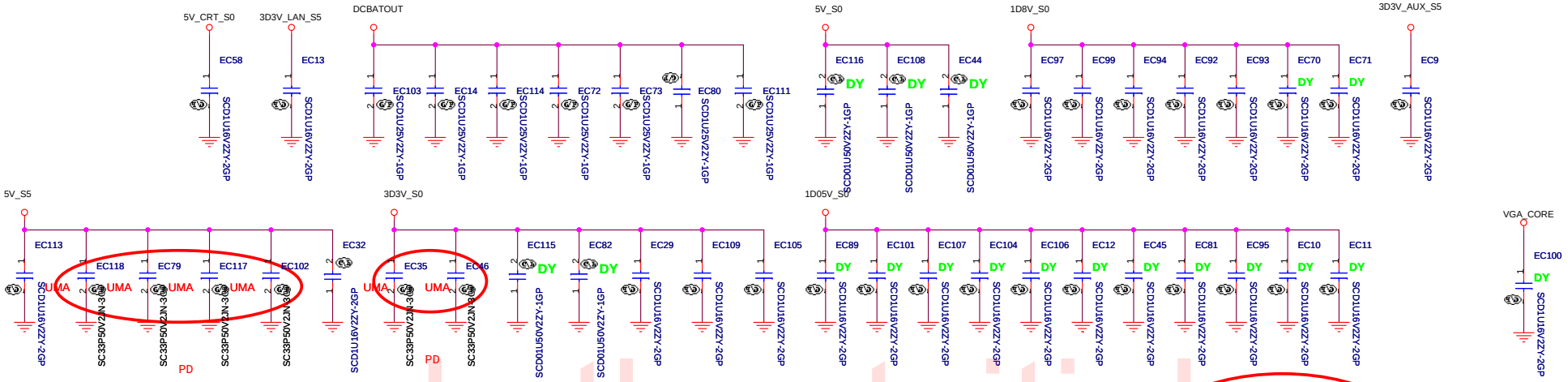


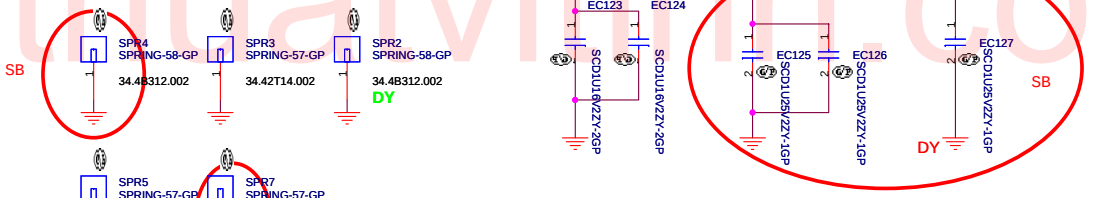
ZZZZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

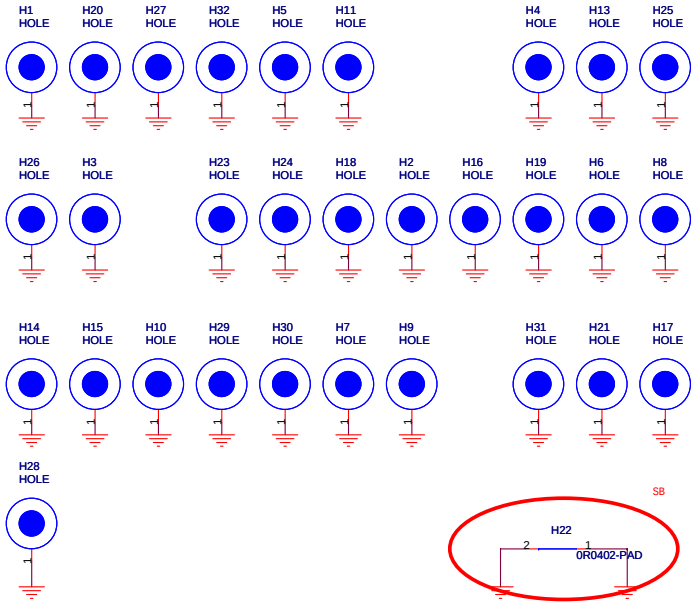
Title	AD/BATT CONN	
Size	Document Number D45/D46	Rev PD
Date: Monday, March 24, 2008	Sheet 39 of 47	

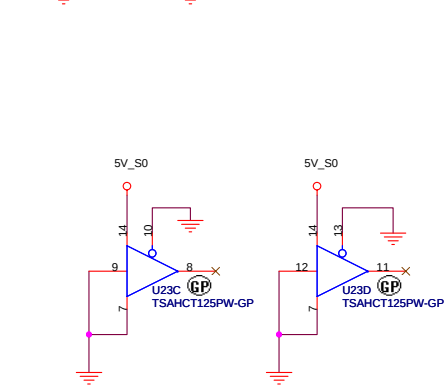
EMI Caps



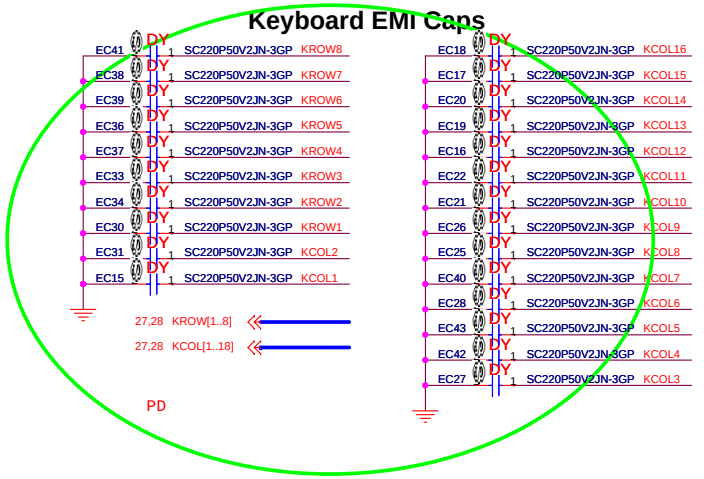


Holes

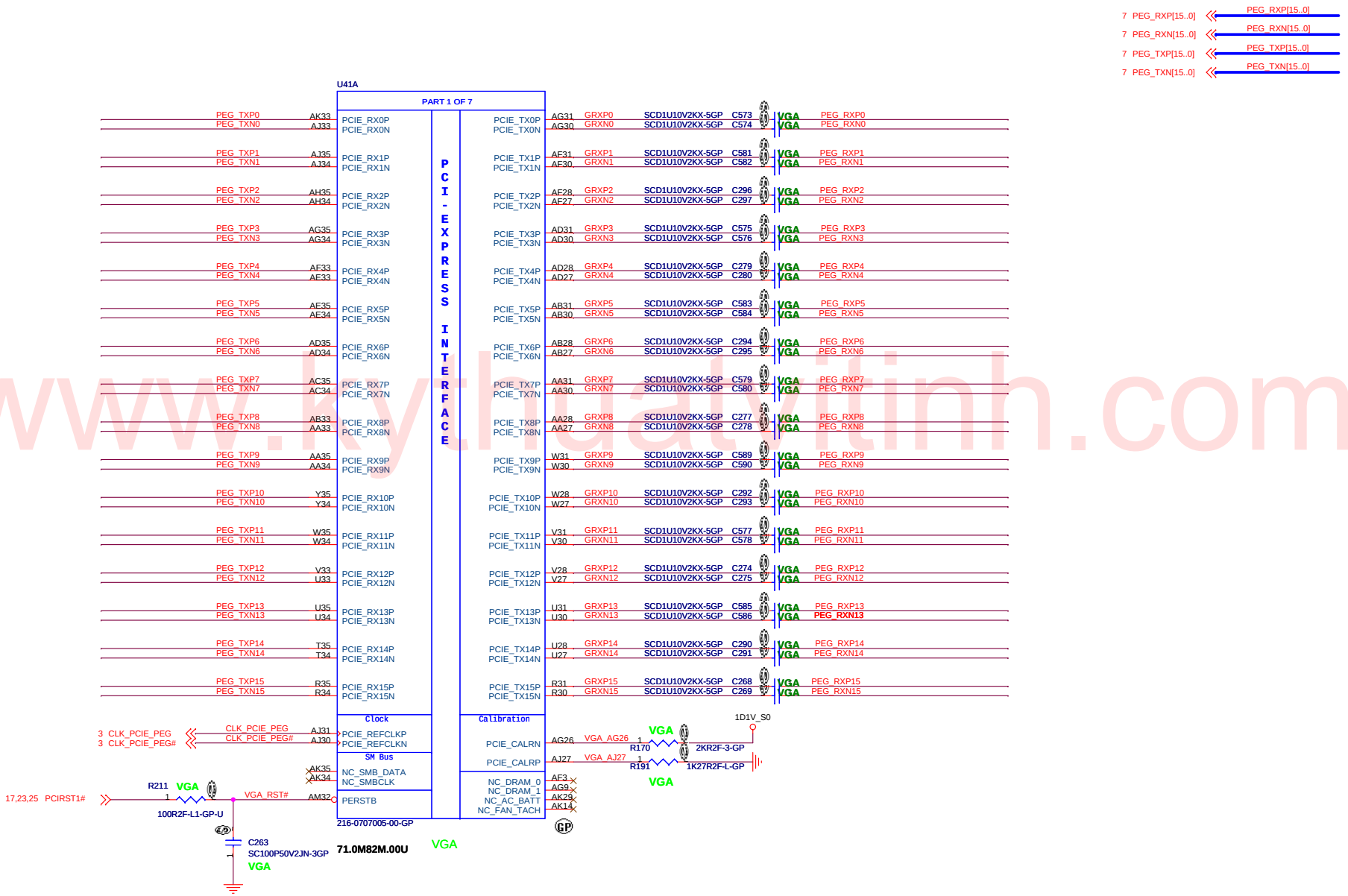




Keyboard EMI Caps

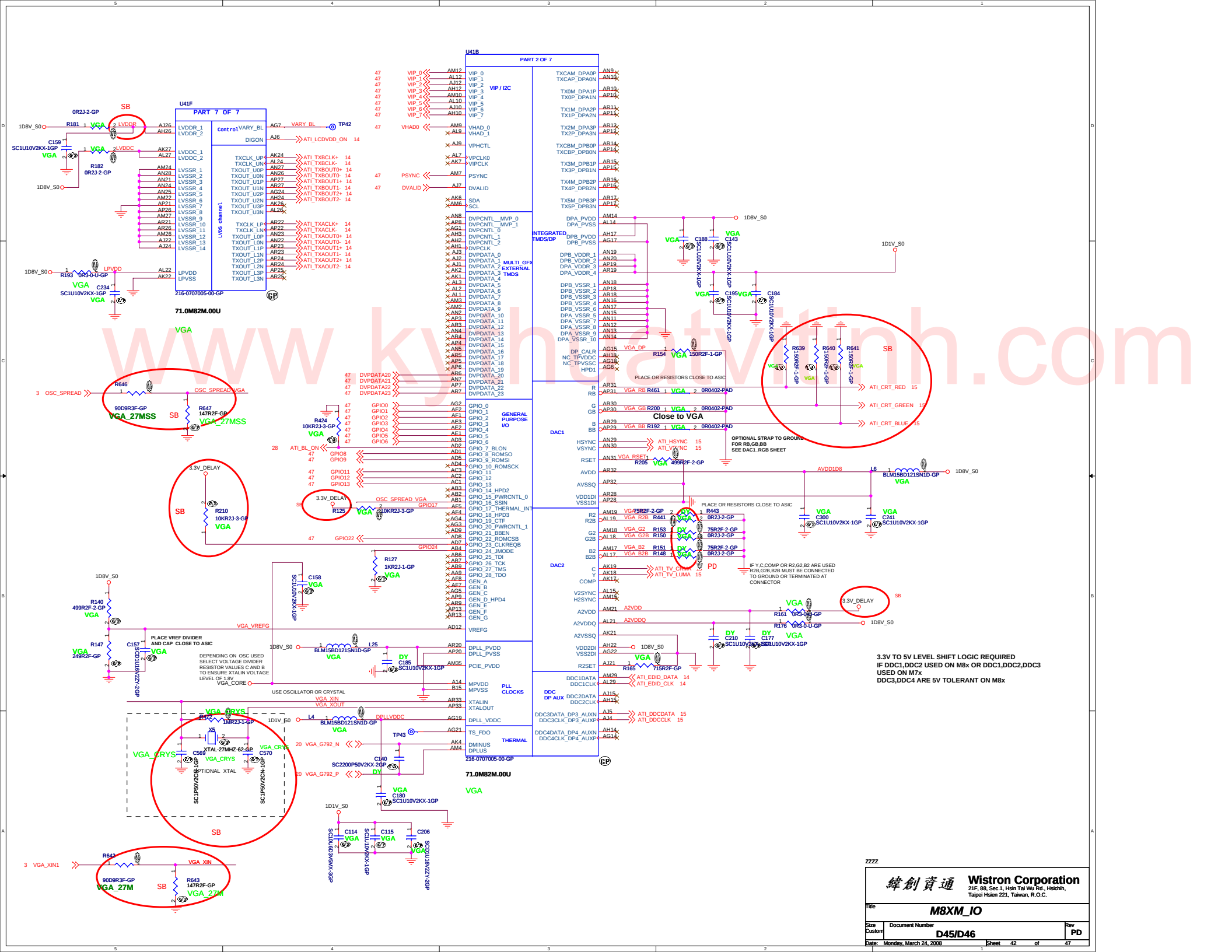


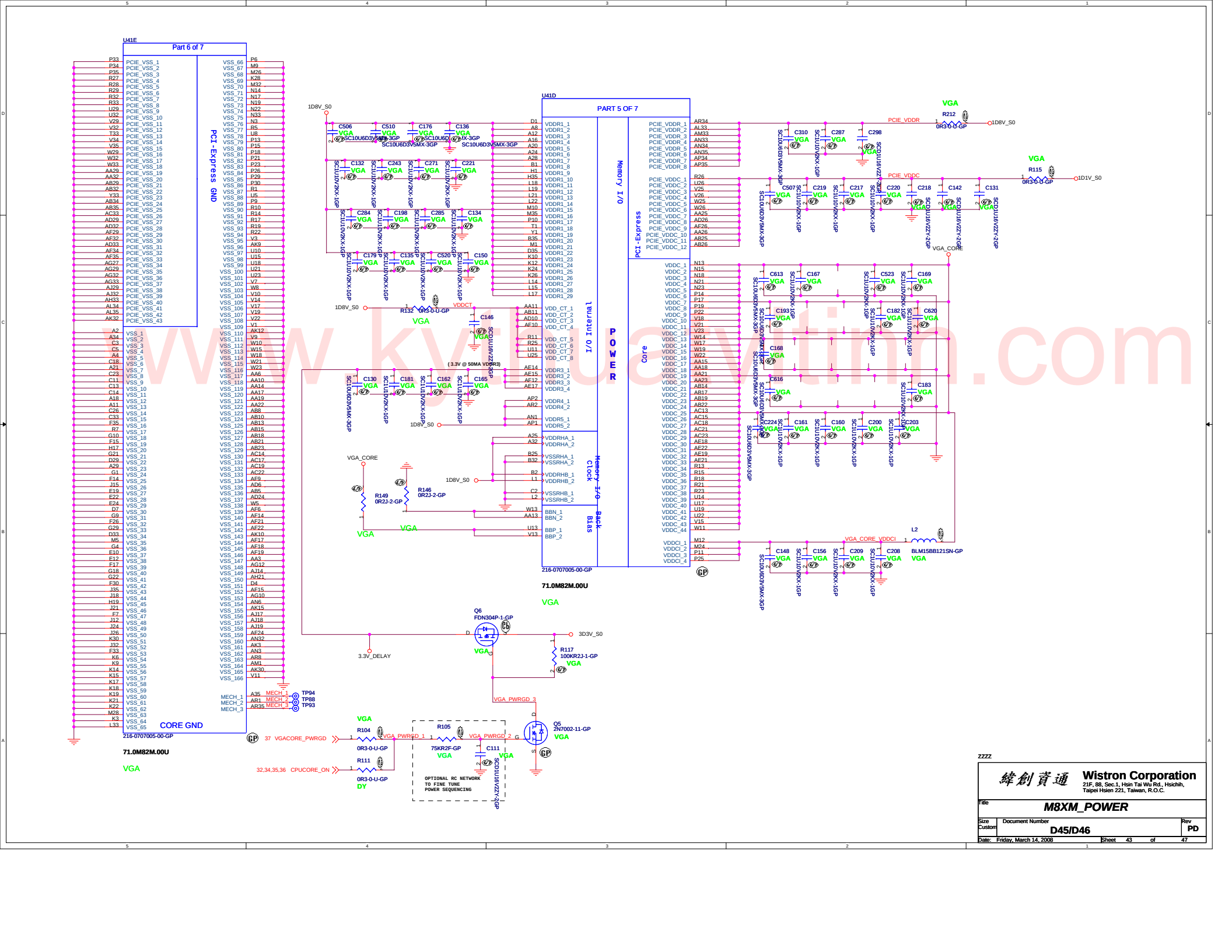
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***EMI/Spring/Boss***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Monday, March 17, 2008	Sheet 40 of 47	

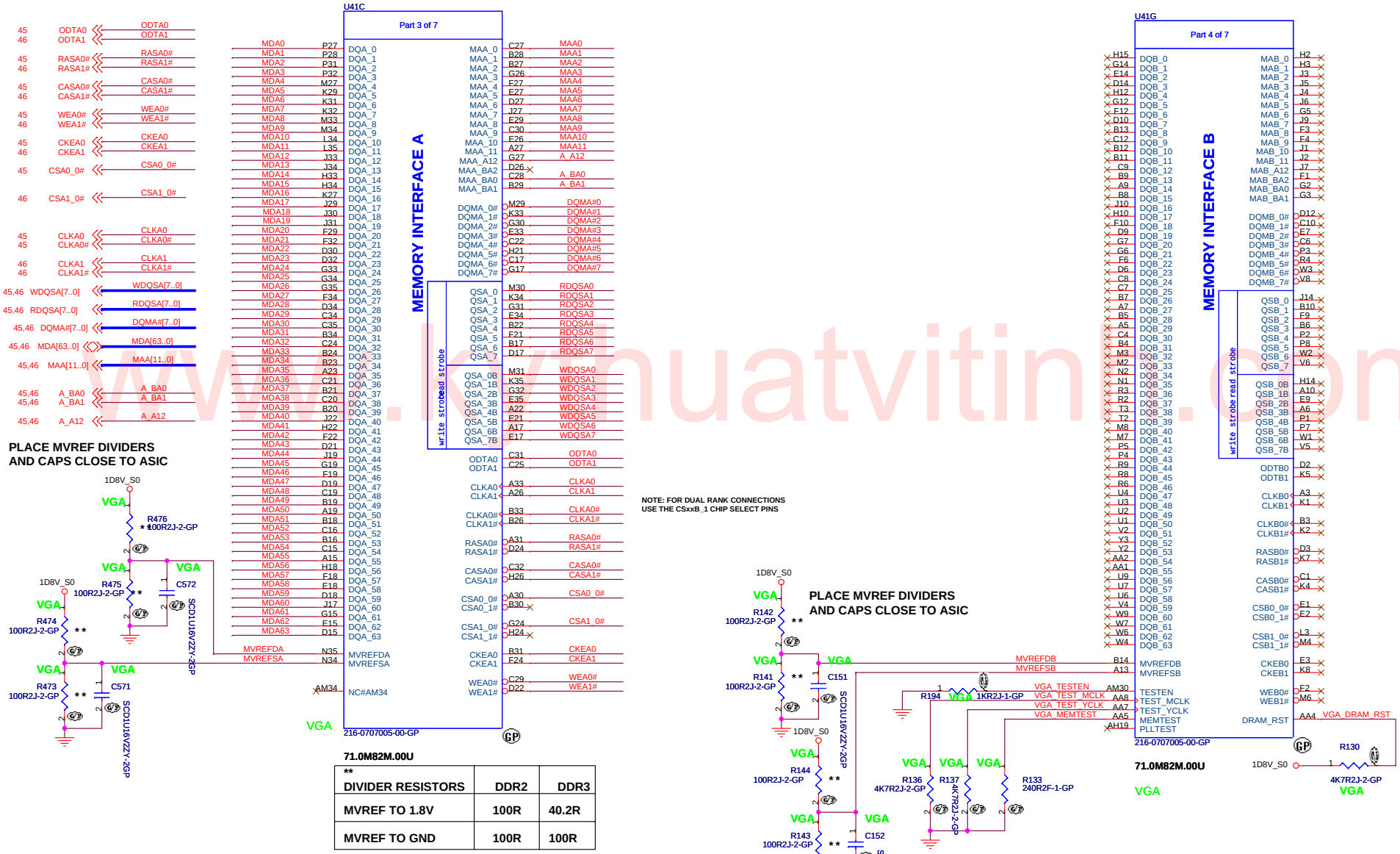


ZZZZ

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M8XM_PCIE		
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 41 of 47	







** DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

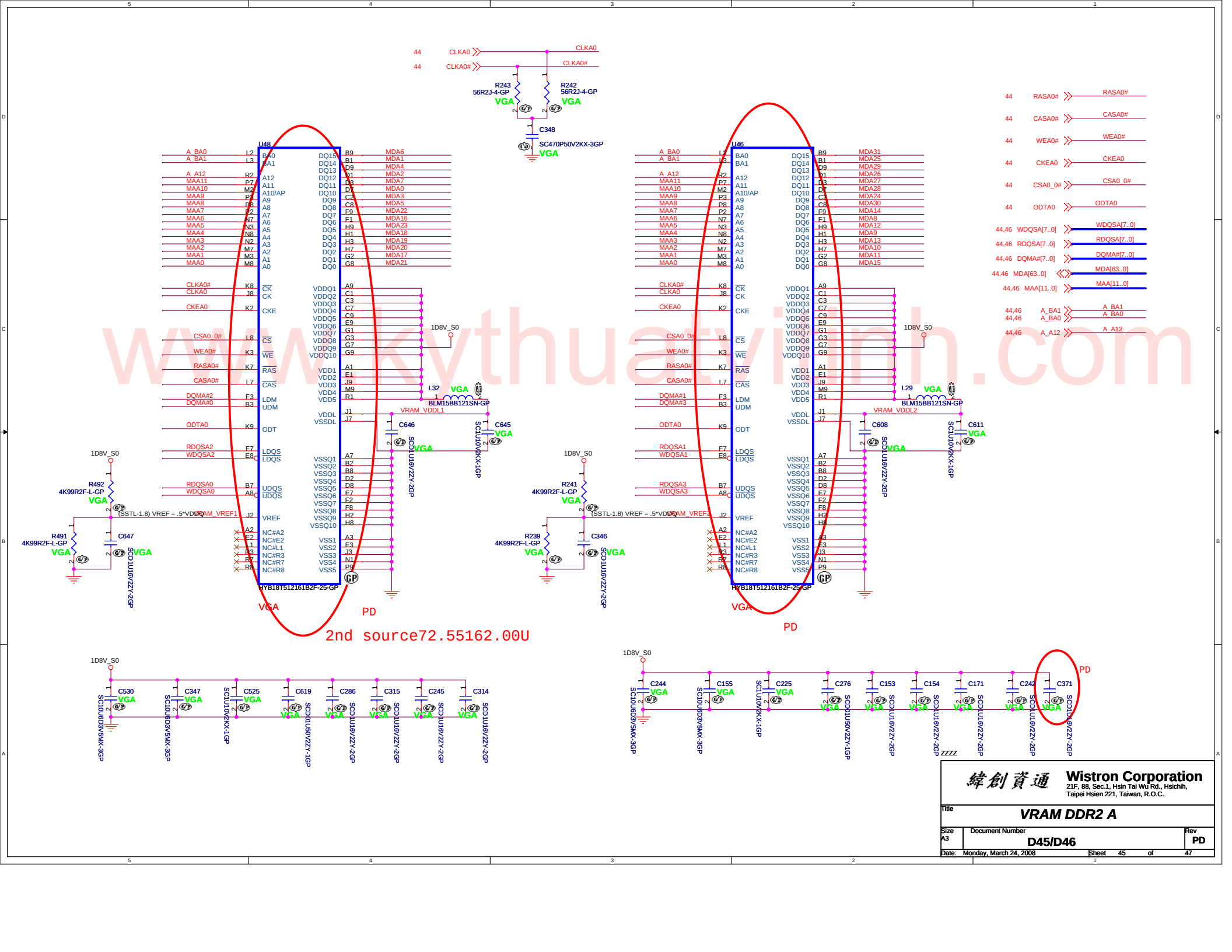
ZZZZ

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M8XM_MEMORY

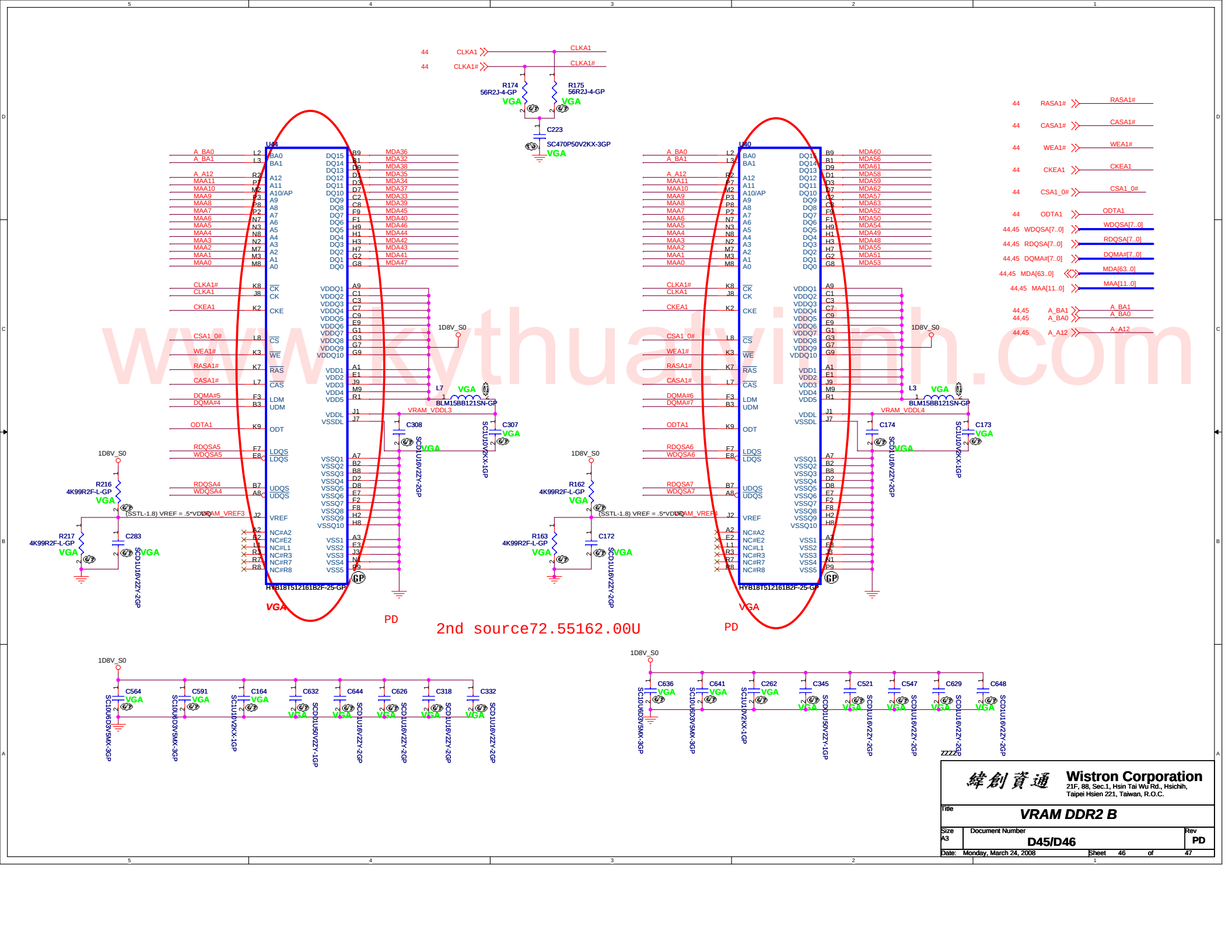
Size: A3 | Document Number: D45/D46 | Rev: PD

Date: Friday, March 14, 2008 | Sheet 44 of 47



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

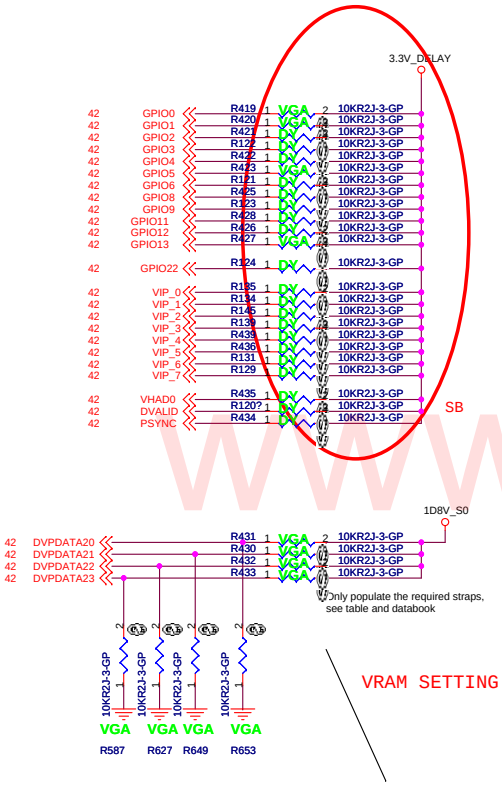
Title	VRAM DDR2 A	
Size A3	Document Number D45/D46	Rev PD
Date: Monday, March 24, 2008	Sheet 45 of 47	



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM DDR2 B	
Size: A3	Document Number: D45/D46
Rev: PD	
Date: Monday, March 24, 2008	Sheet 46 of 47

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

For Hynix 上R431,R430,R432,R433 (63.10334.1DL)
Delete R587,R627,R649,R653

For Qimonda 上R431,R430,R432,R587 (63.10334.1DL)
Delete R433,R627,R649,R653

For Samsung 上R431,R430,R627,R433 (63.10334.1DL)
Delete R587,R432,R649,R653

DVPDATA20 1
DVPDATA21 1 HY5PS121621CFP-25 Hynix
DVPDATA22 1 72.51216.F0U
DVPDATA23 1

DVPDATA20 1
DVPDATA21 1 HYB18T512161B2F-25 Qimonda
DVPDATA22 1 72.18512.M0U
DVPDATA23 0

DVPDATA20 1
DVPDATA21 1 K4N51163QE-ZC25 SamSung
DVPDATA22 0 72.45116.A0U
DVPDATA23 1

DVPDATA20 1
DVPDATA21 1 H5PS5162FFR-25C
DVPDATA22 0 HYNIX
DVPDATA23 0 72.55162.00U

D45 VRAM SELECT

手動改D45 BOM U43 71.CNTIG.H0U
U57 71.ICH9M.E0U

R186,187,188,198,201,202-> 63.R0034.1DL

手動改D46 BOM U43 71.CNTIG.G0U
U57 71.ICH9M.E0U

手動改共同BOM

DM2 62.10017.G31
U49 84.04634.037
U15 84.08896.037
H29 34.4B417.001
H30 34.4B417.001
H27 34.4F403.001
H31 34.4F403.001
H7 34.4F403.001
H9 34.4F403.001
H10 34.4G501.001

U11 71.00773.00G
U64 71.00380.003
U35 62.10053.401
U7 71.08111.E03

手動改NET

DM2 62.10017.G31
U35 62.10053.401

zzzz

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **STRAPS**

Size: Custom | Document Number: **D45/D46** | Rev: **PD**

Date: Monday, March 17, 2008 | Sheet 47 of 47