First International Computer,Inc

Portable Computer Group HW Department

Board name : Mother Board Schematic

Project : VA250

Version : 0.4

Current Date : Dec 05, 2006

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Net name Description :
5. Board Stack up Description :
6. Schematic modify Item and History :
7. power on & off & S3 Sequence :
8. Layout Guideline :
9. switch setting

Manager Sign by: Avery Lee

Drawing by : Richard Wang

Total confirm by:

LAN Circuit check by:

Audio Circuit check by:

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Title: VA250 < Yonah + VN896 + VT8237A >

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1. Schematic Page Description :

VA250 Schematic Ver : 0.3

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)

PCIINT	CHIP		
IRQA	NB		
IRQB	MiniPCI		
IRQC	MiniPCI		
IRQD		IRQH	PCI-E

BUSMASTER

REQ	CHIP
REQ0 / GNT0	
REQ1 / GNT1	
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Casacde)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	PS/2 mouse	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

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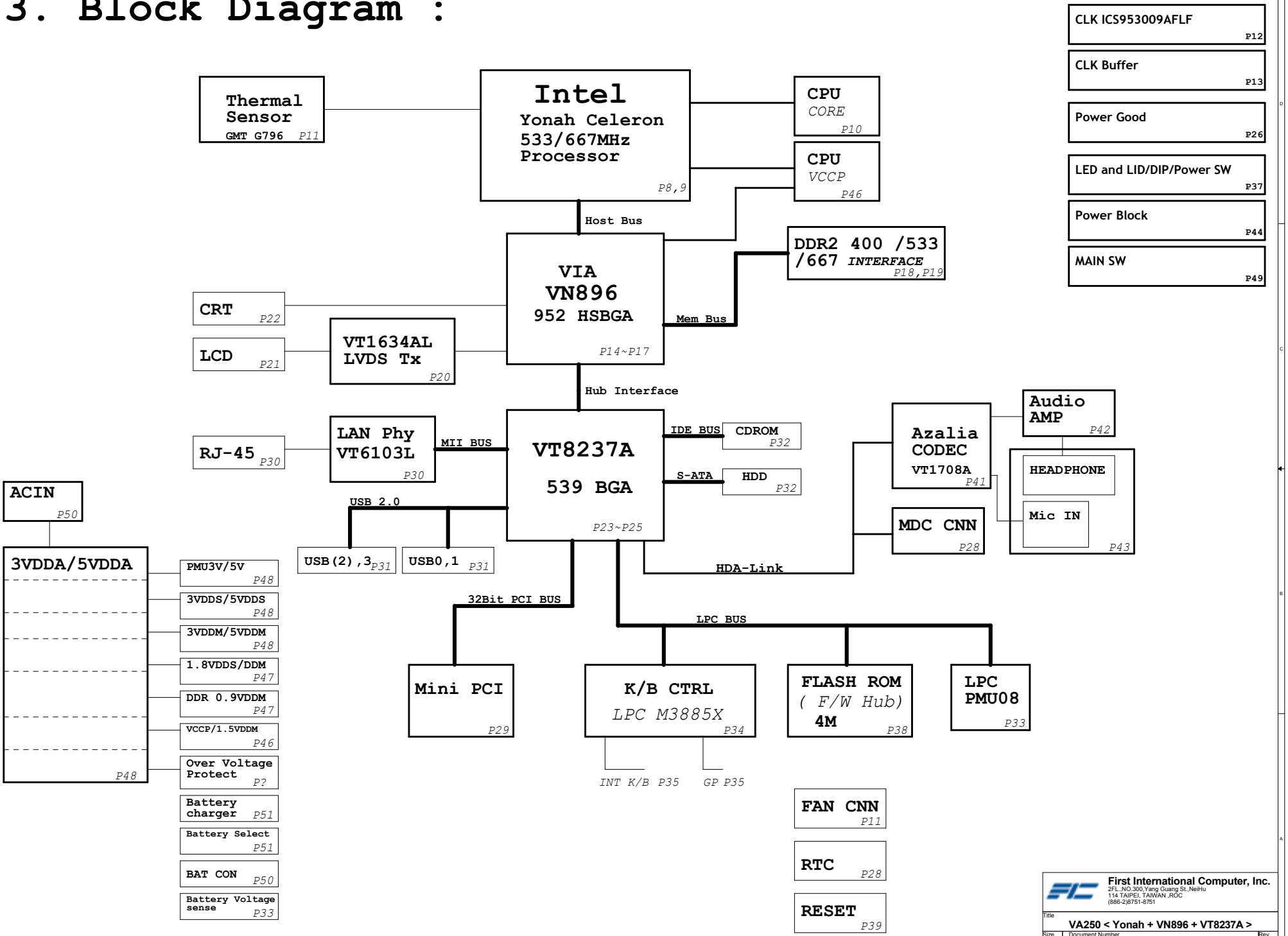
3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	ICs
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer(AGTL,CLOCK,DDR)
Layer 4	Stripline Layer(Analog,LVDS,other)
Layer 5	Power Plane
Layer 6	Solder Side,Microstrip signal Layer

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6.Schematic modify Item and History :

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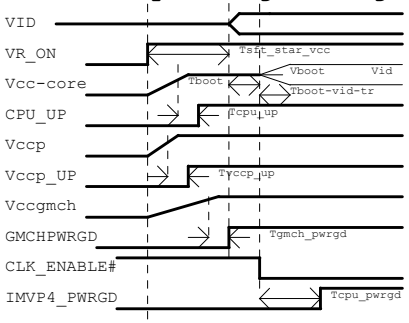
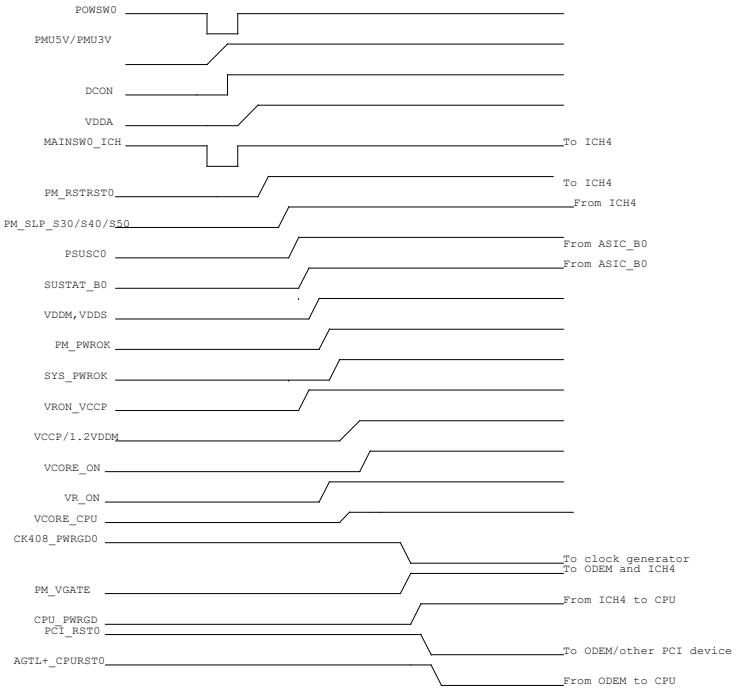
7. power on & off & S3 Sequence :

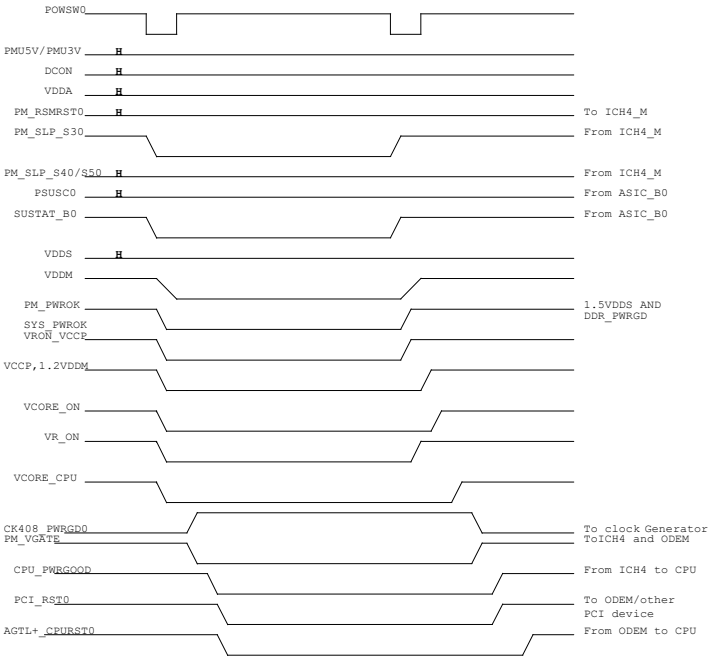
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

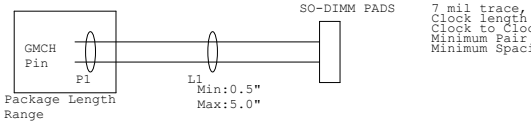
Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12:6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

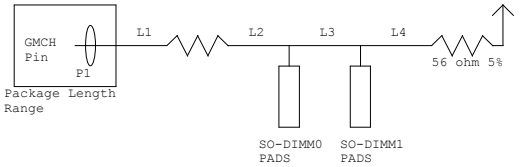
CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between + & -)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH	4.5" ~ 9.0 "	5 / 20 mils	* 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
AGPCLK_ATI	MAX : 8.5"		
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2.Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"~9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerenve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines

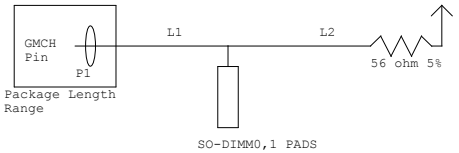


Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5", Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/- 25 mils

SDQ/SDM to SDQS Mapping

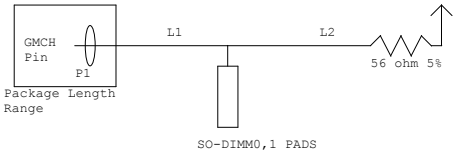
Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

Control Signals Topologies and Routing Guidelines



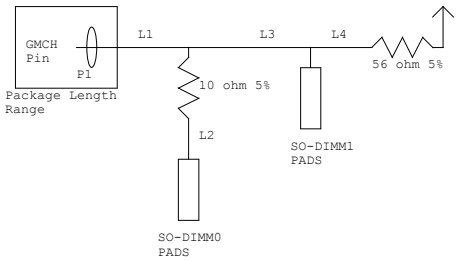
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

CPC Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

Command Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"

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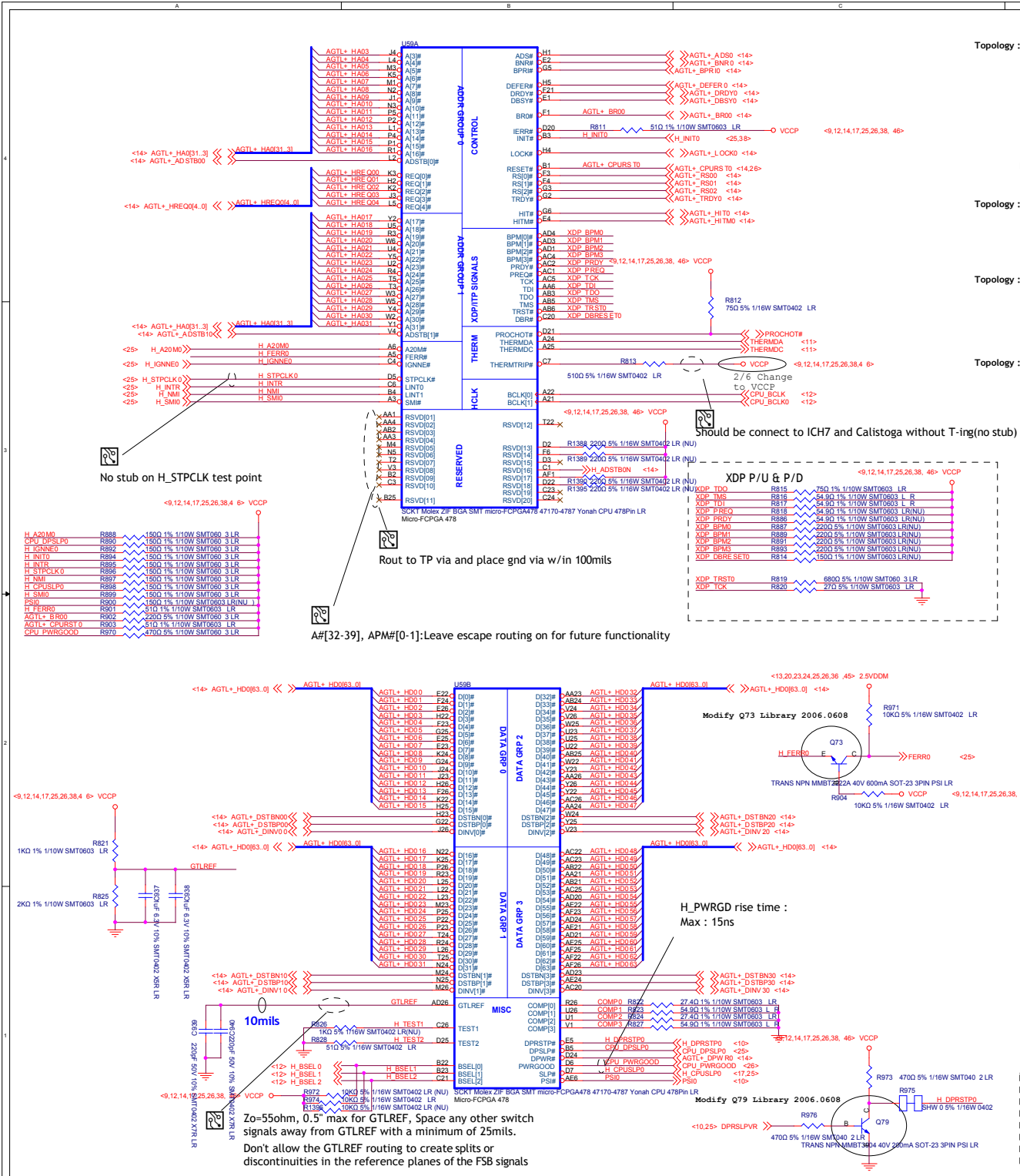
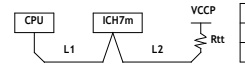
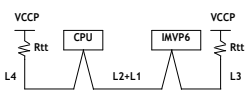


Topology : FERR#

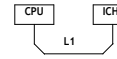


L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line



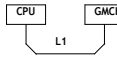
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Strip-line

Topology : PWRGOOD



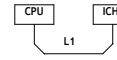
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#



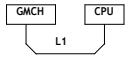
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SMI# , SMCLK#



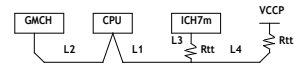
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 - 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils

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Place these inside socket cavity on L8
(North side secondary)

Place these inside socket cavity on
L8 (South side secondary)

<10,33, 36> VCORE_CPU

Place these inside socket cavity on L1
(North side Primary)

Place these inside socket cavity on L1
(South side Primary)

North side secondary

South side secondary

U59C

SCKT Molex ZIF BGA SMT micro-FCPGA478 47170-4787 Yonah CPU 478Pin LR
Micro-FCPGA 478

Via:2.5A

>100mils

VCCP <8,12,14,17,25,26,38,4 6>

C873
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR

Place these inside socket cavity on L8
(North side secondary)

Close to CPU
pin B26

<17,20,4 6>

1.5VDDM

20mils

C892
0.01uF 16V 10% SMT0402 X7R LR

C893
10uF 6.3V 10% 0805 X5R TDK LR

H_VID0 <10>
H_VID1 <10>
H_VID2 <10>
H_VID3 <10>
H_VID4 <10>
H_VID5 <10>
H_VID6 <10>

VCCSENSE <10>
VSSSEN SE <10>

18mil
7mil space

Route VCCSENSE and VSSSENSE traces
at 27.4 ohms with 50mil spacing.
Place PU and PD within 1 inch of CPU

U59D

SCKT Molex ZIF BGA SMT micro-FCPGA478 47170-4787 Yonah CPU 478Pin LR
Micro-FCPGA 478

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Rn
=[Rparallel*(Rntc+Rserial)/(Rparallel+Rntc+Rserial)
=[R813*(R815+R811)]/(R813+R815+R811)
=3.4K

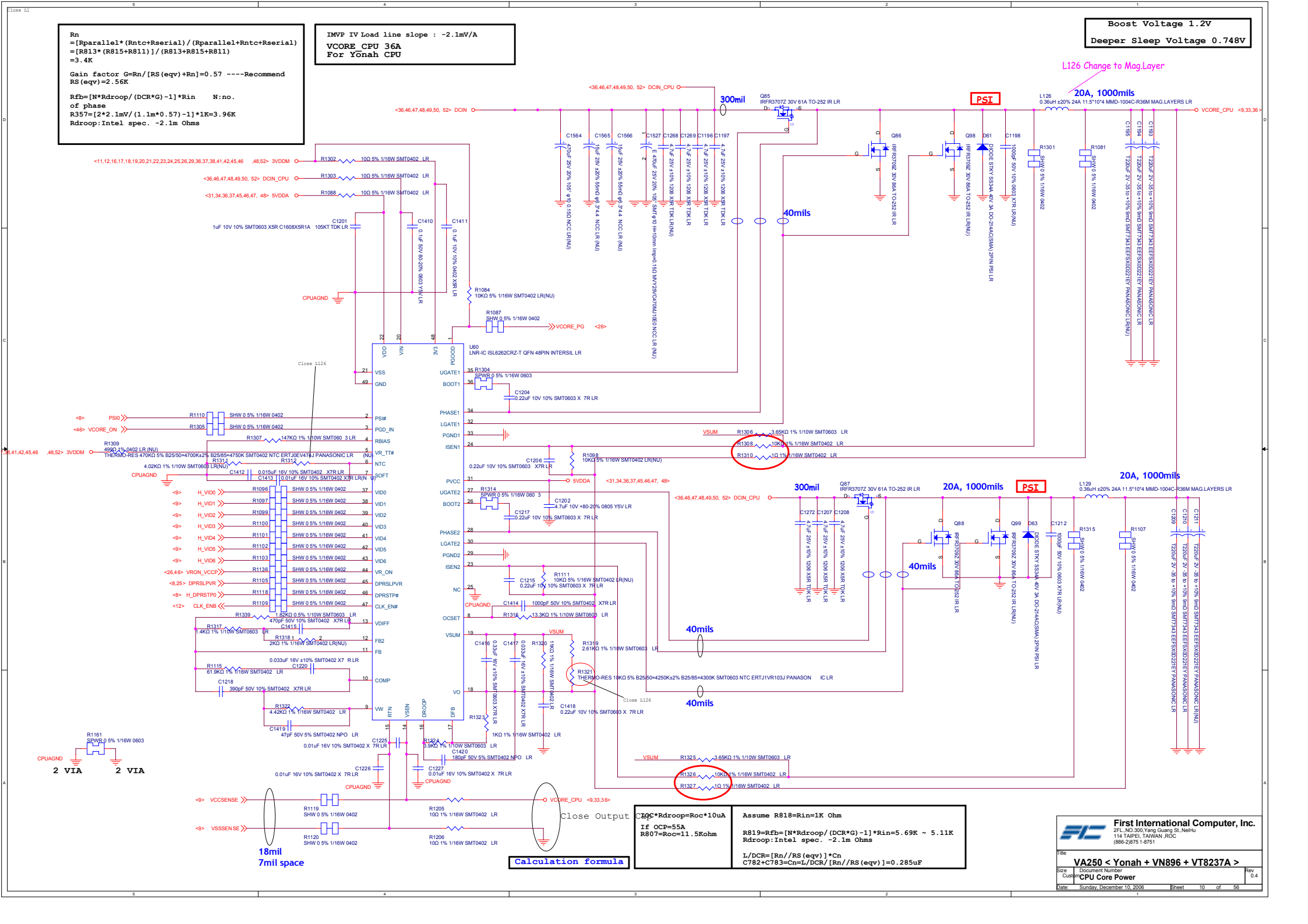
Gain factor G=Rn/[RS(eqv)+Rn]=0.57 ----Recommend
RS(eqv)=2.56K

Rfb=[N*Rdroop/(DCR*G)-1]*Rin N:no.
of phase
R357=[2*2.1mV/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms

IMVP IV Load line slope : -2.1mV/A
VCORE_CPU 36A
For Yonah CPU

Boost Voltage 1.2V
Deeper Sleep Voltage 0.748V

L126 Change to Mag.Layer



Calculation formula

IOC*Rdroop=Roc*10uA If OCP=55A R807=Roc=11.5Kohm	Assume R818=Rin=1K Ohm R819=Rfb=[N*Rdroop/(DCR*G)-1]*Rin=5.69K ~ 5.11K Rdroop:Intel spec. -2.1m Ohms L/DCR=[Rn//RS(eqv)]*Cn C782+C783=Cn=L/DCR/[Rn//RS(eqv)]=0.285uF

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Size: Custom | Document Number: CPU Core Power | Rev: 0.4
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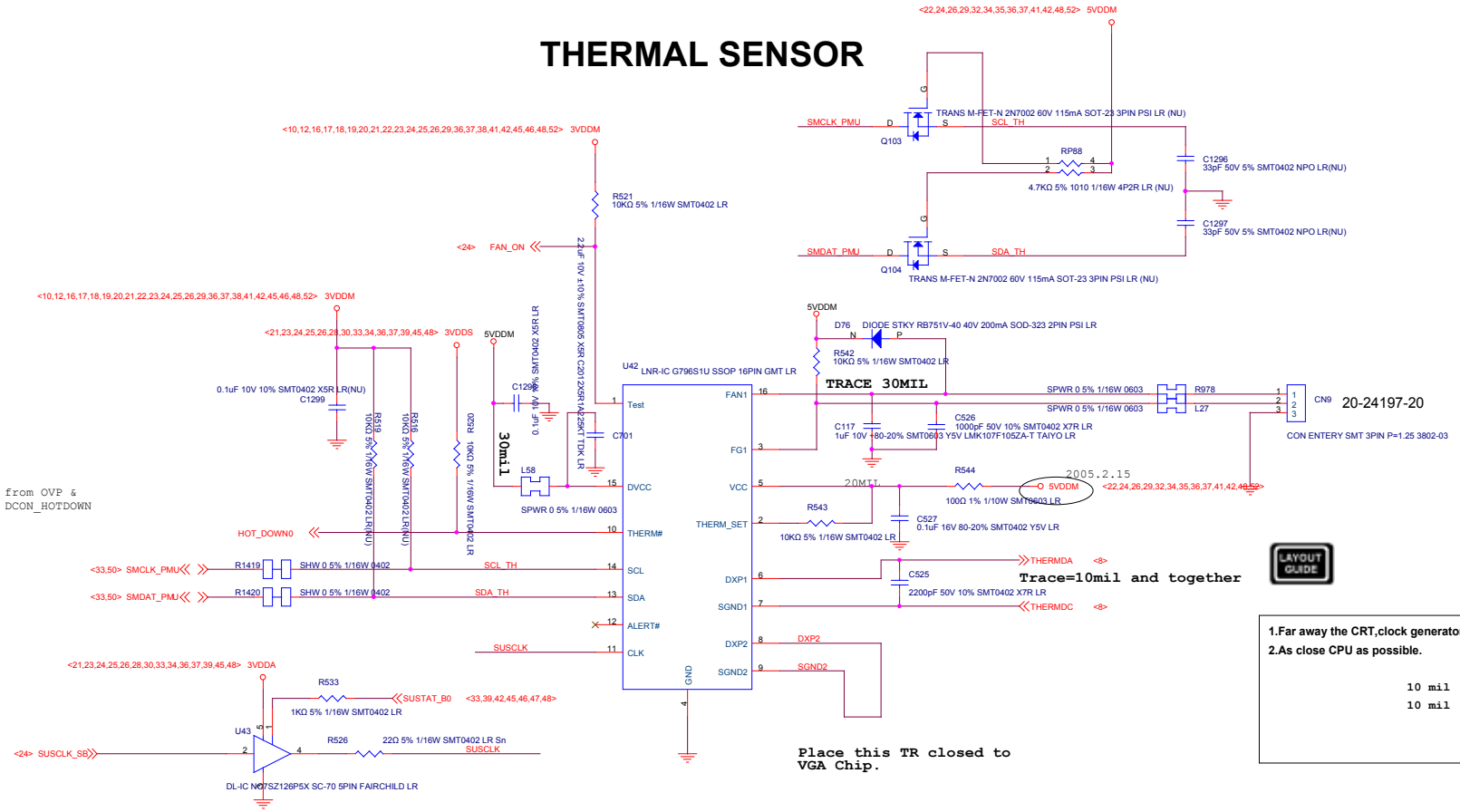
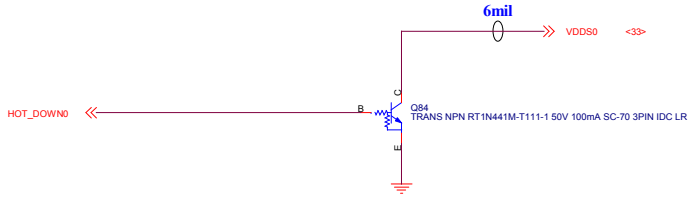
THERMAL SENSOR



1.Far away the CRT,clock generator,memory bus,PCI bus.
2.As close CPU as possible.

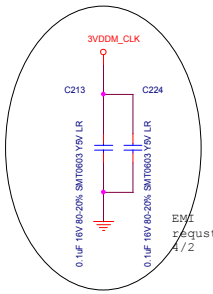
10 mil
10 mil

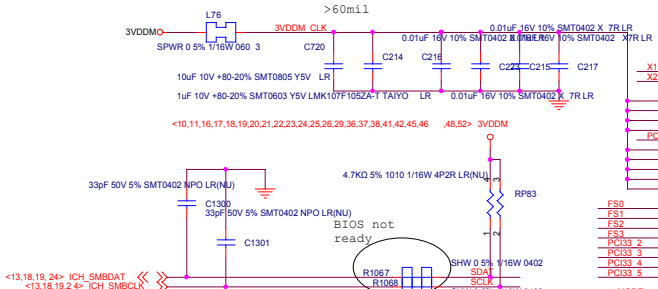


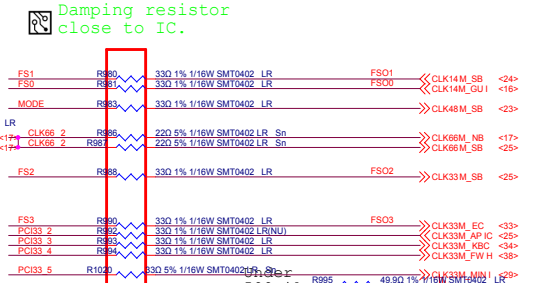
<22,24,26,29,32,34,35,36,37,41,42,48,52> 5VDDM
5VDDM
<21,23,24,25,26,28,30,33,34,36,37,39,45,48> 3VDDS
3VDDS

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title	VA250 < Yonah + VN896 + VT8237A >	
Size C	Document Number <Thermal / RTC>	Rev 0.4
Date: Sunday, December 10, 2006	Sheet 11 of 56	





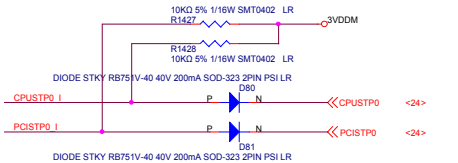


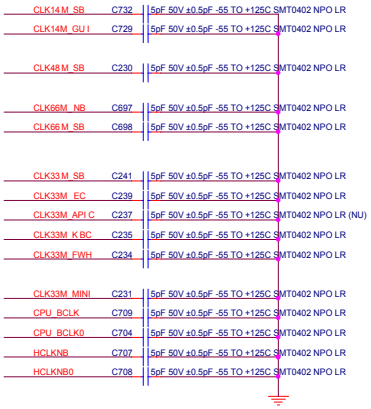
Clock Latout Guideline

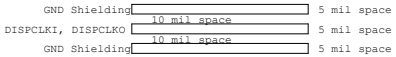
	CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock	CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between 1 & 0)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 20 mil
CLK66 Clock	CLK_ICH66 CLK_MCH66 CLK_AGP	4.5" ~ 9.0 " MAX : 8.5"	5 / 20 mils	Length mismatch within 100 mils
CLK33 Clock	CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" ~ 9.0 "	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock	CLK_MINIPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock	CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"~9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
	CLK_ICH48 CLK_MCH48	3.5" ~ 12.5"	5 / 20 mils	

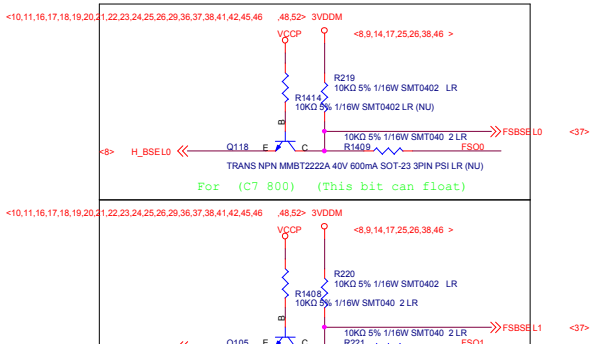
Clock Layout :
1. Close to Clock generator
2. Trace as short as possible and use 12 mil
3. Place crystal within 500 mils of CLK Generator

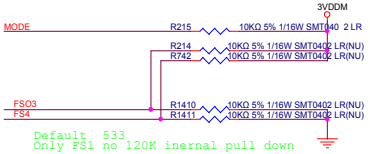
FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	REF
0	0	0	0	0	266.00M	66.67M	33.33M	14.318M
0	0	0	0	1	133.00M	66.67M	33.33M	14.318M
0	0	0	1	0	200.00M	66.67M	33.33M	14.318M
0	0	0	1	1	166.67M	66.67M	33.33M	14.318M
0	0	1	0	0	333.33M	66.67M	33.33M	14.318M
0	0	1	0	1	100.00M	66.67M	33.33M	14.318M
0	0	1	1	0	400.00M	66.67M	33.33M	14.318M
0	0	1	1	1	200.00M	66.67M	33.33M	14.318M



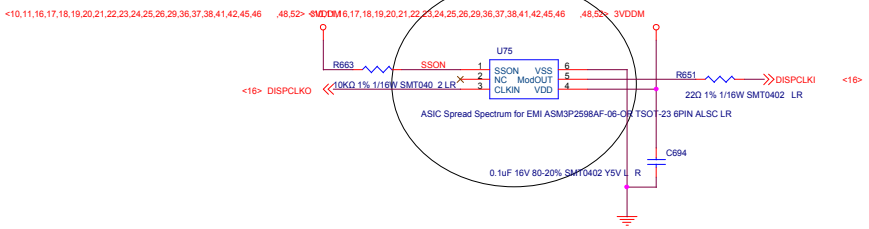








Change to 05-23728-01 libarary 2006.07.25 Modify



R1409,R221,R217, R214,R1410, (R742,R1411) should be very, very close to their lines. Q118,Q105,Q117 needn't.

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114 TAIPEI, TAIWAN ,ROC
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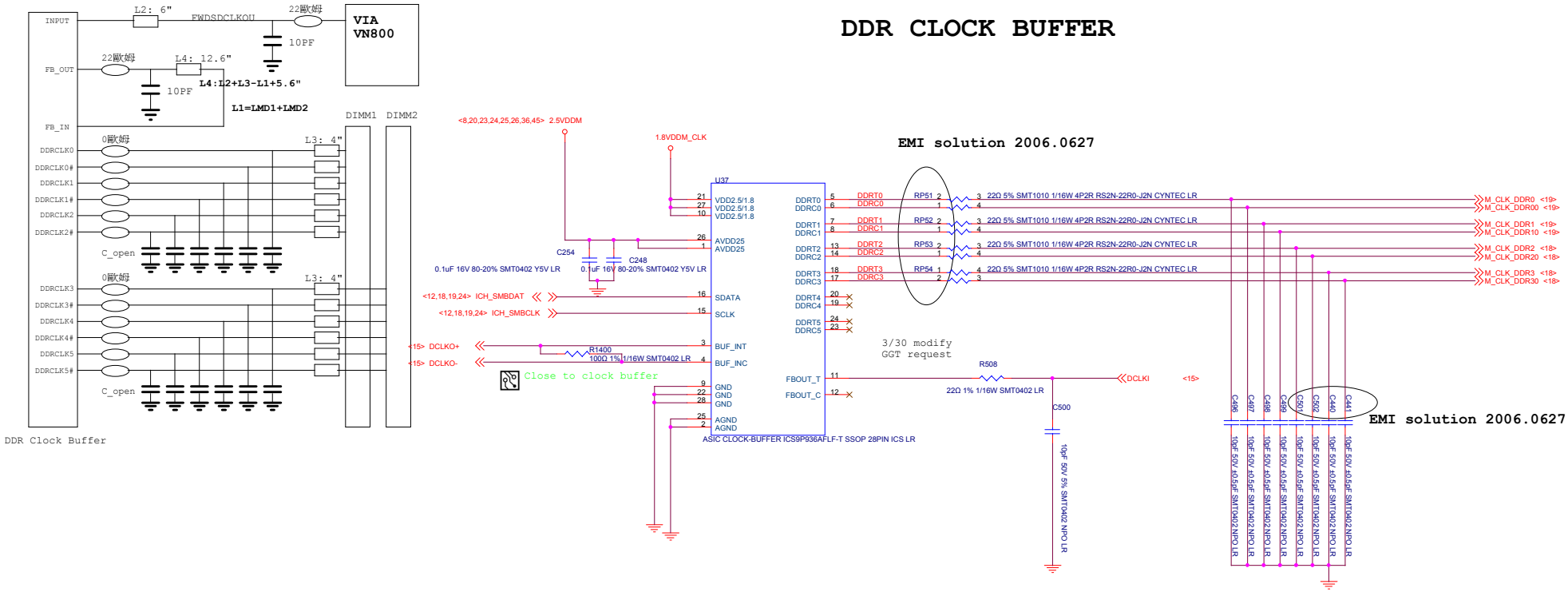
Title: VA250 < Yonah + VN896 + VT8237A >

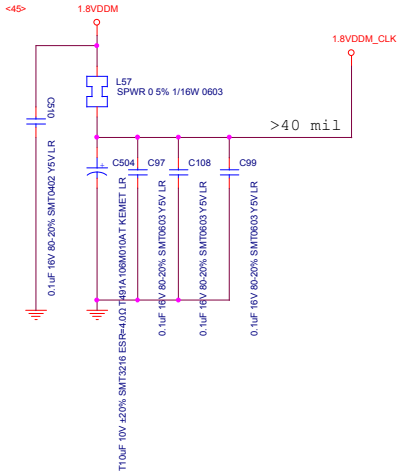
Size: C | Document Number: <Clock-Gen> | Rev: 0.4

Date: Sunday, December 10, 2006 | Sheet 12 of 56

DDR CLOCK BUFFER



Mount these capacitor 2006.0602 Modify



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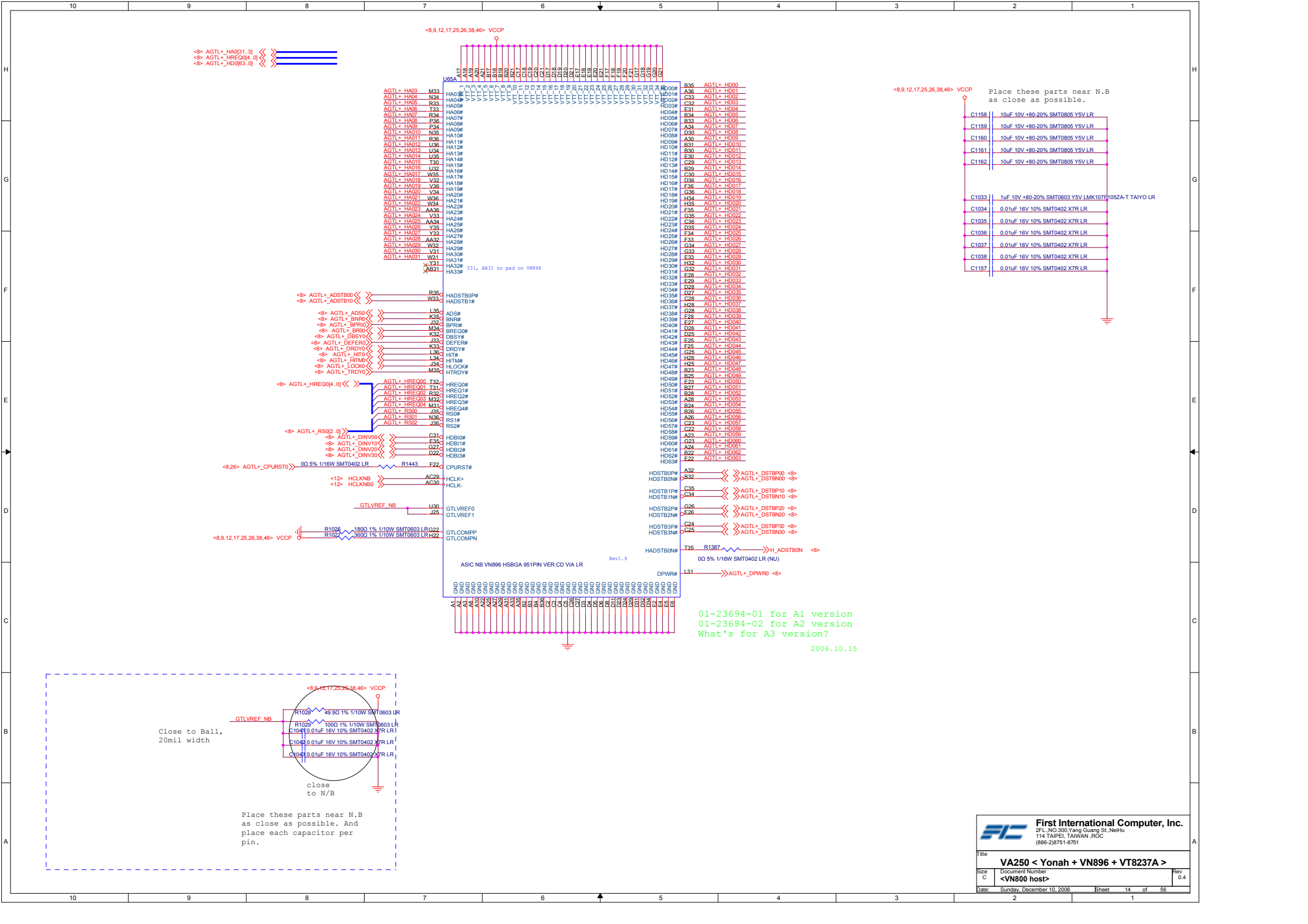
Title: VA250 < Yonah + VN896 + VT8237A >		
Size: C	Document Number: <clock buffer>	Rev: 0.4
Date: Sunday, December 10, 2006	Sheet 13 of 56	



Company	First International Computer, Inc.
Address	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	VA250 < Yonah + VN896 + VT8237A >
Size	C
Document Number	<VN800 host>
Rev	0.4
Date	Sunday, December 10, 2006
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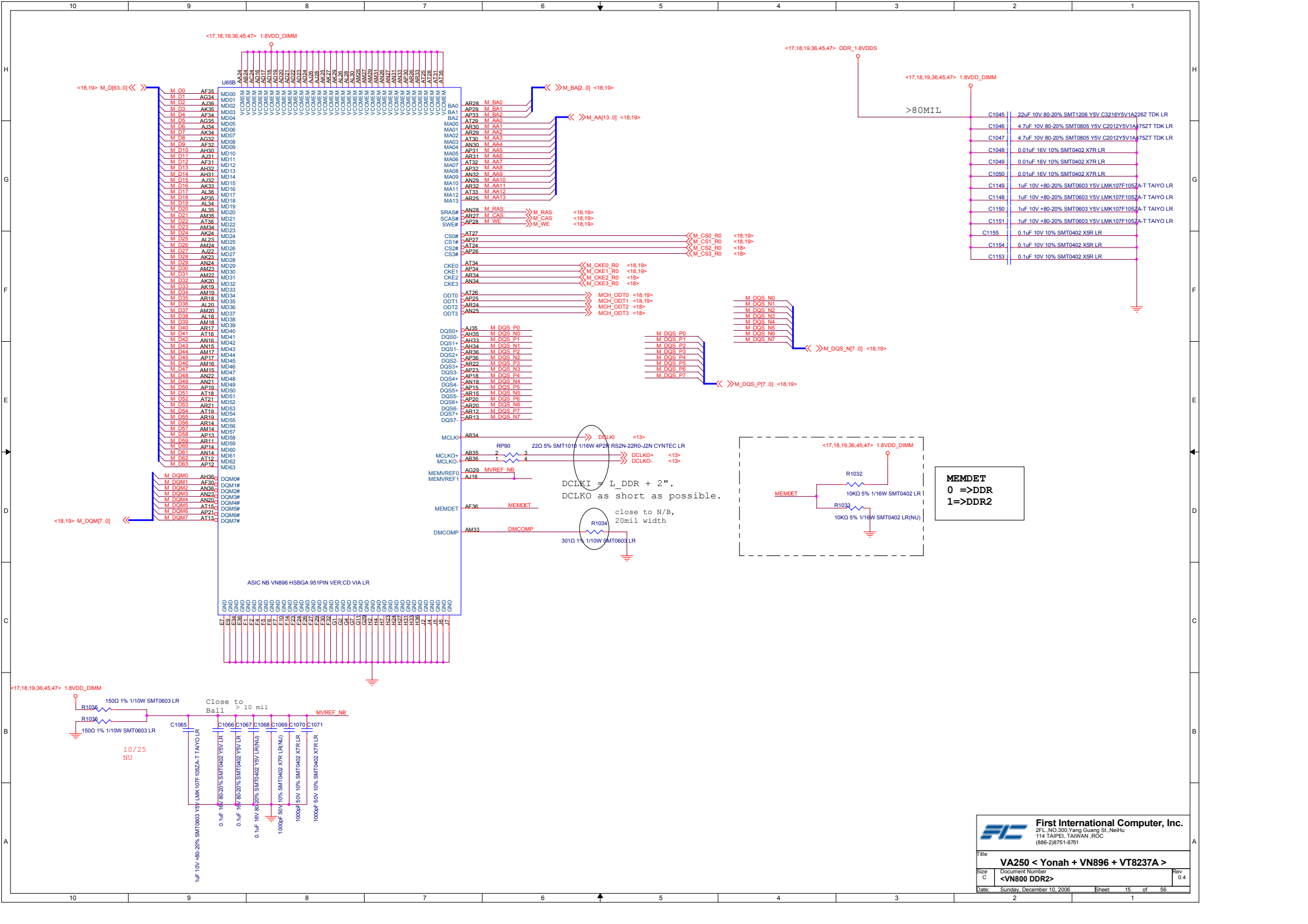
U65B
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
<17,18,19,36,45,47> 1.8VDD_DIMM
<18,19> M_D[63..0]
<18,19> M_DQM[7..0]
M_BA[2..0] <18,19>
M_AA[13..0] <18,19>
M_RAS <18,19>
M_CAS <18,19>
M_WE <18,19>
M_CS0_R0 <18,19>
M_CS1_R0 <18,19>
M_CS2_R0 <18>
M_CS3_R0 <18>
M_CKE0_R0 <18,19>
M_CKE1_R0 <18,19>
M_CKE2_R0 <18>
M_CKE3_R0 <18>
MCH_ODT0 <18,19>
MCH_ODT1 <18,19>
MCH_ODT2 <18>
MCH_ODT3 <18>
M_DQS_N[7..0] <18,19>
M_DQS_P[7..0] <18,19>
DCLKI <13>
DCLKO+ <13>
DCLKO- <13>
RP90
22Ω 5% SMT1010 1/16W 4P2R RS2N-22R0-J2N CYNTEC LR
MVREF_NB
MEMDET
DMCOMP
R1034
301Ω 1% 1/10W SMT0603 LR
DCLKI = L_DDR + 2".
DCLKO as short as possible.
close to N/B,
20mil width
<17,18,19,36,45,47> DDR_1.8VDDS
>80MIL
C1045 22uF 10V 80-20% SMT1206 Y5V C3216Y5V1A226Z TDK LR
C1046 4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
C1047 4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
C1048 0.01uF 16V 10% SMT0402 X7R LR
C1049 0.01uF 16V 10% SMT0402 X7R LR
C1050 0.01uF 16V 10% SMT0402 X7R LR
C1149 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1148 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1150 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1151 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1155 0.1uF 10V 10% SMT0402 X5R LR
C1154 0.1uF 10V 10% SMT0402 X5R LR
C1153 0.1uF 10V 10% SMT0402 X5R LR
R1032
10KΩ 5% 1/16W SMT0402 LR
R1033
10KΩ 5% 1/16W SMT0402 LR(NU)
MEMDET
0 =>DDR
1=>DDR2
<17,18,19,36,45,47> 1.8VDD_DIMM
R1035 150Ω 1% 1/10W SMT0603 LR
R1036 150Ω 1% 1/10W SMT0603 LR
Close to Ball > 10 mil
10/25 NU
C1065 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1066 0.1uF 16V 80-20% SMT0402 Y5V LR
C1067 0.1uF 16V 80-20% SMT0402 Y5V LR
C1068 0.1uF 16V 80-20% SMT0402 Y5V LR(NU)
C1069 1000pF 50V 10% SMT0402 X7R LR(NU)
C1070 1000pF 50V 10% SMT0402 X7R LR
C1071 1000pF 50V 10% SMT0402 X7R LR
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
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Title
VA250 < Yonah + VN896 + VT8237A >
Size C
Document Number <VN800 DDR2>
Rev 0.4
Date: Sunday, December 10, 2006
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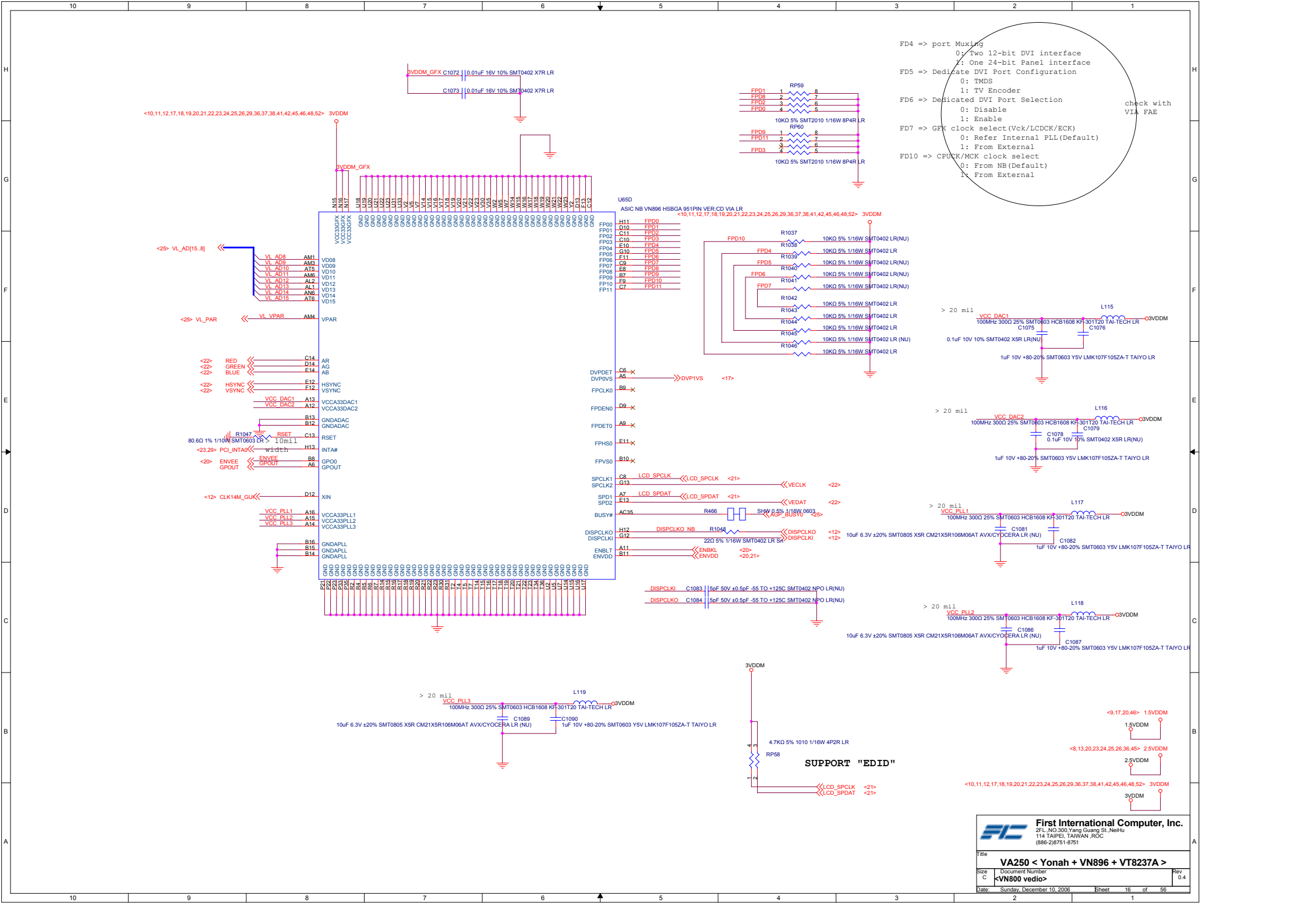
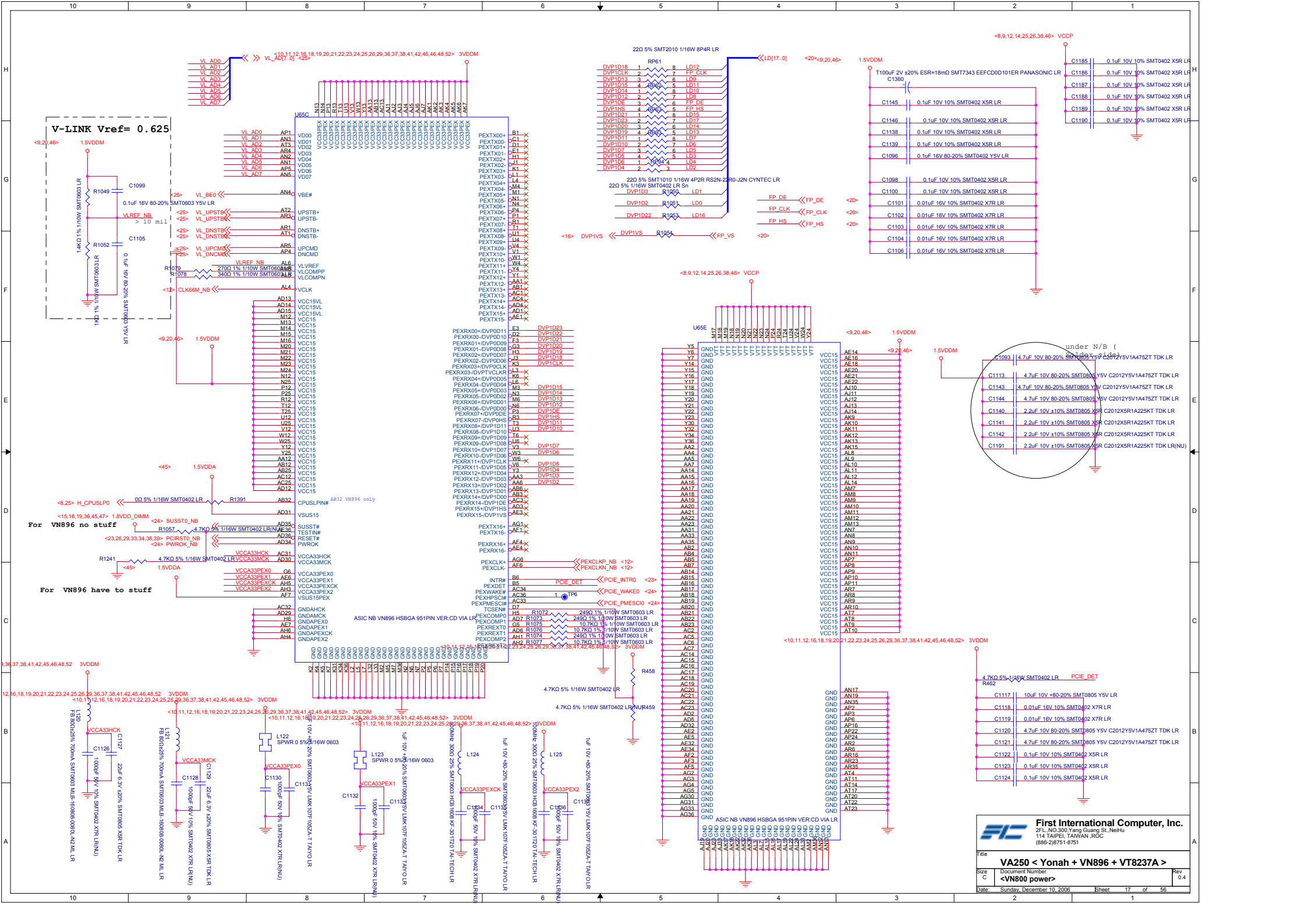

FD4 => port Muxing
0: Two 12-bit DVI interface
1: One 24-bit Panel interface
FD5 => Dedicate DVI Port Configuration
0: TMDS
1: TV Encoder
FD6 => Dedicated DVI Port Selection
0: Disable
1: Enable
FD7 => GFX clock select(Vck/LCDCK/ECK)
0: Refer Internal PLL(Default)
1: From External
FD10 => CPUCK/MCK clock select
0: From NB(Default)
1: From External
check with VIA FAE
U65D
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
SUPPORT "EDID"
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
VA250 < Yonah + VN896 + VT8237A >
Size C
Document Number
<VN800 vedio>
Rev 0.4
Date: Sunday, December 10, 2006
Sheet 16 of 56


V-LINK Vref= 0.625
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
For VN896 no stuff
For VN896 have to stuff
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
VA250 < Yonah + VN896 + VT8237A >
<VN800 power>
Date: Sunday, December 10, 2006
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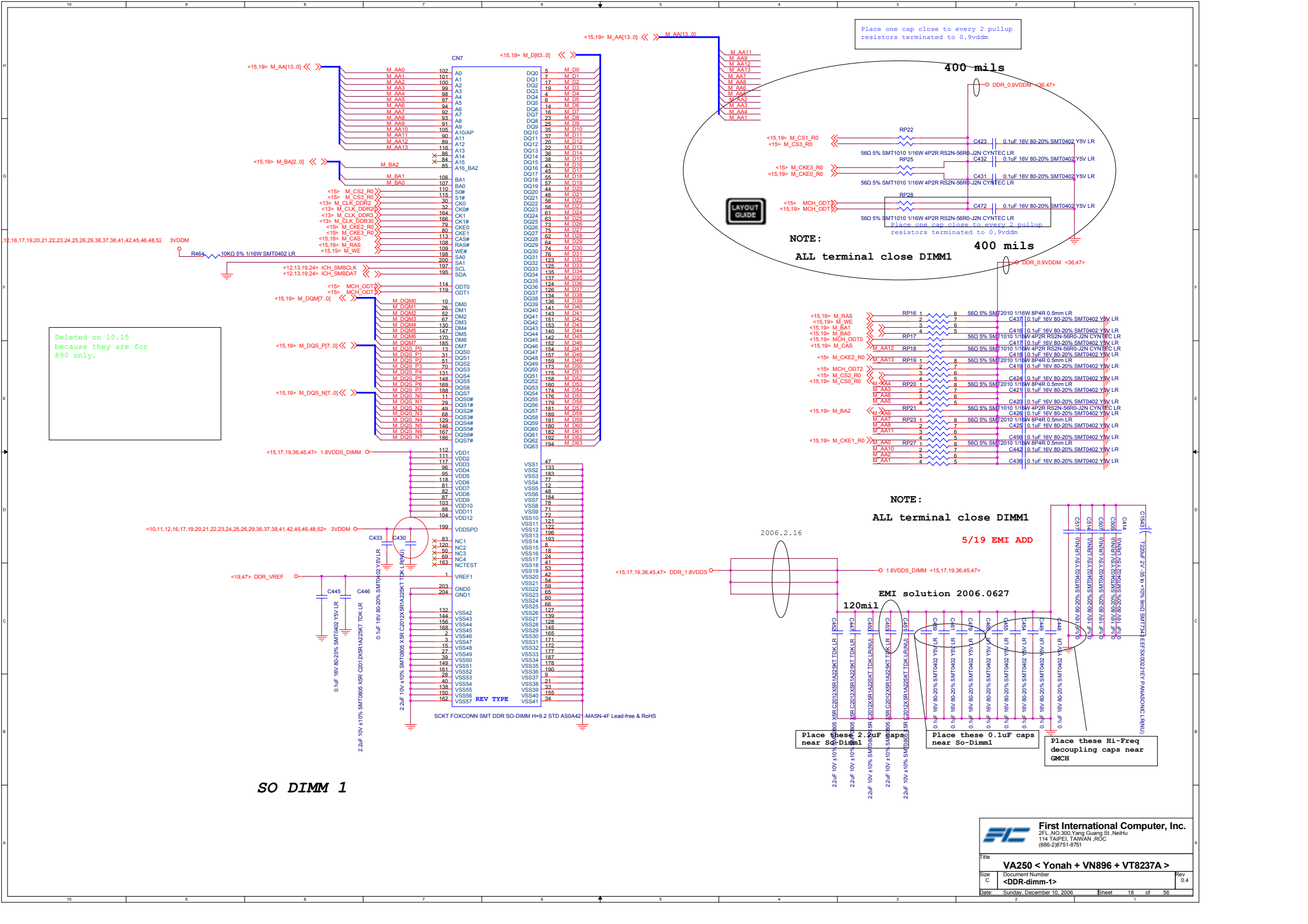
CN7
SO DIMM 1
SCKT FOXCONN SMT DDR SO-DIMM H=9.2 STD AS0A42-MASN-4F Lead-free & RoHS
REV TYPE
Deleted on 10.15 because they are for 890 only.
Place one cap close to every 2 pullup resistors terminated to 0.9vddm
400 mils
NOTE:
ALL terminal close DIMM1
LAYOUT GUIDE
56Ω 5% SMT1010 1/16W 4P2R RS2N-56R0-J2N CYNTEC LR
0.1uF 16V 80-20% SMT0402 Y5V LR
10KΩ 5% 1/16W SMT0402 LR
5/19 EMI ADD
2006.2.16
EMI solution 2006.0627
120mil
Place these 2.2uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm1
Place these Hi-Freq decoupling caps near GMCH
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2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
VA250 < Yonah + VN896 + VT8237A >
<DDR-dimm-1>
Sunday, December 10, 2006
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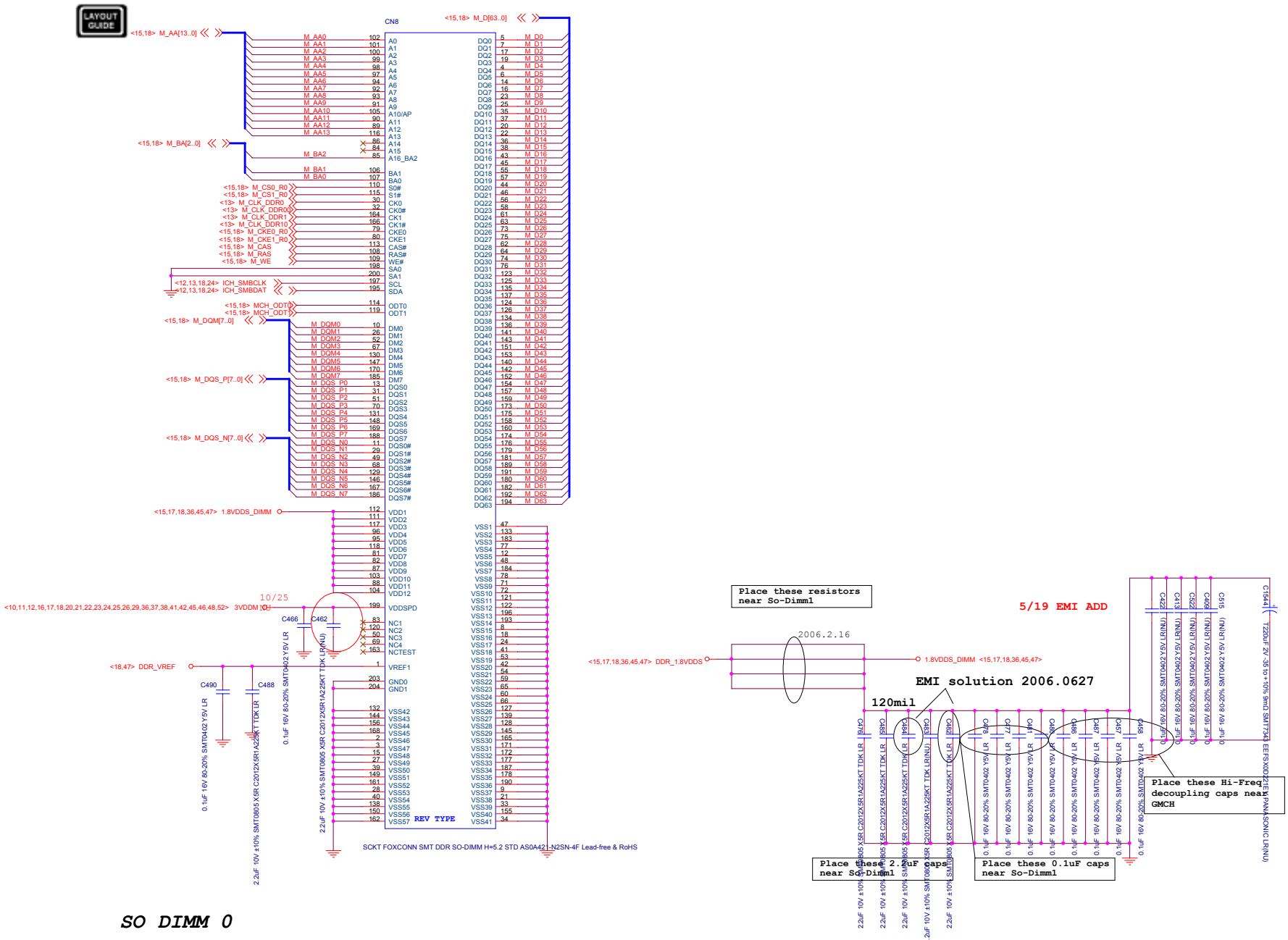

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Title: VA250 < Yonah + VN896 + VT8237A >

Size: C | Document Number: <DDR-dimm-2> | Rev: 0.4

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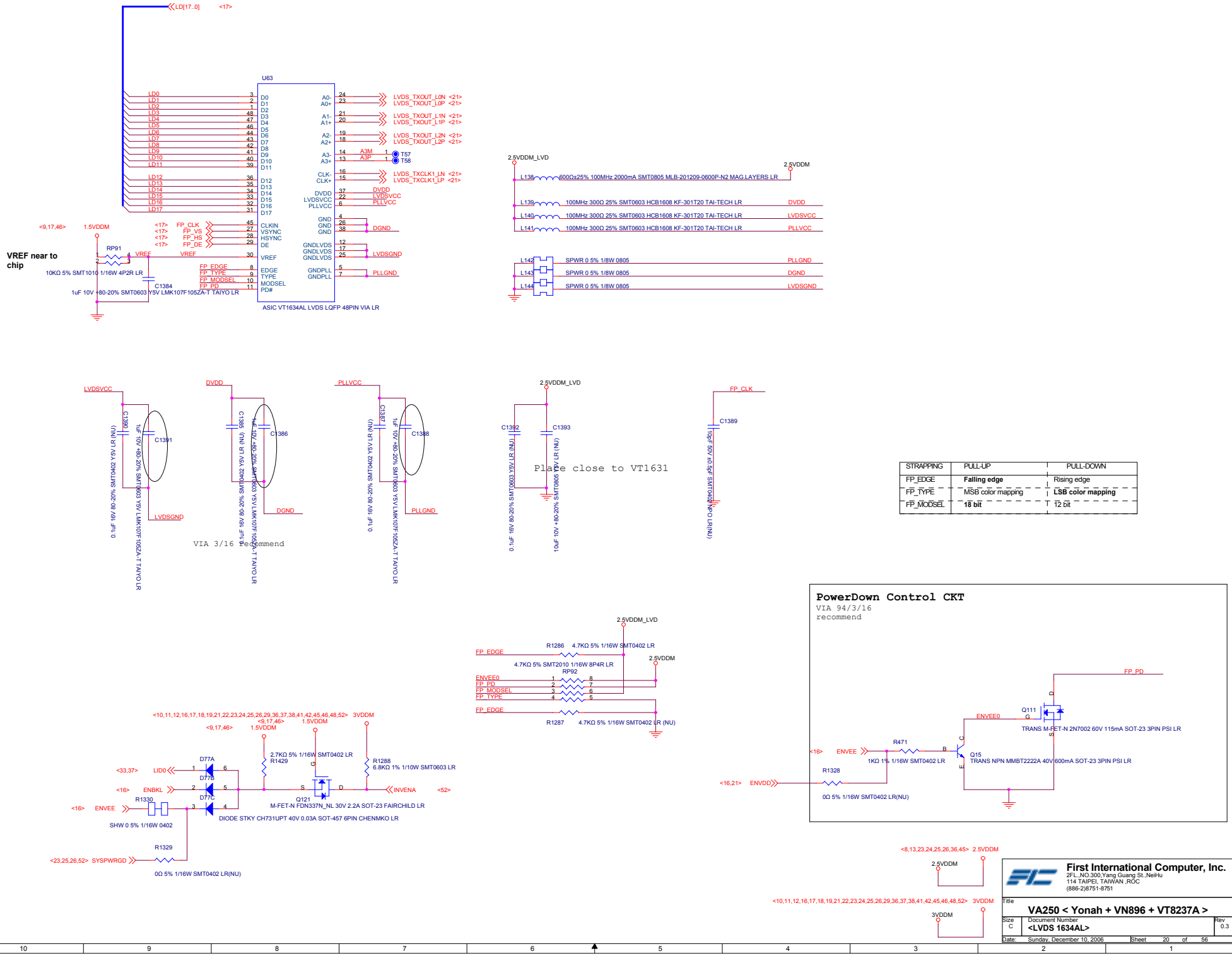
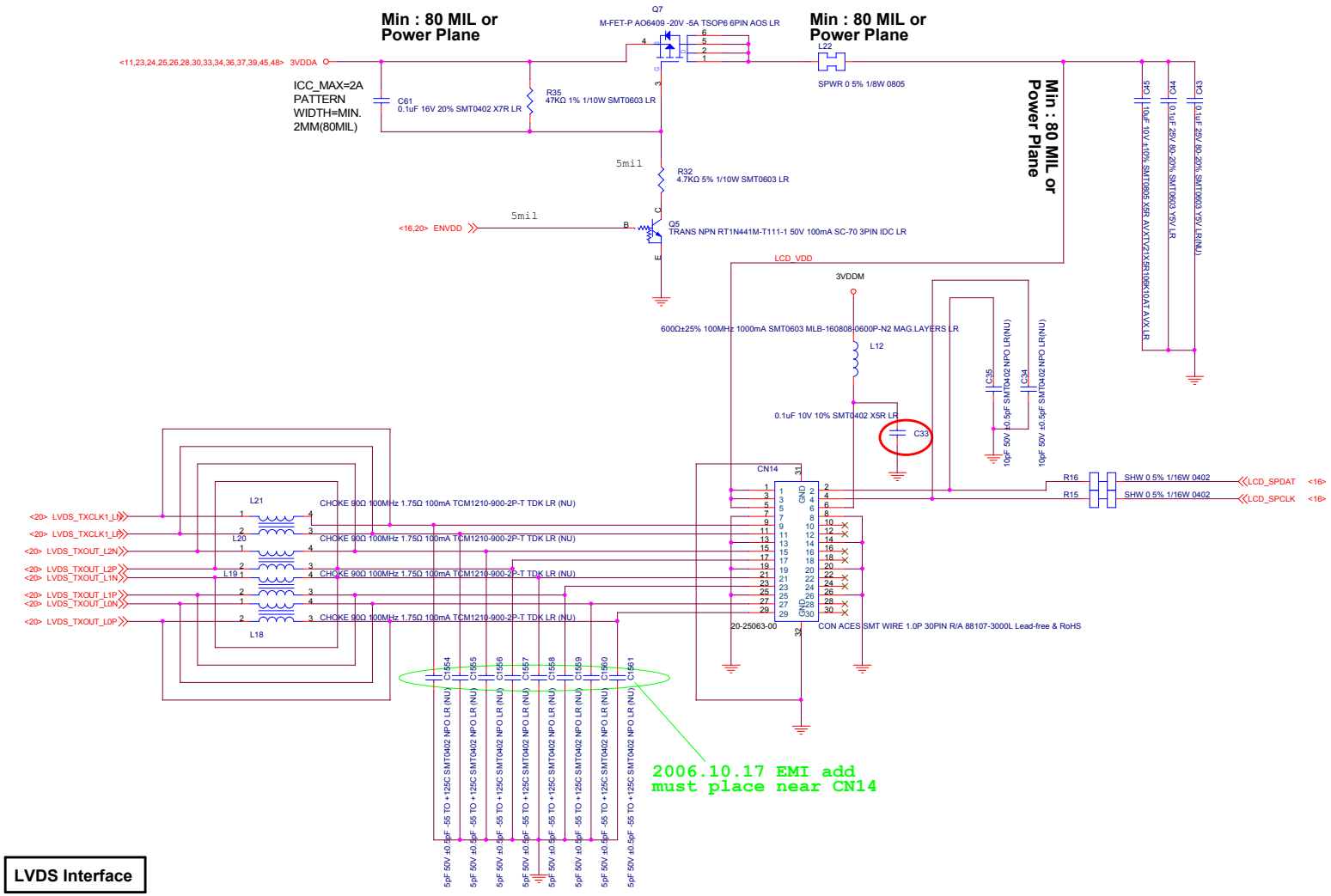

LD[17..0] <17>
U63
LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8 LD9 LD10 LD11 LD12 LD13 LD14 LD15 LD16 LD17
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17
A0- A0+ A1- A1+ A2- A2+ A3- A3+ CLK- CLK+
LVDS_TXOUT_L0N <21> LVDS_TXOUT_L0P <21>
LVDS_TXOUT_L1N <21> LVDS_TXOUT_L1P <21>
LVDS_TXOUT_L2N <21> LVDS_TXOUT_L2P <21>
A3M A3P T57 T58
LVDS_TXCLK1_LN <21> LVDS_TXCLK1_LP <21>
DVDD LVDSVCC PLLVCC
GND GND GND
DGND LVDSGND PLLGND
GNDLVDS GNDLVDS GNDLVDS
GNDPLL GNDPLL
<9,17,46> 1.5VDDM
RP91
10KΩ 5% SMT1010 1/16W 4P2R LR
VREF near to chip
<17> FP_CLK <17> FP_VS <17> FP_HS <17> FP_DE
CLKIN VSYNC HSYNC DE VREF
FP_EDGE FP_TYPE FP_MODSEL FP_PD
EDGE TYPE MODSEL PD#
C1384
1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
ASIC VT1634AL LVDS LQFP 48PIN VIA LR
2.5VDDM_LVD
2.5VDDM
L138 600Ω±25% 100MHz 2000mA SMT0805 MLB-201209-0600P-N2 MAG.LAYERS LR
L139 100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR DVDD
L140 100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR LVDSVCC
L141 100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR PLLVCC
L142 SPWR 0 5% 1/8W 0805 PLLGND
L143 SPWR 0 5% 1/8W 0805 DGND
L144 SPWR 0 5% 1/8W 0805 LVDSGND
LVDSVCC DVDD PLLVCC
C1390 1uF 10V +80-20% SMT0402 Y5V LR (NU)
C1391 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1385 (NU) LR 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1386 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1387 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1388 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
LVDSGND DGND PLLGND
VIA 3/16 recommend
2.5VDDM_LVD
C1392 0.1uF 16V 80-20% SMT0603 Y5V LR (NU)
C1393 10uF 10V +80-20% SMT0805 Y5V LR (NU)
Place close to VT1631
FP_CLK
C1389 10pF 50V ±0.5pF SMT0402 NPO LR(NU)
STRAPPING | PULL-UP | PULL-DOWN
FP_EDGE | Falling edge | Rising edge
FP_TYPE | MSB color mapping | LSB color mapping
FP_MODSEL | 18 bit | 12 bit
2.5VDDM_LVD
FP_EDGE R1286 4.7KΩ 5% 1/16W SMT0402 LR
4.7KΩ 5% SMT2010 1/16W 8P4R LR
RP92
2.5VDDM
ENVEE0 FP_PD FP_MODSEL FP_TYPE FP_EDGE
R1287 4.7KΩ 5% 1/16W SMT0402 LR (NU)
PowerDown Control CKT
VIA 94/3/16
recommend
FP_PD
Q111 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
ENVEE0
<16> ENVEE
R471 1KΩ 1% 1/16W SMT0402 LR
Q15 TRANS NPN MMBT2222A 40V 600mA SOT-23 3PIN PSI LR
<16,21> ENVDD
R1328 0Ω 5% 1/16W SMT0402 LR(NU)
<10,11,12,16,17,18,19,21,22,23,24,25,26,29,36,37,38,41,42,45,46,48,52> 3VDDM
<9,17,46> 1.5VDDM
<33,37> LID0
<16> ENBKL
<16> ENVEE
D77A D77B D77C
R1330 SHW 0 5% 1/16W 0402
R1329 0Ω 5% 1/16W SMT0402 LR(NU)
<23,25,26,52> SYSPWRGD
2.7KΩ 5% 1/16W SMT0402 LR R1429
R1288 6.8KΩ 1% 1/10W SMT0603 LR
Q121 M-FET-N FDN337N_NL 30V 2.2A SOT-23 FAIRCHILD LR
INVENA <52>
DIODE STKY CH731UPT 40V 0.03A SOT-457 6PIN CHENMKO LR
<8,13,23,24,25,26,36,45> 2.5VDDM
2.5VDDM
<10,11,12,16,17,18,19,21,22,23,24,25,26,29,36,37,38,41,42,45,46,48,52> 3VDDM
3VDDM
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
VA250 < Yonah + VN896 + VT8237A >
Size C
Document Number
<LVDS 1634AL>
Rev 0.3
Date: Sunday, December 10, 2006
Sheet 20 of 56



LVDS Interface

Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10" Cable MAX 16"	4 mils (stripline) 6 mils (microstrip)	20 mils 7 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to data) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils

<10,11,12,16,17,18,19,20,22,23,24,25,26,29,36,37,38,41,42,45,46,48,52> 3VDDM

3VDDM

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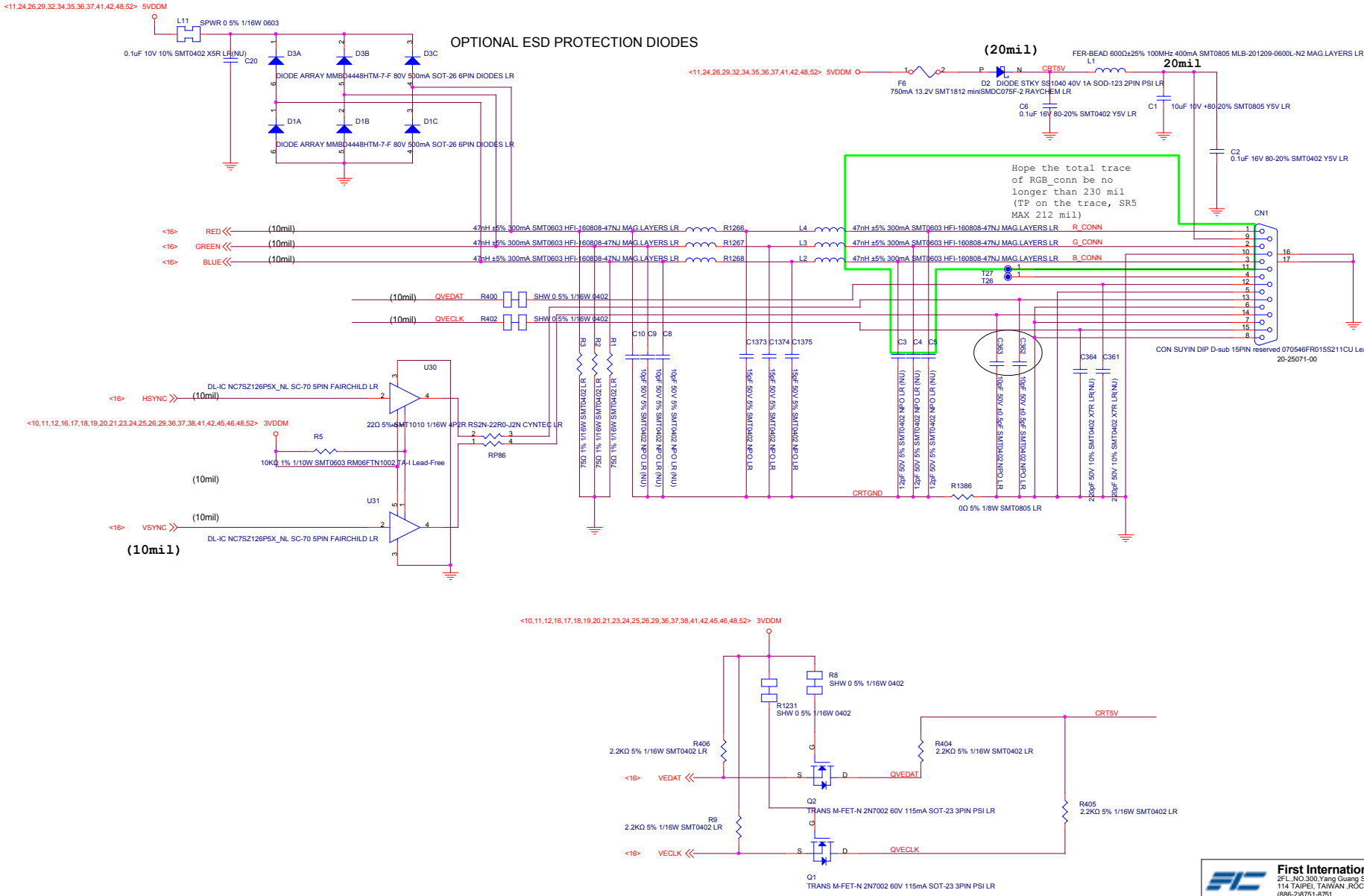
Title: VA250 < Yonah + VN896 + VT8237A >

Size: C | Document Number: <LCD connecter> | Rev: 0.4

Date: Sunday, December 10, 2006 | Sheet 21 of 56



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Title: VA250 < Yonah + VN896 + VT8237A >

Size	Document Number	Rev
C	<CRT connector>	0.4

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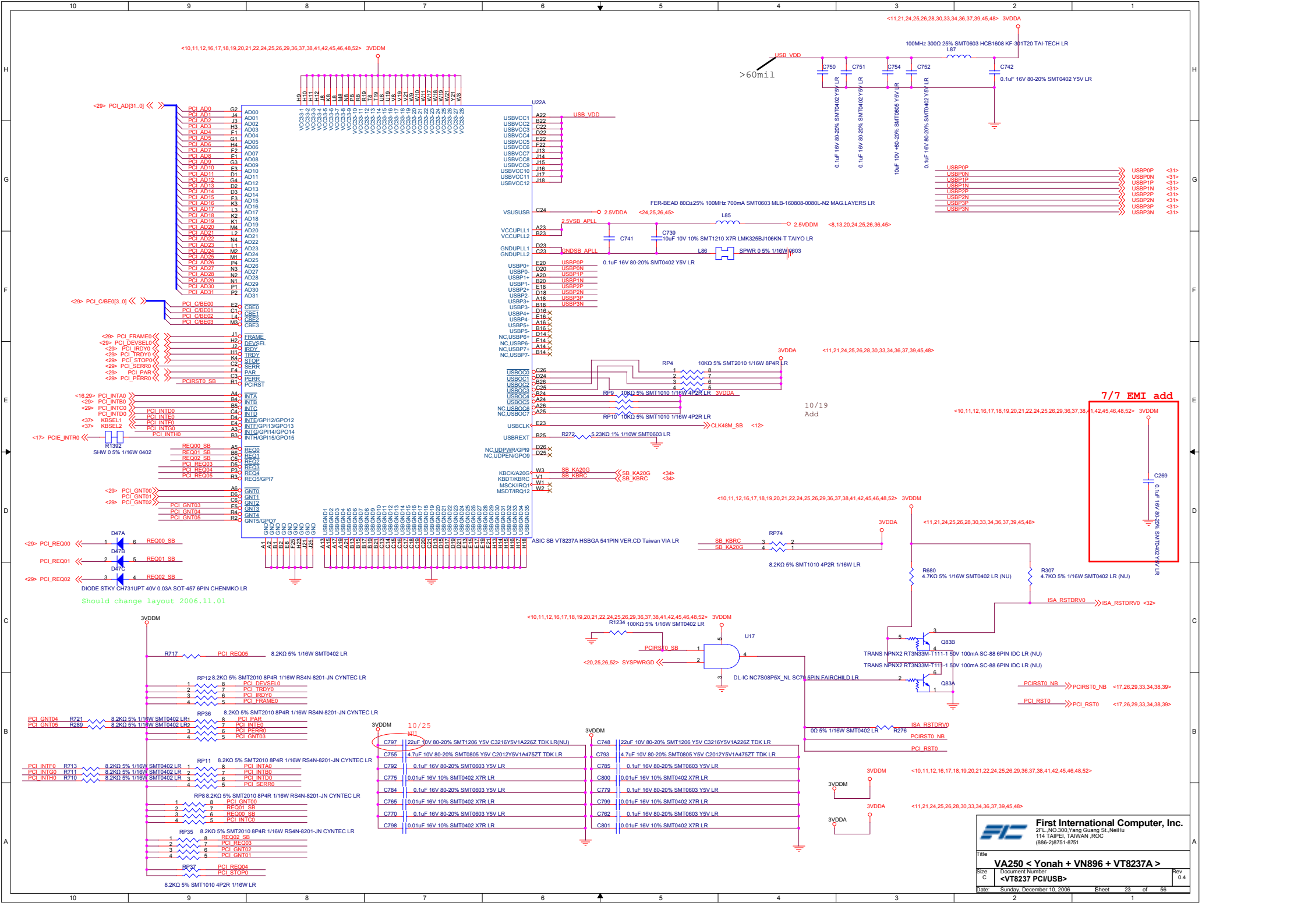
U22A
ASIC SB VT8237A HSBGA 541PIN VER:CD Taiwan VIA LR
DIODE STKY CH731UPT 40V 0.03A SOT-457 6PIN CHENMKO LR
SHW 0 5% 1/16W 0402
Should change layout 2006.11.01
10/19
Add
7/7 EMI add
10/25
NI
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
TRANS NPNX2 RT3N33M-T111-1 50V 100mA SC-88 6PIN IDC LR (NU)
FER-BEAD 80Ω±25% 100MHz 700mA SMT0603 MLB-160808-0080L-N2 MAG.LAYERS LR
100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR
First International Computer, Inc.
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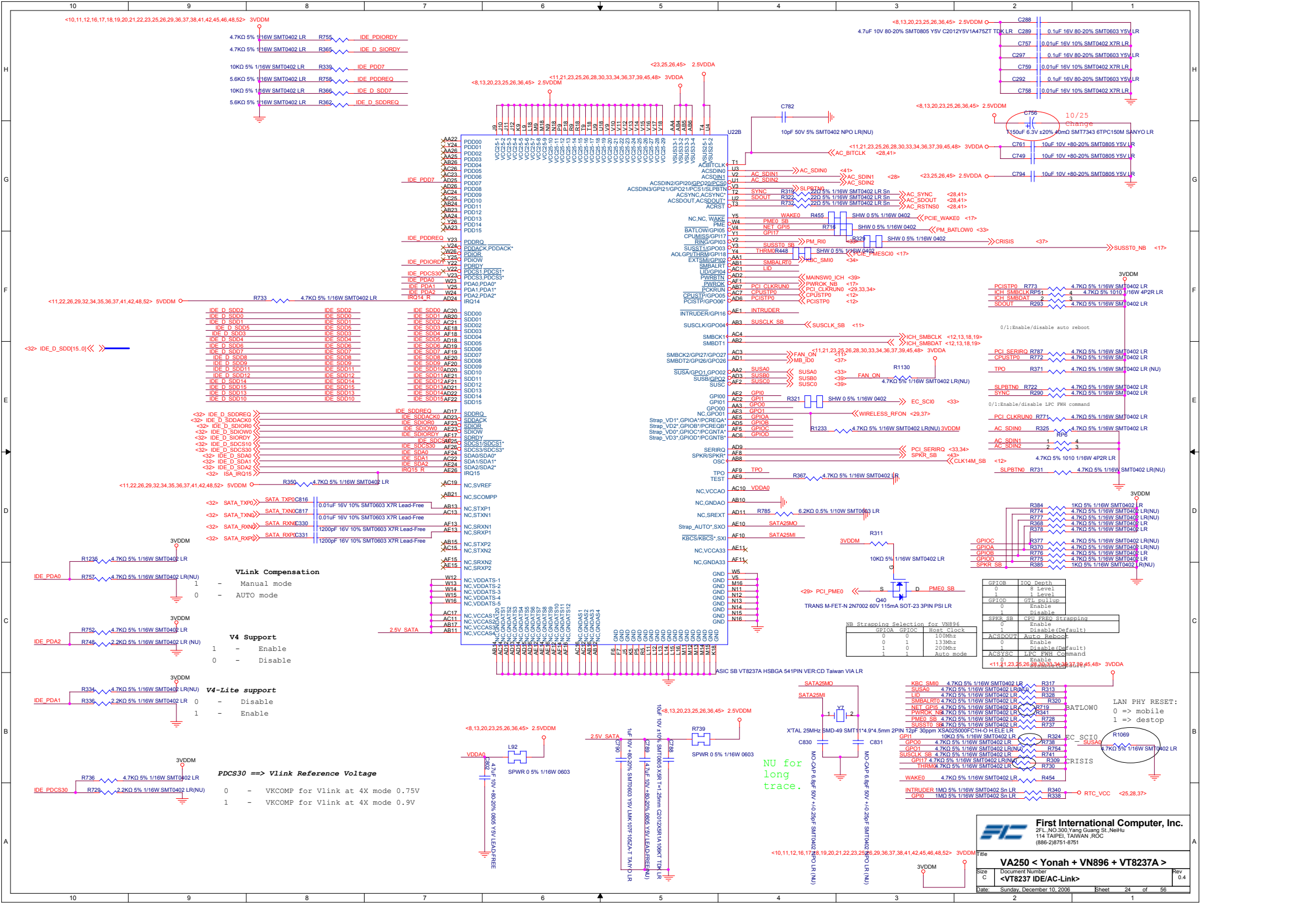
(886-2)8751-8751
VA250 < Yonah + VN896 + VT8237A >
<VT8237 PCI/USB>
Sunday, December 10, 2006


VLink Compensation
1 - Manual mode
0 - AUTO mode
V4 Support
1 - Enable
0 - Disable
V4-Lite support
1 - Enable
0 - Disable
PDCS30 ==> Vlink Reference Voltage
0 - VKCOMP for Vlink at 4X mode 0.75V
1 - VKCOMP for Vlink at 4X mode 0.9V
NB Strapping Selection for VN896
GPIOA GPIOC Host Clock
0 0 100Mhz
0 1 133Mhz
1 0 200Mhz
1 1 Auto mode
GPIOB IOQ Depth
0 8 Level
1 1 Level
GPIOD GTL pullup
0 Enable
1 Disable
SPKR_SB CPU FREQ Strapping
0 Enable
1 Disable(Default)
ACSDOUT Auto Reboot
0 Enable
1 Disable(Default)
ACSYSC LPC FWH Command
0 Enable
1 Disable(Default)
0/1:Enable/disable auto reboot
0/1:Enable/disable LPC FWH command
LAN PHY RESET:
0 => mobile
1 => destop
NU for long trace.
ASIC SB VT8237A HSBGA 541PIN VER:CD Taiwan VIA LR
First International Computer, Inc.
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VA250 < Yonah + VN896 + VT8237A >
Size C
Document Number <VT8237 IDE/AC-Link>
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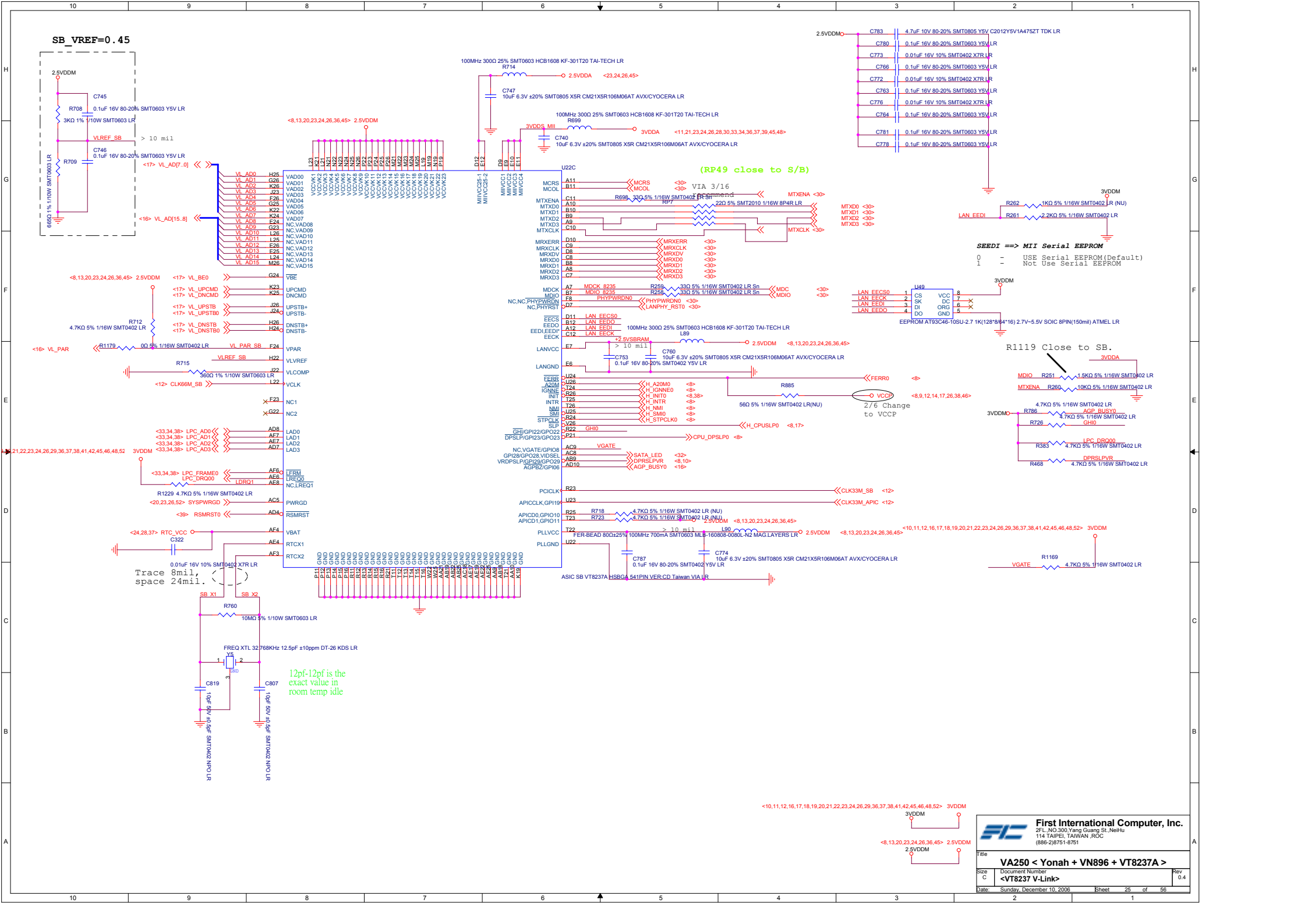
Date: Sunday, December 10, 2006
Sheet 24 of 56


SB_VREF=0.45
2.5VDDM
C745
R708 0.1uF 16V 80-20% SMT0603 Y5V LR
3KΩ 1% 1/10W SMT0603 LR
VLREF_SB
> 10 mil
C746 0.1uF 16V 80-20% SMT0603 Y5V LR
R709
665Ω 1% 1/10W SMT0603 LR
100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR
R714
2.5VDDA <23,24,26,45>
C747 10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/CYOCERA LR
100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR
R699
3VDDS_MII
3VDDA <11,21,23,24,26,28,30,33,34,36,37,39,45,48>
C740 10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/CYOCERA LR
<8,13,20,23,24,26,36,45> 2.5VDDM
C783 4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
C780 0.1uF 16V 80-20% SMT0603 Y5V LR
C773 0.01uF 16V 10% SMT0402 X7R LR
C766 0.1uF 16V 80-20% SMT0603 Y5V LR
C772 0.01uF 16V 10% SMT0402 X7R LR
C763 0.1uF 16V 80-20% SMT0603 Y5V LR
C776 0.01uF 16V 10% SMT0402 X7R LR
C764 0.1uF 16V 80-20% SMT0603 Y5V LR
C781 0.1uF 16V 80-20% SMT0603 Y5V LR
C778 0.1uF 16V 80-20% SMT0603 Y5V LR
U22C
(RP49 close to S/B)
VIA 3/16
recommend
R698 33Ω 5% 1/16W SMT0402 LR SI
RP7 22Ω 5% SMT2010 1/16W 8P4R LR
MTXENA <30>
MTXD0 <30>
MTXD1 <30>
MTXD2 <30>
MTXD3 <30>
MTXCLK <30>
3VDDM
R262 1KΩ 5% 1/16W SMT0402 LR (NU)
LAN_EEDI
R261 2.2KΩ 5% 1/16W SMT0402 LR
SEEDI ==> MII Serial EEPROM
0 - USE Serial EEPROM(Default)
1 - Not Use Serial EEPROM
U49
LAN_EECS0
LAN_EECK
LAN_EEDI
LAN_EEDO
CS VCC
SK DC
DI ORG
DO GND
EEPROM AT93C46-10SU-2.7 1K(128*8/64*16) 2.7V~5.5V SOIC 8PIN(150mil) ATMEL LR
R1119 Close to SB.
3VDDA
MDIO R251 1.5KΩ 5% 1/16W SMT0402 LR
MTXENA R260 10KΩ 5% 1/16W SMT0402 LR
R786 4.7KΩ 5% 1/16W SMT0402 LR
AGP_BUSY0
R726 4.7KΩ 5% 1/16W SMT0402 LR
GHI0
LPC_DRQ00
R383 4.7KΩ 5% 1/16W SMT0402 LR
DPRSLPVR
R468 4.7KΩ 5% 1/16W SMT0402 LR
<16> VL_AD[7..0]
<16> VL_AD[15..8]
VL_AD0 H25 VAD00
VL_AD1 G26 VAD01
VL_AD2 K26 VAD02
VL_AD3 J23 VAD03
VL_AD4 F26 VAD04
VL_AD5 G25 VAD05
VL_AD6 K22 VAD06
VL_AD7 K24 VAD07
VL_AD8 E24 NC,VAD08
VL_AD9 G23 NC,VAD09
VL_AD10 L26 NC,VAD10
VL_AD11 L25 NC,VAD11
VL_AD12 E26 NC,VAD12
VL_AD13 E25 NC,VAD13
VL_AD14 L24 NC,VAD14
VL_AD15 M26 NC,VAD15
<8,13,20,23,24,26,36,45> 2.5VDDM
<17> VL_BE0 G24 VBE
<17> VL_UPCMD K23 UPCMD
<17> VL_DNCMD K25 DNCMD
<17> VL_UPSTB J26 UPSTB+
<17> VL_UPSTB0 J24 UPSTB-
<17> VL_DNSTB H26 DNSTB+
<17> VL_DNSTB0 H24 DNSTB-
R712 4.7KΩ 5% 1/16W SMT0402 LR
<16> VL_PAR
R1179 0Ω 5% 1/16W SMT0402 LR
VL_PAR_SB F24 VPAR
VLREF_SB H22 VLVREF
R715 360Ω 1% 1/10W SMT0603 LR
J22 VLCOMP
<12> CLK66M_SB L22 VCLK
F23 NC1
G22 NC2
<33,34,38> LPC_AD0 AD8 LAD0
<33,34,38> LPC_AD1 AF7 LAD1
<33,34,38> LPC_AD2 AE7 LAD2
<33,34,38> LPC_AD3 AD7 LAD3
<21,22,23,24,26,29,36,37,38,41,42,45,46,48,52> 3VDDM
<33,34,38> LPC_FRAME0 AF6 LFRM
LPC_DRQ00 AE6 LREQ0
LDRQ1 AE8 NC,LREQ1
R1229 4.7KΩ 5% 1/16W SMT0402 LR
<20,23,26,52> SYSPWRGD AC5 PWRGD
<39> RSMRST0 AD4 RSMRST
<24,28,37> RTC_VCC AF4 VBAT
C322
AE4 RTCX1
AF3 RTCX2
0.01uF 16V 10% SMT0402 X7R LR
Trace 8mil, space 24mil.
SB_X1
SB_X2
R760 10MΩ 5% 1/10W SMT0603 LR
FREQ XTL 32.768KHz 12.5pF ±10ppm DT-26 KDS LR
Y5
C819 10pF 50V ±0.5pF SMT0402 NPO LR
C807 10pF 50V ±0.5pF SMT0402 NPO LR
12pf-12pf is the exact value in room temp idle
MCRS A11 MCRS <30>
MCOL B11 MCOL <30>
MTXENA C11
MTXD0 A10
MTXD1 B10
MTXD2 B9
MTXD3 A9
MTXCLK C10
MRXERR D10 MRXERR <30>
MRXCLK C9 MRXCLK <30>
MRXDV D8 MRXDV <30>
MRXD0 C8 MRXD0 <30>
MRXD1 B8 MRXD1 <30>
MRXD2 A8 MRXD2 <30>
MRXD3 C7 MRXD3 <30>
MDCK A7 MDCK_8235 R259 33Ω 5% 1/16W SMT0402 LR Sn MDC <30>
MDIO B7 MDIO_8235 R258 33Ω 5% 1/16W SMT0402 LR Sn MDIO <30>
NC,NC,PHYPWRDN F8 PHYPWRDN0 PHYPWRDN0 <30>
NC,PHYRST D7 LANPHY_RST0 <30>
EECS D11 LAN_EECS0
EEDO B12 LAN_EEDO
EEDI,EEDI* A12 LAN_EEDI
EECK C12 LAN_EECK
100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR
LANVCC E7
+2.5VSBRAM
> 10 mil
L89
2.5VDDM <8,13,20,23,24,26,36,45>
C753 0.1uF 16V 80-20% SMT0402 Y5V LR
C760 10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/CYOCERA LR
LANGND E6
FERR U24 FERR0 <8>
A20M U26
IGNNE T24 H_IGNNE0 <8>
INIT R26 H_INIT0 <8,38>
INTR T25 H_INTR <8>
NMI T26 H_NMI <8>
SMI U25 H_SMI0 <8>
STPCLK R24 H_STPCLK0 <8>
SLP V26
GHI/GPI22/GPO22 R22 GHI0
DPSLP/GPI23/GPO23 P21 CPU_DPSLP0 <8>
R885
56Ω 5% 1/16W SMT0402 LR(NU)
VCCP <8,9,12,14,17,26,38,46>
2/6 Change to VCCP
NC,VGATE/GPIO8 AC9 VGATE
GPI28/GPO28,VIDSEL AC8 SATA_LED <32>
VRDPSLP/GPI29/GPO29 AB9 DPRSLPVR <8,10>
AGPBZ/GPIO6 AD10 AGP_BUSY0 <16>
PCICLK R23 CLK33M_SB <12>
APICCLK,GPI19 U23 CLK33M_APIC <12>
APICD0,GPIO10 R25 R718 4.7KΩ 5% 1/16W SMT0402 LR (NU)
APICD1,GPIO11 T23 R723 4.7KΩ 5% 1/16W SMT0402 LR (NU)
2.5VDDM <8,13,20,23,24,26,36,45>
PLLVCC T22
> 10 mil
L90
FER-BEAD 80Ω±25% 100MHz 700mA SMT0603 MLB-160808-0080L-N2 MAG.LAYERS LR
2.5VDDM <8,13,20,23,24,26,36,45>
<10,11,12,16,17,18,19,20,21,22,23,24,26,29,36,37,38,41,42,45,46,48,52> 3VDDM
PLLGND U22
C787 0.1uF 16V 80-20% SMT0402 Y5V LR
C774 10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/CYOCERA LR
ASIC SB VT8237A HSBGA 541PIN VER:CD Taiwan VIA LR
R1169
VGATE 4.7KΩ 5% 1/16W SMT0402 LR
<10,11,12,16,17,18,19,20,21,22,23,24,26,29,36,37,38,41,42,45,46,48,52> 3VDDM
3VDDM
<8,13,20,23,24,26,36,45> 2.5VDDM
2.5VDDM
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
VA250 < Yonah + VN896 + VT8237A >
Size C
Document Number <VT8237 V-Link>
Rev 0.4
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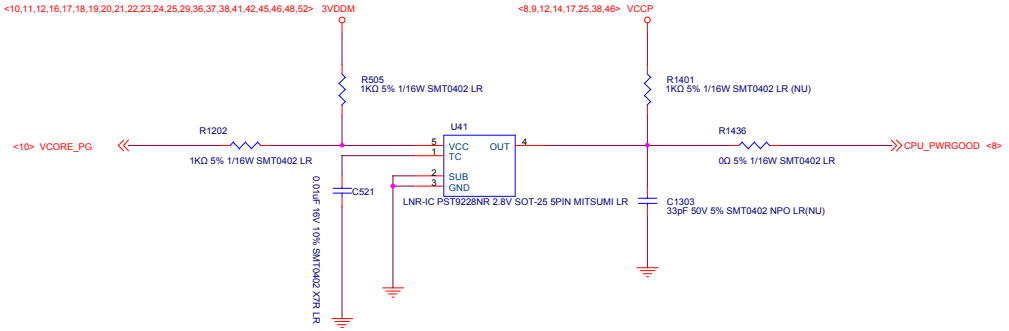
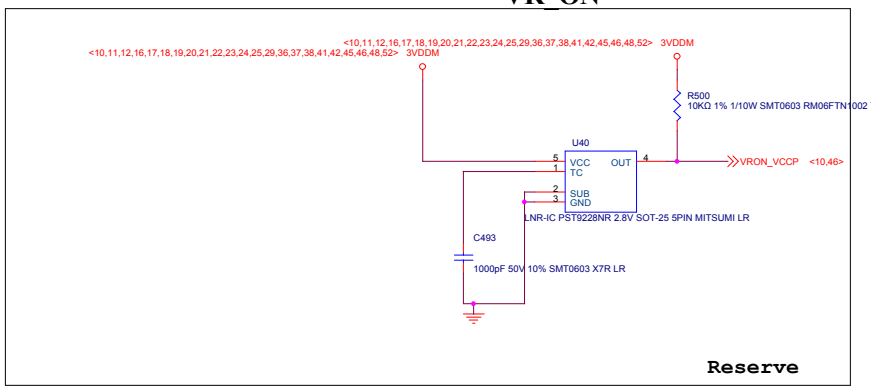
Sheet 25 of 56

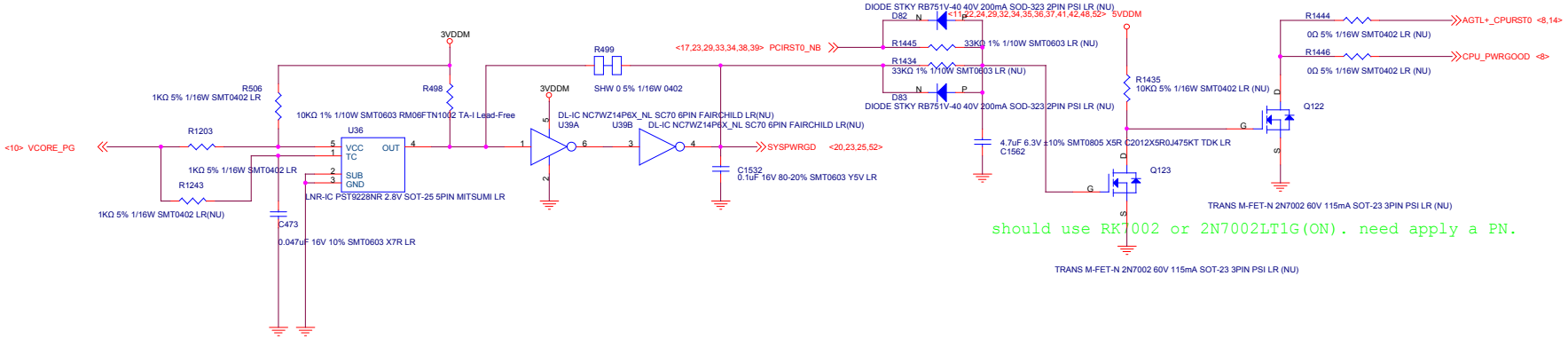
CPU POWER OK CIRCUIT



VR_ON



SYSTEM POWER OK CIRCUIT



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Title	VA250 < Yonah + VN896 + VT8237A >	
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Title

VA250 < VIA VN896 + VT8237A >

Size	Document Number	Rev
C	**< Blank>**	0.4

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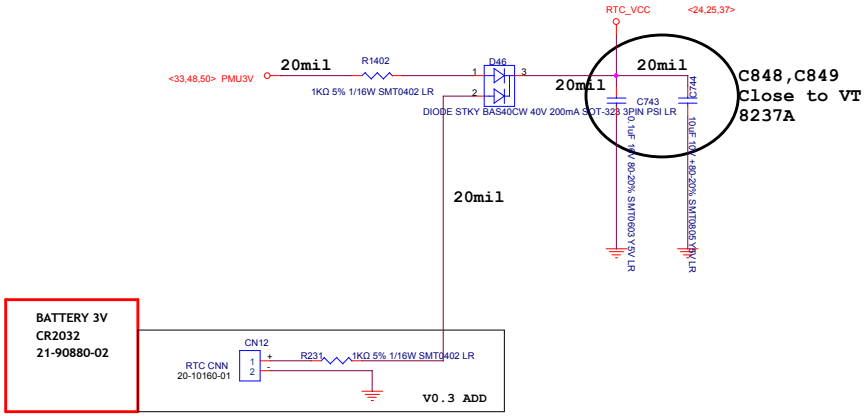
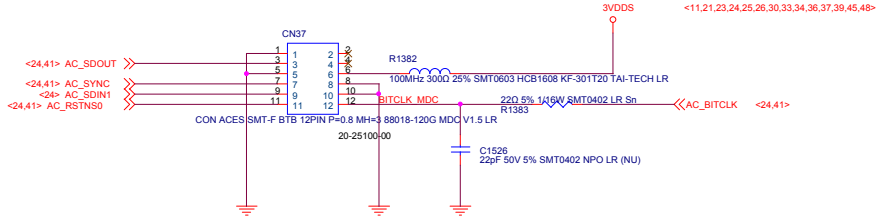
RTC Discharge Circuit



MDC CNN



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Title	VA250 < Yonah + VN896 + VT8237A >	
Size: C	Document Number: < CardBus Power/CNN >	Rev: 0.4
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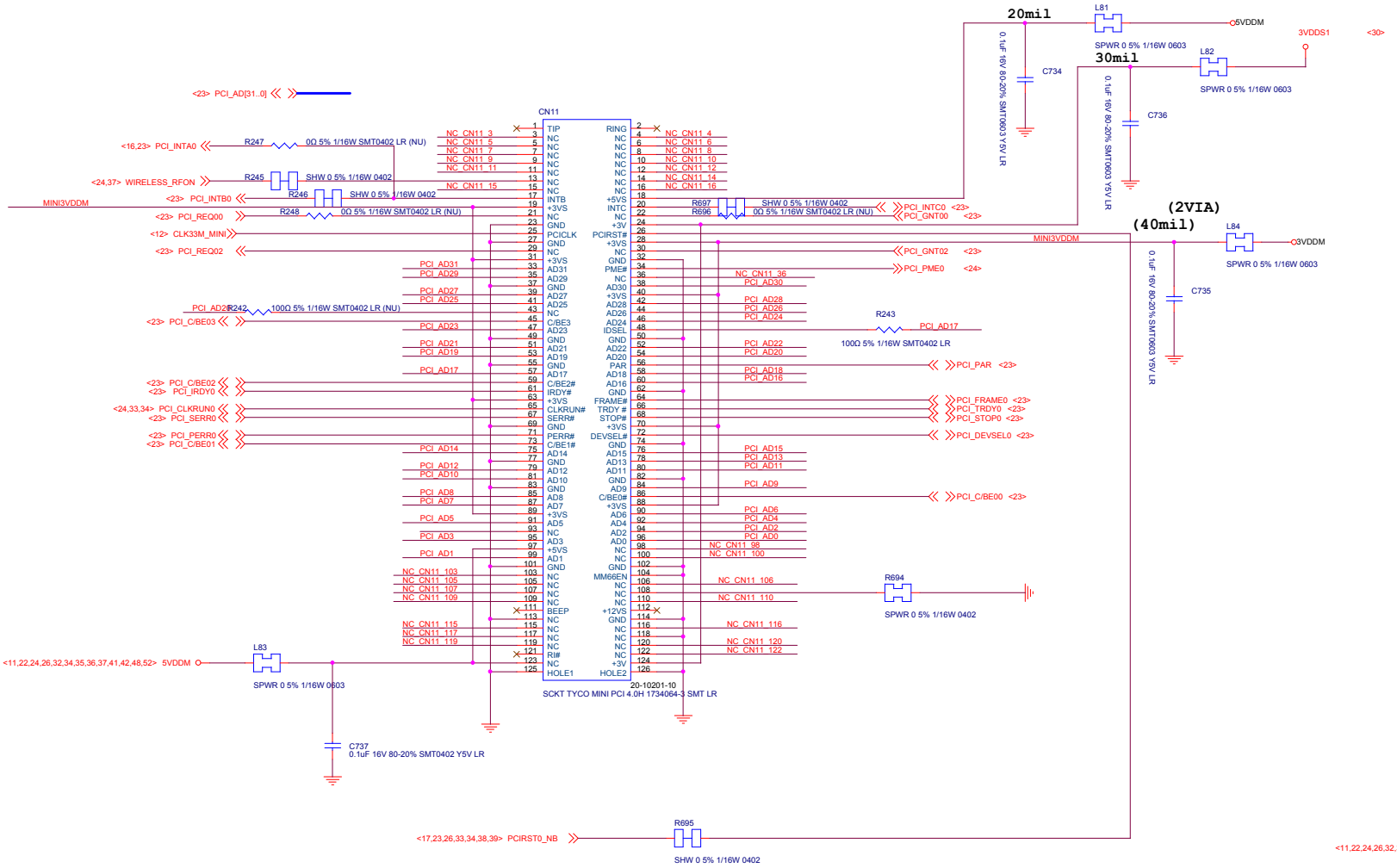
TYPE III MODEM / LAN CONNECTOR



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Title	VA250 < Yonah + VN896 + VT8237A >	
Size C	Document Number <Mini-PCI>	Rev 0.4
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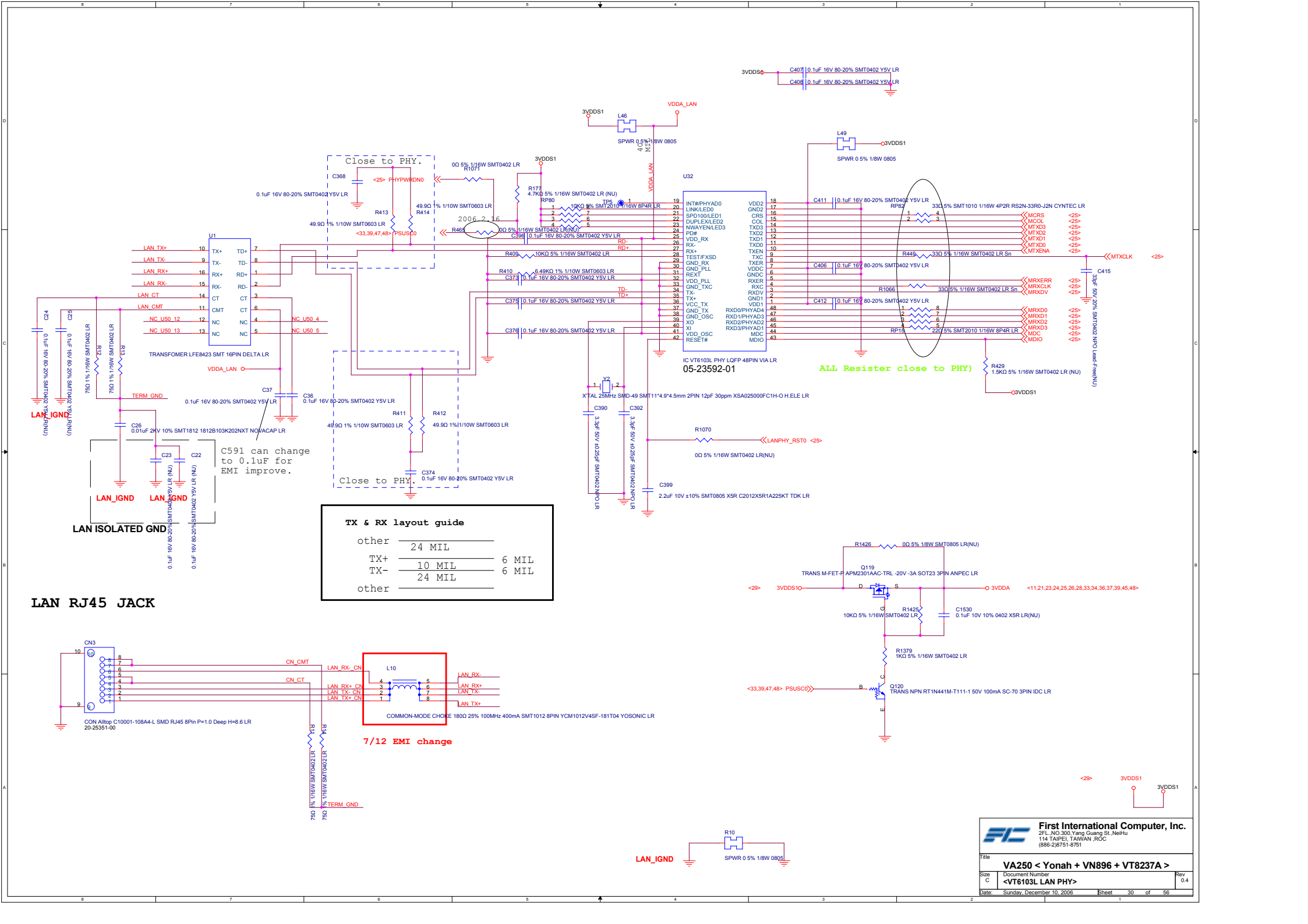
Close to PHY.
U1
TRANSFOMER LFE8423 SMT 16PIN DELTA LR
U32
IC VT6103L PHY LQFP 48PIN VIA LR
05-23592-01
ALL Resister close to PHY)
X'TAL 25MHz SMD-49 SMT11*4.9*4.5mm 2PIN 12pF 30ppm XSA025000FC1H-O H.ELE LR
C591 can change to 0.1uF for EMI improve.
LAN ISOLATED GND
LAN_IGND
TERM_GND
VDDA_LAN
3VDDS1
LAN RJ45 JACK
CON Alltop C10001-108A4-L SMD RJ45 8Pin P=1.0 Deep H=8.6 LR
20-25351-00
COMMON-MODE CHOKE 180Ω 25% 100MHz 400mA SMT1012 8PIN YCM1012V4SF-181T04 YOSONIC LR
7/12 EMI change
TX & RX layout guide
other 24 MIL
TX+ 6 MIL
TX- 10 MIL 6 MIL
other 24 MIL
Q119
TRANS M-FET-P APM2301AAC-TRL -20V -3A SOT23 3PIN ANPEC LR
Q120
TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
First International Computer, Inc.
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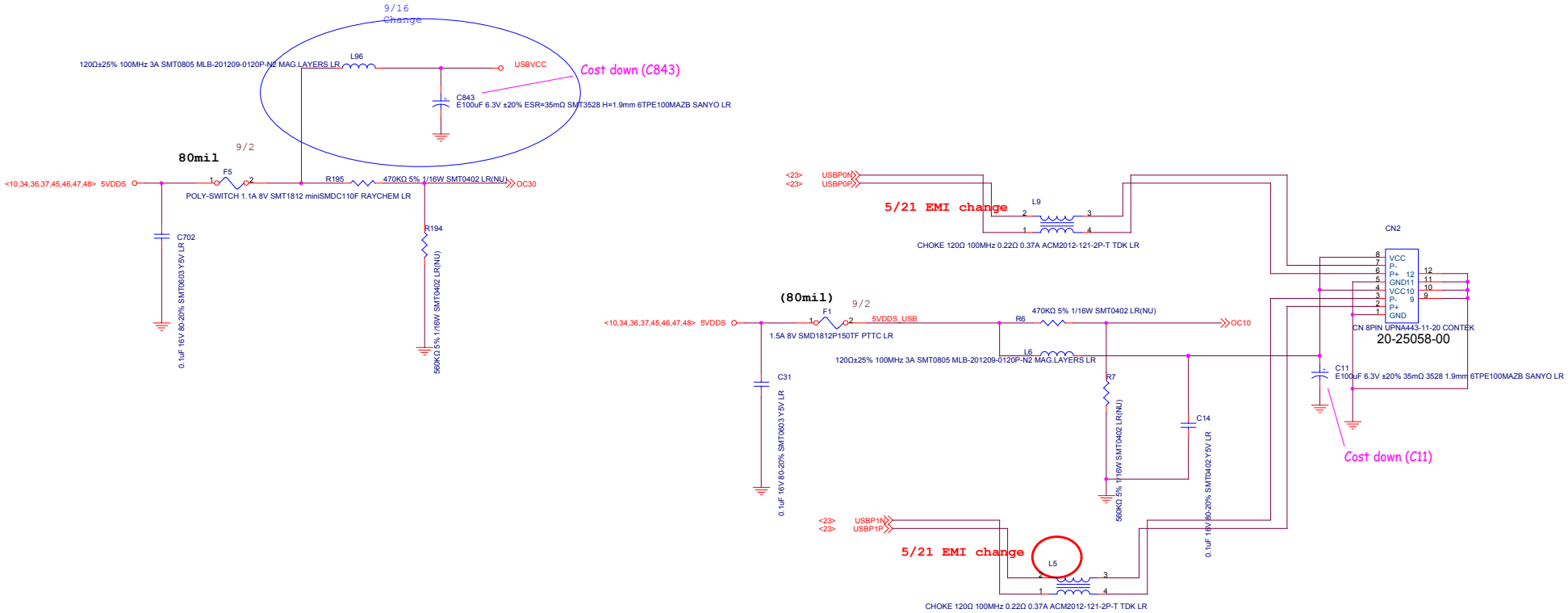
VA250 < Yonah + VN896 + VT8237A >
<VT6103L LAN PHY>
Sunday, December 10, 2006



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Title	VA250 < Yonah + VN896 + VT8237A >
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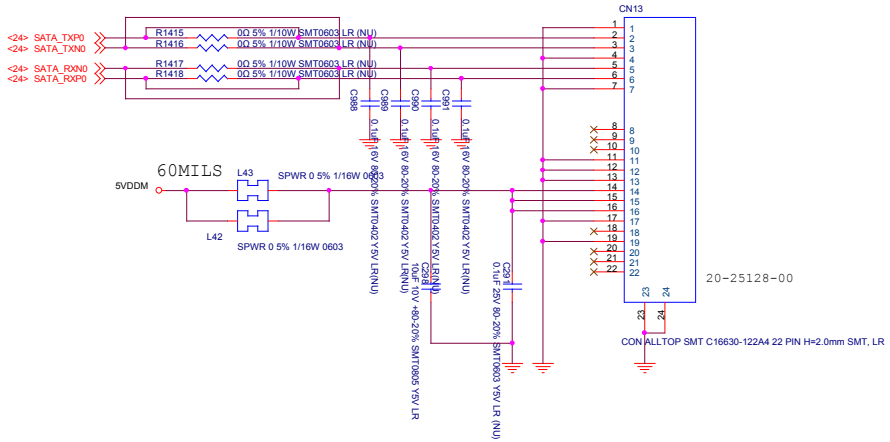
NOTE

SATA differential stripline 20:4:7:7:4:20
SATA differential mircostripline 20:5:7:5:20
請包GROUND



SATA Layout Note:

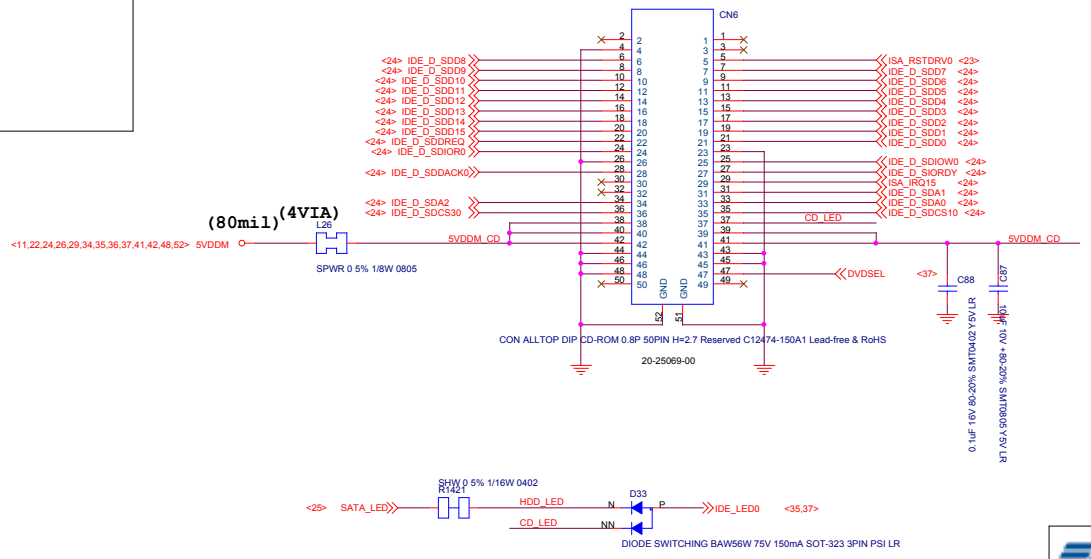
MS or SL:

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN



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Title: VA250 < Yonah + VN896 + VT8237A >

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PMU08

CLOSE TO PIN 1 OF PMU08

ATTENTION

IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79

GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT

C116 change to X5R

C105, C110 change to X5R

down size (C120)

For abnormal

MAIN BATTERY VOLTAGE SENSE

pull up at SB

pull up at SB

Mark REM 3月30日 請擺在上層

ASIC PMU08A MIT MASK M38857M8-A09HP LQFP(80P6Q-A) 80PIN MITSUBISHI LR

APL5151-33BC-TRL 3.3V 150mA SOT-23-5 ANPEC LR

LNR-IC PST9228NR 2.8V SOT-25 5PIN MITSUMI LR

4.19MHz 3PIN 15pF ±5000ppm CSTCC4M19G53-R0 MURATA LR

DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR

TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR

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Title: VA250 < Yonah + VN896 + VT8237A >

Size: C | Document Number: <LPC PMU08> | Rev: 0.4

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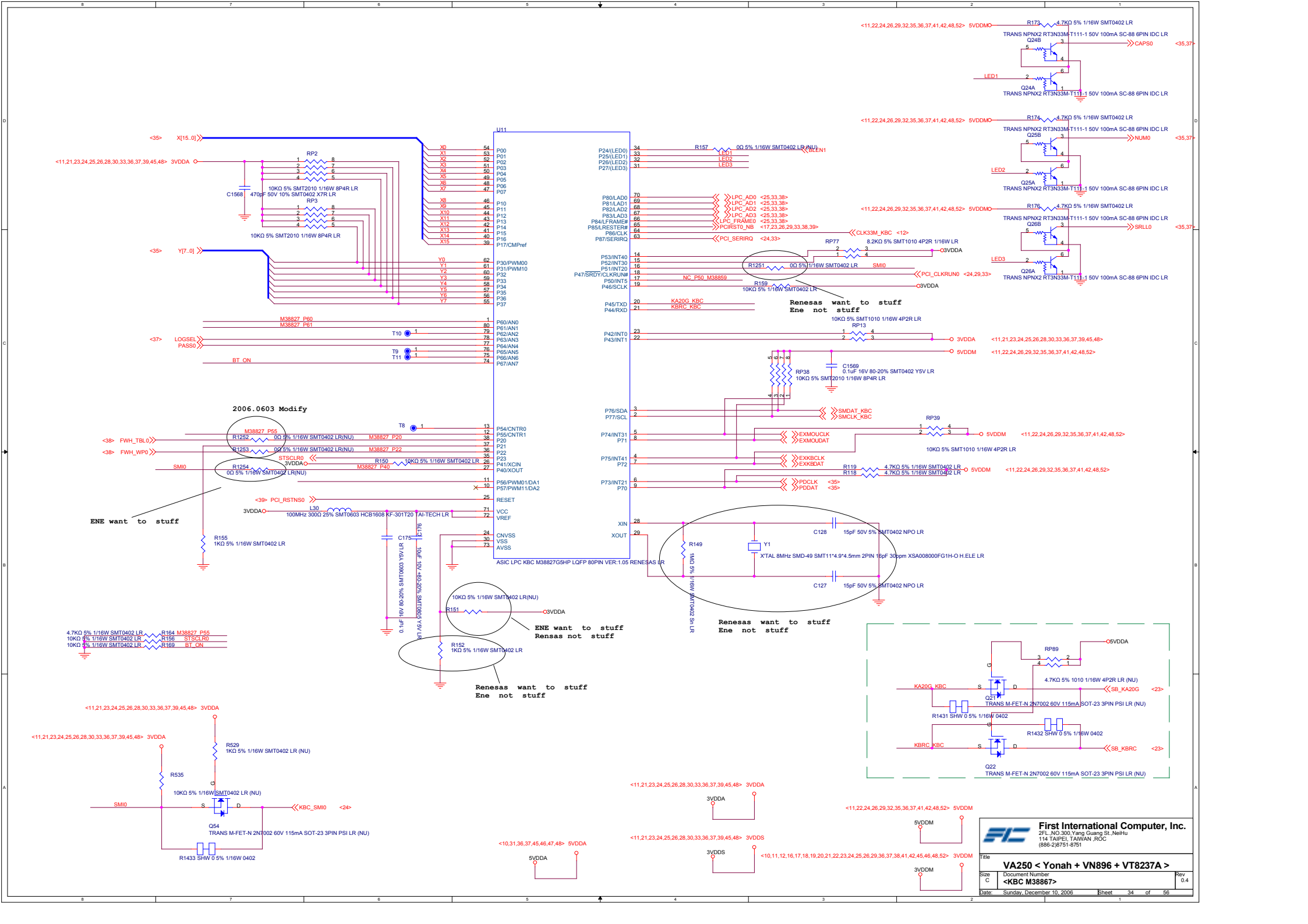
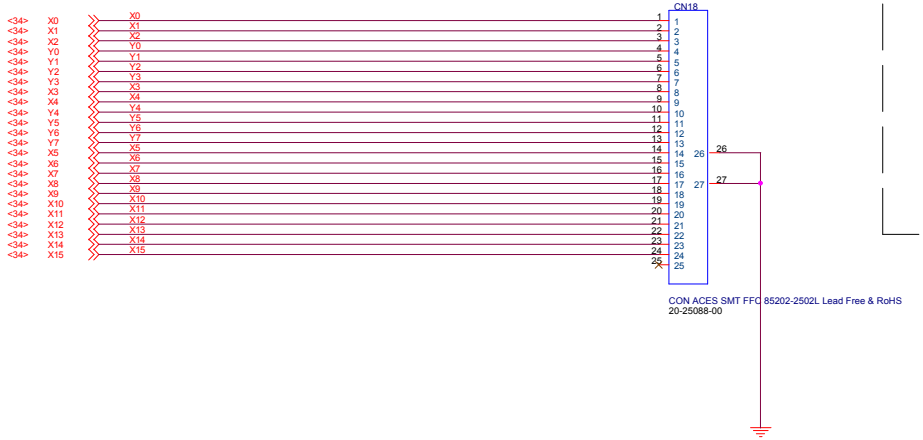
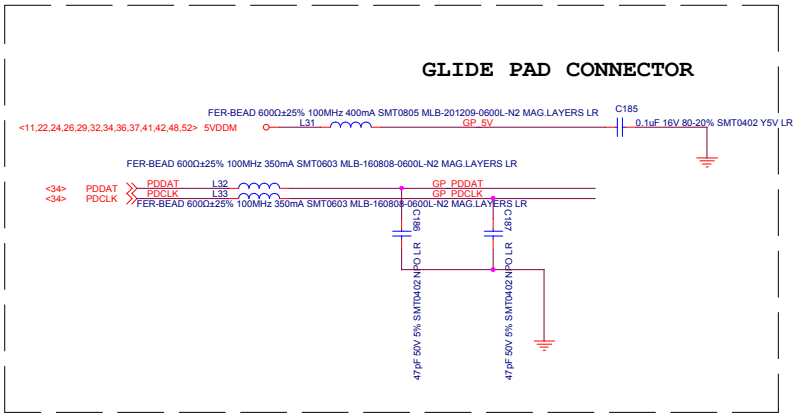
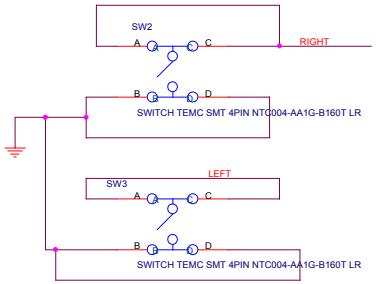

U11
ASIC LPC KBC M38827G5HP LQFP 80PIN VER:1.05 RENESAS LR
2006.0603 Modify
ENE want to stuff
Renesas want to stuff
Ene not stuff
Renesas want to stuff
Rensas not stuff
Renesas want to stuff
Ene not stuff
Renesas want to stuff
Ene not stuff
X'TAL 8MHz SMD-49 SMT11*4.9*4.5mm 2PIN 18pF 30ppm XSA008000FG1H-O H.ELE LR
TRANS NPNX2 RT3N33M-T111-1 50V 100mA SC-88 6PIN IDC LR
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR (NU)
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
VA250 < Yonah + VN896 + VT8237A >
<KBC M38867>
Sunday, December 10, 2006

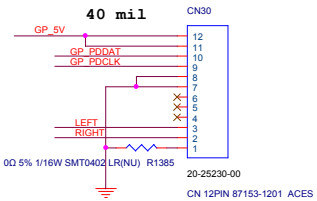
INT KB CNN



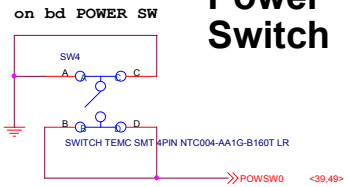
GLIDE PAD CONNECTOR

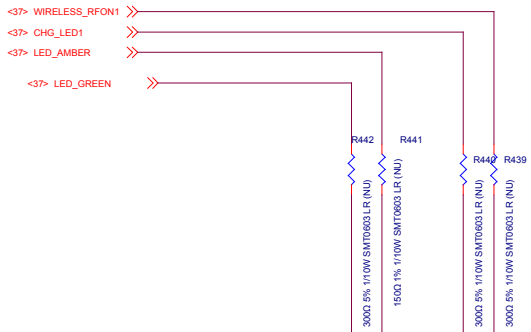


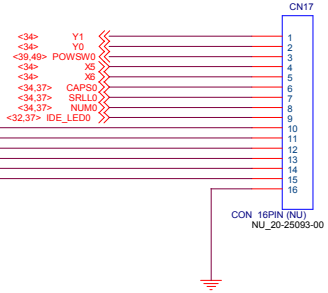




Power Switch

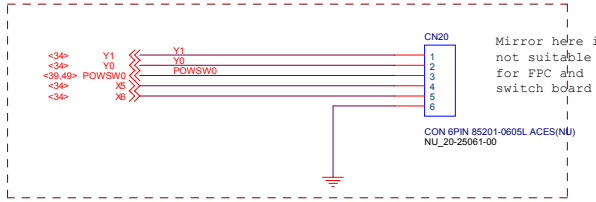






switch board con ID3

switch board con ID2



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Title	VA250 < Yonah + VN896 + VT8237A >	
Size C	Document Number <INT K/B /GP/SW CNN>	Rev 0.4
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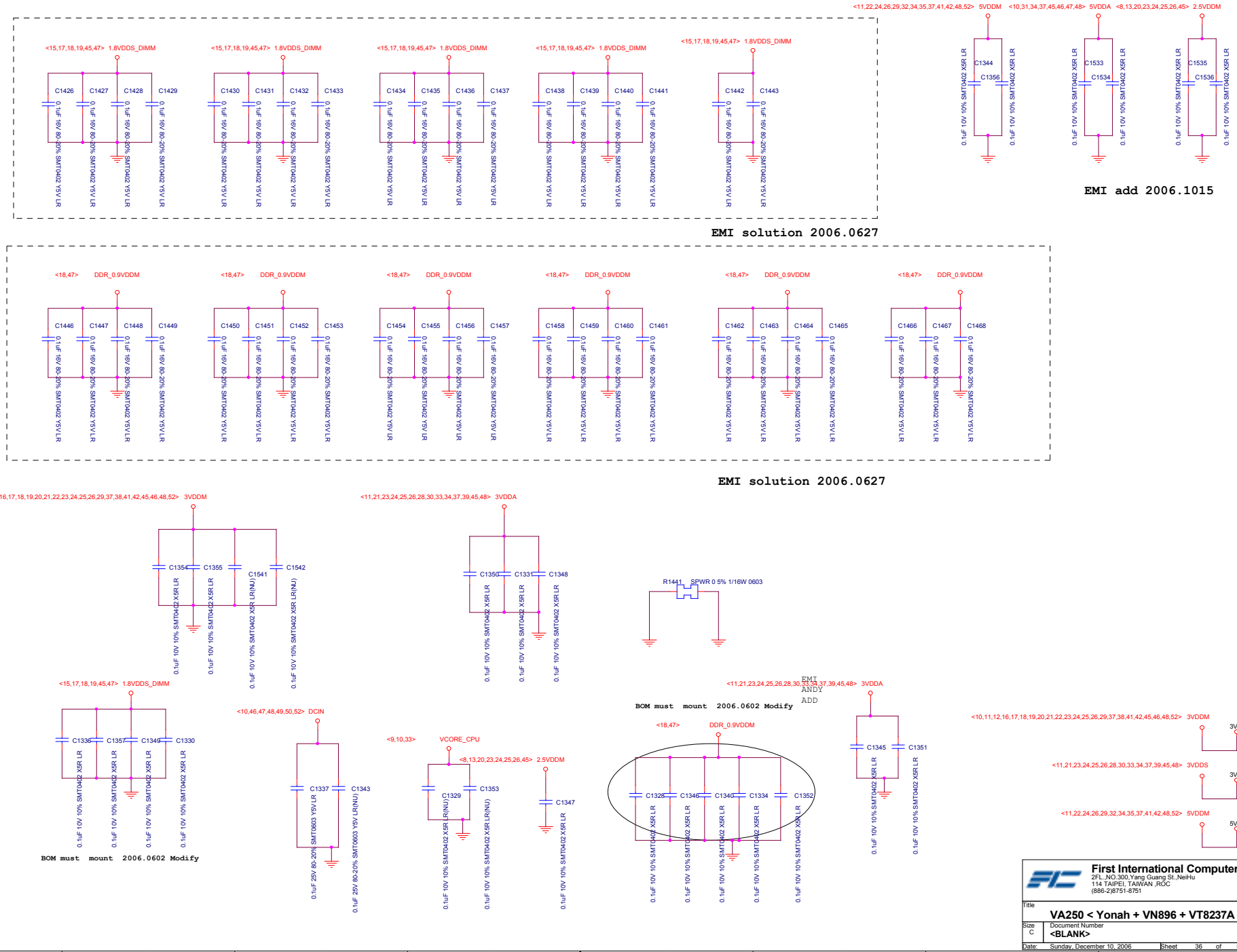
<15,17,18,19,45,47> 1.8VDDS_DIMM
C1426 C1427 C1428 C1429
C1430 C1431 C1432 C1433
C1434 C1435 C1436 C1437
C1438 C1439 C1440 C1441
C1442 C1443
0.1uF 16V 80-20% SMT0402 Y5V LR
EMI solution 2006.0627
<11,22,24,26,29,32,34,35,37,41,42,48,52> 5VDDM
<10,31,34,37,45,46,47,48> 5VDDA
<8,13,20,23,24,25,26,45> 2.5VDDM
C1344 C1356
C1533 C1534
C1535 C1536
0.1uF 10V 10% SMT0402 X5R LR
EMI add 2006.1015
<18,47> DDR_0.9VDDM
C1446 C1447 C1448 C1449
C1450 C1451 C1452 C1453
C1454 C1455 C1456 C1457
C1458 C1459 C1460 C1461
C1462 C1463 C1464 C1465
C1466 C1467 C1468
0.1uF 16V 80-20% SMT0402 Y5V LR
EMI solution 2006.0627
<10,11,12,16,17,18,19,20,21,22,23,24,25,26,29,37,38,41,42,45,46,48,52> 3VDDM
C1354 C1355 C1541 C1542
0.1uF 10V 10% SMT0402 X5R LR
0.1uF 10V 10% SMT0402 X5R LR(NU)
<11,21,23,24,25,26,28,30,33,34,37,39,45,48> 3VDDA
C1350 C1331 C1348
R1441 SPWR 0 5% 1/16W 0603
<15,17,18,19,45,47> 1.8VDDS_DIMM
C1336 C1357 C1349 C1330
BOM must mount 2006.0602 Modify
<10,46,47,48,49,50,52> DCIN
C1337 C1343
0.1uF 25V 80-20% SMT0603 Y5V LR
0.1uF 25V 80-20% SMT0603 Y5V LR(NU)
<9,10,33> VCORE_CPU
<8,13,20,23,24,25,26,45> 2.5VDDM
C1329 C1353 C1347
0.1uF 10V 10% SMT0402 X5R LR(NU)
EMI ANDY ADD
BOM must mount 2006.0602 Modify
C1328 C1346 C1340 C1334 C1352
C1345 C1351
<10,11,12,16,17,18,19,20,21,22,23,24,25,26,29,37,38,41,42,45,46,48,52> 3VDDM
<11,21,23,24,25,26,28,30,33,34,37,39,45,48> 3VDDS
<11,22,24,26,29,32,34,35,37,41,42,48,52> 5VDDM
First International Computer, Inc.
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(886-2)8751-8751
Title
VA250 < Yonah + VN896 + VT8237A >
Size C
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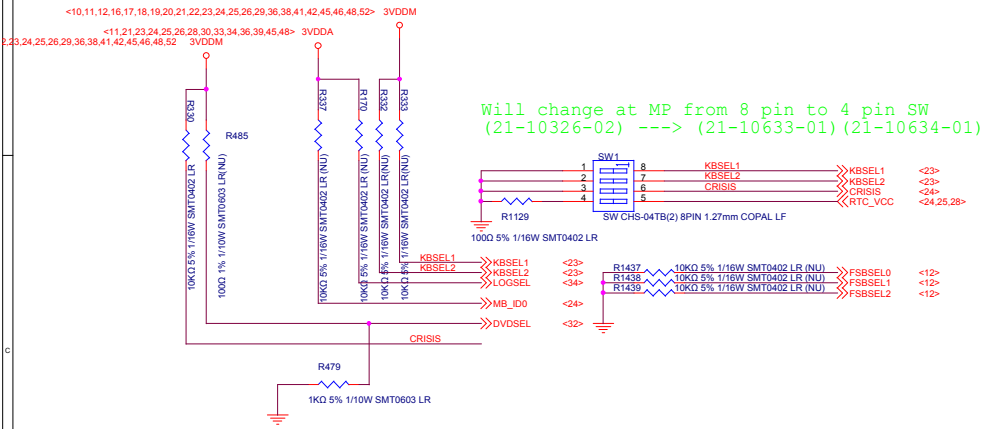
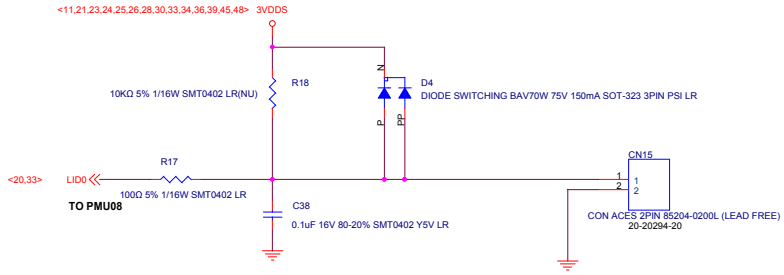
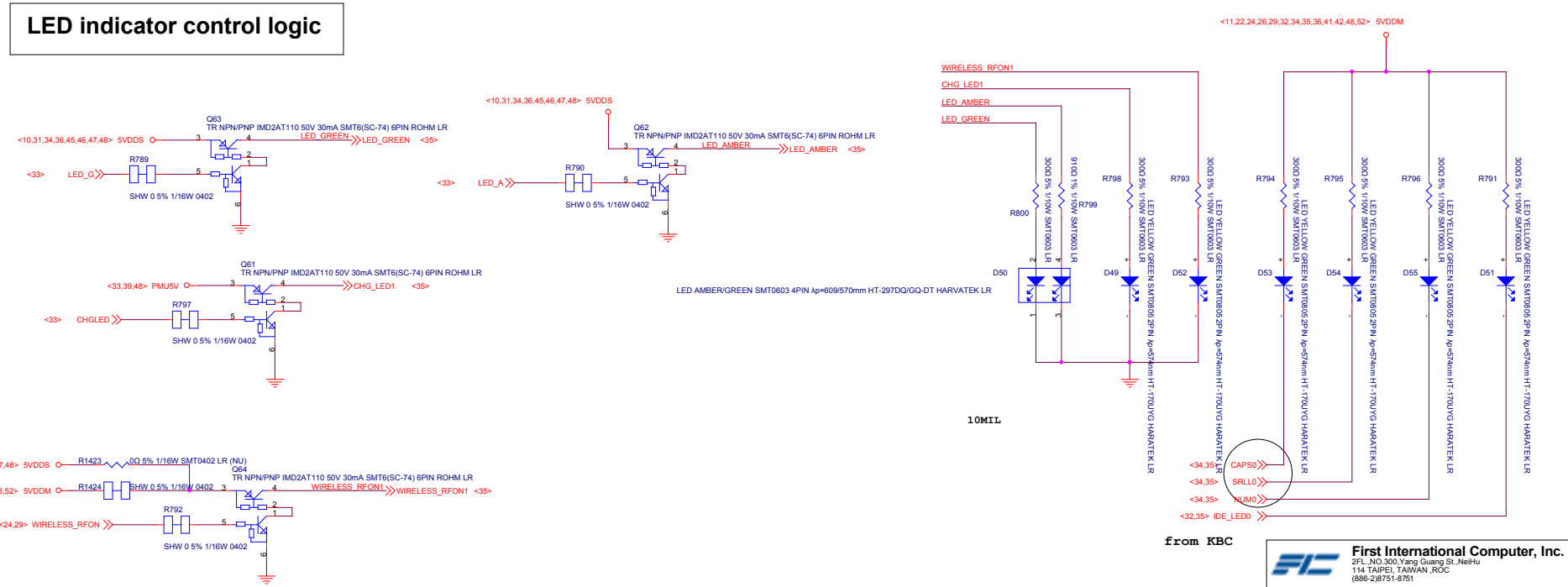
DIP SWITCH



LID Switch



LED indicator control logic



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Title	VA250 < VIA VN896 + VT8237A >	
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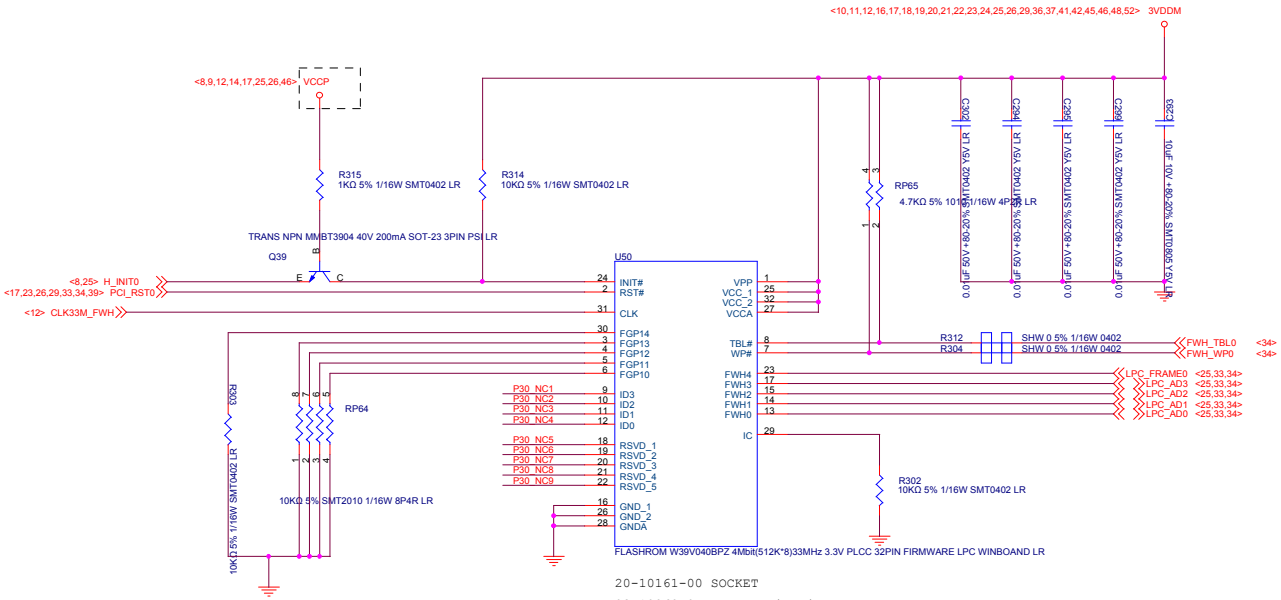
4M FLASH ROM



20-10161-00 SOCKET

03-10262-04 LPC BIOSic winbond

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(886-2)8751-8751		
Title	VA250 < Yonah + VN896 + VT8237A >	
Size C	Document Number <LID SW/ BIOS>	Rev 0.4
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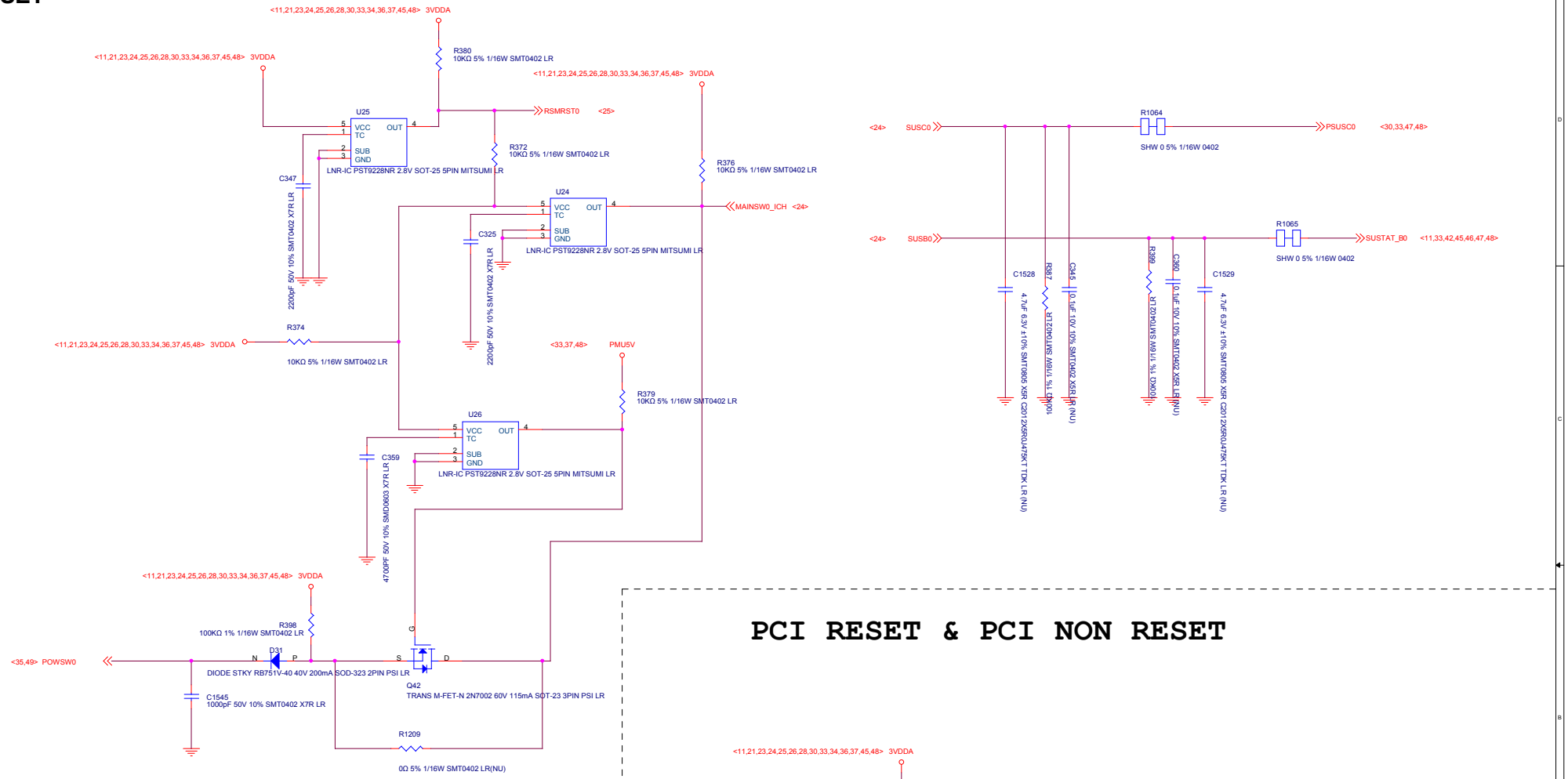
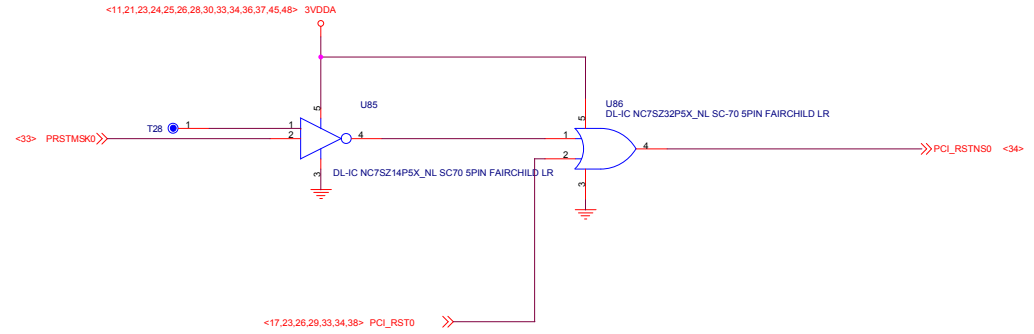
RESUME RESET



PCI RESET & PCI NON RESET



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Title	VA250 < Yonah + VN896 + VT8237A >	
Size: C	Document Number: <Reset Circuit>	Rev: 0.4
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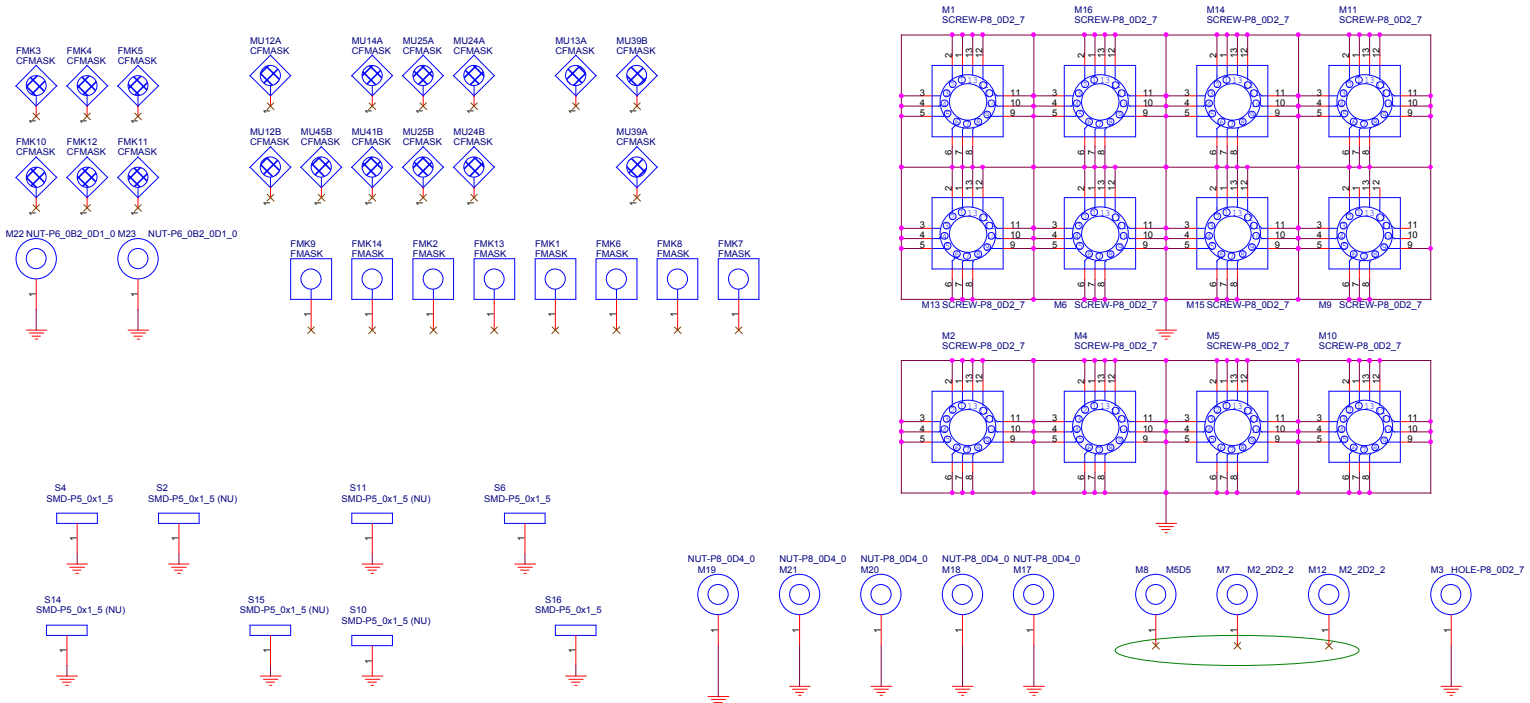
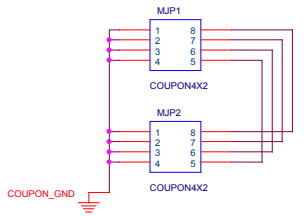


COUPON4X2



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Title: **VA250 < Yonah + VN896 + VT8237A >**

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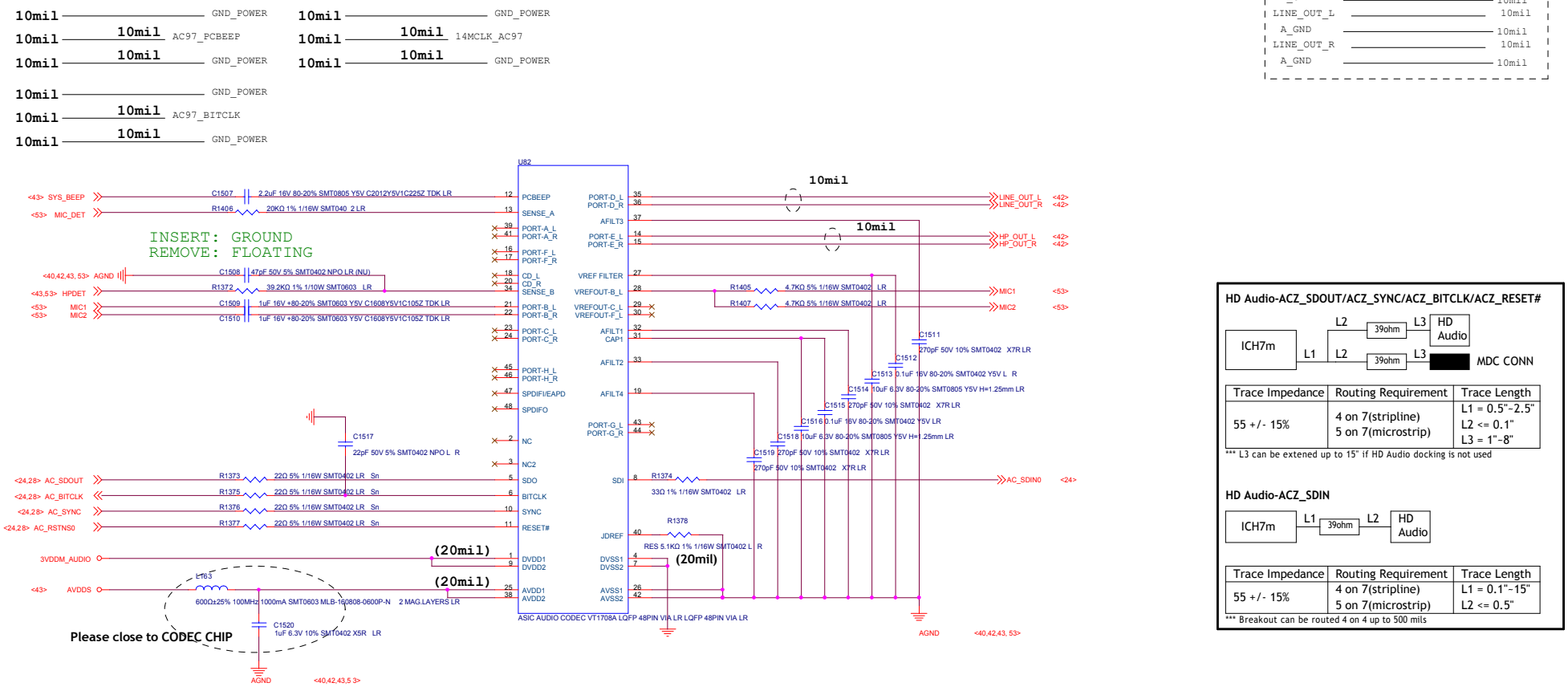

AZALIA CODEC POWER

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
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(886-2)87 51-8751

Title: VA250W/D < VIA C7 + VN896 + VT8237A >
Size: C | Document Number: VA250 < Yonah + VN896 + VT8237A > | Rev: 0.4
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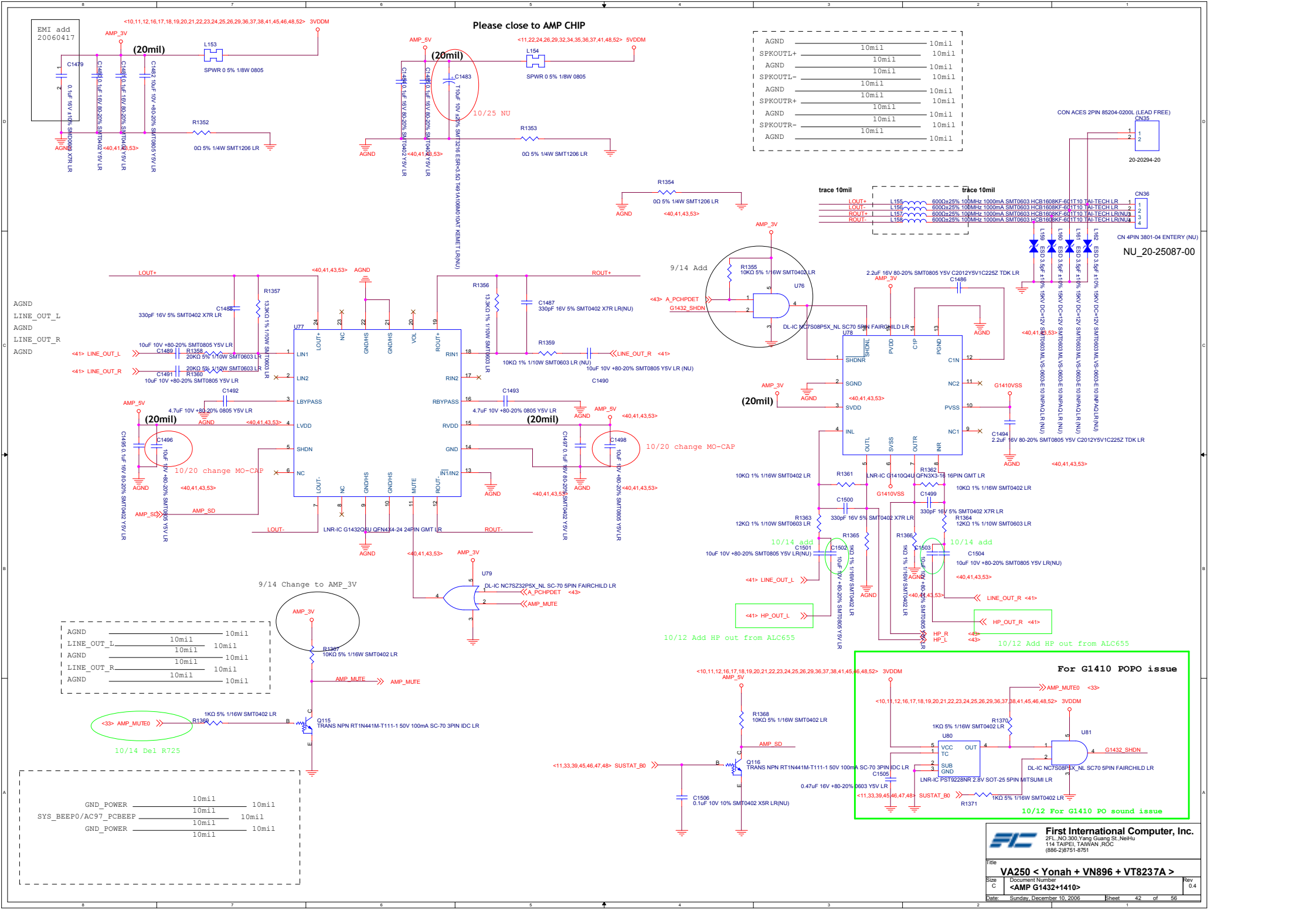
EMI add 20060417
Please close to AMP CHIP
(20mil)
10/25 NU
SPWR 0 5% 1/8W 0805
0Ω 5% 1/4W SMT1206 LR
AGND
AMP_3V
AMP_5V
3VDDM
5VDDM
L153
L154
C1479
C1480 0.1uF 16V 80-20% SMT0402 Y5V LR
C1481 0.1uF 16V 80-20% SMT0402 Y5V LR
C1482 10uF 10V +80-20% SMT0805 Y5V LR
C1483 T10uF 10V +20% SMT3216 ESR=3.5Ω T491A106M010AT KEMET LR(NU)
C1484 0.1uF 16V 80-20% SMT0402 Y5V LR
C1485 0.1uF 16V 80-20% SMT0402 Y5V LR
R1352
R1353
R1354
AGND 10mil 10mil
SPKOUTL+ 10mil 10mil
AGND 10mil 10mil
SPKOUTL- 10mil 10mil
AGND 10mil 10mil
SPKOUTR+ 10mil 10mil
AGND 10mil 10mil
SPKOUTR- 10mil 10mil
AGND 10mil 10mil
CON ACES 2PIN 85204-0200L (LEAD FREE)
CN35
20-20294-20
CN36
CN 4PIN 3801-04 ENTERY (NU)
NU_20-25087-00
trace 10mil
L155 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
L156 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
L157 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR(NU)
L158 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR(NU)
L159 ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR (NU)
L160 ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR (NU)
L161 ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR (NU)
L162 ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR (NU)
AGND
LINE_OUT_L
AGND
LINE_OUT_R
AGND
LOUT+
ROUT+
LOUT-
ROUT-
U77
LNR-IC G1432GSU QFN4X4-24 24PIN GMT LR
C1488 330pF 16V 5% SMT0402 X7R LR
C1487 330pF 16V 5% SMT0402 X7R LR(NU)
C1490
R1357 13.3KΩ 1% 1/10W SMT0603 LR
R1356 13.3KΩ 1% 1/10W SMT0603 LR
R1358 20KΩ 5% 1/10W SMT0603 LR
R1359 10KΩ 1% 1/10W SMT0603 LR (NU)
R1360 20KΩ 5% 1/10W SMT0603 LR
C1489 10uF 10V +80-20% SMT0805 Y5V LR
C1491 10uF 10V +80-20% SMT0805 Y5V LR
C1492 4.7uF 10V +80-20% 0805 Y5V LR
C1493 4.7uF 10V +80-20% 0805 Y5V LR
C1496 10uF 10V +80-20% SMT0805 Y5V LR
C1497 0.1uF 16V 80-20% SMT0402 Y5V LR
C1498 10uF 10V +80-20% SMT0805 Y5V LR
10/20 change MO-CAP
<41> LINE_OUT_L
<41> LINE_OUT_R
LINE_OUT_R <41>
AMP_SD
9/14 Add
U76
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
<43> A_PCHPDET
G1432_SHDN
R1355 10KΩ 5% 1/16W SMT0402 LR
U78
LNR-IC G1410Q4U QFN3X3-16 16PIN GMT LR
2.2uF 16V 80-20% SMT0805 Y5V C2012Y5V1C225Z TDK LR
C1486
C1494 2.2uF 16V 80-20% SMT0805 Y5V C2012Y5V1C225Z TDK LR
G1410VSS
R1361 10KΩ 1% 1/16W SMT0402 LR
R1362 10KΩ 1% 1/16W SMT0402 LR
C1499 330pF 16V 5% SMT0402 X7R LR
C1500 330pF 16V 5% SMT0402 X7R LR
R1363 12KΩ 1% 1/10W SMT0603 LR
R1364 12KΩ 1% 1/10W SMT0603 LR
R1365 1KΩ 1% 1/16W SMT0402 LR
R1366 1KΩ 1% 1/16W SMT0402 LR
C1501 10uF 10V +80-20% SMT0805 Y5V LR(NU)
C1502 10uF 10V +80-20% SMT0805 Y5V LR
C1503 10uF 10V +80-20% SMT0805 Y5V LR
C1504 10uF 10V +80-20% SMT0805 Y5V LR(NU)
10/14 add
<41> HP_OUT_L
HP_OUT_R <41>
HP_R <43>
HP_L <43>
10/12 Add HP out from ALC655
9/14 Change to AMP_3V
U79
DL-IC NC7SZ32P5X_NL SC-70 5PIN FAIRCHILD LR
A_PCHPDET <43>
AMP_MUTE
R1367 10KΩ 5% 1/16W SMT0402 LR
R1369 1KΩ 5% 1/16W SMT0402 LR
<33> AMP_MUTE0
Q115 TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
10/14 Del R725
GND_POWER 10mil 10mil
SYS_BEEP0/AC97_PCBEEP 10mil 10mil
GND_POWER 10mil 10mil
For G1410 POPO issue
<10,11,12,16,17,18,19,20,21,22,23,24,25,26,29,36,37,38,41,45,46,48,52> 3VDDM
AMP_MUTE0 <33>
R1368 10KΩ 5% 1/16W SMT0402 LR
R1370 1KΩ 5% 1/16W SMT0402 LR
U80
U81
Q116 TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
<11,33,39,45,46,47,48> SUSTAT_B0
C1505 0.47uF 16V +80-20% 0603 Y5V LR
C1506 0.1uF 10V 10% SMT0402 X5R LR(NU)
LNR-IC PST9228NR 2.8V SOT-25 5PIN MITSUMI LR
R1371 1KΩ 5% 1/16W SMT0402 LR
10/12 For G1410 PO sound issue
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
VA250 < Yonah + VN896 + VT8237A >
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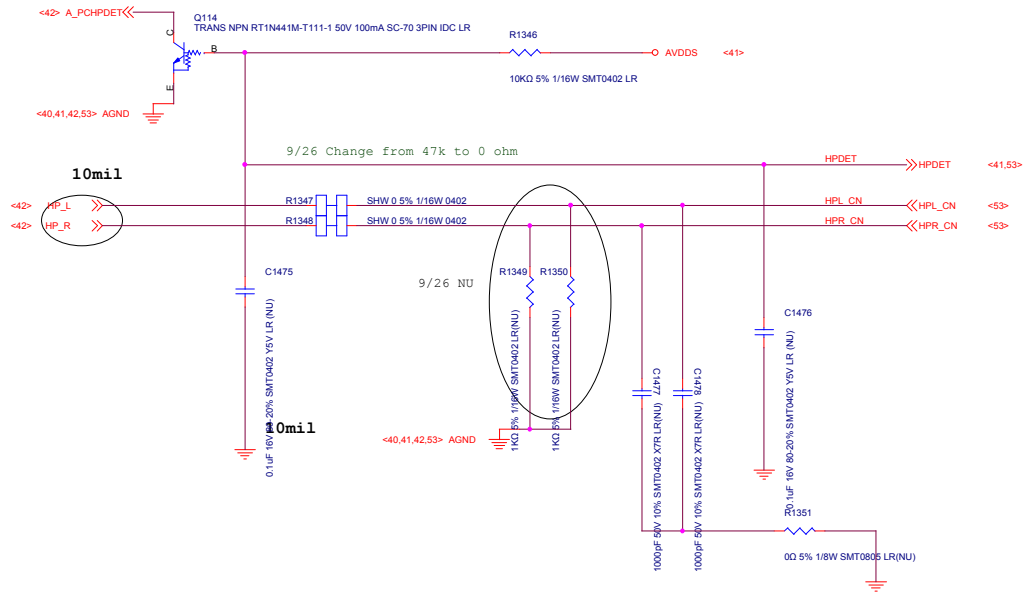
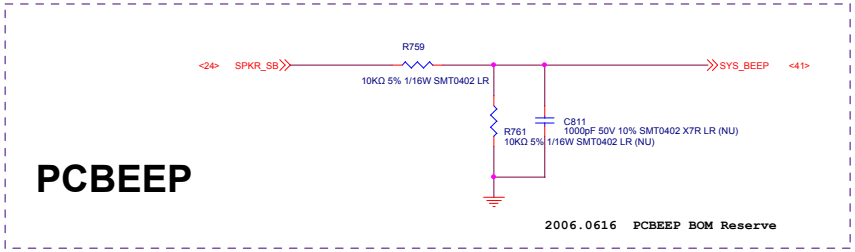
Normal=LOW
Headphone insert=High



2006.7.6 Cancel Audio CONN



<11,22,24,26,29,32,34,35,36,37,41,42,48,52> 5VDDM
5VDDM

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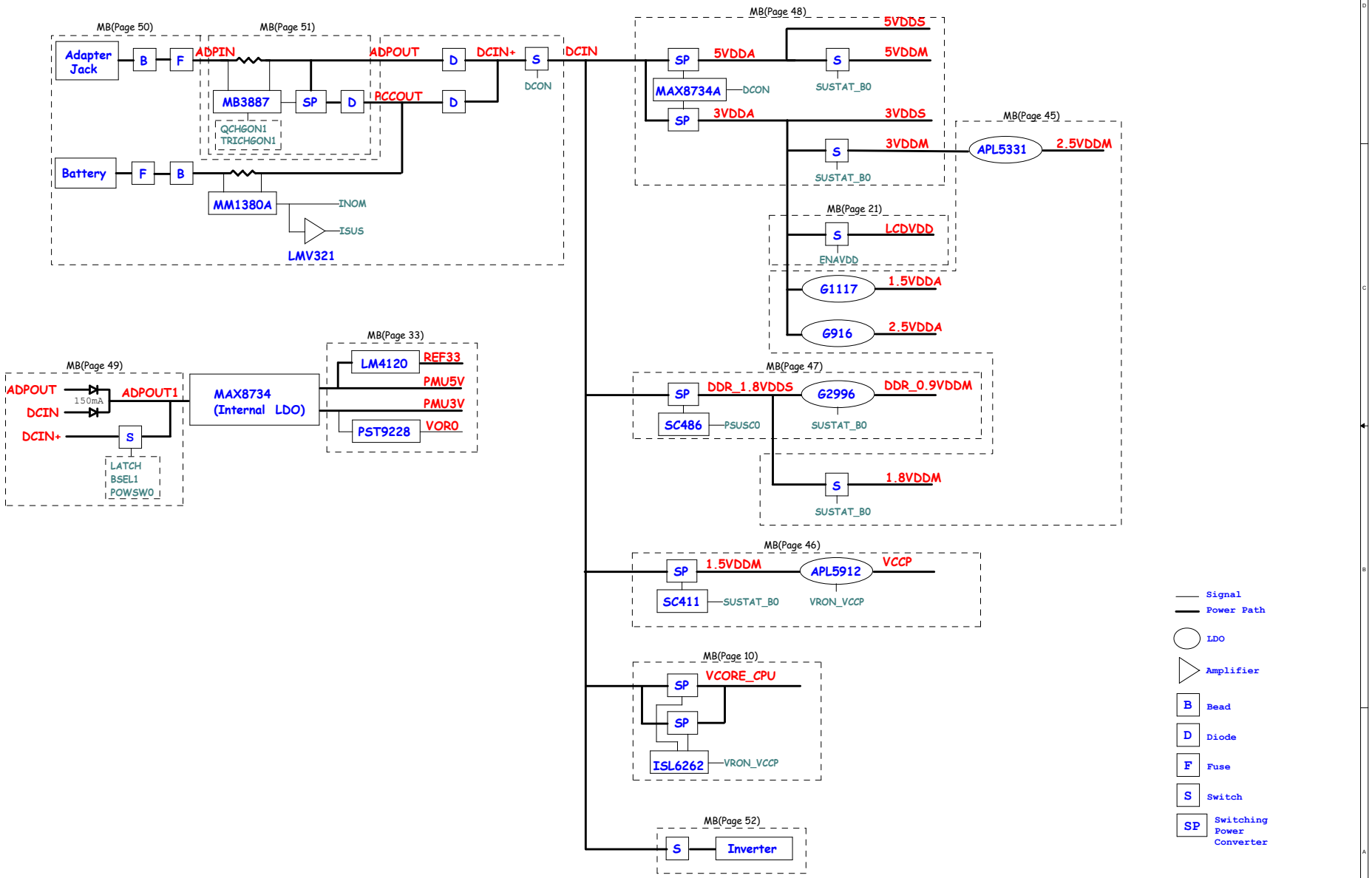
VA250 Power Block



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Title: VA250 < Yonah + VN896 + VT8237A >

Size: C | Document Number: <POWER BLOCK> | Rev: 0.4

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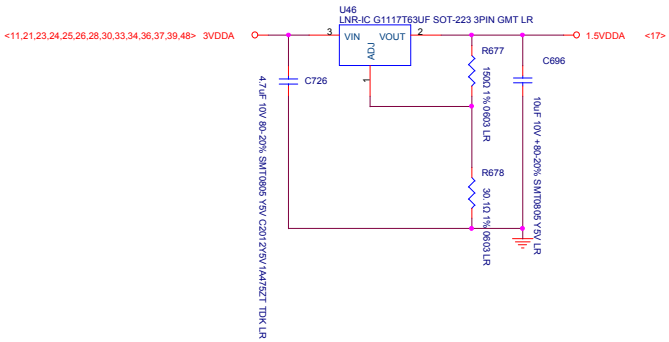
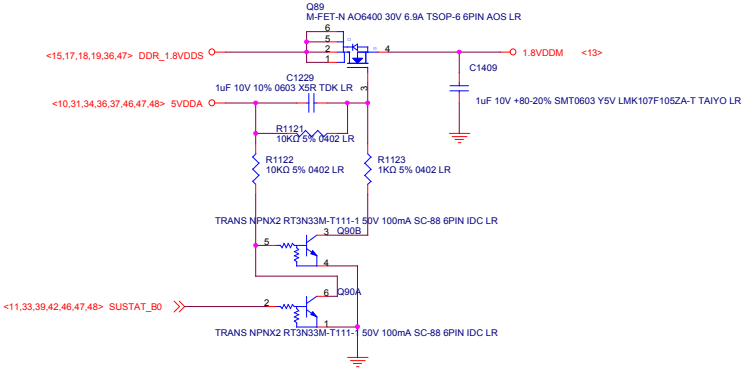
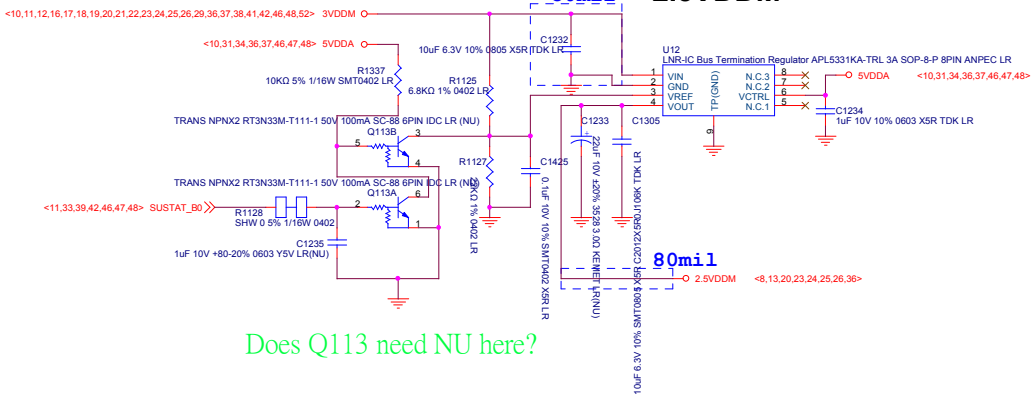
1.5VDDA 0.5A



1.8VDDM 1.5A

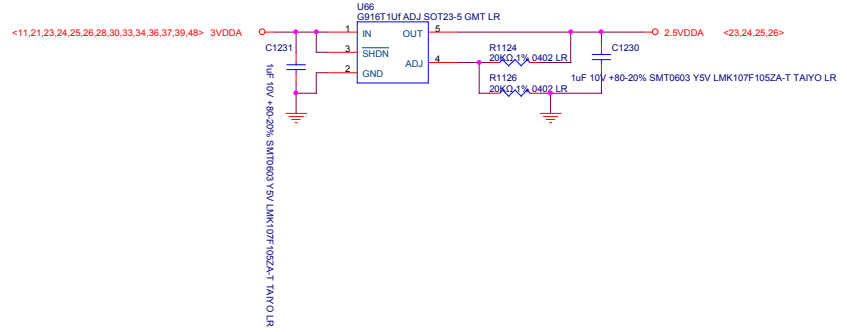


2.5VDDM



Does Q113 need NU here?

2.5VDDA 0.5A



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114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: VA250 < Yonah + VN896 + VT8237A >

Size: C | Document Number: <1.5V / 2.5V /1.8V> | Rev: 0.4

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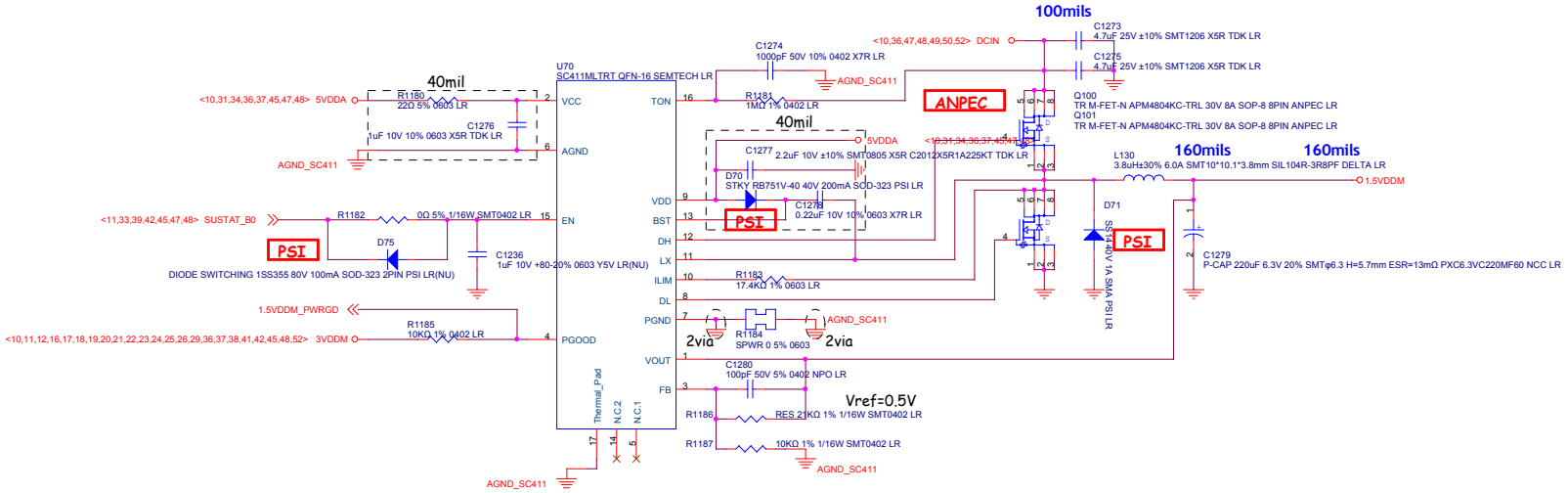
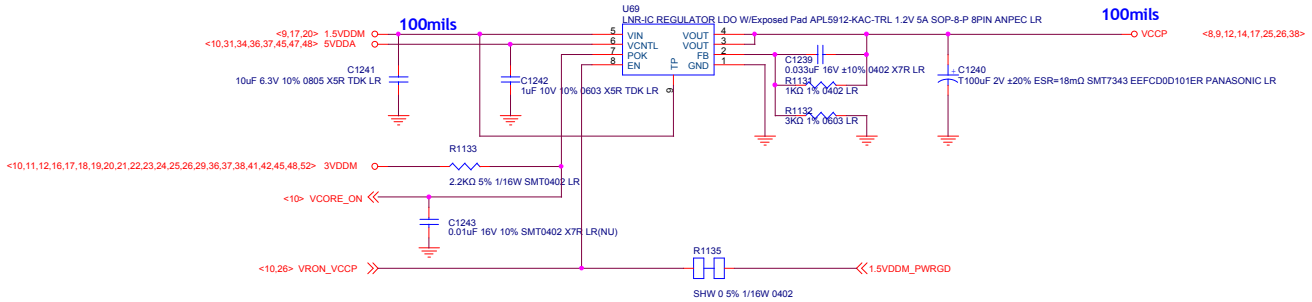
1.5VDDM



VCCP



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Title: VA250 < Yonah + VN896 + VT8237A >

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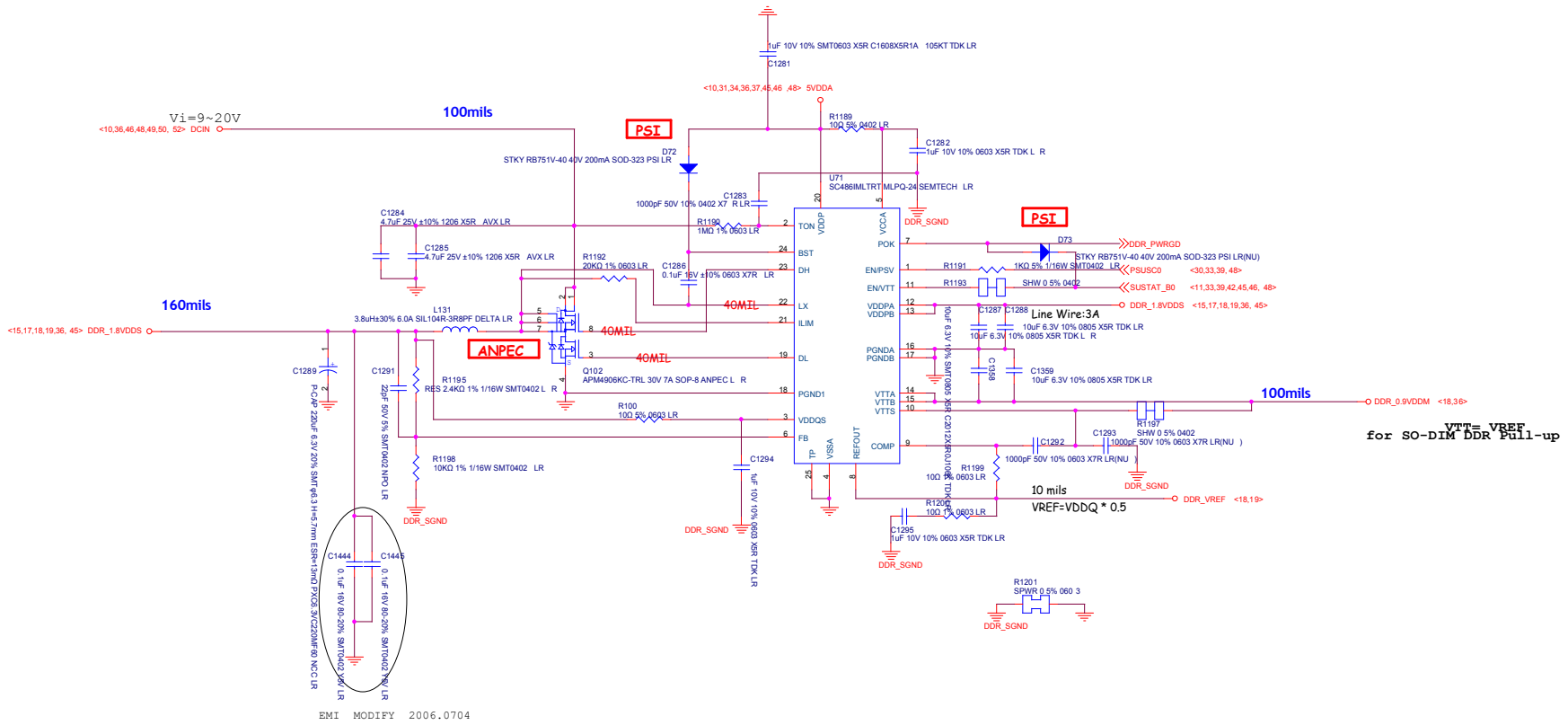

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Title: VA250 < Yonah + VN896 + VT8237A >

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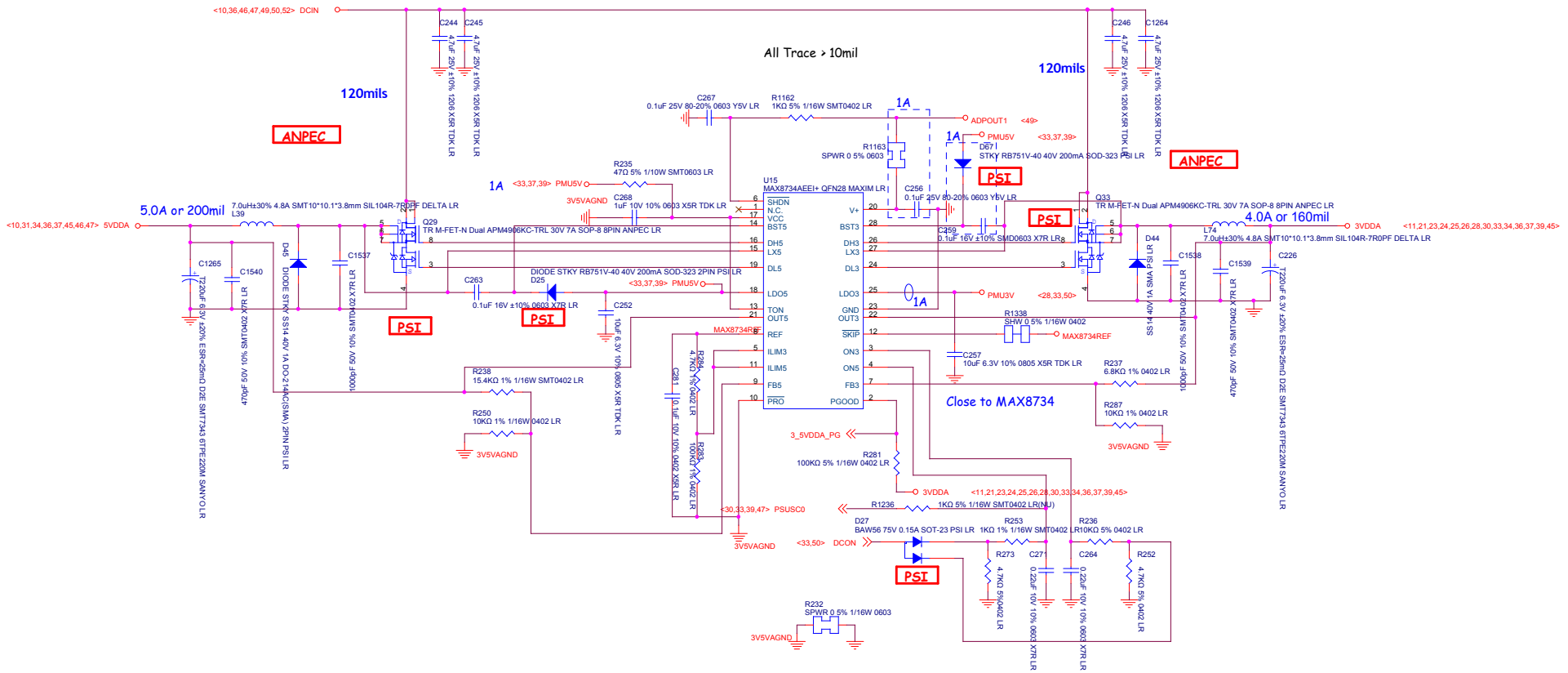
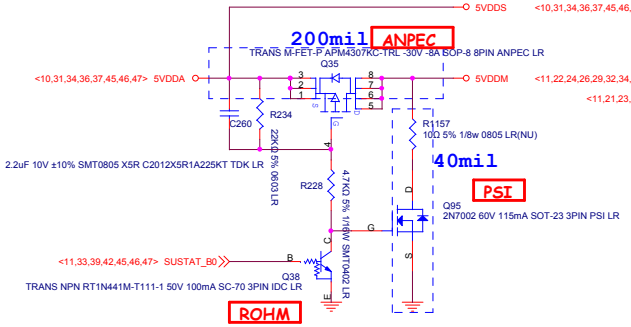
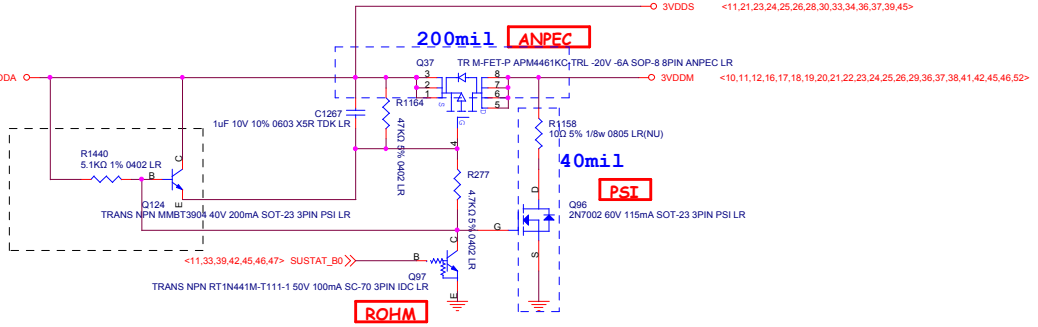
5VDDA/S/M, 3VDDA/S/M



5VDDS/5VDDM



3VDDS/3VDDM



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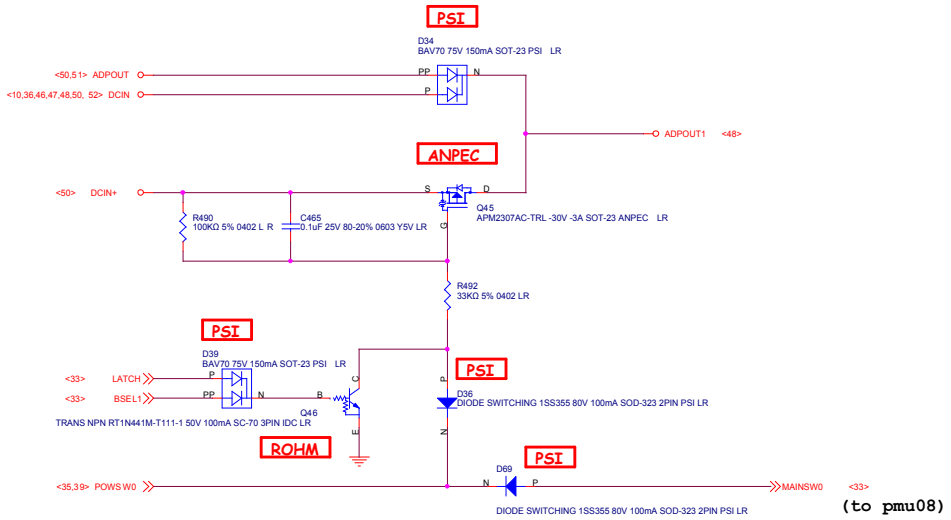

(to pmu08)

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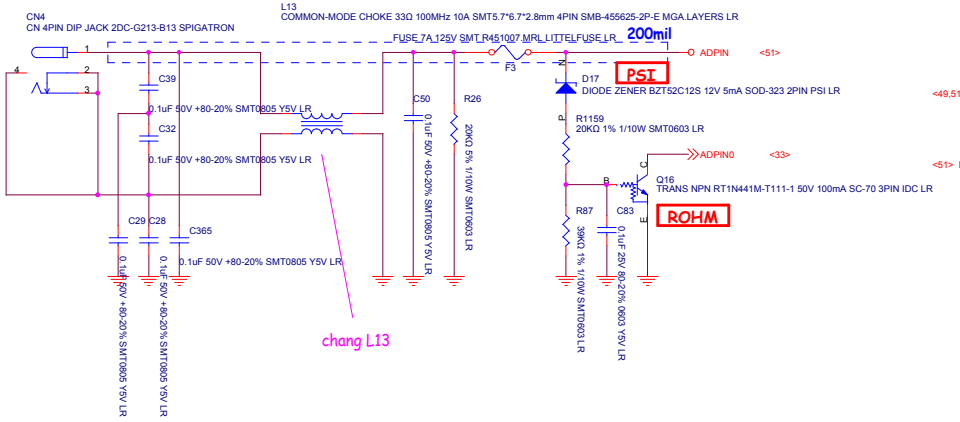
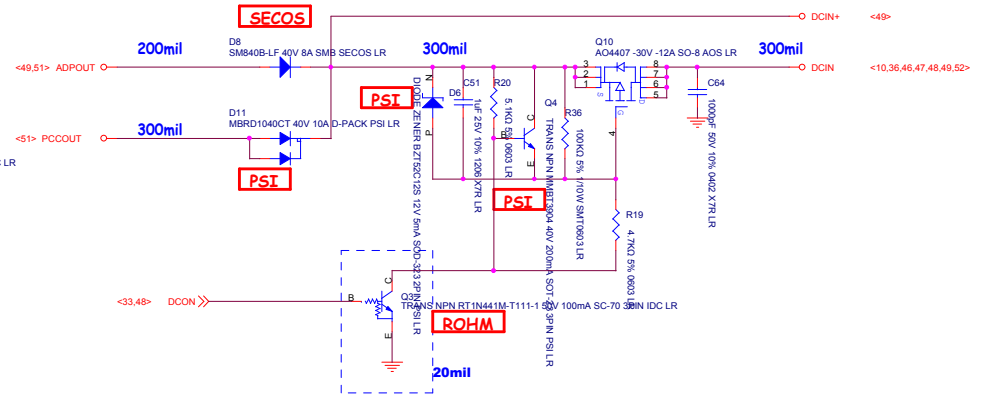
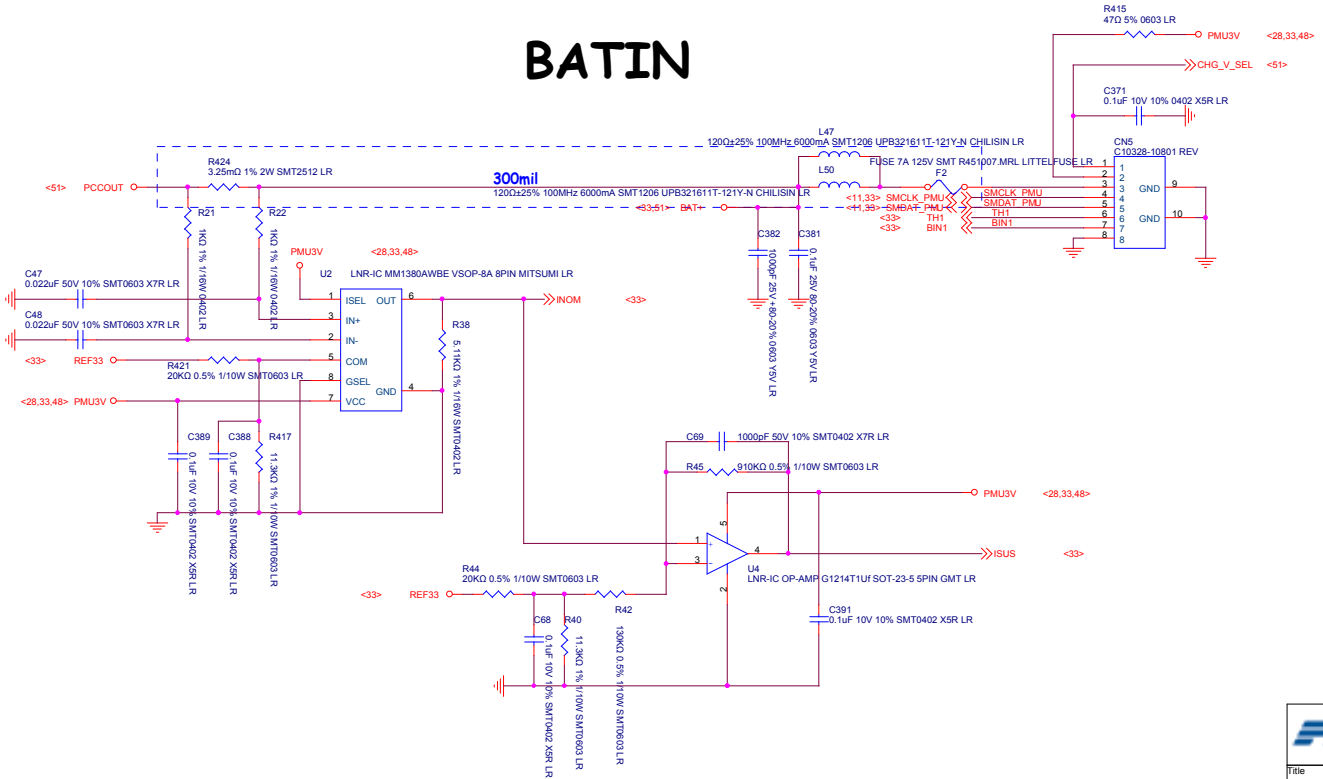
ADPIN



DCIN



BATIN



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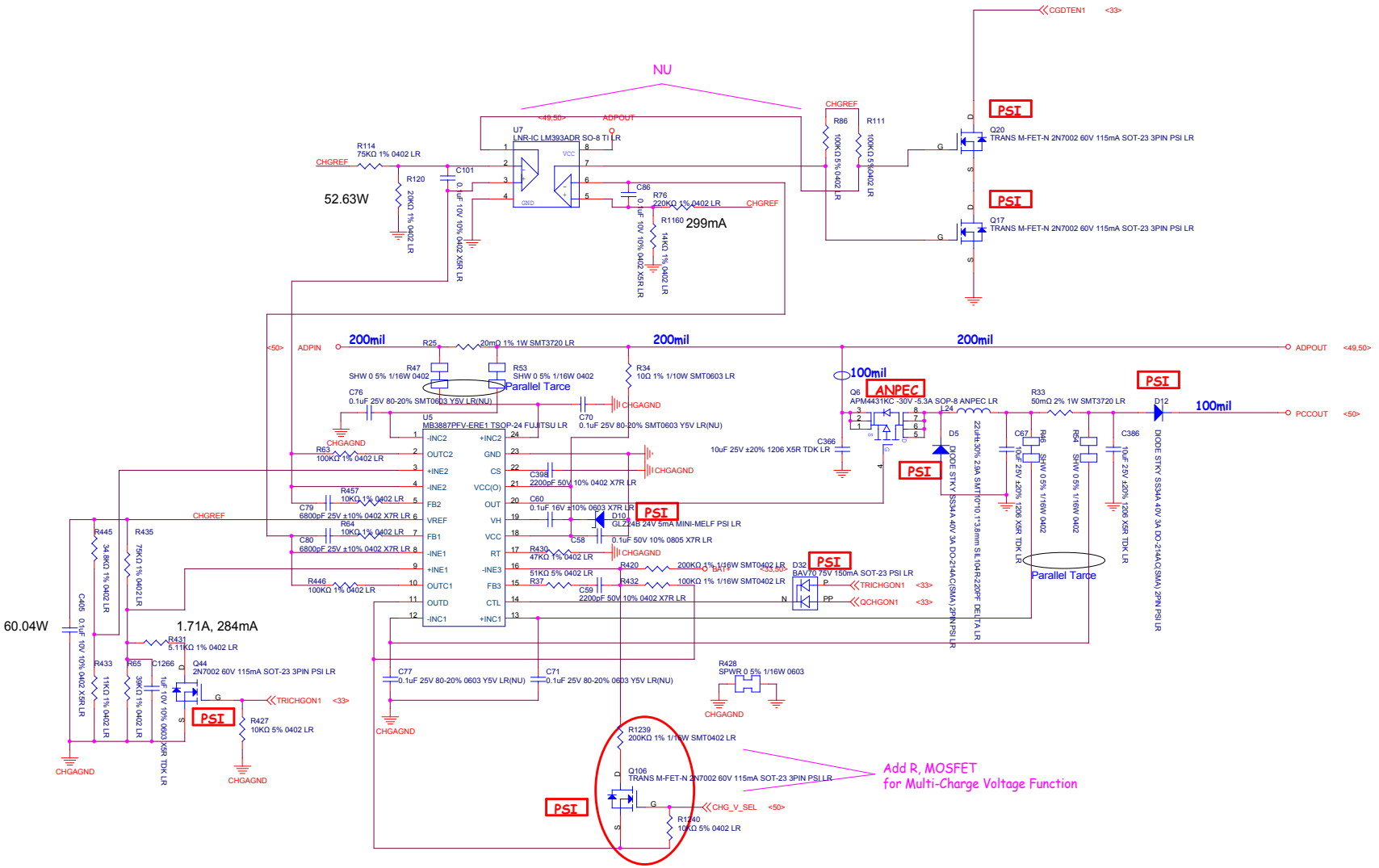
Charger



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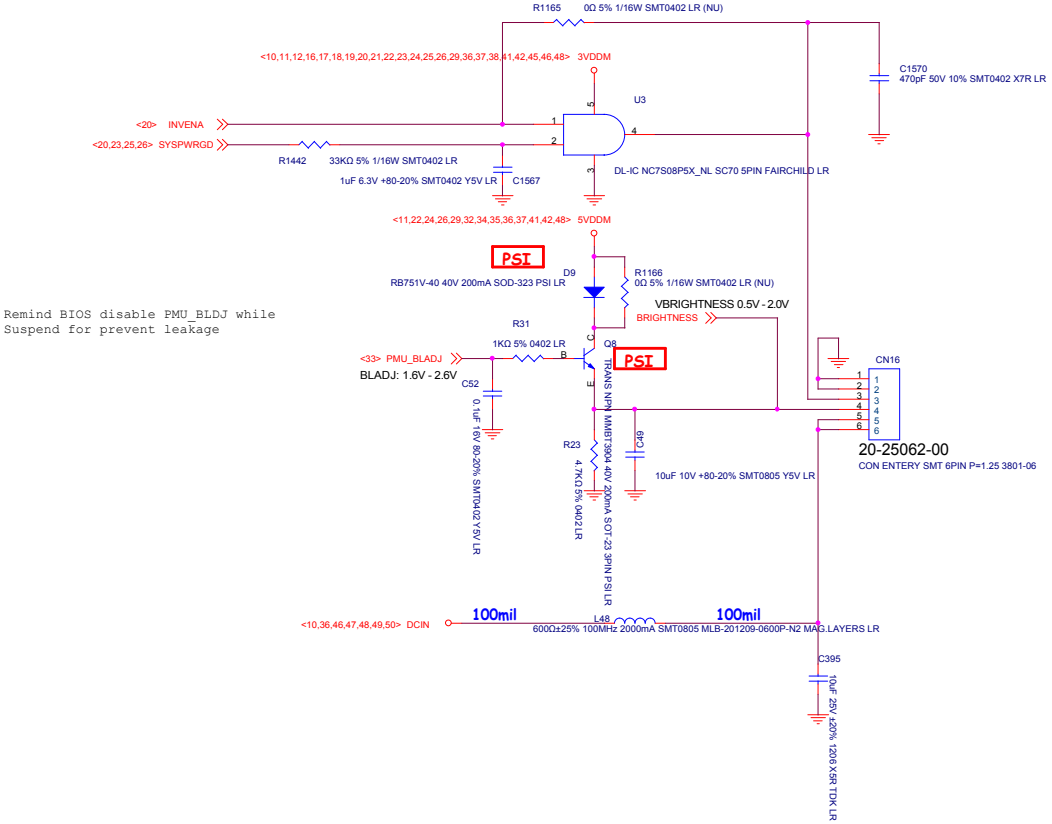
Inverter Connector



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Title	VA250 < Yonah + VN896 + VT8237A >	
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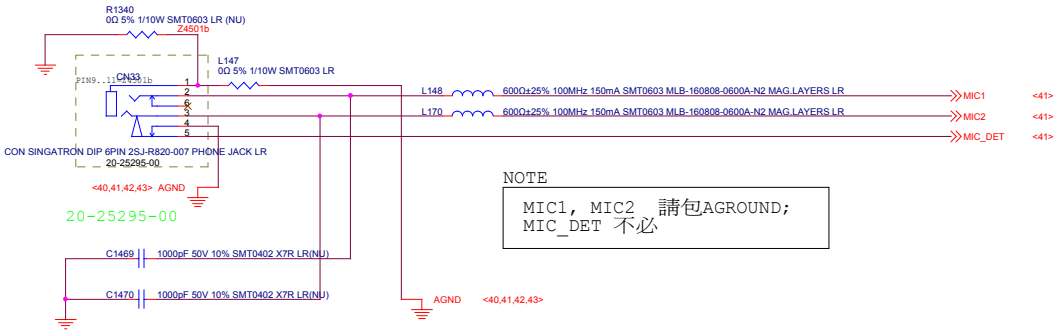
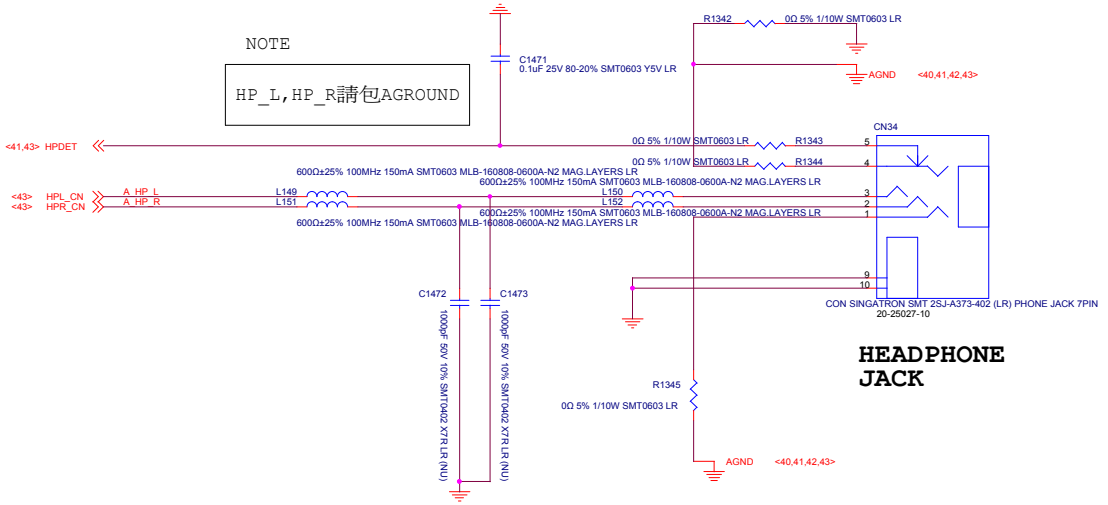


NOTE

MIC1, MIC2 請包AGROUND;
MIC_DET 不必



HEADPHONE JACK

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114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title
VA250 < Yonah + VN896 + VT8237A >

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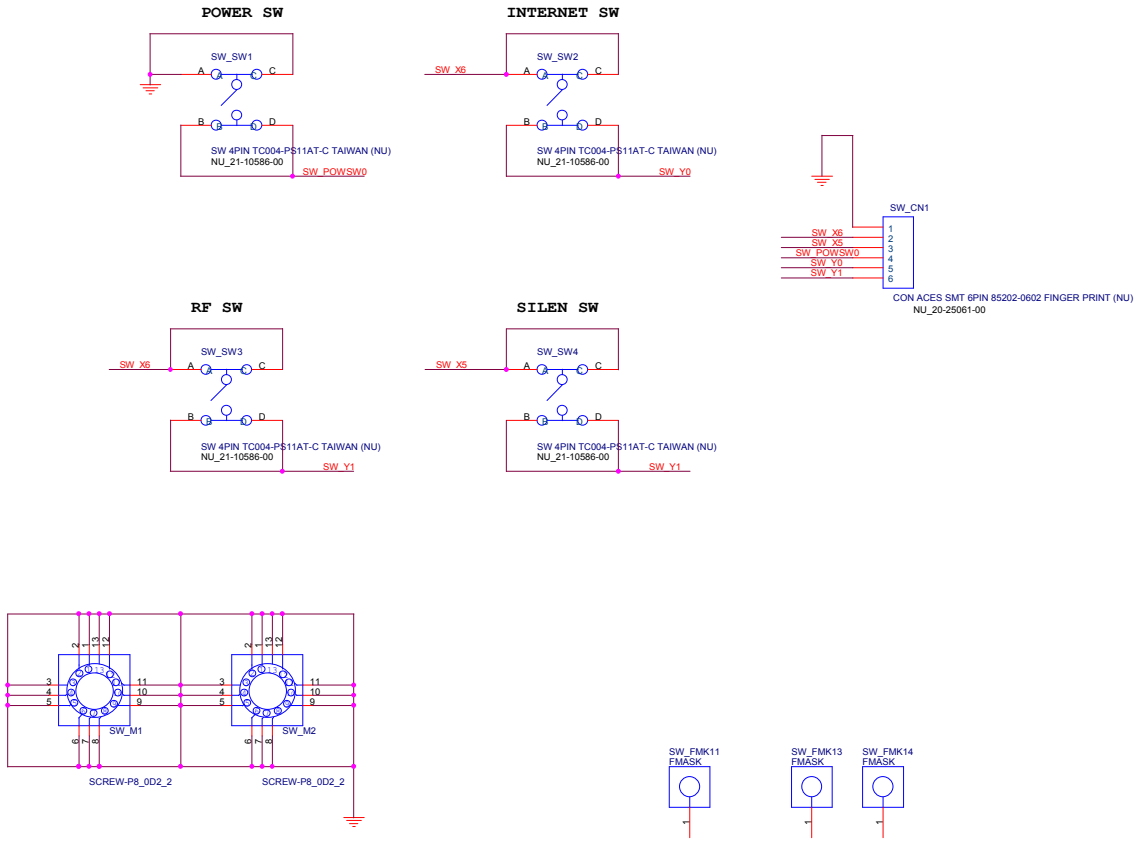

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Title	**VA250 < Yonah + VN896 + VT8237A >**	
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Title

VA250 < Yonah + VN896 + VT8237A >

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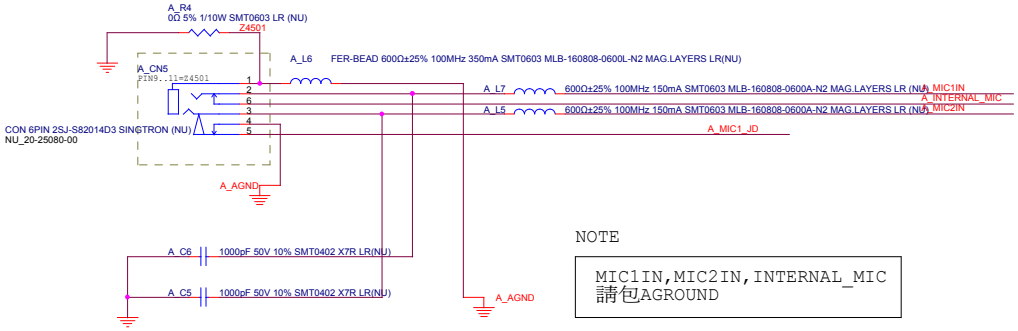
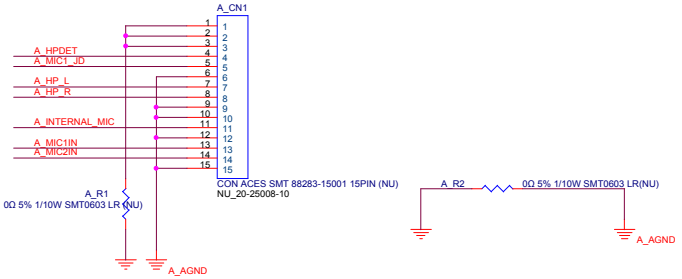


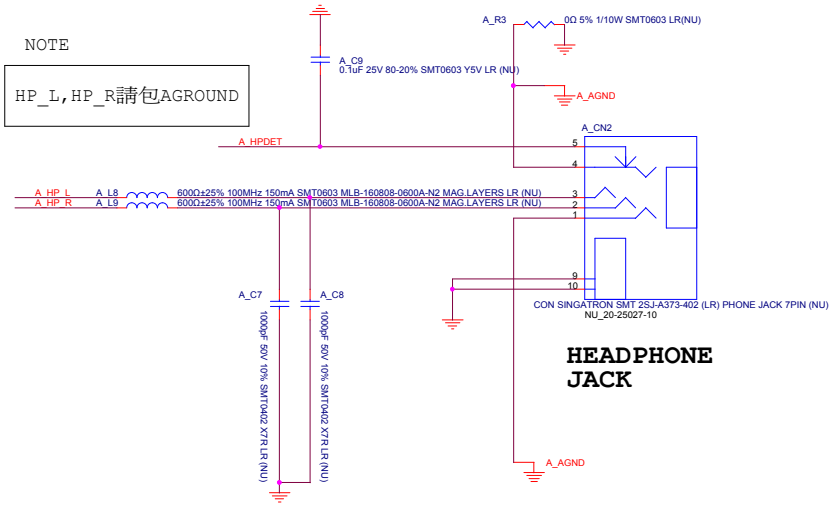
NOTE

MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND

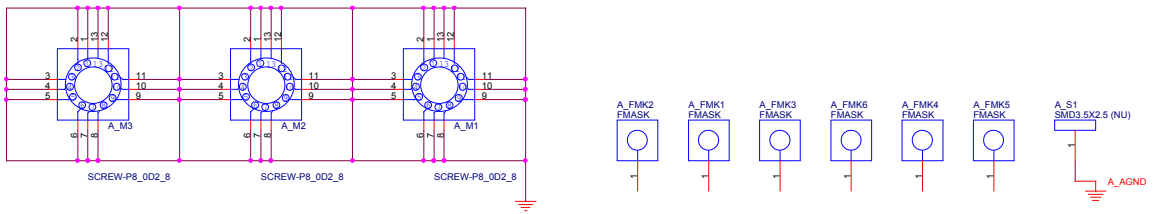


NOTE

HP_L,HP_R請包AGROUND



HEADPHONE JACK



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Size: C	Document Number: <Audio Board>	Rev: 0.4
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