TIGA Main Board Rev.04

Dolphin

Index

System Block

Power Block

System resource assign

USB Channel

Port#	Device
USB0	System #1
USB1	System #2
USB2	System #3
USB3	Bay
USB4	Finger-Print
USB5	P-R (to USB Hub)
USB6	Reserve(TP)
USB7	BlueTooth

SMBus

SMBCNT[2:0]	Device
0,0,0	uDIMM0,THRM
0,0,1	PMU
0,1,0	PLL
0,1,1	uDIMM1,THRM

PCI REQ#/GNT#

REQ#/GNT#	Device
REQ#0	PCMCIA
REQ#1	UNUSED
REQ#2	Unused
REQ#3	On Board LAN
REQ#4	Mini PCI
REQ#5	Unused

PCI INTERRUPT

PCIINT#	Device	
INT#0	PCIC	USB#1 / IDE
INT#1	PCIC	SMbus/AC-97
INT#2	Mini-PCI	USB#3
INT#3	Mini-PCI	USB#2
INT#4	On Board LAN	
INT#5	UNUSED	
INT#6	Unused	
INT#7	Unused	

PCI BUS #1

IDSEL	Dev.ID	Device
AD16	00h	
AD17	01h	
AD18	02h	
AD19	03h	PCMCIA/IEEE1394
AD20	04h	Internal LAN
AD21	05h	miniPCI
AD22	06h	
AD23	07h	

#05
Add and Correct Configuration

Revision History

Rev	Date	Description
01	2005.08.30	Official Release.
02	2005.10.07	Change P24,28. ECO No. F0205A14919.
03	2005.10.11	Change P12. ECO No. F0205A15271.
04	2005.12.02	Change P10,17,50,51,56. ECO No. F0205A18869.
05	2005.12.12	Change P4-6,12,22,23,38,44. ECO No. F0205A19559.
06	2006.03.14	Change P23. ECO No. F0206A04590.

Main Board Model Configurations

Model	Destination	CPU	PR	Int. Mic	TPM	BT	TP	ODD	4in1
VB238AA	Overseas	Pentium-M 753 ULV	○	○	○	○	×	○	○
VB238AB	Overseas	Celeron-M 383 ULV	○	○	○	○	×	○	○
VB238AC	Japan Retail	Pentium-M 753 ULV	×	×	×	×	×	○	○
VB238AD	Japan Retail	Celeron-M 383 ULV	×	×	×	×	×	○	○
VB238AE	Overseas(FKL)	Celeron-M 383 ULV	×	×	×	○	×	○	○
VB238AF	Japan Customized	Pentium-M 753 ULV	×	×	○	×	○	×	×
VB238AG	Japan Retail	Pentium-M 773 ULV	×	×	×	×	×	○	○
VB238AH	Japan Retail	Celeron-M 383 ULV	×	×	×	×	×	○	○

Refernce drawings.

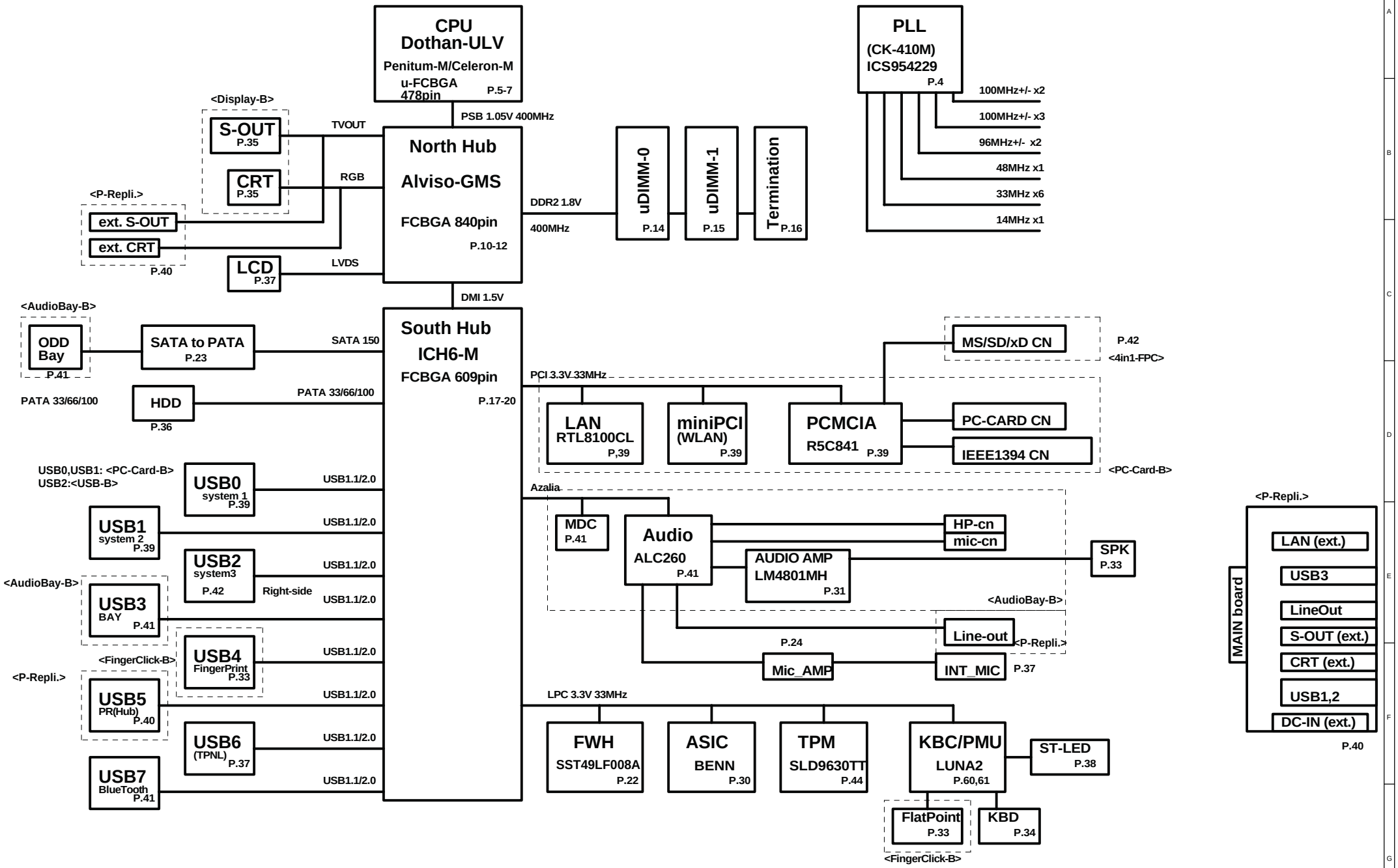
DWG#	Description	
C1CP250060-XX	Schematics ; PC-CARD Board (VB238BA)	
C1CP250079-XX	Schematics ; Audio Bay Board (VB238FA)	
C1CP250077-XX	Schematics ; Fingerprint Sensor board (VB238EA)	
C1CP254631-XX	Schematics ; 4in1 FPC (VB238XA)	
C1CP250066-XX	Schematics ; Port Replicator Board (VB238CA)	
A3CP254680-01	Hardware specification.	

[TOP PAGE]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2005.08.30	Murayama	MAKINO	Miura	

TITLE: Tiga Main Board
DRAW. NO.: C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 1 / 66

System block diagram



[BLOCK DIAGRAM]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
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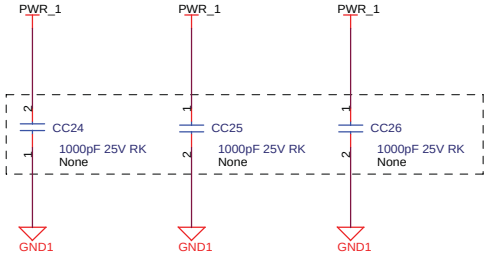

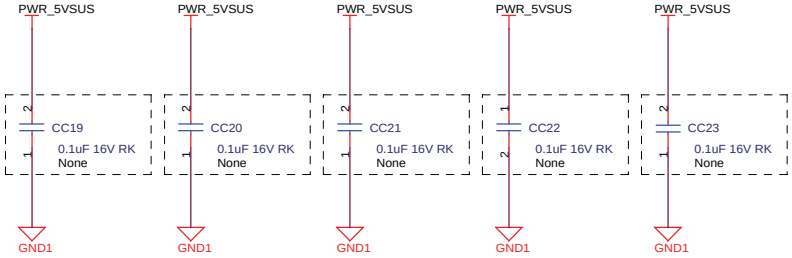

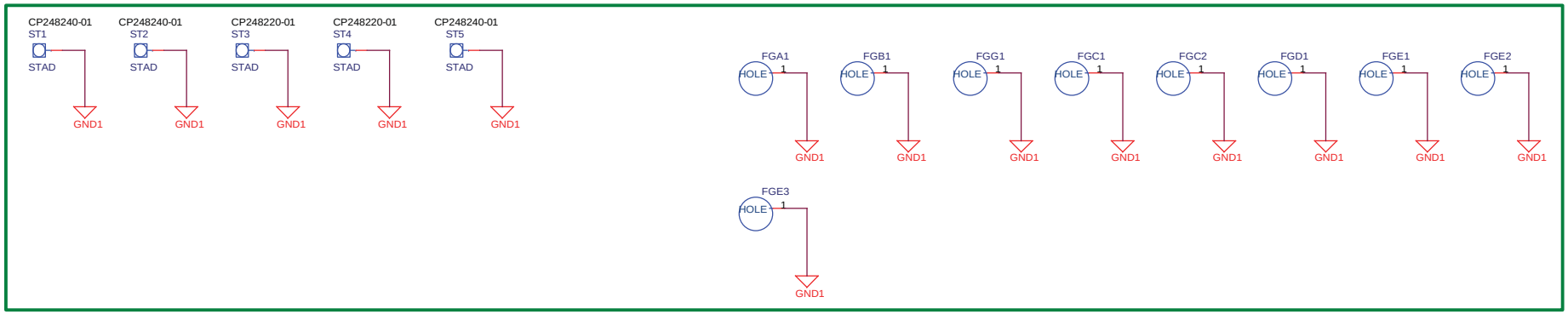

[EMI]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

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FUJITSU LTD. SHEET 3 / 66

CK-410M Spec

FSA	FSB	FSC	Function
1	0	0	133MHz Host CLK
1	0	1	100MHz Host CLK
1	1	0	MHz Host CLK
1	1	1	MHz Host CLK

※のパターンの[illegible]
また、各対のクロックライン同士の間隔（CLK_133_CPUx+/-# 間）は、
信号線間インピーダンス100Ωで引くこと（9mil幅）。

Control the impedance of signals that "*" are marked are 55ohm. (the width is 4mil)
Control the impedance between the pair of clock (i.e. CLK_133_CPUx+/-) 100ohm.
(the width is 9mil)

R1-R4,R8-R13,R17-R22の抵抗はM1の近傍に配置すること。
Place R1-R4,R8-R13,R17-R22 near PLL as possible.

M1 ICS954229AGLF

XTAL_IN, XTAL_OUT, FSA/USB_48, FSB/TEST_MODE, FSC/TEST_SEL/REF1, SCLOCK, SDATA, PCI/SRC_STOP#, CPU_STOP#, VTT_PWRGD#/PD, IREF

CPU0, CPU#0, CPU1, CPU#1, CPU_2_ITP/SRC_7, CPU2_ITP/SRC#7, PCIF0/ITP_EN, PCIF1/SELSRC_LCDCLK#, PCI2, PCI3, PCI4, PCI5, SRC0/LCDCLK_SS, SRC#0/LCDCLK_SS#, SRC1, SRC#1, SRC2, SRC#2, SRC3, SRC#3, SRC4_SATACLK, SRC#4_SATACLK#, SRC5, SRC#5, DOT96, DOT96#, REF0, CLKREQA#, CLKREQB#

VDD_SRC0, VDD_SRC1, VDD_SRC2, VDD_PCI0, VDD_PCI1, VDD_CPU, VDD_REF, VDD_48, VDD_A, VSS_A, VSS_48, VSS_SRC, VSS_CPU, VSS_PCI0, VSS_PCI1, VSS_REF

reserve(PELAN)

R<IREF>	IREF
220ohm	5mA
475ohm	2.32mA

#05(F0205A19559)
Mount R16 for VB238AF.

R30,R31 are JUMPER for VB255AF.
Other models mount 49.9 1/16W 0.5%.

これらのコンデンサは、PLLの近傍に
配置すること。
Place these capacitors near PLL.

バックライト制御をASICで行わなければ、
14.318MHzをASICに供給しなくても平気

option pin	target	High	Low
SELSRC_LCDCLK#	17,18pin	SRC0	LCDCLK_SS
ITP_EN	35,36pin	CPU_2_ITP	SRC6

[Refference:Greek]

[PLL]

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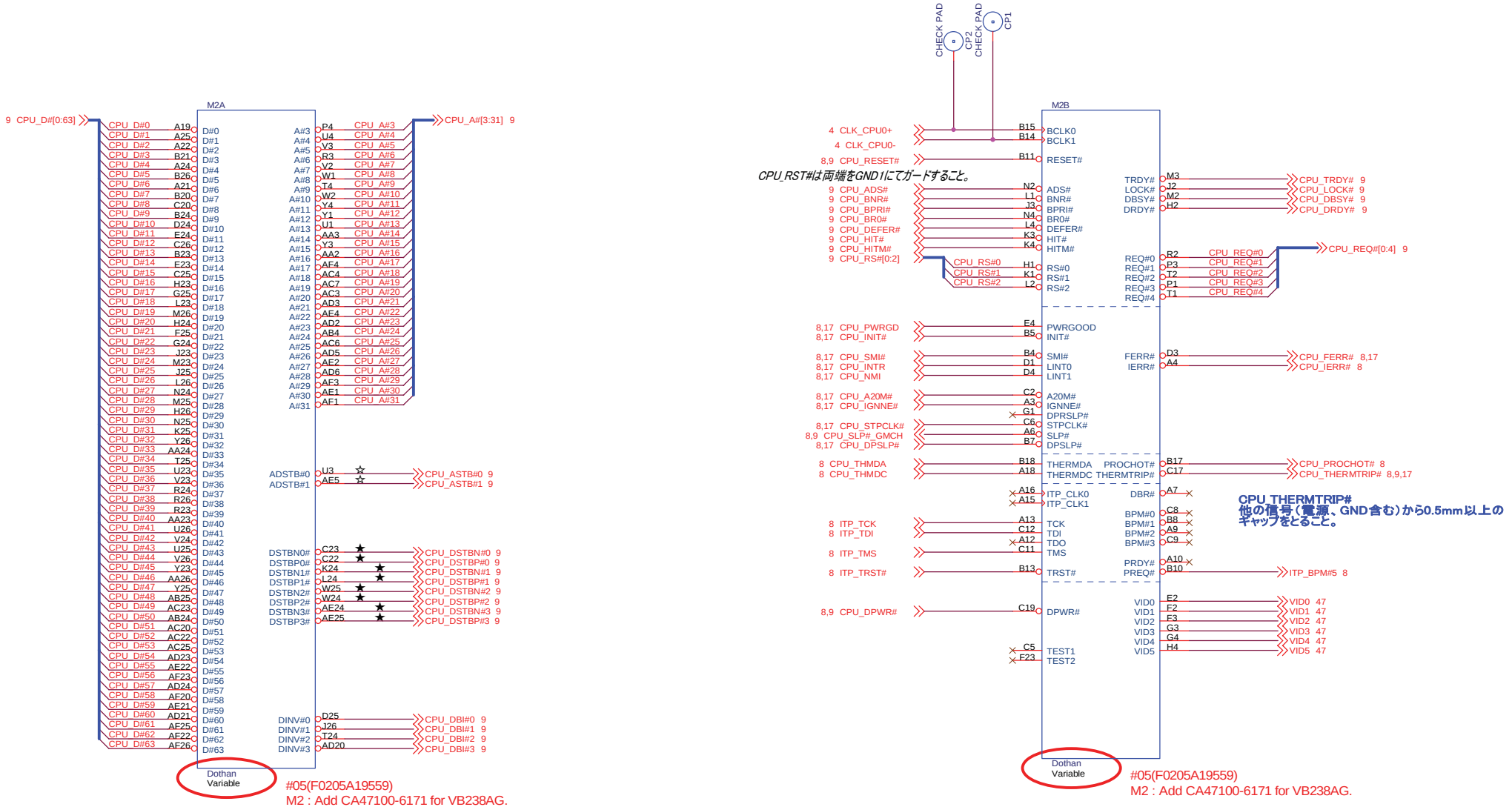

☆ CPU_ASTB#0,CPU_ASTB#1はそれぞれの両側をGND1にて囲うこと
(Guard CPU_ASTB#0, CPU_ASTB#1 with GND1 respectively.)

★ CPU_DSTBx#[0:3]は各ペアごとに両側をGND1にて囲うこと
(Each CPU_DSTBx#[0:3] strobe pear should be guarded with GND1 respectively.)

△ GND1で両側をガードすること （12ページ参照）
(Guard CPU_THMDA/CPU_THMDC with GND1.)

[Refference:Greek]

[CPU-1 (FSB)]

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	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
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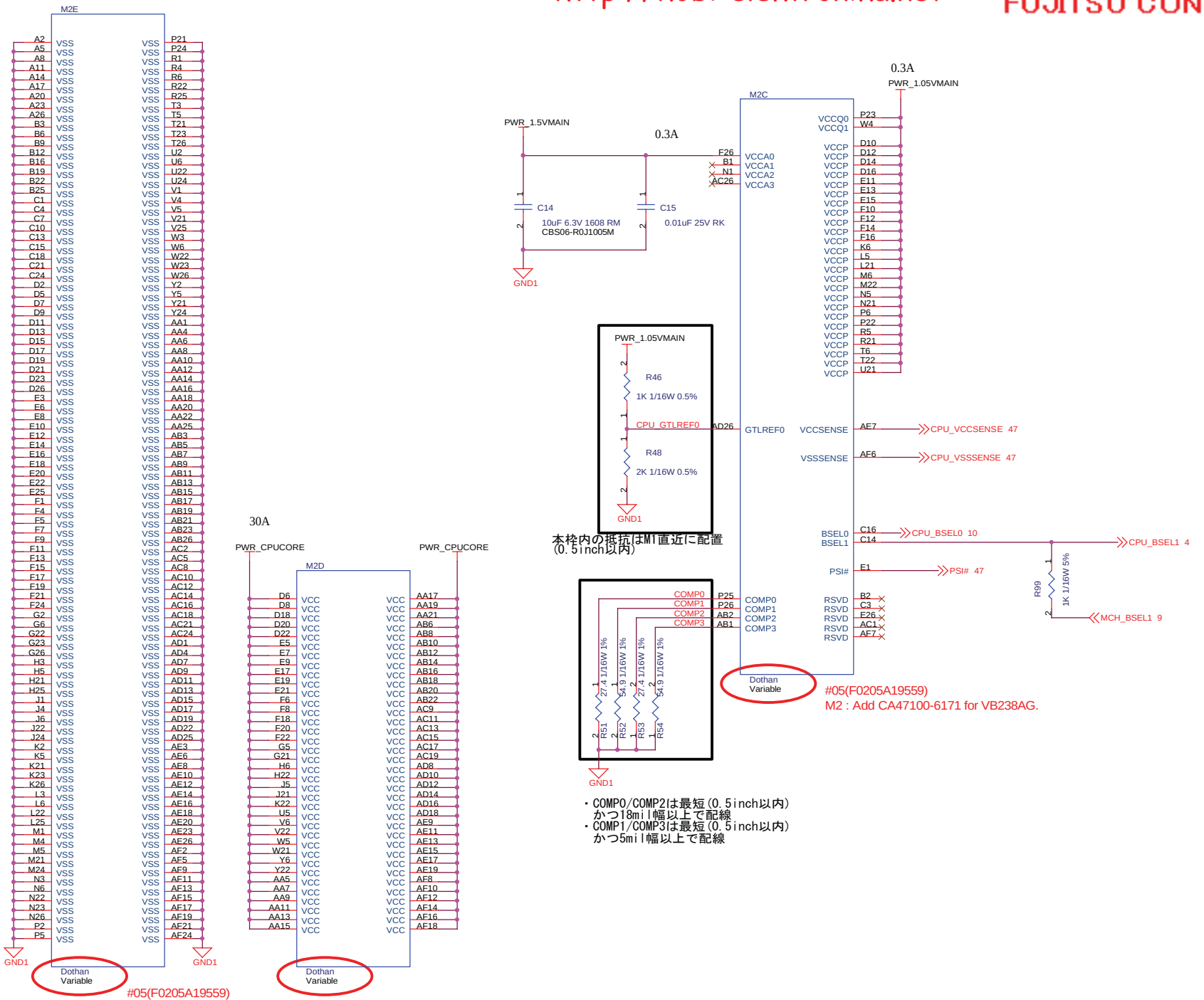

本枠内の抵抗はMT直近に配置
(0.5inch以内)

#05(F0205A19559)
M2 : Add CA47100-6171 for VB238AG.

・COMP0/COMP2は最短(0.5inch以内)
かつ18mil幅以上で配線
・COMP1/COMP3は最短(0.5inch以内)
かつ5mil幅以上で配線

VID5	VID4	VID3	VID2	VID1	VID0	V
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

[Refference:Greek]

[CPU-2 (POW)]

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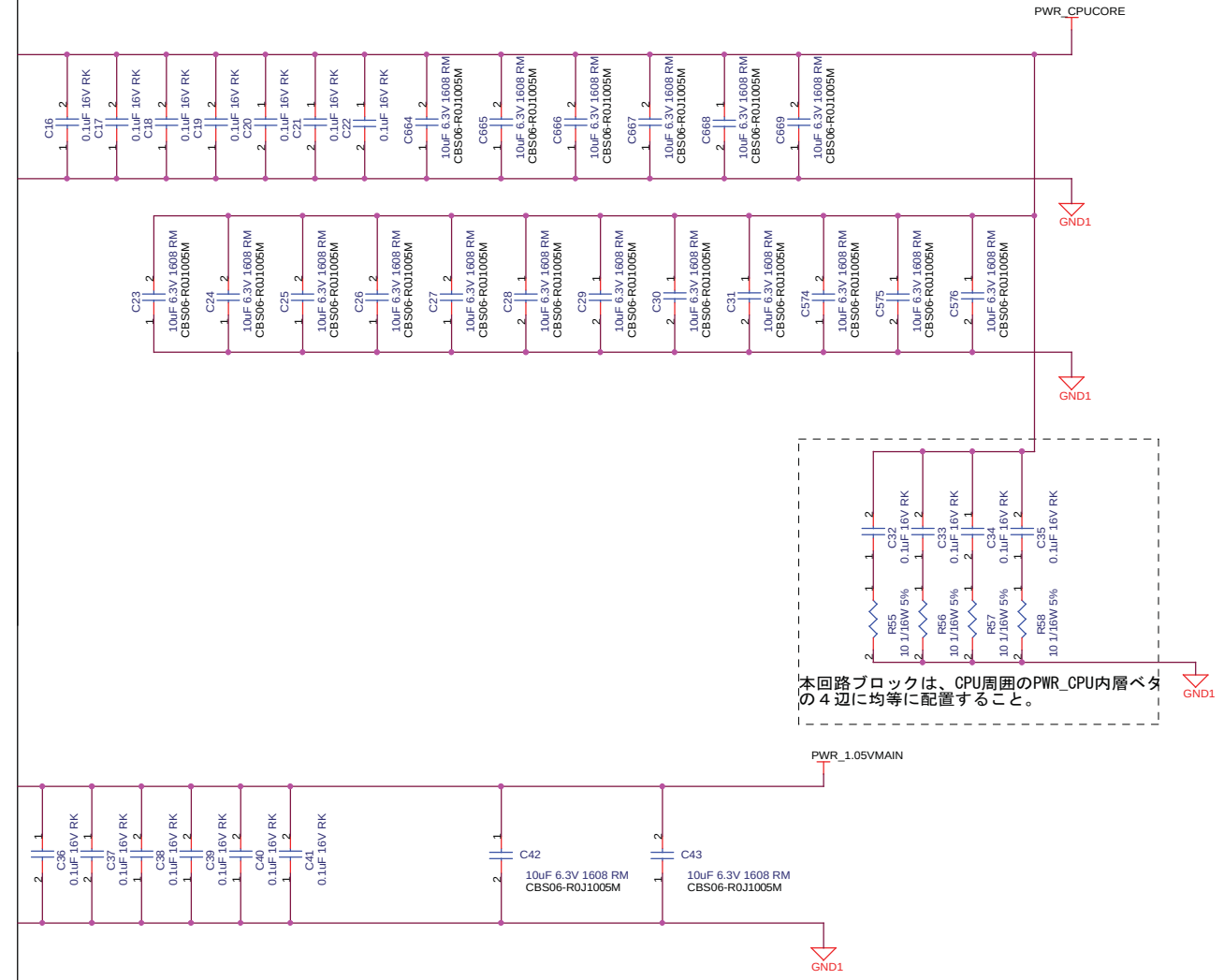
M2

Pentium-M
Celeron-M



[Refference:Greek]

[CPU CAP]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

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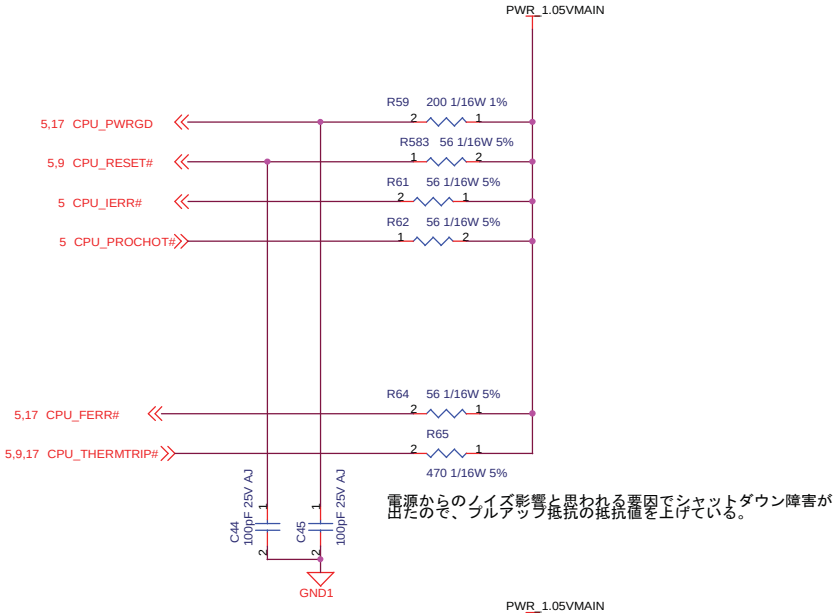
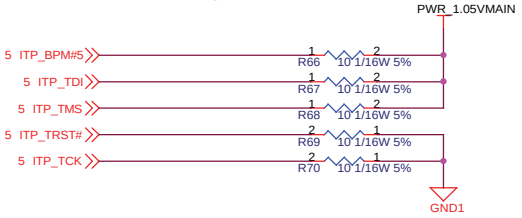
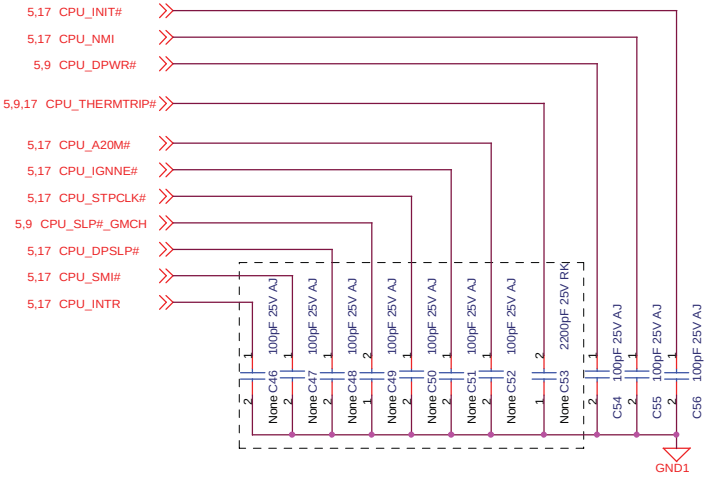
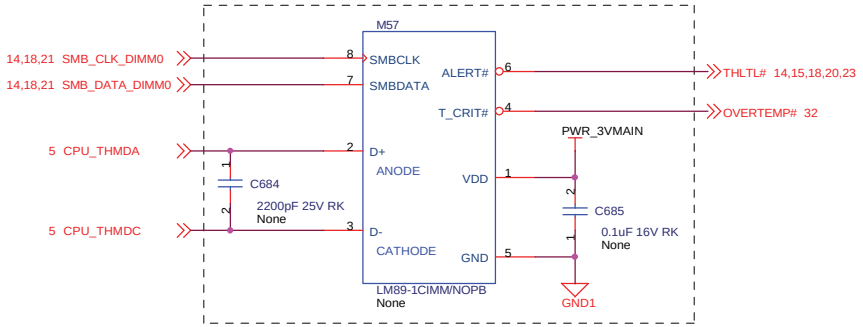


電源からのノイズ影響と思われる要因でシャットダウン障害が出たので、プルアップ抵抗の抵抗値を上げている。







[Refference:Greek]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

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[CPU PU/etc.]

[GMCH-1 (FSB/DMI)]

M3A

915GMS
CA46120-0113

GMCHのスロットリングは外部端子を使わない。
（そもそも使われていない）

[Refference:Greek]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	DESIGN	CHECK	APPR.			

TITLE Tiga Main board
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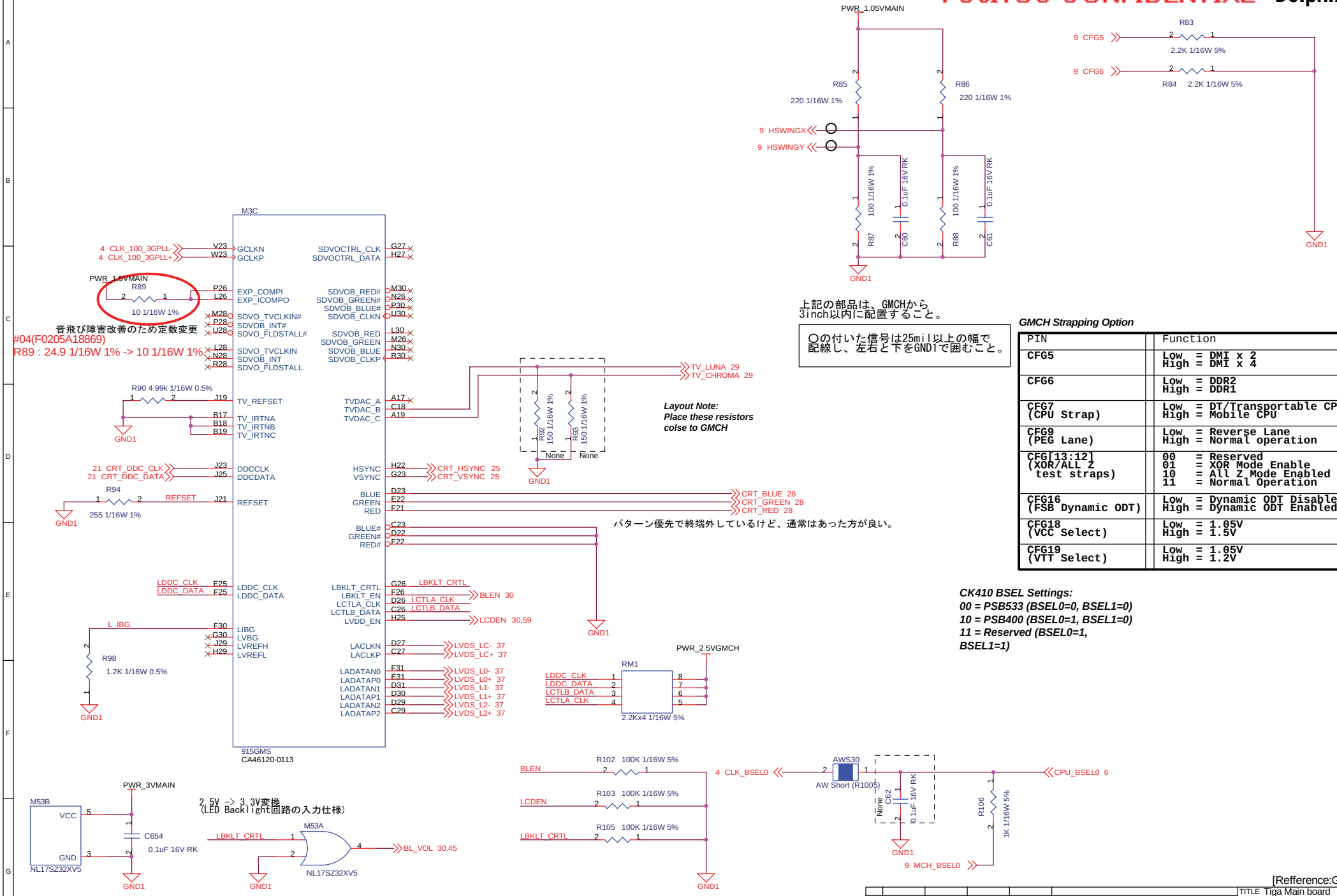
[GMCH-2 (VGA/etc.)]



GMCH Strapping Option

PIN	Function
CFG5	Low = DMI x 2 High = DMI x 4
CFG6	Low = DDR2 High = DDR1
CFG7 (CPU Strap)	Low = DT/Transportable CPU High = Mobile CPU
CFG9 (PEG Lane)	Low = Reverse Lane High = Normal operation
CFG[13:12] (XOR/ALL Z test straps)	00 = Reserved 01 = XOR Mode Enable 10 = All Z Mode Enabled 11 = Normal Operation
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled
CFG18 (VCC Select)	Low = 1.05V High = 1.5V
CFG19 (VTT Select)	Low = 1.05V High = 1.2V

CK410 BSEL Settings:
00 = PSB533 (BSEL0=0, BSEL1=0)
10 = PSB400 (BSEL0=1, BSEL1=0)
11 = Reserved (BSEL0=1, BSEL1=1)

[Refference:Greek]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK		APPR.

TITLE Tiga Main board
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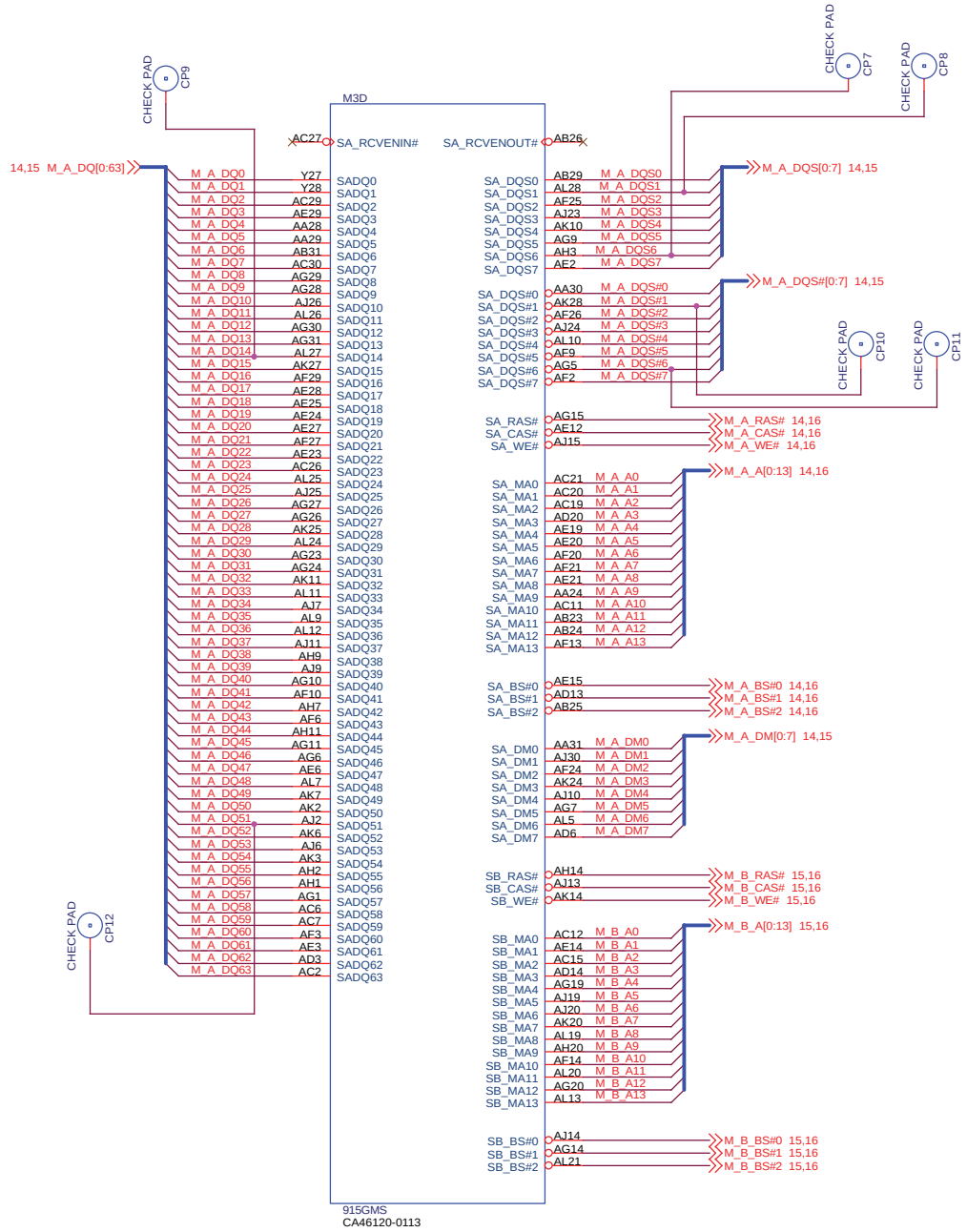

[Refference:Greek]

[GMCH-3 (DDR2)]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 11 / 66

C63-C66 are JUMPER for VB255AF.
Other models mount 0.1uF 16V RK.

#03(F0205A15271)
C75 for VB238AF : JUMPER -> None.
#05(F0205A19559)
Mount C75 for VB238AF.

~~C75~~,C76 are JUMPER for VB238AF.

Layout Note:
VSSA_CRTDAC route caps within 250mils of Alviso.
FL8 route within 3inch of Alviso.

PEGの電圧がシビアな為、
L5の部品には注意が必要。
（電圧降下が起きない事！）

[GMCH-4 (POW1)]

[Refference:Greek]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK		APPR.

TITLE Tiga Main board
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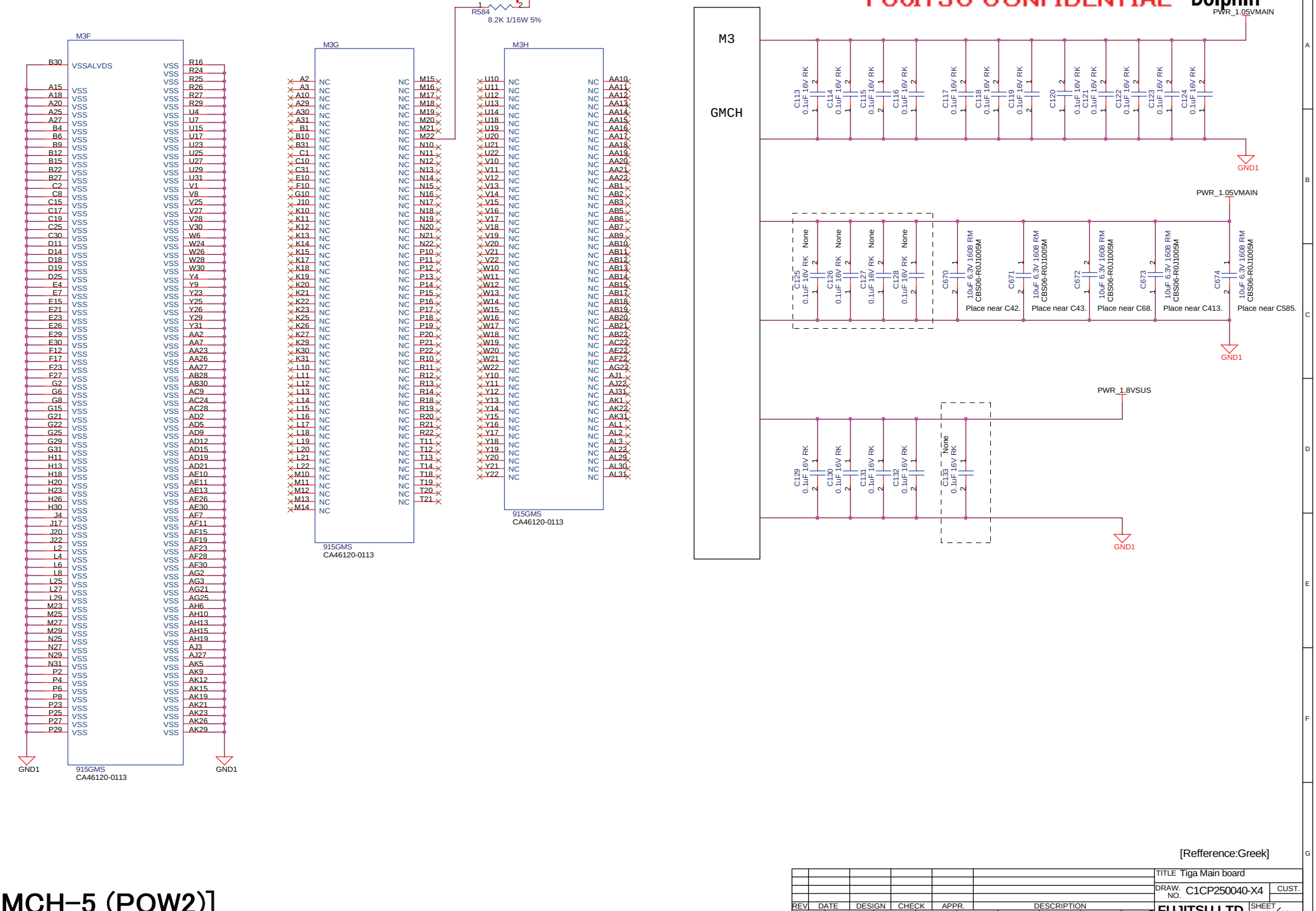
FUJITSU CONFIDENTIAL

Dolphin



[Refference:Greek]

[GMCH-5 (POW2)]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

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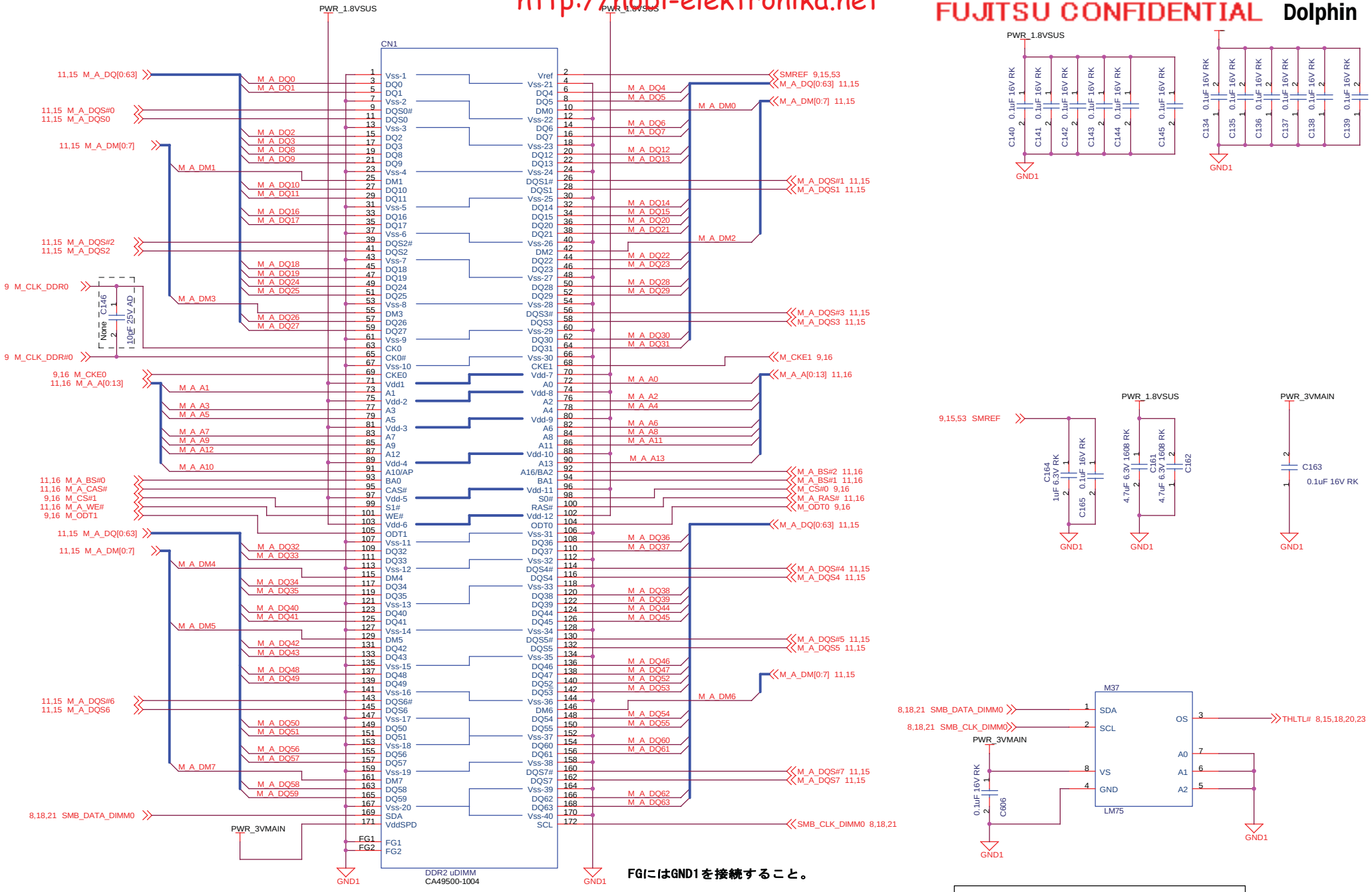

FGにはGND1を接続すること。

※M37はDIMMの中央部の温度を関知できるように配置すること。

[Refference:Pinon]

[DDR2 SLOT0]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	DESIGN	CHECK	APPR.			

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CUST.
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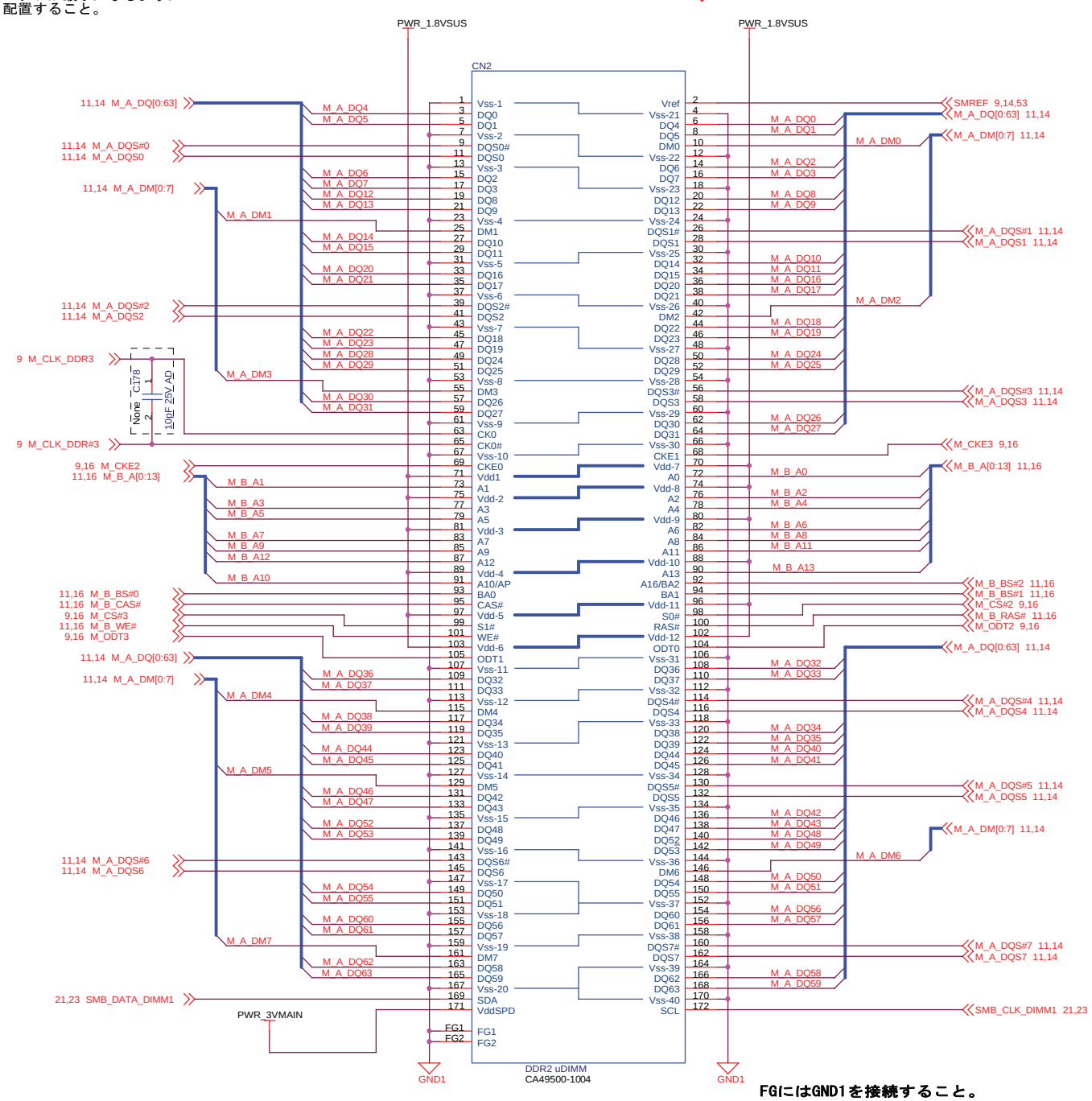
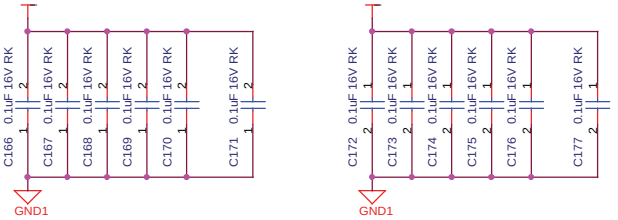
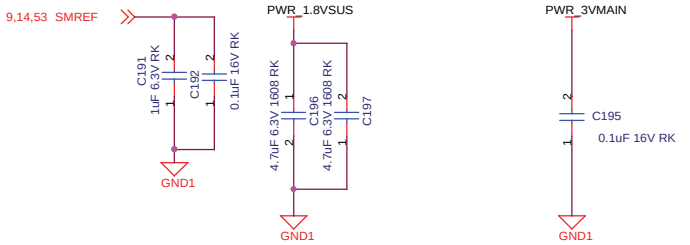
右記の抵抗はREF_MEMの
スタブが最小になるように
配置すること。

コネクタ近くにGNDのpinの近く
容量の小さいコンデンサをコネクタ近辺に配置

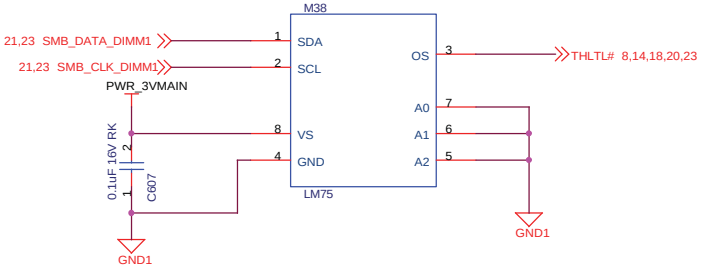


FGにはGND1を接続すること。





上記のコンデンサはメモリコネクタの近辺に配置し
電源ピンx1に対し、コンデンサx2を配置すること



※M38はDIMMの中央部の温度を
関知できるように配置すること。

[Refference:PINON]

[DDR2 SLOT1]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
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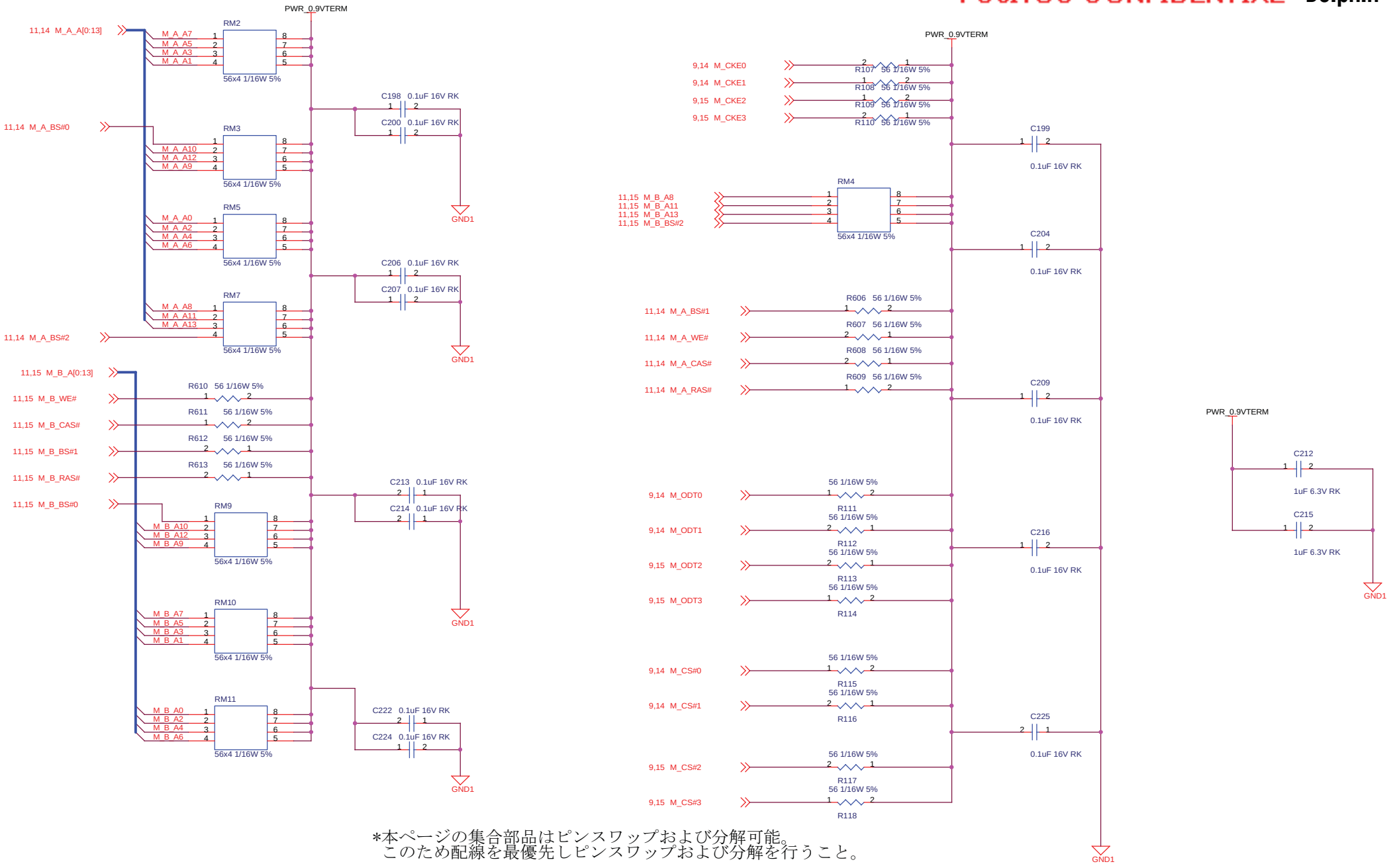

*本ページの集合部品はピンスワップおよび分解可能。
このため配線を最優先しピンスワップおよび分解を行うこと。

特に、アドレス部はモジュール間でのピン変更。集合部品の
分解および再集合が可能。

*本ページのパスコンは抵抗2つに対し1つ配置すること
(集合抵抗はx8, x4に対し、各々4つ, 2つ)

[Refference:Greek]

[DDR2 REF/TERM]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 16 / 66

[ICH-1 (CPU/DMI/PCI/USB]

M4A

CHECK PAD CP13 CHECK PAD CP14

4 CLK_14_ICH
4 CLK_48_ICH
E10 CLK14
A27 CLK48
SUSCLK V6

9 DMI_RXP0
9 DMI_RXN0
T24 DMI0RXP
T25 DMI0RXN
DMI0TXP R26 DMI_TXP0 9
DMI0TXN R27 DMI_TXN0 9

9 DMI_RXP1
9 DMI_RXN1
V24 DMI1RXP
V25 DMI1RXN
DMI1TXP U26 DMI_TXP1 9
DMI1TXN U27 DMI_TXN1 9

CHECK PAD CP16 CHECK PAD CP17
Y24 DMI2RXP
Y25 DMI2RXN
DMI2TXP W26
DMI2TXN W27
AB23 DMI3RXP
AB24 DMI3RXN
DMI3TXP AA26
DMI3TXN AA27

4 CLK_100_ICH+
4 CLK_100_ICH-
AC25 DMI_CLKP
AD25 DMI_CLKN
DMI_IRCOMP F23
DMI_ZCOMP F24
R119 2 1 10 1/16W 1%
PWR_1.5VMAIN

Place R119 within 500 mils of ICH.

音飛び障害改善のため定数変更

#04(F0205A18869)
R119 : 24.9 1/16W 1% -> 10 1/16W 1%.

H24 HSIP0
H25 HSIN0
HSOP0 G26
HSON0 G27
K24 HSIP1
K25 HSIN1
HSOP1 J26
HSON1 J27
M24 HSIP2
M25 HSIN2
HSOP2 L26
HSON2 L27
P23 HSIP3
P24 HSIN3
HSOP3 N26
HSON3 N27

30 ICH6_LAN_RST#
R588 2 1 0 1/16W None
F12 LAN_CLK
LAN_RSTSYNC B11
E12 LAN_RXD0
E11 LAN_RXD1
C13 LAN_RXD2
LAN_TXD0 C12
LAN_TXD1 C11
LAN_TXD2 E13
9,20,22,31,36,44,61 PLT_RST#
R649 1 2 0 1/16W
V5 LAN_RST#
EE_CS D12
EE_SHCLK B12
EE_DOUT D11
F13 EE_DIN

この端子をHi -> Lowにすると、
ちょっと省電力になるらしい

61 KBC_A20G
A20GATE
A20M# AF23 CPU_A20M# 5,8
20,61 KBC_INIT#
AD23 RCIN#
STPCLK# AE26 CPU_STPCLK# 5,8
5,8 CPU_FERR#
R120 1 2 56 1/16W 5%
AF24 FERR#
CPUSLP# AE27 (CPU_SLP_ICHdel)
5,8,9 CPU_THERMTRIP#
R121 1 2 56 1/16W 5%
AF23 THRMTRIP#
DPSLP# AD27
STP_CPU#/GPO20 AD22
R122 2 1 0 1/16W
CPU_DPSLP# 5,8
STP_CPU# 4,47

Place ThisRegisiter within 2inch of ICH6.

PWR_1.05VMAIN
C226 2 1 None 100pF 25V AJ
DPRSLPR AE24
DPRSLPVR AE20 DPRSLPVR 47
SUS_STAT#/LPCPD# W3 SUSTAT# 22
STP_PCI#/GPO18 AC21 STP_PCI# 4

IGNNE# AG26 CPU_IGNNE# 5,8
INIT3_3V# AE22 FWHINIT# 22
INIT# AE27 CPU_INIT# 5,8
INTR AG24 CPU_INTR 5,8
NMI AE25 CPU_NMI 5,8
SMI# AG27 CPU_SMI# 5,8

9,20,21,30,31,32,39 3VMAINOK
AA1 PWROK
PLLB# V2 BATLOW#
CPUPWRGD AG25 CPU_PWRGD 5,8
30 BSRBTN# U1 PWRBTN#
20,30 RSMRST#
R125 2 1 100 1/16W 1%
Y3 RSMRST#
T4 SLP_S3#
T5 SLP_S4#
T6 SLP_S5#
SUSB# 24,30,31,50,53,59,60,61
SUSC# 30,40,49,51,59,61

ICH6-M

PWR_1.05VMAIN
C229 2200pF 25V RK
CPU_THERMTRIP#
C230 2200pF 25V RK None
GND1

PWR_3VSTD
R130 8.2K 1/16W 5%
PLLB# 40
30,60 PMU_PLLB
Q1 2SK3541
GND1

TP3 TESTPAD
CN3 RTC BAT CN
CA52205-4062
C233 0.1uF 16V RK
GND1

PWR_RTCBATT
R131 1K 1/16W 5%
D1
PWR_PMU
R132 1K 1/16W 5%
DAN222M

PWR_RTC
C234 1uF 6.3V RK
CL1 TESTPAD
CL2 TESTPAD
GND1

位置指定

4 CLK_33_ICH
39 PCI_AD[0:31]
CHE G6 PCICLK
PCIRST# R2 PCI_RST# 20,30,31,39
PLT_RST# R5 PLT_RST# 9,20,22,31,36,44,61

PCI_AD0 E2
PCI_AD1 E5
PCI_AD2 C2
PCI_AD3 F5
PCI_AD4 F3
PCI_AD5 E9
PCI_AD6 F2
PCI_AD7 D6
PCI_AD8 E6
PCI_AD9 D3
PCI_AD10 A2
PCI_AD11 D2
PCI_AD12 D5
PCI_AD13 H3
PCI_AD14 B4
PCI_AD15 J5
PCI_AD16 K2
PCI_AD17 K5
PCI_AD18 D4
PCI_AD19 L6
PCI_AD20 G3
PCI_AD21 H4
PCI_AD22 H2
PCI_AD23 H5
PCI_AD24 B3
PCI_AD25 M6
PCI_AD26 B2
PCI_AD27 K6
PCI_AD28 K3
PCI_AD29 A5
PCI_AD30 L1
PCI_AD31 K4

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

C/BE#0 J6 PCI_C/BE#0
C/BE#1 H6 PCI_C/BE#1
C/BE#2 G4 PCI_C/BE#2
C/BE#3 G2 PCI_C/BE#3
PCI_C/BE#[0:3] 39

FRAME# J3 PCI_FRAME# 20,39
DEVSEL# C3 PCI_DEVSEL# 20,39
IRDY# A3 PCI_IRDY# 20,39
TRDY# J2 PCI_TRDY# 20,39
STOP# J1 PCI_STOP# 20,39
PAR E1 PCI_PAR 39
PLOCK# C5 PCI_LOCK# 20

PERR# E3 PCI_PERR# 20,39

PWR_3VSTD
R664 4.7K 1/16W 5%
20,39 PCI_SERR# G5 SERR#
30 PME#_ICH P6 PME#

20,39 PCI_REQ#0 L5 REQ#0
20 PCI_REQ#1 B5 REQ#1
20 PCI_REQ#2 M5 REQ#2
20,39 PCI_REQ#3 B8 REQ#3
20,39 PCI_REQ#4 F7 REQ#4/GPI40
E8 REQ#5/GPI1
20 CPPE#0
20,30 EXTSMI#_ICH B7 REQ#6/GPI0

GNT#0 C1 PCIC PCI_GNT#0 39
GNT#1 B6
GNT#2 E1
GNT#3 C8 LAN MINI_PCI E7 PCI_GNT#3 39 PCI_GNT#4 39
GNT#4/GPO48 F6
GNT#5/GPO17
GNT#6/GPO16 D8

39 USB_OC#0 C27 OC#0
39 USB_OC#1 B27 OC#1
42 USB_OC#2 B26 OC#2
20 USB_OC#3 C26 OC#3
20 USB_OC#4 C23 OC#4/GPI9
20 USB_OC#5 D23 OC#5/GPI10
20 USB_OC#6 C25 OC#6/GPI14
20,41 BLUE_RI# C24 OC#7/GPI15

USBP0P D21 USB_P0+ 39
USBP0N C21 USB_P0- 39
USBP1P B20 USB_P1+ 39
USBP1N A20 USB_P1- 39
USBP2P C19 USB_P2+ 42
USBP2N D19 USB_P2- 42
USBP3P B18 USB_P3+ 41
USBP3N A18 USB_P3- 41
USBP4P D17 USB_P4+ 33
USBP4N E17 USB_P4- 33
USBP5P A16 USB_P5+ 40
USBP5N B16 USB_P5- 40
USBP6P D15 USB_P6+ 37
USBP6N C15 USB_P6- 37
USBP7P B14 USB_P7+ 41
USBP7N A14 USB_P7- 41

Place R124 within 500 mils of ICH.

USBRBIAS_PN
2 1 R124 22.6 1/16W 1%
GND1
USBRBIAS B22
USBRBIAS# A22

C227 2 1 12pF 25V AJ
GND1
X2 FC-135(32KHz) 20ppm
RTCX1 Y1
R126 10M 1/16W 5%
C228 12pF 25V AJ
R127 0 1/16W
RTCX2 Y2
GND1

RTCX1
RTCX2
RTCRST# AA2
INTRUDER# AA3
INTVRMEN AA5

PWR_RTC
R128 10K 1/16W 5% RTC_RST#
R129 1M 1/16W 5% INTRUDER#
C231 1uF 6.3V RK
C232 0.1uF 16V RK
GND1

PIRQ#A N2 PCI_INT#0 20,39
PIRQ#B L2 PCI_INT#1 20,39
PIRQ#C M1 PCI_INT#2 20,39
PIRQ#D L3 PCI_INT#3 20,39
PIRQ#E/GPI2 D9 PCI_INT#4 20,39
PIRQ#F/GPI3 C7 PCI_INT#5 20
PIRQ#G/GPI4 C6 PCI_INT#6 20
PIRQ#H/GPI5 M3 CPPE#1_ICH 20

ICH6-M

PWR_RTC
R585 330K 1/16W 5%

内蔵1.5VLDOストラップオプション

[Refference:Greek]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
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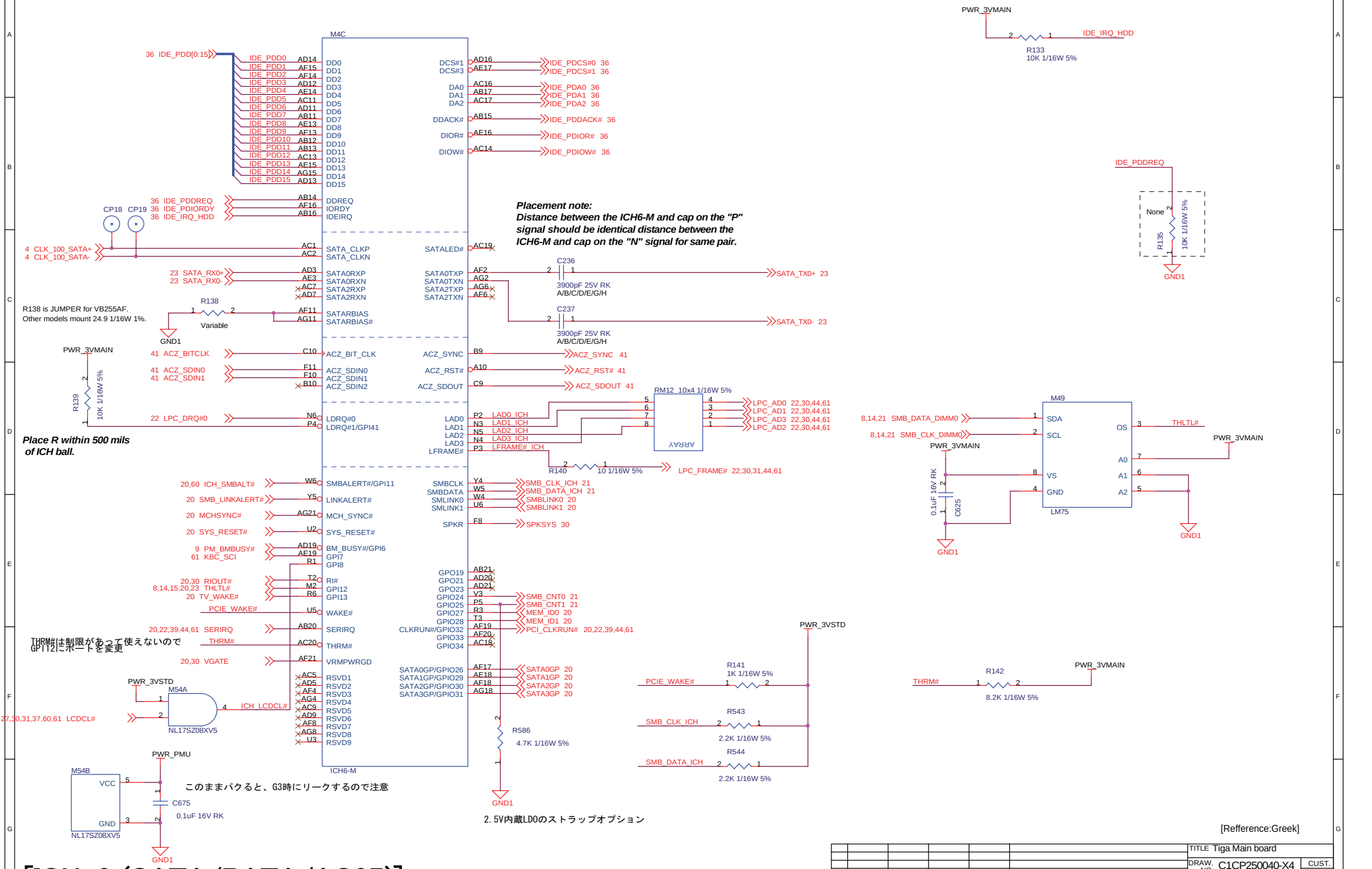
TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 17 / 66

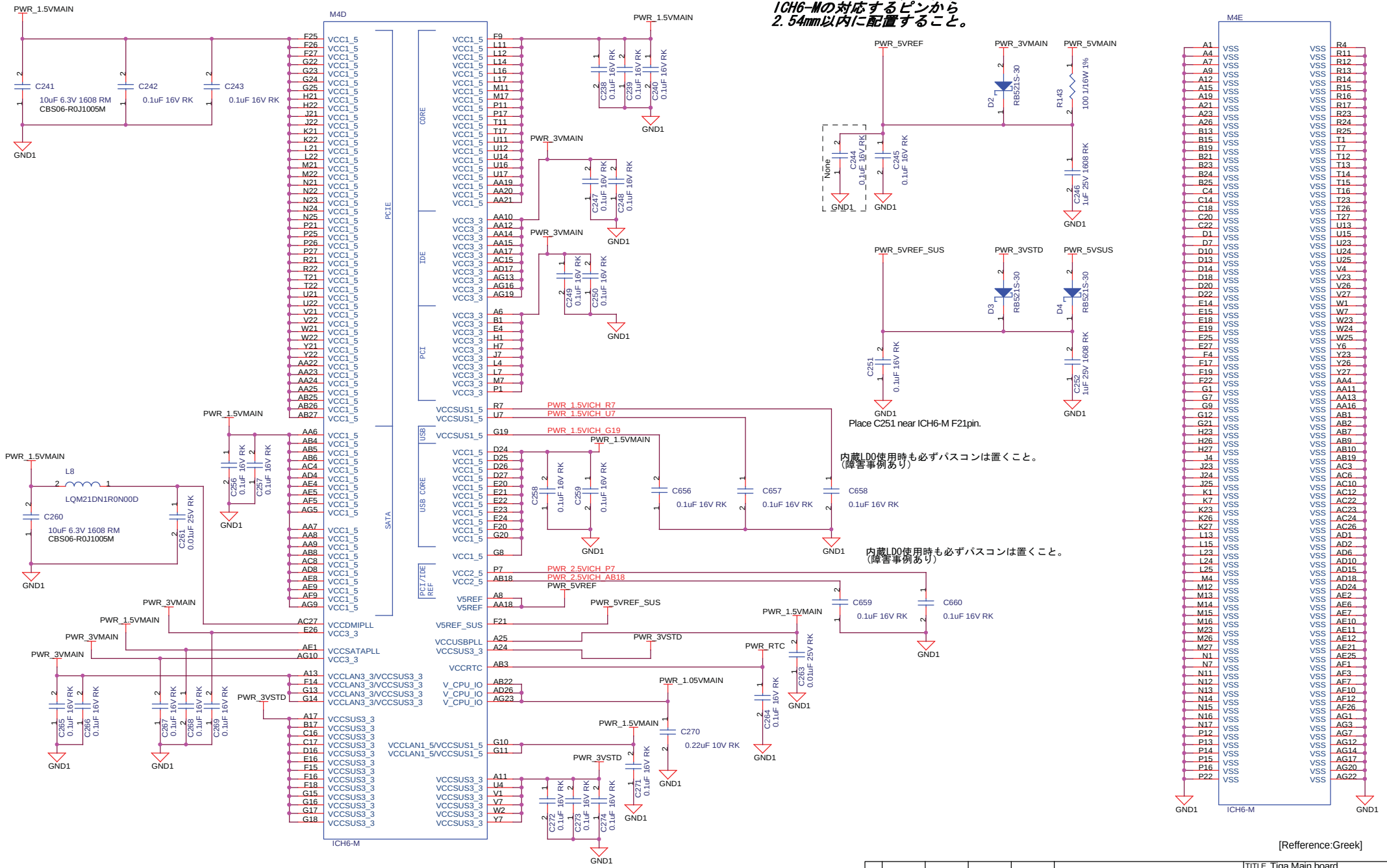


[ICH-2 (SATA/PATA/AC97)]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	DESIGN		CHECK	APPR.		

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 18 / 66

このページのコンデンサは
ICH6-Mの対応するピンから
2.54mm以内に配置すること。



Place C251 near ICH6-M F21pin.

内蔵LDO使用時も必ずパスコンは置くこと。
(障害事例あり)

内蔵LDO使用時も必ずパスコンは置くこと。
(障害事例あり)

[Refference:Greek]

[ICH-3 (POW)]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK		APPR.

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 19 / 66

M7

ICH6-M

PWR_3VSUS

17 USB_OC#4 — R144 100K 1/16W 5% — 1 2

17 USB_OC#3 — R146 100K 1/16W 5% — 1 2

PWR_3VS

RM15

17 USB_OC#5
17,41 BLUE_RI#
17 USB_OC#6

100Kx4 1/16W 5%

PWR_3VMAIN

RM14

17,39 PCI_INT#4
17 CPPE#0
17,39 PCI_REQ#3
17,30 EXTSMI#_ICH

10Kx4 1/16W 5%

RM16

17 PCI_INT#5
17 PCI_INT#6
17,39 PCI_IRDY#
17,39 PCI_INT#0

10Kx4 1/16W 5%

PWR_3VSTD

18 MEM_ID1 — R147 8.2K 1/16W 5%

18 MEM_ID0 — R148 8.2K 1/16W 5%

RM17

18,22,39,44,61 PCI_CLKRUN#
17,39 PCI_REQ#4
17,39 PCI_REQ#0
17,39 PCI_INT#3

10Kx4 1/16W 5%

PWR_1.5VMAIN

C275 0.1uF 16V RK
C276 0.1uF 16V RK
C277 0.1uF 16V RK
C278 0.1uF 16V RK
C279 0.1uF 16V RK

GND1

PWR_3VSTD

RM18

18 SYS_RESET#
18 SMBLINK1
18 TV_WAKE#
8,14,15,18,23 THLTL#

10Kx4 1/16W 5%

PWR_3VMAIN

RM19

17,39 PCI_INT#2
17 PCI_REQ#2
17 CPPE#1_ICH
17,39 PCI_INT#1

10Kx4 1/16W 5%

RM20

18,60 ICH_SMBALT#
18 SMBLINK0
18 SMB_LINKALERT#
18,30 RIOUT#

10Kx4 1/16W 5%

18,22,39,44,61 SERIRQ — R149 8.2K 1/16W 5%

C280 330pF 50V RK None

GND1

PWR_1.5VMAIN

C281 0.1uF 16V RK
C282 0.1uF 16V RK
C283 0.1uF 16V RK

GND1

PWR_3VMAIN

RM21

17 PCI_REQ#1
17 PCI_LOCK#
17,39 PCI_DEVSEL#
17,39 PCI_PERR#

10Kx4 1/16W 5%

RM22

18 SATA3GP
18 SATA2GP
18 SATA1GP
18 SATA0GP

10Kx4 1/16W 5%

PWR_3VMAIN

RM23

17,39 PCI_SERR#
17,39 PCI_FRAME#
17,39 PCI_TRDY#
17,39 PCI_STOP#

10Kx4 1/16W 5%

PWR_3VMAIN

18 MCHSYNC# — R150 10K 1/16W 5%

9,17,22,31,36,44,61 PLT_RST# — R151 10K 1/16W 5%

17,30,31,39 PCI_RST# — R152 10K 1/16W 5%

GND1

18,30 RIOUT# — None C284 100pF 25V AJ
18,30 VGATE — None C285 100pF 25V AJ
9,17,21,30,31,32,39 3VMAINOK — None C286 100pF 25V AJ
17,30 RSMRST# — None C287 100pF 25V AJ
17,61 KBC_INIT# — None C288 100pF 25V AJ

GND1

Those capacitors must close the M6 (GMCH)

[Refference:Greek]

[ICH PU,CAP/PCI PU]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

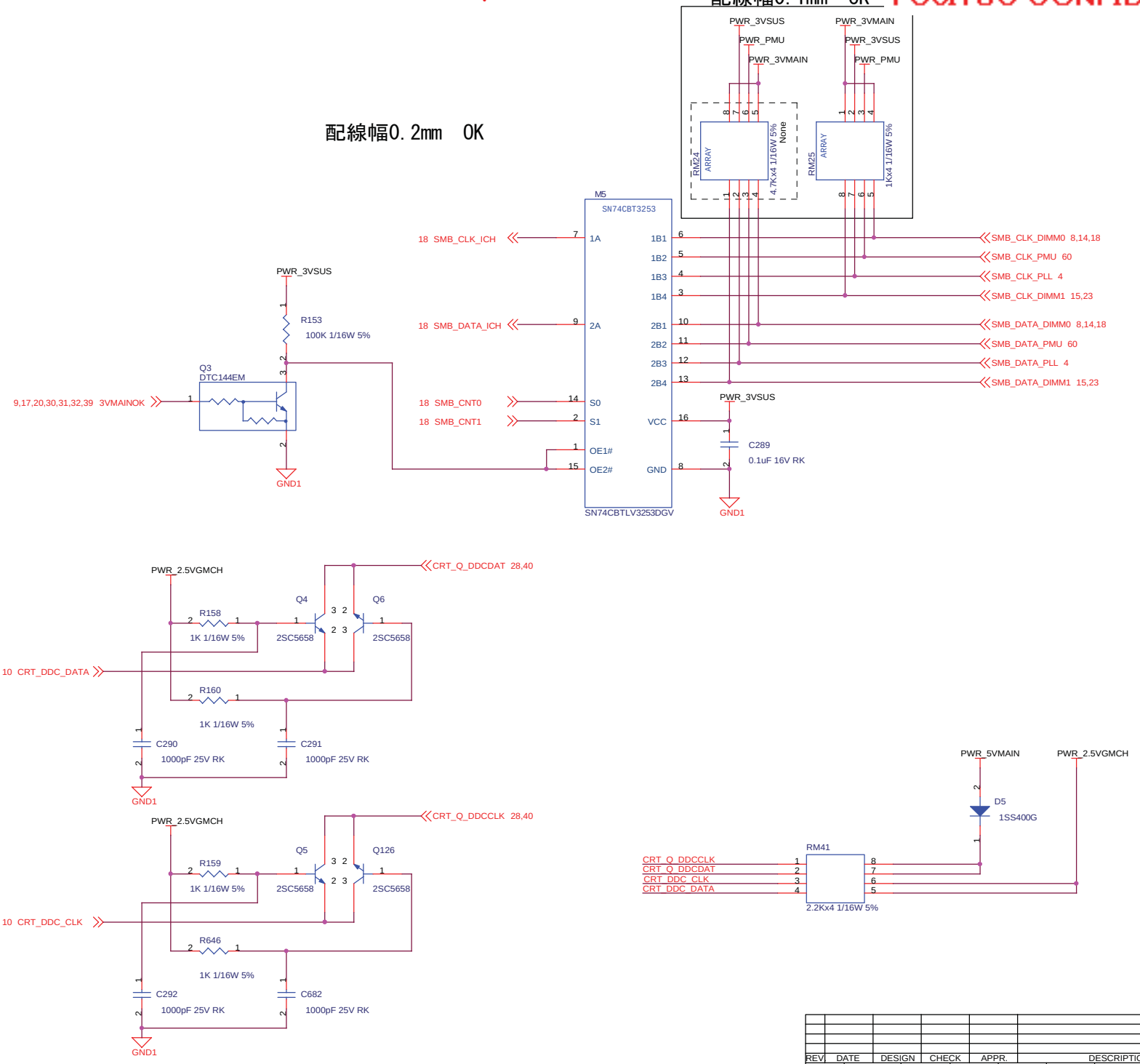
TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 20 / 66

配線幅0.1mm OK

配線幅0.2mm OK



[Refference:Greek]

[SMBus]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 21 / 66

#05(F0205A19559)
Mount R161 for
VB238AF.

R161
1 2
0 1/16W
F

CLK_33_F_TP

M6

4 CLK_33_FWH → CLK (7)

FWH0 (21) → LPC_AD0 18,30,44,61
FWH1 (22) → LPC_AD1 18,30,44,61
FWH2 (23) → LPC_AD2 18,30,44,61
FWH3 (25) → LPC_AD3 18,30,44,61
FWH4 (31) → LPC_FRAME# 18,30,31,44,61

30 FWHTBL# → TBL# (16)
30 FWHWP# → WP# (15)
17 FWHINIT# → INIT# (32)
9,17,20,31,36,44,61 PLT_RST# → RST# (10)

ID0 (20)
ID1 (19)
ID2 (18)
ID3 (17)

PWR_3VMAIN
37,45 LCDID0 → FGPI0 (14)
FGPI1 (13)
FGPI2 (12)
FGPI3 (11)
FGPI4 (6)

RFU0 (29)
RFU1 (28)
RFU2 (27)
RFU3 (26)

PWR_3VMAIN → IC (5)

PWR_3VMAIN
R162 100K 1/16W 5%
37,45 LCDID0 → 2 1

NC0 (1)
NC1 (2)
NC2 (3)
NC3 (9)

VCC0 (8)
VCC1 (30)

PWR_3VMAIN
C293
0.1uF 16V RK

GND0 (4)
GND1 (24)

GND1
PWR_3VMAIN
GND1

SST49LF008A(FWH)

PWR_3VMAIN
PWR_5VMAIN

CN4

Need to pull-down on subboard(Not connect directly to GND).

30,31 TPNL_EXIST# → 5
4 CLK_14_SIO → 6
18,30,44,61 LPC_AD0 → 8
18,30,44,61 LPC_AD1 → 9
18,30,44,61 LPC_AD2 → 10
18,30,44,61 LPC_AD3 → 11
18,30,31,44,61 LPC_FRAME# → 12
18 LPC_DRQ#0 → 13
9,17,20,31,36,44,61 PLT_RST# → 14
17 SUSTAT# → 15
18,20,39,44,61 PCI_CLKRUN# → 16
CLK_33_F_TP → 18
18,20,39,44,61 SERIRQ → 20

TP CN
F

GND1

PWR_3VMAIN
C680
0.1uF 16V RK
F
GND1

PWR_5VMAIN
C681
0.1uF 16V RK
F
GND1

[Refference:Greek]

[FWH/TP]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 22 / 66

※BAY_CN側に搭載

T0	33	PD	0: 1:
T1	34	PU	0: 1:
T2	35	PD	0: Disable SATA SS clocking 1: Enable SATA SS Clocking
T3 T4	36 37	PD PD	T[4,3] 00: 20MHz 01: 25MHz 10: 30MHz 11: 40MHz
T5	38	PU	0: Adjust UDMA mode 1: Fixed UDMA mode
T6	39	PD	0: Power Mode disable 1: Power Mode Enable
T7	40	PD	0: Unplugged SATA cable 1: Plugged SATA cable
CNFG0 CNFG1 CNFG2	18 19 20	PD PU PD	CNFG[2,1,0] 000: Device Mode 100MB/s. 001: Device Mode 133MB/s. 010: Device Mode 150MB/s. 011: Reserved. 100: Host Mode 100MB/s. 101: Host Mode 133MB/s. 110: Host Mode 150MB/s. 111: Reserved.
ATAIOSEL	21	PU	0: Disable the output to ATA 1: enable the output to ATA

*Note:
Device Mode: Host (SATA) Bridge (PATA) HDD
Host Mode: Host (PATA) Bridge (SATA) Bridge (PATA) HDD

Place this Register near IC

#05(F0205A19559)
M7 : Add CA46740-0906 for VB238AG and AH.
#06(F0206A04590)
M7 : Add CA46740-0906 for VB238AA,AB,AC,AD and AE.

常に最新の状況を確認して下さい。

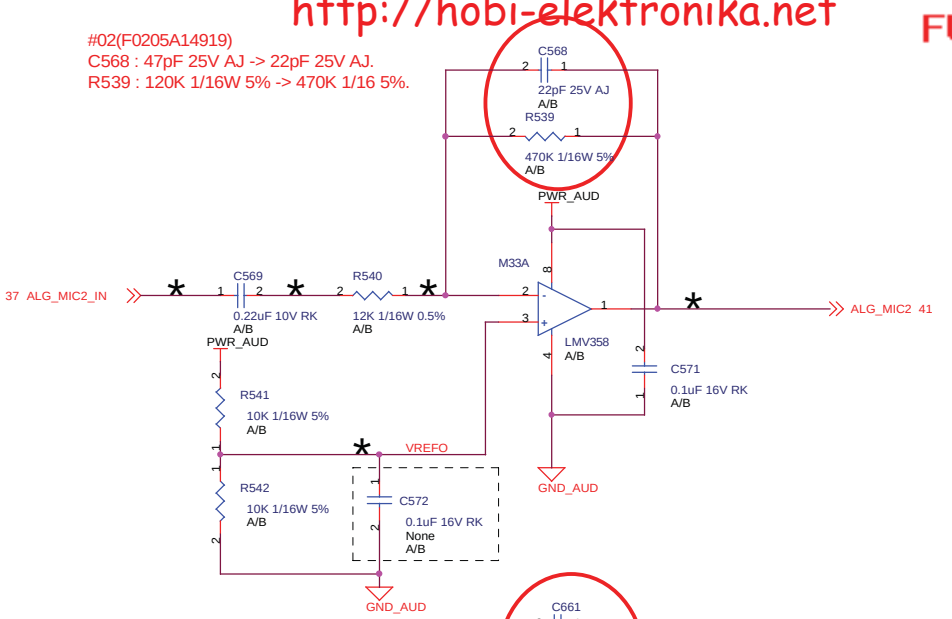
[SATA to PATA]

[Refference:Greek]

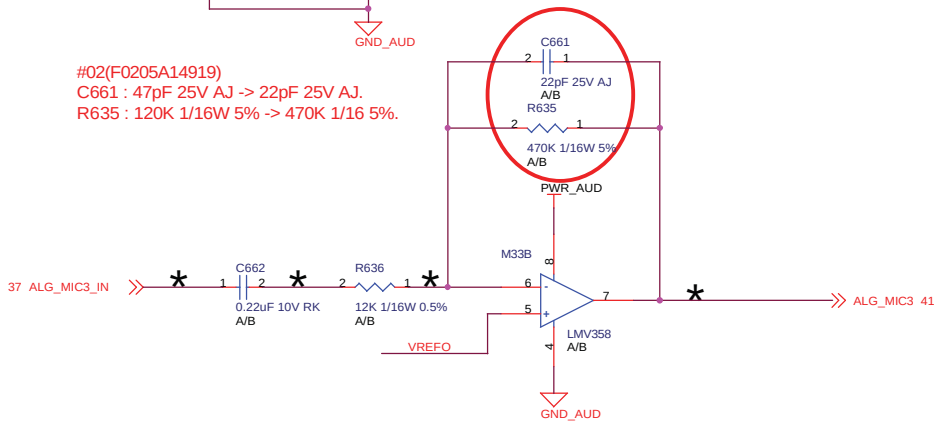
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 23 / 66

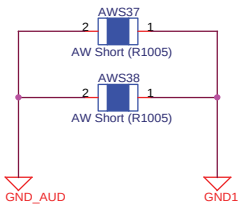
#02(F0205A14919)
C568 : 47pF 25V AJ -> 22pF 25V AJ.
R539 : 120K 1/16W 5% -> 470K 1/16 5%.

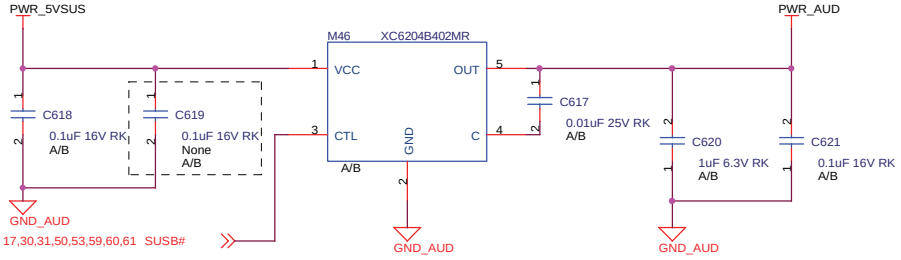


#02(F0205A14919)
C661 : 47pF 25V AJ -> 22pF 25V AJ.
R635 : 120K 1/16W 5% -> 470K 1/16 5%.



fc(min)=72.3Hz(10K,0.22uF)
fc=15.9KHz(100K,100pF)
fc=72.3Hz(10K,0.22uF)
G=20dB



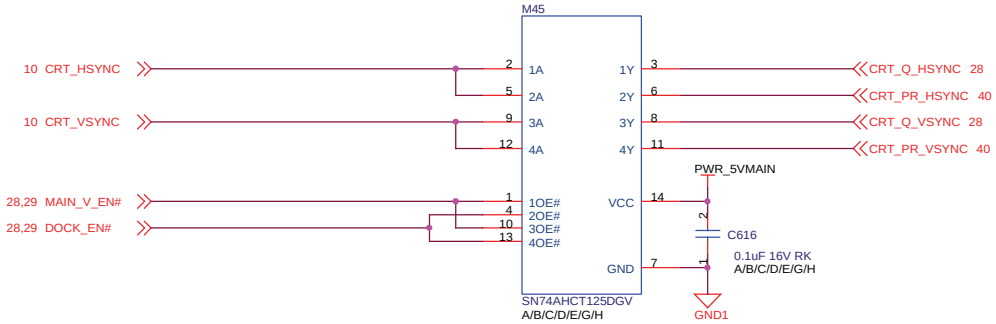


[Refference:POLTER]

Int-Mic AMP

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 24 / 66



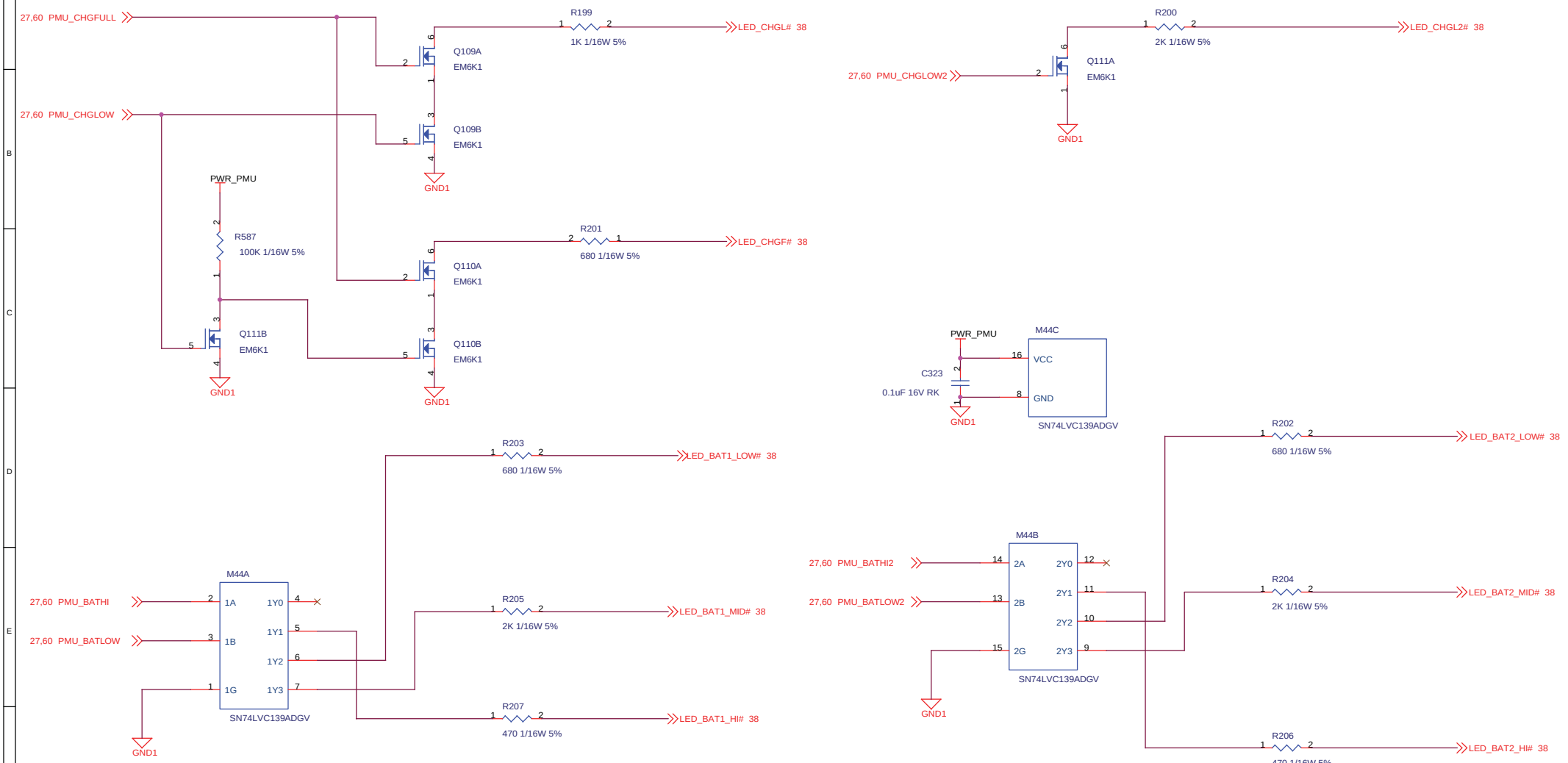
[Level Shift Buffer]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 25 / 66



[Status LED Signal1]

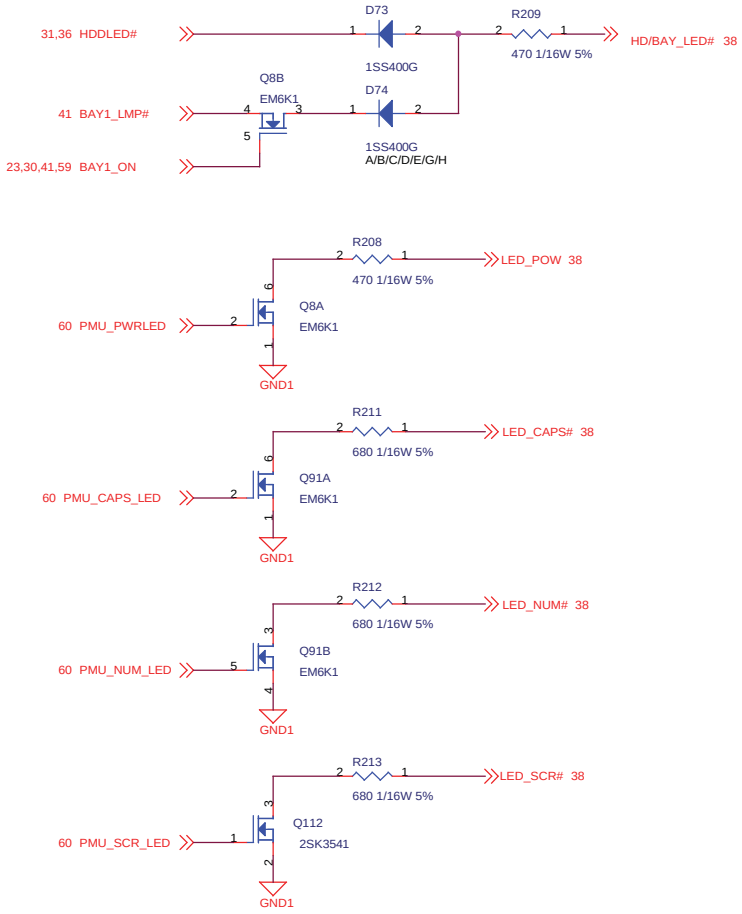
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

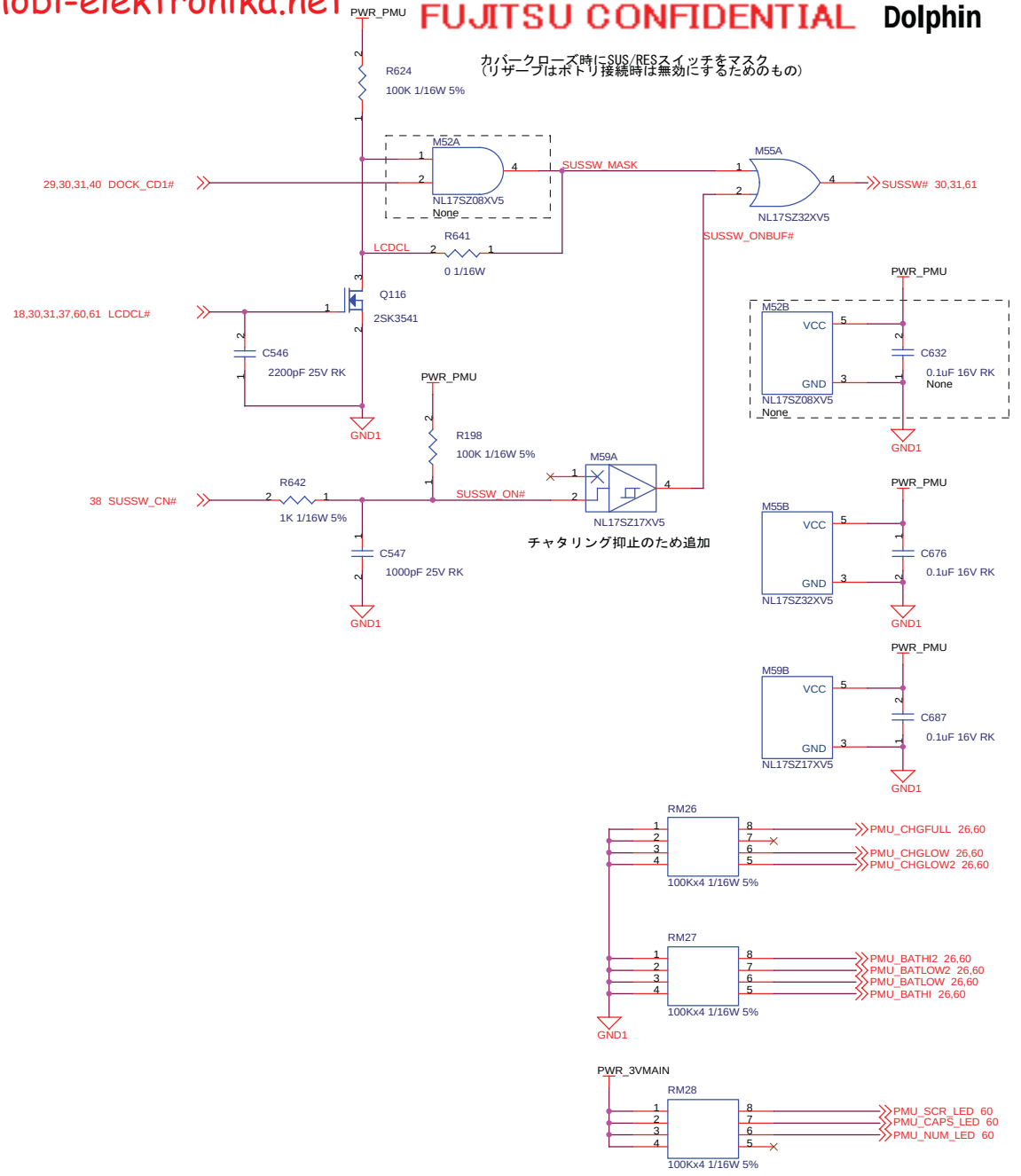
TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 26 / 66

ダイオードがないと、デバイス認識おかしくなるので取らないように。

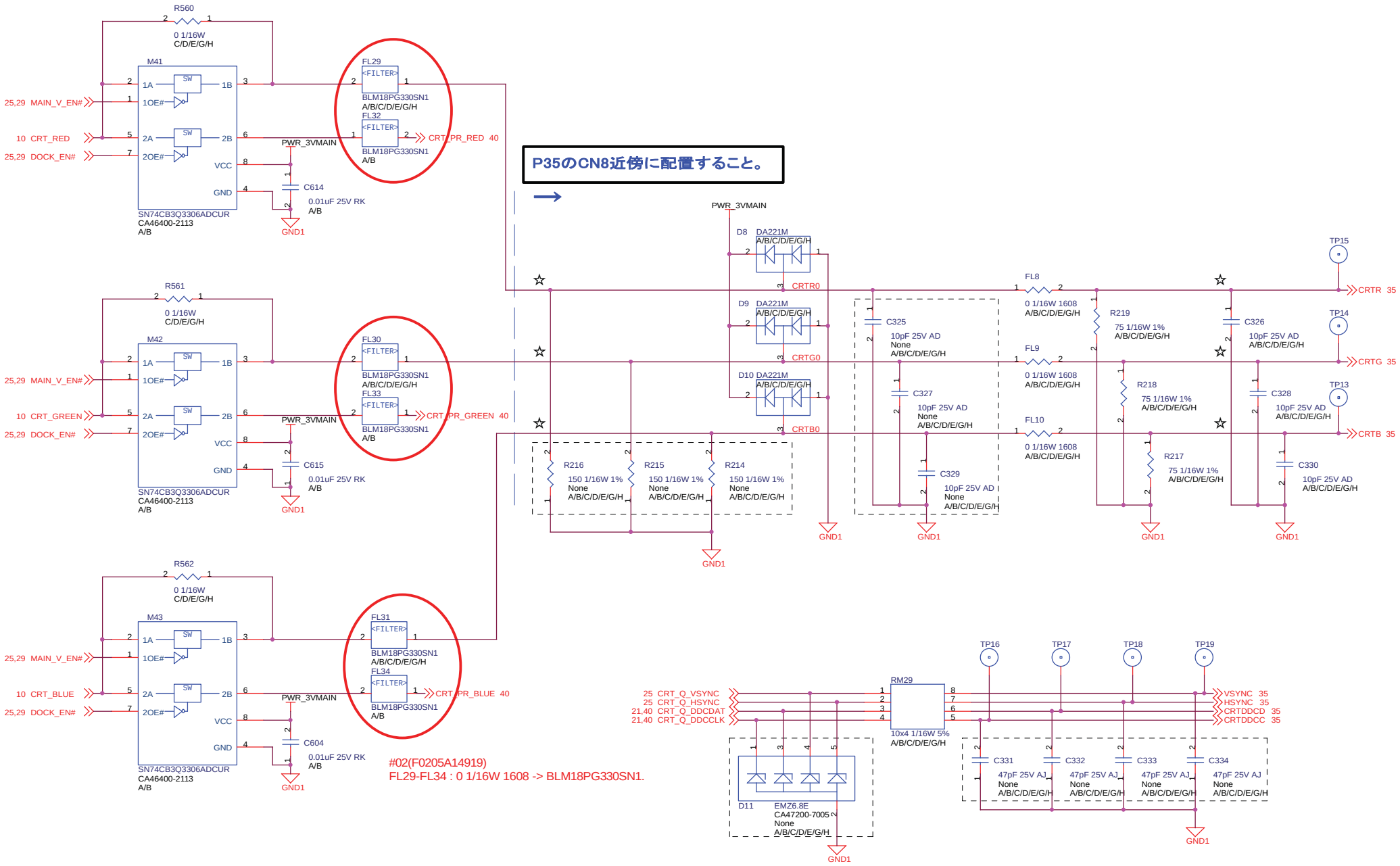




[Status LED Signal2]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 27 / 66



[CRT]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 28 / 66

FUJITSU CONFIDENTIAL

Dolphin

○国内店頭モデル○
・以下の部品はリザーブ
M34,M35,C601−C603
・以下の部品はマウント
R557−R559

PWR_3VMAIN
M34B
VCC 5
GND 3
NL17SZ08XV5
A/B
C601
0.1uF 16V RK
A/B
GND1

27,30,31,40 DOCK_CD1#
R650
100K 1/16W 5%
C/D/E/G/H
M34A
NL17SZ08XV5
A/B
C603
1000pF 25V RK
None
A/B
GND1
DOCK_EN# 25,28

PWR_3VMAIN
R576
10K 1/16W 5%
A/B
Q106
2SK3541
A/B
R651
100K 1/16W 5%
C/D/E/G/H
GND1
MAIN_V_EN# 25,28

点線より右の部品はCN8の近くにおくこと(P35)

R572
0 1/16W
None
A/B/C/D/E/G/H
TV_PR_LUNA 40
R558
0 1/16W
C/D/E/G/H
M39
SN74CB3Q3306ADCUR
CA46400-2113
A/B
10 TV_LUNA
MAIN_V_EN#
DOCK_EN#
TV_LUNA_A
PWR_3VMAIN
C602
0.01uF 25V RK
A/B
GND1

C338
33pF 25V AJ
None
A/B/C/D/E/G/H
FL12
<FILTER>
BLM11A121S
A/B/C/D/E/G/H
PWR_3VMAIN
D13
DA221M
A/B/C/D/E/G/H
GND1
TP21
TV_LUNA_Q 35
R221
75 1/16W 1%
A/B/C/D/E/G/H
C339
100pF 25V AJ
A/B/C/D/E/G/H
C340
270pF 50V RK
A/B/C/D/E/G/H
GND1

M40
SN74CB3Q3306ADCUR
CA46400-2113
A/B
10 TV_CHROMA
MAIN_V_EN#
DOCK_EN#
TV_CHROMA_A
PWR_3VMAIN
C613
0.01uF 25V RK
A/B
GND1
R559
0 1/16W
C/D/E/G/H
R573
0 1/16W
None
A/B/C/D/E/G/H
TV_PR_CHROMA 40

C341
33pF 25V AJ
None
FL13
<FILTER>
BLM11A121S
A/B/C/D/E/G/H
PWR_3VMAIN
D14
DA221M
A/B/C/D/E/G/H
GND1
TP22
TV_CHROMA_Q 35
R222
75 1/16W 1%
A/B/C/D/E/G/H
C342
100pF 25V AJ
A/B/C/D/E/G/H
C343
270pF 50V RK
A/B/C/D/E/G/H
GND1

[S−out]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 29 / 66

#050827
M13-46pin : PMU_SMI -> PMUSMI_M.
#050827B
M13-41pin : PMU_PARST# -> PWR_PMU.
M13-42pin : PMU_PE# -> PWR_PMU.
M13-45pin : PMU_PRM# -> PWR_PMU.
#050827C
M13-46pin : PMUSMI_M -> PMU_SMI.

(miniPCI Wireless LAN)
(Realtek LAN)

(PCIC,1394)

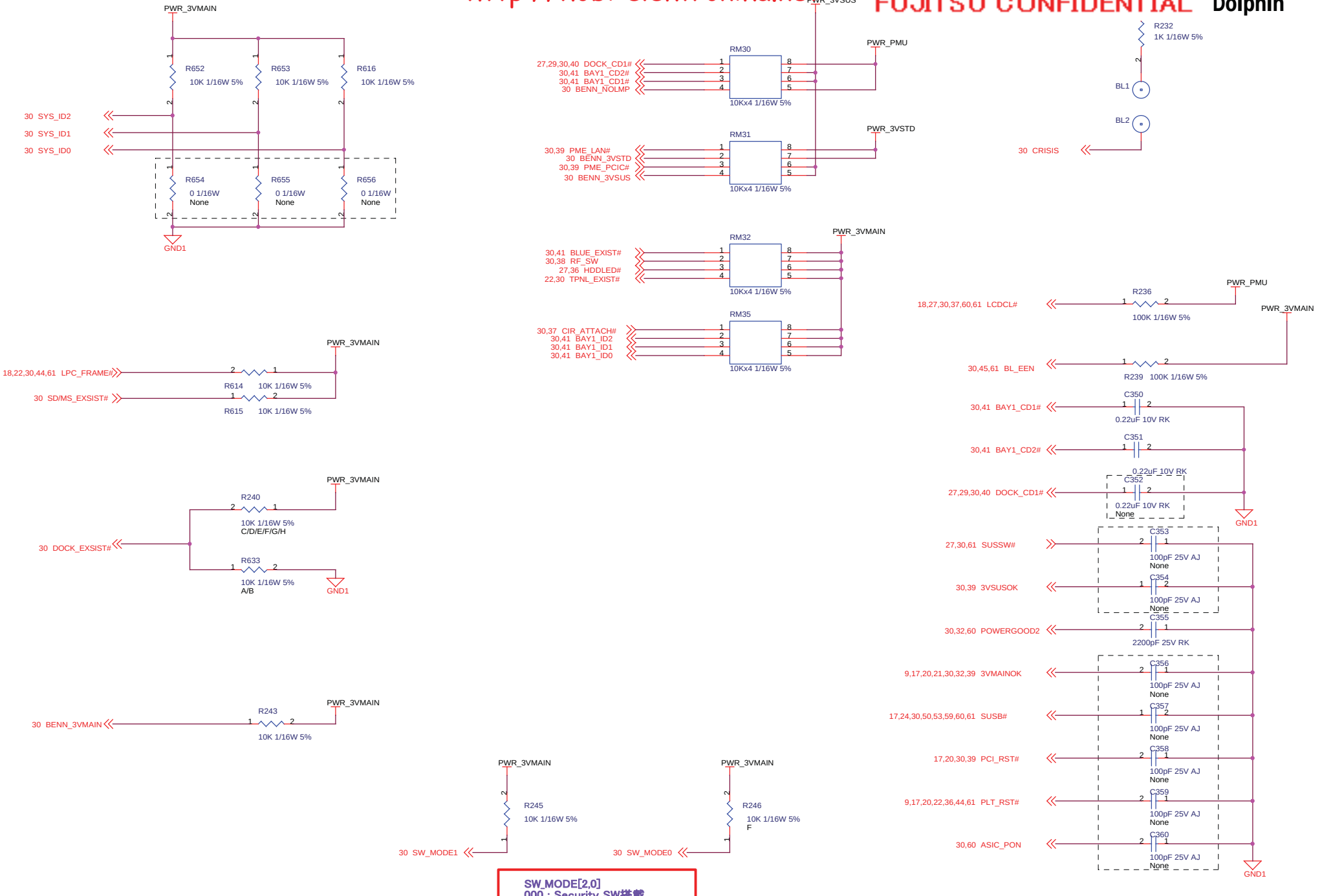
この回路は推奨しません

[Refference:Greek]

[ASIC]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK		APPR.

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 30 / 66



[ASIC PU]

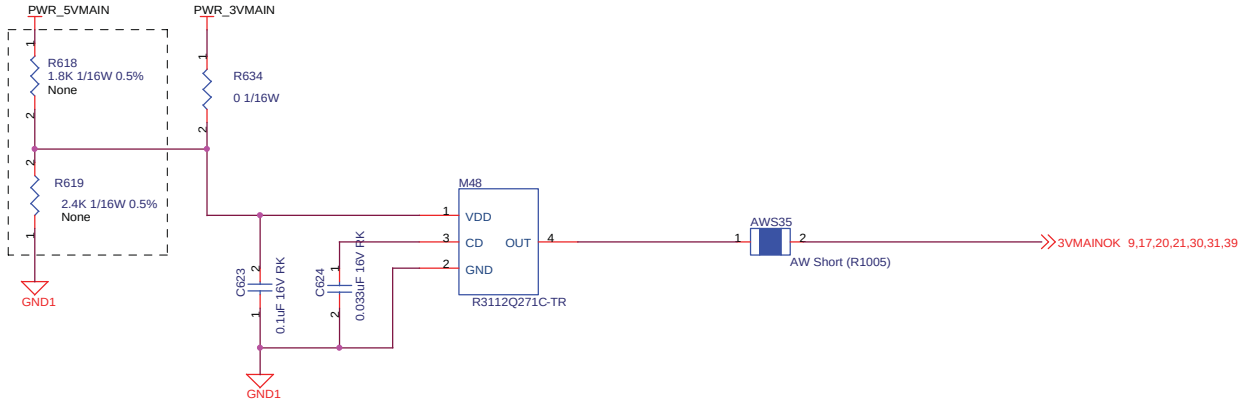
[Refference:Greek]

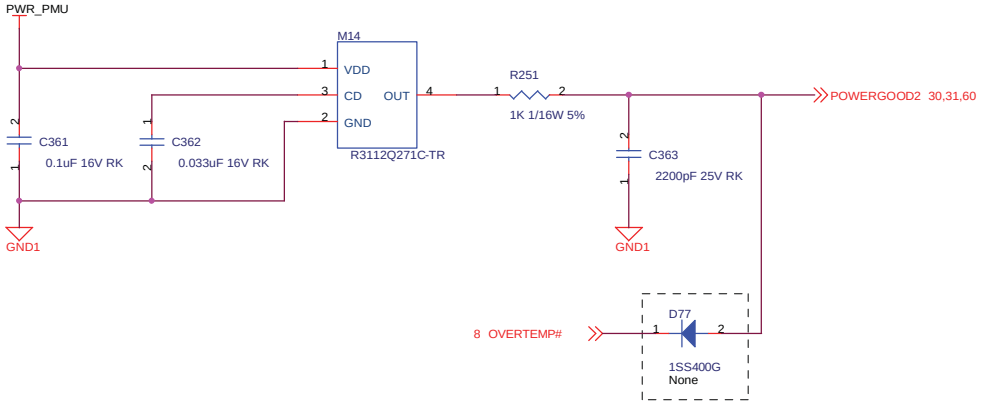
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 31 / 66





[Refference:Greek]

[RESET IC]

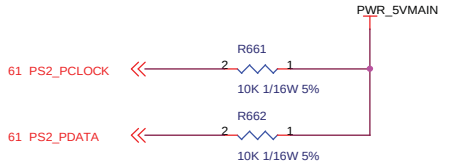
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE		DESIGN	CHECK	APPR.	

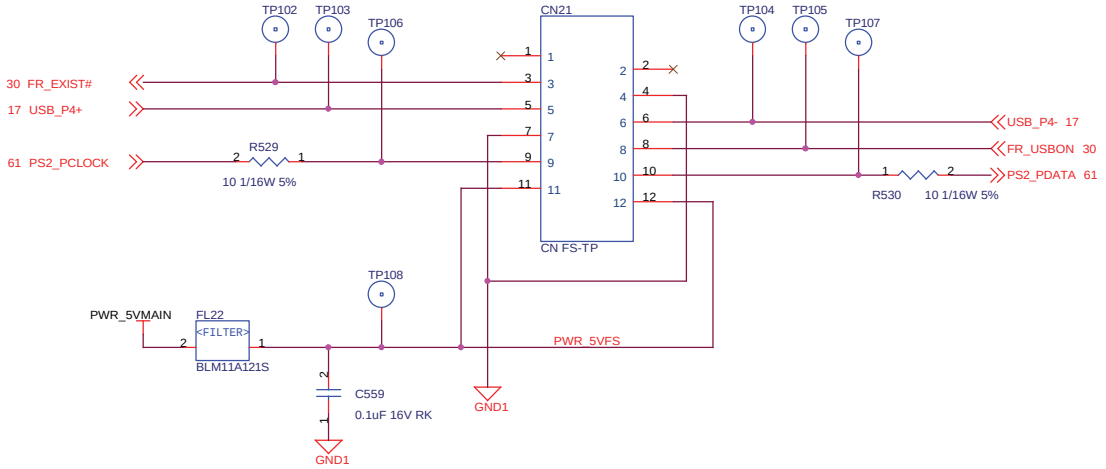
TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

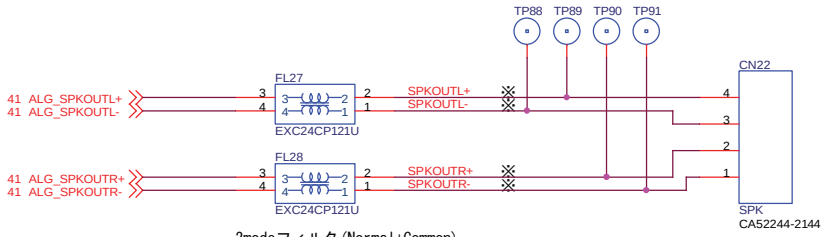
FUJITSU LTD. SHEET 32 / 66

こっちにプルアップを置いておくと、LUNA側に5V引っ張らなくて良い





制御していない



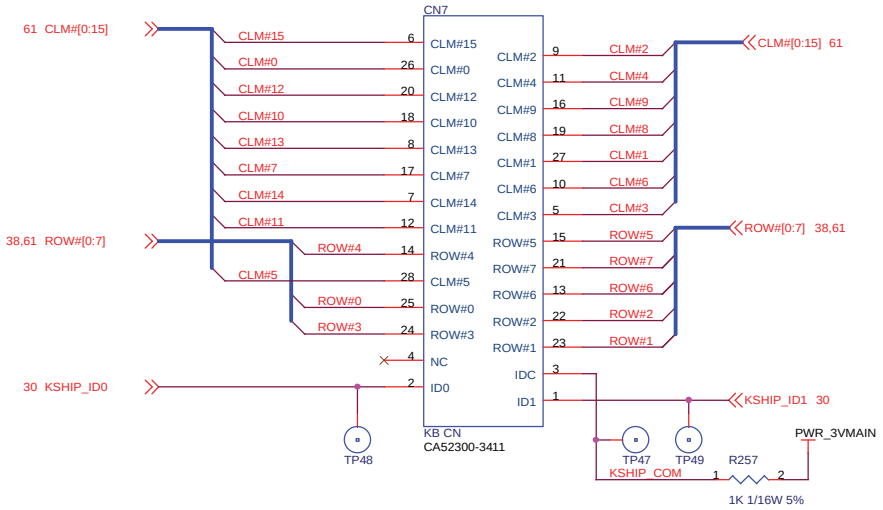
2modeフィルタ(Normal+Common)
ケータイを近づけた時にノイズを拾うような場合には効果あり

[CN FS_TP-SPK]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 33 / 66

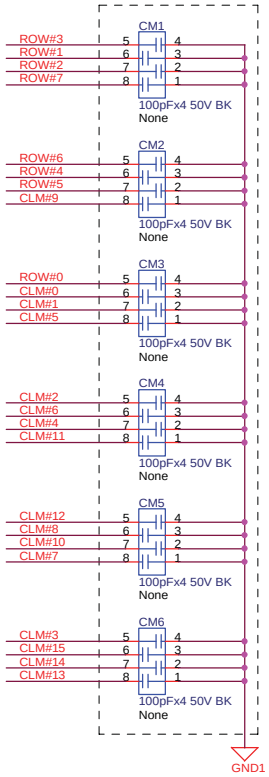
KeyBoard Connector



TPはコネクタからはなれた場所でも,かまいません。
ただし、すべて同一面に搭載すること。

Keyboard Strap (N86C-7664-0203-E)

	ID1:ID0 (KBC Side)
JP	1 1
US	1 0
UK	0 1

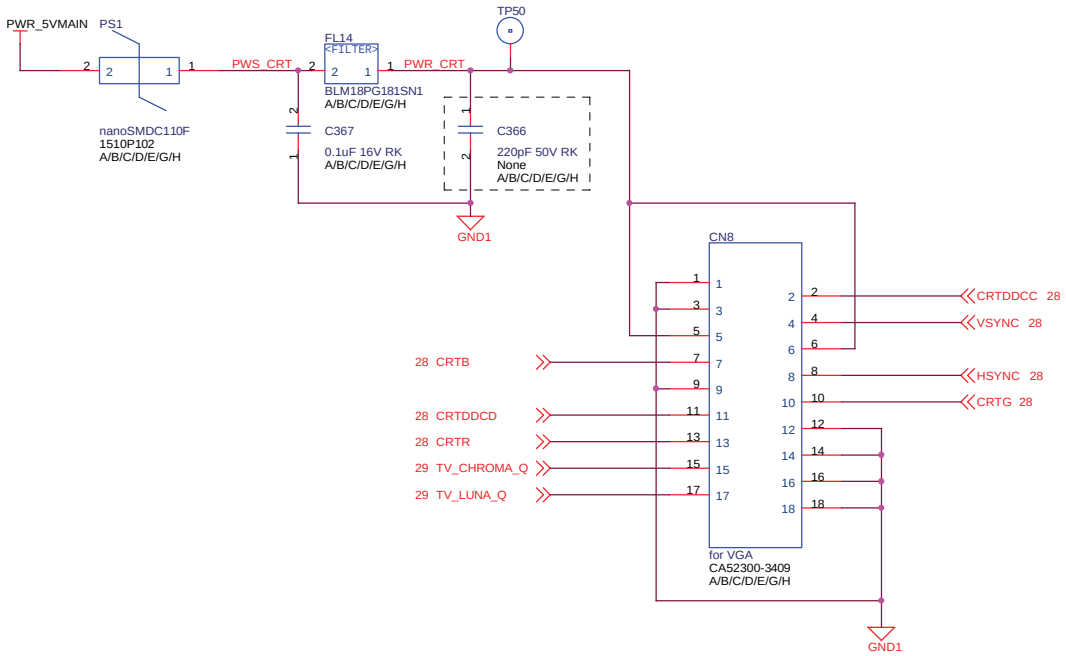


[Refference:Zest]

[CN Keyboard]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK		APPR.

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 34 / 66



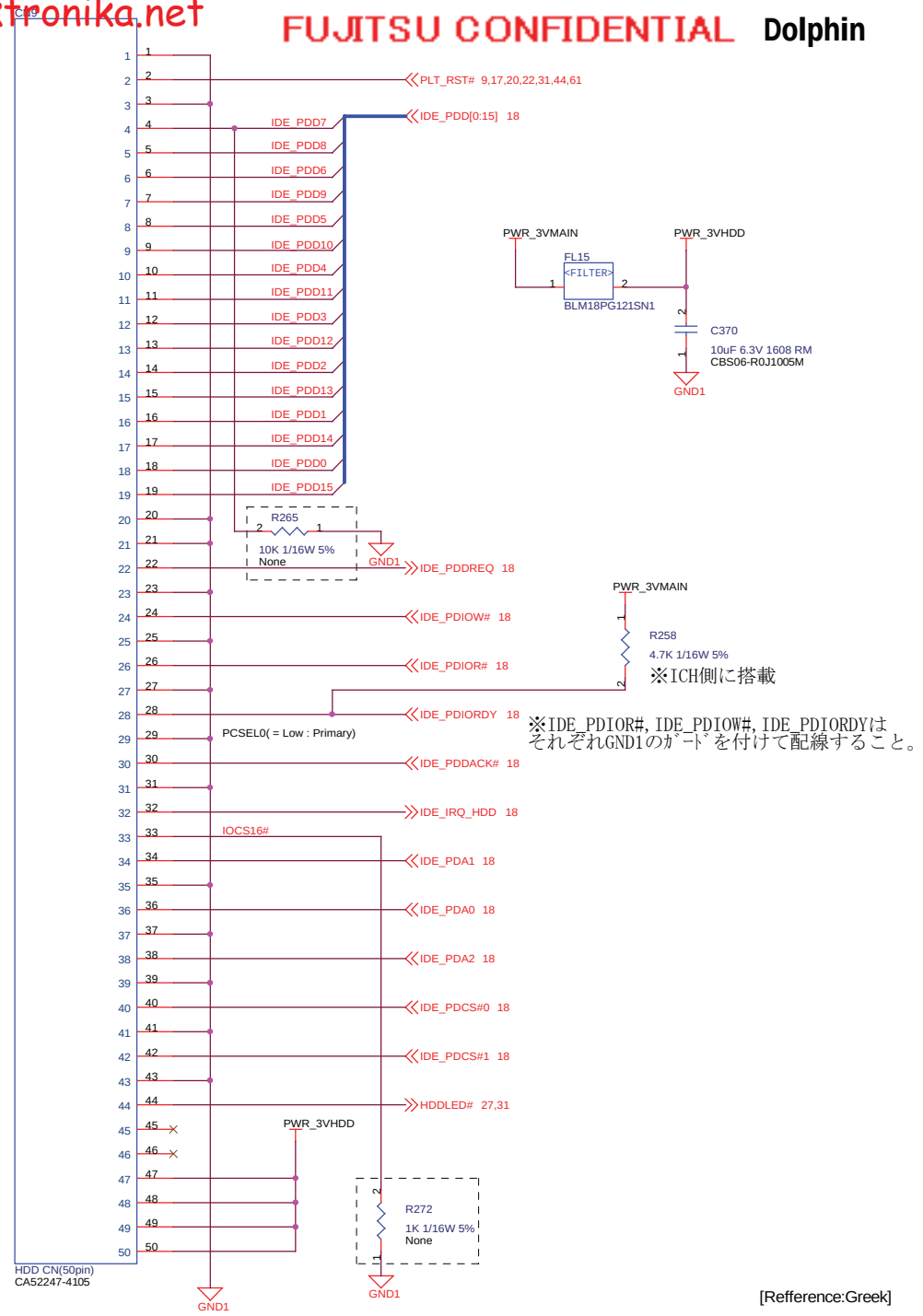
[CN VGA/S-out]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 35 / 66

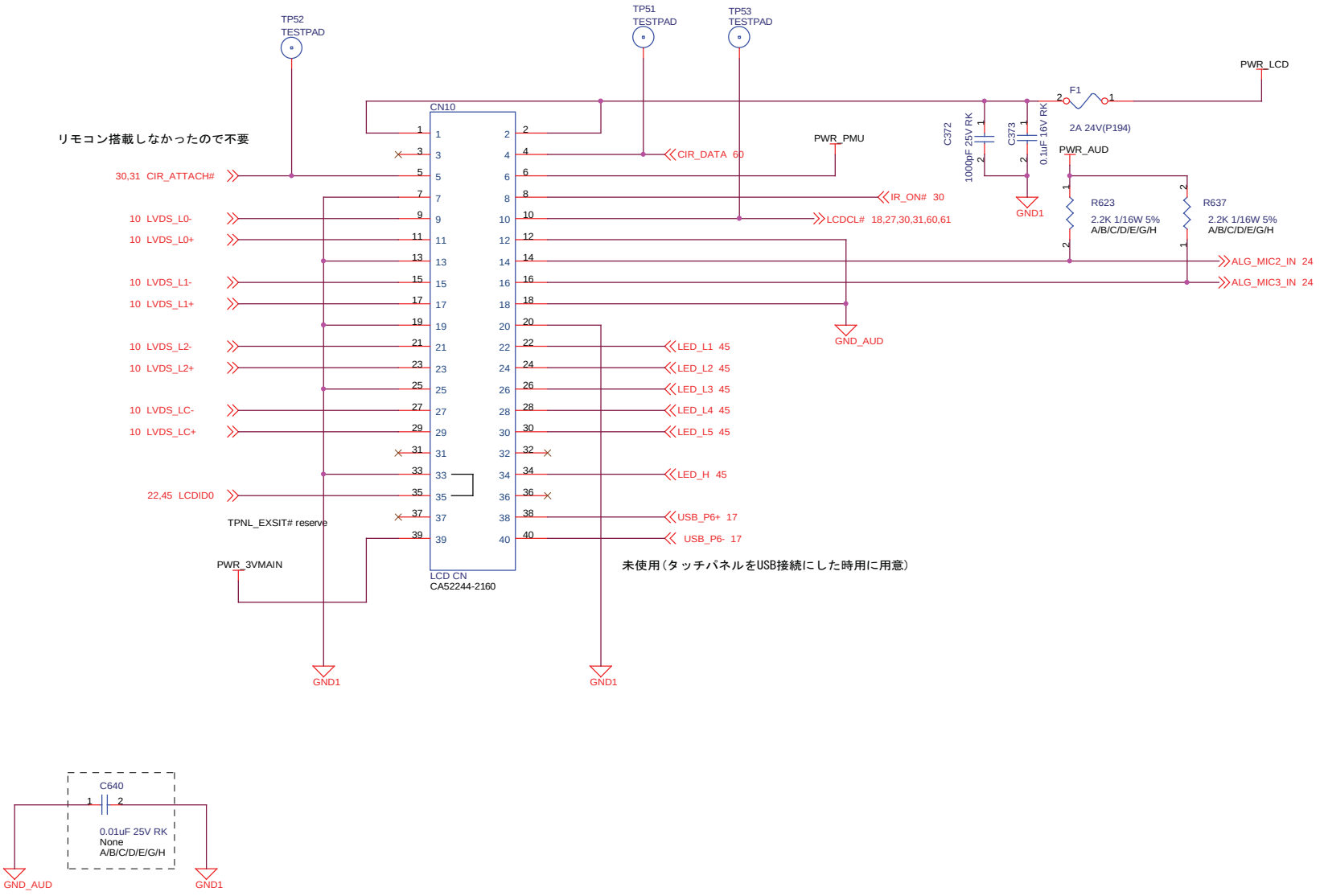


[Refference:Greek]

[CN HDD(PATA)]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 36 / 66



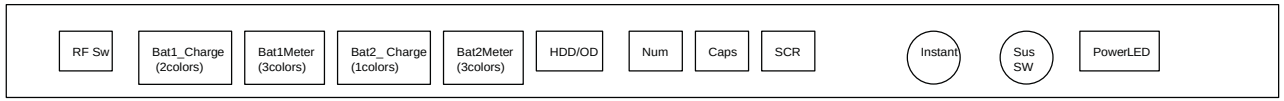
[CN LCD INV]

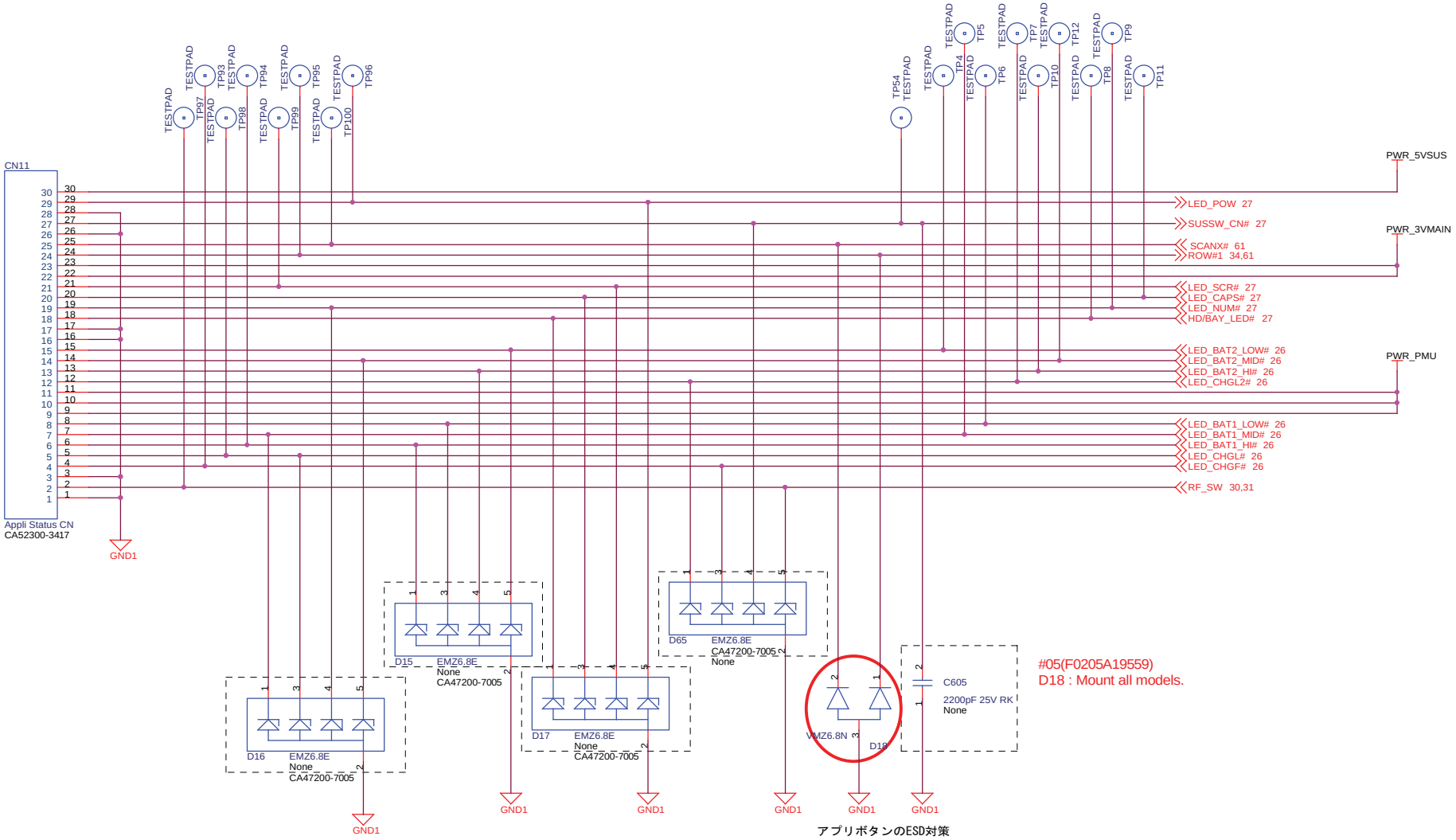
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 37 / 66





[Refference:Pumpkin]

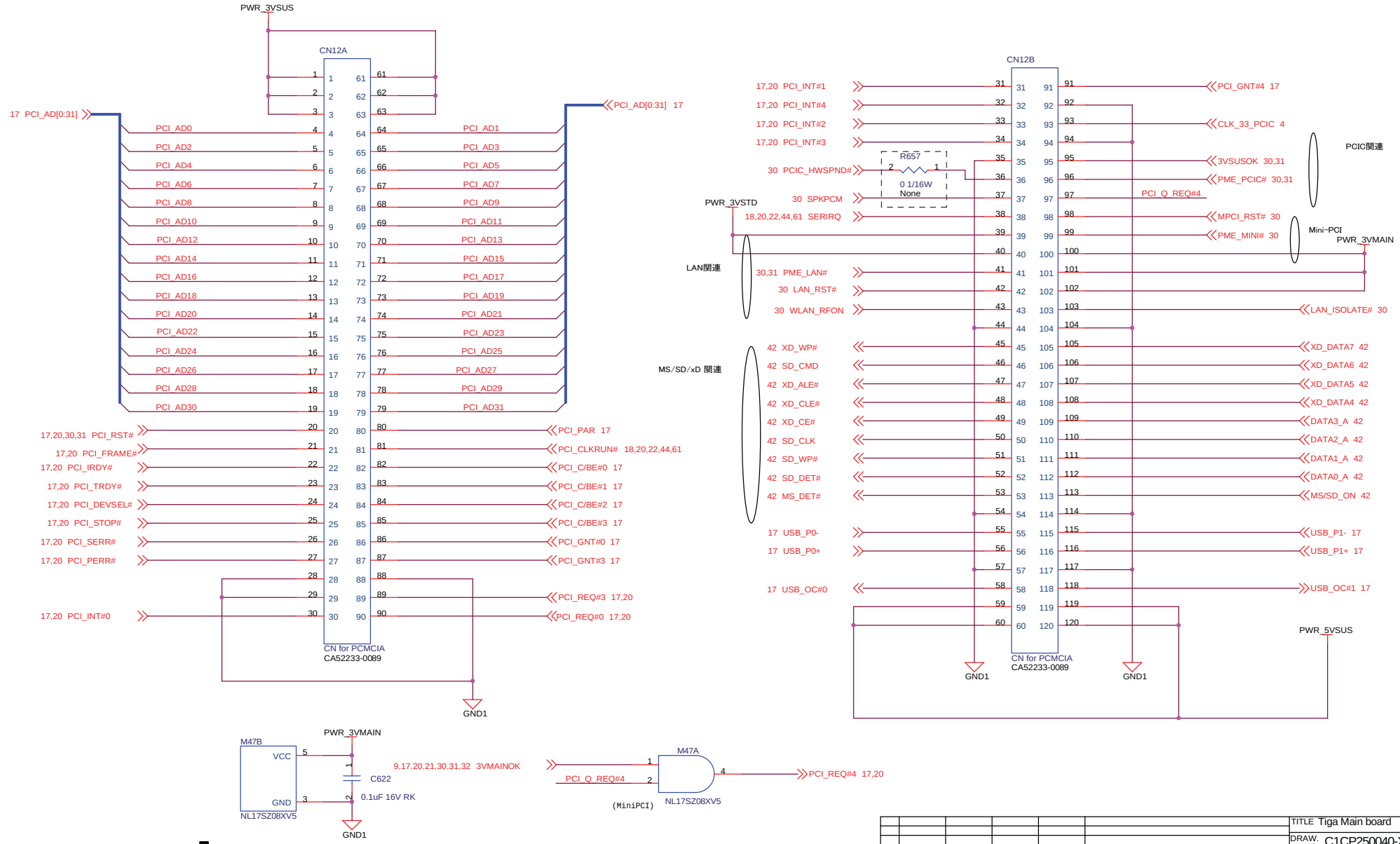
[CN APPLI ST-LED]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 38 / 66



[CN for PCMCIA]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 39 / 66

LAN	USBx1	Lineout	S-OUT	CRT	USBx2	AC

TIGA

Docking CN

[CN DOCK]

PWR_EXTDCIN

FL19 <FILTER> BLM18PG330SN1 A/B

FL20 <FILTER> BLM18PG330SN1 A/B

CN20

1(Pow) 2(Pow) 28(Pow) 29(Pow)

GND1

21,28 CRT_Q_DDCCLK

21,28 CRT_Q_DDCDAT

25 CRT_PR_HSYNC

25 CRT_PR_VSYNC

28 CRT_PR_BLUE

28 CRT_PR_GREEN

28 CRT_PR_RED

GND_AUD

41 ALG_OUTA_DOCK_R

41 ALG_OUTA_DOCK_L

RJ45 CN

8

7

6 RX−

5

4

3 RX+

2 TX−

1 TX+

CN5

8 TRD3- DOCK

7 TRD3+ DOCK

RX- 6 TRD1- DOCK

5 TRD2- DOCK

4 TRD2+ DOCK

RX+ 3 TRD1+ DOCK

TX- 2 TRD0- DOCK

TX+ 1 TRD0+ DOCK

LAN RELAY CN CA52244-2118 A/B

61 AC_CUT

PR CN CA52248-8103 A/B

GND1

C641 0.01uF 25V RK None A/B

GND_AUD

GND1

USB_P5+ 17

USB_P5- 17

USB5 to USB−Hub

DOCK_CD1# 27,29,30,31

C631 1000pF 25V RK A/B

GND1

検出方法が他の装置と違うので、ポトリ側も確認下さい

PR_SUSC#

M58A NL17SZ08XV5 A/B

SUSC# 17,30,49,51,59,61

PLLB# 17

M58B NL17SZ08XV5 A/B

VCC

GND

PWR_3VSTD

C686 0.1uF 16V RK A/B

GND1

Low−Lowバッテリになったら、ポトリ側で作る電源を止めるための回路

TV_PR_LUNA 29

TV_PR_CHROMA 29

DG_SPDIFO 41

DG_SENSE_B 41

PWR_1

C558 0.1uF 25V 1608 RK A/B

C557 1uF 25V 1608 RK A/B

C556 1uF 25V 1608 RK A/B

GND1

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4

CUST.

FUJITSU LTD.

SHEET 40 / 66

電源経由のAudioノイズ対策でMAIN -> SUSに変更
(S3時はAMPをシャットダウンし、LDOを止めている)

PWR_5VSUS

CN15A

ALG MIC3
->内蔵マイク toLCDCN

ALG OUTA DOCK x
->ホトリ LineOut

ALG MIC2
->内蔵マイク toLCDCN

18 ACZ_RST#
18 ACZ_BITCLK
18 ACZ_SYNC
18 ACZ_SDOUT
24 ALG_MIC3
30 GSPKOUT
40 DG_SENSE_B
40 DG_SPDIFO
30 BLUE_DETACH#
17,20 BLUE_RI#
30,31 BLUE_EXIST#
23 IDE_SDD8
23 IDE_SDD9
23 IDE_SDD10
23 IDE_SDD11
23 IDE_SDD12

ACZ_SDIN1 18
ACZ_SDIN0 18
HPON 30
ALG_MIC2 24
ALG_OUTA_DOCK_R 40
ALG_OUTA_DOCK_L 40
ALG_SPKOUTR- 33
ALG_SPKOUTR+ 33
ALG_SPKOUTL+ 33
ALG_SPKOUTL- 33
BAY1_ON 23,27,30,59
USB_P7+ 17
USB_P7- 17
63 PMU_SCONT2
IDE_PRST# 23
IDE_SDD7 23
IDE_SDD6 23
IDE_SDD5 23
IDE_SDD4 23

PWR_3VMAIN

BayAudio
CA52233-0087

GND1
GND_AUD

PWR_PMU
D69
1SS400G
R577
100K 1/16W 5%
PMU_SCONT2#
Q107
2SK3541

CN15B

23 IDE_SDD13
23 IDE_SDD14
23 IDE_SDD15
23 IDE_SDDREQ
23 IDE_SDIOR_BAY#
23 IDE_SDDACK#
23 IDE_SDA2
23 IDE_SDCS#1
30,31 BAY1_ID2
30,31 BAY1_ID1
30,31 BAY1_ID0
17 USB_P3-
17 USB_P3+
57 PMU_BT2CLK0
57 PMU_BT2IN#0

IDE_SDD3 23
IDE_SDD2 23
IDE_SDD1 23
IDE_SDD0 23
IDE_SDIOW_BAY# 23
IDE_SDIORDY_BAY 23
IRQ15_BAY 23
IDE_SDA1 23
IDE_SDA0 23
IDE_SDCS#0 23
BAY1_LMP# 27
BAY1_CD2# 30,31
BAY1_CD1# 30,31
PMU_BT2DAT0 57
PMU_VSENSE2 58,62,63
PMU_BT2TEMP0 57

PWR_BT2ROM

BayAudio
CA52233-0087

PWR_CHARGE2
2ndBatt
MAX 6A

C639
0.01uF 25V RK
None

C690 0.1uF 16V RK
C691 0.1uF 16V RK
C692 0.1uF 16V RK

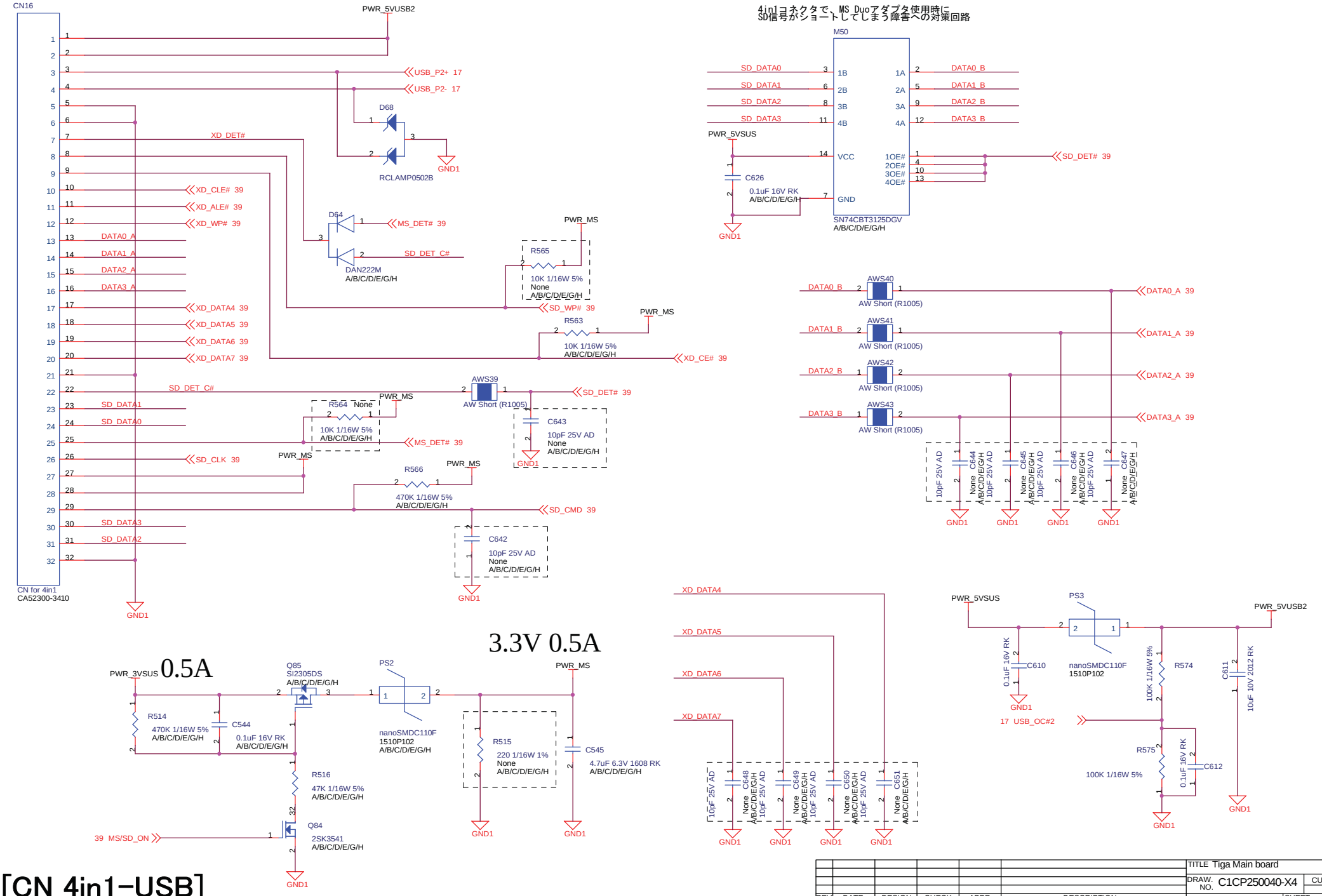
R278
10 1/16W 5%
C387
1000pF 25V RK

[Refference:Pumpkin]

[CN for BAY/AUDIO]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 41 / 66

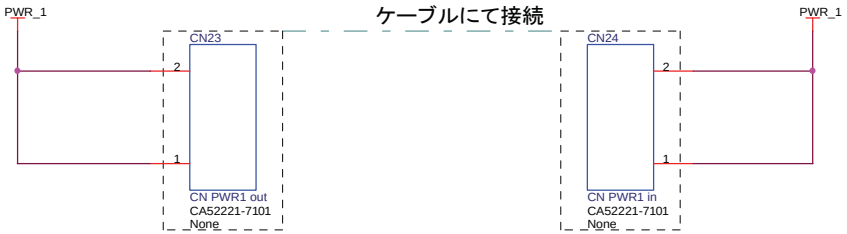


[CN 4in1-USB]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 42 / 66

※CN23はD51,D52近傍に配置すること



内層パターン補強用で用意（製品未使用）

[CN PWR1]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 43／66

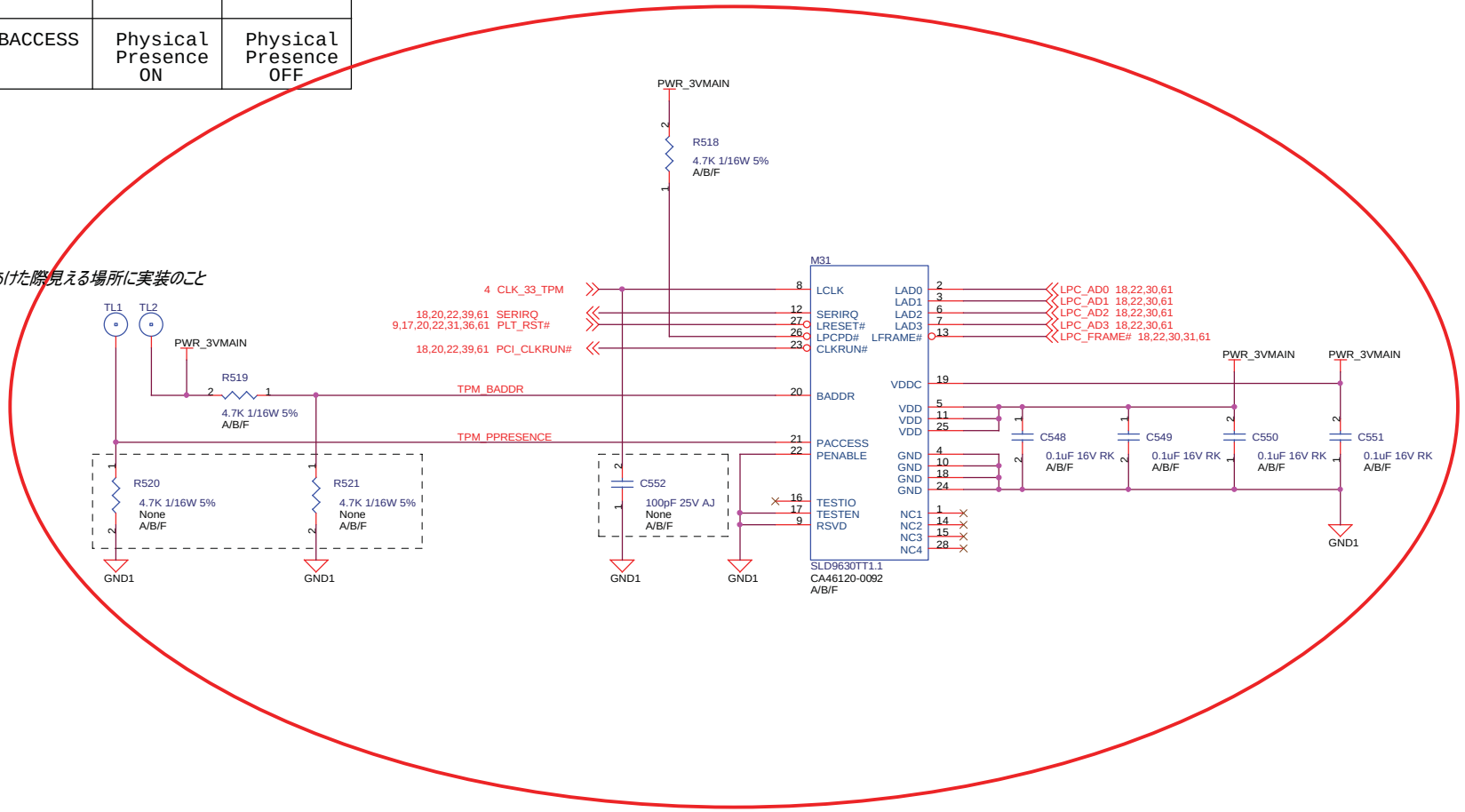
TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh
TPM_BACCESS	Physical Presence ON	Physical Presence OFF

#05(F0205A19559)
Mount all parts of this page for VB238AF.

位置指定

クリアパッドは
メモリモジュールの蓋をあけた際見える場所に実装のこと

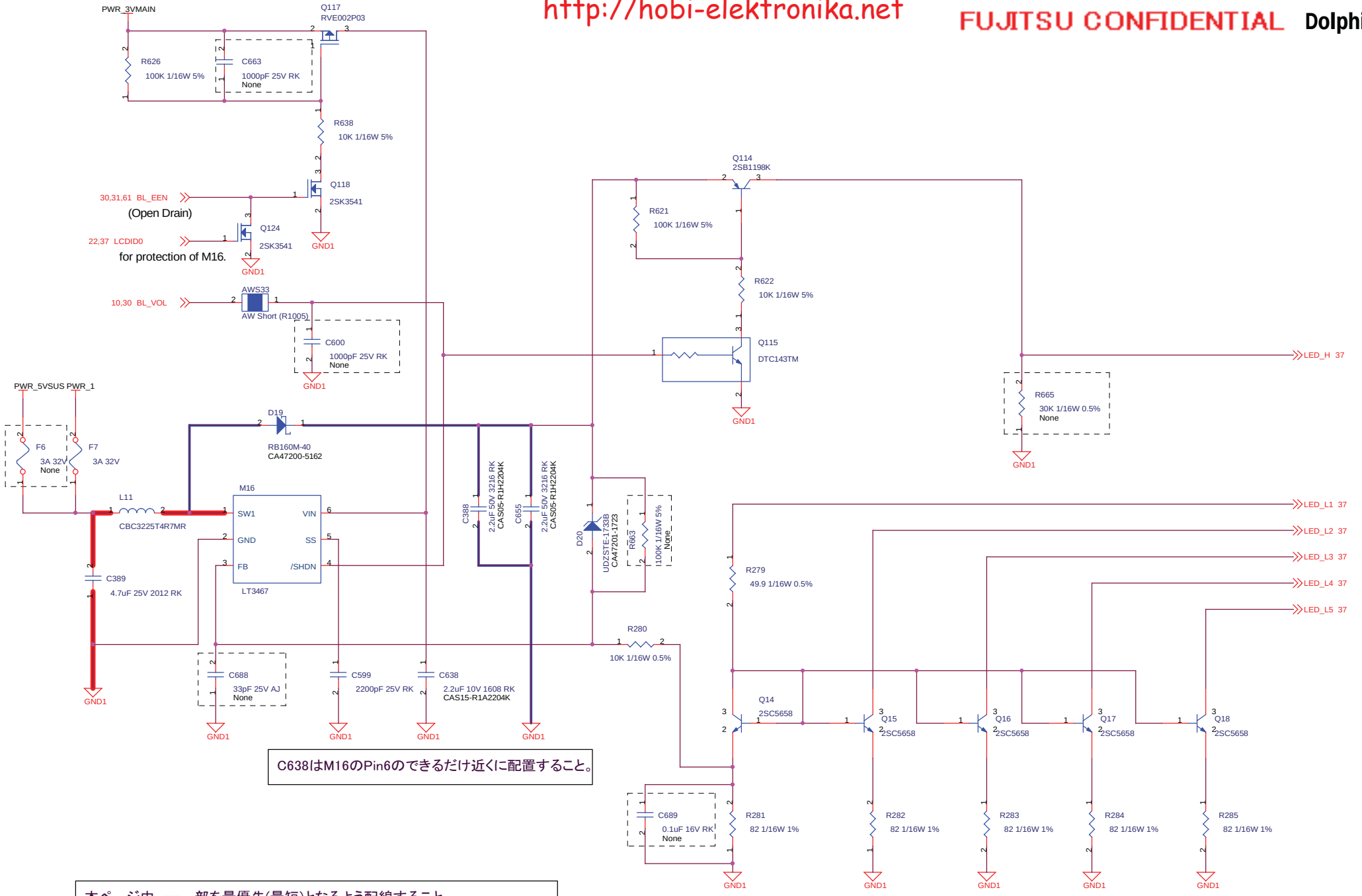


[Refference:Emilia3]

[TPM]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 44 / 66



C638はM16のPin6のできるだけ近くに配置すること。

本ページ中 ━ 部を最優先(最短)となるよう配線すること。
本ページ中 ━ 部を第2優先とし可能限り最短となるよう配線すること。

常に最新の状況を確認下さい

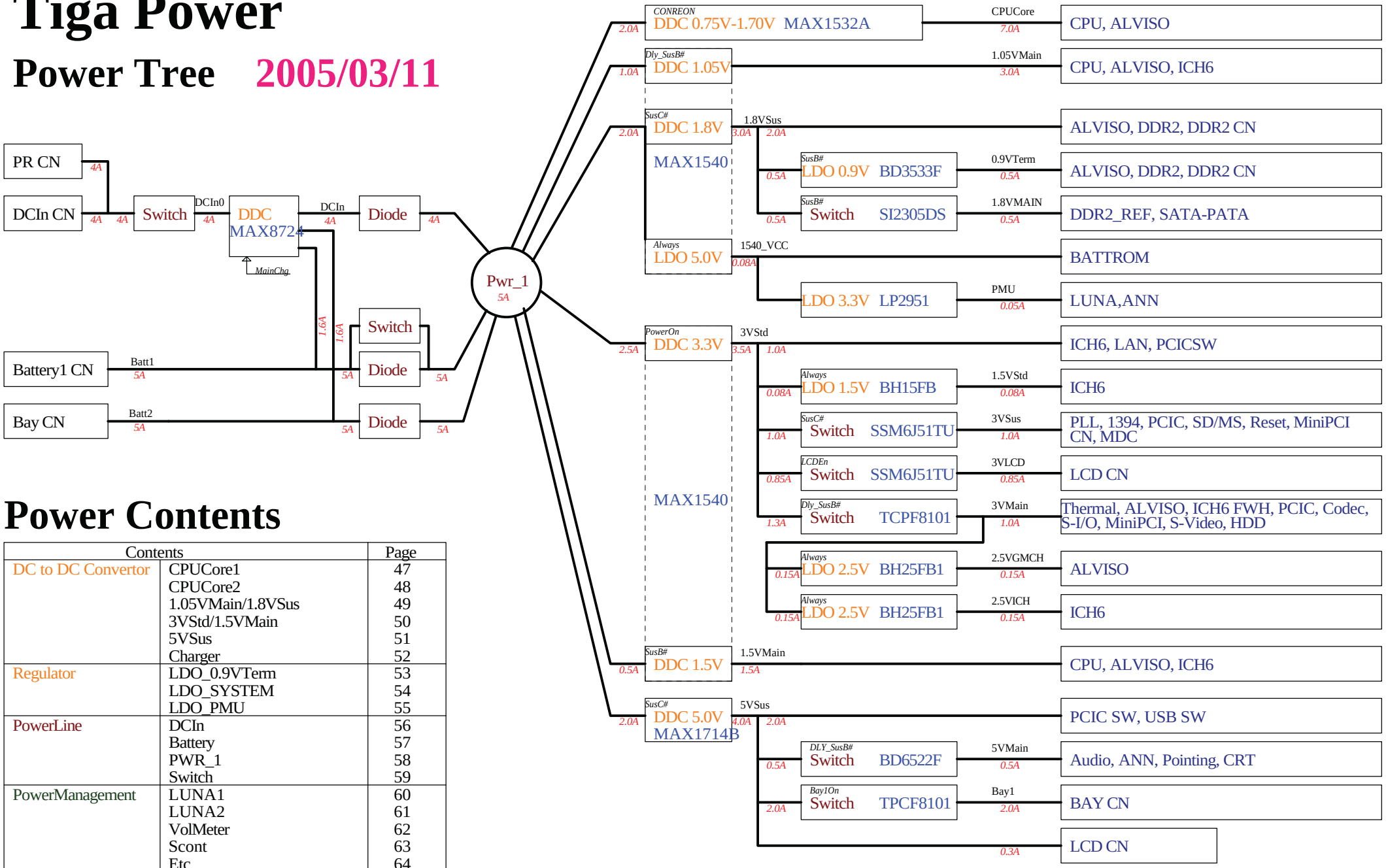
[Power/LED Drive (LCD)]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 45 / 66

Tiga Power

Power Tree 2005/03/11

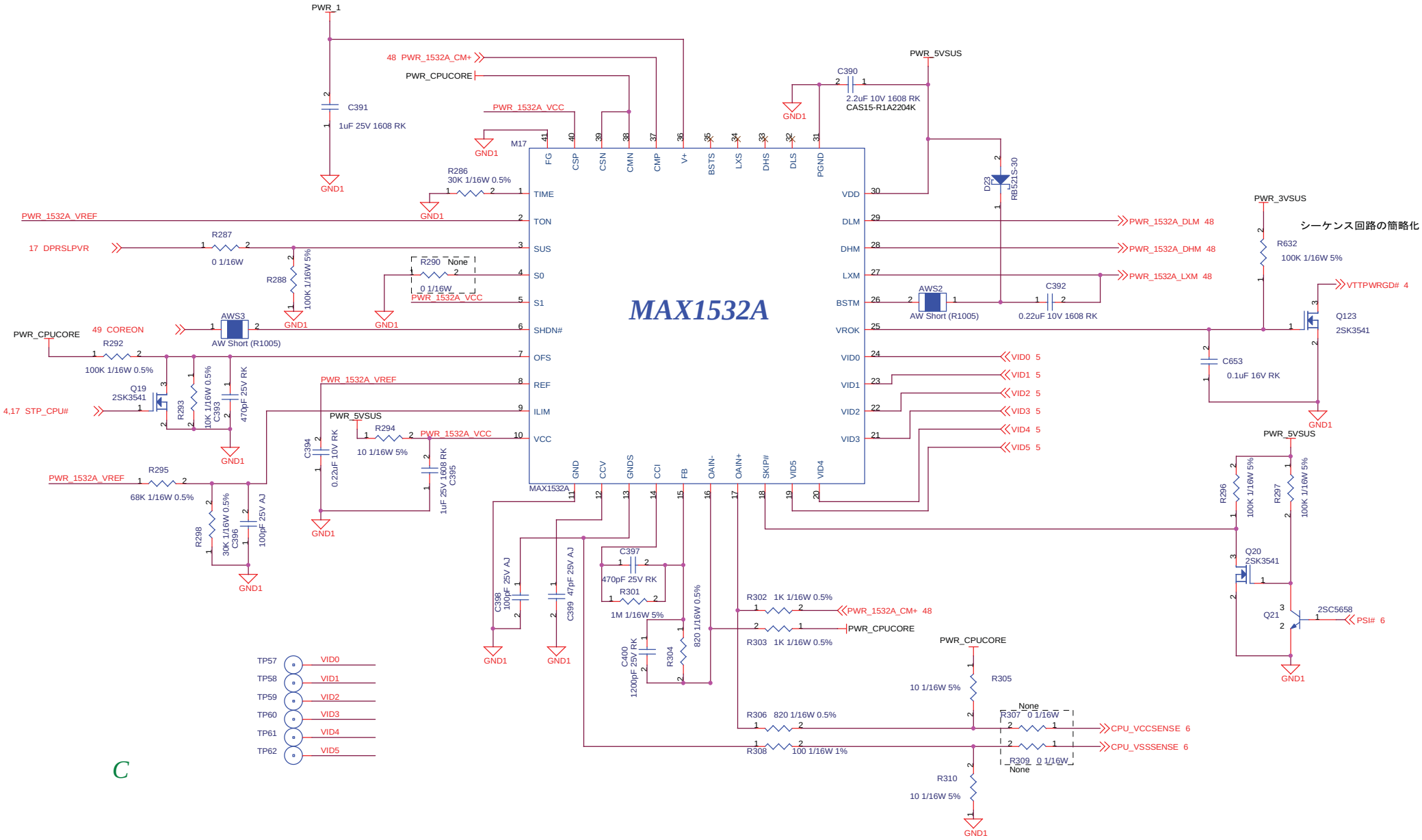


Power Contents

Power/ TopPage

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 46 / 66

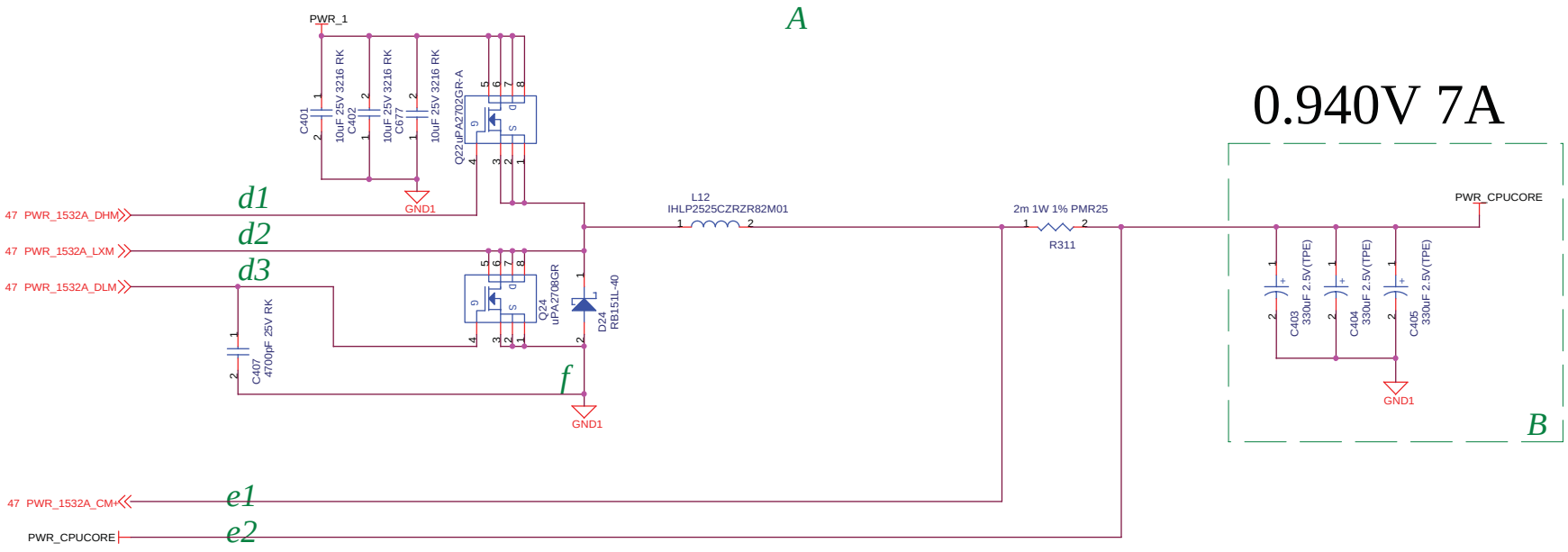


C

Power/ DDC/ CPUCore 1

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
DATE		DESIGN		CHECK		APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 47 / 66



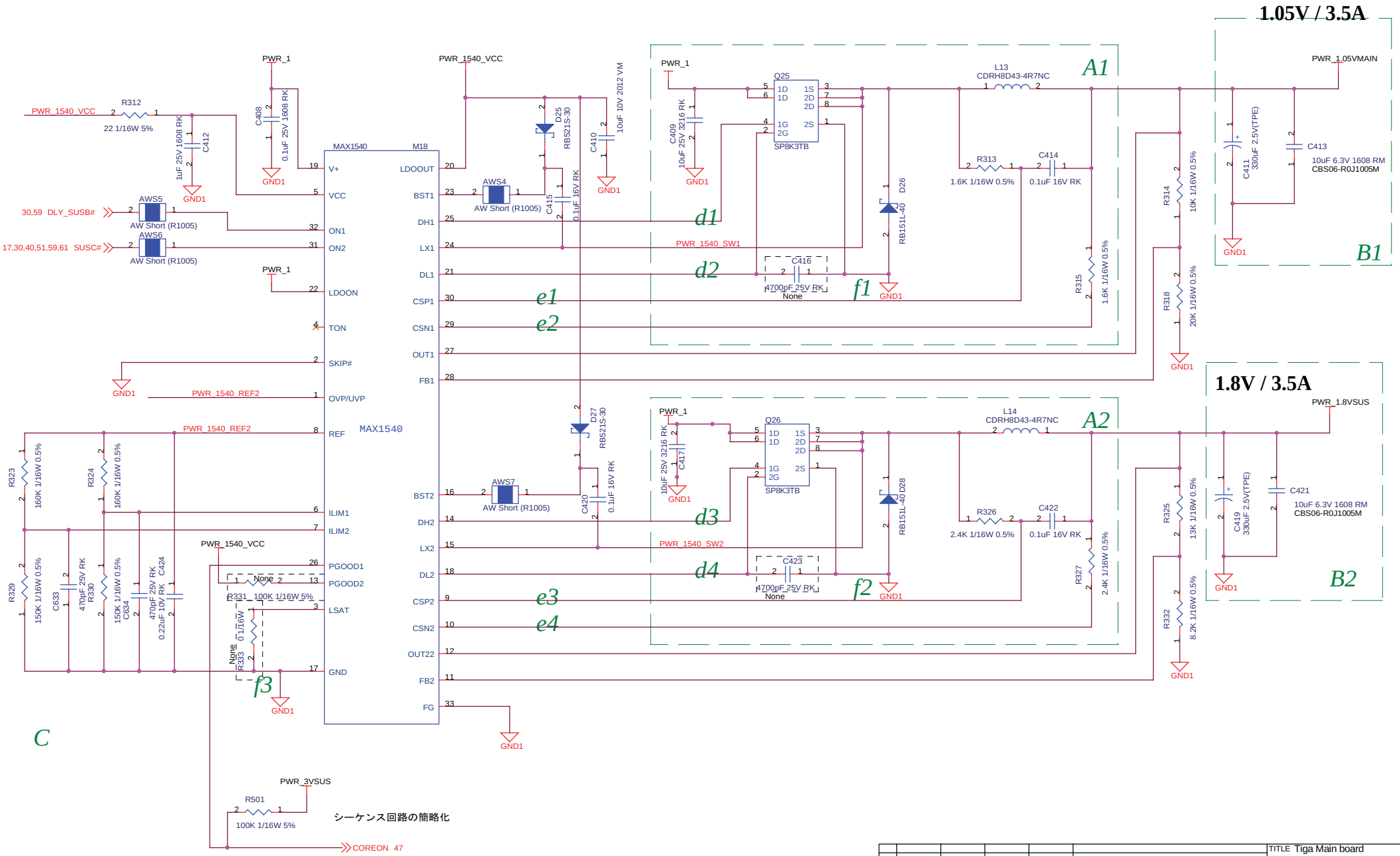
Power/ DDC/ CPUCore2

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 48 / 66

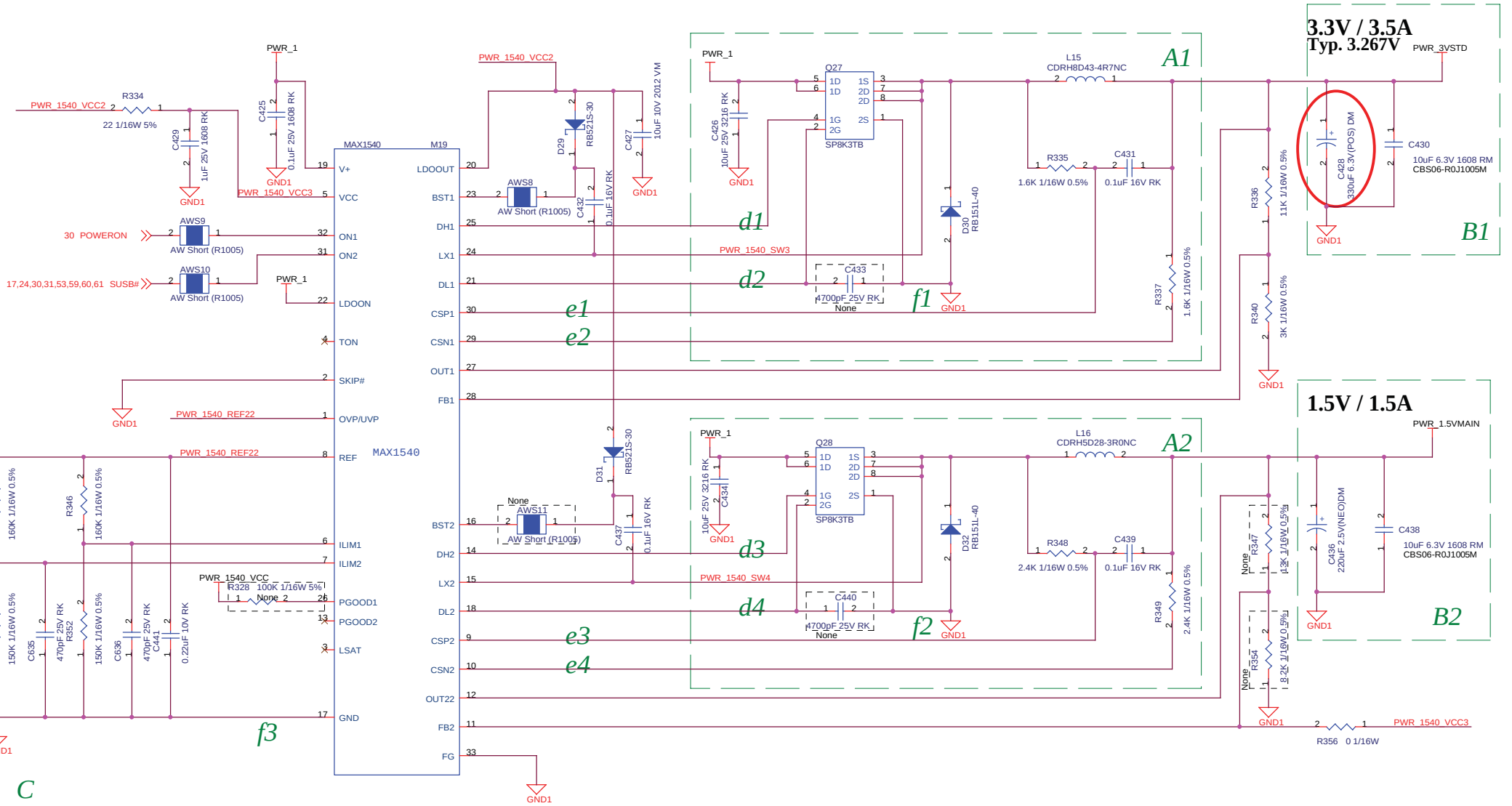


Power/ DDC/ 1.05VMAIN, 1.8VSus

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE		DESIGN		CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 49 / 66

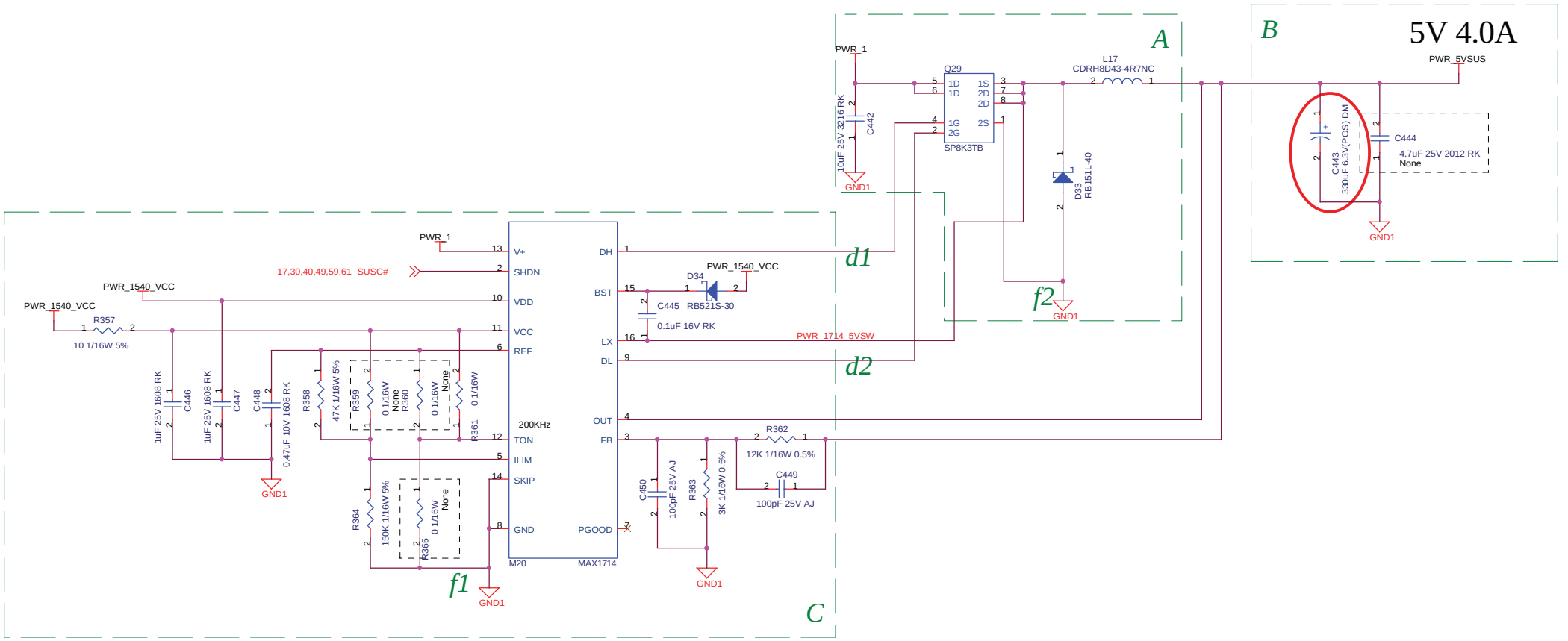
#04(F0205A18869)
C428 : CAJ02-P0J3300M -> CAT35-P0J3300M(for RoHS).



Power/ DDC/ 3VSTD/ 1.5VMAIN

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	TITLE	Tiga Main board
	DATE	DESIGN	CHECK	APPR.		DRAW. NO.	C1CP250040-X4
						CUST.	
						FUJITSU LTD.	SHEET 50 / 66

#04(F0205A18869)
C443 : CAJ02-P0J3300M -> CAT35-P0J3300M(for RoHS).



Power/ DDC/ 5VSUS

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE		DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 51 / 66

Power/ DDC/ Charger

6.0V-8.4V/2.5A

8.4V-12.6V/1.6A

PWR_INTDCIN
R366 10m 1W 1% KOA-SL1
PWR_DCIN

M21
MAX8724

CSSN
CSSP
DCIN
ACIN
REFIN
ICTL
VCTL
ICHG
IINP
SHDN
CCV
CCI
CCS
REF
CLS
ACOK
GND
DHI
CELLS
LDO
BST
DLOV
LX
DLO
PGND
CSIP
CSIN
BATT
FG

VCTL=1.354V
VCLS=1.9275V
linputMax=3.529A
REFIN=2.731V

PWR_PMU
PWR_DCIN
PWR8724_REFIN
PWR8724_REF4
8724_MASK
PMU_MAINCHG 60
PMU_VB1 60
PMU_SERIAL2/3# 60
PMU_CHGFB
PMU_CHGMASK 60
PMU_SCONT1 57,63
PWR_CHARGE1
PWR_CHARGE2

D37 RB521S-30
D38 RB521S-30
D36 RB053L-30FA
D39 RB053L-30FA
Q31 2SK3541
Q32 Q30 uPA2702GR-A
Q33 Q35 RVE002P03
Q34 2SK3541
M22 NJU7141F(TE1)r

L18 CDRH8D43HP-100NC

R367 27m 1W 1% KOA-TSL1
R368 0 1/16W None
R369 33 1/16W 5%
R370 75K 1/16W 0.5%
R371 56K 1/16W 0.5%
R372 20K 1/16W 0.5%
R373 12K 1/16W 0.5%
R374 39K 1/16W 0.5%
R375 20K 1/16W 0.5%
R376 20K 1/16W 0.5%
R377 4.7K 1/16W 0.5%
R378 180K 1/16W 0.5%
R379 160K 1/16W 0.5%
R380 39K 1/16W 0.5%
R381 100 1/16W 1%
R382 100K 1/16W 0.5%
R383 0 1/16W
R384 10K 1/16W 5%
R385 100K 1/16W 5%
R386 1M 1/16W 0.5%
R387 100 1/16W 1%
R388 13K 1/16W 0.5%
R389 100K 1/16W 5% None
R390 20K 1/16W 0.5%
R578 10K 1/16W 5%
R658 470K 1/16W 5%

C451 10uF 25V 3216 RK
C452 1uF 25V 1608 RK
C453 10uF 25V 3216 RK
C454 10uF 25V 3216 RK
C455 10uF 25V 3216 RK
C456 10uF 25V 3216 RK
C457 1uF 25V 1608 RK
C458 0.1uF 25V 1608 RK
C459 1uF 25V 1608 RK
C460 0.022uF 25V 1608 RK
C461 0.01uF 25V RK
C462 1000pF 25V RK
C463 1uF 25V 1608 RK
C464 0.1uF 16V RK
C465 1000pF 25V RK
C466 0.01uF 25V RK

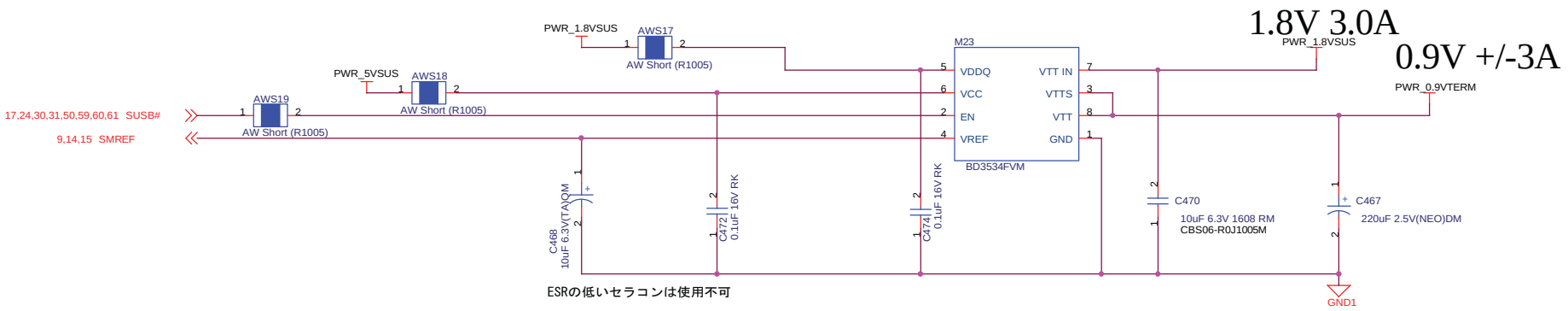
AWS12 AW Short (R1005)
AWS13 AW Short (R1005)
AWS14 AW Short (R1005)
AWS15 AW Short (R1005)

e1 e2 d1 e3 e4 e1 d2 f2 f1 C

GND1

TITLE	Tiga Main board	
DRAW. NO.	C1CP250040-X4	CUST.
FUJITSU LTD.		SHEET 52 / 66

REV. DATE DESIGN CHECK APPR. DESCRIPTION



Power/ DDC/ 1.25VSus

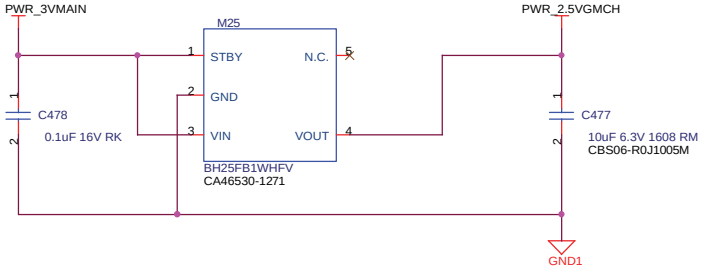
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

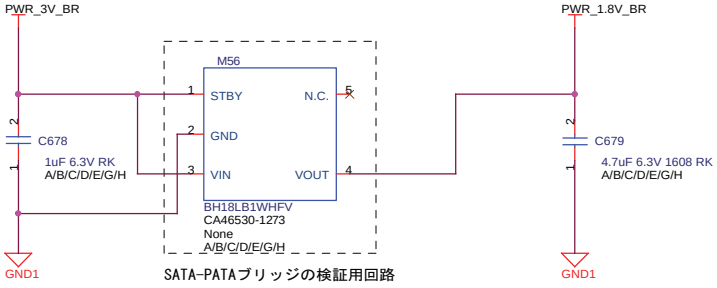
DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 53 / 66

2.5V 0.15A



1.8V 0.1A



SATA-PATAブリッジの検証用回路

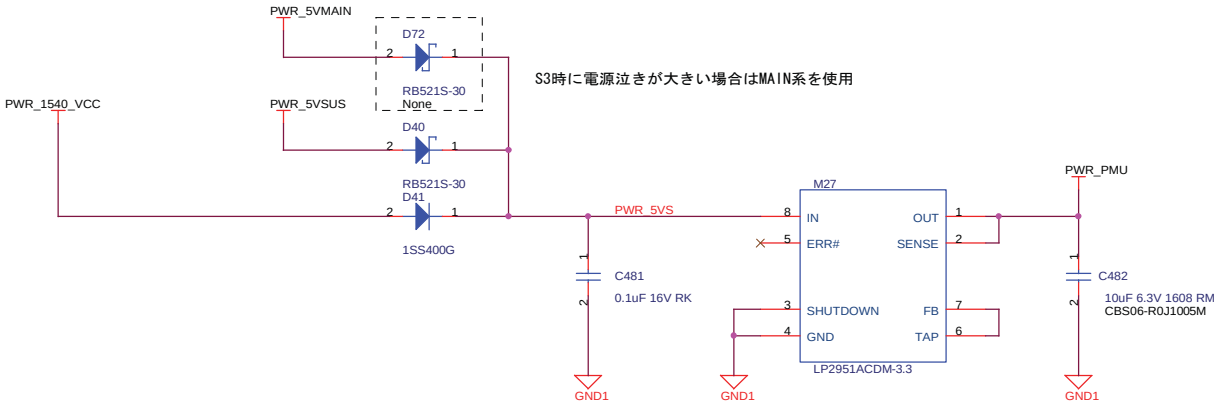
Power/ LDO/ System

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 54 / 66



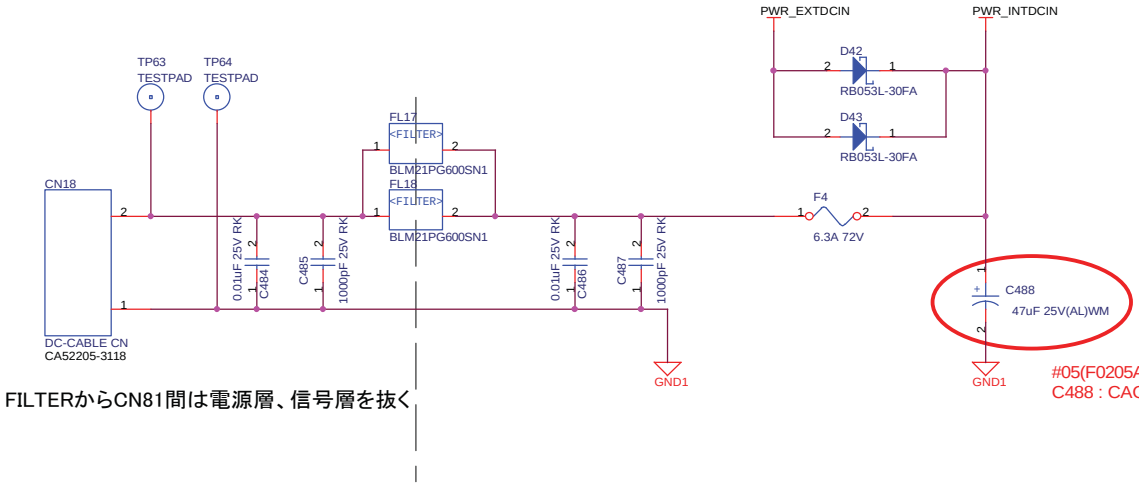
Power/ LDO/ PMU

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 55 / 66



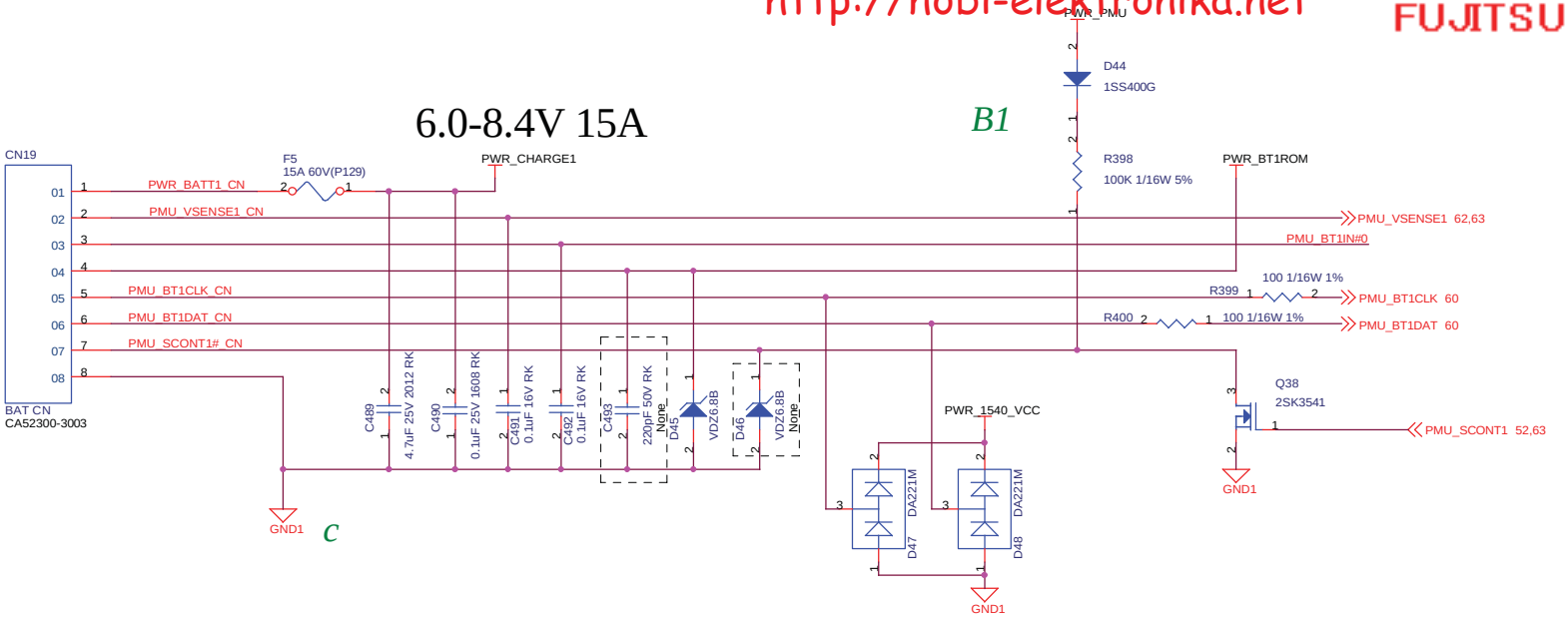
FILTERからCN81間は電源層、信号層を抜く

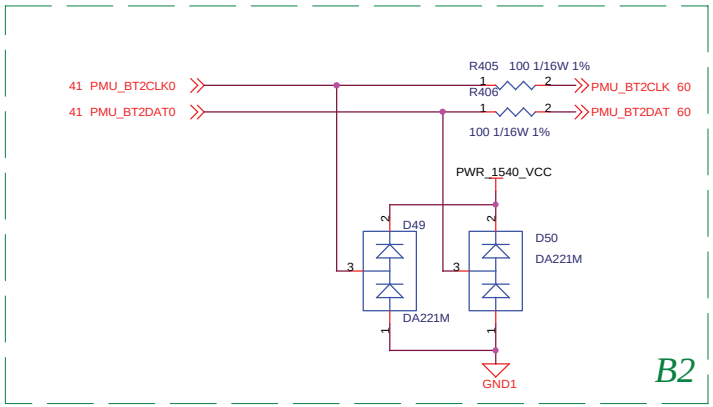
#05(F0205A18869)
C488 : CAG86-W1E47R0M -> CAT63-W1E47R0M(for RoHS).

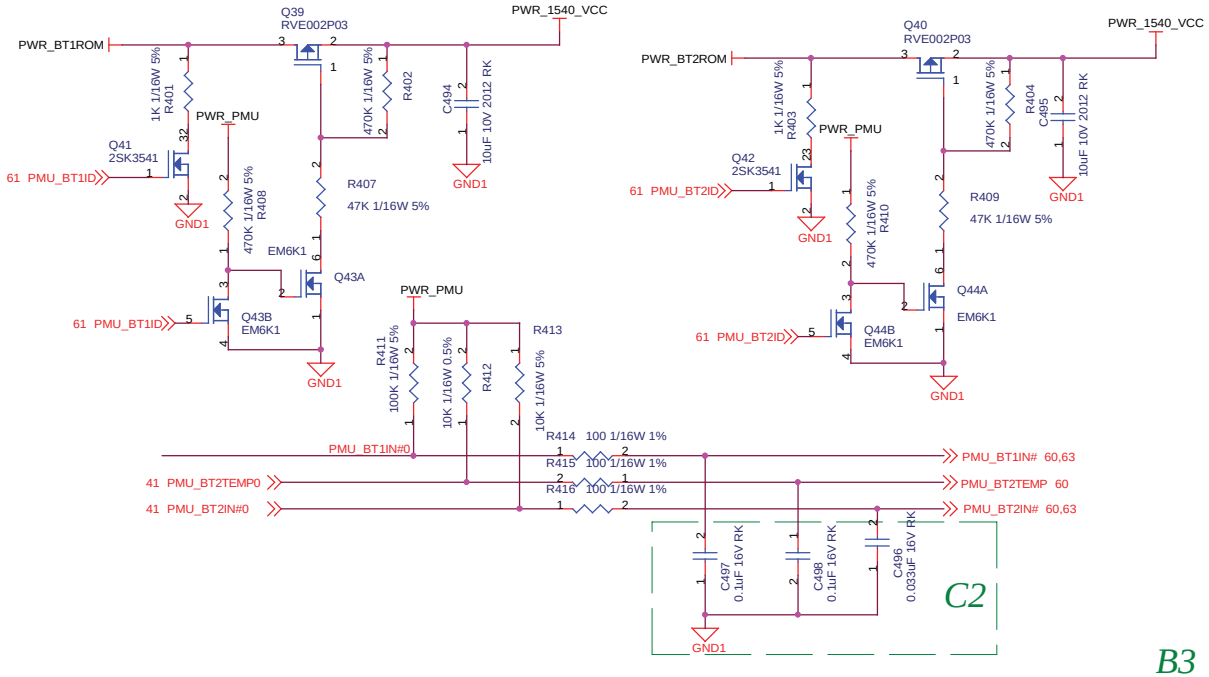
Power/ Node/ DCIn

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 56 / 66



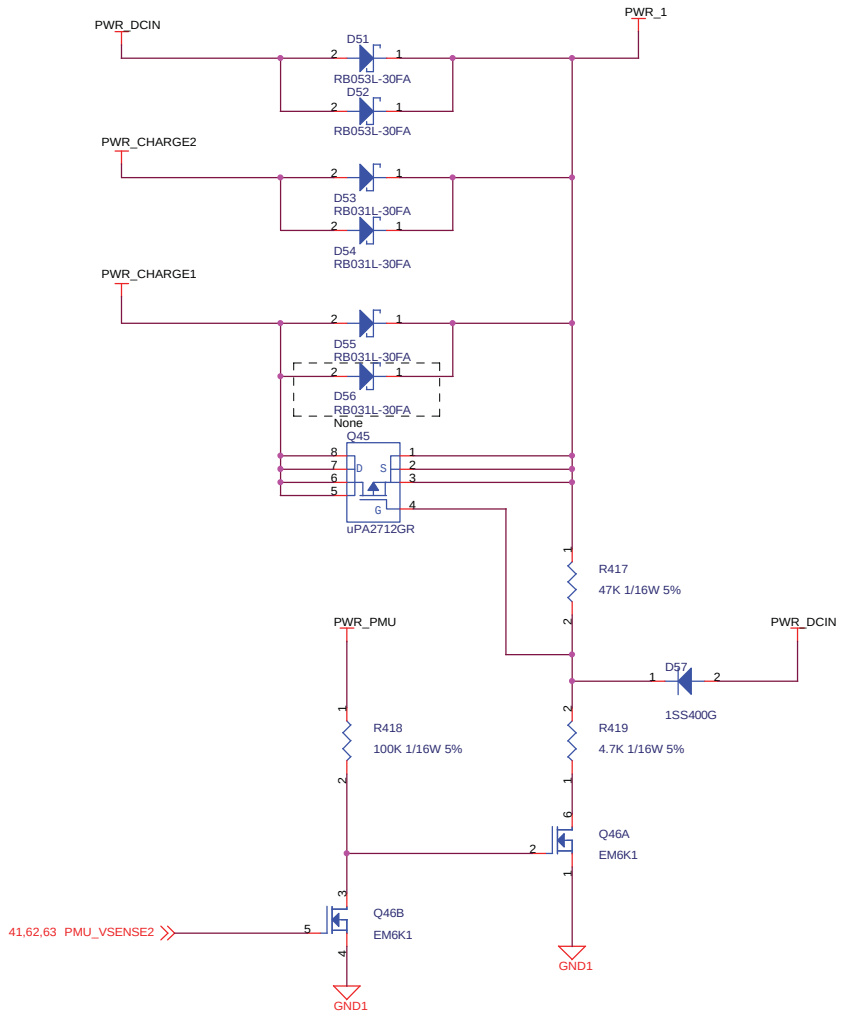




Power/ Node/ Battery

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 57 / 66



Power/ Node/ PWR_1

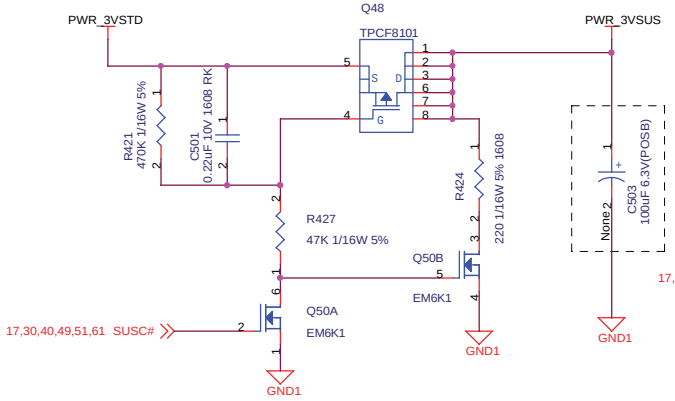
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE		DESIGN	CHECK	APPR.	

TITLE Tiga Main board

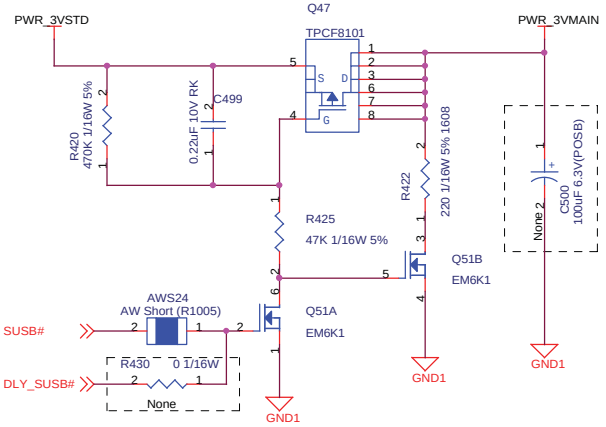
DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 58 / 66

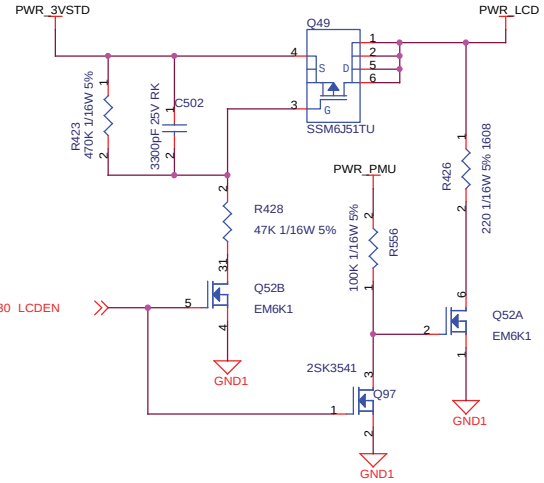
3.3V 2.0A



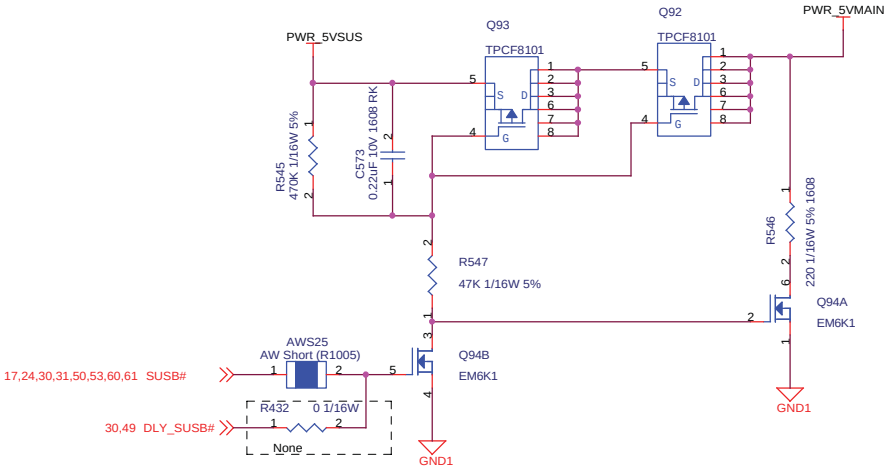
3.3V 2.0A



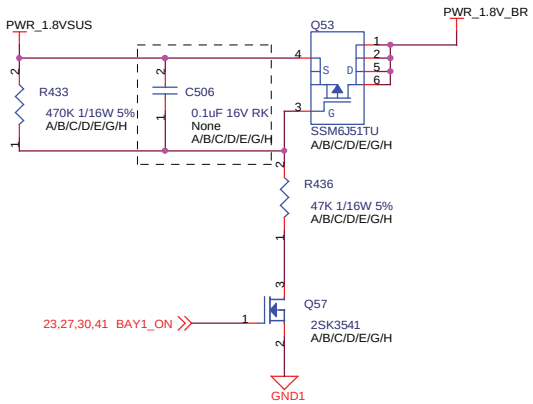
3.3V 1.0A



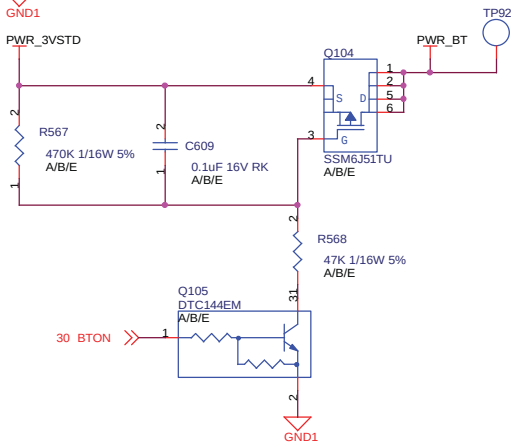
5.0V 0.5A



1.8V 0.1A



3.3V 1A

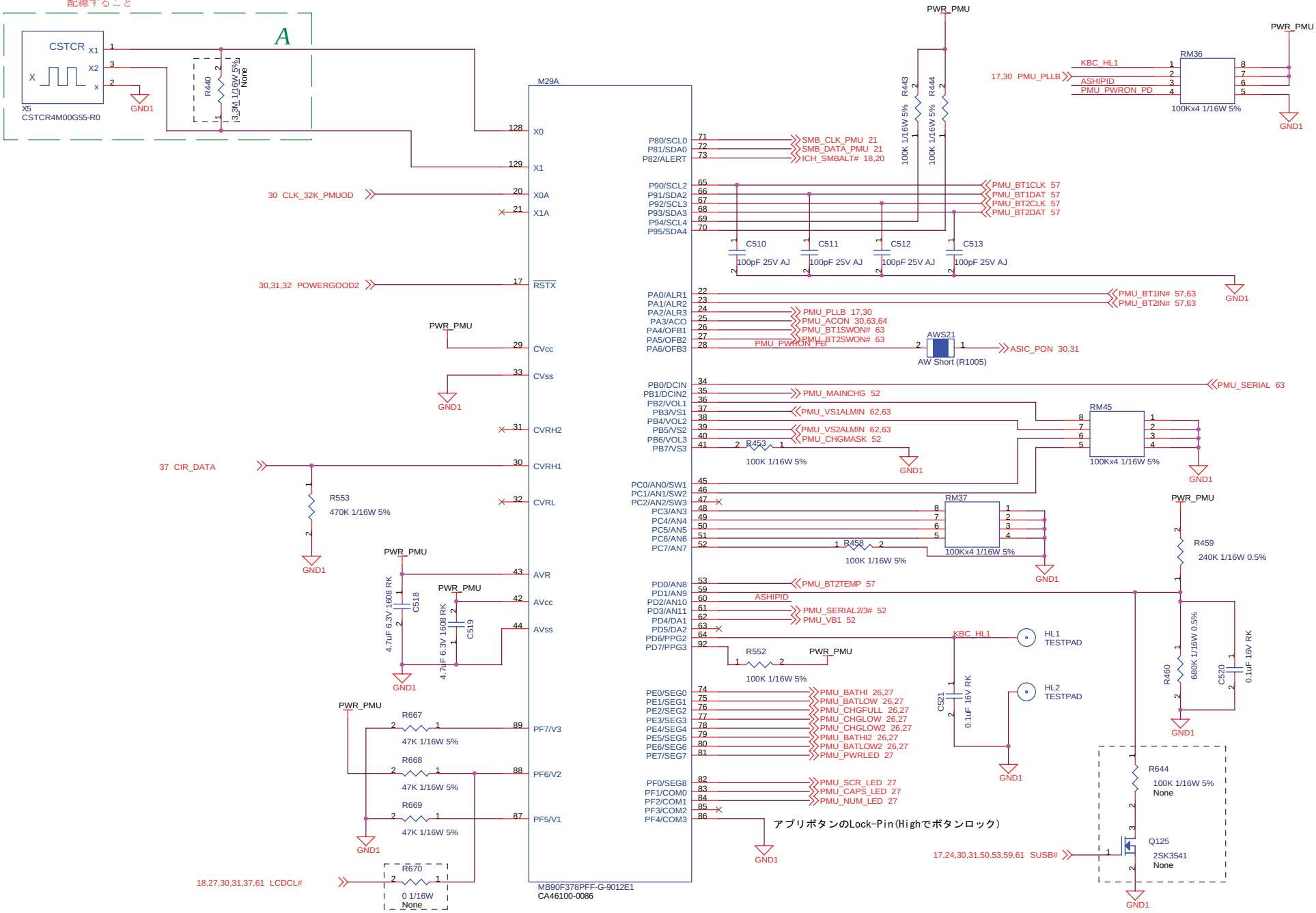


Power/ Node/ Swicth

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 59 / 66

本クロックはノイズに弱いため
上下層に高速な信号が走らないように
配線すること



Power/ PMU/ LUNA1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board
DRAW. NO. C1CP250040-X4
CUST.
FUJITSU LTD.
SHEET 60 / 66

Power/ PMU/ LUNA2

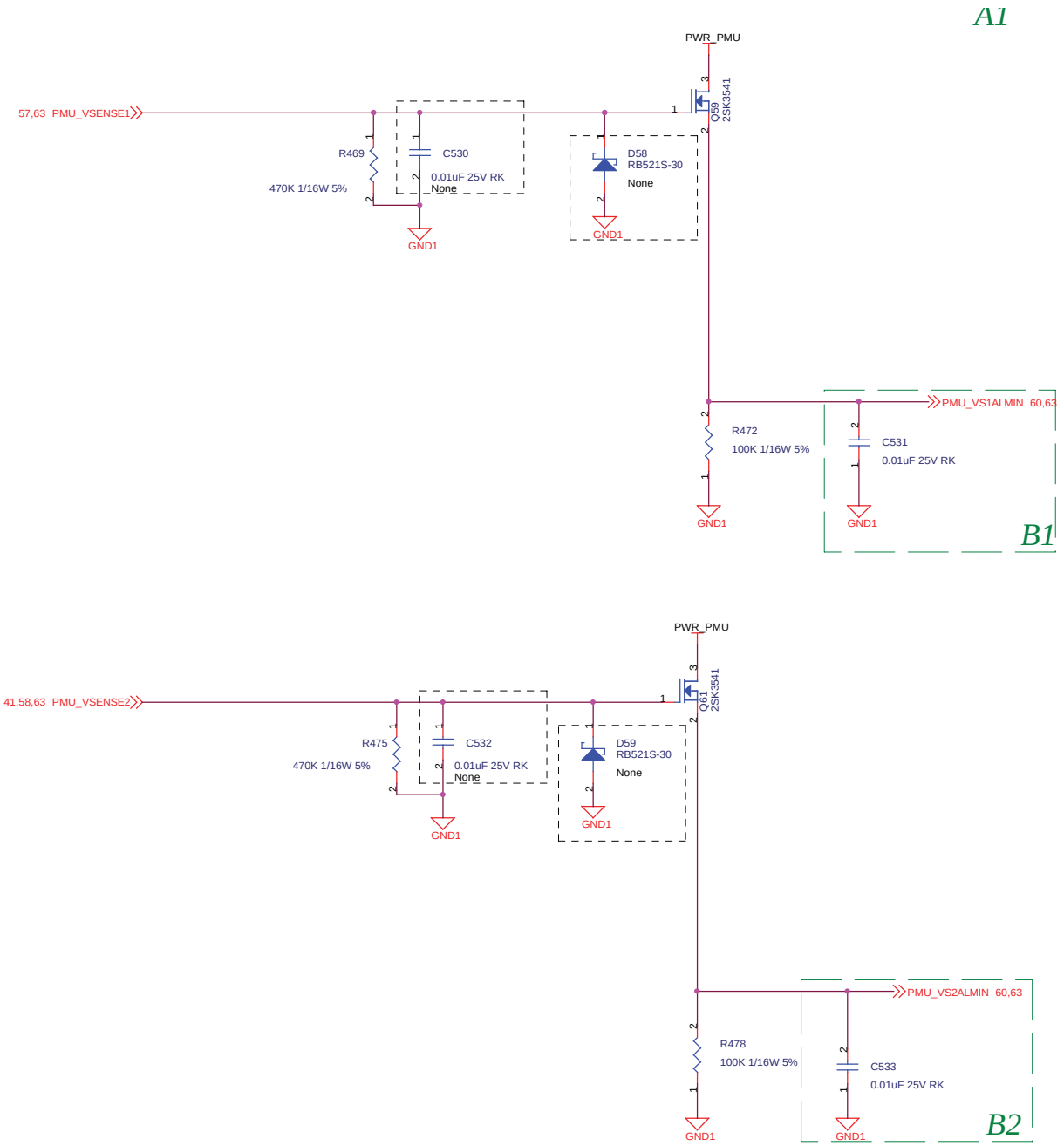
カバークローズ時インスタント抑止
検討用に入れた回路（未使用）

本ページの抵抗・コンデンサはM90F378付近に配置すること。
パスコンについてはM90F378の電源ピンに対して均等になるように配置分散し、
電源ピンまでのリード長を最大限短くなるようレイアウトすること。

MB90F378PFF-G-9012E1
CA46100-0086

TITLE	Tiga Main board	
DRAW. NO.	C1CP250040-X4	CUST.
FUJITSU LTD.	SHEET 61 / 66	

REV | DATE | DESIGN | CHECK | APPR. | DESCRIPTION



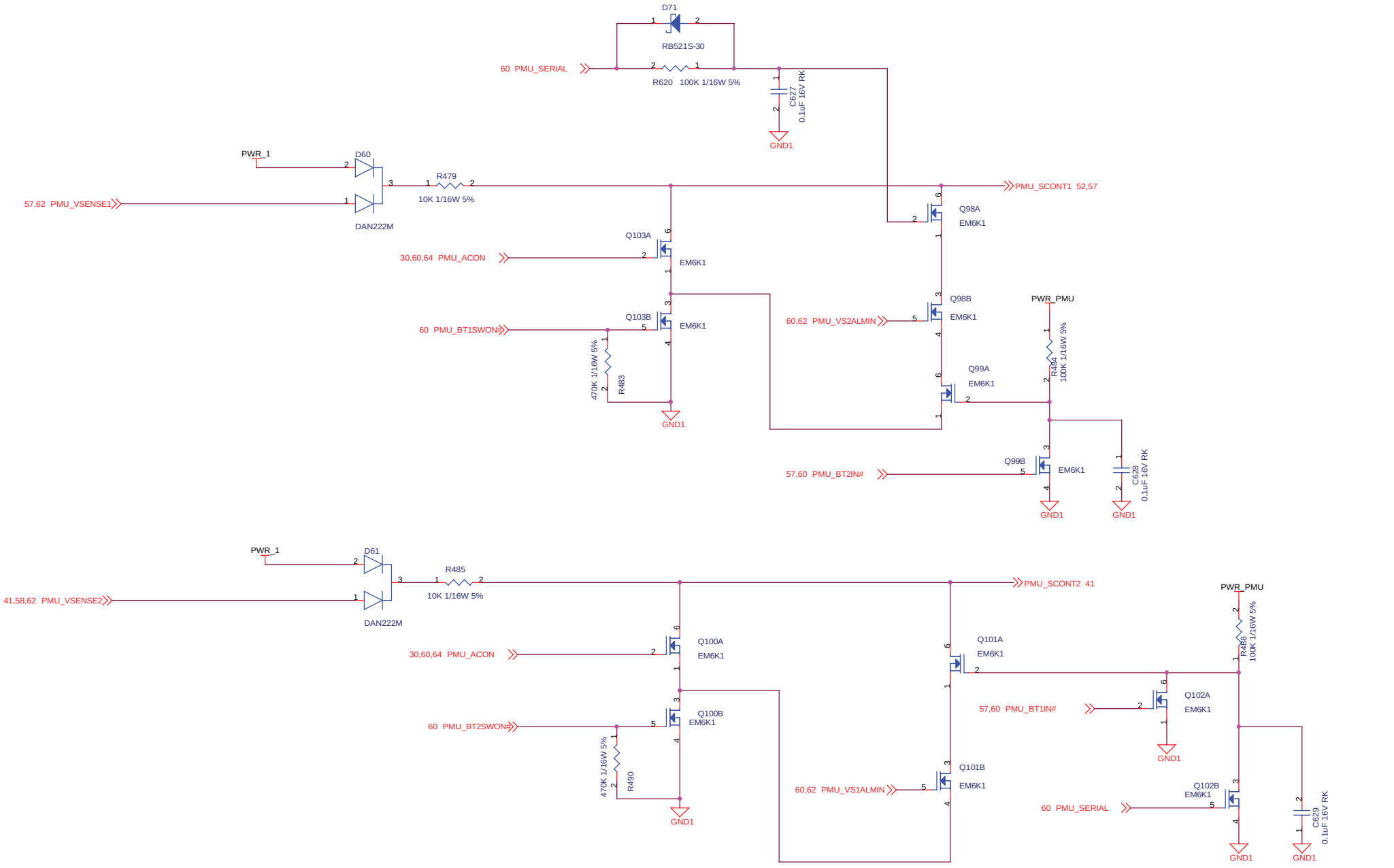
Power/ PMU/ VolMeter

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE		DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 62 / 66



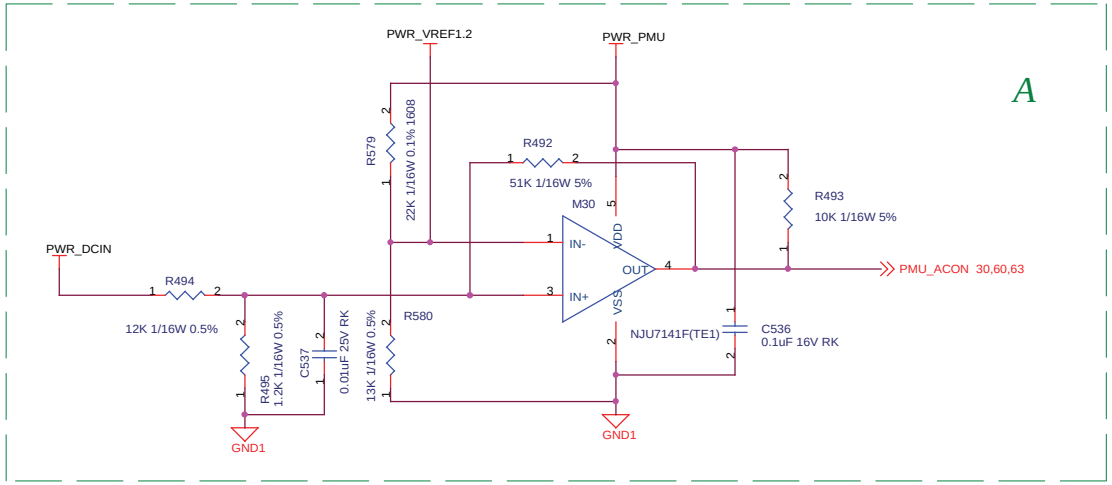
Power/ PMU/ Scont

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE		DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 63 / 66



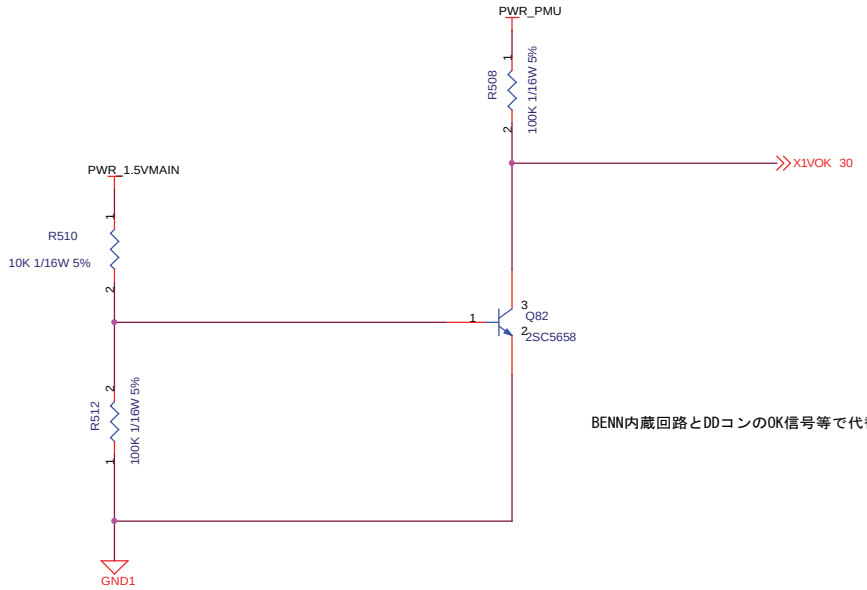
Power/ PMU/ Etc1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 64 / 66



BENN内蔵回路とDDコンのOK信号等で代替によりシンプル化

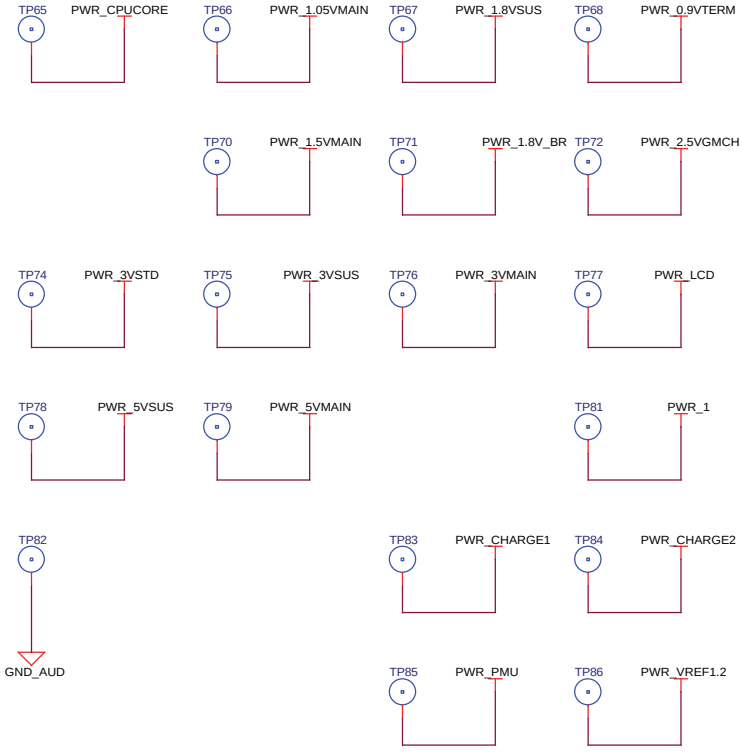
POWER_SEQUENCE

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 65 / 66



[TestPad]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	DESIGN	CHECK	APPR.	

TITLE Tiga Main board

DRAW. NO. C1CP250040-X4 CUST.

FUJITSU LTD. SHEET 66 / 66