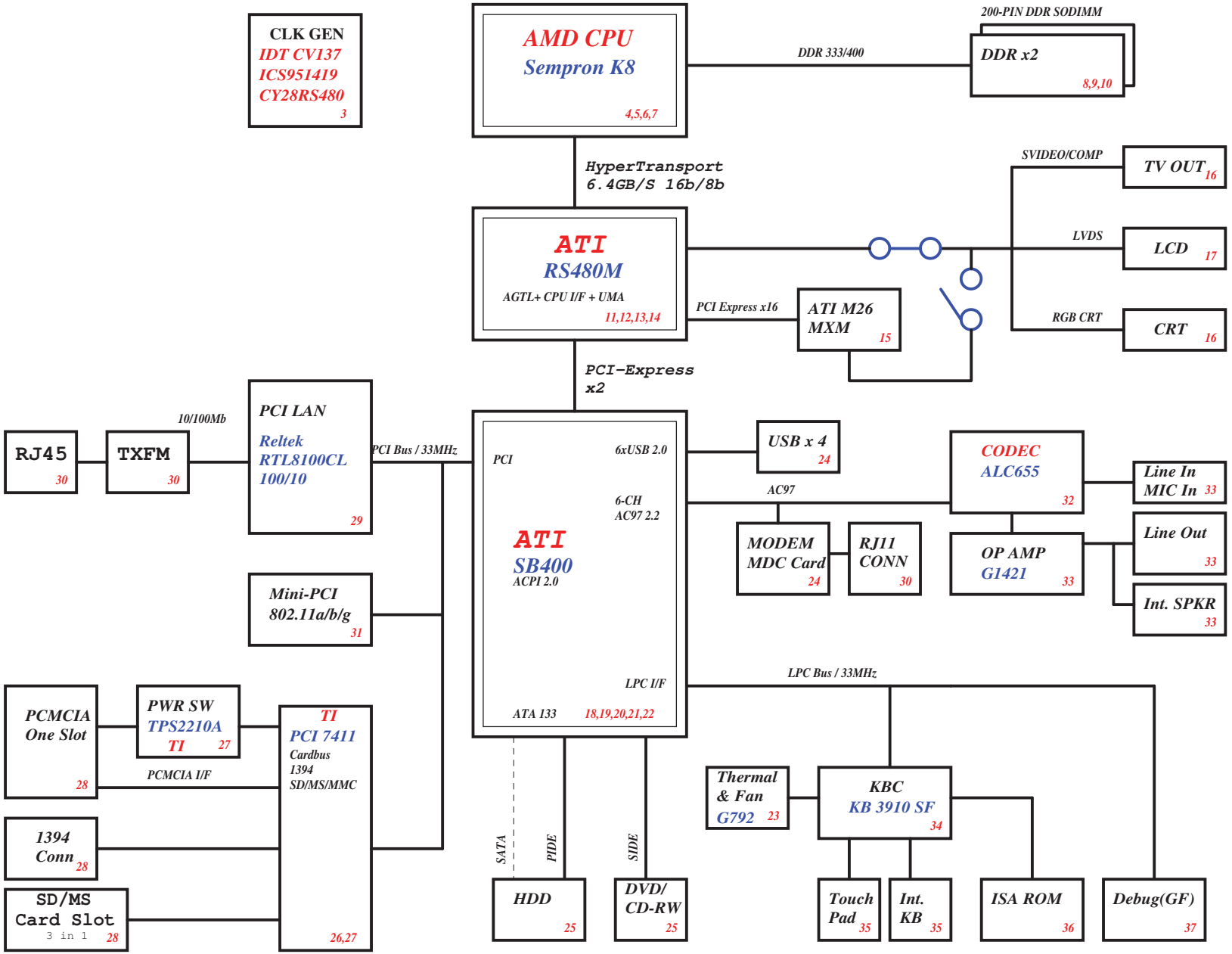
W37 Block Diagram

04241-SA



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Inner Signal 2
L4: Inner Signal 3
L5: VCC
L6: Signal 4

Battery Charger 48
MAX1909ETI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 44
ISL6227

INPUT	OUTPUT
DCBATOUT	2D5V_S3 , 1D8V_S5

SYSTEM DC/DC
TPS 5130 45,46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5 1D2V_S0

CPU V_CORE 42,43
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 47
LP2951ACM/APL5331KAC-TR

INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BLOCK DIAGRAM	
Size A3	Document Number W37	Rev SB
Date: Monday, March 14, 2005	Sheet 1 of 51	

-1 ver will change

CPU(62.10055.091) U70
NB(71.RS48M.B0U) U16
SB(71.SB400.D0U) U34
CLK GEN(71.00137.B0W) U15
DDR cnt.(62.10017.311) DIM2
KBC (71.03910.B0G)U35
Remove SKT1(21.H0080.001)
Hole3(34.46i15.001)
Hole4(34.46i12.001)
Hole8(34.46i14.001)
Hole25(34.4B301.001)
Hole26(34.46i14.001)
GND20(34.4B312.001)

?

1/27
Revise:
 support @D5V_S0 for AVDD (Page 13)□--CRT ripple

  ADD GND8~GND20□--EMI
  change power of MDC form 3D3V_S0 to 3D3V_S5 □--spec issue
 improve power on sequence (1.8/S5 to 3.3/S5)
          C158-->0.01u;C156-->1u
 Add 1u at 3D3V_S0/inverter (C809)

<Variant Name>

緯創資通 Wistron Corporation
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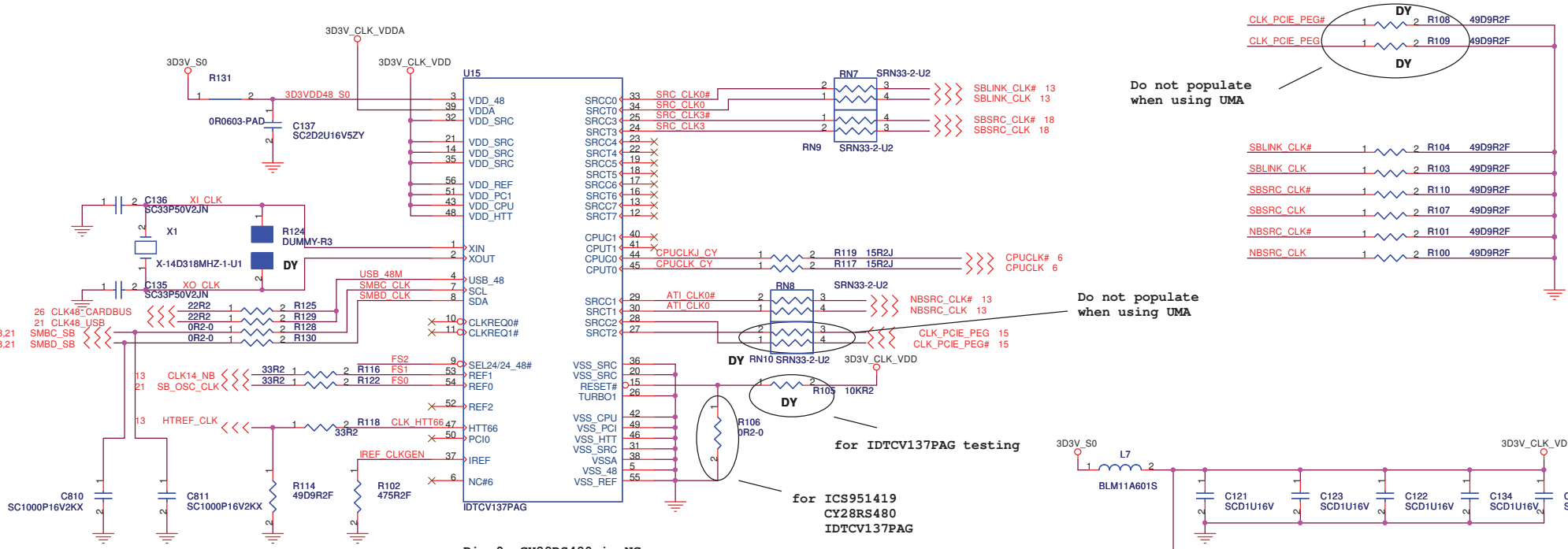
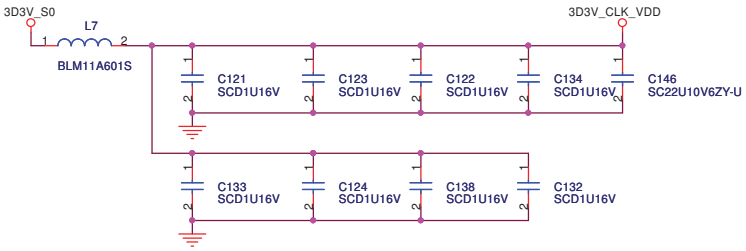
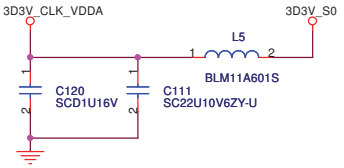
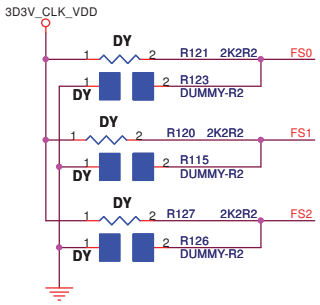
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHANGE HISTORY	
Size A3	Document Number W37	Rev SB
Date: Friday, March 25, 2005	Sheet 2 of 51	





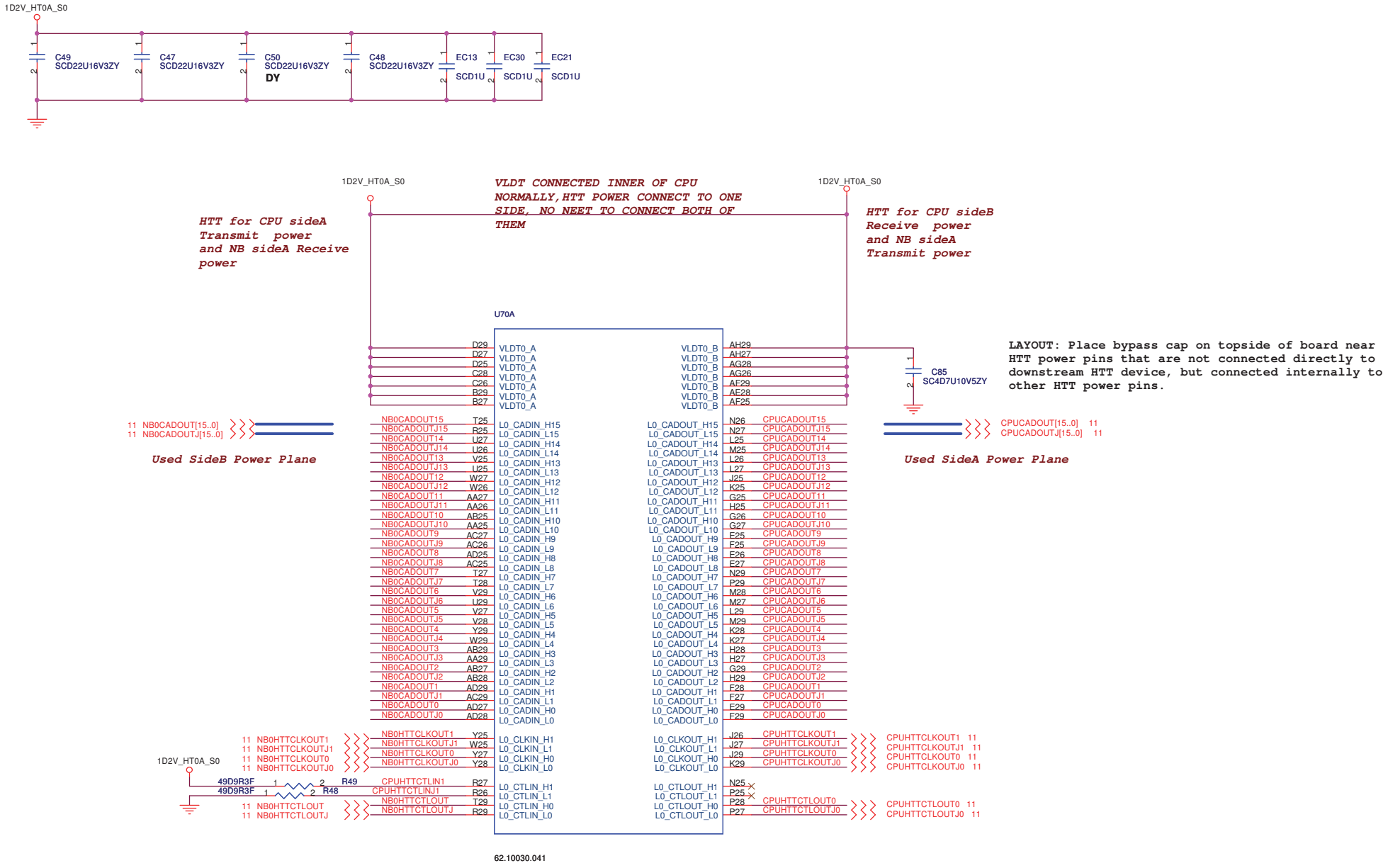




for ICS951419

FS2	FS1	FS0	CPU	HTT	PCI
			MHz	MHz	MHz
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	36.56	73.12
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CLKGEN_ICS951412
Size: A3 | Document Number: W37 | Rev: SB
Date: Friday, April 15, 2005 | Sheet 3 of 51



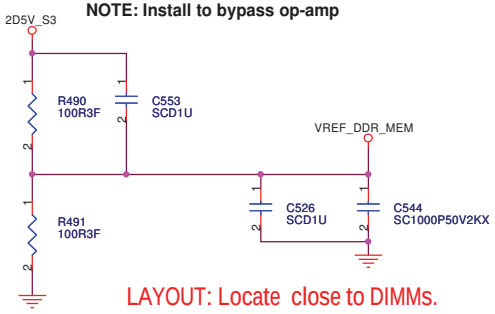
By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.221
Third 62.10053.201

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU(1/4)_HyperTransport I/F
Size A3	Document Number W37
Rev	SB
Date: Friday, March 25, 2005	Sheet 4 of 51

VREF_DDR_MEM

NOTE: Test with passive probes only.

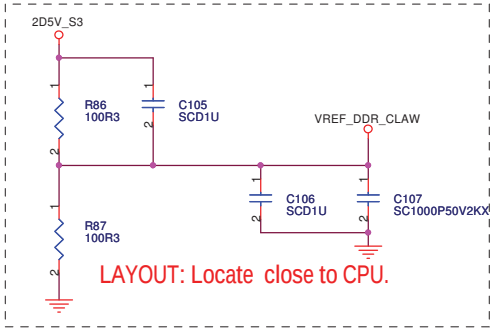
NOTE: Install to bypass op-amp



LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



LAYOUT: Locate close to CPU.

U70B

TP28 TPAD30 — DDRVTT_SENSE — AE13 — VTT_SENSE

2D5V_S3 — VREF_DDR_CLAW — AG12 — MEMVREF1

R37 34D8R2F MEMZN D14 — MEMZN

R36 34D8R2F MEMZP C14 — MEMZP

1D25V_S3

VTT_A D17
VTT_A A18
VTT_A B17
VTT_A C17
VTT_A AF16
VTT_B AG16
VTT_B AH16
VTT_B AJ17
VTT_B

C102 SCD1U — C53 SC1000P50V2KX

For REGISTED DIMM Only
UNBUFFER DIMM NC

MEMRESET_L AG10 MEMRESET#

MEMCKEA AE8 M_CKE#0 — M_CKE#0 8,9
MEMCKEB AE7 M_CKE#1 — M_CKE#1 8,9

MEMCLK_H7	D10	M_CLK7	M_CLK7 8,9
MEMCLK_L7	C10	M_CLK#7	M_CLK#7 8,9
MEMCLK_H6	E12	M_CLK6	M_CLK6 8,9
MEMCLK_L6	E11	M_CLK#6	M_CLK#6 8,9
MEMCLK_H5	AF8	M_CLK5	M_CLK5 8,9
MEMCLK_L5	AG8	M_CLK#5	M_CLK#5 8,9
MEMCLK_H4	AF10	M_CLK4	M_CLK4 8,9
MEMCLK_L4	AE10	M_CLK#4	M_CLK#4 8,9
MEMCLK_H3	V3		
MEMCLK_L3	V4		
MEMCLK_H2	K5		
MEMCLK_L2	K4		
MEMCLK_H1	R5	M_CLK1	
MEMCLK_L1	P5	M_CLK#1	
MEMCLK_H0	P3	M_CLK0	
MEMCLK_L0	P4	M_CLK#0	

2D5V_S3

RN3: M_CLK#1, M_CLK#0, M_CLK1, M_CLK0 — SRN10K-2

MEMCS_L7	D8	M_CS#7	
MEMCS_L6	C8	M_CS#6	
MEMCS_L5	E8	M_CS#5	
MEMCS_L4	E7	M_CS#4	
MEMCS_L3	D6	M_CS#3	M_CS#3 8,9
MEMCS_L2	E6	M_CS#2	M_CS#2 8,9
MEMCS_L1	C4	M_CS#1	M_CS#1 8,9
MEMCS_L0	E5	M_CS#0	M_CS#0 8,9

MEMRASA_L	H5	M_ARAS#	M_ARAS# 8,9
MEMCASA_L	D4	M_ACAS#	M_ACAS# 8,9
MEMWEA_L	G5	M_AWE#	M_AWE# 8,9

MEMBANKA1	K3	M_ABS#1	M_ABS#1 8,9
MEMBANKA0	H3	M_ABS#0	M_ABS#0 8,9

NC_E13 E13 RSVD_M_AA15
NC_C12 C12 RSVD_M_AA14

MEMADDA13	E10	M_AA13
MEMADDA12	AE6	M_AA12
MEMADDA11	AF3	M_AA11
MEMADDA10	M5	M_AA10
MEMADDA9	AE5	M_AA9
MEMADDA8	AB5	M_AA8
MEMADDA7	AD3	M_AA7
MEMADDA6	Y5	M_AA6
MEMADDA5	AB4	M_AA5
MEMADDA4	Y3	M_AA4
MEMADDA3	V5	M_AA3
MEMADDA2	T5	M_AA2
MEMADDA1	T3	M_AA1
MEMADDA0	N5	M_AA0

M_AA[13..0] 8,9

AMD suggested M_AA13 connect to DIMM pin123

MEMRASB_L	H4	M_BRAS#	M_BRAS# 8,9
MEMCASB_L	F5	M_BCAS#	M_BCAS# 8,9
MEMWEB_L	F4	M_BWE#	M_BWE# 8,9

MEMBANKB1	L5	M_BBS#1	M_BBS#1 8,9
MEMBANKB0	J5	M_BBS#0	M_BBS#0 8,9

NC_E14 E14 RSVD_M_BA15
NC_D12 D12 RSVD_M_BA14

MEMADDB13	E9	M_BA13
MEMADDB12	AF6	M_BA12
MEMADDB11	AF4	M_BA11
MEMADDB10	M4	M_BA10
MEMADDB9	AD5	M_BA9
MEMADDB8	AC5	M_BA8
MEMADDB7	AD4	M_BA7
MEMADDB6	AA5	M_BA6
MEMADDB5	AB3	M_BA5
MEMADDB4	Y4	M_BA4
MEMADDB3	W5	M_BA3
MEMADDB2	U5	M_BA2
MEMADDB1	T4	M_BA1
MEMADDB0	M3	M_BA0

M_BA[13..0] 8,9

AMD suggested M_BA13 connect to DIMM pin123

MEMCHECK7	N3	CB7
MEMCHECK6	N1	CB6
MEMCHECK5	U3	CB5
MEMCHECK4	V1	CB4
MEMCHECK3	N2	CB3
MEMCHECK2	P1	CB2
MEMCHECK1	U1	CB1
MEMCHECK0	U2	CB0

TP68 TPAD30, TP64 TPAD30, TP65 TPAD30, TP61 TPAD30, TP67 TPAD30, TP63 TPAD30, TP60 TPAD30, TP66 TPAD30

BGA754-SKT-U

9 M_DATA[63..0]

M_DATA63	A16	MEMDATA63
M_DATA62	B15	MEMDATA62
M_DATA61	A12	MEMDATA61
M_DATA60	B11	MEMDATA60
M_DATA59	A17	MEMDATA59
M_DATA58	A15	MEMDATA58
M_DATA57	C13	MEMDATA57
M_DATA56	A11	MEMDATA56
M_DATA55	A10	MEMDATA55
M_DATA54	B9	MEMDATA54
M_DATA53	C7	MEMDATA53
M_DATA52	A6	MEMDATA52
M_DATA51	C11	MEMDATA51
M_DATA50	A9	MEMDATA50
M_DATA49	A5	MEMDATA49
M_DATA48	B5	MEMDATA48
M_DATA47	C5	MEMDATA47
M_DATA46	A4	MEMDATA46
M_DATA45	F2	MEMDATA45
M_DATA44	E1	MEMDATA44
M_DATA43	A3	MEMDATA43
M_DATA42	B3	MEMDATA42
M_DATA41	E3	MEMDATA41
M_DATA40	F1	MEMDATA40
M_DATA39	G2	MEMDATA39
M_DATA38	G1	MEMDATA38
M_DATA37	L3	MEMDATA37
M_DATA36	L1	MEMDATA36
M_DATA35	G3	MEMDATA35
M_DATA34	J2	MEMDATA34
M_DATA33	L2	MEMDATA33
M_DATA32	M1	MEMDATA32
M_DATA31	W1	MEMDATA31
M_DATA30	W3	MEMDATA30
M_DATA29	AC1	MEMDATA29
M_DATA28	AC3	MEMDATA28
M_DATA27	W2	MEMDATA27
M_DATA26	Y1	MEMDATA26
M_DATA25	AC2	MEMDATA25
M_DATA24	AD1	MEMDATA24
M_DATA23	AE1	MEMDATA23
M_DATA22	AE3	MEMDATA22
M_DATA21	AG3	MEMDATA21
M_DATA20	AJ4	MEMDATA20
M_DATA19	AE2	MEMDATA19
M_DATA18	AF1	MEMDATA18
M_DATA17	AH3	MEMDATA17
M_DATA16	AJ3	MEMDATA16
M_DATA15	AJ5	MEMDATA15
M_DATA14	AJ6	MEMDATA14
M_DATA13	AJ7	MEMDATA13
M_DATA12	AH9	MEMDATA12
M_DATA11	AG5	MEMDATA11
M_DATA10	AH5	MEMDATA10
M_DATA9	AJ9	MEMDATA9
M_DATA8	AJ10	MEMDATA8
M_DATA7	AH11	MEMDATA7
M_DATA6	AJ11	MEMDATA6
M_DATA5	AH15	MEMDATA5
M_DATA4	AJ15	MEMDATA4
M_DATA3	AG11	MEMDATA3
M_DATA2	AJ12	MEMDATA2
M_DATA1	AJ14	MEMDATA1
M_DATA0	AJ16	MEMDATA0

9 M_ADM[7..0]

M_ADM8	R1	MEMDQS17
M_ADM7	A13	MEMDQS16
M_ADM6	A7	MEMDQS15
M_ADM5	C2	MEMDQS14
M_ADM4	H1	MEMDQS13
M_ADM3	AA1	MEMDQS12
M_ADM2	AG1	MEMDQS11
M_ADM1	AH7	MEMDQS10
M_ADM0	AH13	MEMDQS9
M_DQS8	T1	MEMDQS8
M_DQS7	A14	MEMDQS7
M_DQS6	A8	MEMDQS6
M_DQS5	D1	MEMDQS5
M_DQS4	J1	MEMDQS4
M_DQS3	AB1	MEMDQS3
M_DQS2	AJ2	MEMDQS2
M_DQS1	AJ8	MEMDQS1
M_DQS0	AJ13	MEMDQS0

9 M_DQS[7..0]

MEMZN TP2 TPAD30
MEMZP TP1 TPAD30
M_DQS8 TP62 TPAD30
M_ADM8 TP69 TPAD30

MEMRESET# TP31 TPAD30
M_CS#7 TP10 TPAD30
M_CS#6 TP12 TPAD30
M_CS#5 TP9 TPAD30
M_CS#4 TP11 TPAD30
RSVD_M_AA15 TP5 TPAD30
RSVD_M_AA14 TP7 TPAD30
RSVD_M_BA15 TP6 TPAD30
RSVD_M_BA14 TP8 TPAD30

NOT SUPPORT ECC CHECK
AMD suggested remove
PULL-HI resistor.

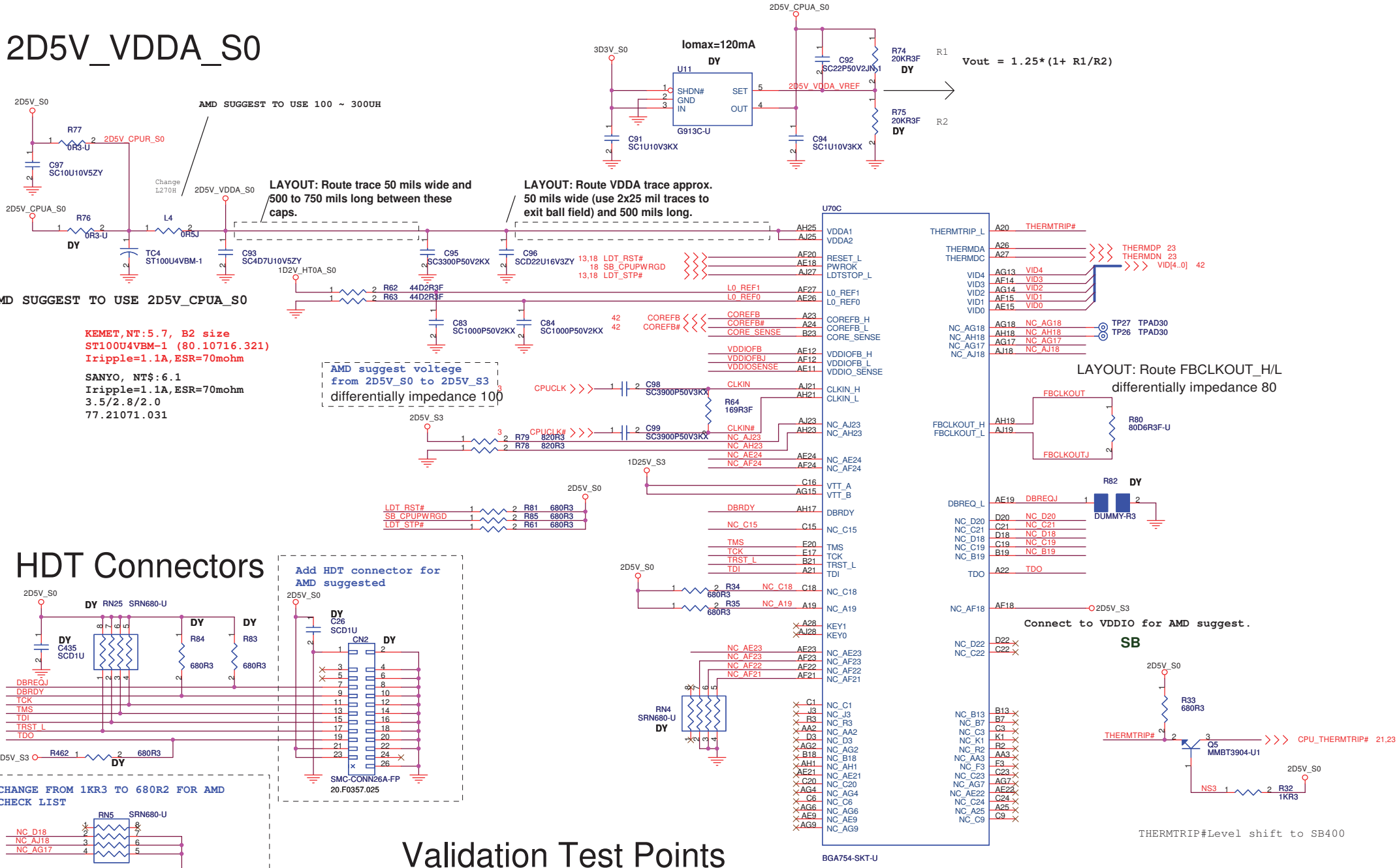
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size: A3 | Document Number: W37 | Rev: SB

Date: Friday, March 25, 2005 | Sheet 5 of 51

2D5V_VDDA_S0

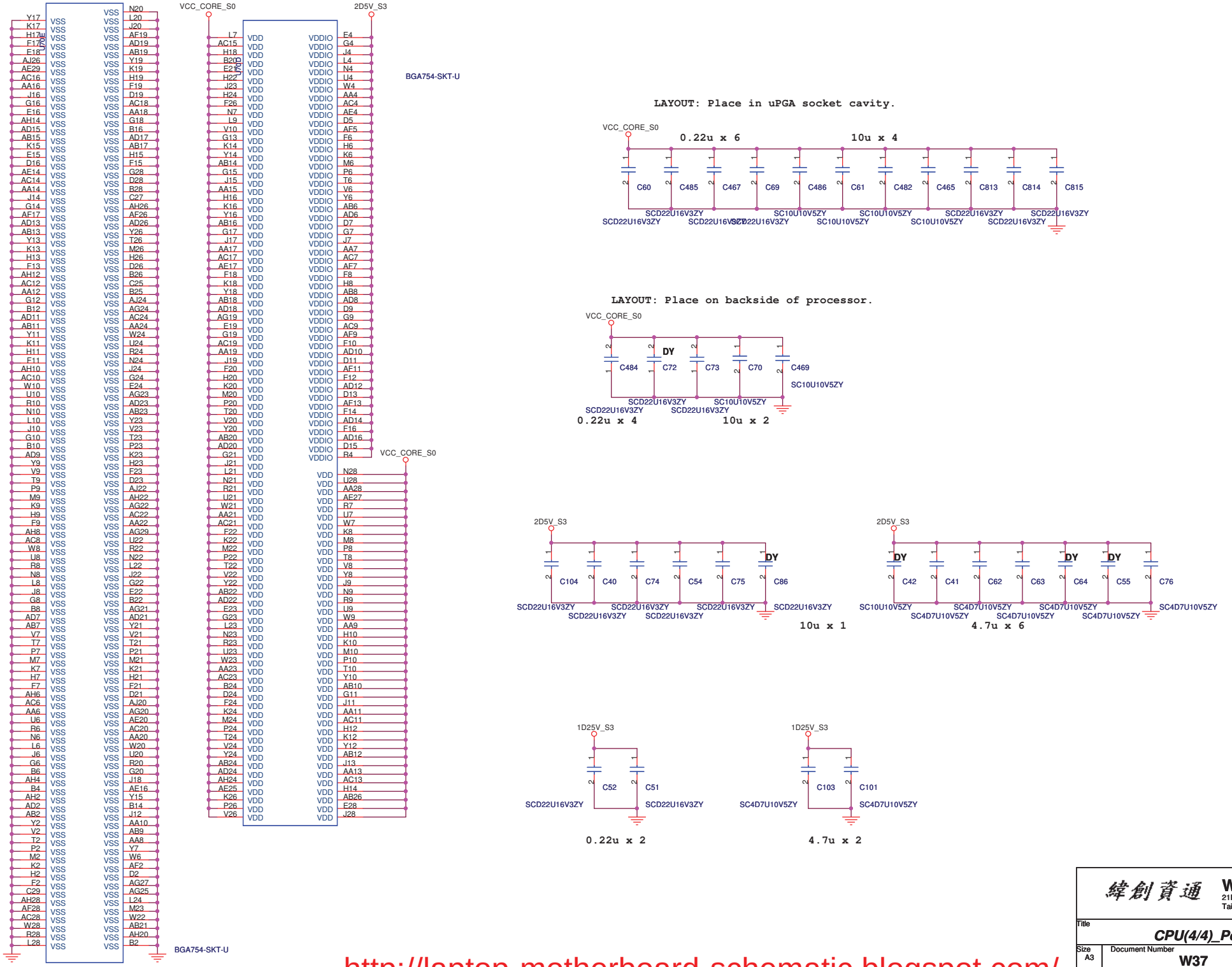


HDT Connectors

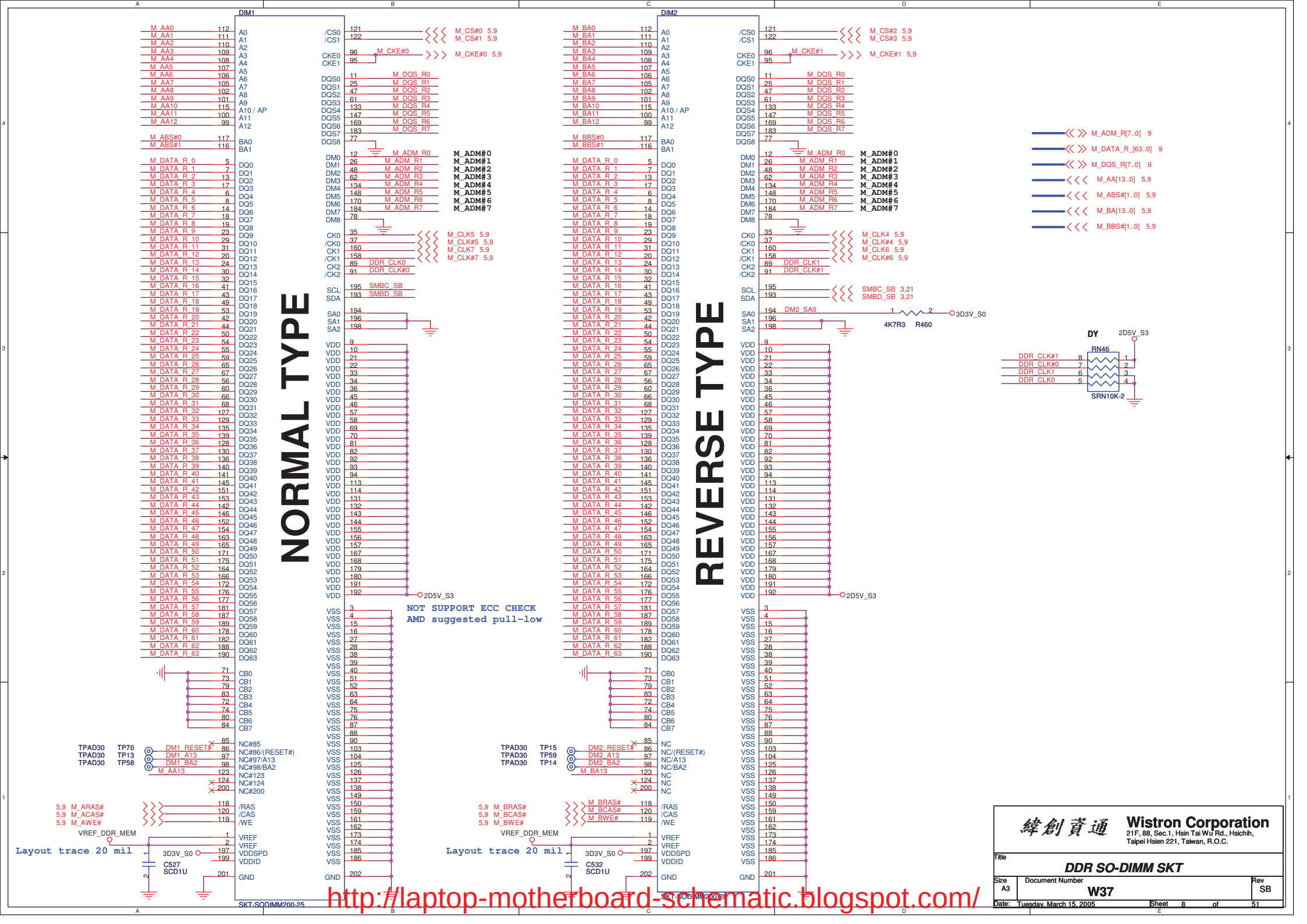
Validation Test Points

LAYOUT: Place close to the CPU.

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU(3/4)_Control & Debug	
Size A3	Document Number W37	Rev SB
Date: Friday, March 25, 2005	Sheet 6 of 51	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU(4/4)_Power***
Size: A3	Document Number: **W37**
Rev: SB	
Date: Friday, March 25, 2005	Sheet 7 of 51



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR SO-DIMM SKT

Size: A3 | Document Number: W37 | Rev: SB

Date: Tuesday, March 15, 2005 | Sheet 8 of 51

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

RN55

M_DATA4	1	16	M_DATA_R_4
M_DATA5	2	15	M_DATA_R_5
M_ADM0	3	14	M_ADM_R0
M_DATA6	4	13	M_DATA_R_6
M_DATA7	5	12	M_DATA_R_7
M_DATA13	6	11	M_DATA_R_13
M_DATA12	7	10	M_DATA_R_12
M_ADM1	8	9	M_ADM_R1

SRN10J-3

RN30

M_DATA37	1	16	M_DATA_R_37
M_DATA32	2	15	M_DATA_R_32
M_DATA33	3	14	M_DATA_R_33
M_DATA36	4	13	M_DATA_R_36
M_DQS4	5	12	M_DQS_R4
M_ADM4	6	11	M_ADM_R4
M_DATA34	7	10	M_DATA_R_34
M_DATA39	8	9	M_DATA_R_39

SRN10J-3

RN56

M_DATA0	1	16	M_DATA_R_0
M_DATA1	2	15	M_DATA_R_1
M_DQS0	3	14	M_DQS_R0
M_DATA2	4	13	M_DATA_R_2
M_DATA3	5	12	M_DATA_R_3
M_DATA8	6	11	M_DATA_R_8
M_DATA9	7	10	M_DATA_R_9
M_DQS1	8	9	M_DQS_R1

SRN10J-3

RN32

M_DATA35	1	16	M_DATA_R_35
M_DATA41	2	15	M_DATA_R_41
M_DATA40	3	14	M_DATA_R_40
M_DQS5	4	13	M_DQS_R5
M_DATA42	5	12	M_DATA_R_42
M_DATA43	6	11	M_DATA_R_43
M_DATA49	7	10	M_DATA_R_49
M_DATA48	8	9	M_DATA_R_48

SRN10J-3

RN47

M_DATA14	1	16	M_DATA_R_14
M_DATA15	2	15	M_DATA_R_15
M_DATA21	3	14	M_DATA_R_21
M_DATA20	4	13	M_DATA_R_20
M_ADM2	5	12	M_ADM_R2
M_DATA23	6	11	M_DATA_R_23
M_DATA22	7	10	M_DATA_R_22
M_DATA25	8	9	M_DATA_R_25

SRN10J-3

RN31

M_DATA38	1	16	M_DATA_R_38
M_DATA45	2	15	M_DATA_R_45
M_DATA44	3	14	M_DATA_R_44
M_ADM5	4	13	M_ADM_R5
M_DATA47	5	12	M_DATA_R_47
M_DATA46	6	11	M_DATA_R_46
M_DATA53	7	10	M_DATA_R_53
M_DATA52	8	9	M_DATA_R_52

SRN10J-3

RN48

M_DATA11	1	16	M_DATA_R_11
M_DATA10	2	15	M_DATA_R_10
M_DATA17	3	14	M_DATA_R_17
M_DATA16	4	13	M_DATA_R_16
M_DQS2	5	12	M_DQS_R2
M_DATA19	6	11	M_DATA_R_19
M_DATA18	7	10	M_DATA_R_18
M_DATA24	8	9	M_DATA_R_24

SRN10J-3

RN27

M_DQS6	1	16	M_DQS_R6
M_DATA50	2	15	M_DATA_R_50
M_DATA51	3	14	M_DATA_R_51
M_DATA56	4	13	M_DATA_R_56
M_DATA57	5	12	M_DATA_R_57
M_DQS7	6	11	M_DQS_R7
M_DATA58	7	10	M_DATA_R_58
M_DATA59	8	9	M_DATA_R_59

SRN10J-3

RN43

M_DATA29	1	16	M_DATA_R_29
M_DATA28	2	15	M_DATA_R_28
M_DQS3	3	14	M_DQS_R3
M_ADM3	4	13	M_ADM_R3
M_DATA26	5	12	M_DATA_R_26
M_DATA27	6	11	M_DATA_R_27
M_DATA30	7	10	M_DATA_R_30
M_DATA31	8	9	M_DATA_R_31

SRN10J-3

RN26

M_ADM6	1	16	M_ADM_R6
M_DATA54	2	15	M_DATA_R_54
M_DATA55	3	14	M_DATA_R_55
M_DATA61	4	13	M_DATA_R_61
M_DATA60	5	12	M_DATA_R_60
M_ADM7	6	11	M_ADM_R7
M_DATA62	7	10	M_DATA_R_62
M_DATA63	8	9	M_DATA_R_63

SRN10J-3

5,8 M_CKE#0 <<< M_CKE#0

5,8 M_CKE#1 <<< M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

RN57

M_ADM_R1	1	16	M_DATA_R_39
M_DATA_R_13	2	15	M_DATA_R_38
M_DATA_R_12	3	14	M_DQS_R4
M_DATA_R_6	4	13	M_ADM_R4
M_DATA_R_7	5	12	M_DATA_R_32
M_ADM_R0	6	11	M_DATA_R_33
M_DATA_R_5	7	10	M_DATA_R_37
M_DATA_R_4	8	9	M_DATA_R_36

SRN68J-1

RN36

	1	16	M_DATA_R_39
	2	15	M_DATA_R_38
	3	14	M_DQS_R4
	4	13	M_ADM_R4
	5	12	M_DATA_R_32
	6	11	M_DATA_R_33
	7	10	M_DATA_R_37
	8	9	M_DATA_R_36

SRN68J-1

RN58

M_DATA_R_0	1	16	M_DATA_R_48
M_DATA_R_1	2	15	M_DATA_R_49
M_DQS_R0	3	14	M_DATA_R_43
M_DATA_R_2	4	13	M_DATA_R_42
M_DATA_R_3	5	12	M_DQS_R5
M_DATA_R_8	6	11	M_DATA_R_41
M_DATA_R_9	7	10	M_DATA_R_40
M_DQS_R1	8	9	M_DATA_R_34

SRN68J-1

RN35

	1	16	M_DATA_R_48
	2	15	M_DATA_R_49
	3	14	M_DATA_R_43
	4	13	M_DATA_R_42
	5	12	M_DQS_R5
	6	11	M_DATA_R_41
	7	10	M_DATA_R_40
	8	9	M_DATA_R_34

SRN68J-1

RN49

M_DATA_R_25	1	16	M_DATA_R_35
M_DATA_R_22	2	15	M_DATA_R_44
M_DATA_R_23	3	14	M_DATA_R_45
M_ADM_R2	4	13	M_ADM_R5
M_DATA_R_20	5	12	M_DATA_R_46
M_DATA_R_21	6	11	M_DATA_R_47
M_DATA_R_14	7	10	M_DATA_R_53
M_DATA_R_15	8	9	M_DATA_R_52

SRN68J-1

RN34

	1	16	M_DATA_R_35
	2	15	M_DATA_R_44
	3	14	M_DATA_R_45
	4	13	M_ADM_R5
	5	12	M_DATA_R_46
	6	11	M_DATA_R_47
	7	10	M_DATA_R_53
	8	9	M_DATA_R_52

SRN68J-1

RN50

M_DATA_R_10	1	16	M_DATA_R_59
M_DATA_R_11	2	15	M_DATA_R_58
M_DATA_R_16	3	14	M_DQS_R7
M_DATA_R_17	4	13	M_DATA_R_57
M_DQS_R2	5	12	M_DATA_R_56
M_DATA_R_19	6	11	M_DATA_R_51
M_DATA_R_18	7	10	M_DATA_R_50
M_DATA_R_24	8	9	M_DQS_R6

SRN68J-1

RN29

	1	16	M_DATA_R_59
	2	15	M_DATA_R_58
	3	14	M_DQS_R7
	4	13	M_DATA_R_57
	5	12	M_DATA_R_56
	6	11	M_DATA_R_51
	7	10	M_DATA_R_50
	8	9	M_DQS_R6

SRN68J-1

RN45

M_DATA_R_30	1	16	M_ADM_R6
M_DATA_R_31	2	15	M_DATA_R_55
M_DATA_R_26	3	14	M_DATA_R_54
M_DATA_R_27	4	13	M_DATA_R_60
M_ADM_R3	5	12	M_DATA_R_61
M_DQS_R3	6	11	M_ADM_R7
M_DATA_R_29	7	10	M_DATA_R_63
M_DATA_R_28	8	9	M_DATA_R_62

SRN68J-1

RN28

	1	16	M_ADM_R6
	2	15	M_DATA_R_55
	3	14	M_DATA_R_54
	4	13	M_DATA_R_60
	5	12	M_DATA_R_61
	6	11	M_ADM_R7
	7	10	M_DATA_R_63
	8	9	M_DATA_R_62

SRN68J-1

1D25V_S3

RN41

M_CKE#1	2	3	
M_BA12	1	4	

SRN47J
RN40

M_CKE#0	2	3	
M_AA12	1	4	

SRN47J
RN44

M_AA11	1	16	
M_AA9	2	15	
M_AA7	3	14	
M_AA5	4	13	
M_AA4	5	12	
M_AA8	6	11	
M_AA6	7	10	
M_AA3	8	9	

SRN47J-1-U
RN39

M_CS#3	1	16	
M_BA13	2	15	
M_CS#2	3	14	
M_BRAS#	4	13	
M_BBS#1	5	12	
M_BCAS#	6	11	
M_BA0	7	10	
M_BA2	8	9	

SRN47J-1-U
RN37

M_AA1	1	16	
M_AA10	2	15	
M_AA2	3	14	
M_AA0	4	13	
M_ABS#1	5	12	
M_ABS#0	6	11	
M_AWE#	7	10	
M_ARAS#	8	9	

SRN47J-1-U
RN42

M_BA7	1	16	
M_BA3	2	15	
M_BA6	3	14	
M_BA9	4	13	
M_BA10	5	12	
M_BA1	6	11	
M_BBS#0	7	10	
M_BWE#	8	9	

SRN47J-1-U
RN38

M_BA5	1	8	
M_BA8	2	7	
M_BA4	3	6	
M_BA11	4	5	

SRN47-1

RN33

M_AA13	1	8	
M_CS#0	2	7	
M_CS#1	3	6	
M_ACAS#	4	5	

SRN47-1

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8

M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8

M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8

M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

Place it near CPU

R42 121R2F: M_CLK7 / M_CLK#7 → M_CLK7 5,8 / M_CLK#7 5,8

R41 121R2F: M_CLK6 / M_CLK#6 → M_CLK6 5,8 / M_CLK#6 5,8

R66 121R2F: M_CLK5 / M_CLK#5 → M_CLK5 5,8 / M_CLK#5 5,8

R65 121R2F: M_CLK4 / M_CLK#4 → M_CLK4 5,8 / M_CLK#4 5,8

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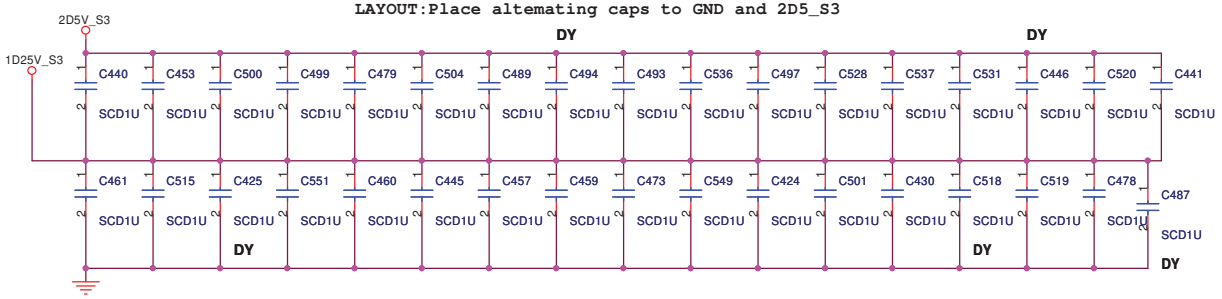
Taipei Hsien 221, Taiwan, R.O.C.

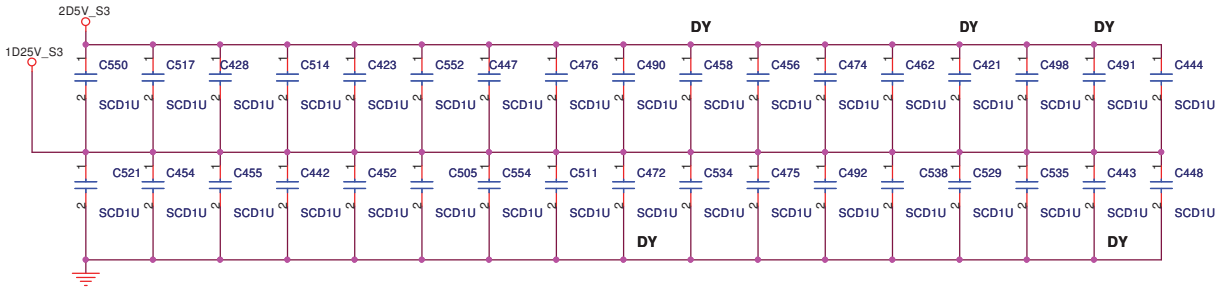
Title: DDR DAMPING & TERMINATION

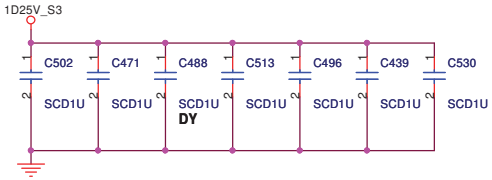
Size	Document Number	Rev
A3	W37	SB

Date: Tuesday, March 15, 2005 Sheet 9 of 51

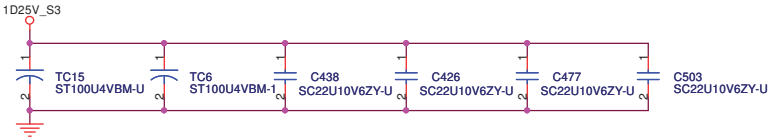
LAYOUT:Place altemating caps to GND and 2D5_S3







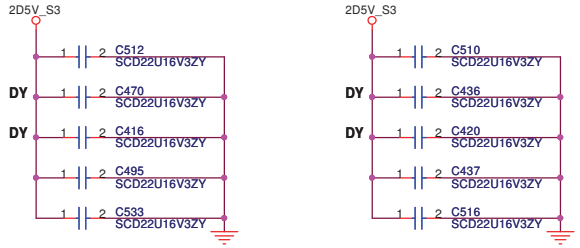
LAYOUT:Place at end of the DIMMs



KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

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Taipei Hsien 221, Taiwan, R.O.C.

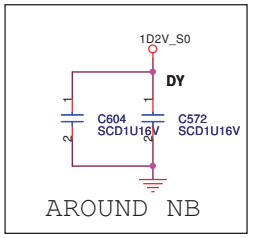
Title: DDR DECOUPLING

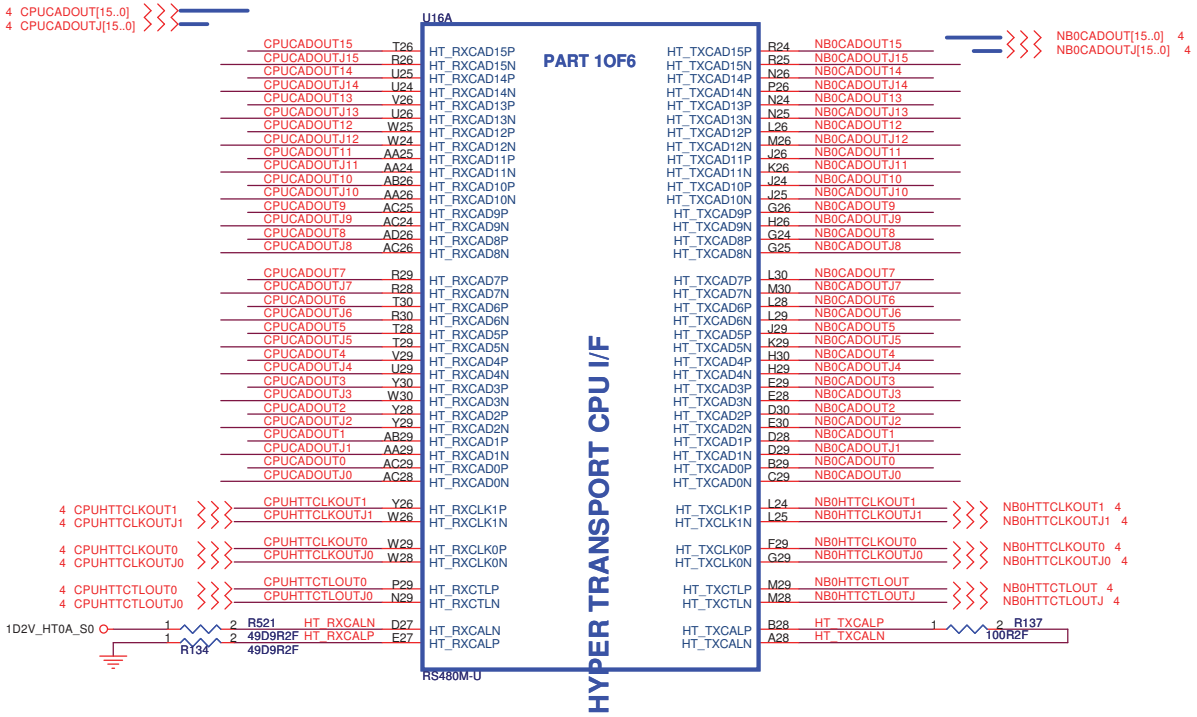
Size	Document Number	Rev
A3	W37	SB

Date: Tuesday, March 15, 2005 Sheet 10 of 51

CLAW HAMMER TO NB

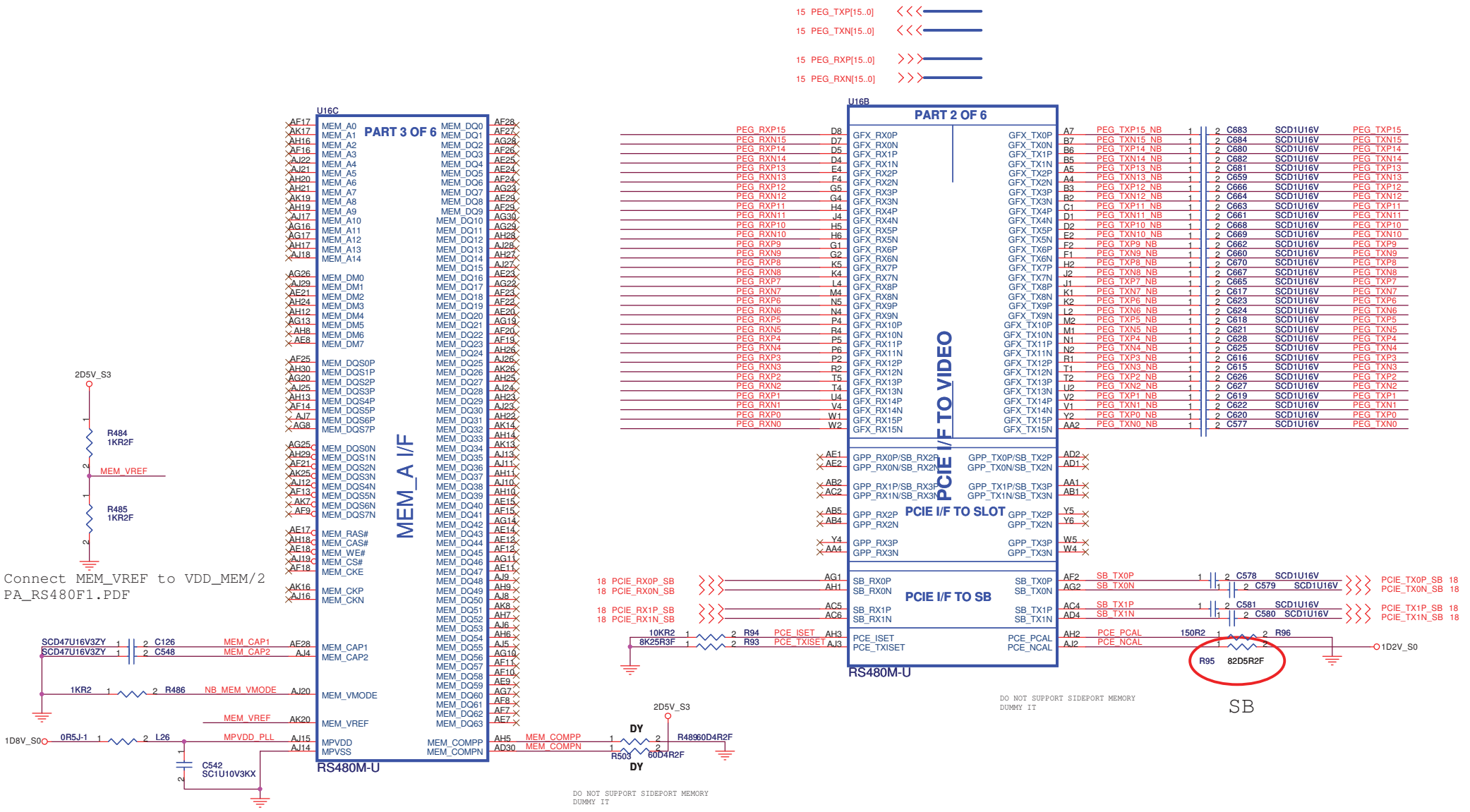
NB TO CLAW HAMMER





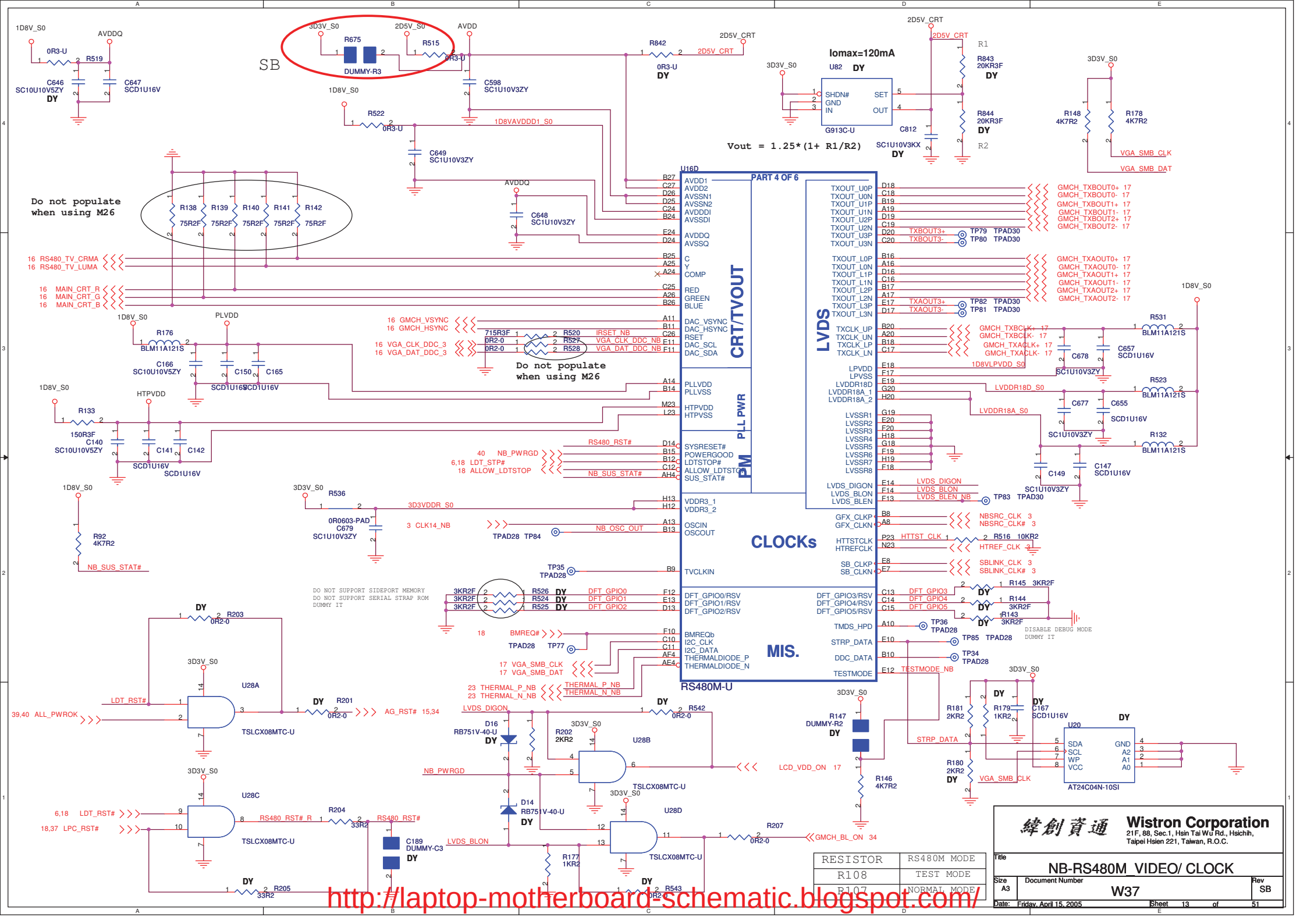
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

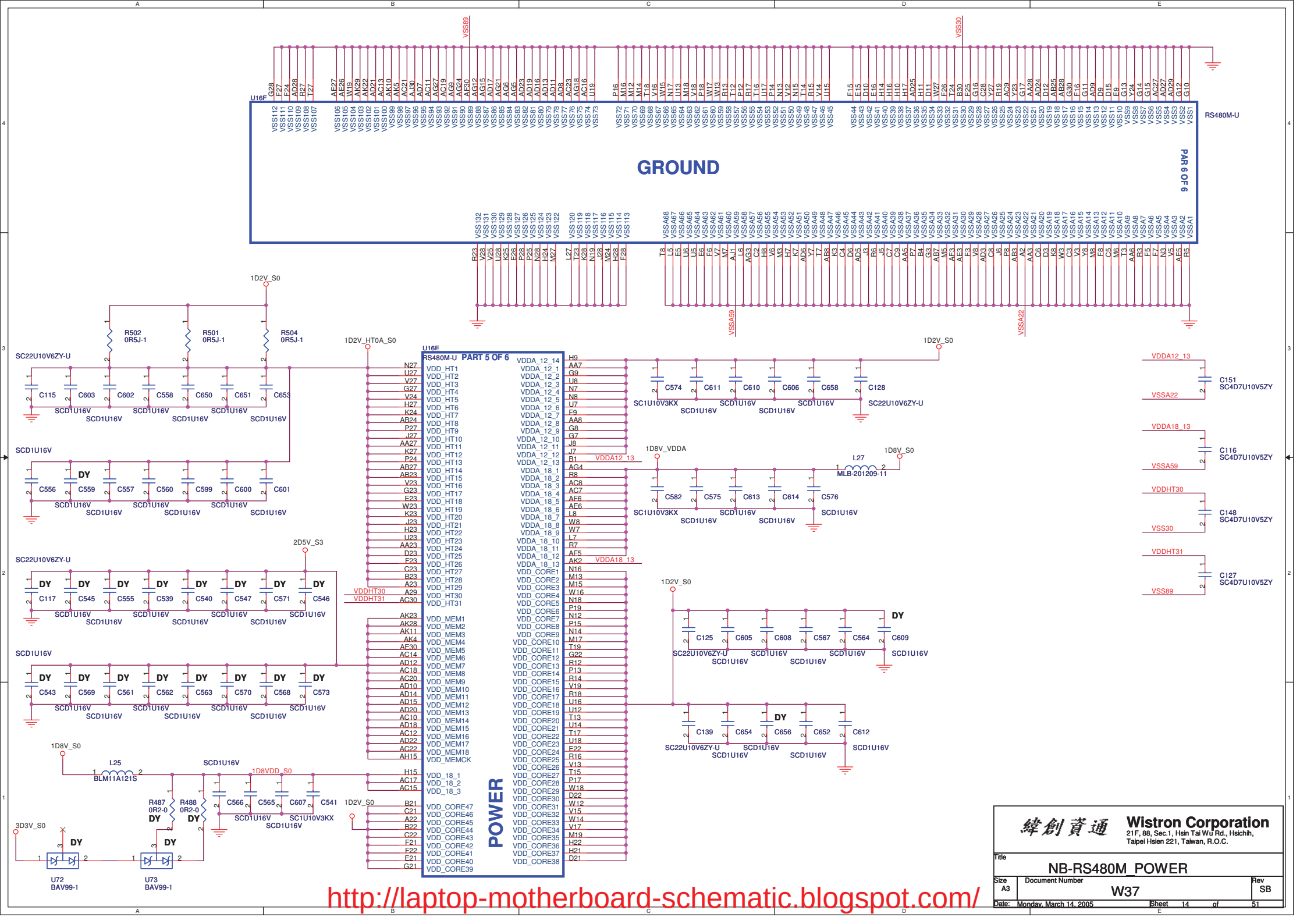
Title	NB-RS480M_HT	
Size A3	Document Number W37	Rev SB
Date: Tuesday, March 15, 2005	Sheet 11 of 51	



When disable local frame buffer, VDD_MEM connect to 2D5V_S3, MEM_VMODE connect to GND, MEM_VREF connect to 2D5V_S3, MPVDD connected to 1D8V
DSG-215-RS480-04.PDF

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	NB-RS480M_MEM/PCIE_LINK I/F
Size A3	Document Number W37
Rev	SB
Date: Tuesday, March 15, 2005	Sheet 12 of 51


SB
Do not populate when using M26
Do not populate when using M26
Vout = 1.25*(1+ R1/R2)
Iomax=120mA
U16D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
RS480M-U
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
DISABLE DEBUG MODE
DUMMY IT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB-RS480M_VIDEO/ CLOCK
W37
SB
Friday, April 15, 2005
13
51
RESISTOR | RS480M MODE
R108 | TEST MODE
R107 | NORMAL MODE
http://laptop-motherboard-schematic.blogspot.com/


GROUND
U16F
RS480M-U
PART 6 OF 6
U16E
RS480M-U PART 5 OF 6
POWER
1D2V_S0
1D8V_S0
1D8V_VDDA
2D5V_S3
3D3V_S0
1D2V_HT0A_S0
1D8VDD_S0
VDDA12_13
VDDA18_13
VDDHT30
VDDHT31
SC22U10V6ZY-U
SCD1U16V
SC1U10V3KX
R502 0R5J-1
R501 0R5J-1
R504 0R5J-1
L25 BLM11A121S
L27 MLB-201209-11
R487 0R2-0
R488 0R2-0
U72 BAV99-1
U73 BAV99-1
C151 SC4D7U10V5ZY
C116 SC4D7U10V5ZY
C148 SC4D7U10V5ZY
C127 SC4D7U10V5ZY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS480M_POWER
Size A3
Document Number W37
Rev SB
Date: Monday, March 14, 2005
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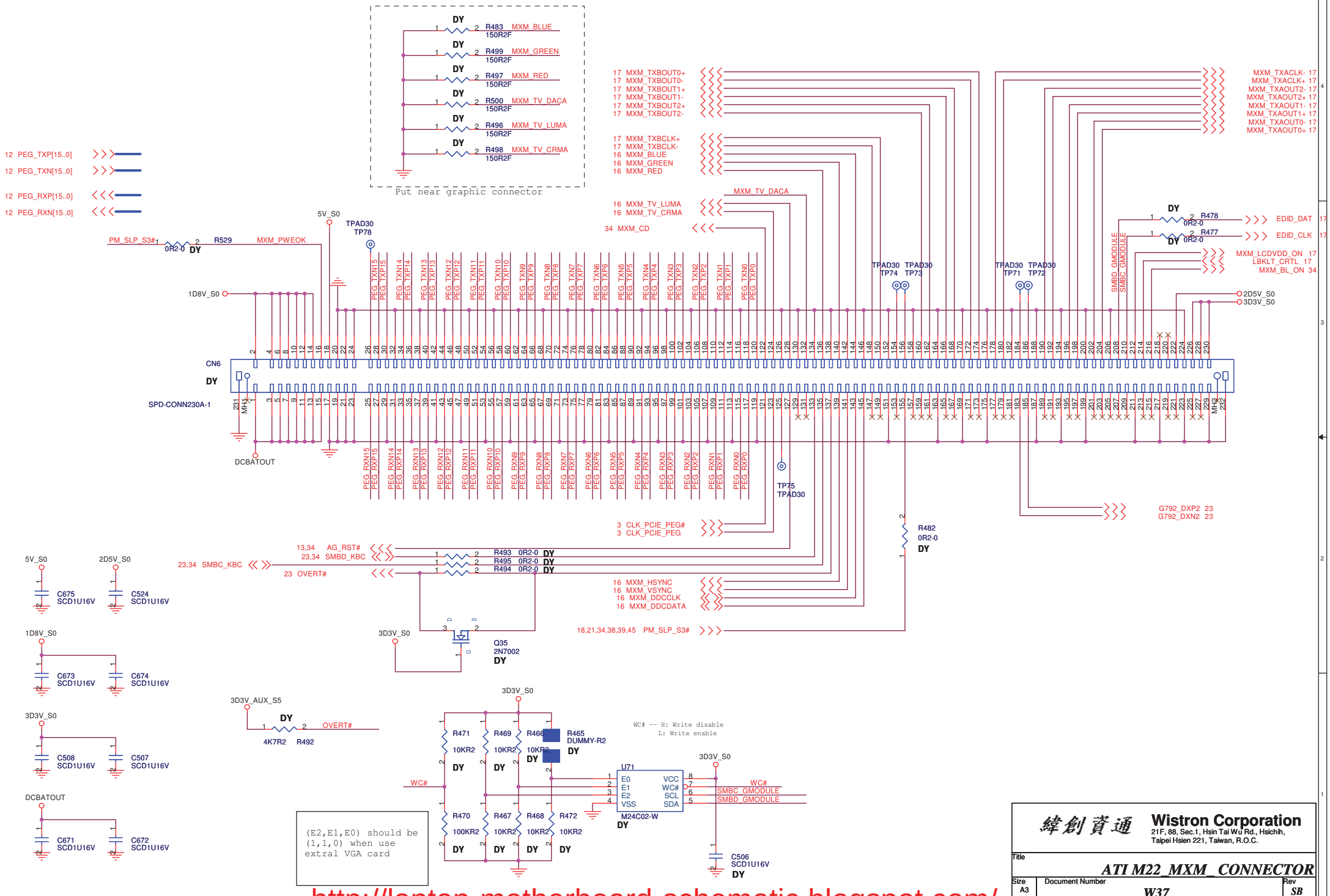
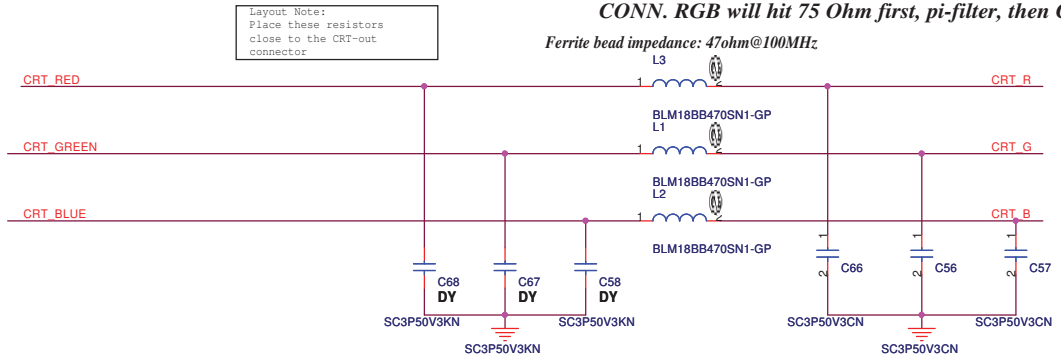
http://laptop-motherboard-schematic.blogspot.com/

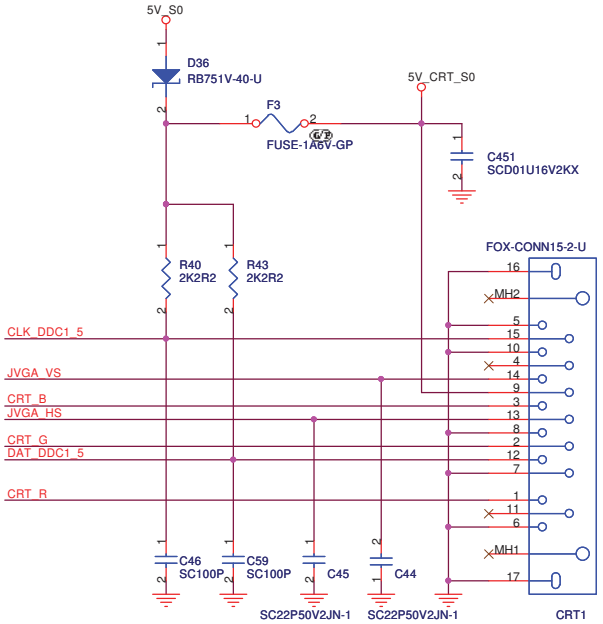


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ATI M22_MXM_CONNECTOR*
Size A3	Document Number *W37* Rev *SB*
Date: Tuesday, March 15, 2005	Sheet 15 of 51

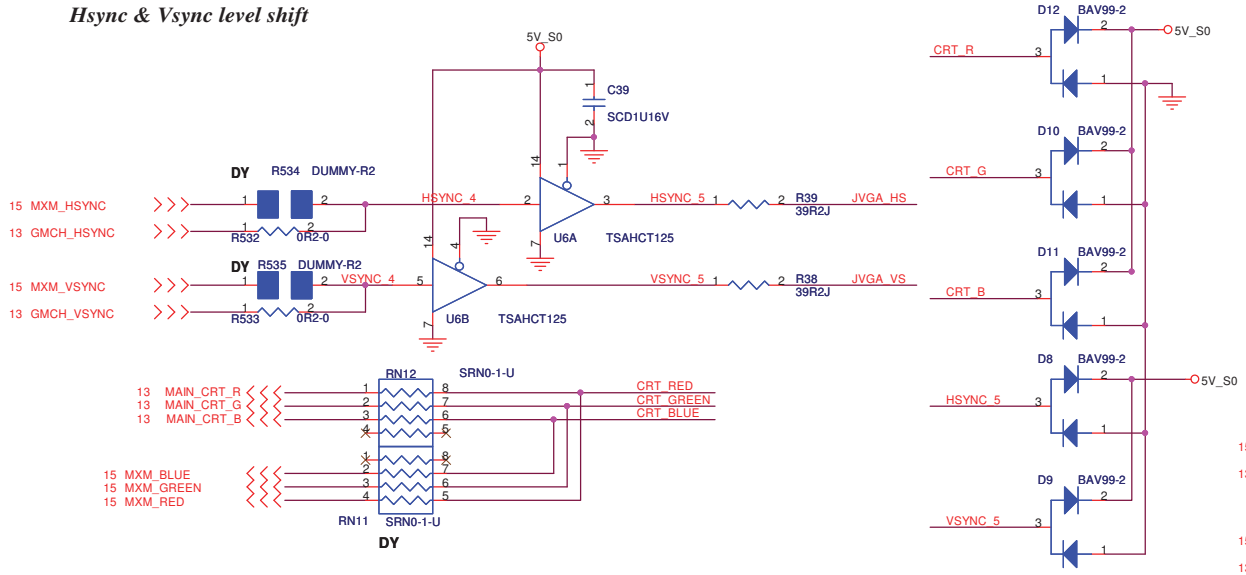
CRT I/F & CONNECTOR

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

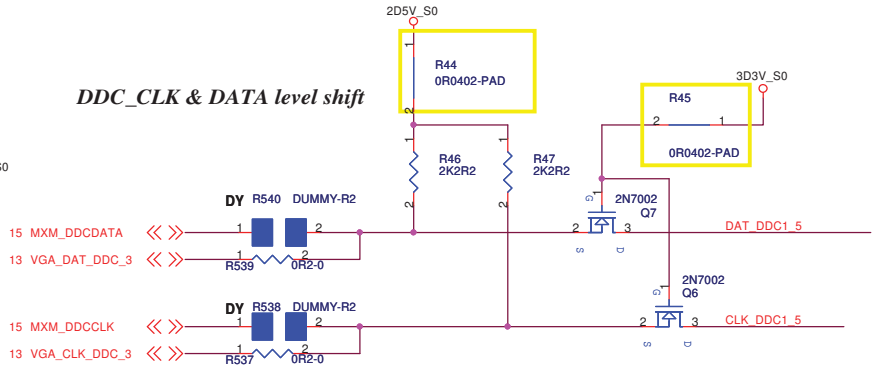




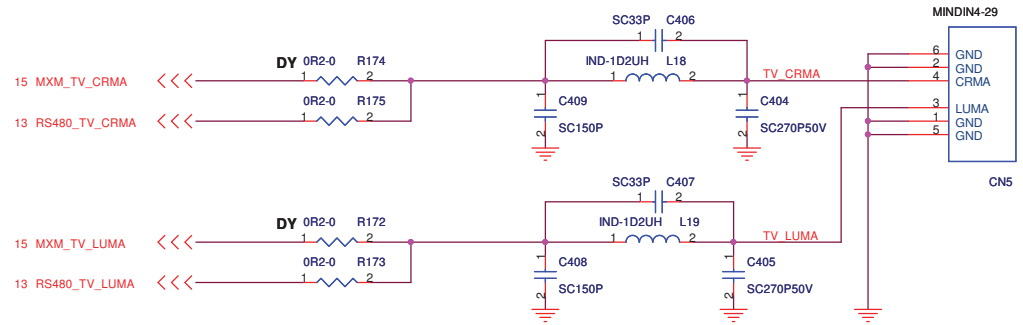
Hsync & Vsync level shift

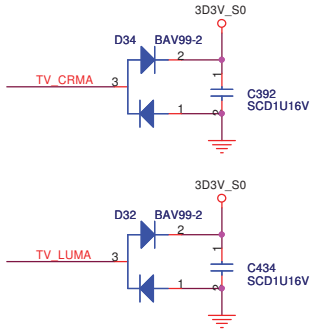


DDC_CLK & DATA level shift



5V @ ext. CRT side





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT/TV Connector		
Size: A3	Document Number: W37	Rev: SB
Date: Friday, April 15, 2005	Sheet 16 of 51	

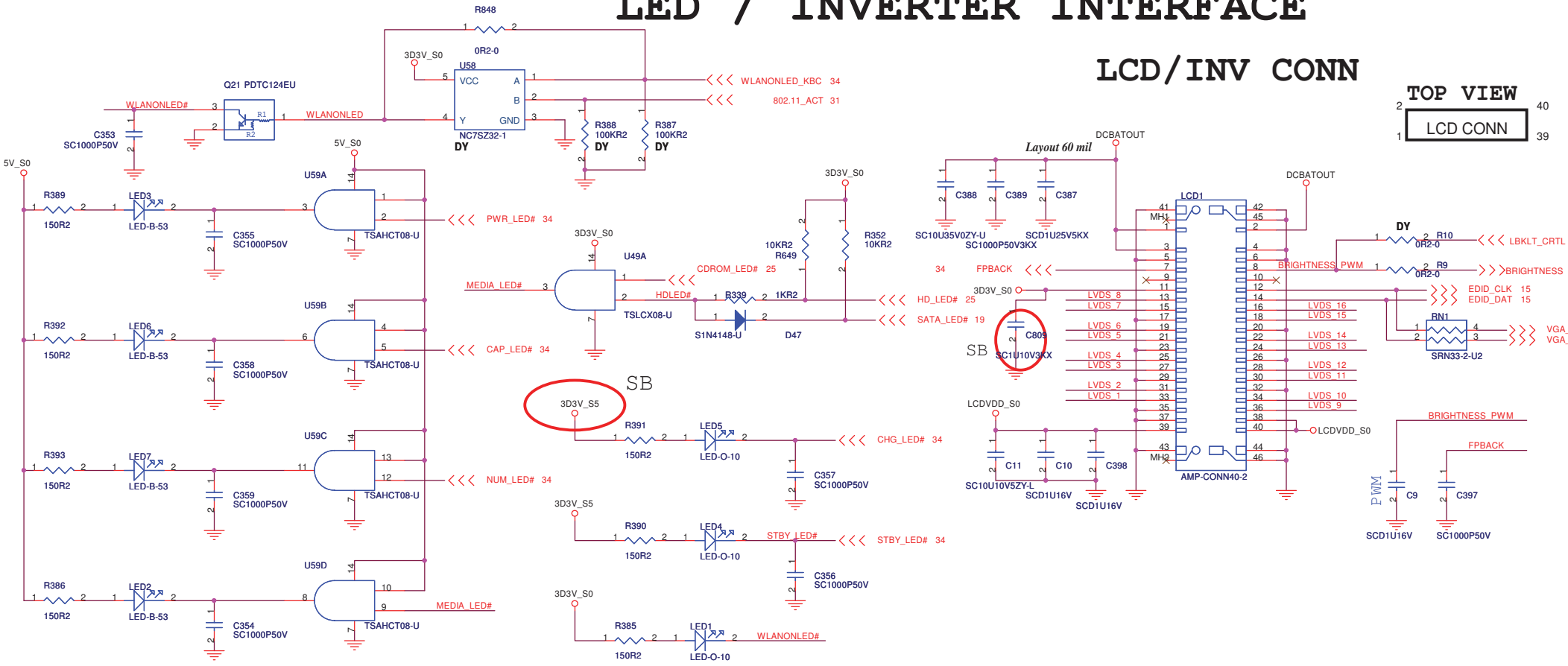
LED / INVERTER INTERFACE

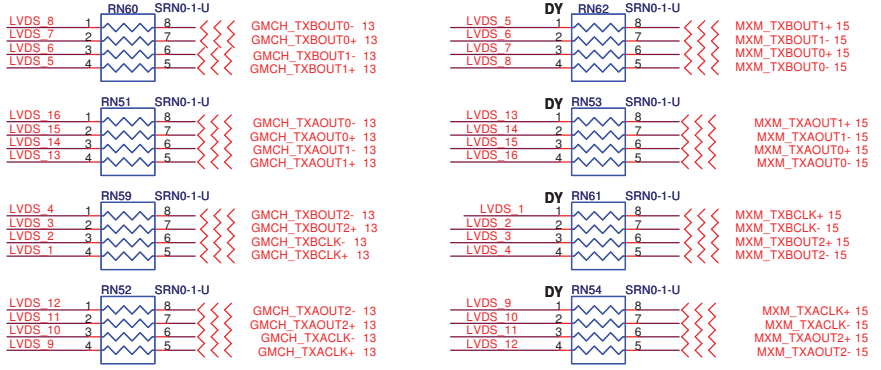
LCD/INV CONN

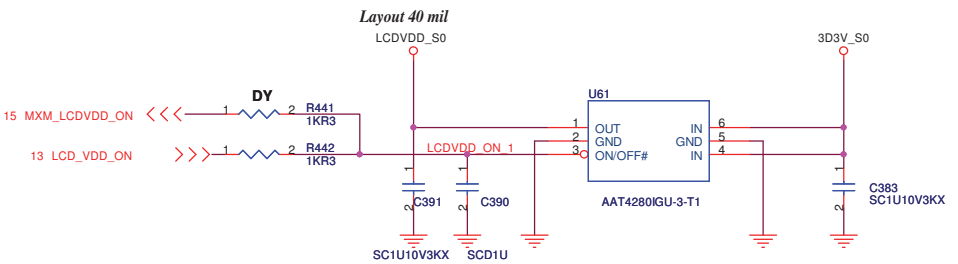
TOP VIEW

LCD CONN

LCD POWER

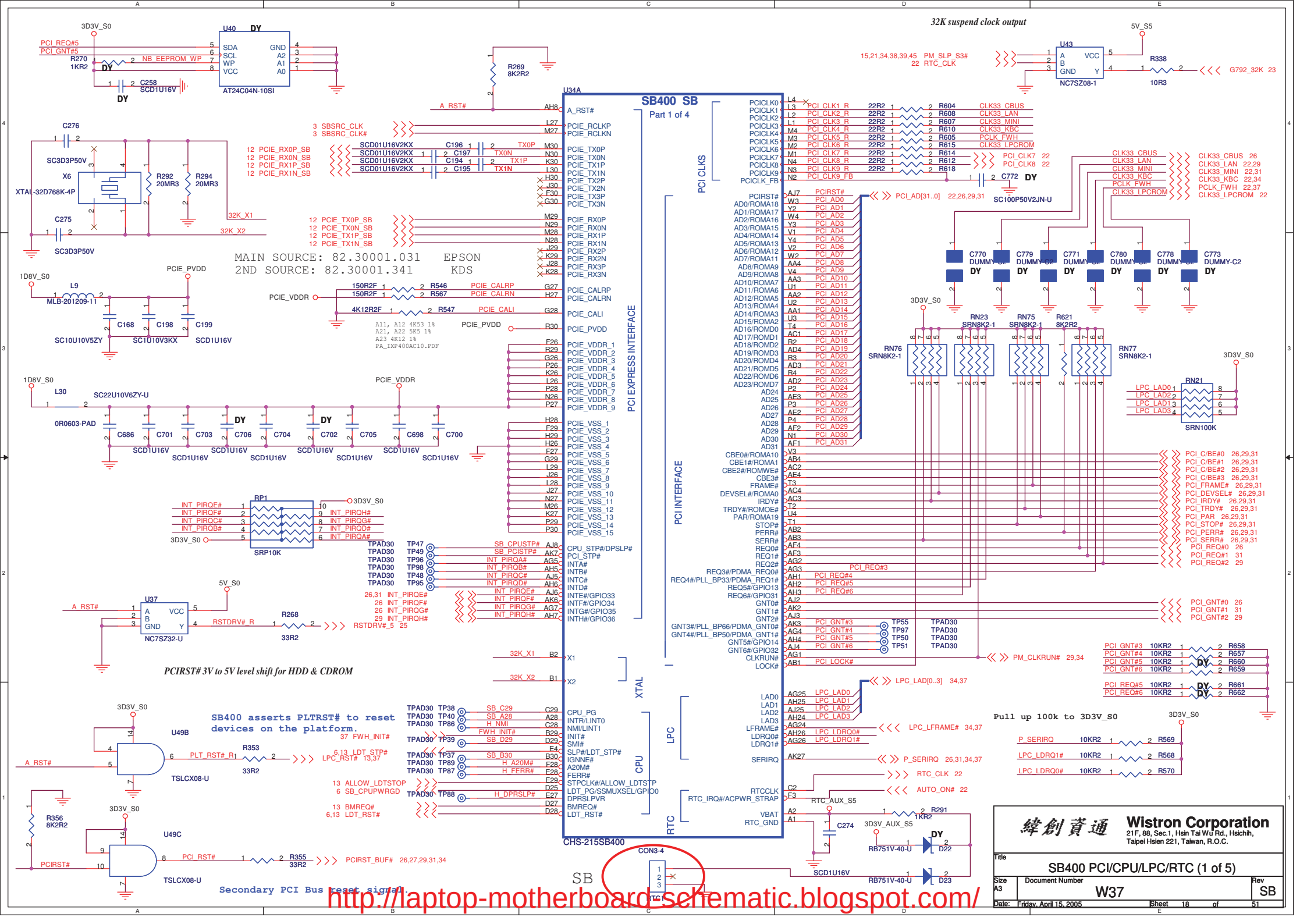


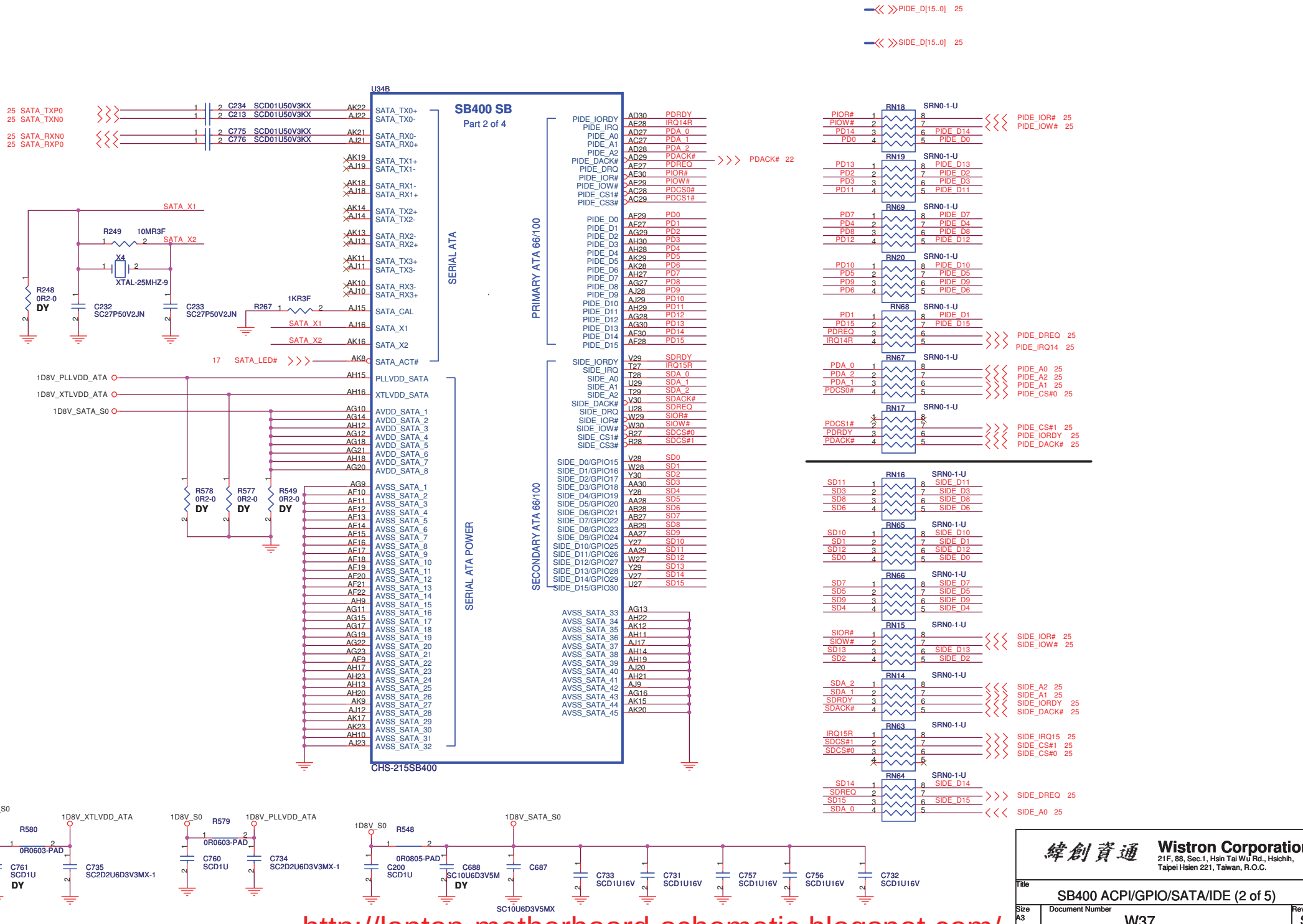


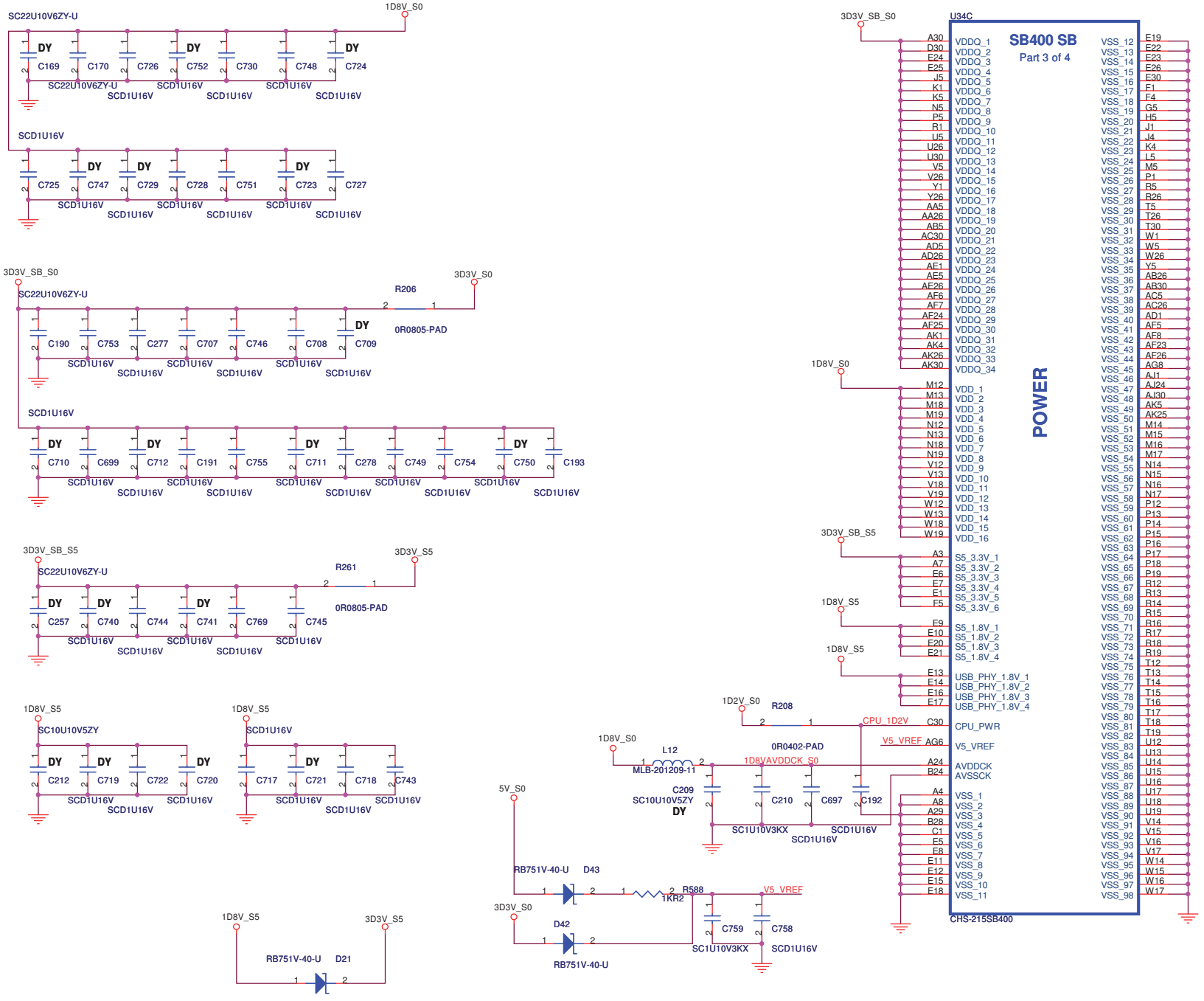


Place them as close to LCD as possible

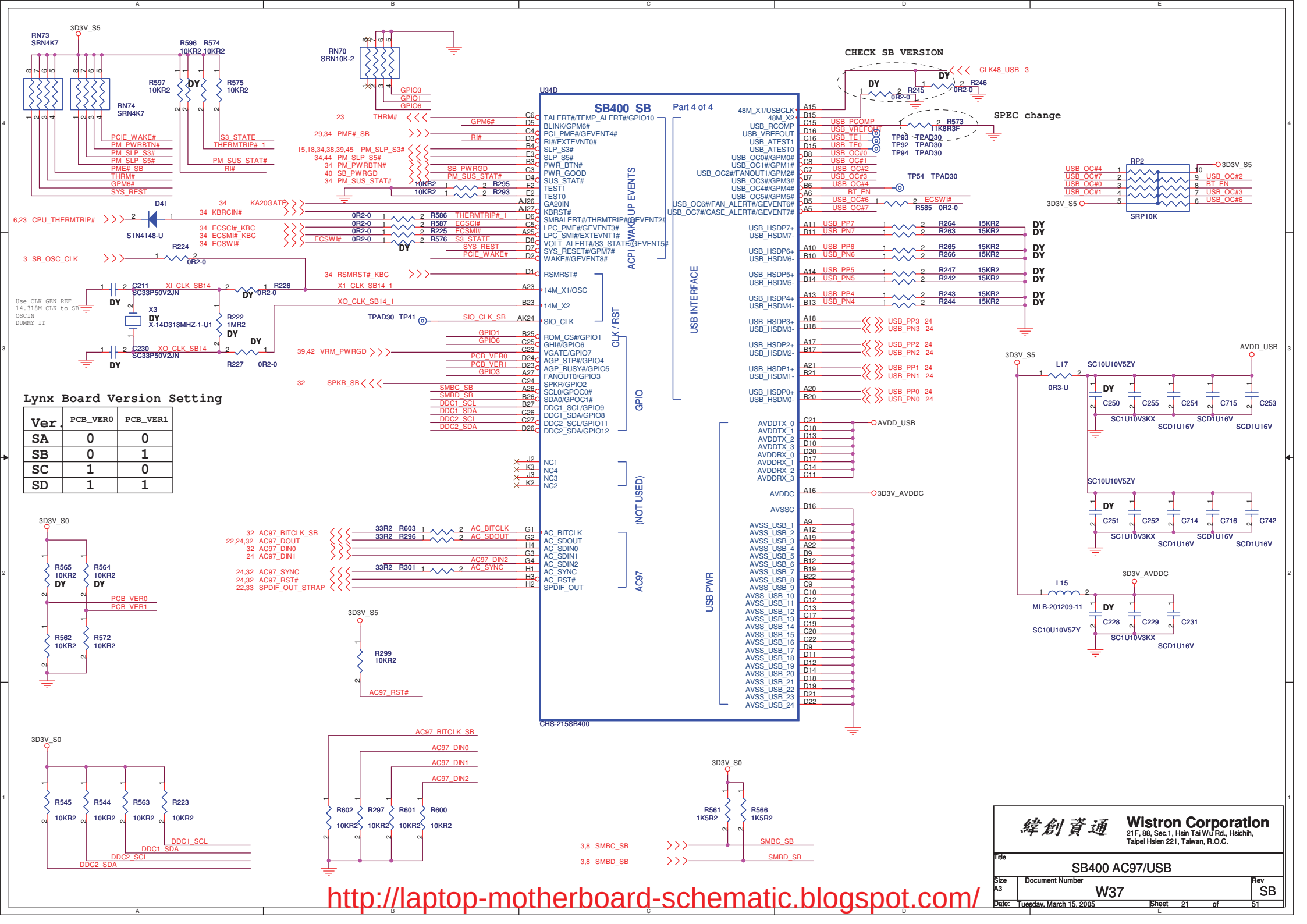
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: INV / LCD		
Size: A3	Document Number: W37	Rev: SB
Date: Wednesday, March 30, 2005	Sheet 17 of 51	

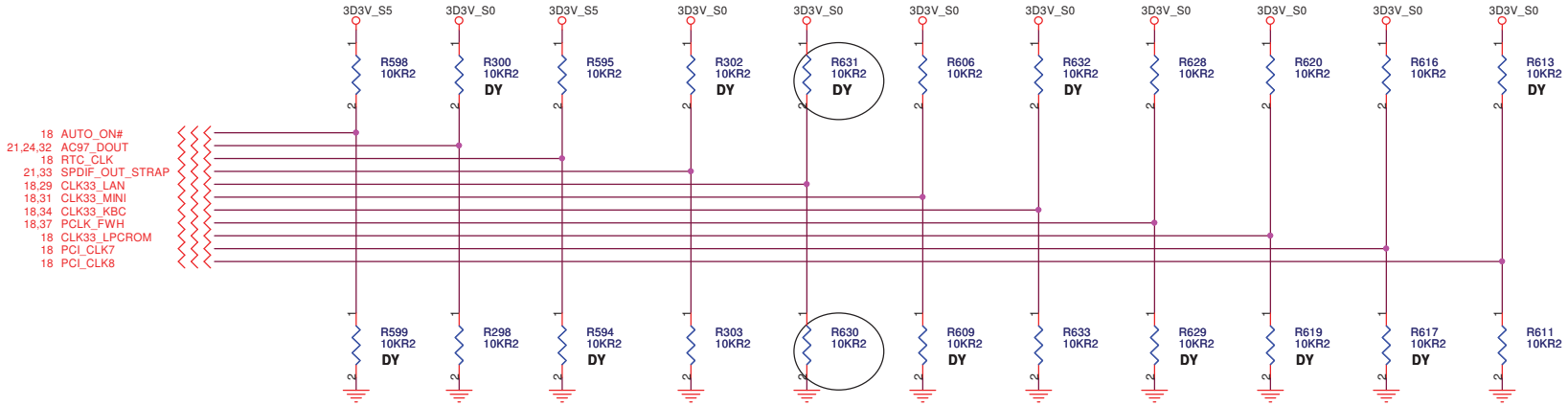

32K suspend clock output
SB400 SB
Part 1 of 4
U34A
CHS-215SB400
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
LPC
CPU
RTC
MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Pull up 100k to 3D3V_S0
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB400 PCI/CPU/LPC/RTC (1 of 5)
Size A3
Document Number W37
Rev SB
Date: Friday, April 15, 2005
Sheet 18 of 51
http://laptop-motherboardschematic.blogspot.com/


PIDE_D[15..0] 25
SIDE_D[15..0] 25
U34B
SB400 SB
Part 2 of 4
SERIAL ATA
SERIAL ATA POWER
PRIMARY ATA 66/100
SECONDARY ATA 66/100
CHS-215SB400
25 SATA_TXP0
25 SATA_TXN0
25 SATA_RXN0
25 SATA_RXP0
C234 SCD01U50V3KX
C213 SCD01U50V3KX
C775 SCD01U50V3KX
C776 SCD01U50V3KX
SATA_X1
SATA_X2
R249 10MR3F
X4
XTAL-25MHZ-9
R248 0R2-0 DY
C232 SC27P50V2JN
C233 SC27P50V2JN
R267 1KR3F
17 SATA_LED#
1D8V_PLLVDD_ATA
1D8V_XTLVDD_ATA
1D8V_SATA_S0
R578 0R2-0 DY
R577 0R2-0 DY
R549 0R2-0 DY
PDACK# 22
RN18 SRN0-1-U
PIOR# PIOW# PD14 PD0
PIDE_IOR# PIDE_IOW# PIDE_D14 PIDE_D0
RN19 SRN0-1-U
PD13 PD2 PD3 PD11
PIDE_D13 PIDE_D2 PIDE_D3 PIDE_D11
RN69 SRN0-1-U
PD7 PD4 PD8 PD12
PIDE_D7 PIDE_D4 PIDE_D8 PIDE_D12
RN20 SRN0-1-U
PD10 PD5 PD9 PD6
PIDE_D10 PIDE_D5 PIDE_D9 PIDE_D6
RN68 SRN0-1-U
PD1 PD15 PDREQ IRQ14R
PIDE_D1 PIDE_D15 PIDE_DREQ 25 PIDE_IRQ14 25
RN67 SRN0-1-U
PDA_0 PDA_2 PDA_1 PDCS0#
PIDE_A0 25 PIDE_A2 25 PIDE_A1 25 PIDE_CS#0 25
RN17 SRN0-1-U
PDCS1# PDRDY PDACK#
PIDE_CS#1 25 PIDE_IORDY 25 PIDE_DACK# 25
RN16 SRN0-1-U
SD11 SD3 SD8 SD6
SIDE_D11 SIDE_D3 SIDE_D8 SIDE_D6
RN65 SRN0-1-U
SD10 SD1 SD12 SD0
SIDE_D10 SIDE_D1 SIDE_D12 SIDE_D0
RN66 SRN0-1-U
SD7 SD5 SD9 SD4
SIDE_D7 SIDE_D5 SIDE_D9 SIDE_D4
RN15 SRN0-1-U
SIOR# SIOW# SD13 SD2
SIDE_IOR# 25 SIDE_IOW# 25 SIDE_D13 SIDE_D2
RN14 SRN0-1-U
SDA_2 SDA_1 SDRDY SDACK#
SIDE_A2 25 SIDE_A1 25 SIDE_IORDY 25 SIDE_DACK# 25
RN63 SRN0-1-U
IRQ15R SDCS#1 SDCS#0
SIDE_IRQ15 25 SIDE_CS#1 25 SIDE_CS#0 25
RN64 SRN0-1-U
SD14 SDREQ SD15 SDA_0
SIDE_D14 SIDE_D15 SIDE_DREQ 25 SIDE_A0 25
1D8V_S0
R580 0R0603-PAD
C761 SCD1U DY
C735 SC2D2U6D3V3MX-1
R579 0R0603-PAD
C760 SCD1U
C734 SC2D2U6D3V3MX-1
R548 0R0805-PAD
C200 SCD1U
C688 SC10U6D3V5M DY
C687 SC10U6D3V5MX
C733 SCD1U16V
C731 SCD1U16V
C757 SCD1U16V
C756 SCD1U16V
C732 SCD1U16V
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB400 ACPI/GPIO/SATA/IDE (2 of 5)
Size A3
Document Number W37
Rev SB
Date: Friday, April 15, 2005
Sheet 19 of 51
http://laptop-motherboard-schematic.blogspot.com/



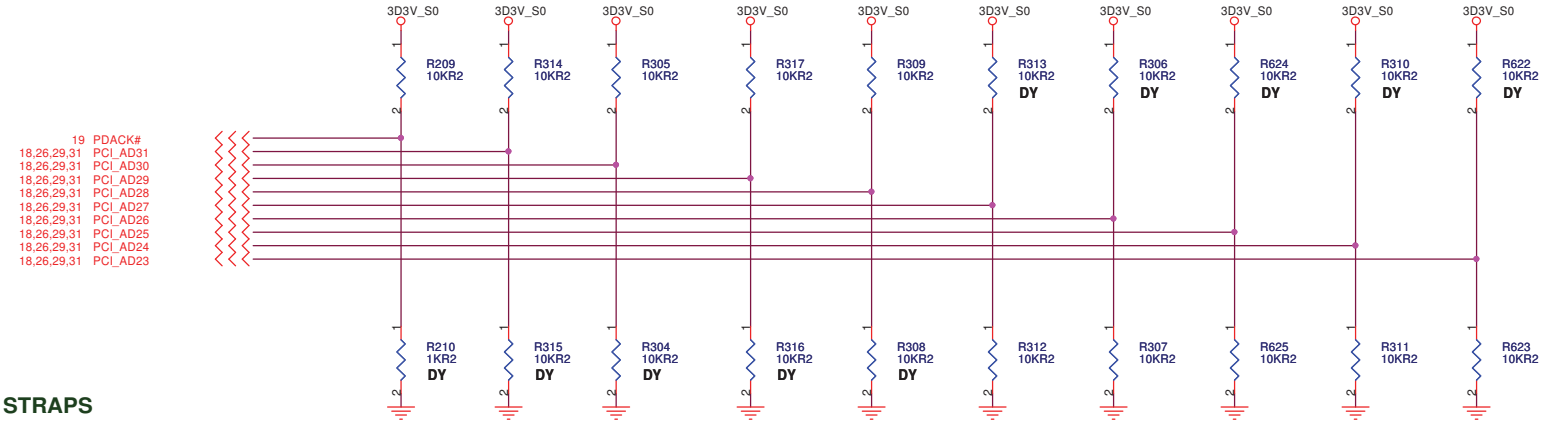
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB400 POWER/DECOUPLING	
Size A3	Document Number W37	Rev SB
Date: Friday, April 15, 2005	Sheet 20 of 51	


SB400 SB
Part 4 of 4
U34D
CHS-215SB400
CHECK SB VERSION
SPEC change
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
(NOT USED)
AC97
USB INTERFACE
USB PWR
Lynx Board Version Setting
Ver. PCB_VER0 PCB_VER1
SA 0 0
SB 0 1
SC 1 0
SD 1 1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB400 AC97/USB
Size A3
Document Number W37
Rev SB
Date: Tuesday, March 15, 2005
Sheet 21 of 51
http://laptop-motherboard-schematic.blogspot.com/



REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

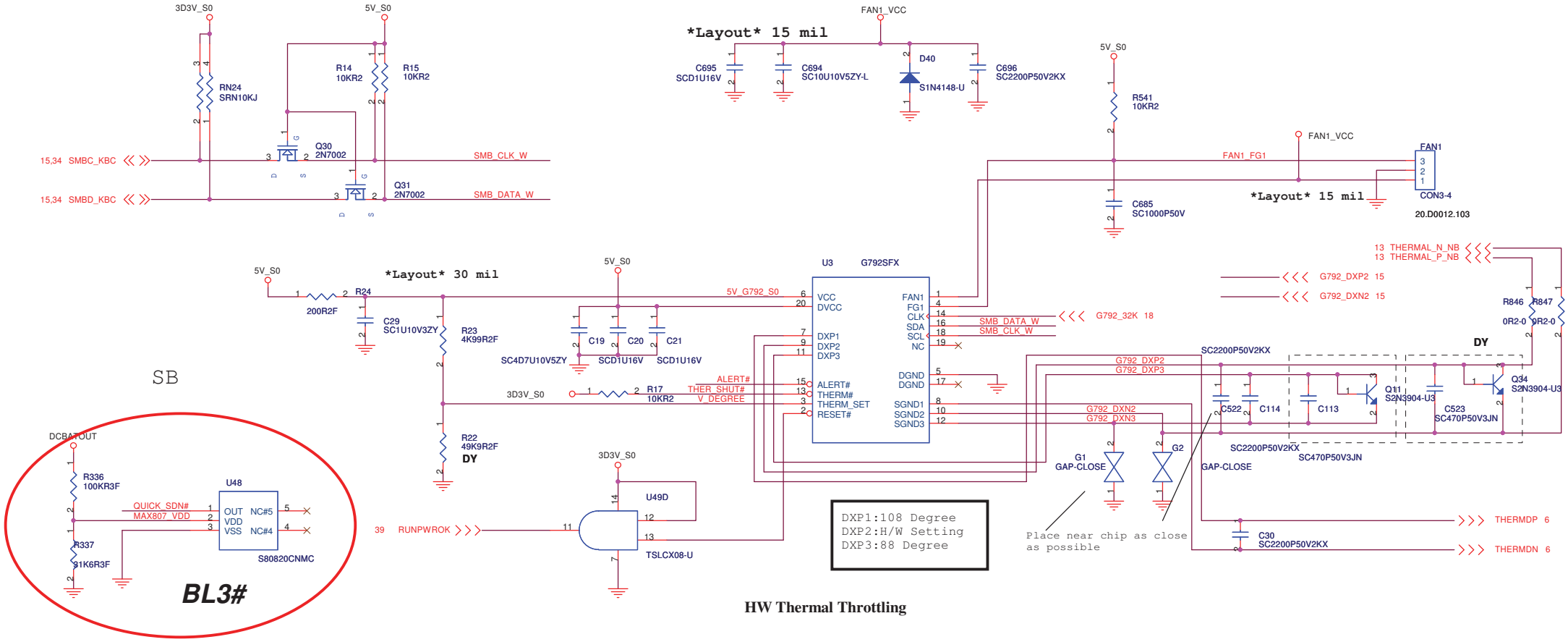
	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

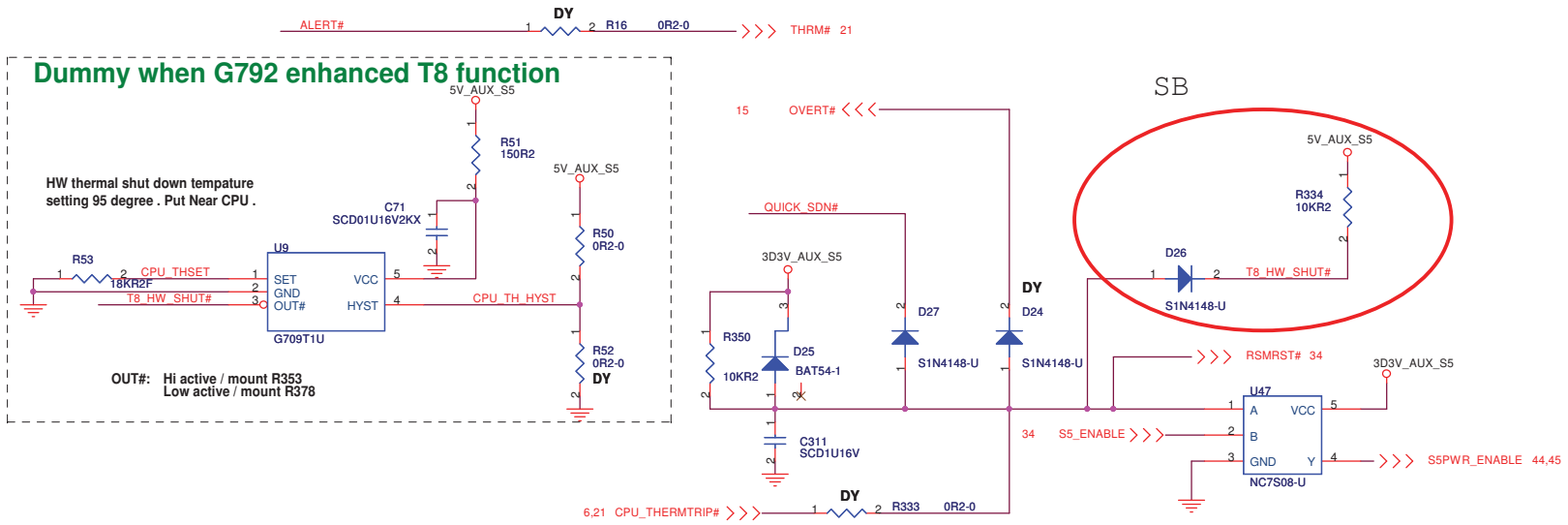
Title: SB400 STRAPPING PIN

Size: A3 | Document Number: W37 | Rev: SB

Date: Tuesday, March 15, 2005 | Sheet 22 of 51



HW Thermal Throttling



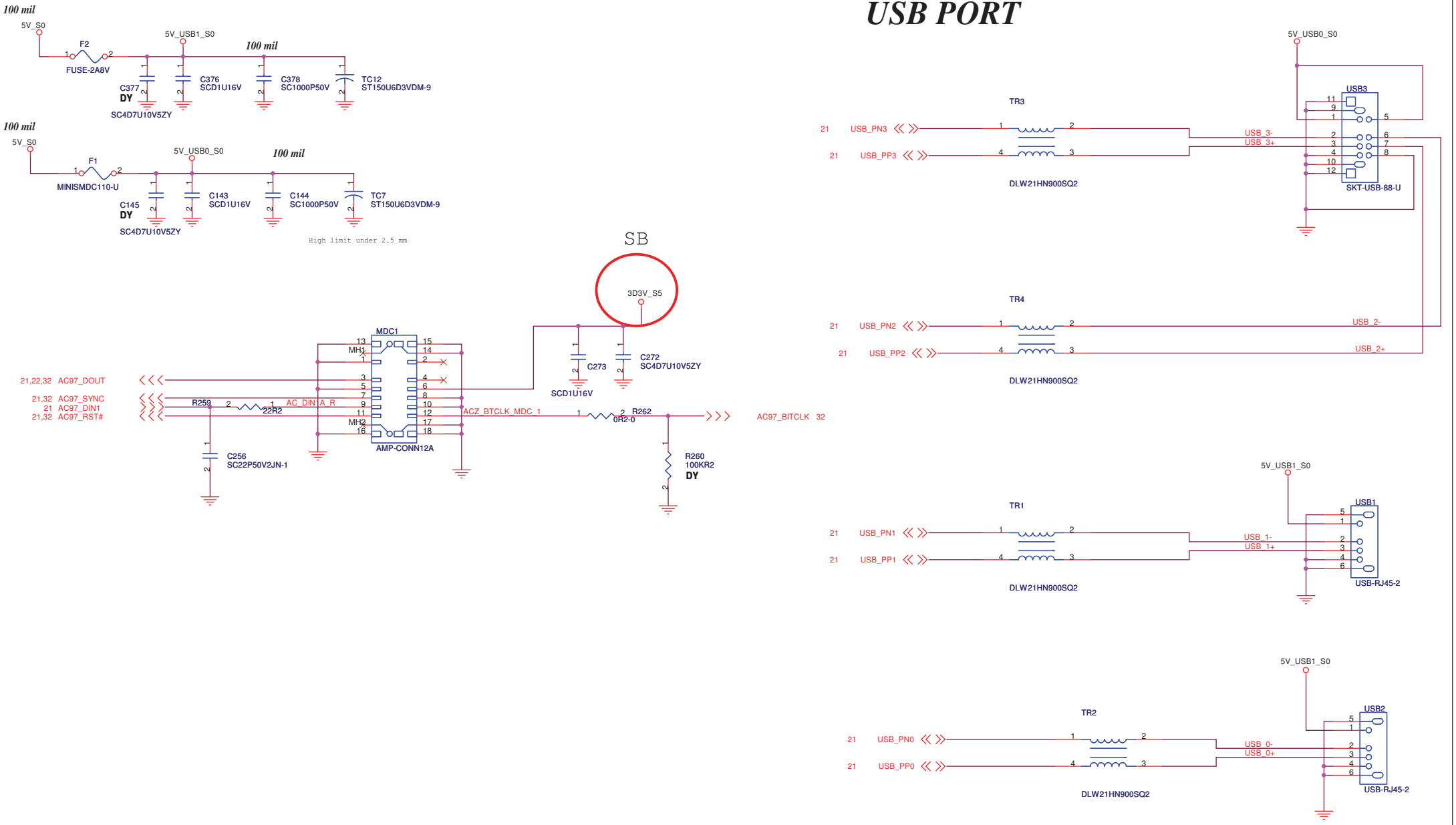
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: W37 | Rev: SB

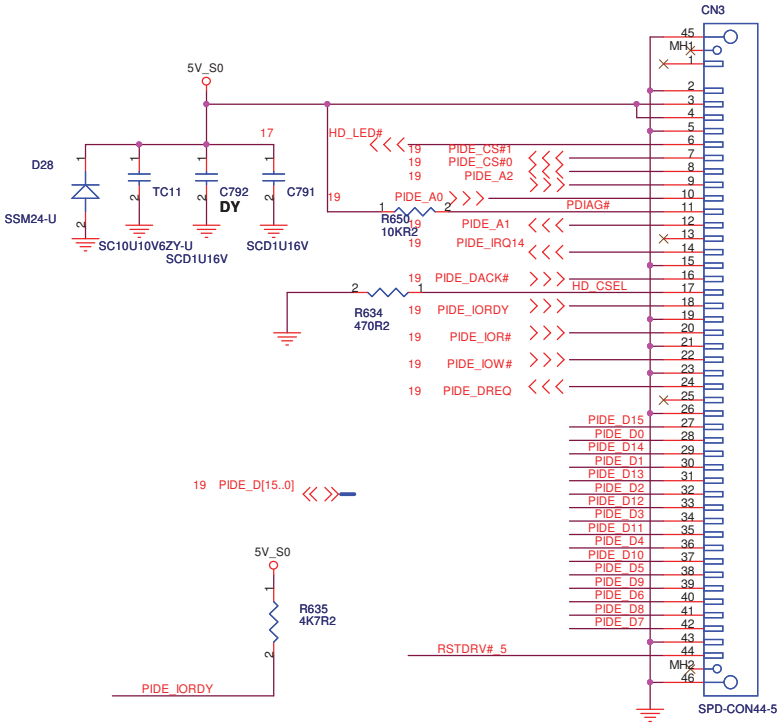
Date: Friday, March 25, 2005 | Sheet 23 of 51

USB PORT



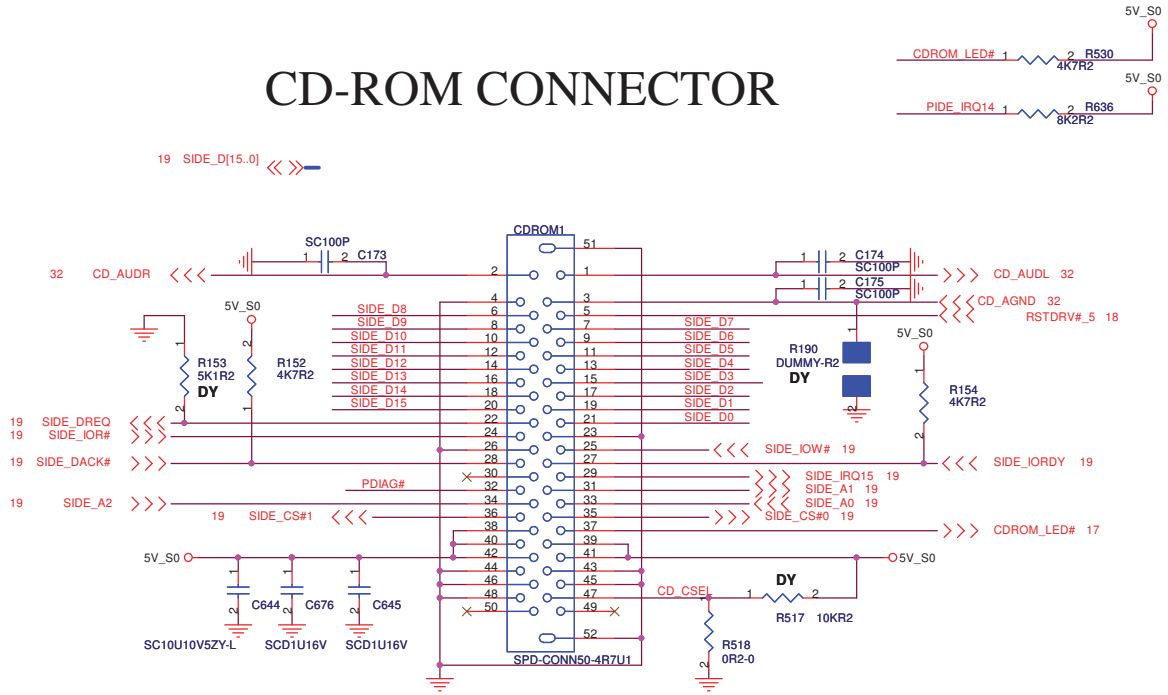
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: USB and MDC I/F		
Size: A3	Document Number: W37	Rev: SB
Date: Friday, March 25, 2005	Sheet 24 of 51	

HD Connector

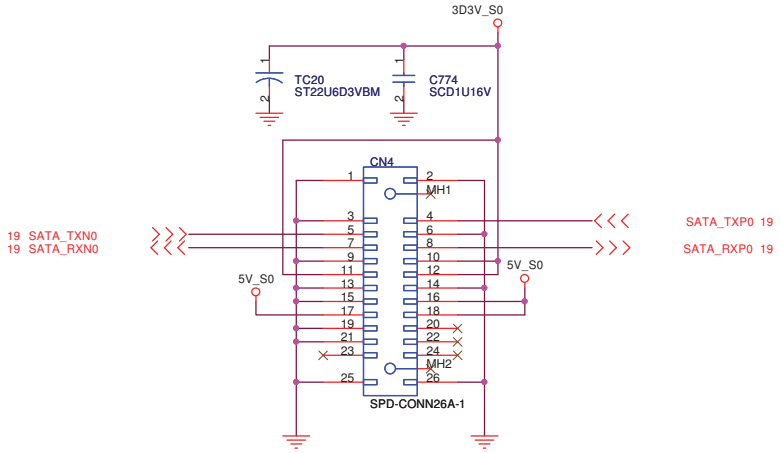


Connector change

CD-ROM CONNECTOR

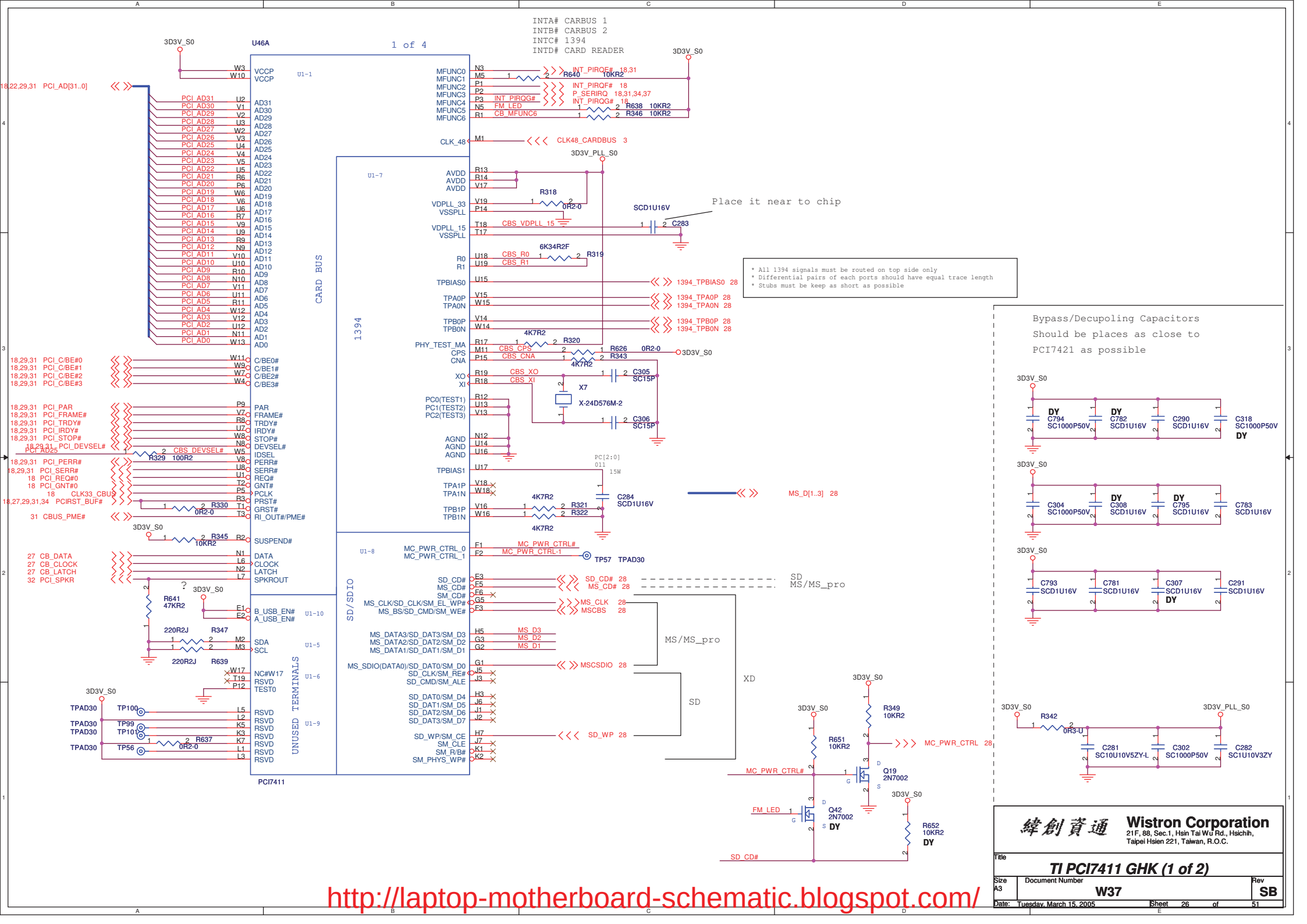


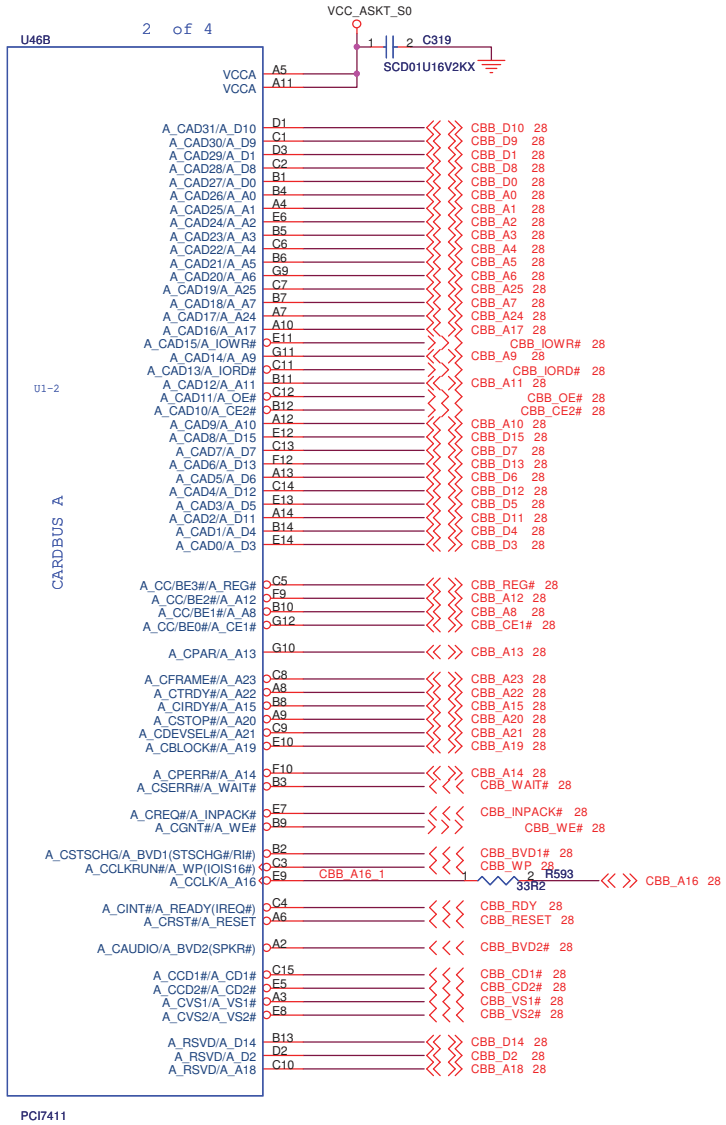
SATA HD Connector

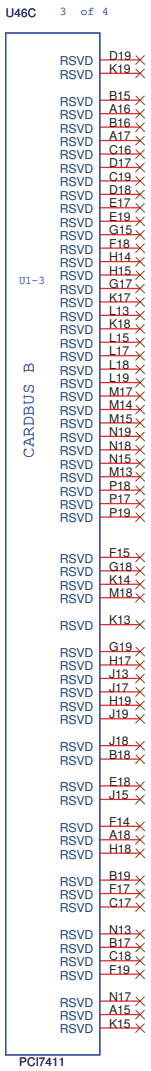


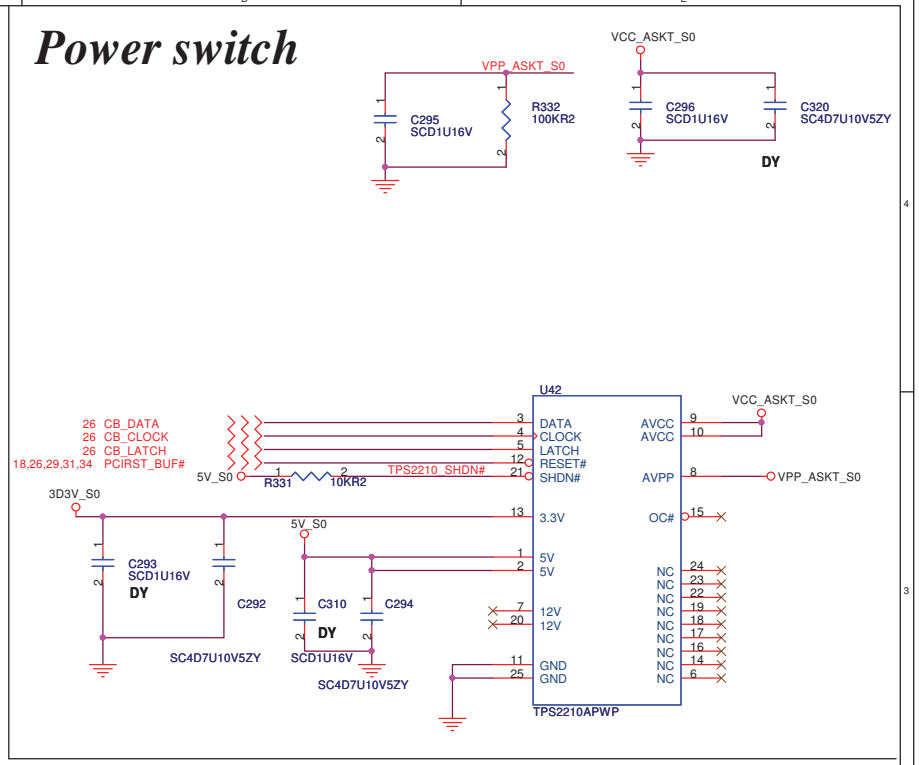
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

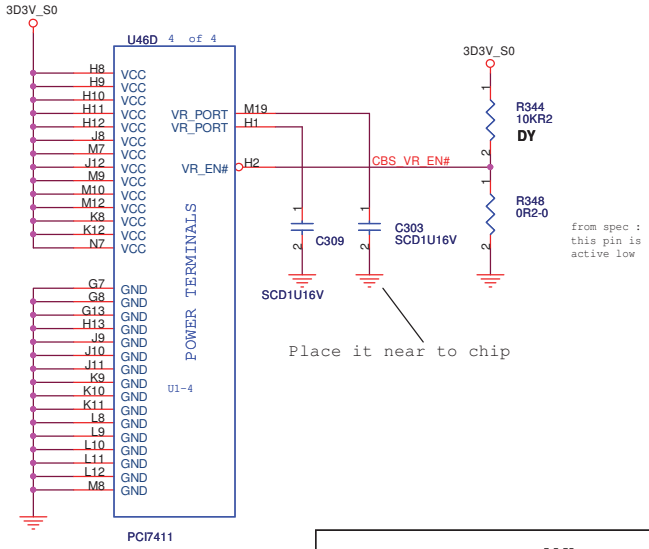
Title	**HD/CDROM**	
Size A3	Document Number **W37**	Rev SB
Date: Wednesday, March 23, 2005	Sheet 25 of 51	







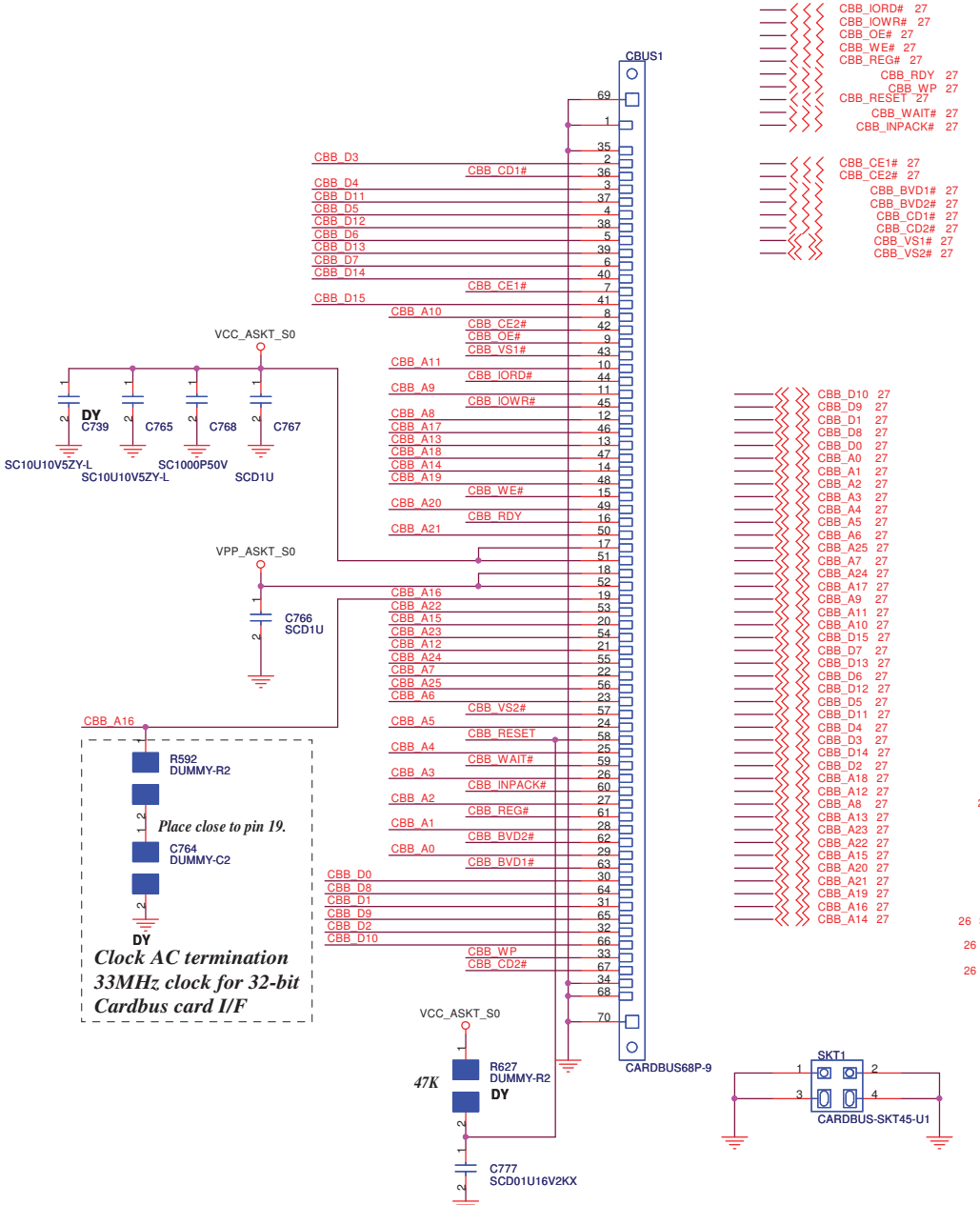




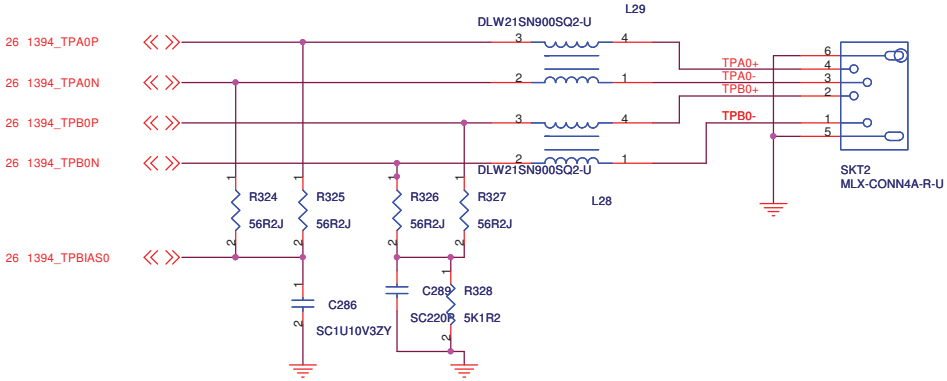
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*TI PCI7411 GHK (2 of 2)*	
Size A3	Document Number **W37**	Rev **SB**
Date: Tuesday, March 15, 2005	Sheet 27 of 51	

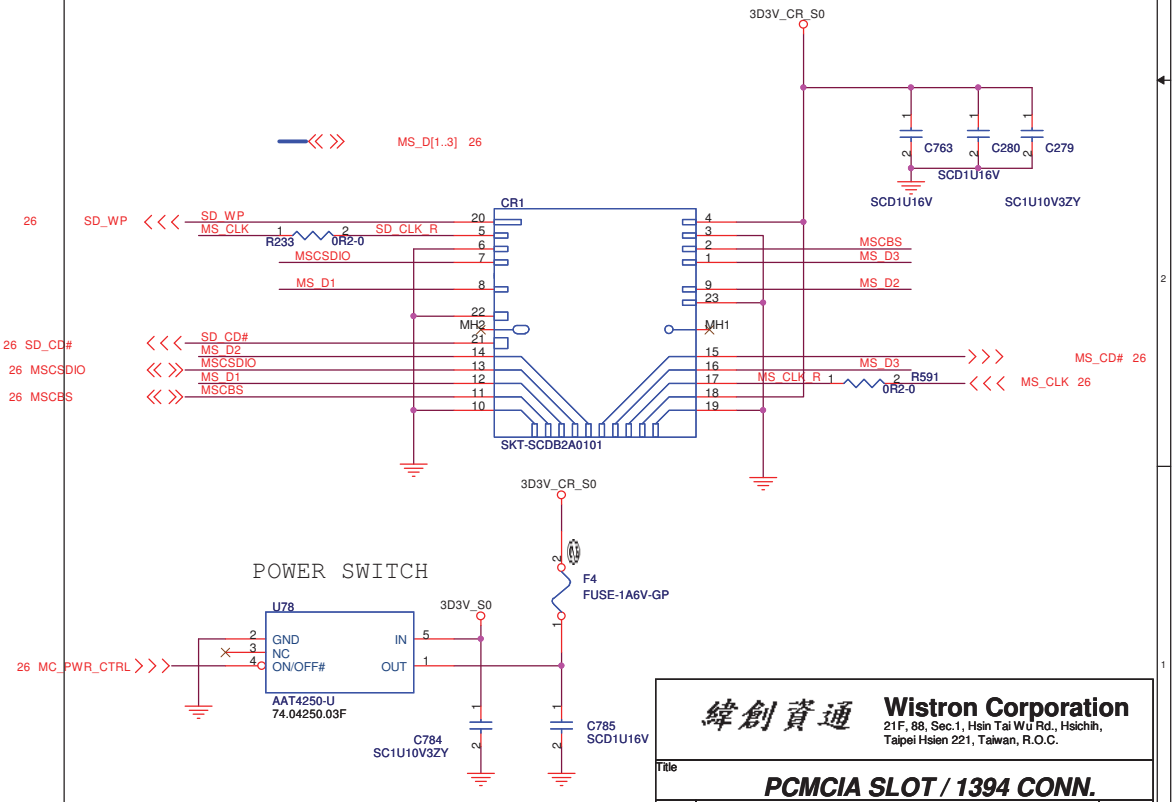
PCMCIA Socket

Cardbus I/F



1394 Connector





緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA SLOT / 1394 CONN.**

Size	Document Number	Rev
A3	W37	SB

Date: Wednesday, March 23, 2005 Sheet 28 of 51

Close to Pin121,Pin122

LAN_X1
LAN_X2
R237
DY
DUMMY-R2
X2
XTAL-25MHZ-35
C222
SC27P50V2JN
C223
SC27P50V2JN

PCI_C/BE#3 18,26,31
PCI_C/BE#2 18,26,31
PCI_C/BE#1 18,26,31
PCI_C/BE#0 18,26,31
PCI_AD[31..0] 18,22,26,31

R381 value should be 5.6K at RTL8100CL application, and 2.49K at RTL8110SBL application.

3K6R3 R557
3D3V_LAN_S5
U77
EECS_3
EESK
EEDI
EEDO
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
C224
SCD1U16V
DY
10KR2
R571
3D3V_LAN_S5

R380 is used only at RTL8110S(B) application and only at 93C56 is used.

3D3V_S5
L16
BLM11A601S
3D3V_LAN_S5
D3.3V
C236
SC10U10V5ZY
C247
C246
C713
C268
C285
C288
C269
SCD1U16V

CLOSE TO LAN CHIP

MDI0+
MDI0-
MDI1+
MDI1-
R234
R235
R98
R99
49D9R2F
C221
SCD01U16V2KX
C131
SCD01U16V2KX

R236
5K6R3F
3D3V_LAN_S5
LAN_RTSET
LAN_X2
LAN_X1
ACTIVE_LED#
100M_LED#
10M_LED#
EESK
EEDI
EEDO
EECS_3
PCI_AD0
PCI_AD1

U36
VSS
RSET
AVDDH18
CTRL18
VSS
VSS
XTAL2
XTAL1
AVDDH
VSSPST
GND
LED0
VDD18
LED1
LED2
LED3
GND
EESK
VDD18
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1

CTRL25
Q17
BCP69T1-U
R285
0R5J-1
D2.5V
DVDD
C264
SCD1U16V3KX
C266
SC22U10V6ZY-U
DY
C239
C287
C225
C265
C267
C270
DY
C248
DY
C226
DY
C238
SCD1U16V

DVDD
AVDDL
AVDD25
ISOLATE
LAN_INTA#
PME#_LAN
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28

MDI0+
MDI0-
AVDDL
VSS
MDI1+
MDI1-
AVDDL
CTRL25
VSS
AVDDH
HSDAC+
HSDAC-
VSS
MDI2+
MDI2-
AVDDL
VSS
MDI3+
MDI3-
AVDDL
VSSPST
GND
ISOLATE#
VDD18
INTA#
VDD33
PCIRST#
PCICLK
GNT#
REQ#
PME#
VDD18
PCIAD31
PCIAD30
GND
PCIAD29
PCIAD28
VSSPST

30 MDI0+
30 MDI0-
30 MDI1+
30 MDI1-
INT_PIRQH#
18,26,27,31,34 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
0R2-0 R287
3D3V_LAN_S5

PCIAD2
VSSPST
GND
VDD18
PCIAD3
PCIAD4
PCIAD5
PCIAD6
VDD33
PCIAD7
CBEB0
VSSPST
PCIAD8
PCIAD9
M66EN
PCIAD10
PCIAD11
PCIAD12
VDD33
PCIAD13
PCIAD14
VSSPST
GND
PCIAD15
VDD18
CBEB1
PAR
SERR#
NC
GND
NC
VDD33
PERR#
STOP#
DEVSEL#
TRDY#
VSSPST
CLKRUN#

PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_C/BE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_C/BE#1
PCI_PAR 18,26,31
PCI_SERR# 18,26,31
PCI_PERR# 18,26,31
PCI_STOP# 18,26,31
PCI_DEVSEL# 18,26,31
PCI_TRDY# 18,26,31
PM_CLKRUN# 18,34

RTL8100CL-U

PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
VDD18
IDSEL
PCIAD23
GND
PCIAD22
PCIAD21
VSSPST
GND
PCIAD20
VDD18
PCIAD19
VDD33
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
GND
IRDY#
VDD18

PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_C/BE#3
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
DVDD
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_C/BE#2
PCI_FRAME#
PCI_IRDY#

3D3V_S0
R258
1KR2F
ISOLATE
R257
15KR2
3D3V_LAN_S5
Q18
DTC124EUA-U1
DY
21,34 PME#_SB
0R2-0 R286
PME# LAN

3D3V_LAN_S5
R323
100R2
PCI_AD23
PCI_IRDY# 18,26,31
PCI_FRAME# 18,26,31

ACTIVE_LED# 30
10M_LED# 10M_LED# 30
100M_LED# 100M_LED# 30

DVDD
AVDD25
R256
0R0805-PAD
A2.5V
C240
SCD1U16V
C243
SCD1U16V

3D3V_LAN_S5
BLM11A601S
L14
AVDDL
A3.3V
C237
C220
C242
C244
C245
DY
C241
SC10U6D3V5MX
SCD1U16V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8100CL
Size: A3
Document Number: W37
Rev: SB
Date: Friday, April 15, 2005
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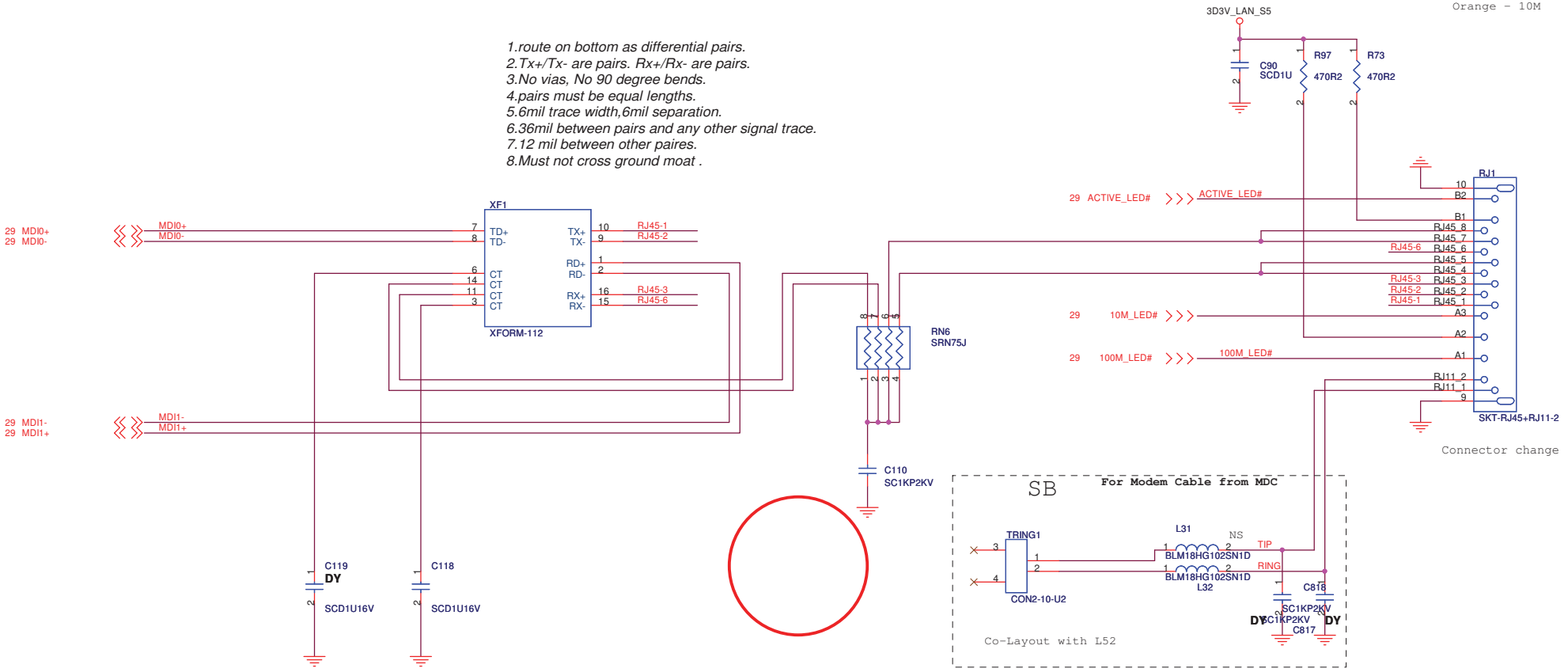
LAN Connector

10/100
Green - 100M
Yellow - Active
Orange - 10M

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,6mil separation.
6.36mil between pairs and any other signal trace.
7.12 mil between other paires.
8.Must not cross ground moat .



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

緯創資通 **Wistron Corporation**
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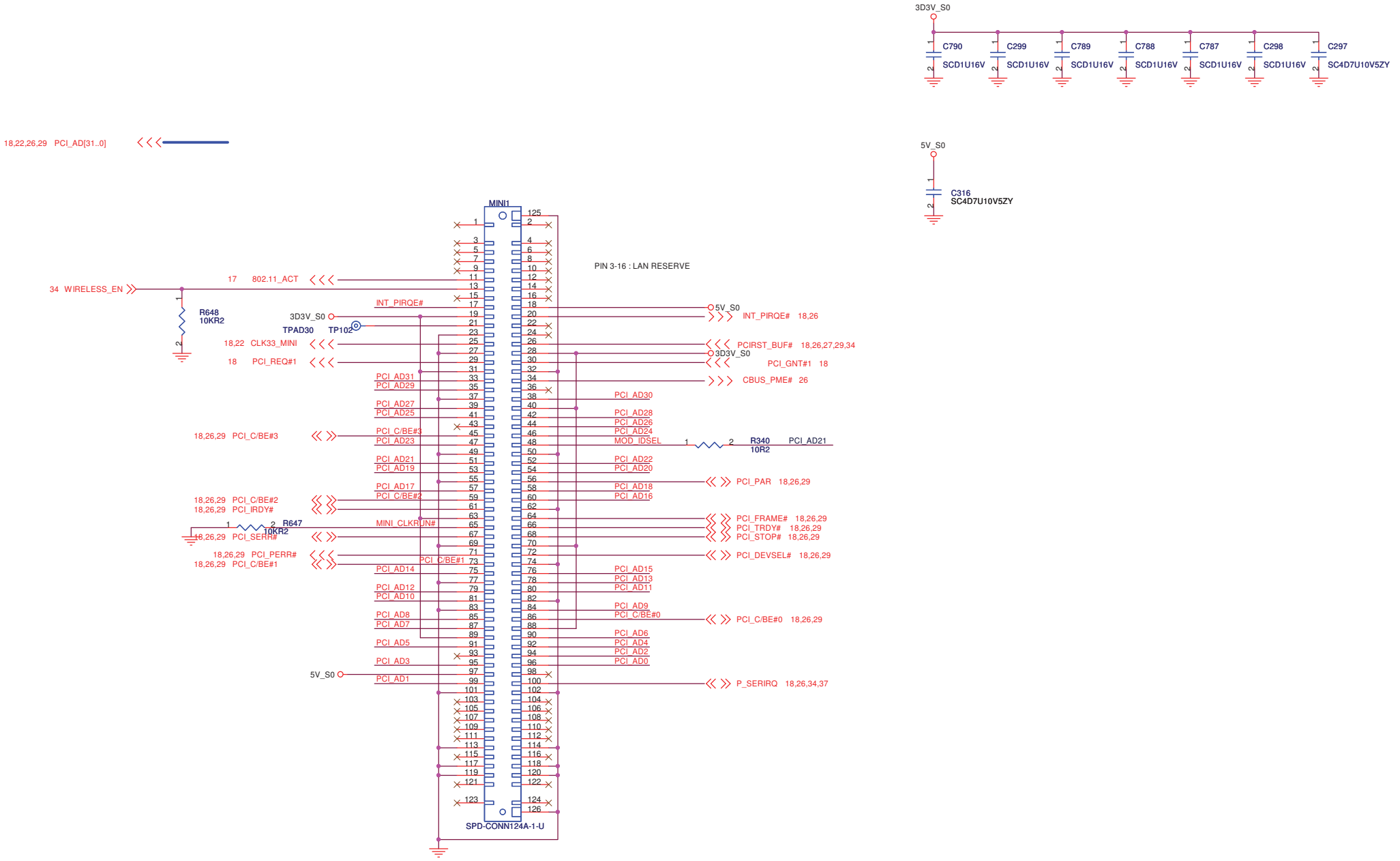
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN Connector		
Size A3	Document Number W37	Rev SB
Date: Monday, April 18, 2005	Sheet 30 of 51	

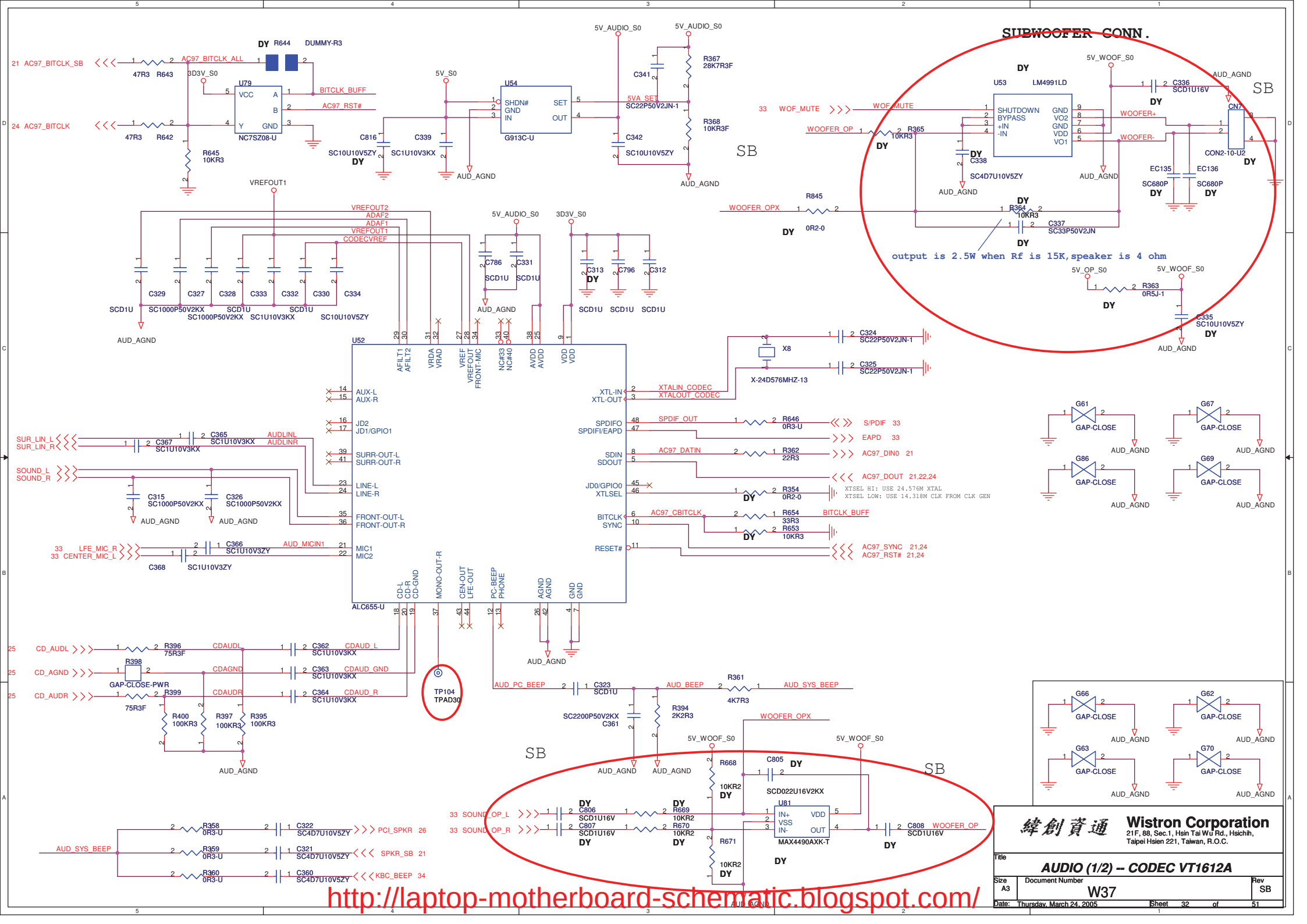


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI-PCI

Size: A3 | Document Number: W37 | Rev: SB

Date: Tuesday, March 15, 2005 | Sheet 31 of 51


SUBWOOFER CONN.
output is 2.5W when Rf is 15K, speaker is 4 ohm
ALC655-U
U52
U53 LM4991LD
U54 G913C-U
U79 NC7SZ08-U
U81 MAX4490AXK-T
X-24D576MHZ-13
AUD_AGND
SB
DY
GAP-CLOSE
TP104 TPAD30
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (1/2) -- CODEC VT1612A
Size A3
Document Number W37
Rev SB
Date: Thursday, March 24, 2005
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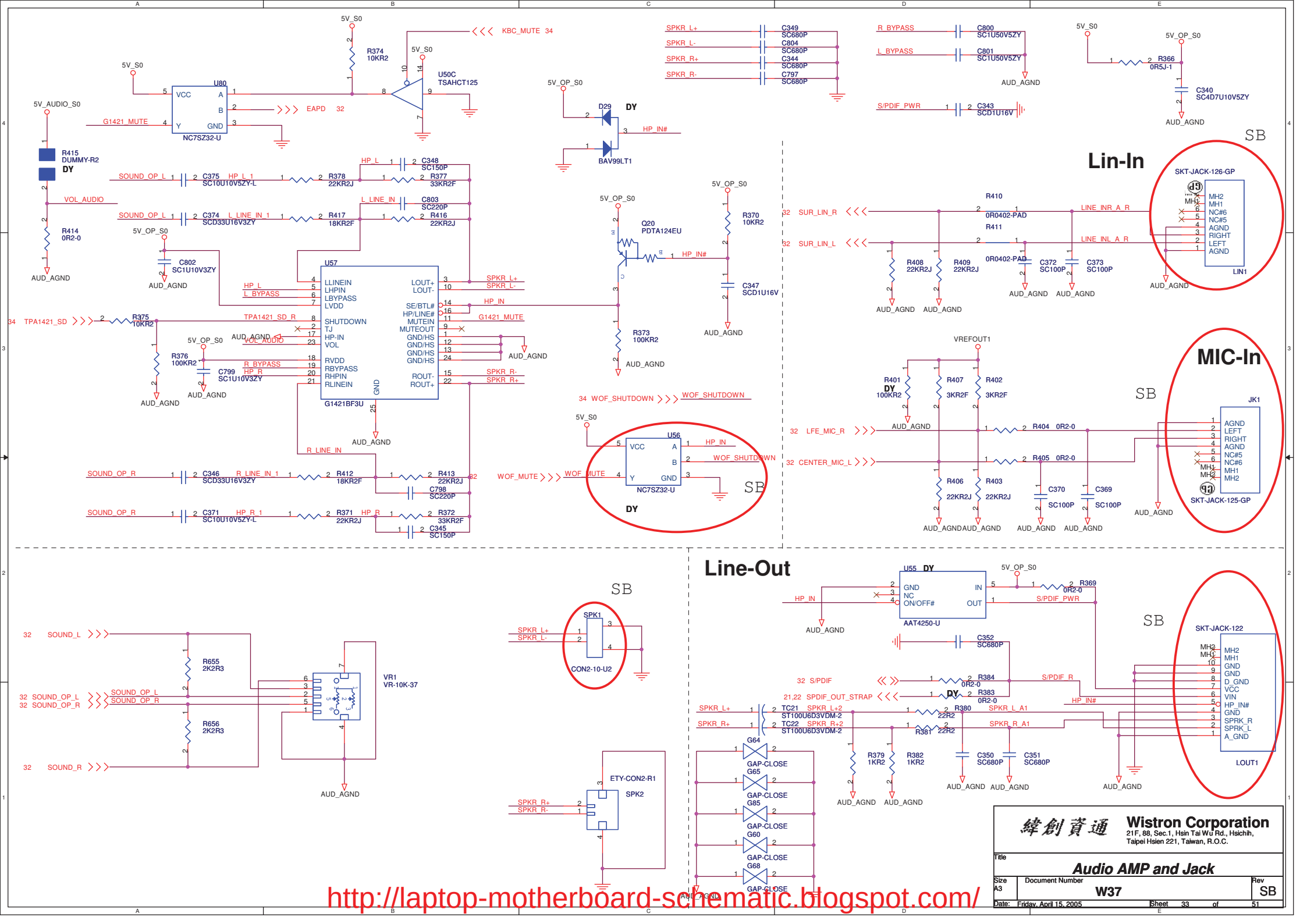
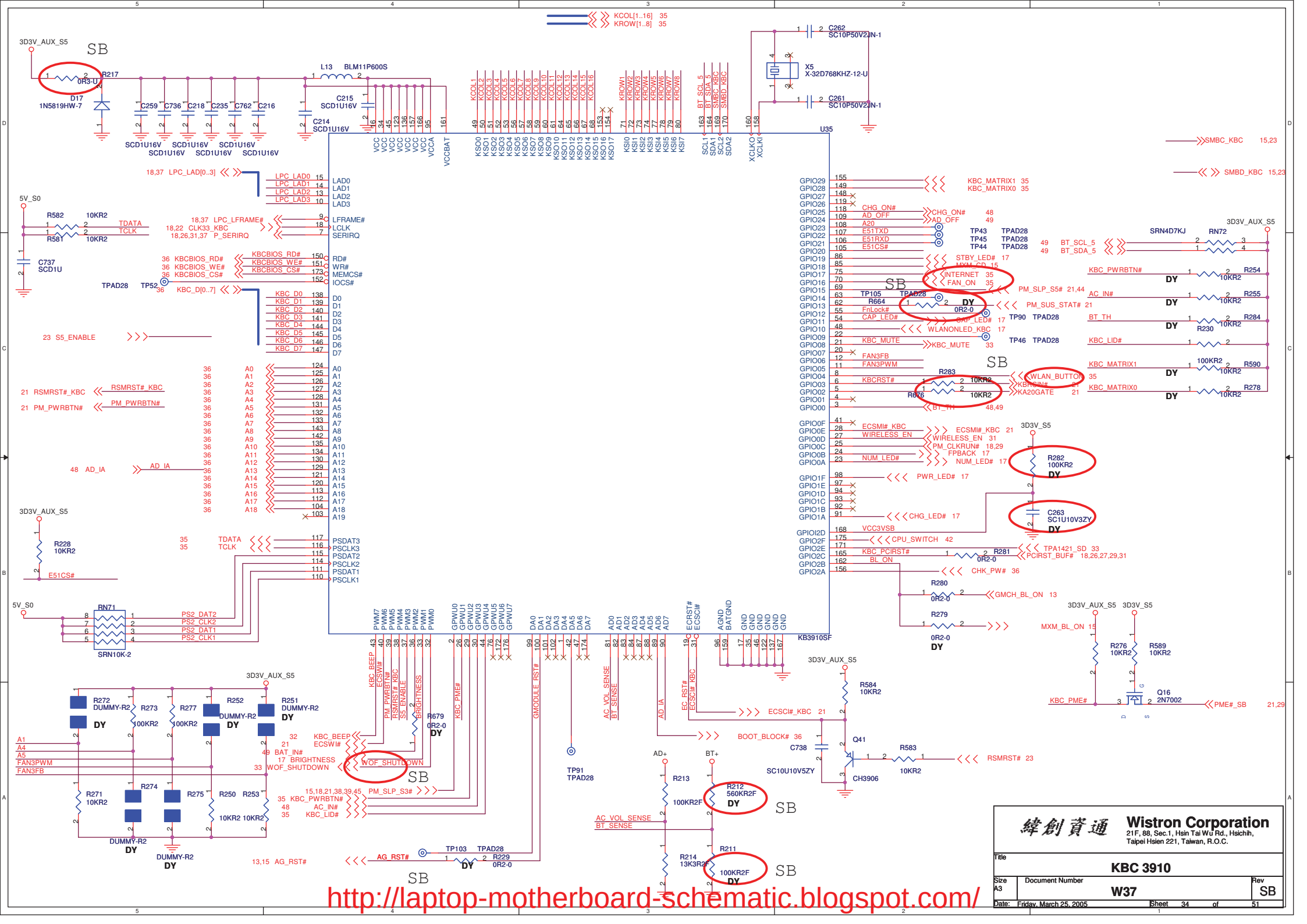
http://laptop-motherboard-schematic.blogspot.com/



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Audio AMP and Jack**	
Size A3	Document Number **W37**	Rev SB
Date: Friday, April 15, 2005	Sheet 33 of 51	


KB3910SF
U35
SB
DY
3D3V_AUX_S5
5V_S0
3D3V_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC 3910
Size A3
Document Number
W37
Rev SB
Date: Friday, March 25, 2005
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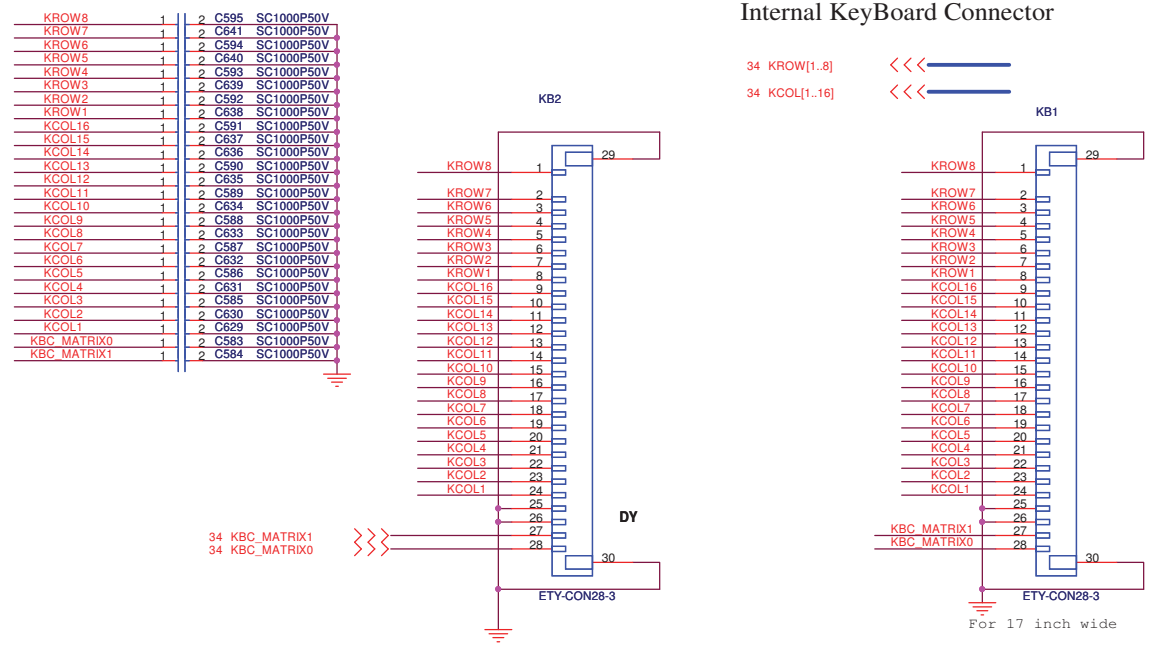
Keyboard matrix (from vendor)

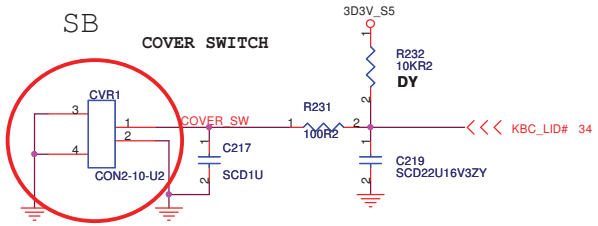
	US	Eur	Jap	Ohter
MATRIXID1#	1	0	1	0
MATRIXID2#	1	1	0	0

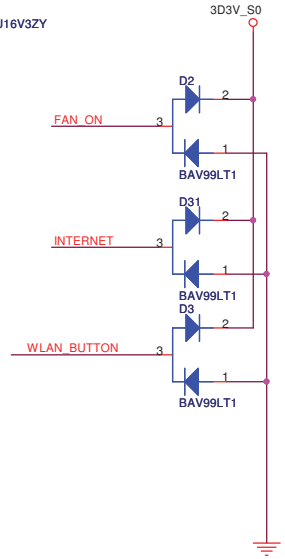
Internal KeyBoard Connector

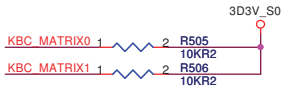


SB

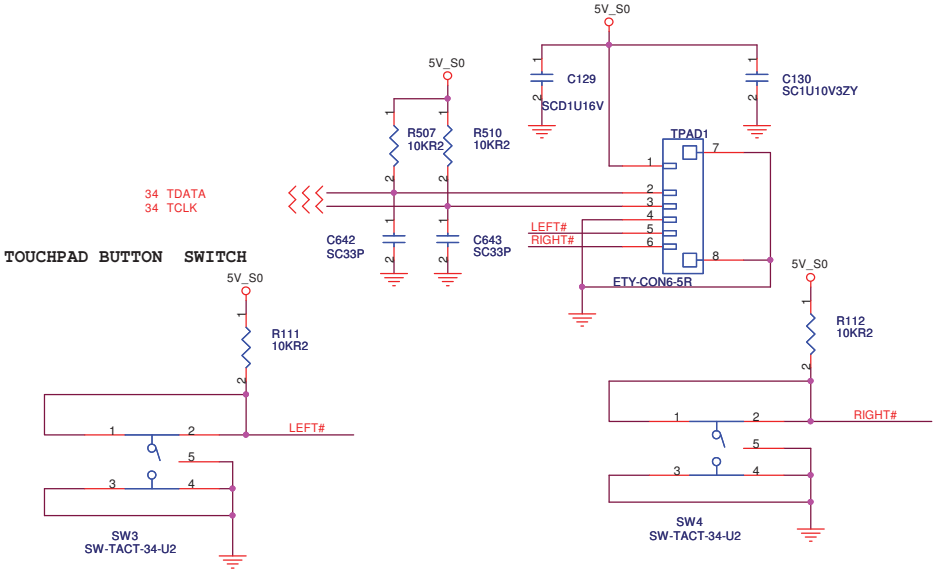
COVER SWITCH



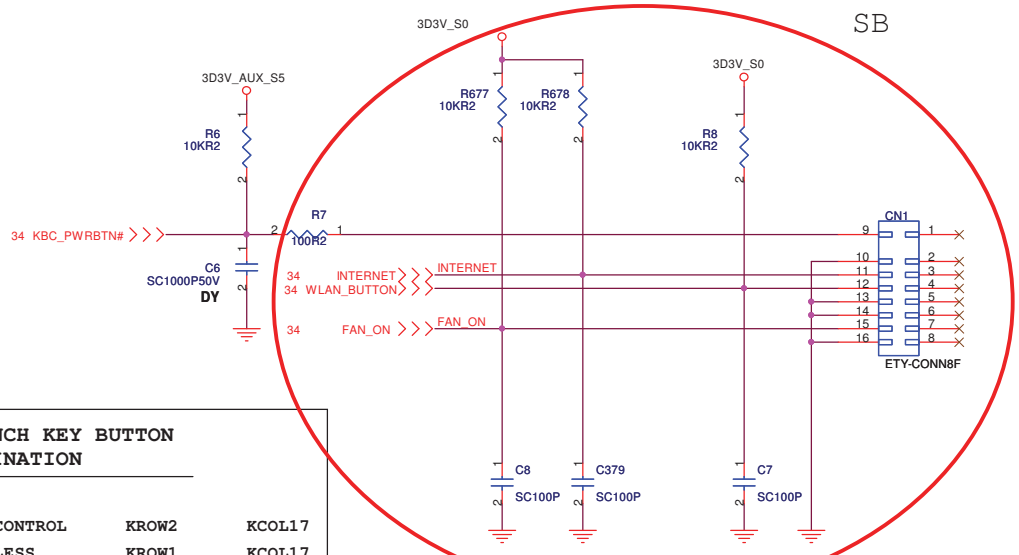




TouchPad Connector



SB



LAUNCH KEY BUTTON DEFINATION

FAN_CONTROL	KROW2	KCOL17
WIRELESS	KROW1	KCOL17

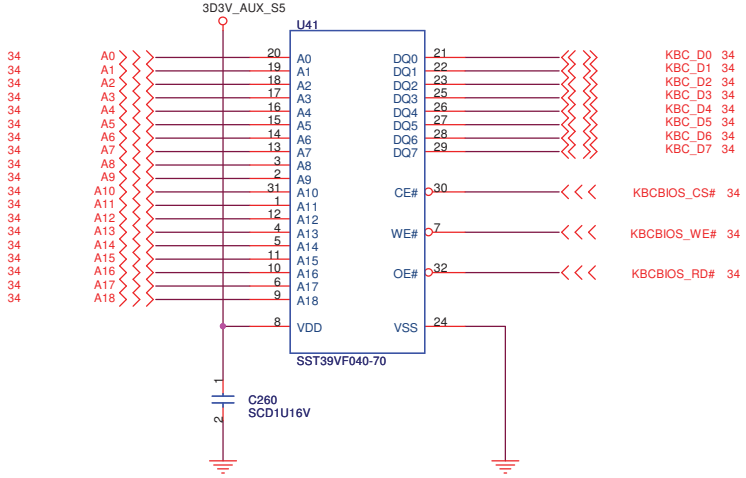
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAUNCH / TOUCHPAD / KB CONN***

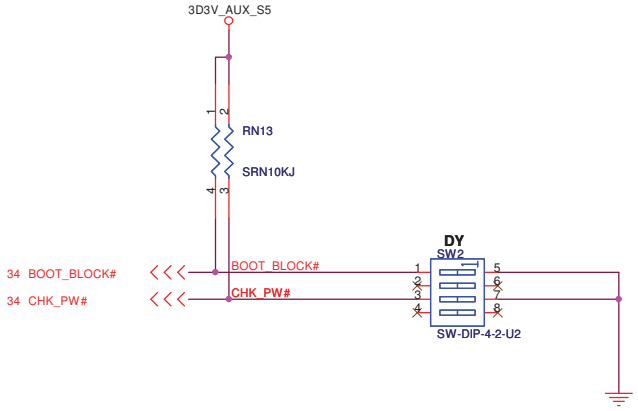
Size	Document Number	Rev
A3	W37	SB

Date: Wednesday, April 06, 2005 Sheet 35 of 51

KBC_D[0..7] 34



ROM SIZE MAX. 512KBYTE



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BIOS ROM		
Size: A3	Document Number: W37	Rev: SB
Date: Tuesday, March 15, 2005	Sheet 36 of 51	

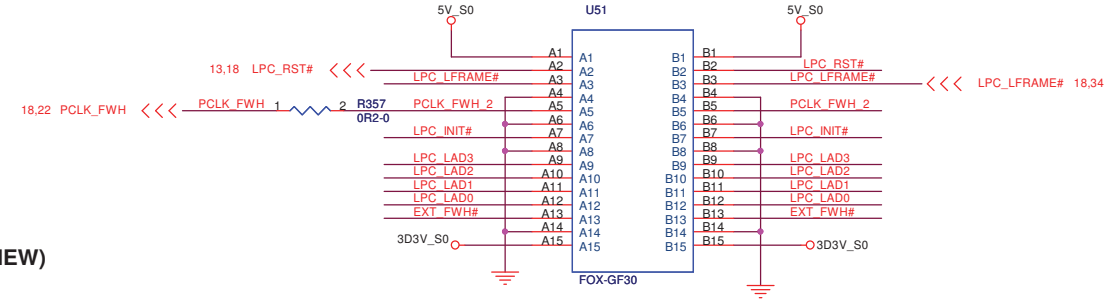
LPC_LAD[0..3] 18,34

GOLDEN FINGER FOR DEBUG BOARD

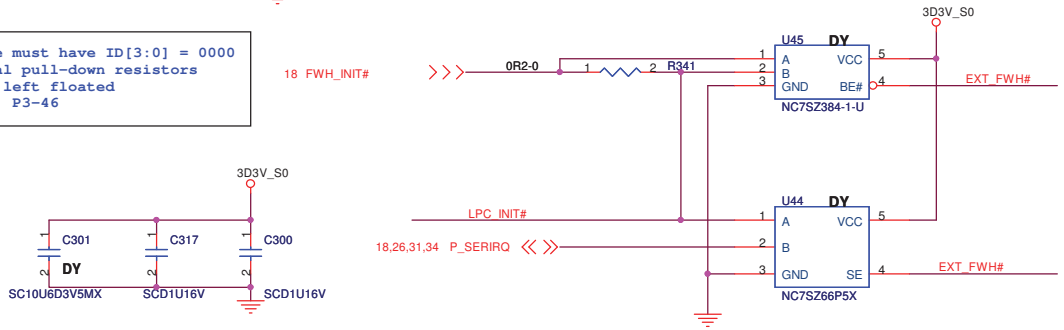
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



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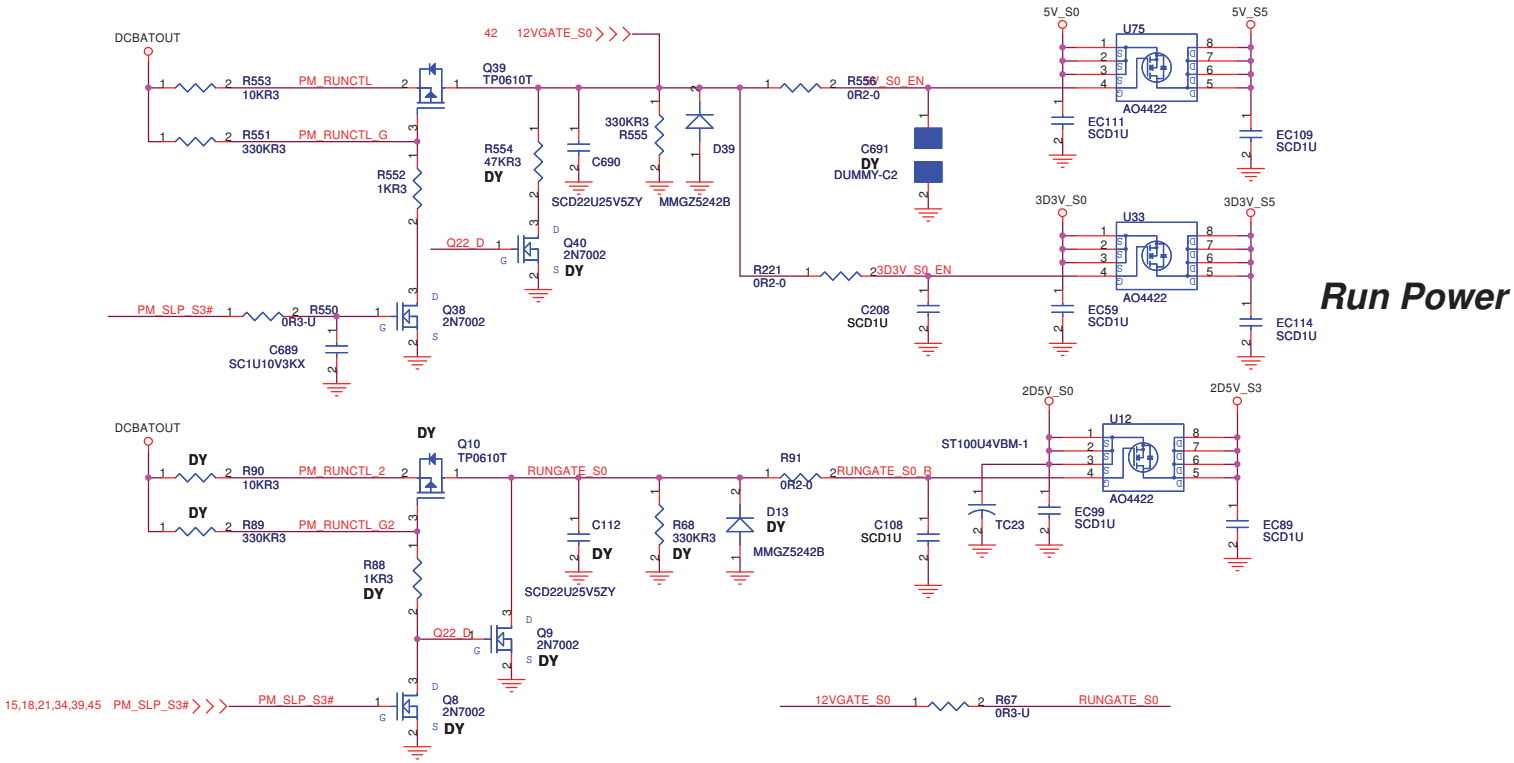
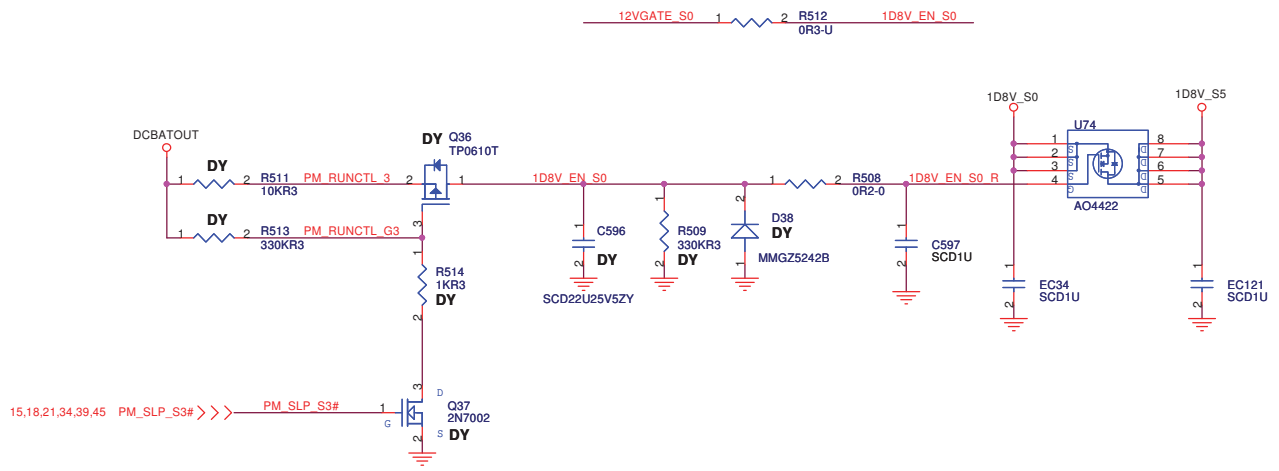
Taipei Hsien 221, Taiwan, R.O.C.

Title	Debug (Gold Finger)	
Size A3	Document Number W37	Rev SB
Date: Tuesday, March 15, 2005	Sheet 37 of 51	

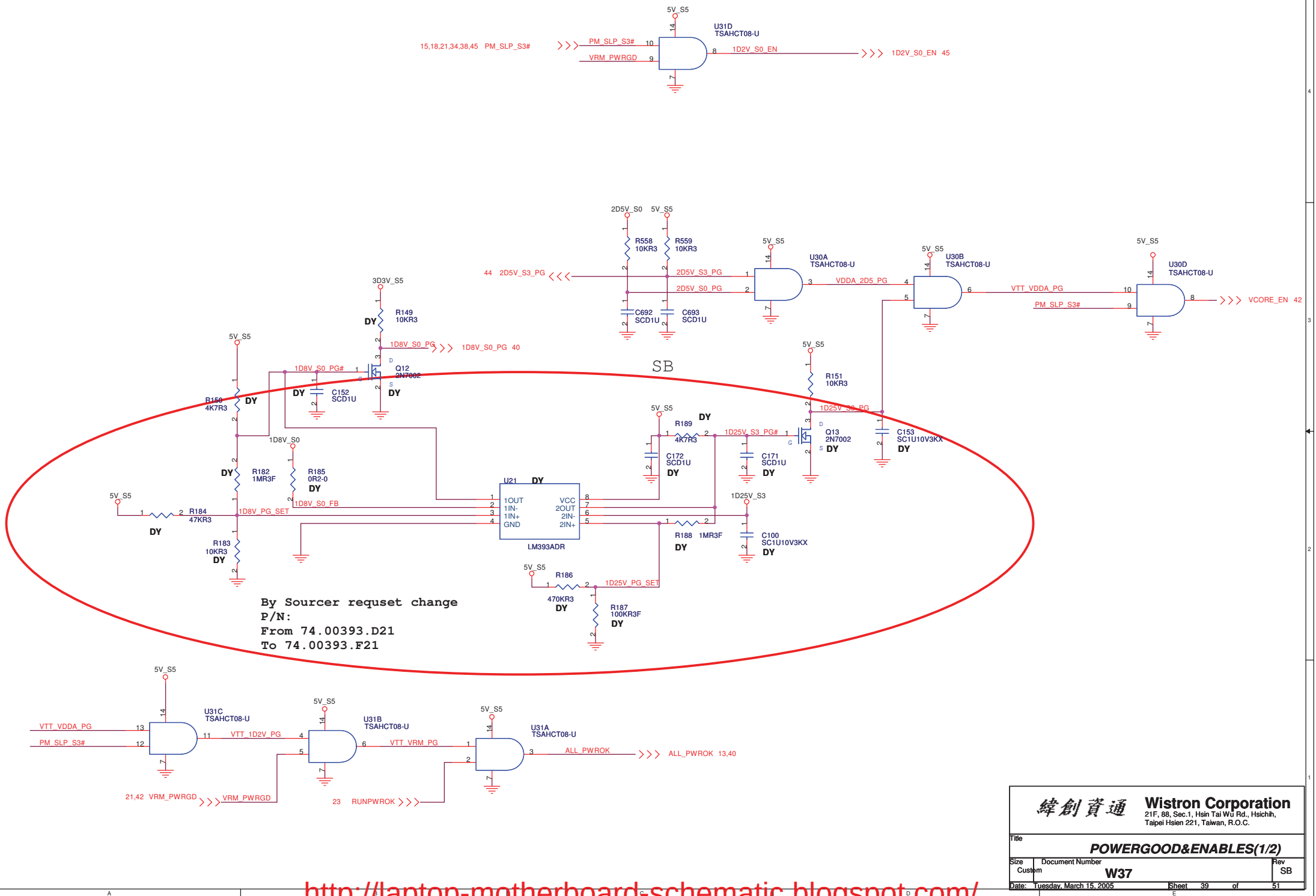


Run Power



Power On Logic

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWR CTL LOGIC / PWR PLANE***
Size A3	Document Number W37 Rev SB
Date: Friday, March 25, 2005	Sheet 38 of 51



緯創資通 **Wistron Corporation**
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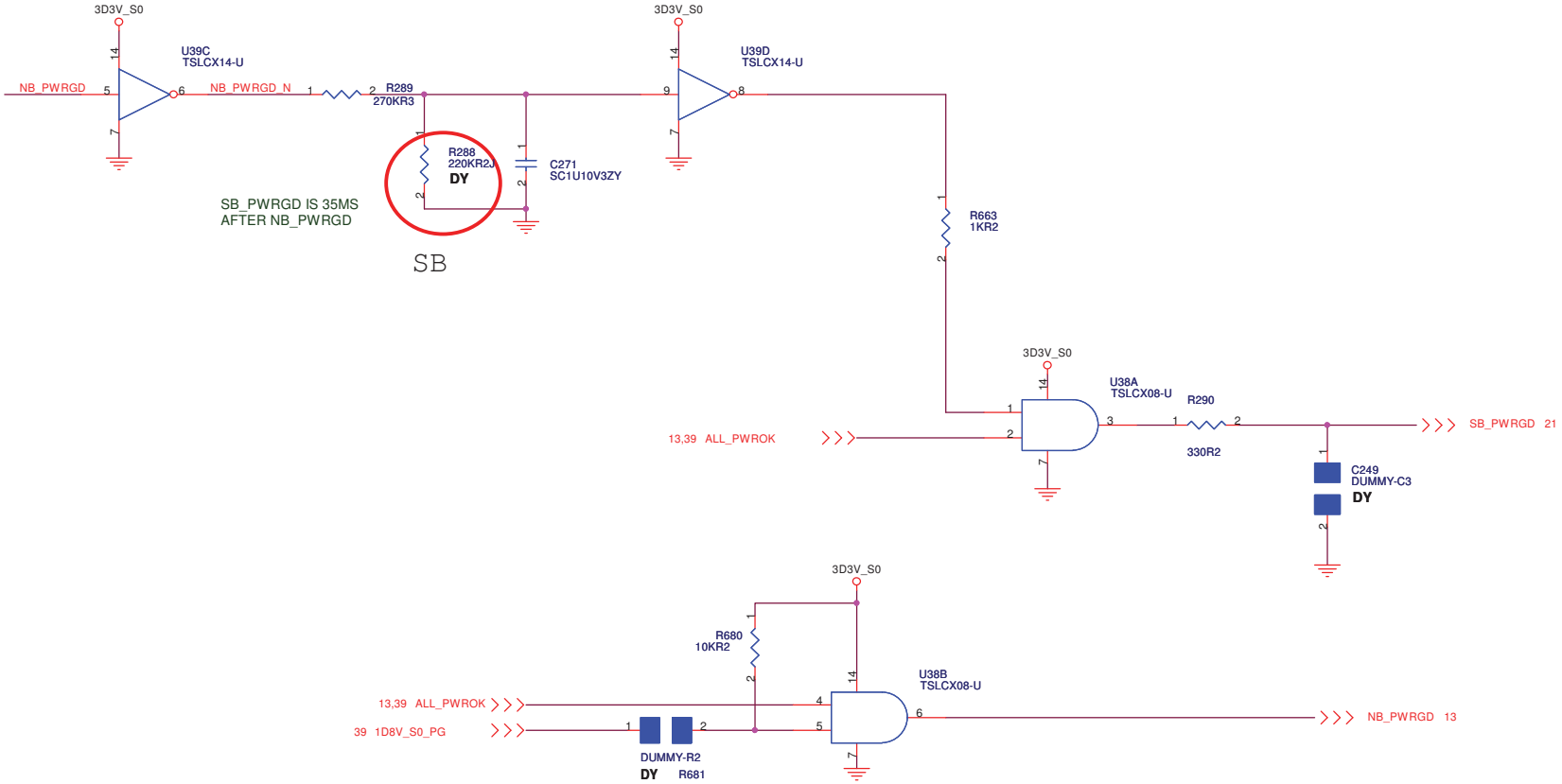
Title: ***POWERGOOD&ENABLES(1/2)***

Size	Document Number	Rev
Custom	W37	SB

Date: Tuesday, March 15, 2005 Sheet 39 of 51

RS480M POWER GOOD CIRCUIT



Title	POWERGOOD&ENABLES(2/2)	
Size A3	Document Number W37	Rev SB
Date: Tuesday, March 15, 2005	Sheet 40 of 51	

CPU_CORE
Intersil 6559CR + ISL6207CB*2 (Dummy *1)

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Output Signal
PGOOD(OD / 3.3V) → VRM_PG

Output Power
VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=43A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

5V_AUX_S5

DCBATOUT → INPUT
OUT → 5V_AUX_S5

LP2951ACM

1D25V_S3

2D5V_S3 → VIN
5V_S5 → VCNTL
APL5331_1D25V_VREF → VREF
VOUT → 1D25V_S3

APL5331KAC

TI TPS5130
1D2V/3D3V/5V

1D2V_S0_EN
S5PWR_ENABLE
S5PWR_ENABLE

Input Signal
SS_STBY1(I / 5V) FOR 1.2V
SS_STBY2(I / 5V) FOR 3.3V
SS_STBY3(I / 5V) FOR 5.0V

GND ← STBY_LDO(I / 5V)

DCBATOUT_5130
DCBATOUT_5130

STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)

Output Signal
PGOUT(OD / 5V) → Pull High (5V)

Output Power
5V(O) → 5V (5.4A)
1D2V(O) → 1D2V (5A)
3D3V(O) → 3D3V 4A)
LDO(O) → ✕

DCBATOUT
5V_S5
5V_AUX_S5
5V_S0

Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT

ISL6227CA
1D8V/2D5V

S5PWR_ENABLE
PM_SLP_S5#

Input Signal
EN1 (I / 3.3V)
EN2 (I / 3.3V)

Output Signal
PG1(OD / 1D8V) → 1D8_S5_PG
PG2(OD /2D5V) → 2D5_S3_PG

Input Power
DCBATOUT
V+
5V_S5
VCC (I / 5V)

Output Power
2D5V(O) → 2D5V_S3 (6.4A)
1D8V(O) → 1D8V_S5 (5A)

Charger_Max1909

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V) → AD_IN
XTAL2/PB4 (O/5V) → CHARGE_LED#
XTAL1/PB3 (O/5V) → BL2#

Output Power
VCC (O) → DCBATOUT
VCC (O) → BT+

AD+

Input Power
DCIN (I)

Adapter

AD_OFF

Input Signal
(I)

Output Signal
(O) → AD_IN

AD_JK
5V_AUX_S5

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

緯創資通 Wistron Corporation
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Title: **Power Block Diagram**
Size: A3 | Document Number: W37 | Rev: SB
Date: Monday, March 14, 2005 | Sheet 41 of 51

Vdrop is over spec
under max loading

SB

CPU_SWITCH : (KBC GPIO14)
H: 35W CPU
L: 62W CPU

Gain value large,
then bandwidth large!
=> 2.74K or 3.65K

Rt=10^[11.09-1.13log(fs)]
Rt=107K,=>fs=230KHz
But real freq.=270KHz

Main Source:
KEMET 2D5V/ 330uF / ESR=9mohm / Iripple=3.7A / ST330U2D5VDM-3
80.3371V.191/ 7.3*4.3*1.9 / NT$:9.0
2'nd Source:
Panasonic 2V/ 330uF / ESR=9mohm / Iripple=3.0A/ SE330U2VDM-2
79.33719.20A/ 7.3*4.3*1.9 / NT$:9.5

Panasonic 25V / E1 Cap.
8.5*6.5mm / SMD
ESR=0.26ohm, Iripple=0.3A
FX Serial

Follow MOSFET rise time spec.
=> Mount 0ohm first.

DCR=1.3mohm+-10% / Imax=40A /
Panasonic /
ETQP2H0R7BF / 0.48uH /
13.4*13.3*4.9

D-PAK
Id=51A
Qg=13~17nC
Rdson=9~13mohm
USD$:0.16

D-PAK
Id=35A
Qg=24~32nC
Rdson=5.7~6.8mohm
USD$:0.23

Place close to ISL6559
Iocset=90uA ; Iocp=1.5*I(full)
90uA/1.5=60uA----> respect to Full load
If full load is 44A
60uA*Rsen=(44A/2)*(6.8m/2)*1.3
Rsen~ 1.62K

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Title: CPU Vcore Power_1
Size: A3 | Document Number: W37 | Rev: SB
Date: Friday, April 15, 2005 | Sheet 42 of 51

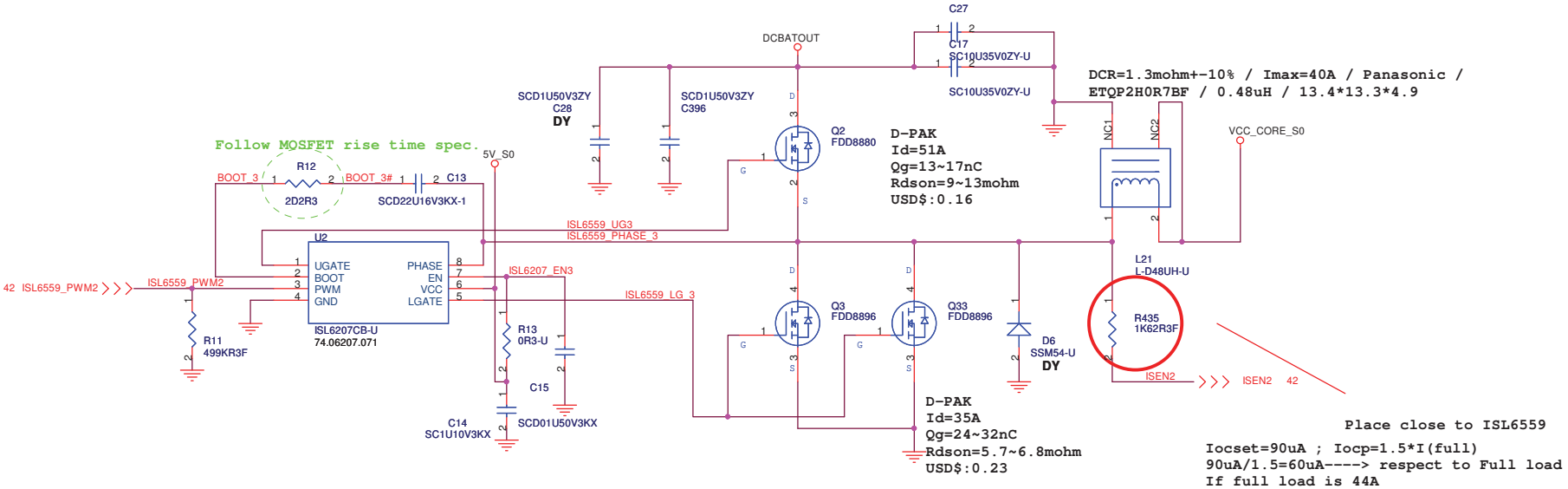

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

緯創資通 Wistron Corporation
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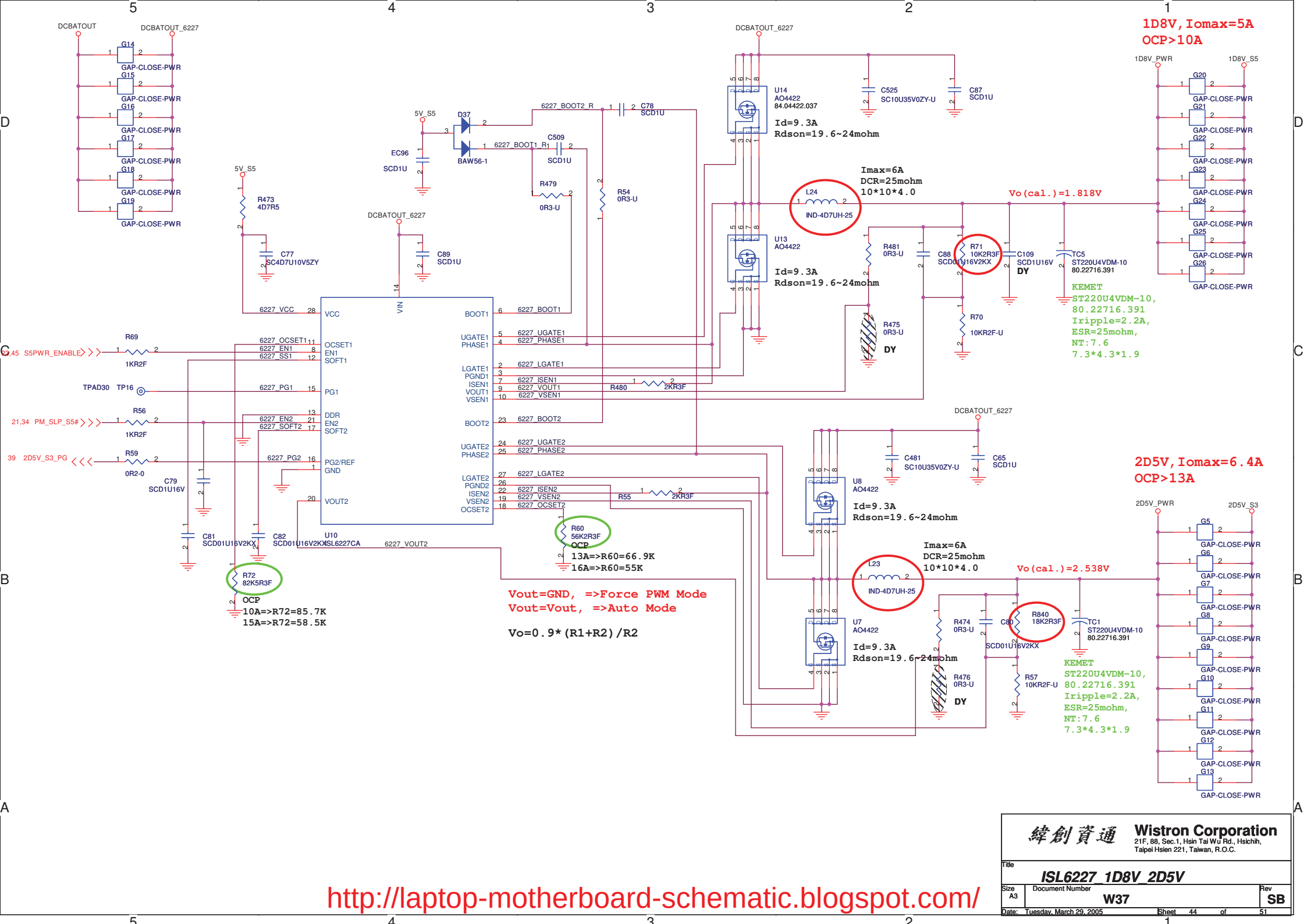
Title: CPU Vcore Power_2
Size: A3
Document Number: W37
Rev: SB
Date: Tuesday, March 29, 2005
Sheet 43 of 51



Wistron Corporation	緯創資通
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Title: ISL6227_1D8V_2D5V	
Size: A3	Document Number: W37
Rev: SB	
Date: Tuesday, March 29, 2005	Sheet 44 of 51

TI TPS5130 for 1D2V, 3D3V, 5V

(1D2V=>CH1 , 3D3V=>CH2 , 5V =>CH3)

For 3.3V
SETTING=3.349V

For 5V
SETTING=5.0915V

For 1.2V
SETTING=1.217V

Vo=(R1*0.85)/R2+0.85

T(soft)=1.736ms

close to IC

SB

1D2V_OCP
3D3V_OCP
5V_OCP

OCP
12A=>R199=18K
18A=>R199=28K

OCP
8.4A=>R200=13K
10A=>R200=22K

OCP
8.4A=>R195=12.65K
10A=>R195=22K

LDO SETTING

TPS5130

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

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Taipei Hsien 221, Taiwan, R.O.C.

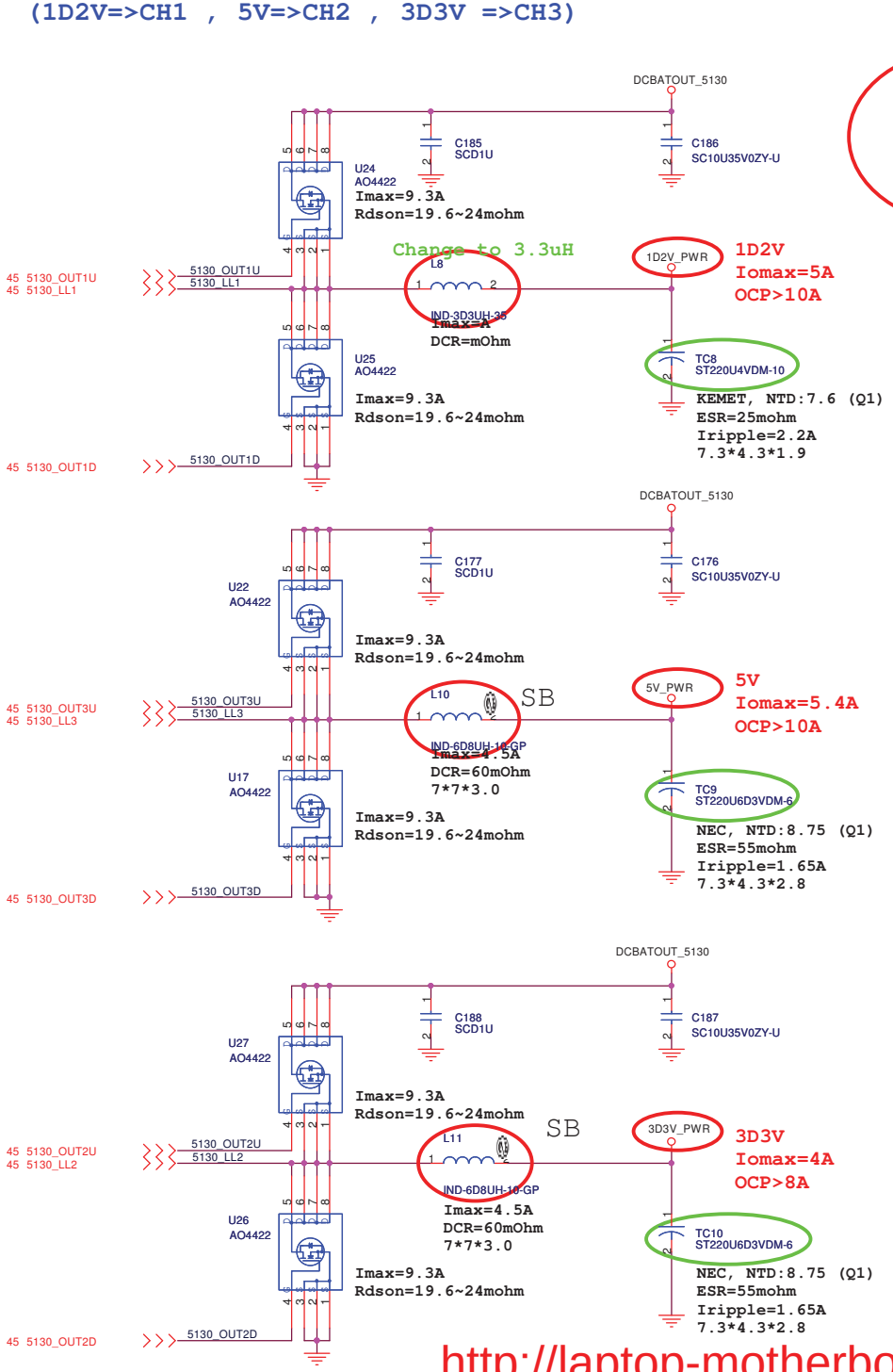
Title: TI TPS5130 1D2V/3D3V/5V (1/2)

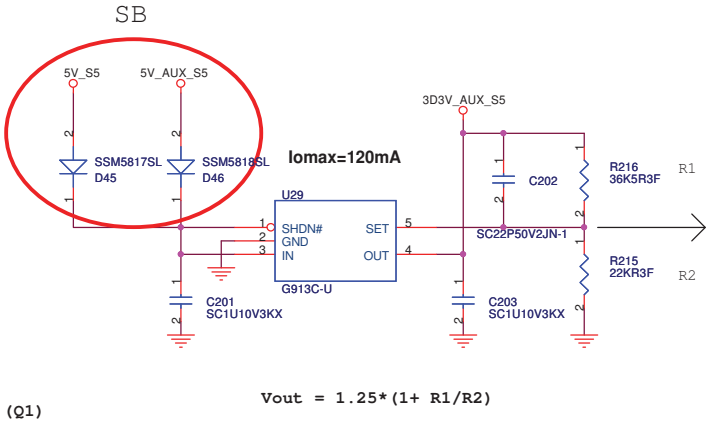
Size: A3 | Document Number: W37 | Rev: SB

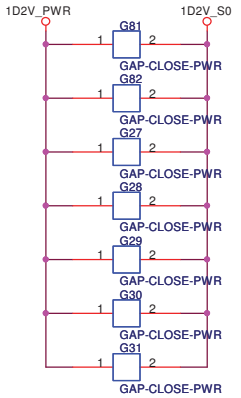
Date: Tuesday, March 15, 2005 | Sheet 45 of 51

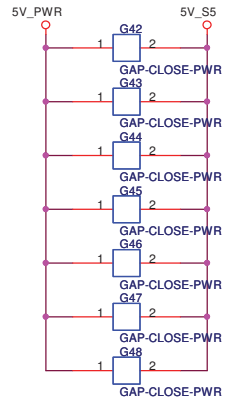
TI TPS5130 for 1D2V, 5V, 3D3V

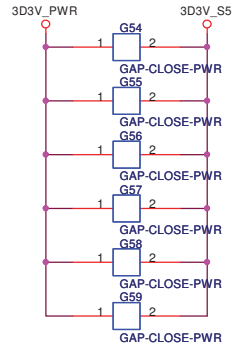
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)











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Taipei Hsien 221, Taiwan, R.O.C.

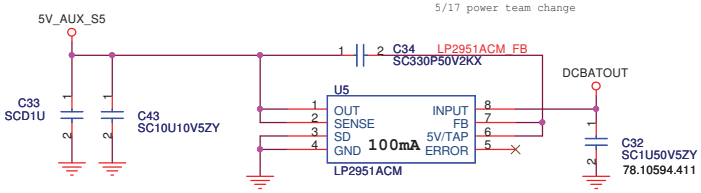
Title: TI TPS5130 1D2V/3D3V/5V (2/2)

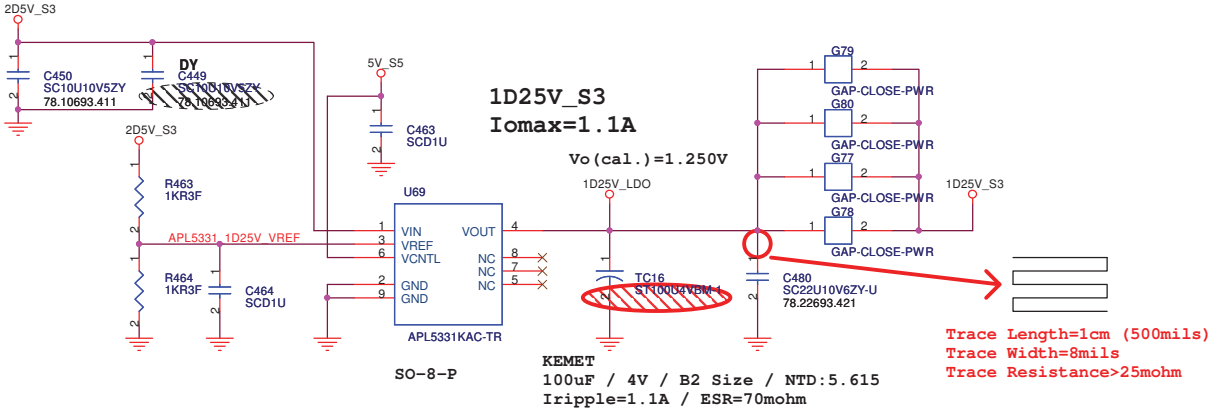
Size: A3 | Document Number: W37 | Rev: SB

Date: Monday, April 18, 2005 | Sheet 46 of 51

5V_AUX_S5

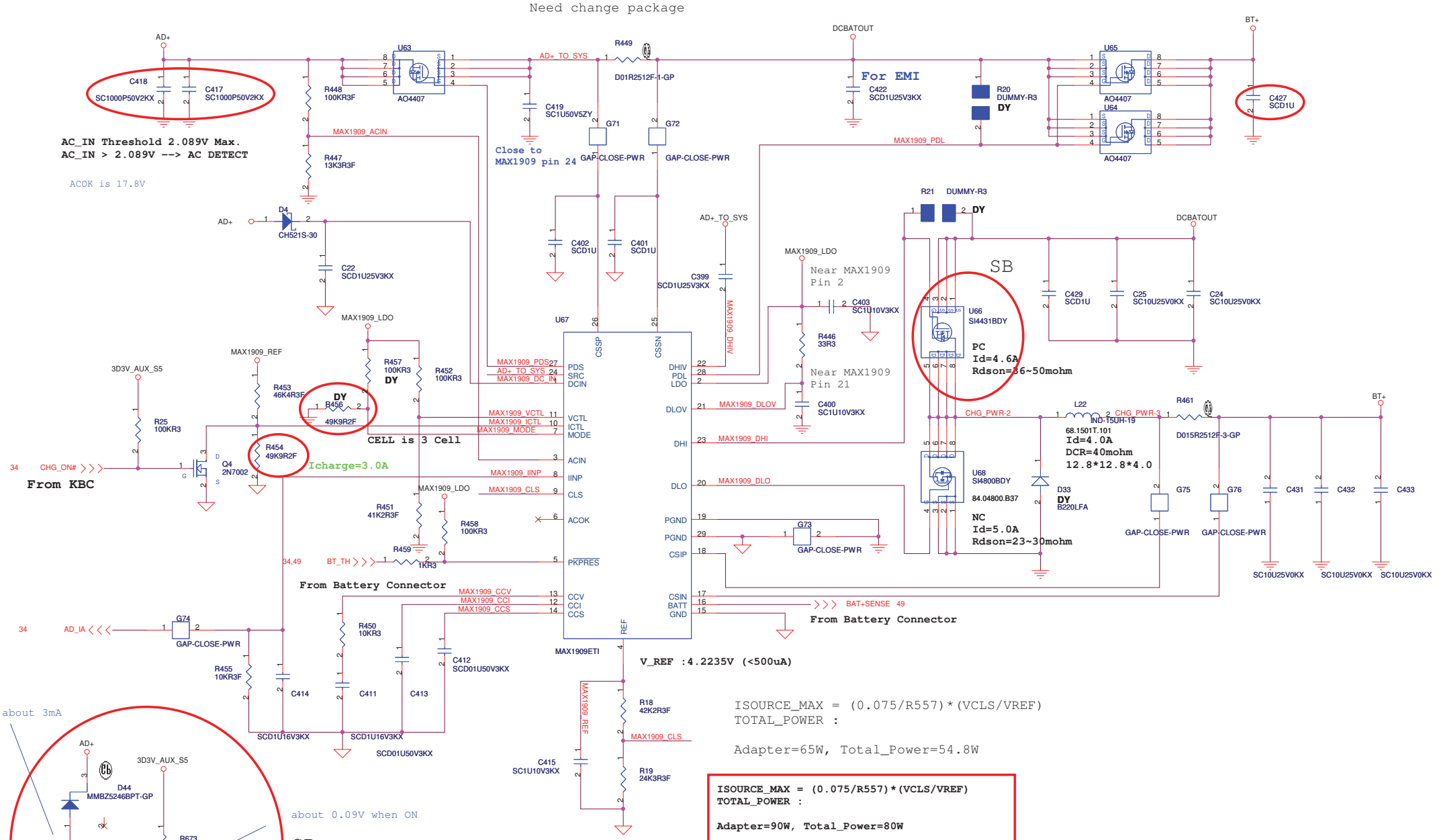
5/17 power team change





<Variant Name>

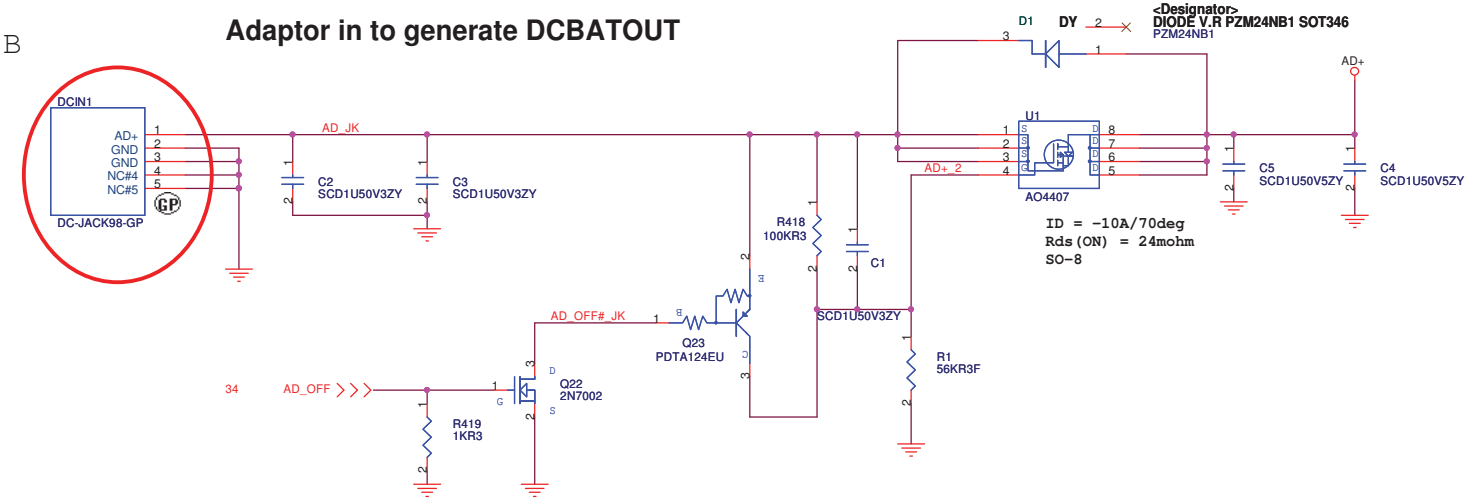
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***1D25V_LDO/5V_AUX***
Size: A3	Document Number: **W37**
Rev: SB	
Date: Monday, March 14, 2005	Sheet 47 of 51



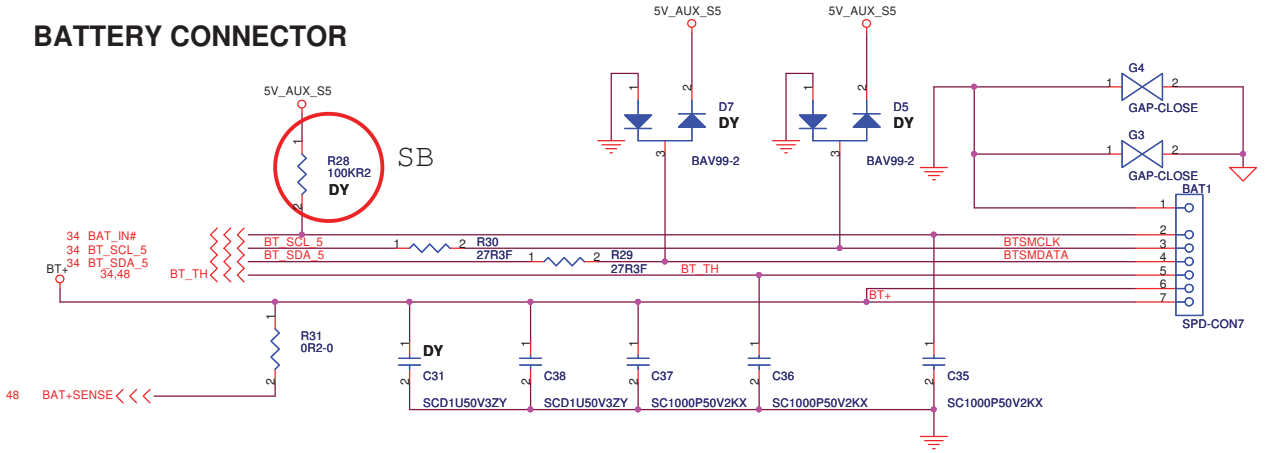
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CHARGER MAX1909	
Size: Custom	Document Number: W37	Rev: SB
Date: Friday, April 15, 2005	Sheet 48 of 51	

SB

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 **Wistron Corporation**
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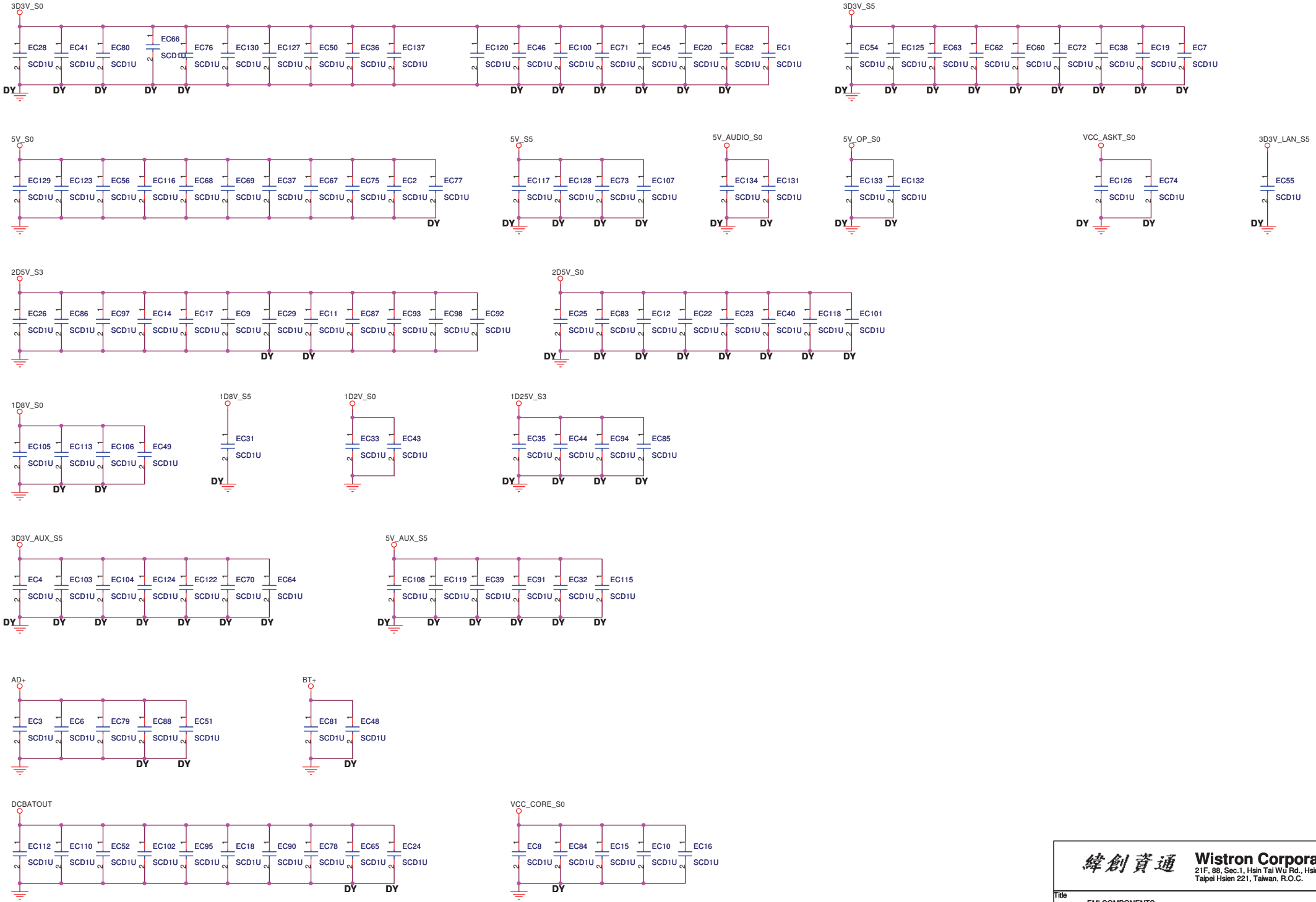
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BAT CONN***	
Size A3	Document Number W37	Rev SB
Date: Tuesday, March 15, 2005	Sheet 49 of 51	



緯創資通 **Wistron Corporation**
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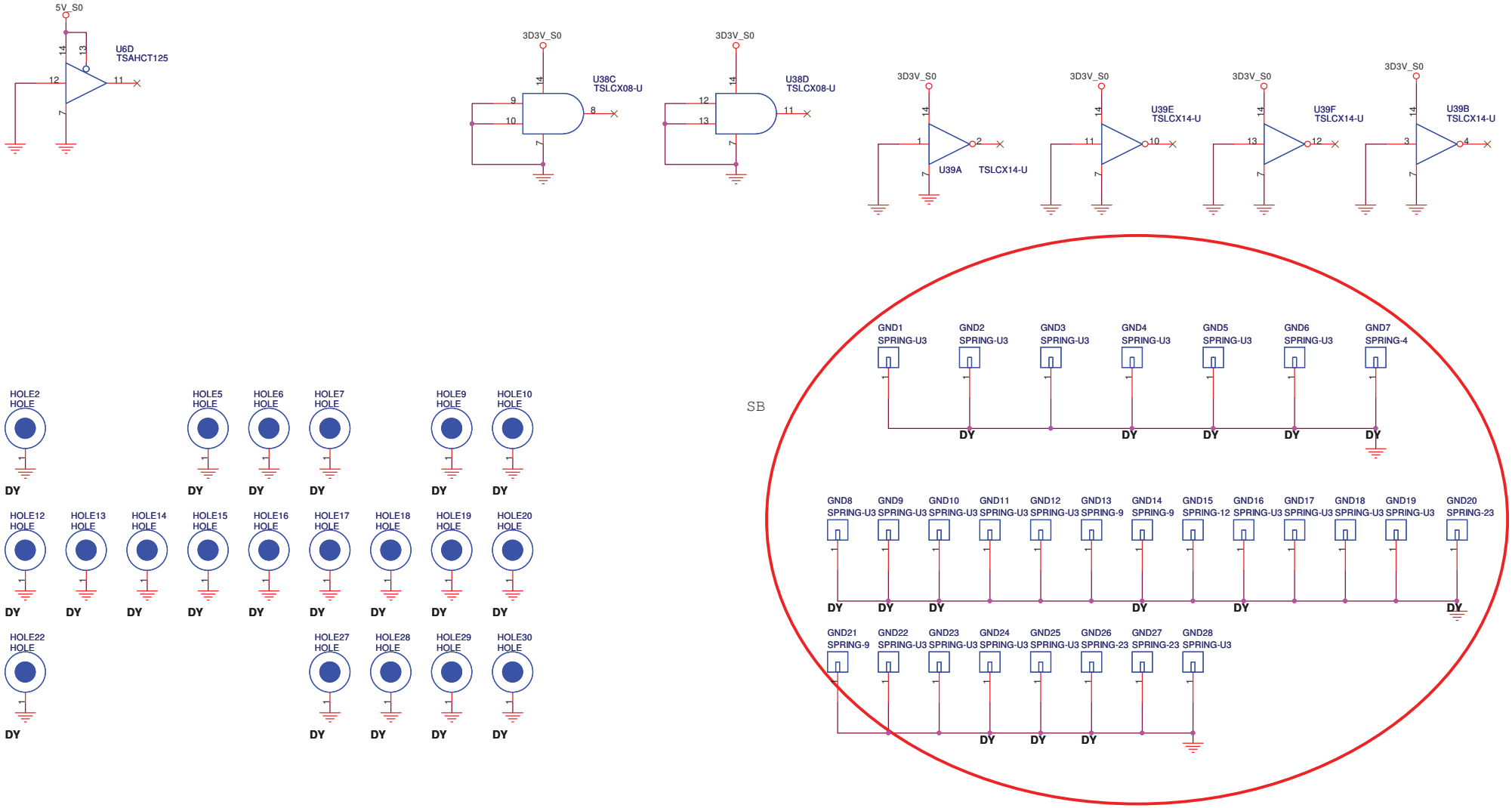
Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI COMPONENTS	
Size A3	Document Number W37	Rev SB
Date: Friday, March 25, 2005	Sheet 50 of 51	



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MISC		
Size: A3	Document Number: W37	Rev: SB
Date: Monday, April 18, 2005	Sheet 51 of 51	