Intel Calpella BlOCK DIAGRAM

INTEL DISCRETE SYSTEM DIAGRAM 01

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT
+1.05V_PCH
+1.05V_VTT

CPU VR
DC/DC
+3VPCU/+5VPCU/

POWER

SYSTEM RESET CIRCUIT
BATT CHARGER
RUN POWER SW
+3V_S5/+5V_S5
+3V_SUS/+5V_SUS
+5V_RUN/+3V_RUN/+1.8V_RUN

AC/BATT CONNECTOR

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

PCI-E x16

AMD
PARK-LP
23mm X 23mm
TDP 8W
(S3)

CRT
LVDS

CRT
LVDS

DDR3-SODIMM1 CHA
DDR3-SODIMM2 CHB
Dual Channel DDR3
1066 1.5V

DDR3 800MHz

VRAM
64Mx16x2,32bit

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD
SATA-HDD
SATA

USB conn x 3
Card Reader SD MS CARD
RTS5159
USB2.0 x 3
USB2.0

LAN
Realtek 10/100/ LAN RTL8103EL
PCIEx1

MINI-CARD
WLAN
PCIEx2

IHDA

AUDIO/AMP
ALC269

Audio SPK conn
Audio Jacks

LPC
SPI

EC
ITE8502

FLASH 2Mbyts

18X8
Keyboard

SPI
PS/2

FLASH 2Mbyts
Touchpad

Quanta Computer Inc.
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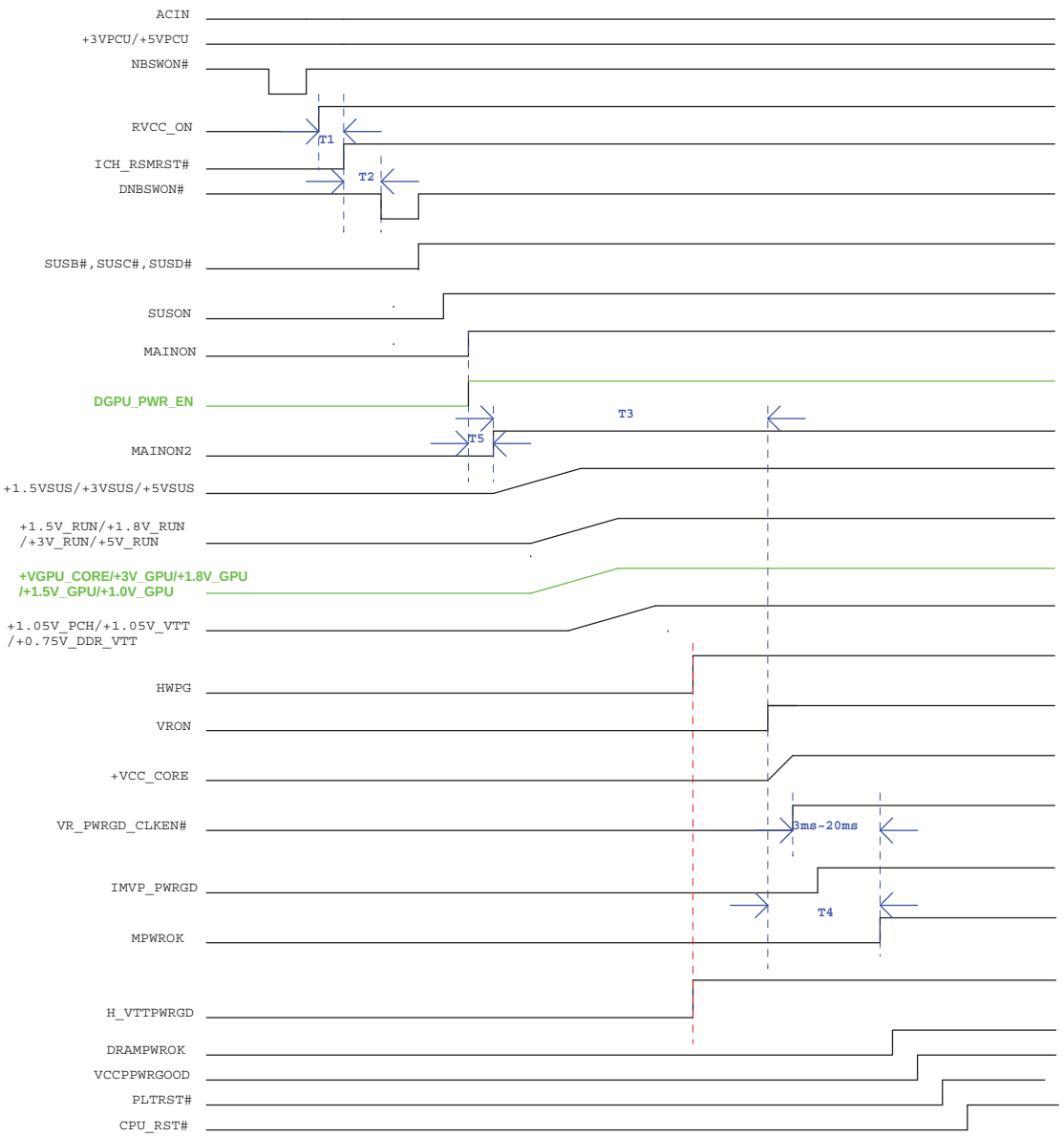
Power Sequence



T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to DNBSWON = 680us

Quanta Computer Inc.
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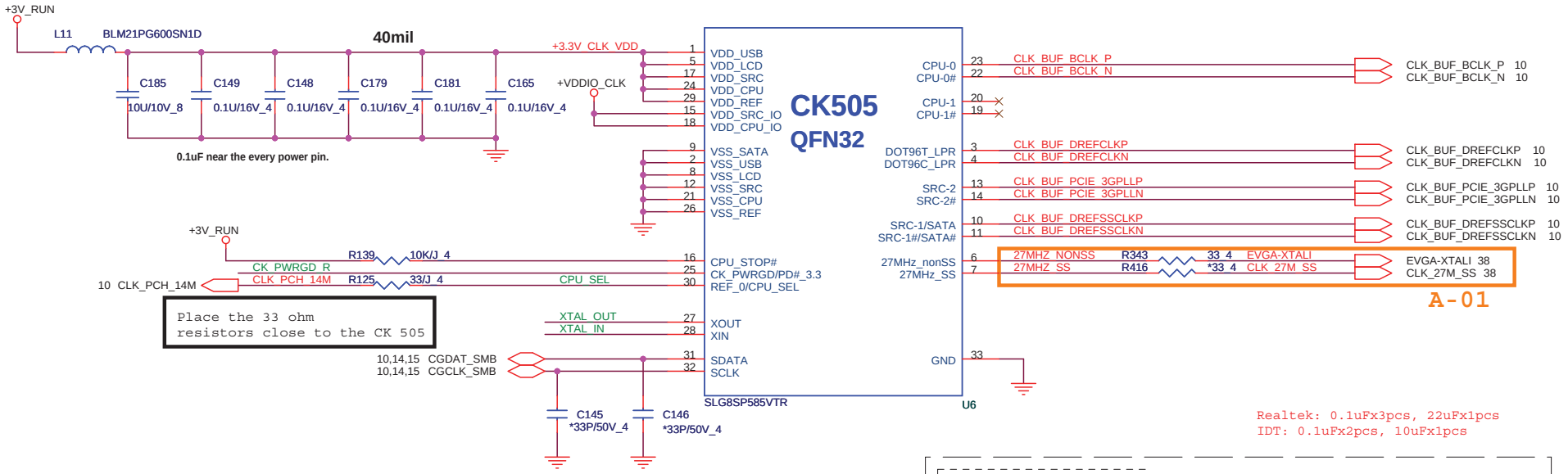

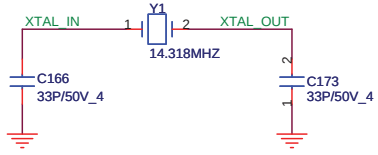

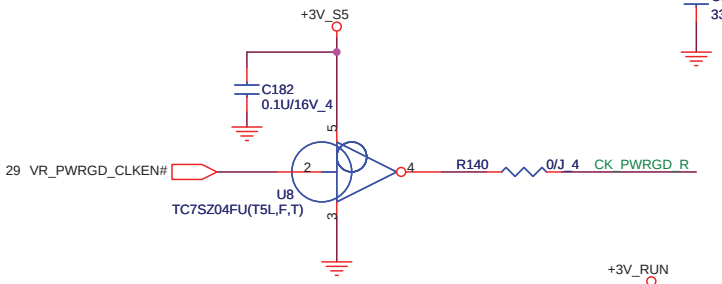

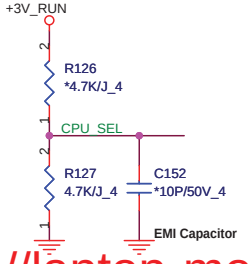

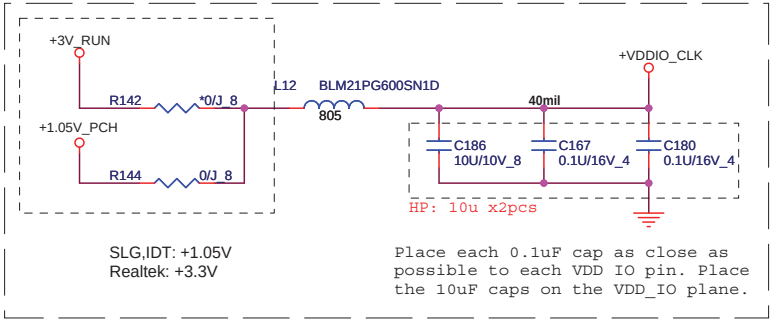

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V

PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

Quanta Computer Inc.
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Size	Document Number	Rev
	Clock Generator	1A
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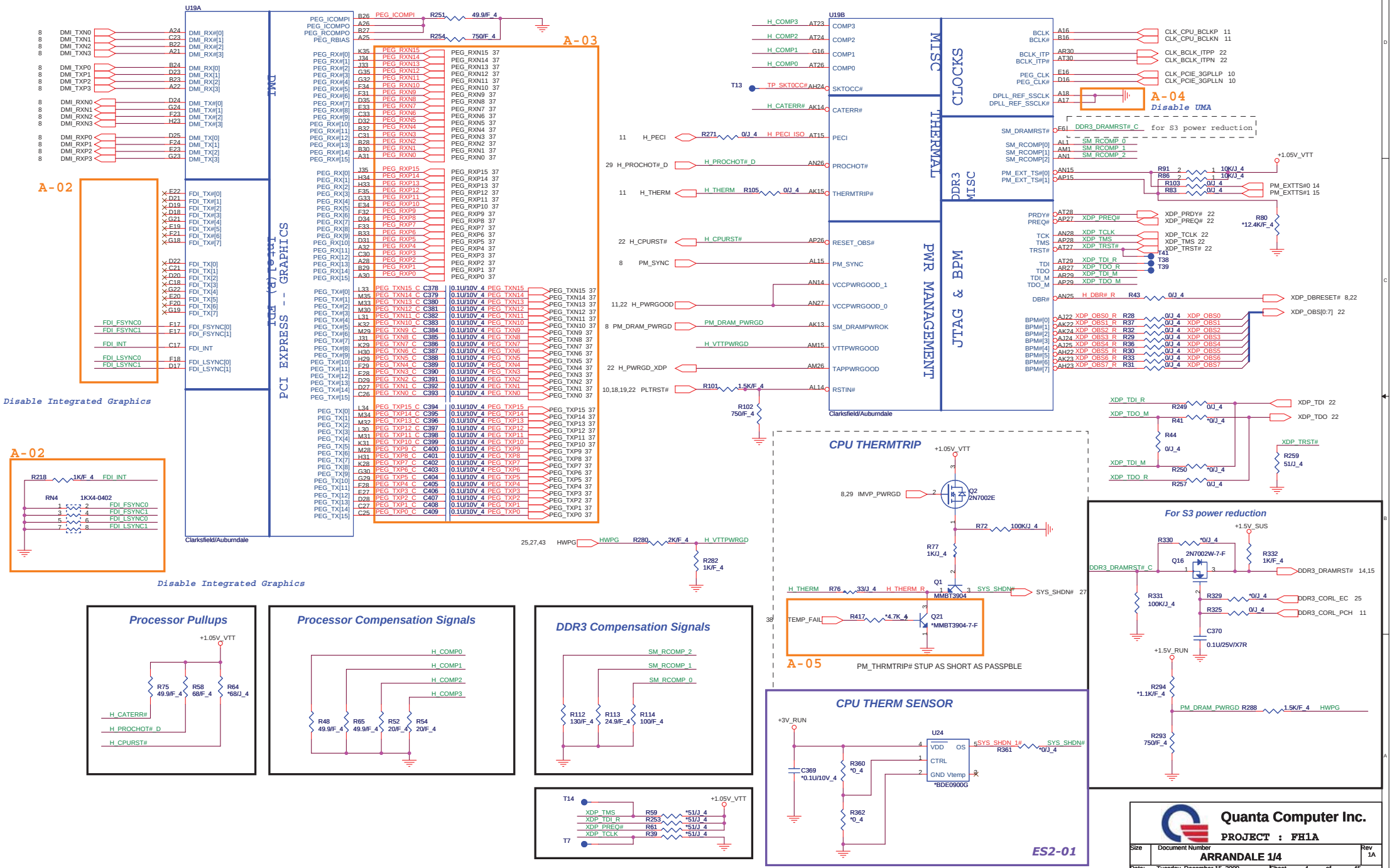
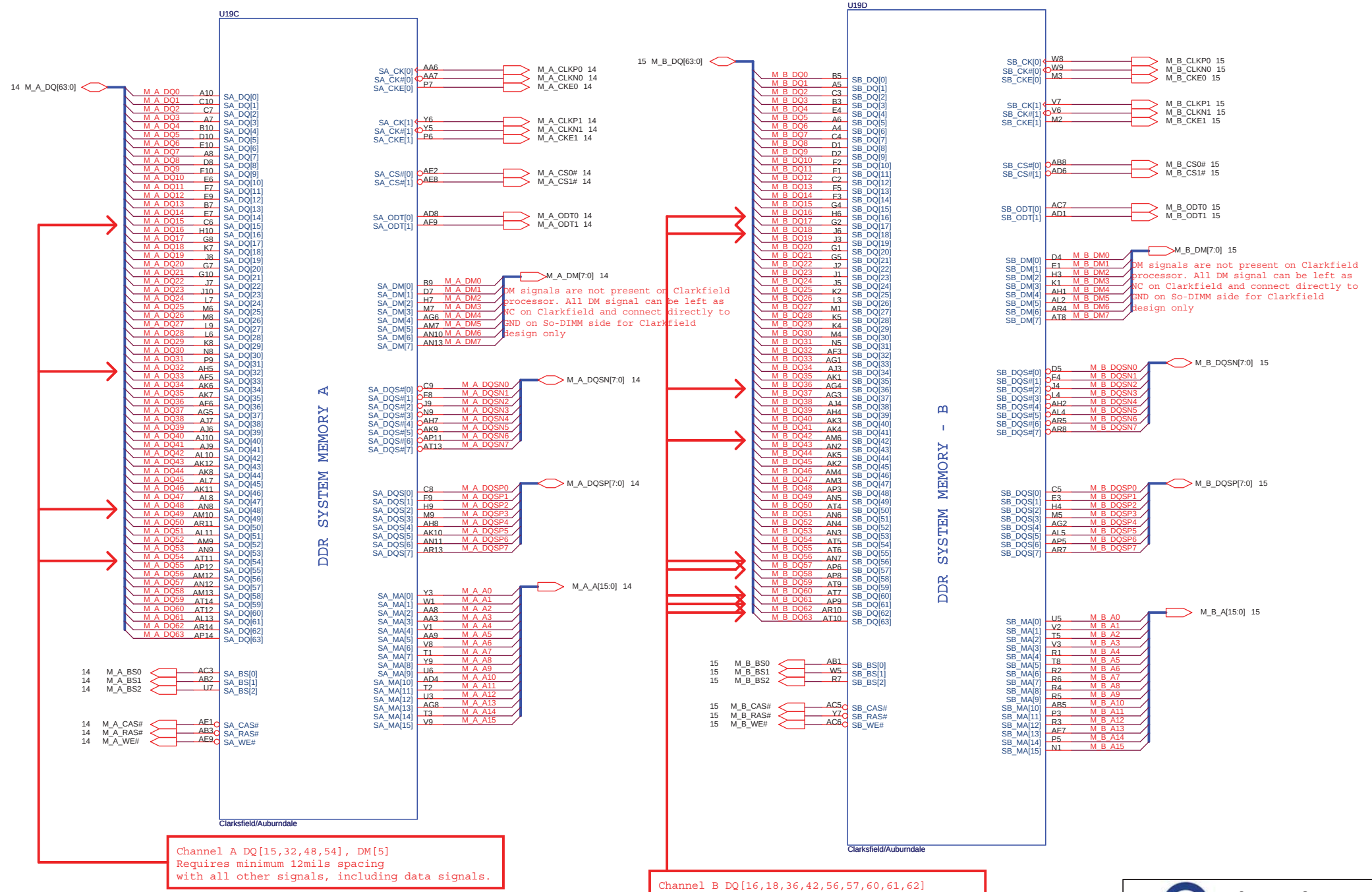


ARRANDALE PROCESSOR (DDR3)

05



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PROJECT : FH1A

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ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU Core Power

U19F

+VCC_CORE=4.8 max

+VCC_CORE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

+1.05V_VTT=1.8 max

+1.05V_VTT

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

PSI# AN33 H_PSI# → H_PSI# 29

VID[0] AK35 VID0 → VID0 29
VID[1] AK33 VID1 → VID1 29
VID[2] AK34 VID2 → VID2 29
VID[3] AL35 VID3 → VID3 29
VID[4] AL33 VID4 → VID4 29
VID[5] AM33 VID5 → VID5 29
VID[6] AM35 VID6 → VID6 29
PROC_DPRSLPVR AM34 DPRSLPVR → DPRSLPVR 29

VTT_SELECT G15 → H_VTTVID1 30

ISENSE AN35 → I_MON 29

VCC_SENSE AJ34 → VCCSENSE 29
VSS_SENSE AJ35 → VSSSENSE 29

VTT_SENSE B15 → VTT_SENSE 30
VSS_SENSE_VTT A15 → VSS_SENSE_VTT 30

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

+VCC_CORE

R216 100/F_4

R217 100/F_4

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

A-06

U19G

GRAPHICS POWER

PCI & DMI

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

1.1V

1.8V

A-06 Disable UMA

R220 1K/F_4

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

+1.5V_RUN

+1.8V_RUN

Clarksfield/Auburndale

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

Quanta Computer Inc.

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	ARRANDALE 3/4	1A
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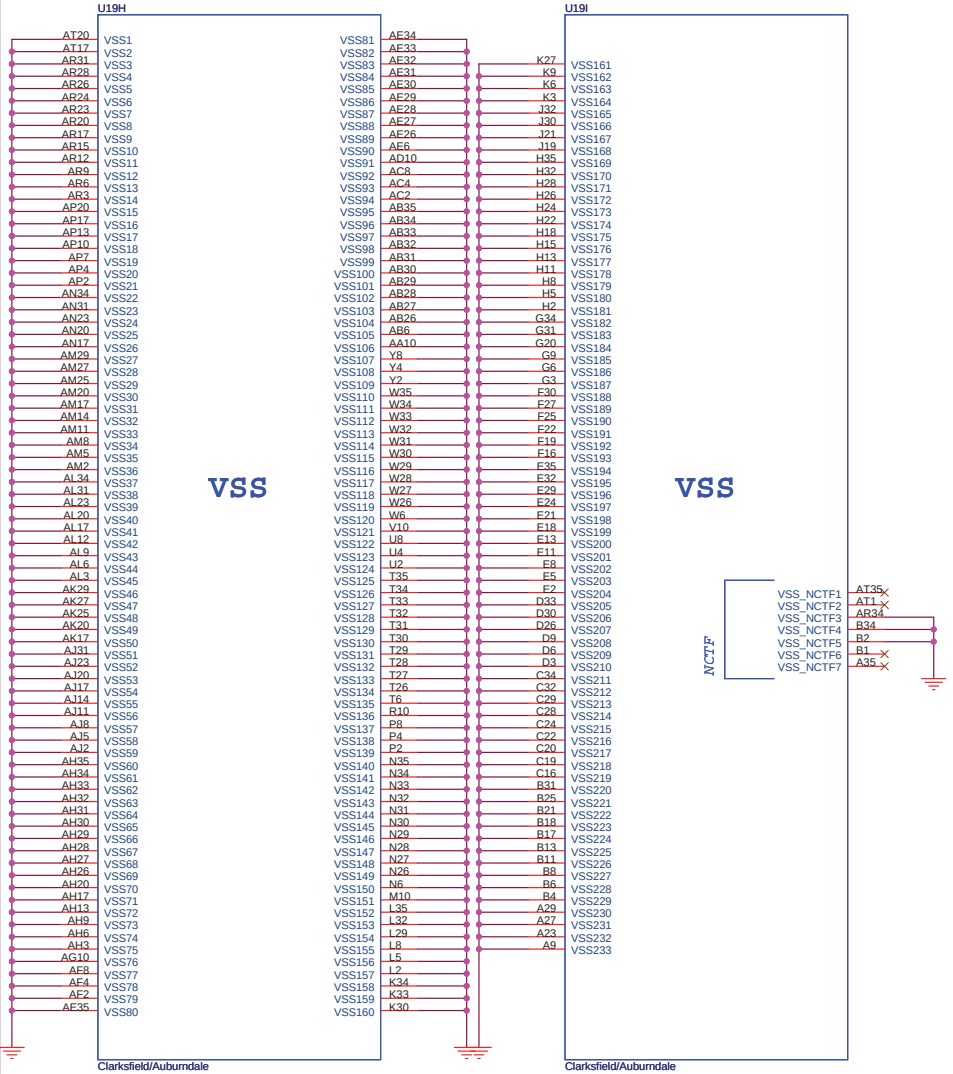
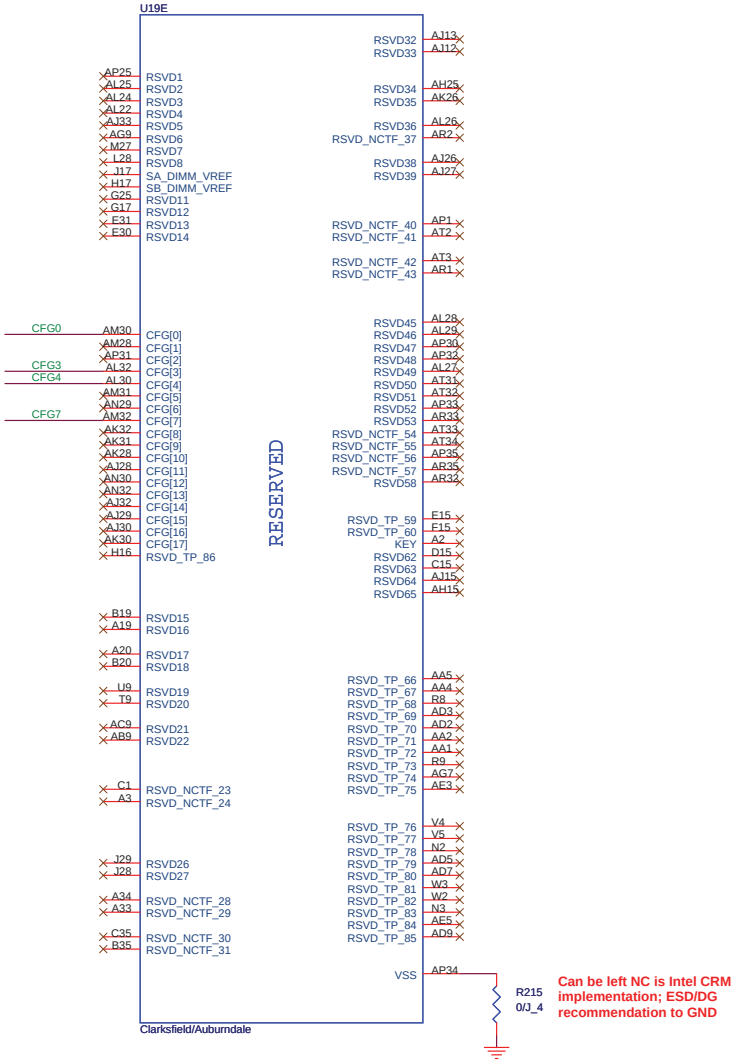
ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR(RESERVED, CFG)



07

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.

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	ARRANDALE 4/4	1A
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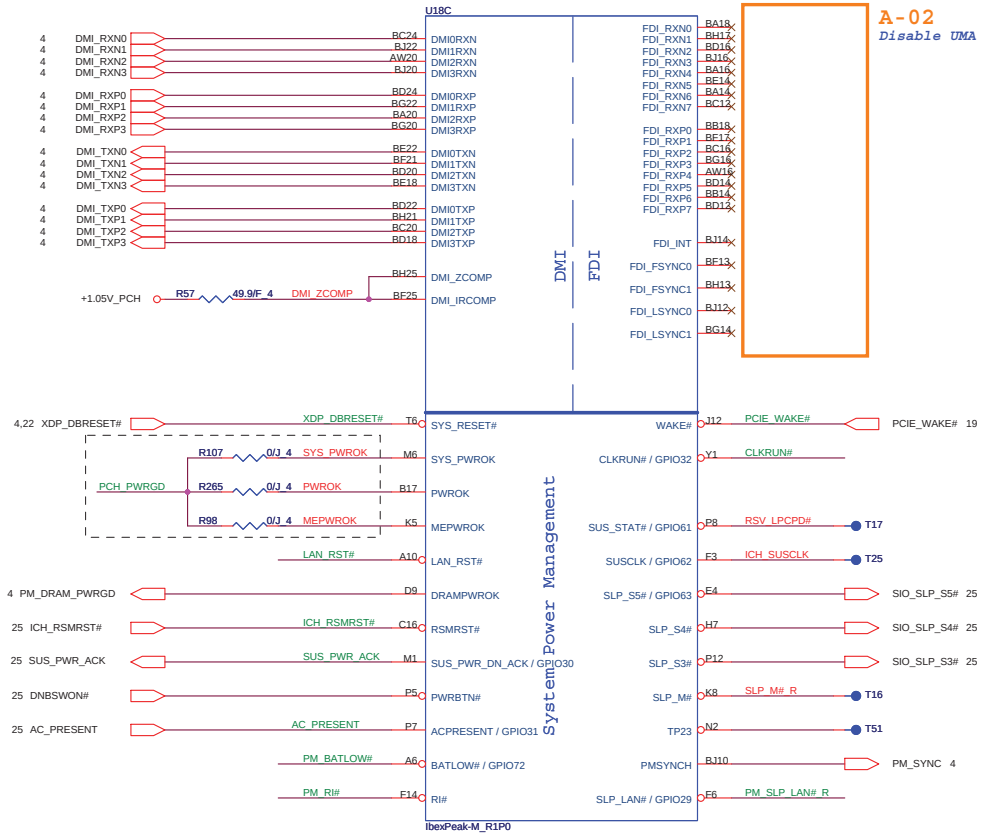
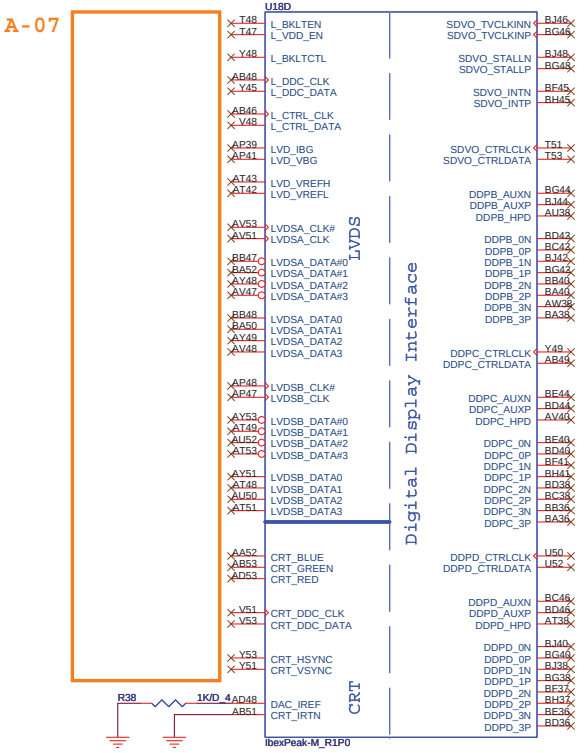
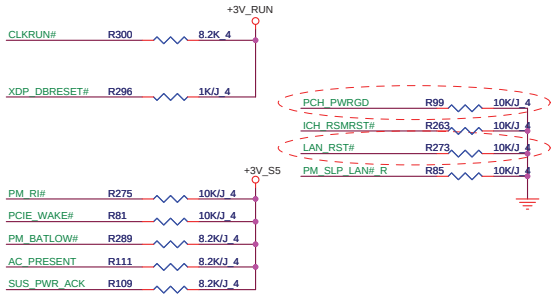
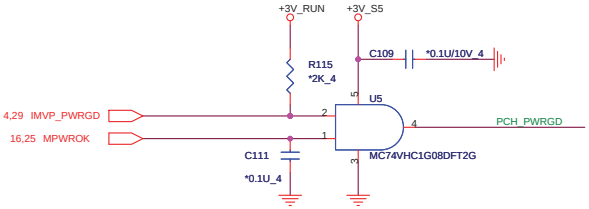
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)







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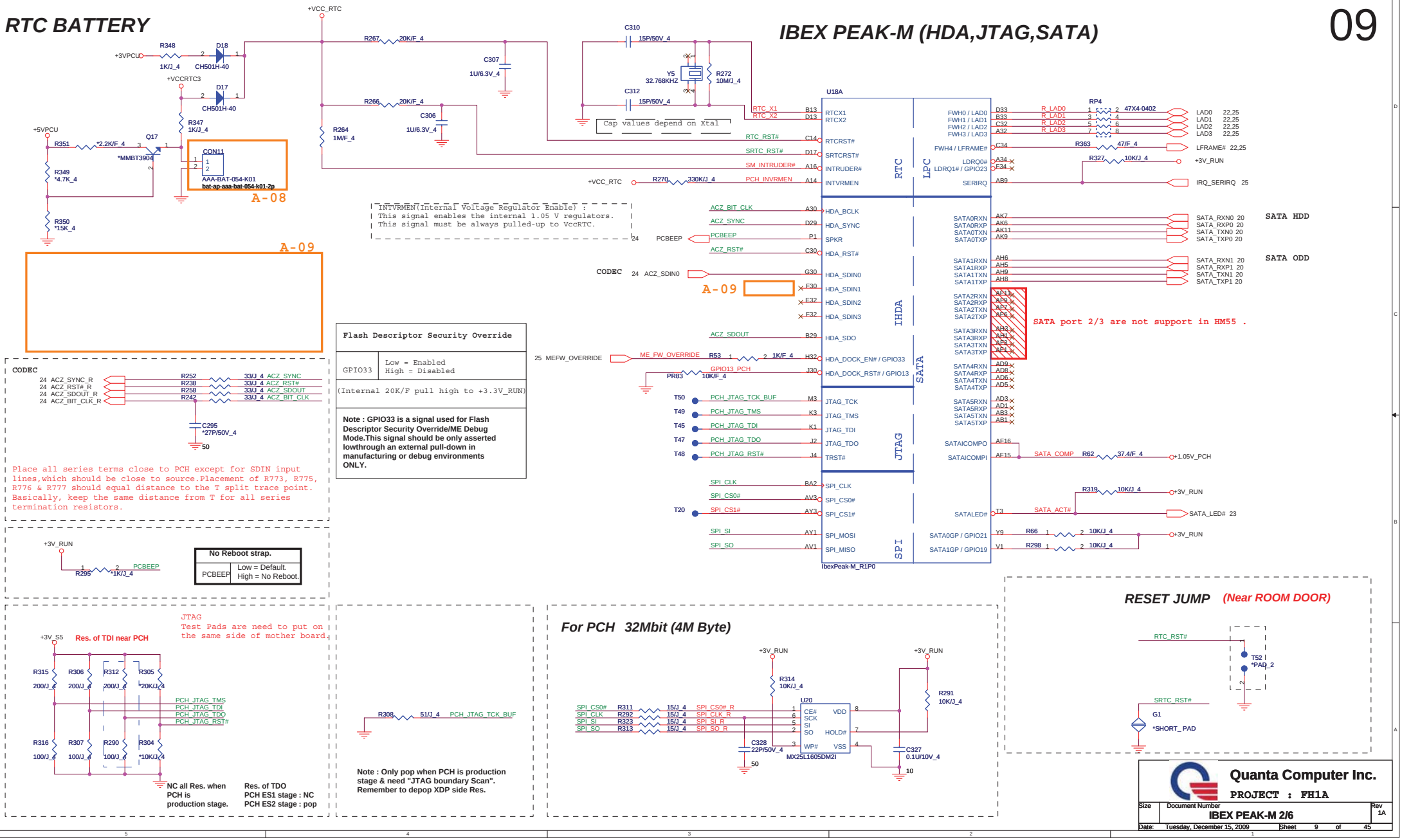
RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09



Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.

PCBEEP	Low = Default. High = No Reboot.

Quanta Computer Inc.

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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

PCIE port 7/8 are not support in HM55 .

USB port 6/7 are not support in HM55 .

USB PORT 1(DB)
USB PORT 2(MB)
USB PORT 4(MB)
CAMERA
BT
WLAN
CARD READER

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected
if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

OC0#-OC7#:
DG(V1.0)P214

Pin	Default Port Mapping
OC0#	Port0,Port1
OC1#	Port2,Port3
OC2#	Port4,Port5

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

CLKOUTFLEX3:
EDS(V1.0) :support 48MHz
33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is
recommend (PCI & non PCI routing,
single & double load)

SMLOCLK/SMLODATA:
DG(V1.1) P255: The 82577 SMBus signals
(SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SMLODATA and SMLOCLK pins, respectively.

FOR DDR3 SPD/CLOCK GE
EXPRESS CARD/MINI CAR
0 FOR INTEL LAN
1 FOR EC

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

Quanta Computer Inc.	
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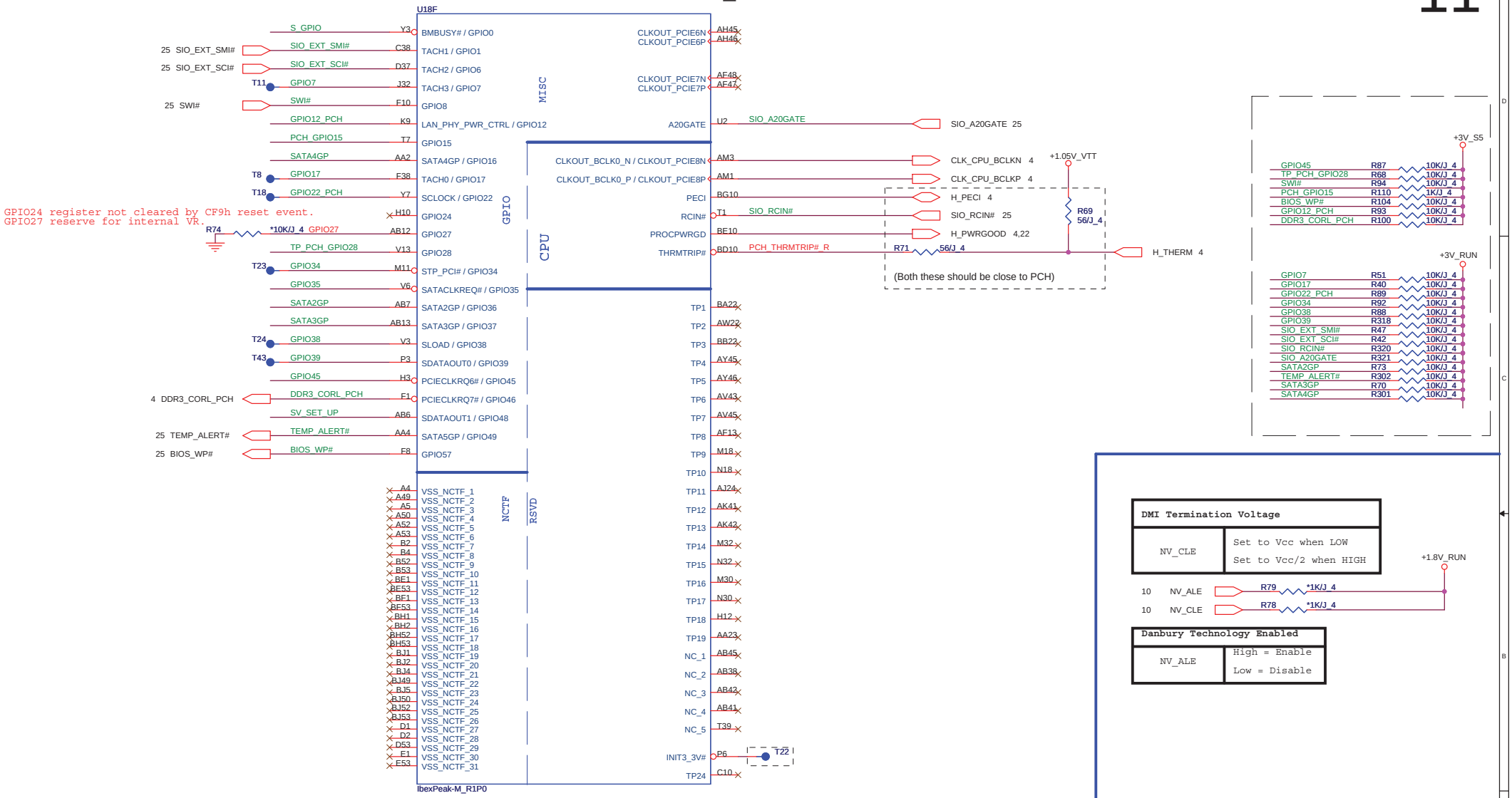
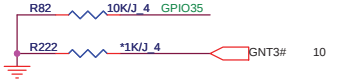
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



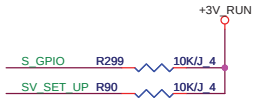
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high



SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

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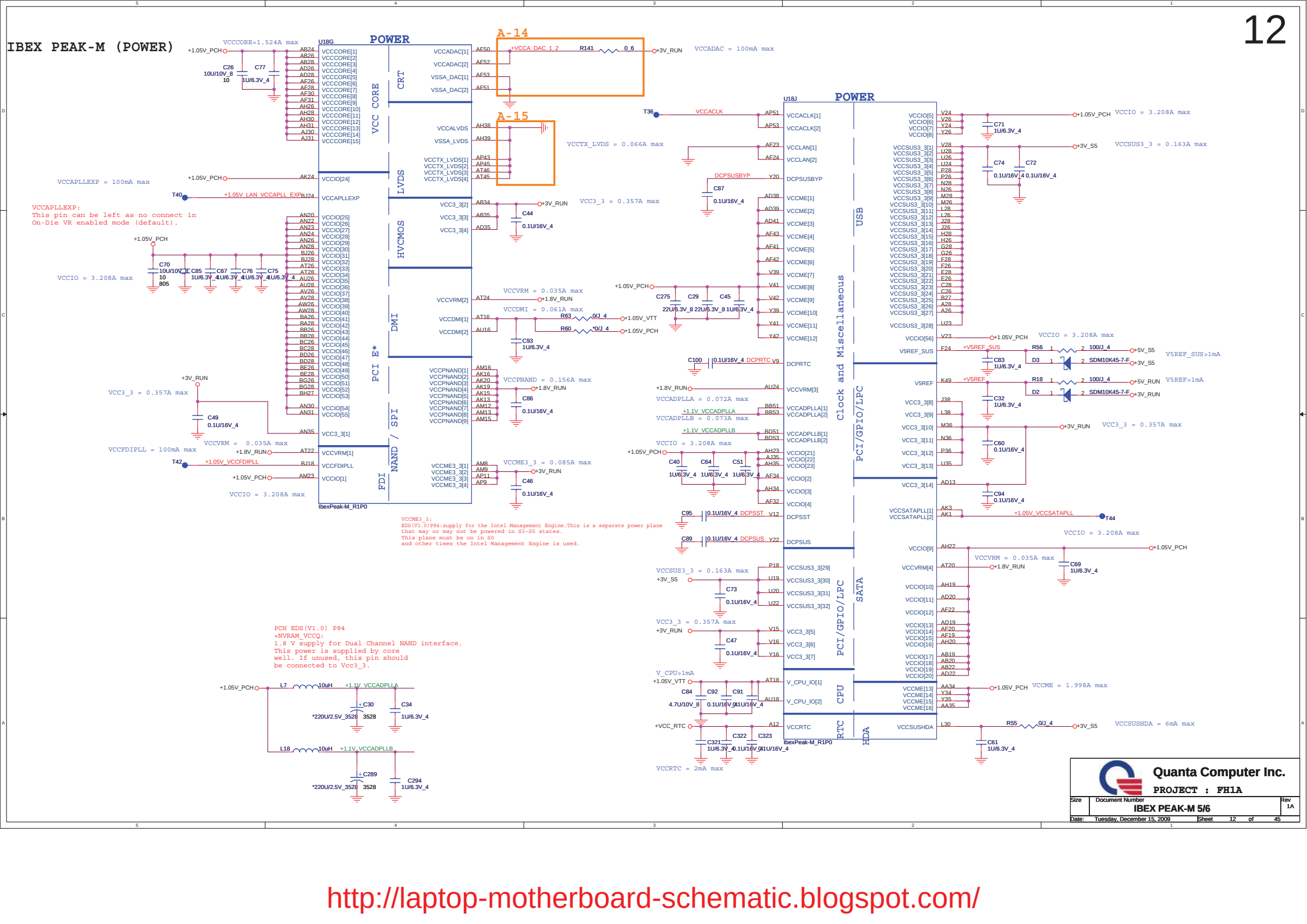
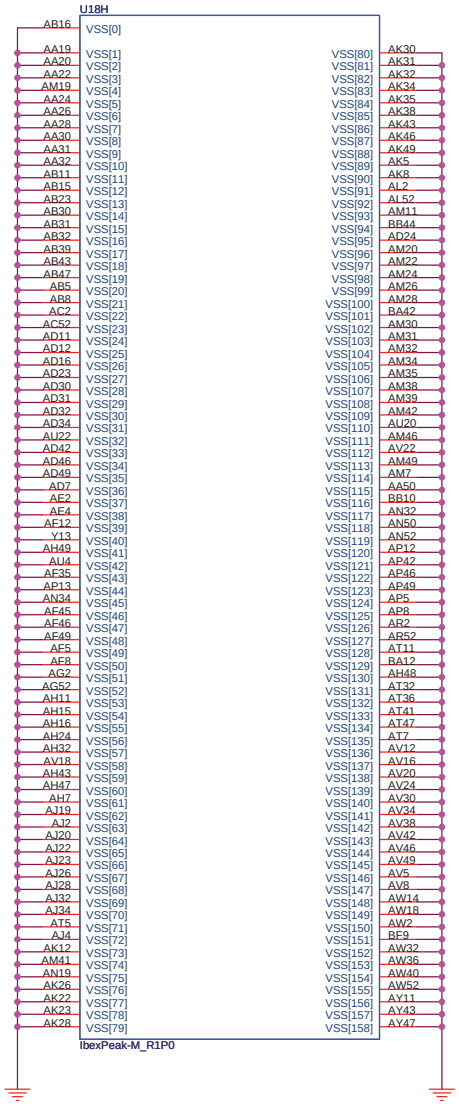
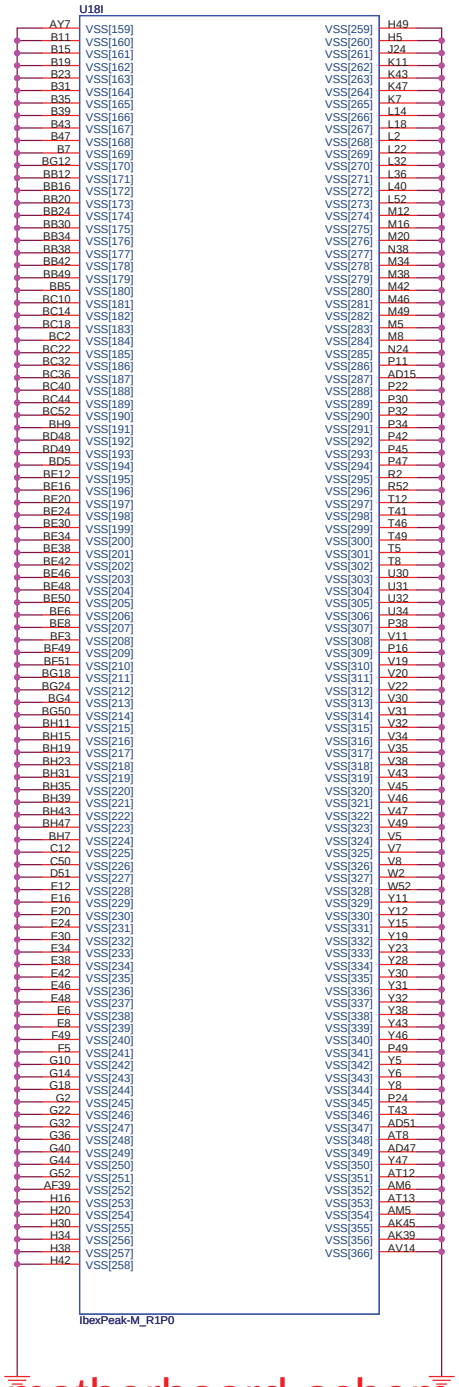
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





Quanta Computer Inc.

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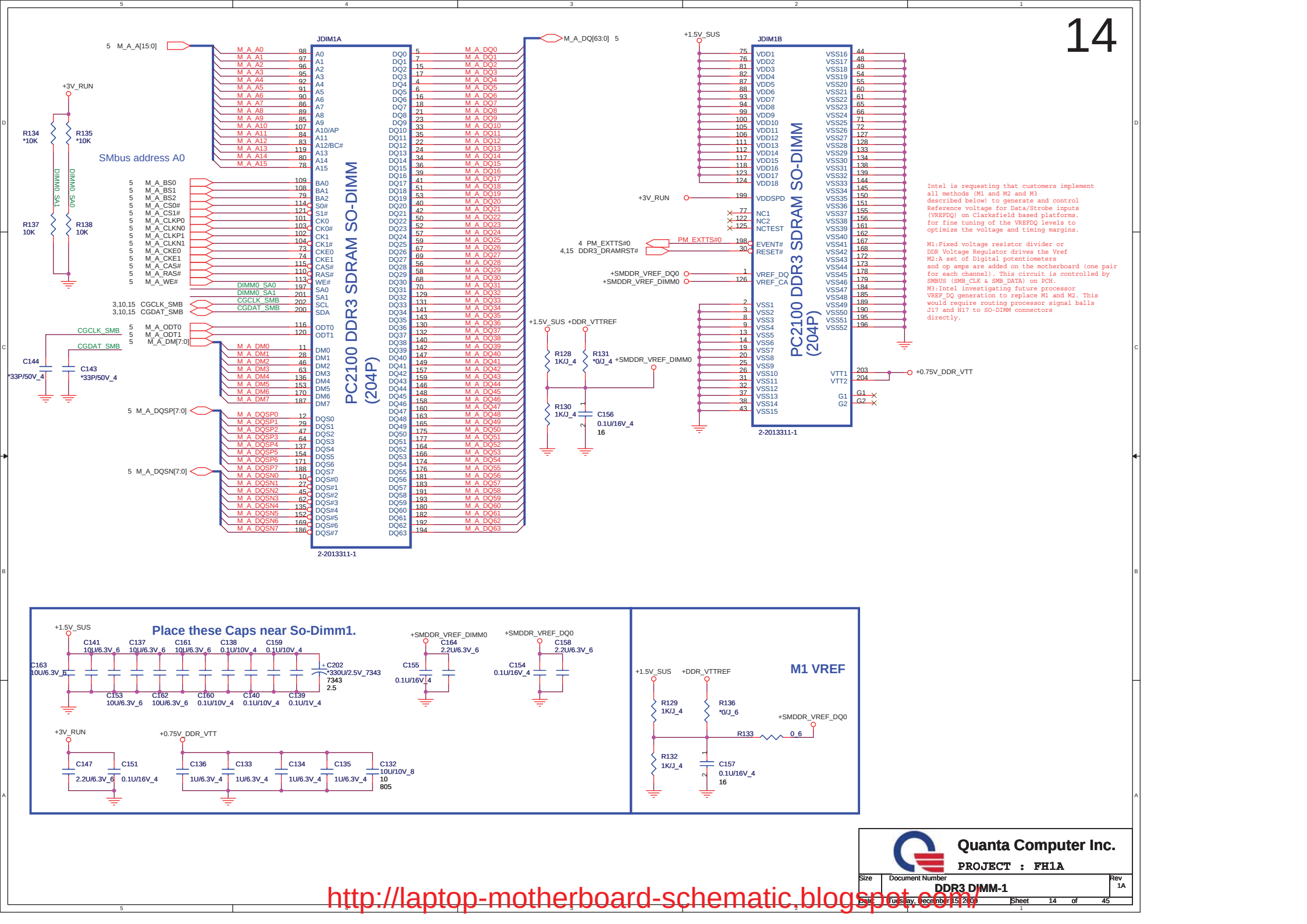

Quanta Computer Inc.

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	DDR3 DIMM-1	1A
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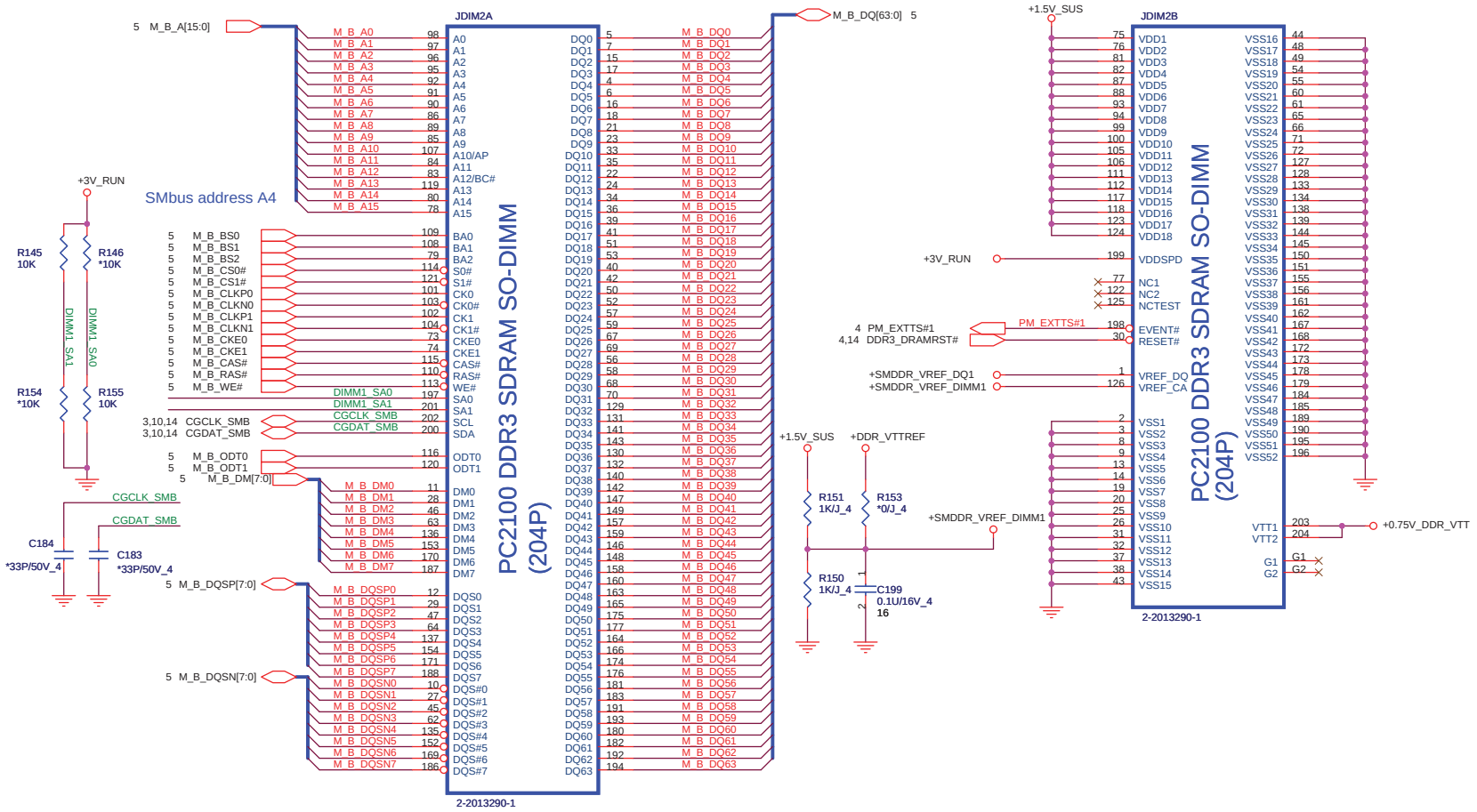

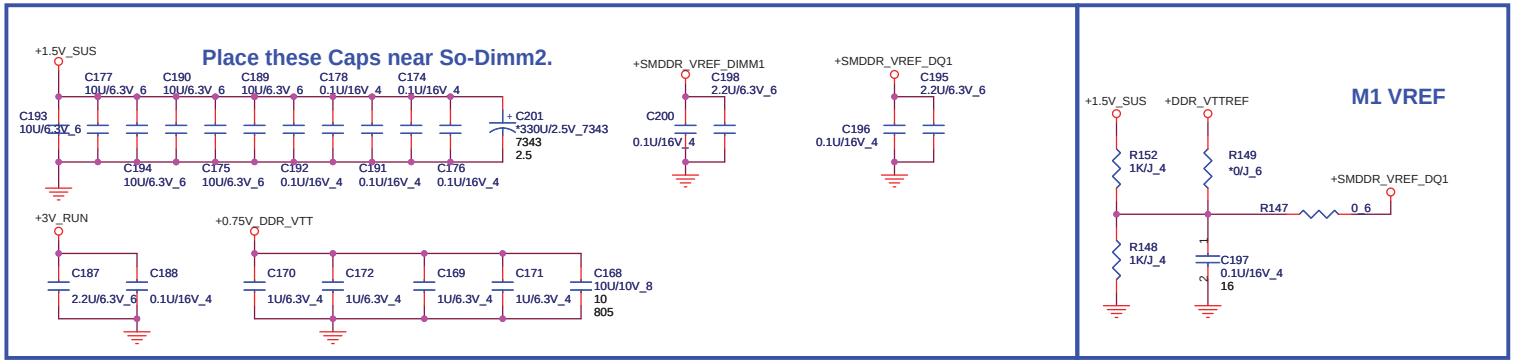

Quanta Computer Inc.

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	DDR3 DIMM-2	1A
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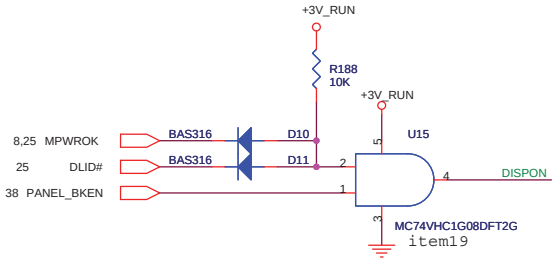
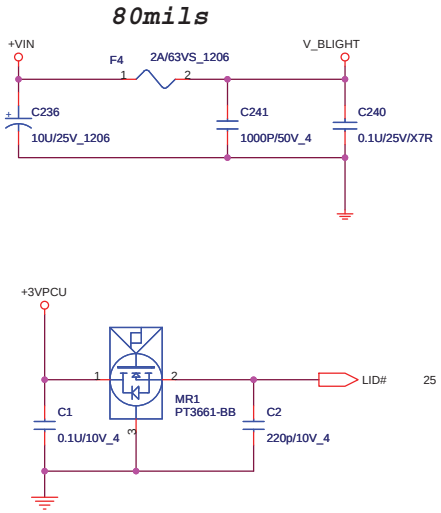
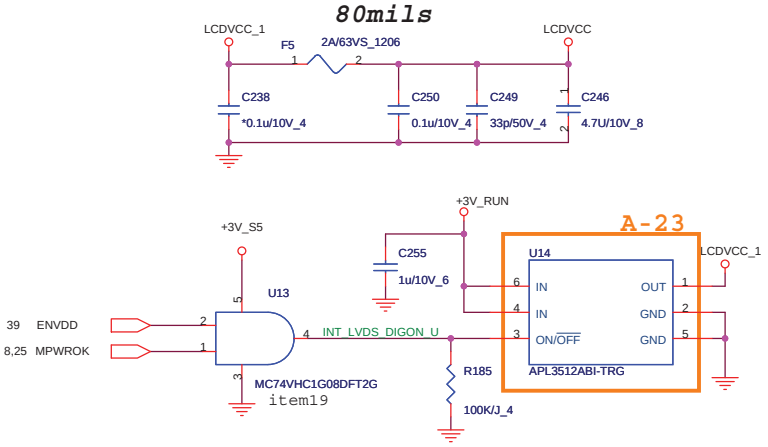
Backlight Control(LDS)

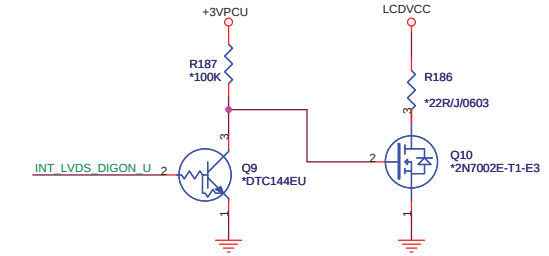


BACKLIGHT POWER

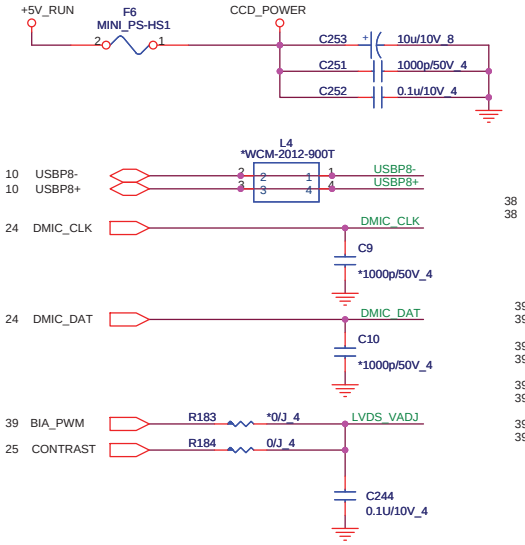


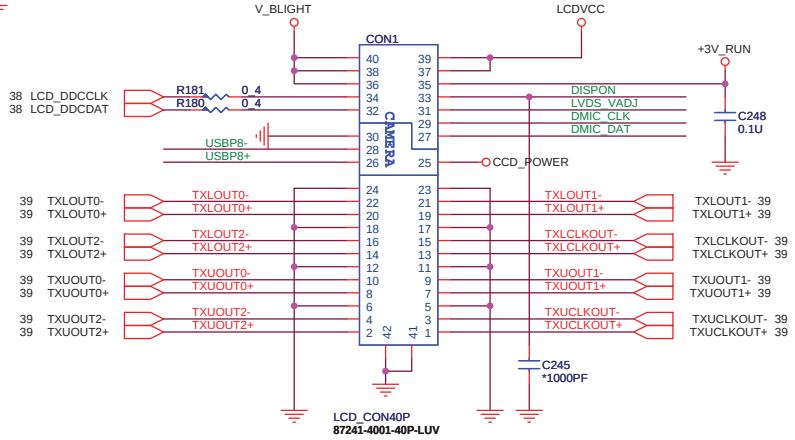
LED Panel POWER SWITCH(LVDS)





LVDS/CCD





Quanta Computer Inc.

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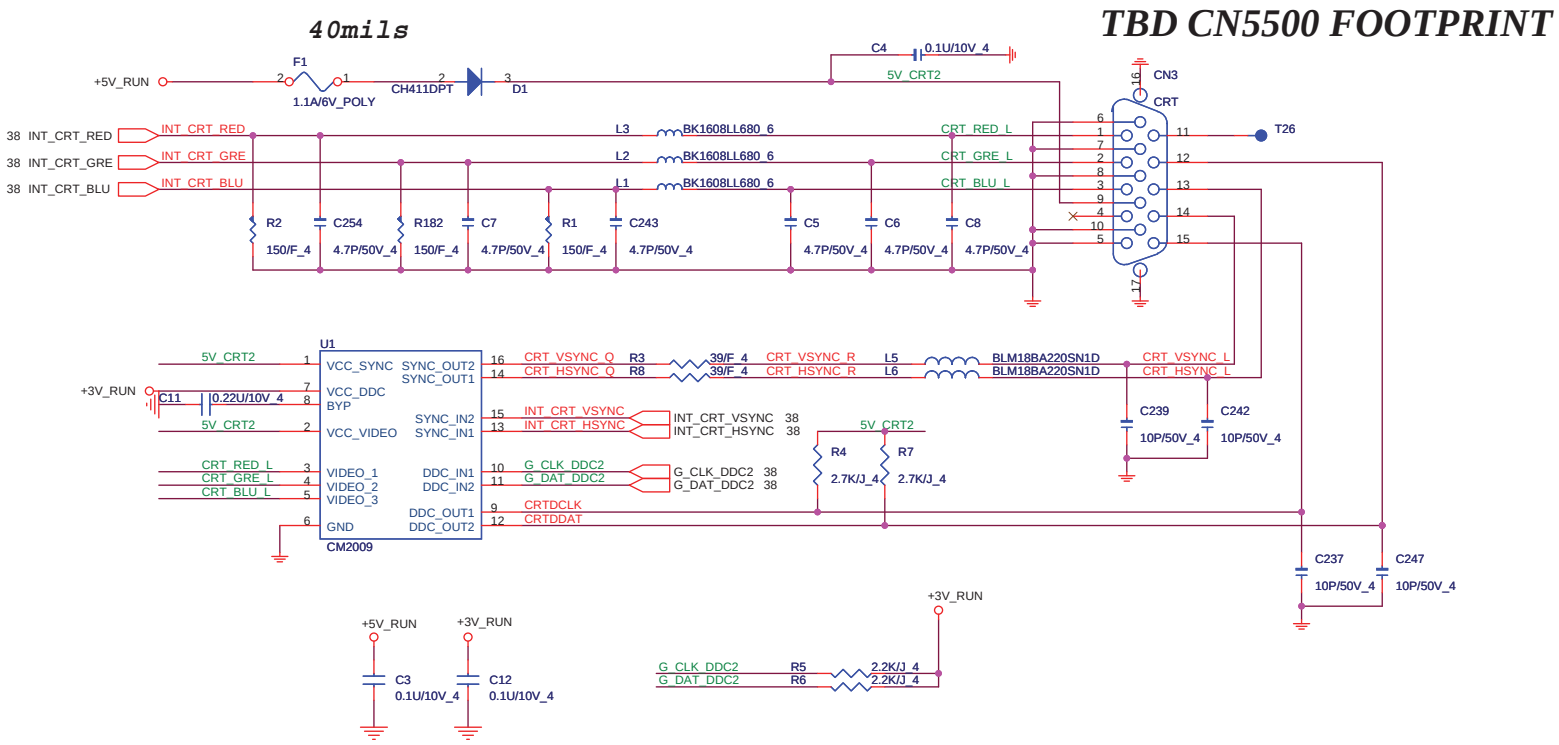
CRT CONN/DDC LEVEL SHIFT



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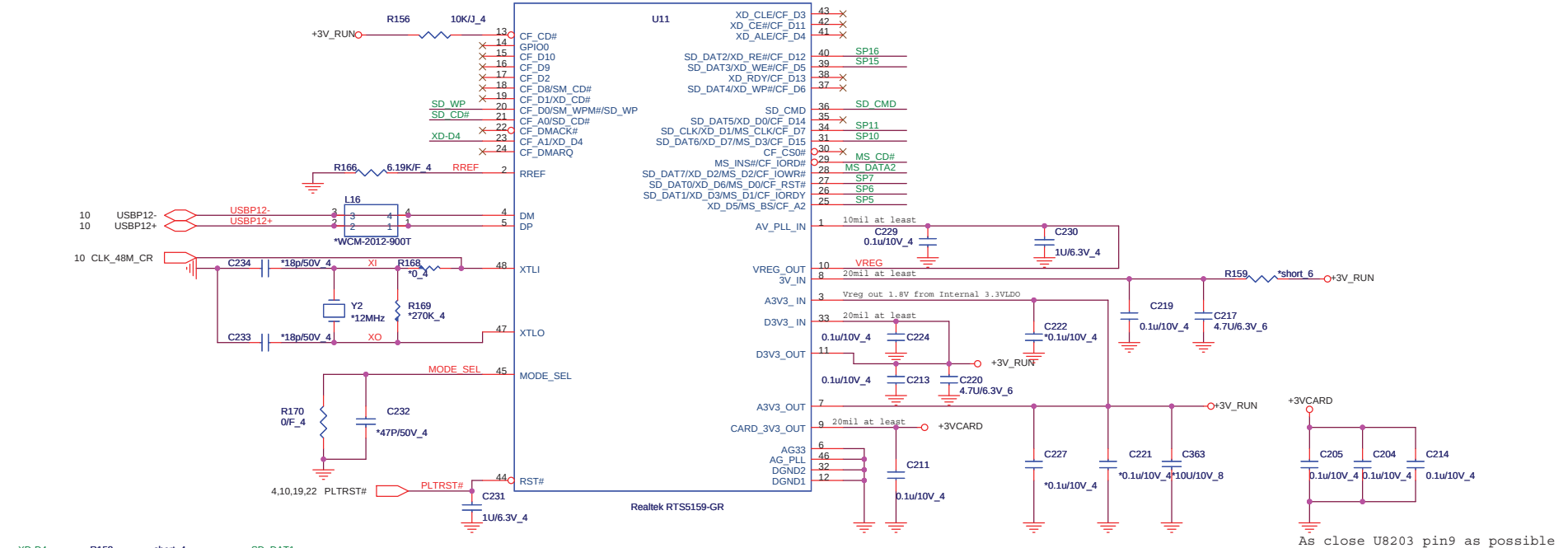
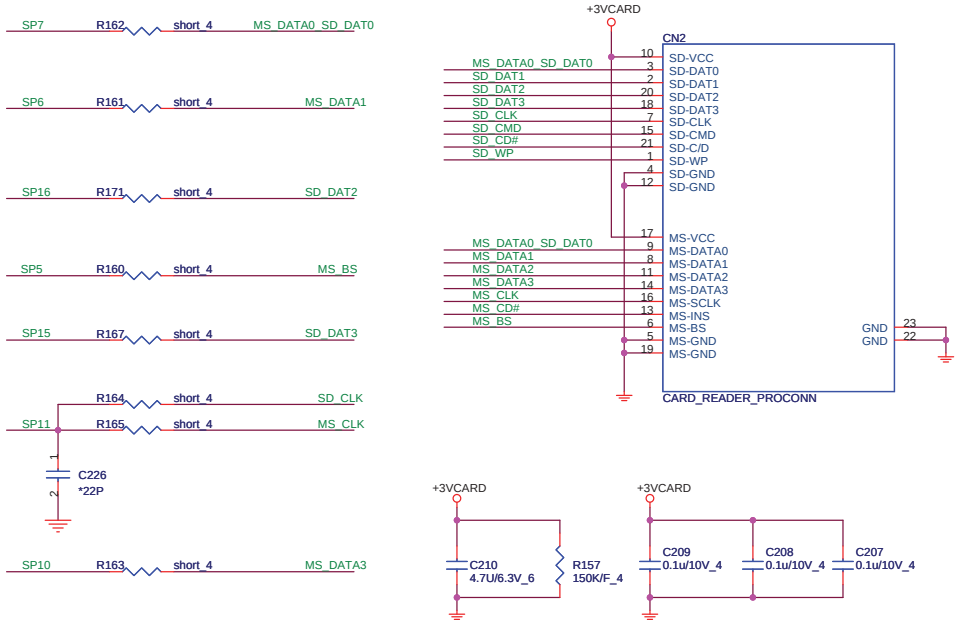
Card Reader



As close U8203 pin9 as possible

For 5158E

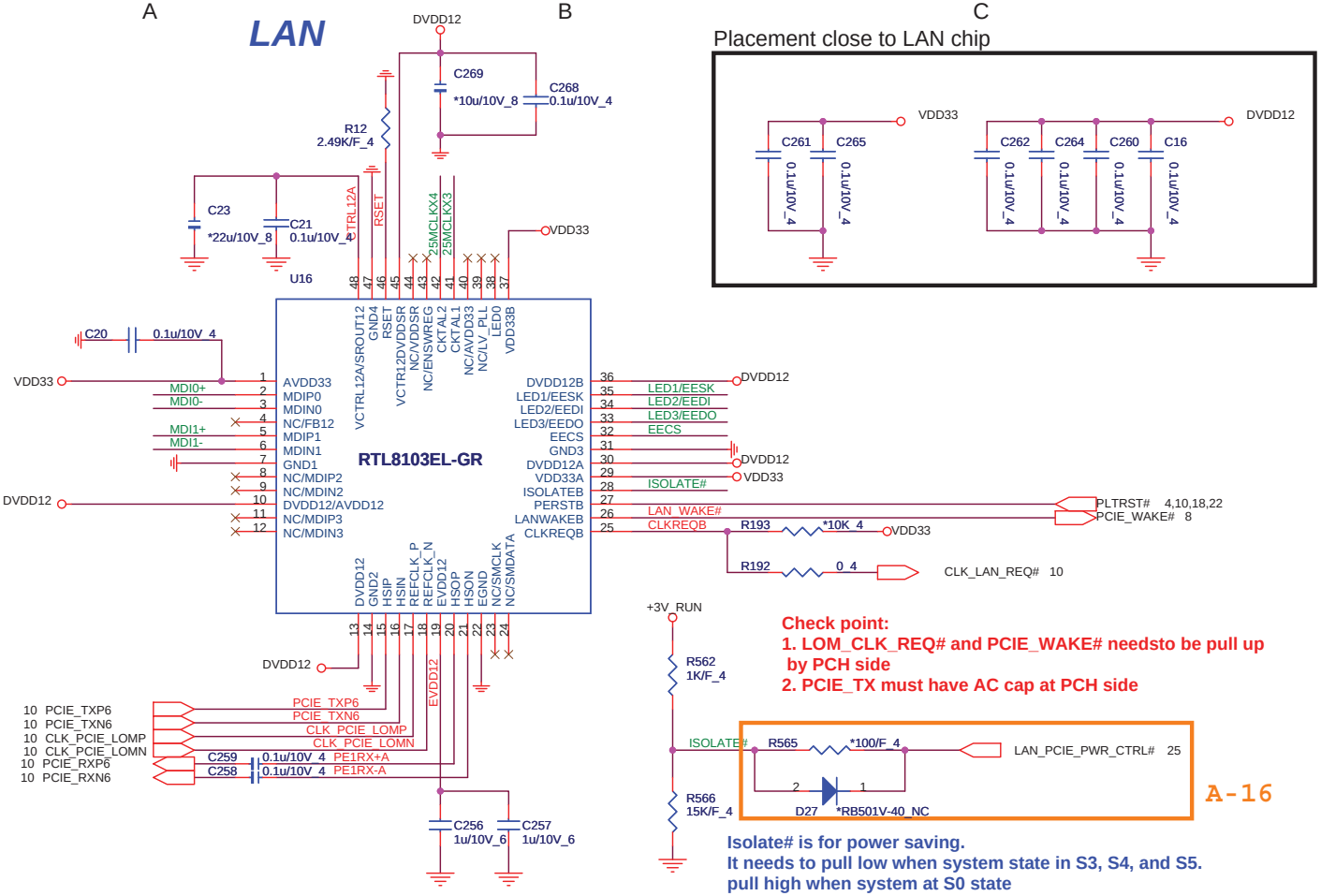


Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	Card Reader RTS5159	1A
Date: Monday, December 07, 2009	Sheet 18 of 45	

LAN



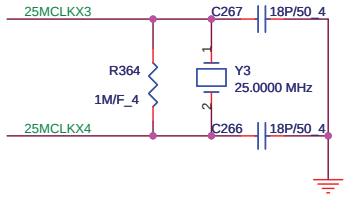
Placement close to LAN chip

Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

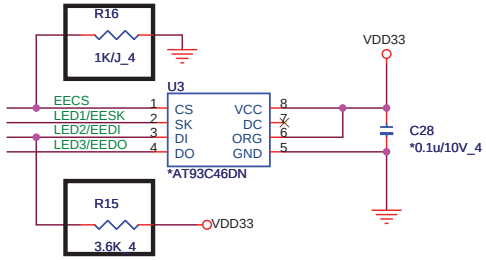
A-16

Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

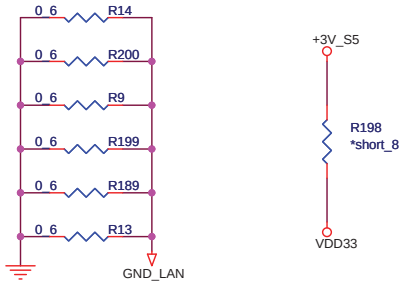
X'tal 25MHz



LAN EEPROM

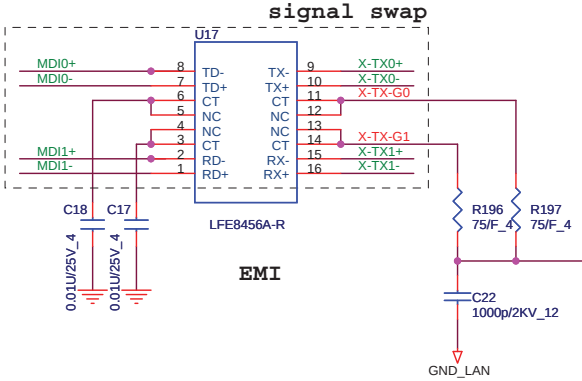


LAN Power

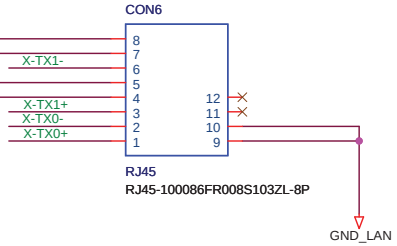


10/100 Transformer

signal swap



RJ45



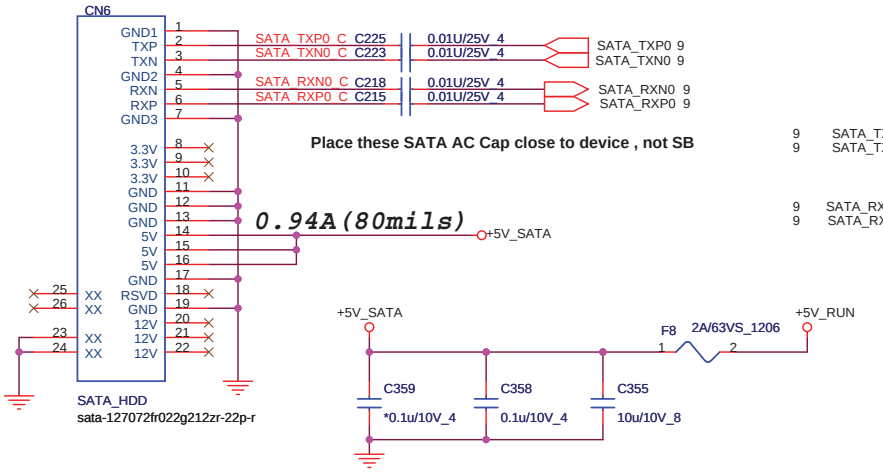
Quanta Computer Inc.

PROJECT : FH1A

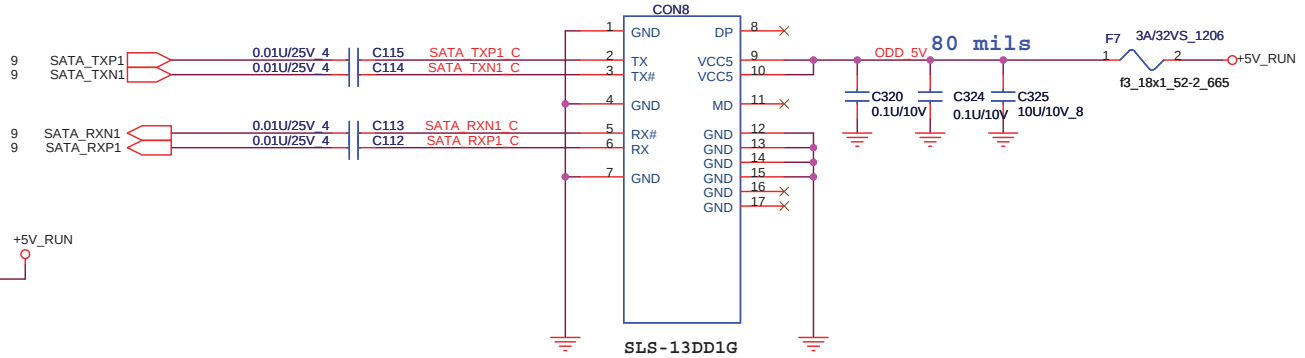
Size	Document Number	Rev
	LAN_RTL8103EL/RJ45	1A
Date: Tuesday, December 08, 2009	Sheet 19 of 45	

REQ by layout

2.5" SATA HDD

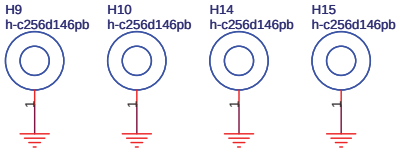


SATA ODD

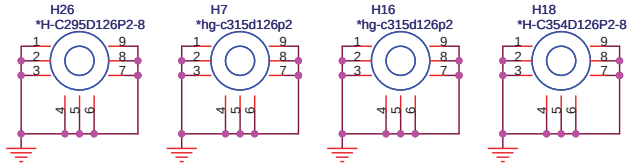


Hole

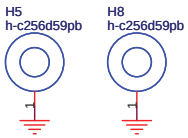
CPU Nut



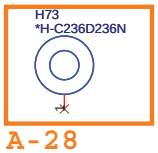
Hole for ESD

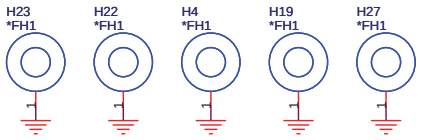


MINI CARD



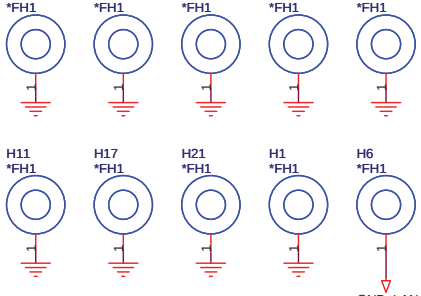
Antenna Hole





Thermal Module

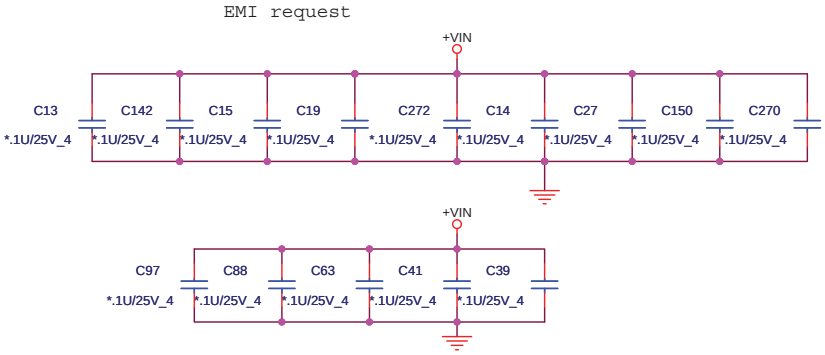
VGA Nut



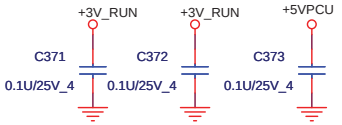
Fan Hole

A-17

Decoupling Cap



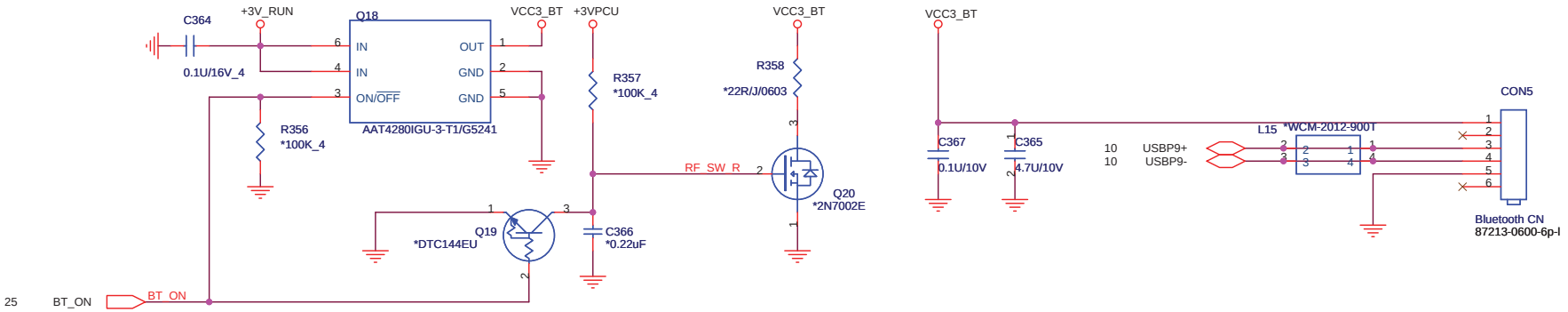
EMI(Decoupling Cap)



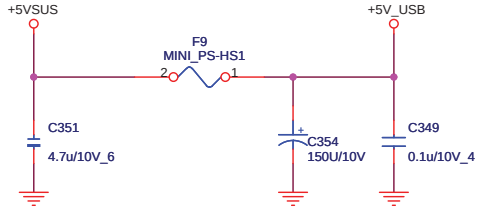
Quanta Computer Inc.
PROJECT : FH1A

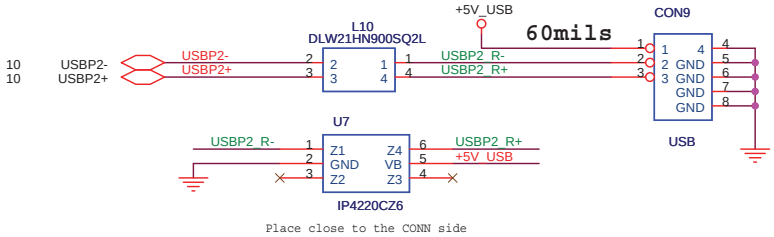
Size	Document Number	Rev
	HDD/ ODD/HOLE	1A
Date: Tuesday, December 15, 2009	Sheet 20 of 45	

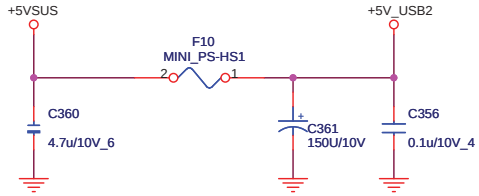
BuleTooth (BTM)

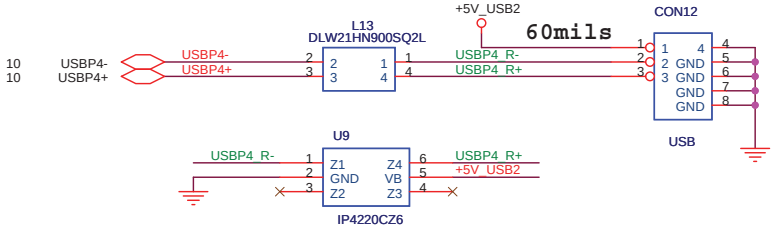


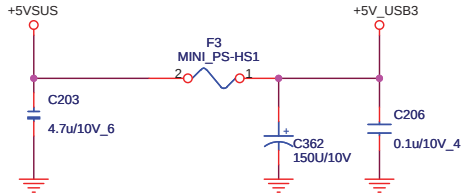
USB Connector

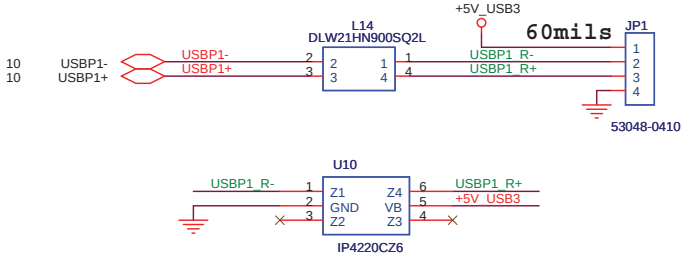










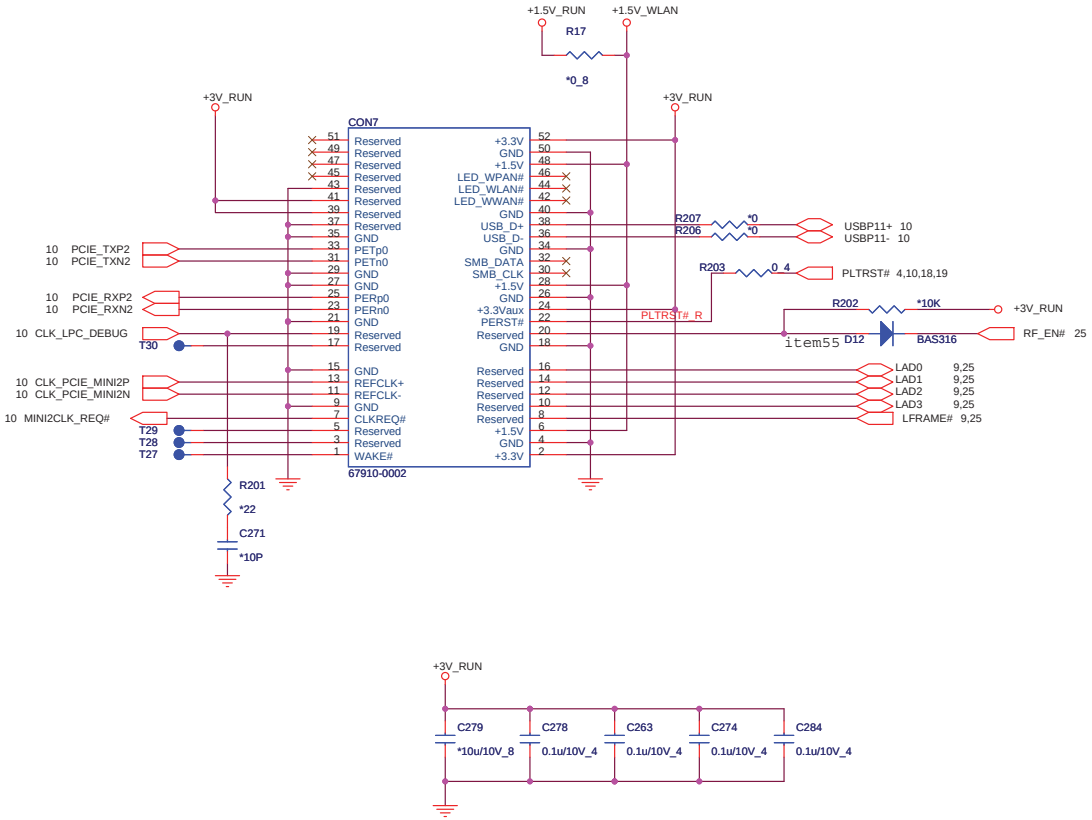


Quanta Computer Inc.

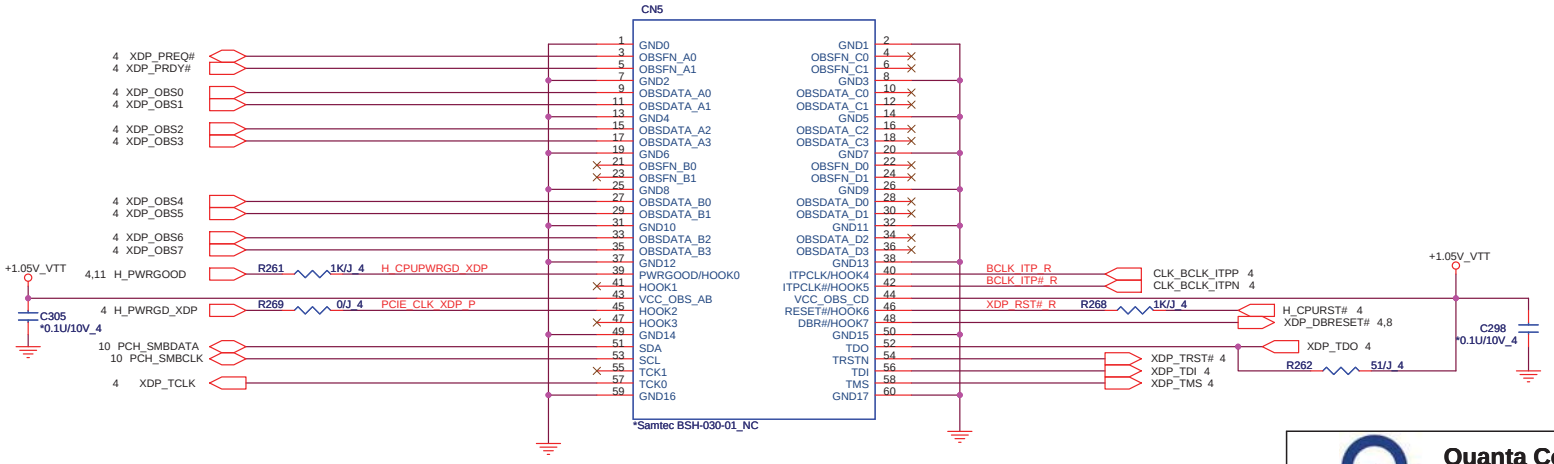
PROJECT : FH1A

Size	Document Number	Rev
	USB/BLUE TOOTH	1A
Date: Monday, December 07, 2009	Sheet 21 of 45	

MINI CARD (WLAN)



XDP



It is for debug. requesst vendeer provide 200 pcs sample.

Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	MINI CARD(WLAN)/XDP	1A

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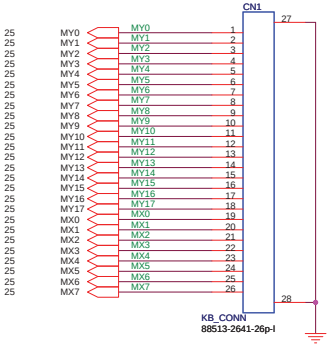
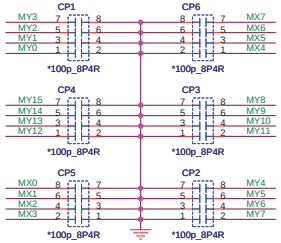
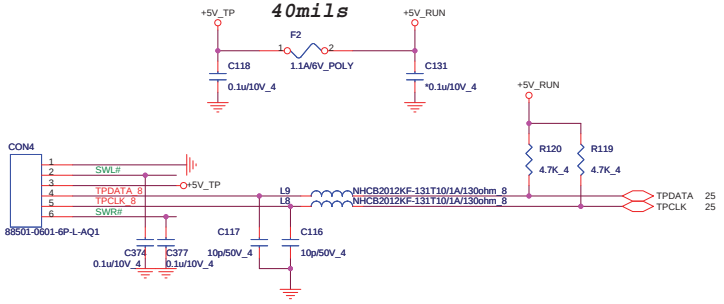
Keyboard(KBC)

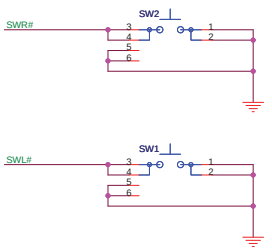


For EMI Reserve Caps for debug

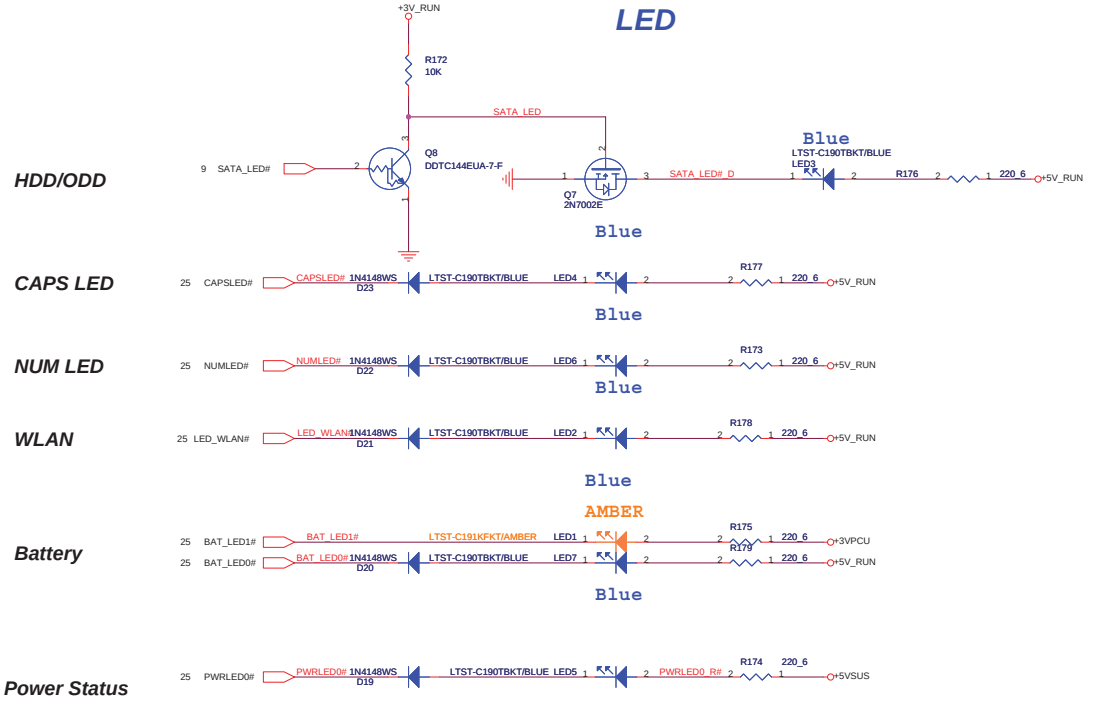


Touch Pad





LED



Quanta Computer Inc.	
PROJECT : FH1A	
Size	Document Number: KB/TOUCH PAD/LED — Rev: 1A
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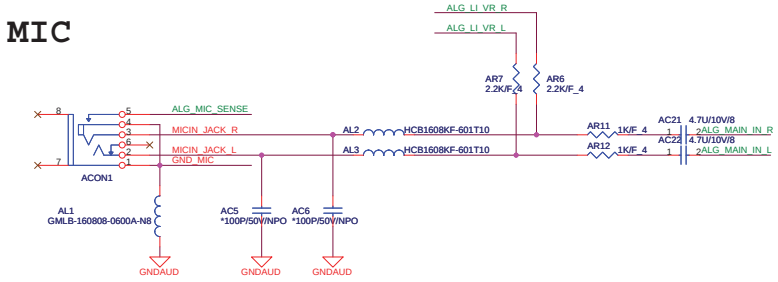
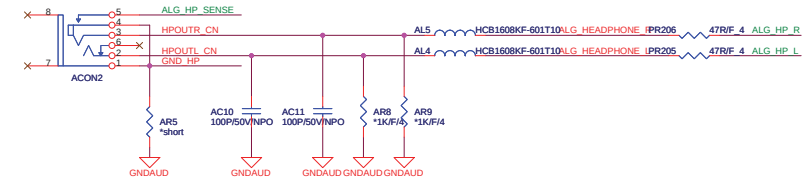
Codec ALC269 A-18

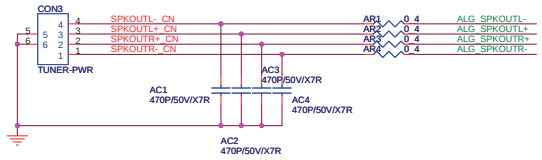
MIC



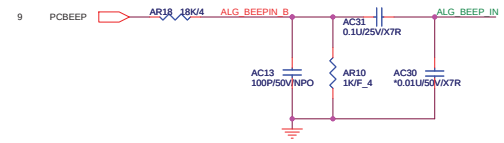
HP



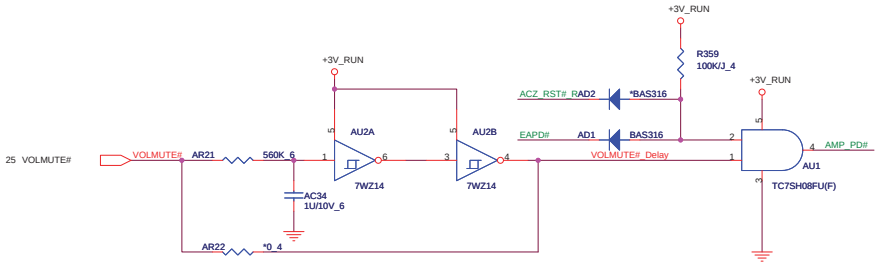
SPKR



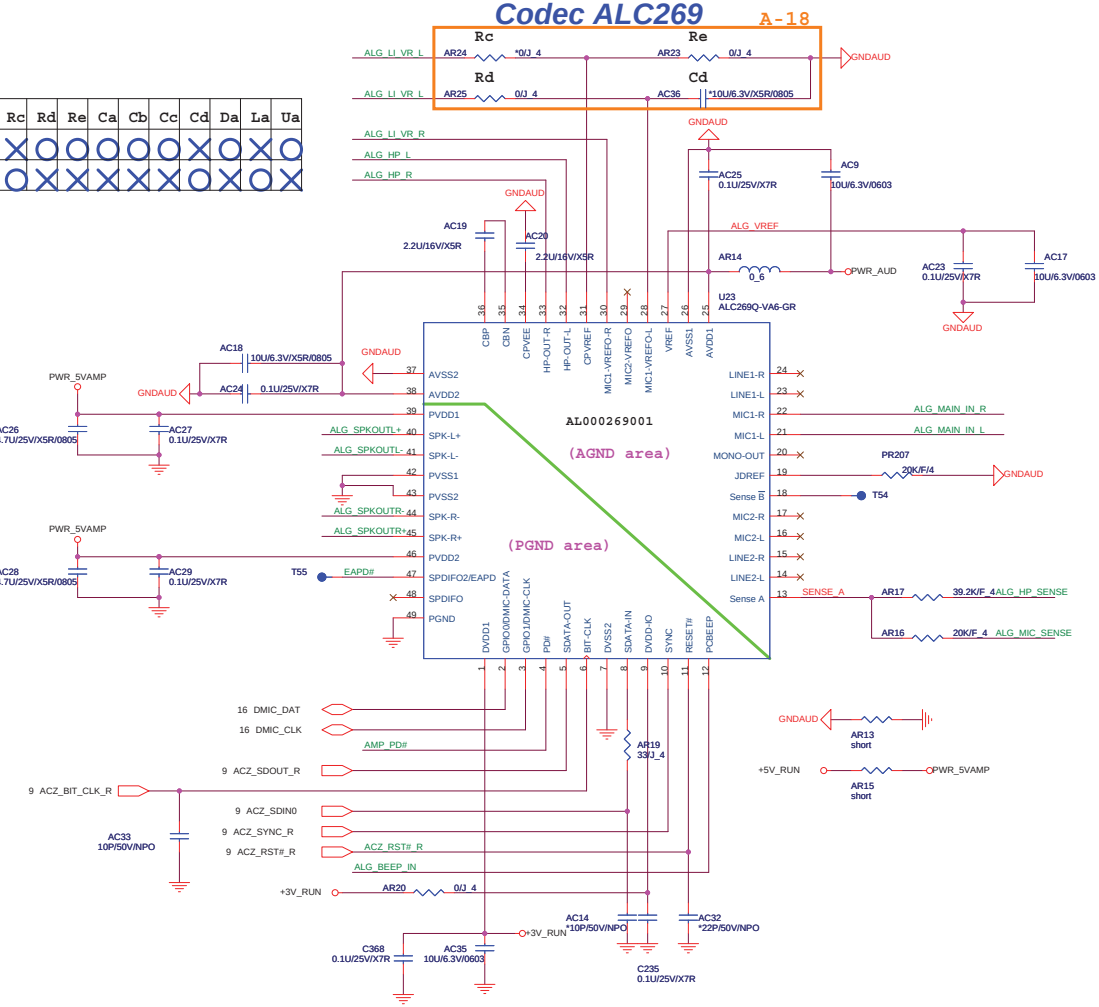
BEEP

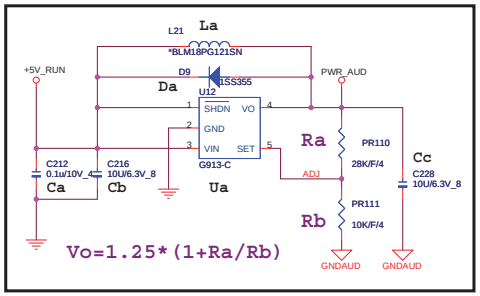


VOLMUTE

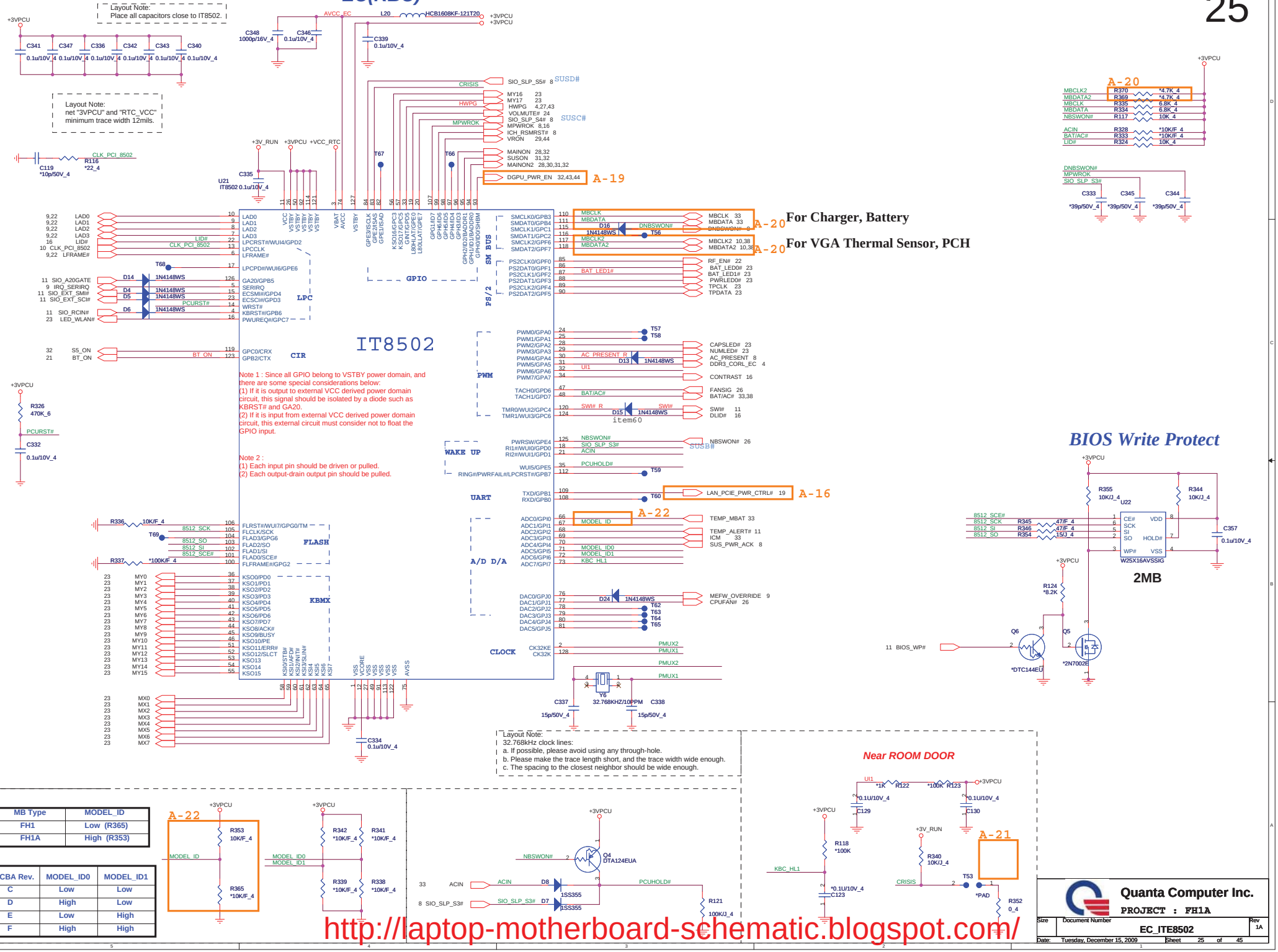


U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X





EC(KBC)



MB Type	MODEL_ID
FH1	Low (R365)
FH1A	High (R353)

PCBA Rev.	MODEL_ID0	MODEL_ID1
C	Low	Low
D	High	Low
E	Low	High
F	High	High

Quanta Computer Inc.
PROJECT : FH1A
Size | Document Number | Rev
EC_ITE8502 | 1A
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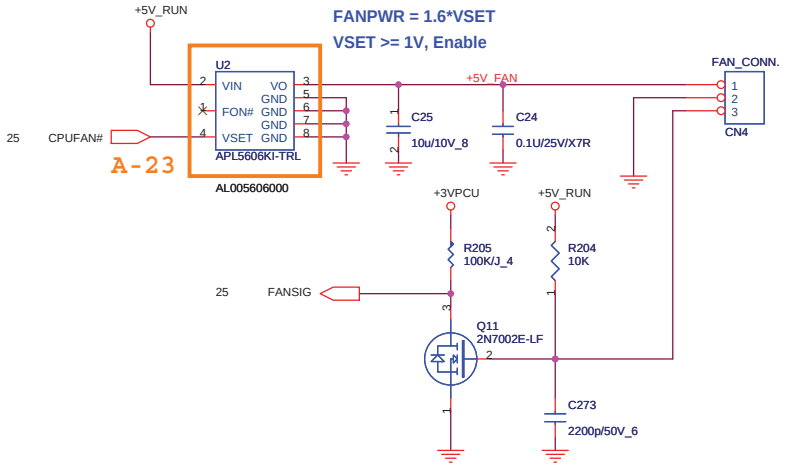
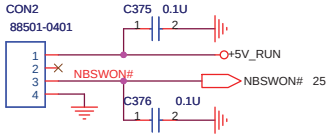
CPU FAN CTRL



SW BOARD CON



Quanta Computer Inc.
PROJECT : FH1A

Size	Document Number	Rev
	FAN/SW CON	1A
Date: Tuesday, December 15, 2009	Sheet 26 of 45	

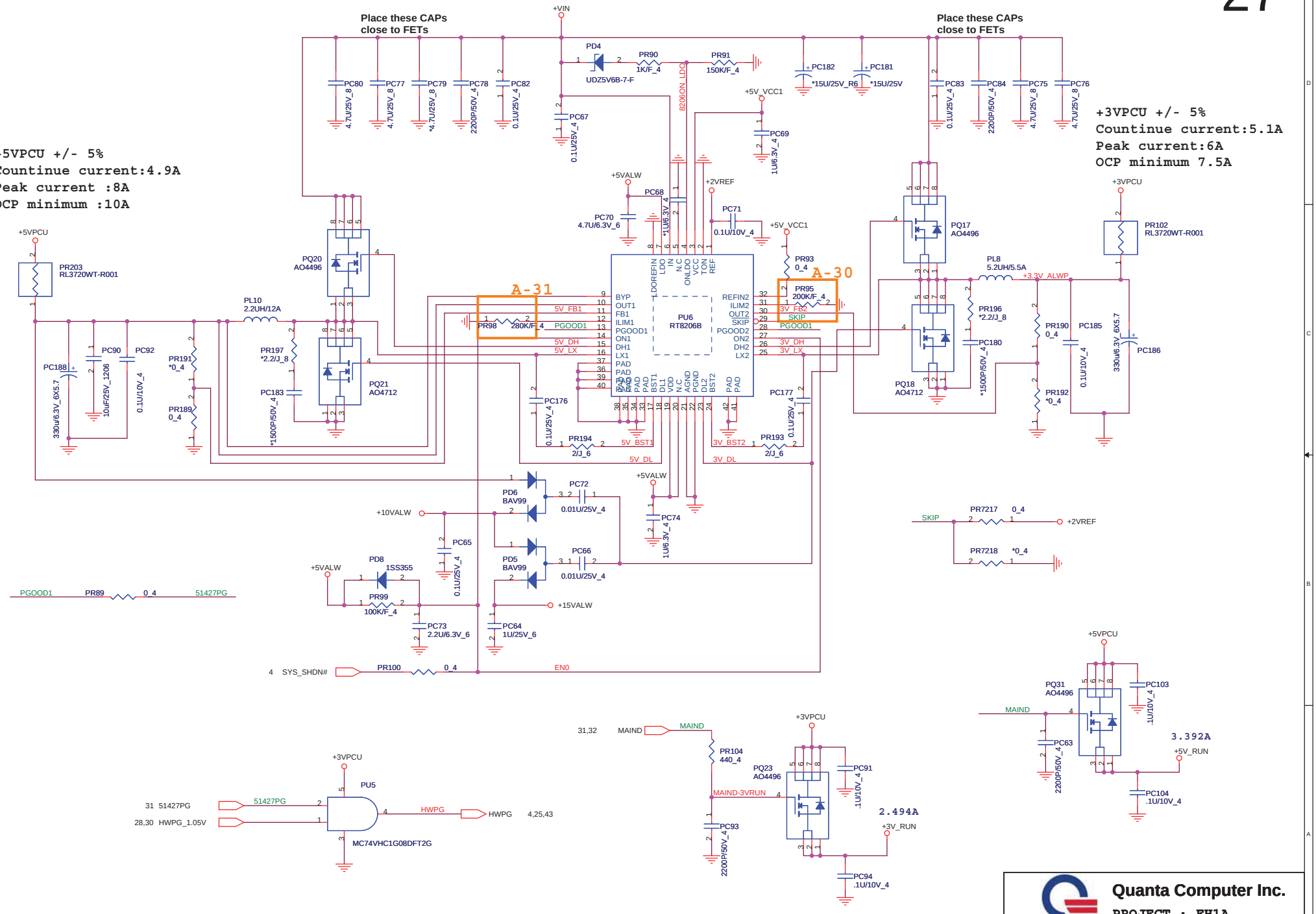
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5VPCU +/- 5%
Countinue current:4.9A
Peak current :8A
OCP minimum :10A

+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A

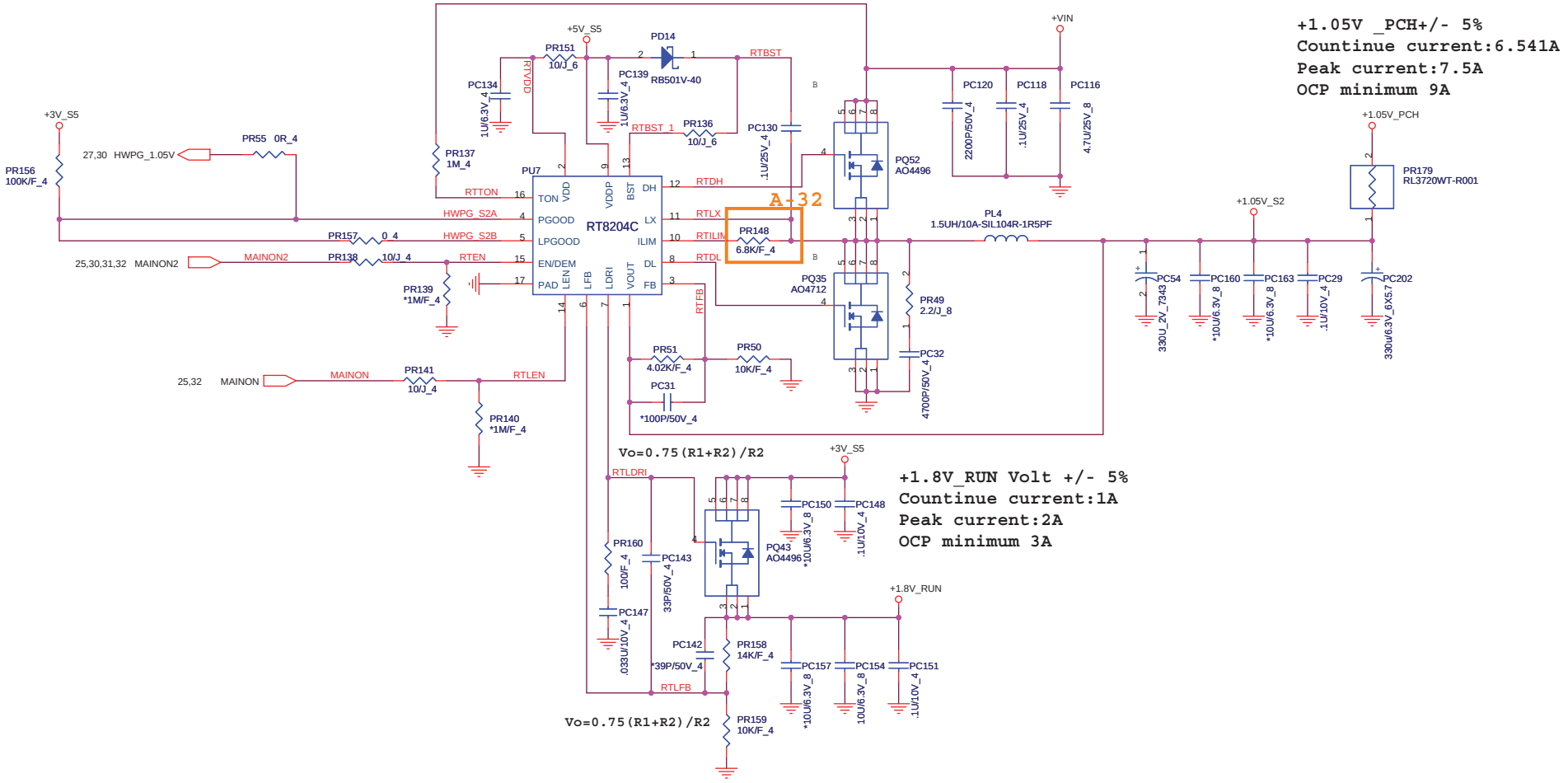
Place these CAPs close to FETs

Place these CAPs close to FETs



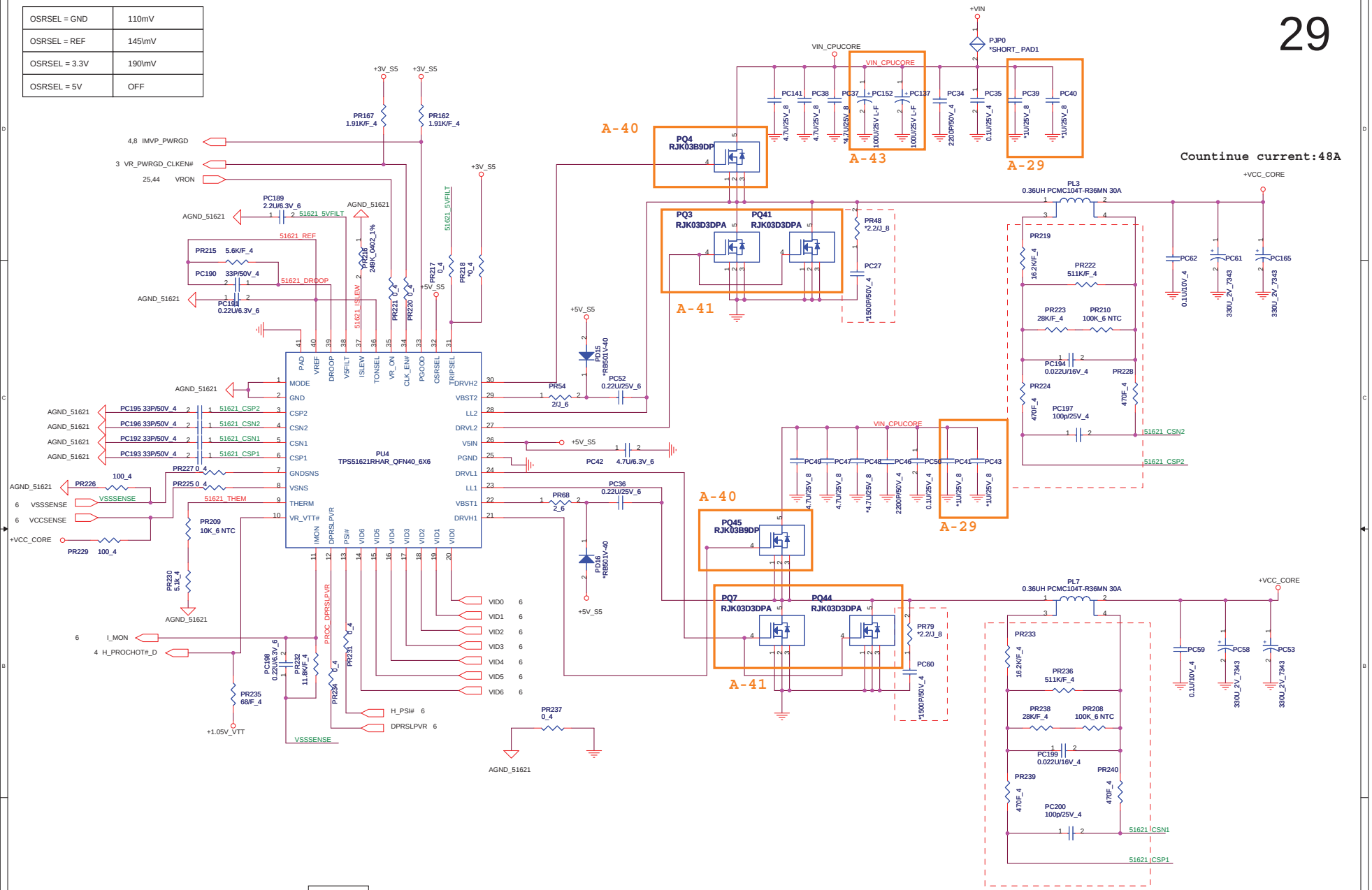
Quanta Computer Inc.
PROJECT : FH1A

Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
Date: Friday, December 11, 2009	Sheet 27 of 45	



OSRSEL = GND	110mV
OSRSEL = REF	145\mV
OSRSEL = 3.3V	190\mV
OSRSEL = 5V	OFF

Countinue current:48A

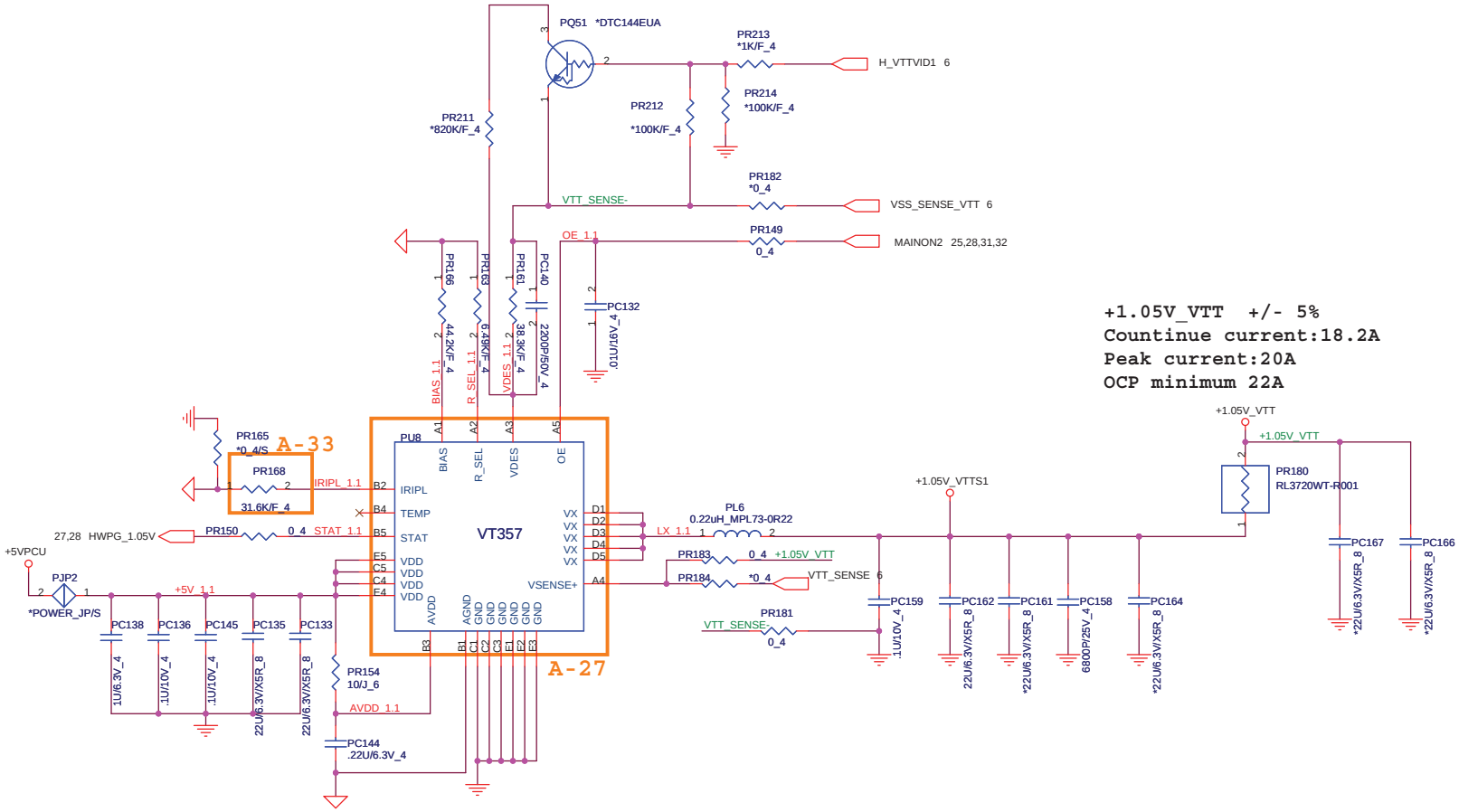


VID
VID5=1 VID4=0 VID3=0

Quanta Computer Inc.

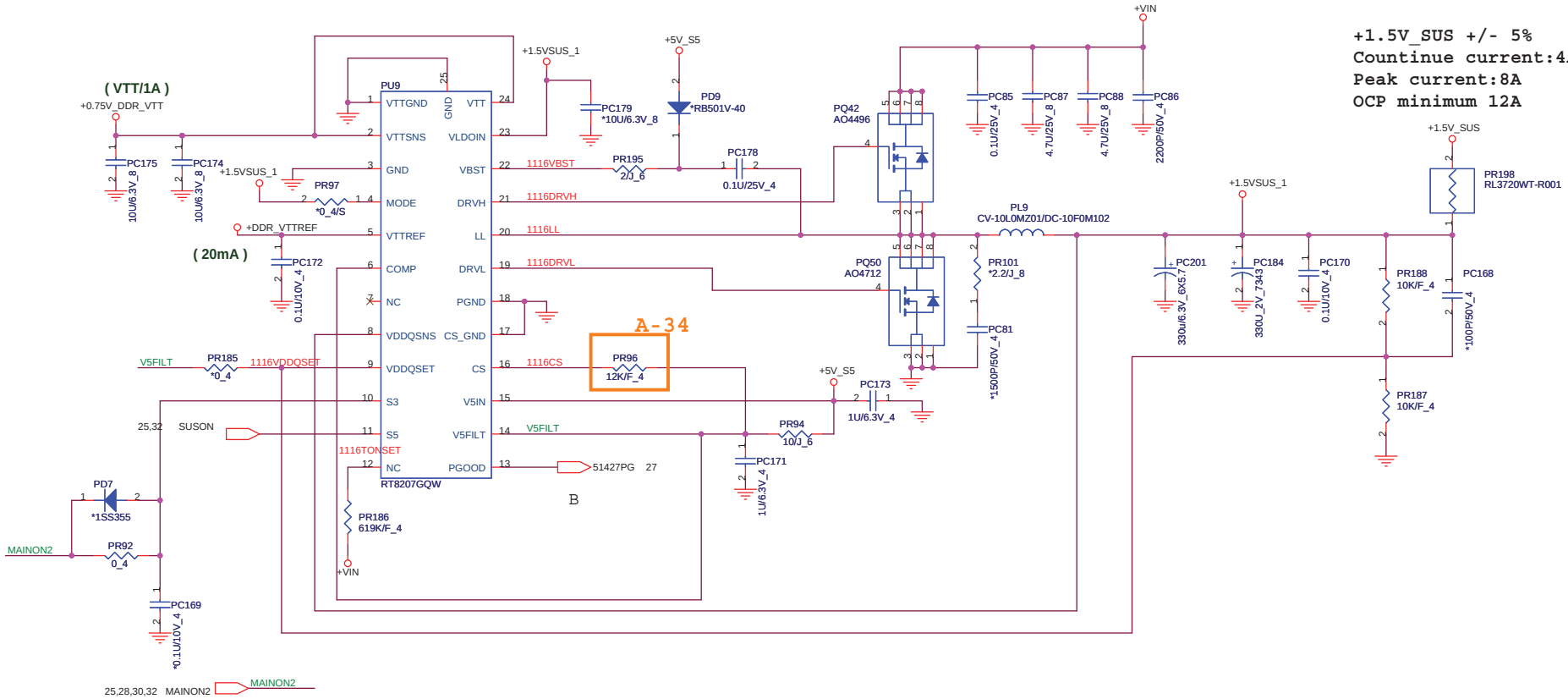
PROJECT : FH1A

Size	Document Number	Rev
	CPU Core (TPS51621)	1A
Date: Monday, December 14, 2009	Sheet 29 of 45	

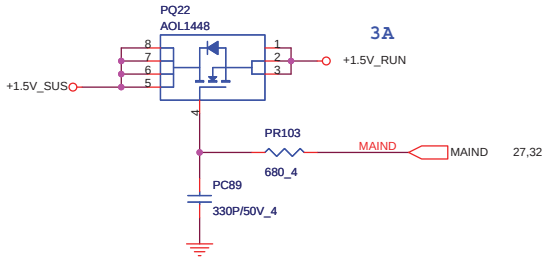


Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: +1.05V_VTT (VT358)	Rev: 1A
Date: Friday, December 11, 2009	Sheet 30 of 45	

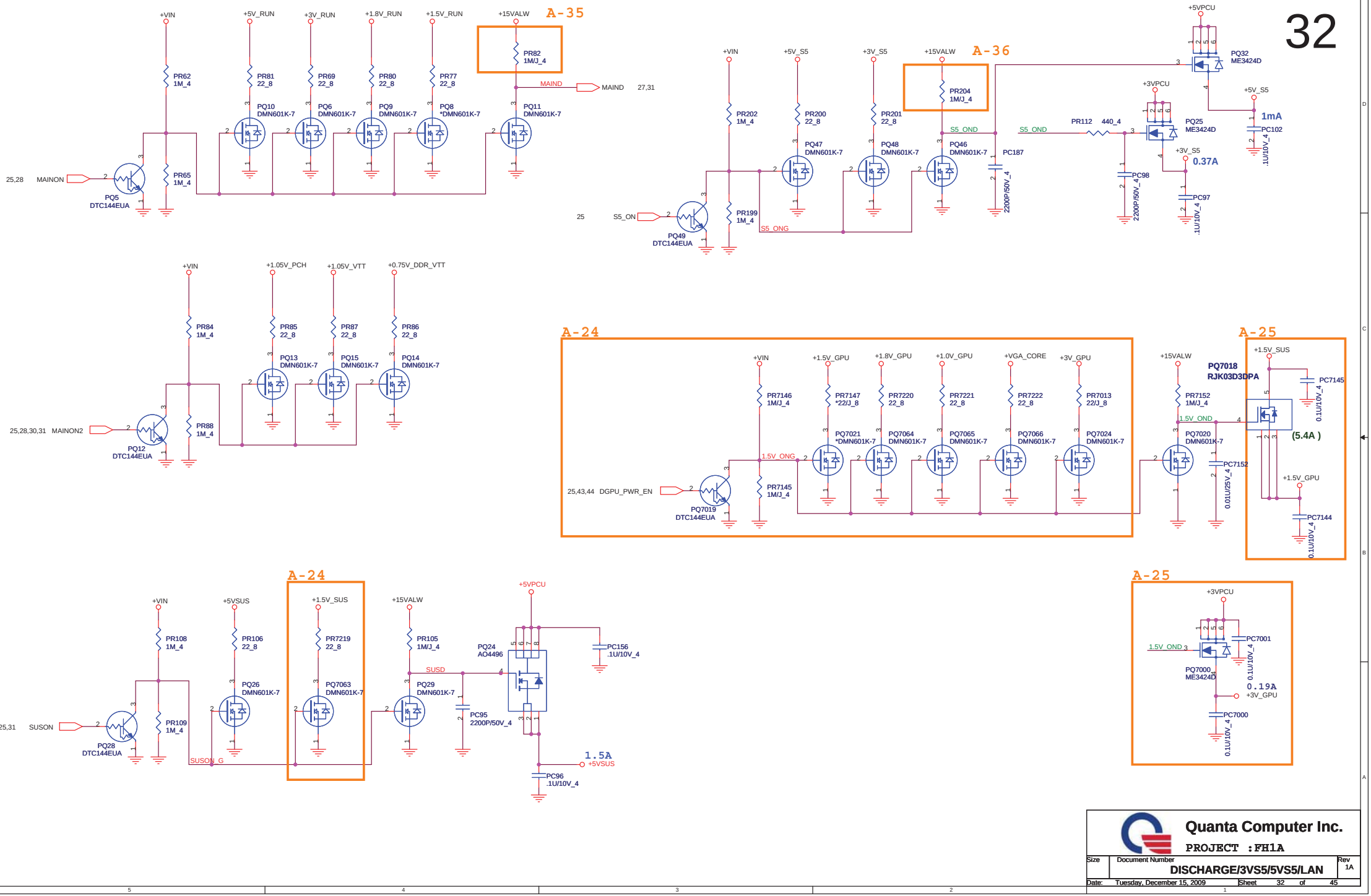
+1.5V_SUS +/- 5%
Countinue current:4A
Peak current:8A
OCP minimum 12A



DIS_MODE
Tracking discharge : VDDQ
Non tracking discharge : GND
No discharge : VCC5



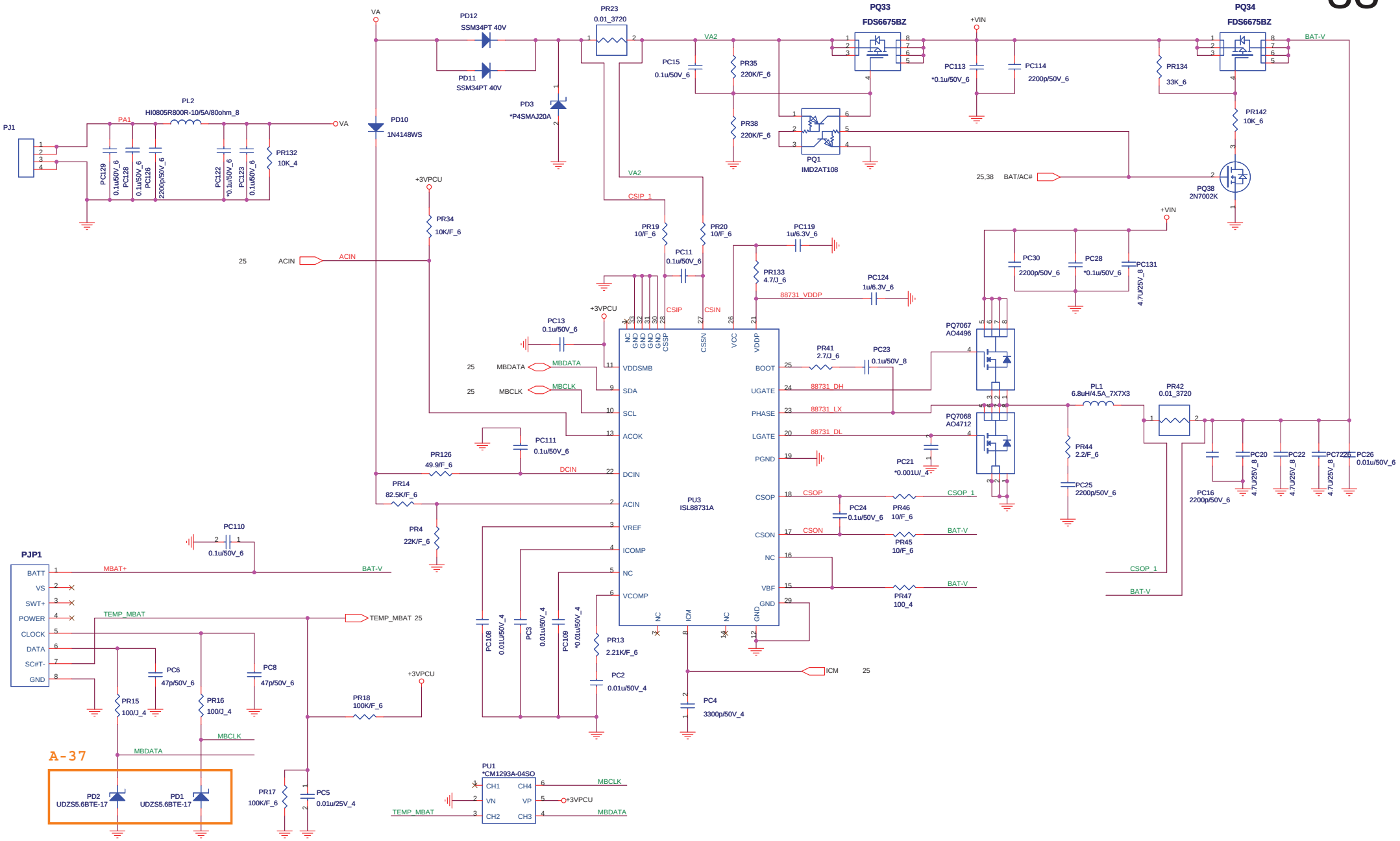
Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Friday, December 11, 2009	Sheet 31 of 45	

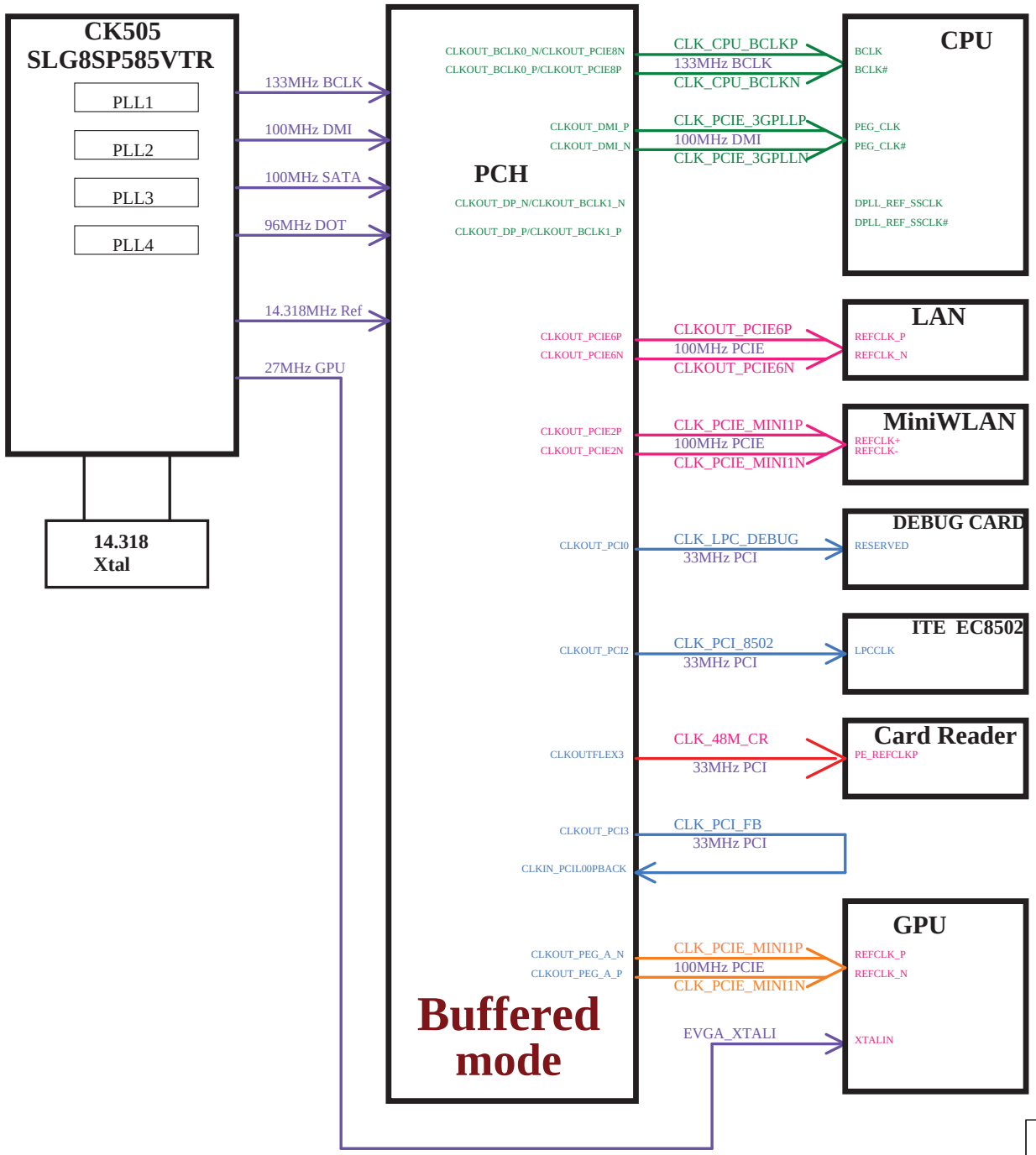


Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Tuesday, December 15, 2009	Sheet 32 of 45	





Quanta Computer Inc.

PROJECT : FH1A

Size: Document Number: Clock Distribution Rev 1A

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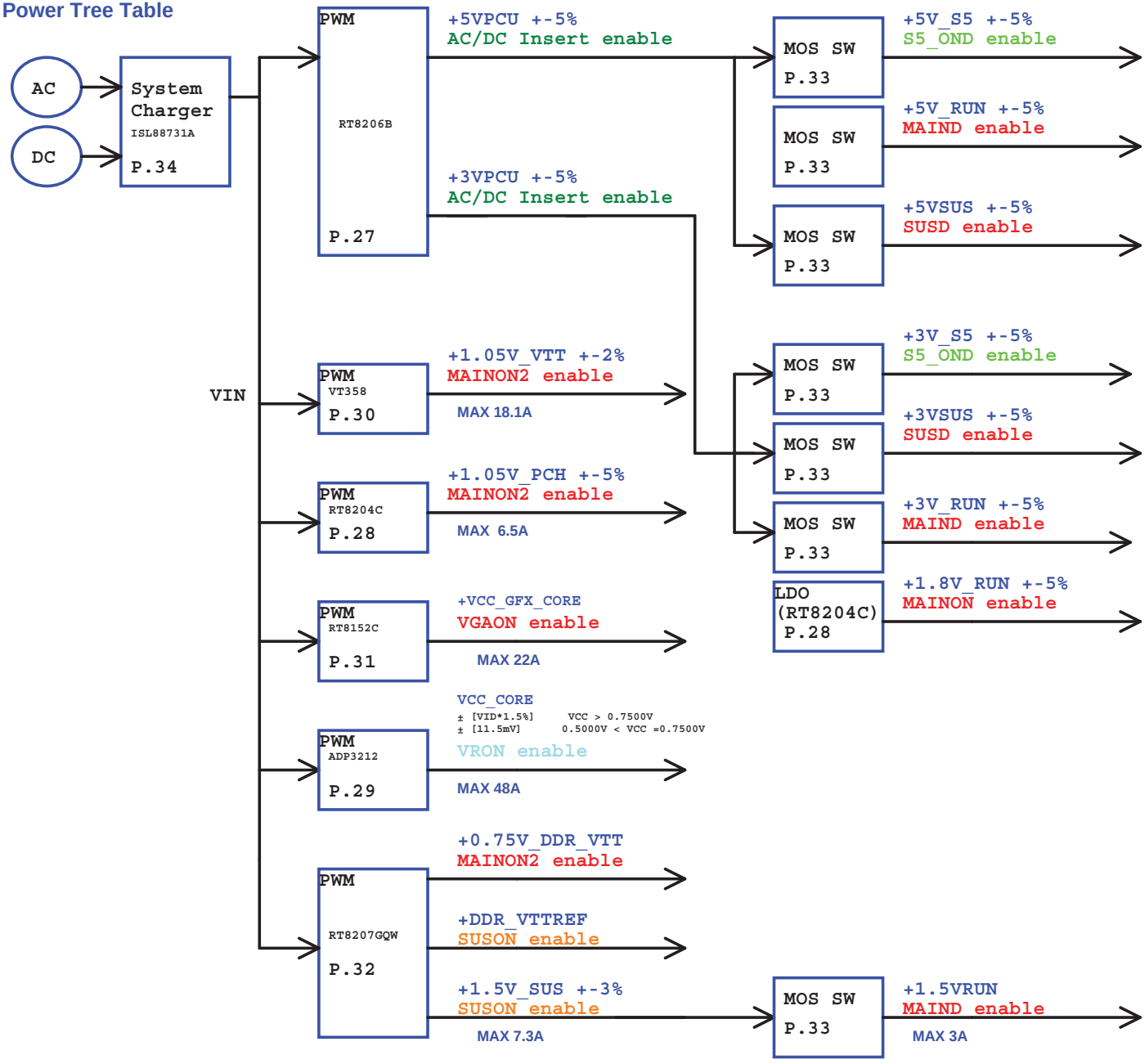
Power Tree Table



Quanta Computer Inc.
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Power Tree
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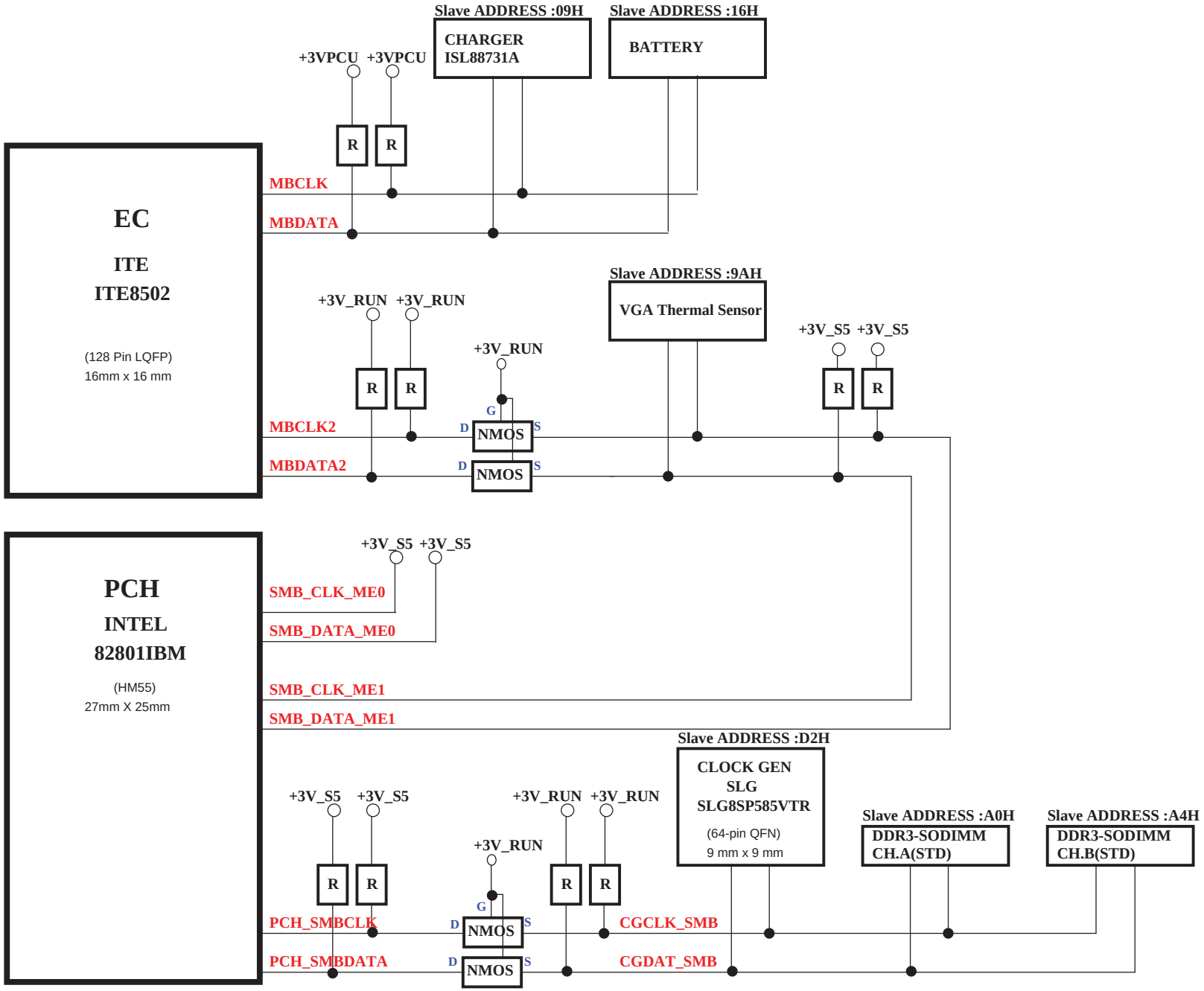

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	SM BUS	1A
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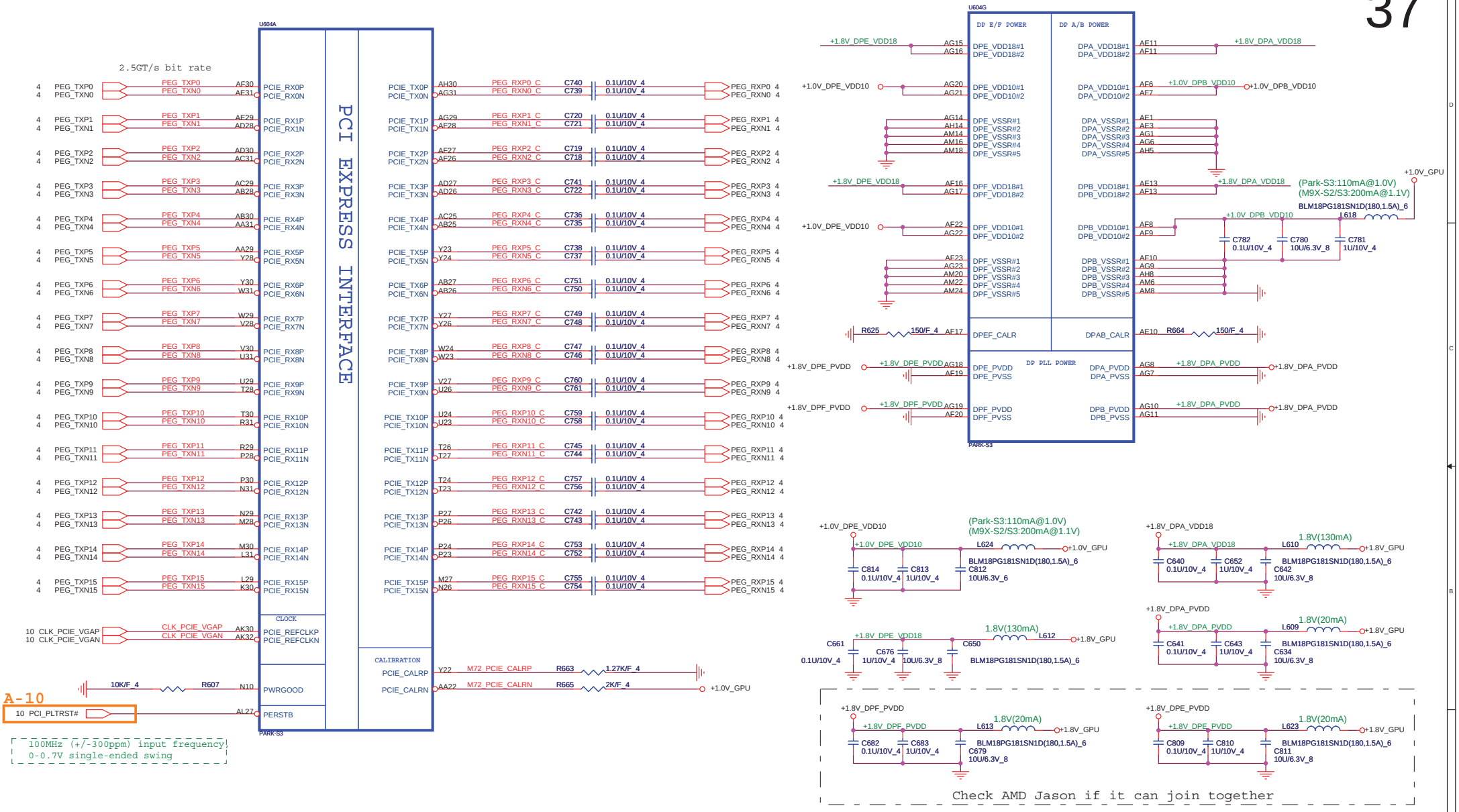

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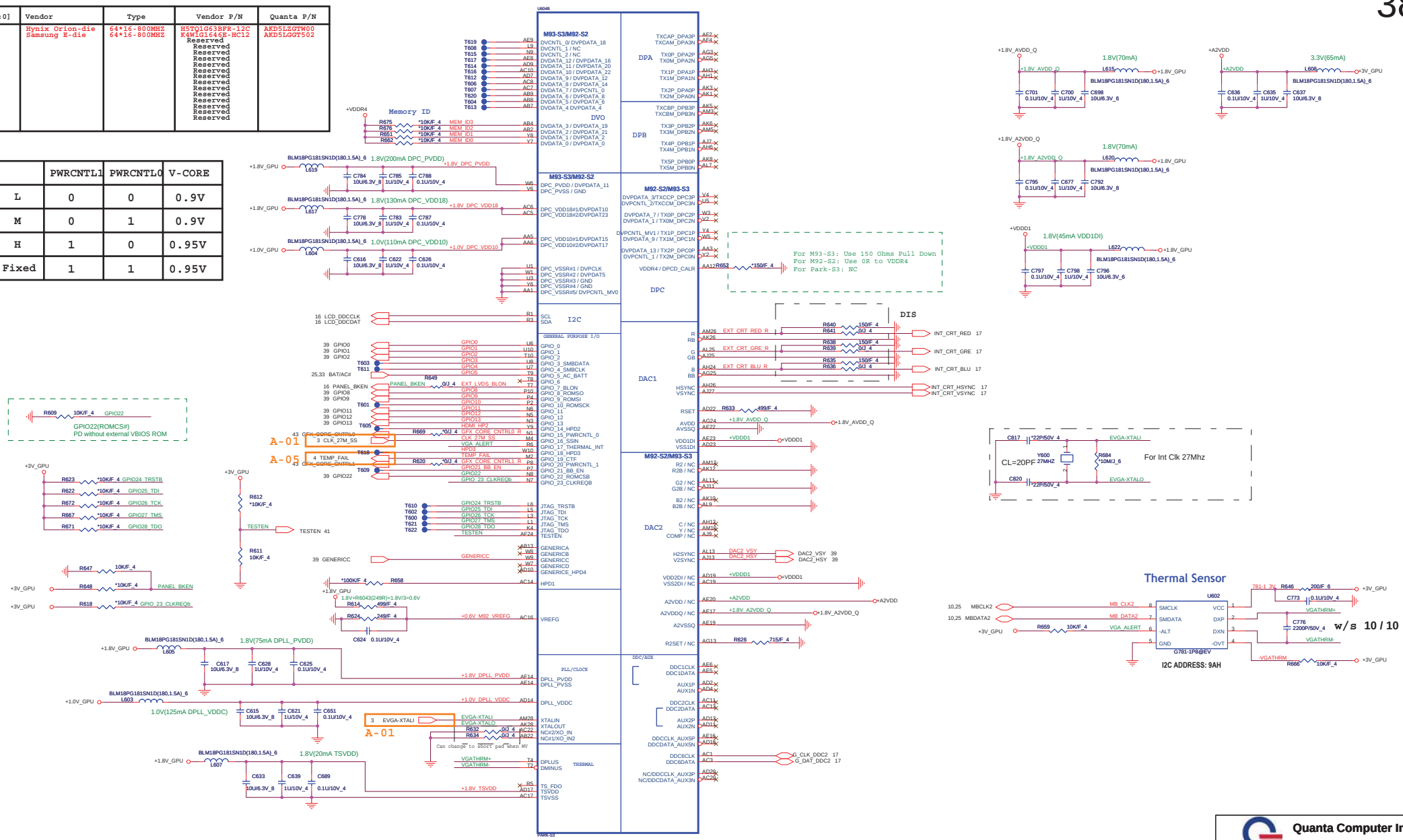
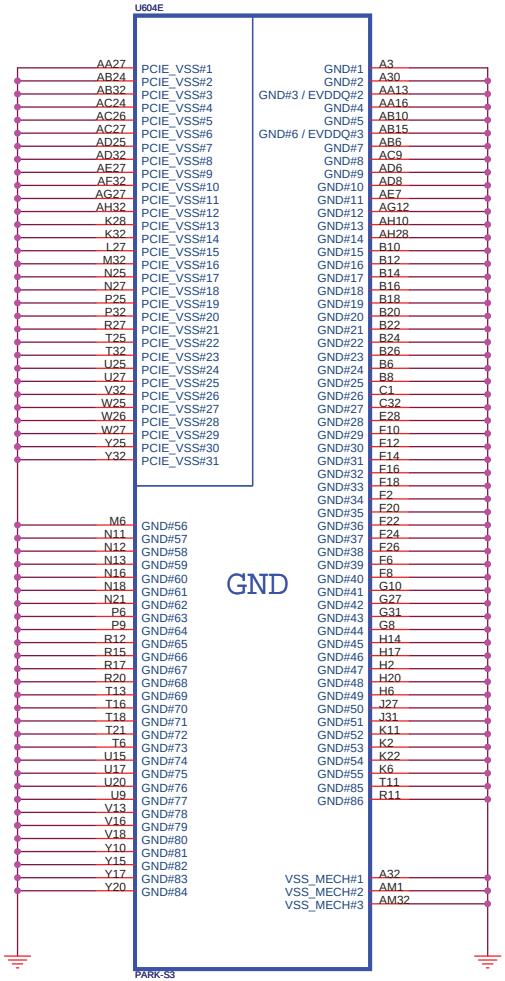
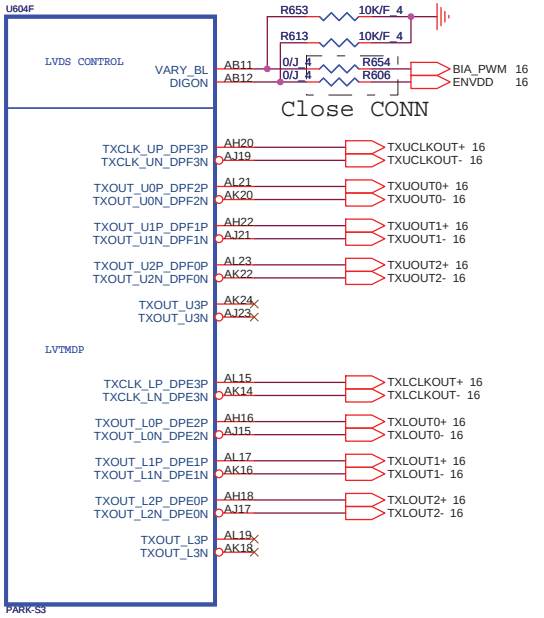
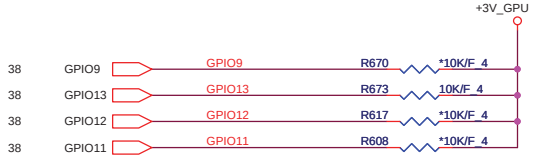
MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	AKD5LZGTW00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010			Reserved	
0011			Reserved	
0100			Reserved	
0101			Reserved	
0110			Reserved	
0111			Reserved	
1000			Reserved	
1001			Reserved	
1010			Reserved	
1011			Reserved	
1100			Reserved	
1101			Reserved	
1110			Reserved	
1111			Reserved	

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V









CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

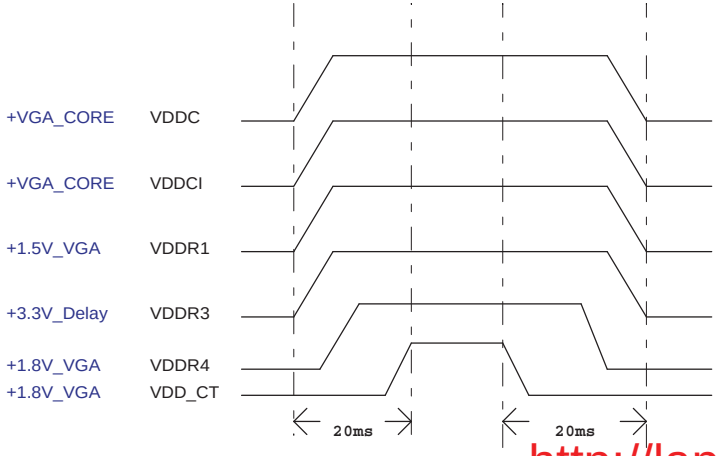
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

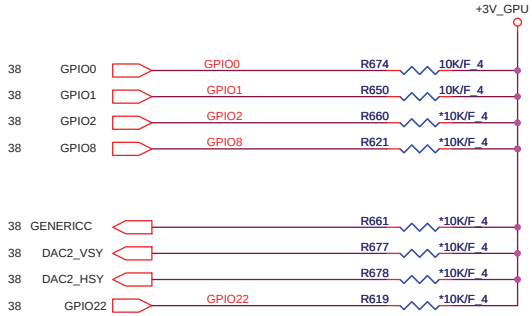
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



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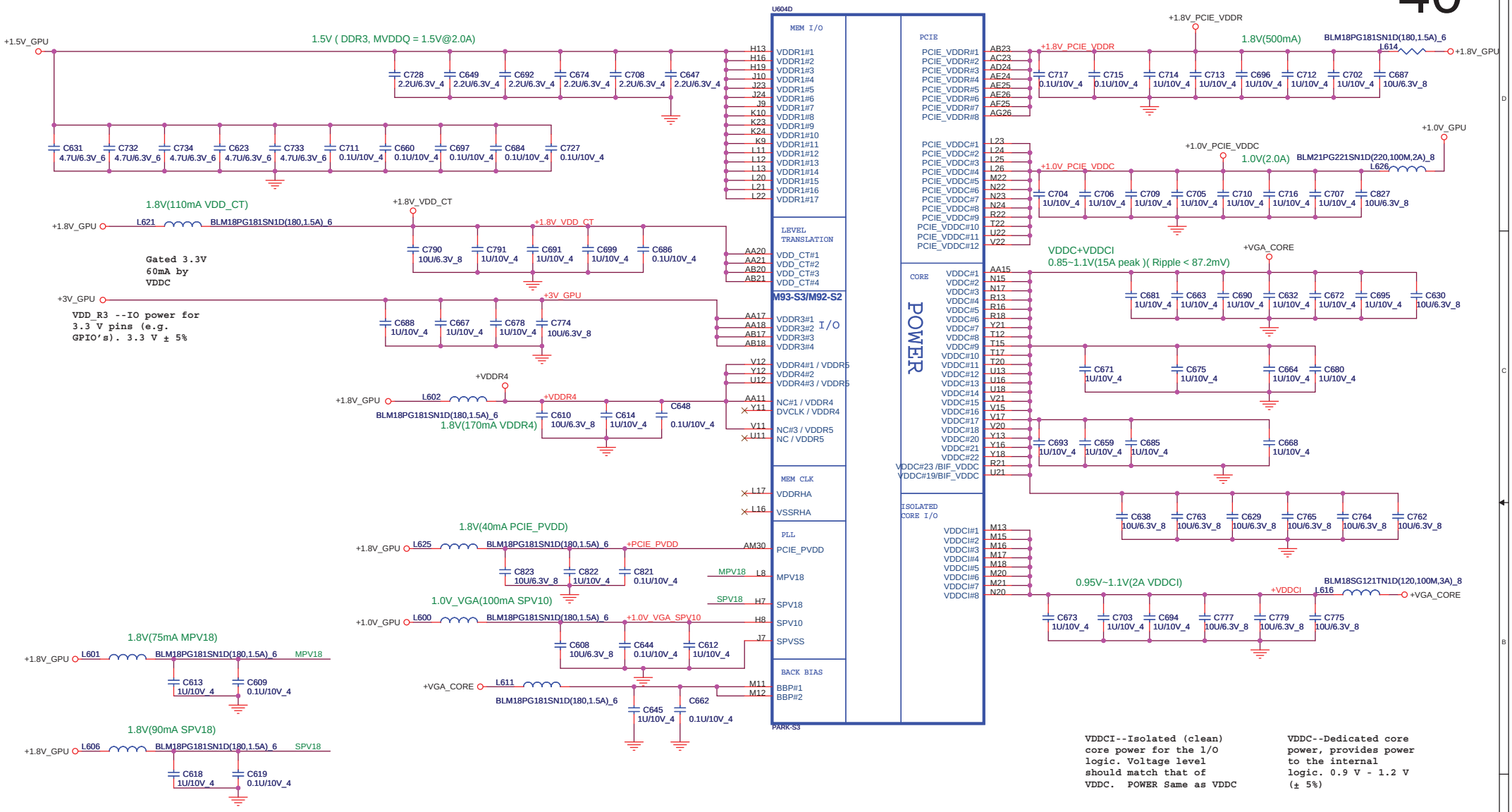
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



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	PARK_Power_and_NC	1A
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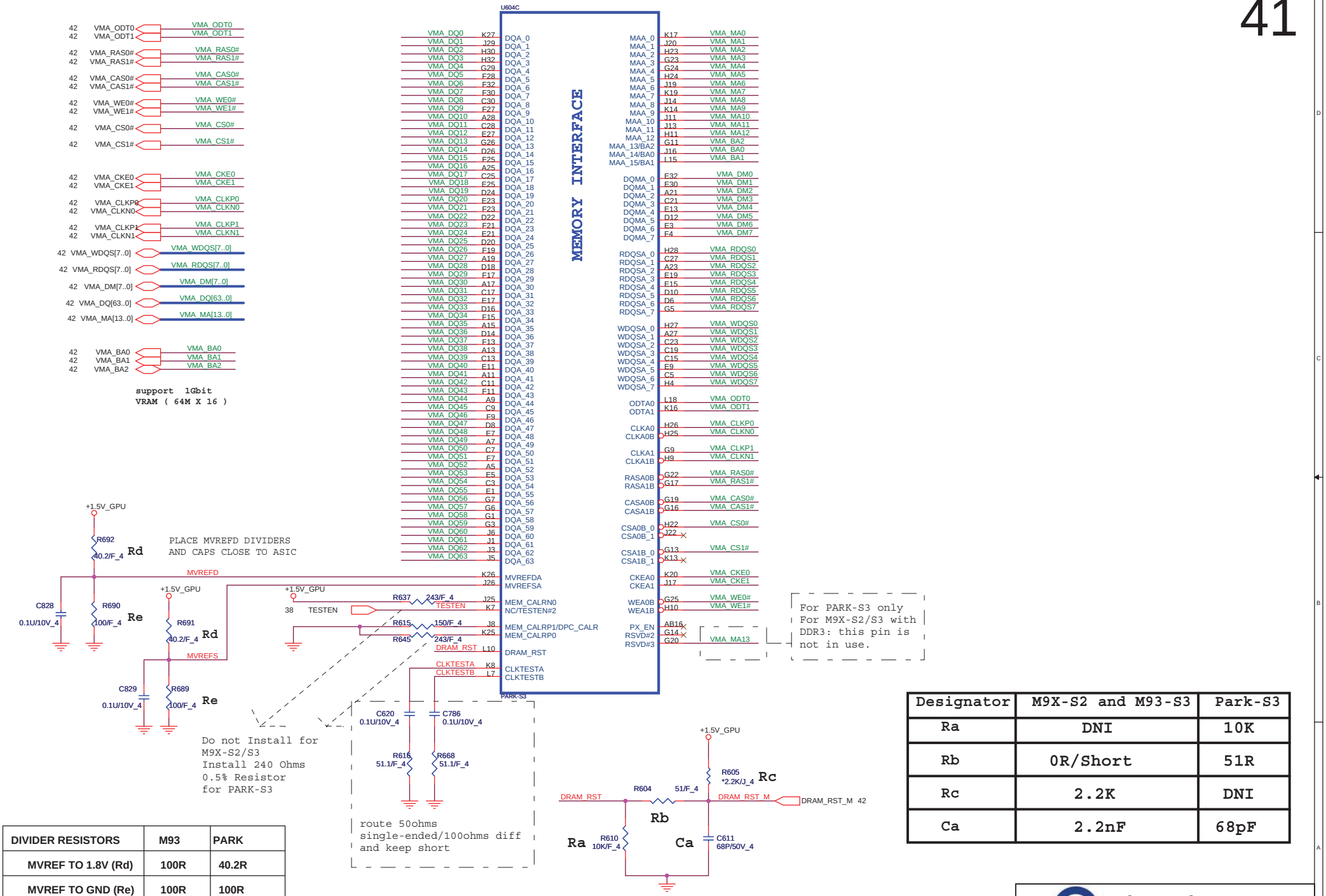

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

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	PARK/MEM_Interface	1A

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512MB DDR3

41 VMA_MA[13..0]
41 VMA_DM[7..0]
VMA_MA[13..0]
VMA_DM[7..0]

41 VMA_DQ[63..0]
41 VMA_WDQS[7..0]
41 VMA_RDQS[7..0]
VMA_DQ[63..0]
VMA_WDQS[7..0]
VMA_RDQS[7..0]

U601 / U605 / U600 / U603

H5TQ1G63BFR-12C

100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R642 243/F_4
R679 243/F_4
R629 243/F_4
R655 243/F_4

+1.5V_GPU

R685 4.99K/F_4
R686 4.99K/F_4
C824 0.1U/10V_4
R631 4.99K/F_4
R630 4.99K/F_4
C653 0.1U/10V_4
R683 4.99K/F_4
R682 4.99K/F_4
C808 0.1U/10V_4
R687 4.99K/F_4
R688 4.99K/F_4
C826 0.1U/10V_4
R627 4.99K/F_4
R628 4.99K/F_4
C646 0.1U/10V_4
R602 4.99K/F_4
R603 4.99K/F_4
C601 0.1U/10V_4
R656 4.99K/F_4
R657 4.99K/F_4
C770 0.1U/10V_4
R681 4.99K/F_4
R680 4.99K/F_4
C802 0.1U/10V_4

VREFC_VMA1 VREFD_VMA1 VREFC_VMA2 VREFD_VMA2 VREFC_VMA3 VREFD_VMA3 VREFC_VMA4 VREFD_VMA4

VMA_CLKP0
R644 56/F_4
VMA_CLK0_COMM
C726 0.01U/25V_4
R643 56/F_4
VMA_CLKN0
VMA_CLKP1
R601 56/F_4
VMA_CLK1_COMM
C600 0.01U/25V_4
R600 56/F_4
VMA_CLKN1

C655 C654 C669 C665 C666 C656 C657 C815 1U/6.3V_4
C607 C772 C605 C603 C604 C602 C606 C771 1U/6.3V_4
C793 C789 C794 C670 C769 4.7U/6.3V_6
C803 C804 C801 C658 C800 C816 C805 C806 1U/6.3V_4
C723 C730 C729 C825 C818 C819 C725 C724 1U/6.3V_4
C766 C807 C799 C767 C731 C768 C627 4.7U/6.3V_6

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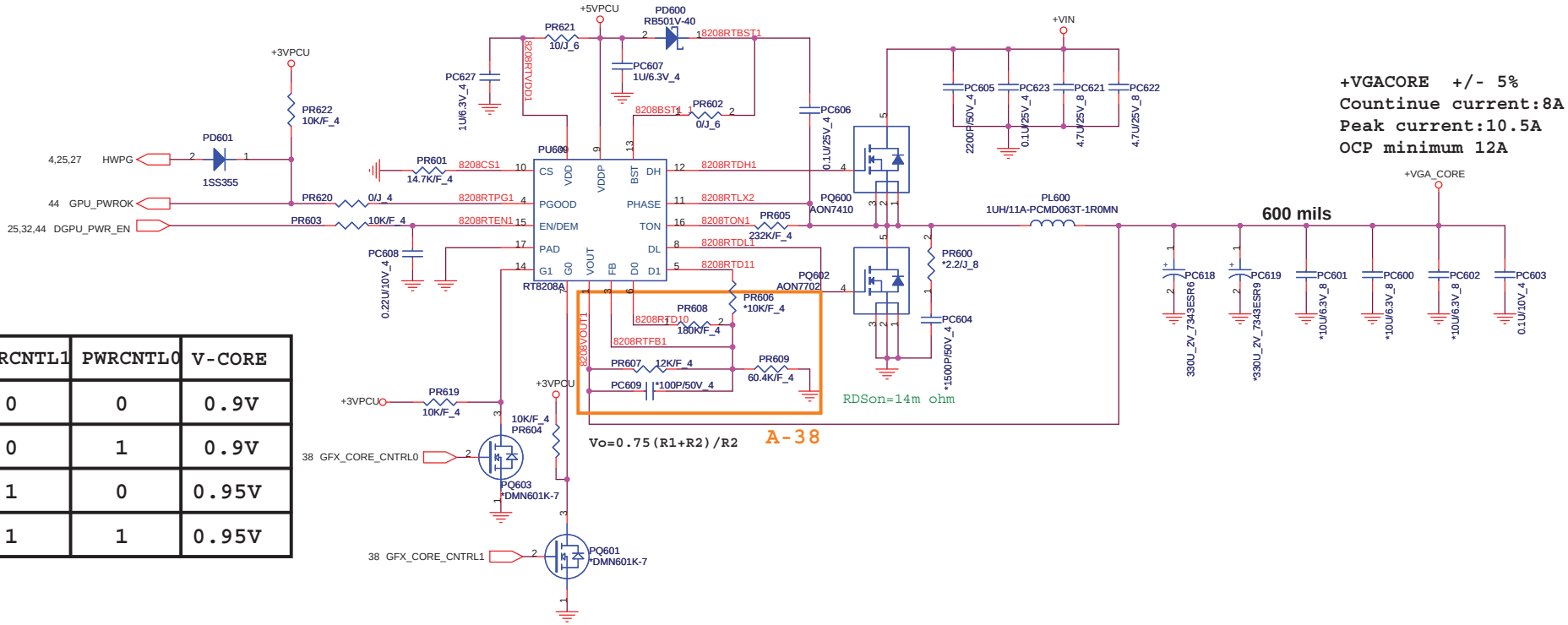
VGA Core



	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V

Quanta Computer Inc.

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	+VGACORE (RT8208/1.8V)	1A
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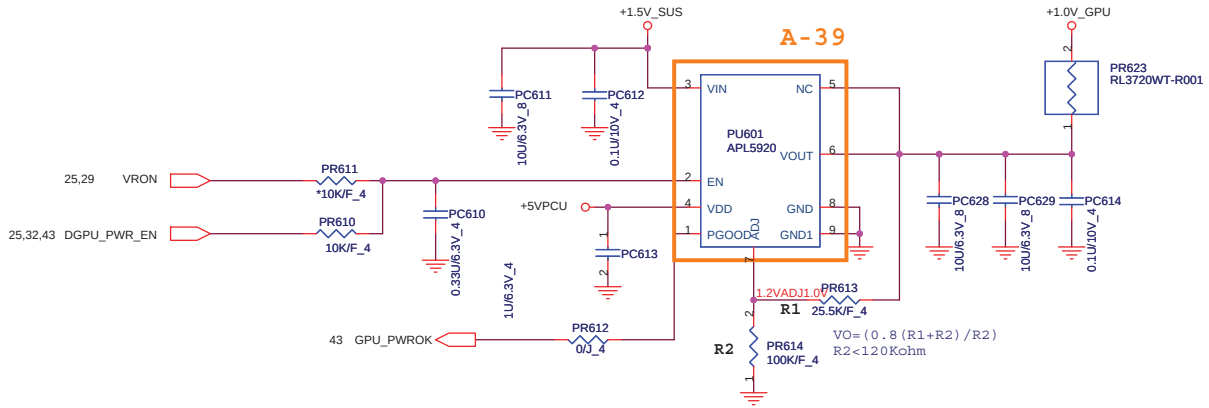
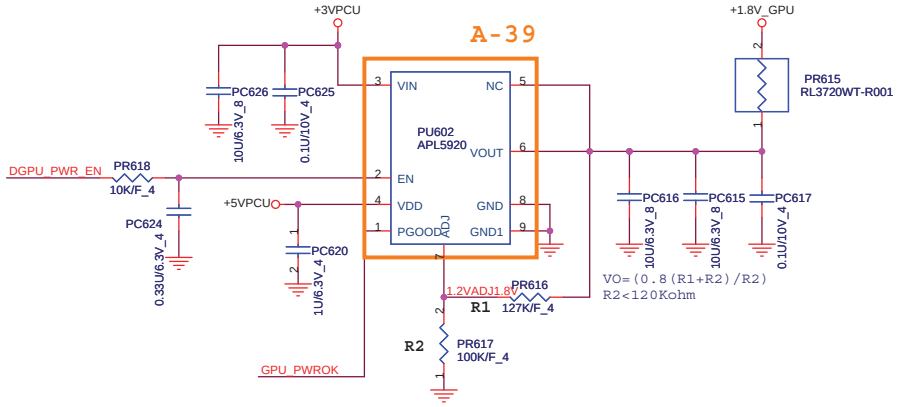
+1.0V +/- 5%
Countinue current:2A
Peak current:3A



+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A



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	DDR3 (RT8207)	1A
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Change List

A-01 PAGE 3,38 : Add EVGA-XTALI and CLK_27M_SS, and stuff R343, nonstuff R416 for providing 27MHz clock.
A-02 PAGE 4,8 : NC FDI_TX[7:0]/FDI_TX#[7:0], and FDI_INT,FDI_FSYNC0/1,FDI_LSYNC0/1 connect to GND for disable UMA setting.
A-03 PAGE 4,37 : Add PEG_RXN[15:0],PEG_RXP[15:0],PEG_TXN[15:0],PEG_TXP[15:0] to connect to Park LP PCIE I/F
A-04 PAGE 4,10 : DPLL_REF_SSCLK/DPLL_REF_SSCLK# pull down and NC in PCH side for Disable UMA setting.
A-05 PAGE 4,38 : Reserve TEMP_FAIL circuit for GPU thermal detect signal control.
A-06 PAGE 6 : VAXG_SENSE,VSSAXG_SENSE,GFX_VID[6:0],GFX_VR_EN,GFX_DPRSLPVR to be NC, VAXG connect to GND, and IMON pull down via R220 10Kohm for Disable UMA
A-07 PAGE 8 : LVDS/CRT signals in PCH side to be NC
A-08 PAGE 9 : RTC Battery Connect CON11 change from Cable type to Socket type(PN : DFHS02FS027)
A-09 PAGE 9,26 : Remove MDC circuit
A-10 PAGE 10,37 : PCI_PLTRST# connect to Park LP PinAL23
A-11 PAGE 10 : Change U4 from OR gate to AND gate
A-12 PAGE 10 : Add PU resistors R468,R469 2.2Kohm
A-13 PAGE 10 : Stuff R211 and Nonstuff Y4,R210,C282,C283
A-14 PAGE 12 : VCCADAC0/1 connecto to +3V_RUN and VSSA_DAC0/1 connect to GND for Disable UMA setting
A-15 PAGE 12 : VCCALVDS,VCCTX_LVDS[4:1] connect to GND, and VSSA_LVDS to be NC for Disable UMA setting
A-16 PAGE 19,25 : Reserve R565 and D27, and Add control signal LAN_PCIE_PWR_CTRL# for LAN Power Saving Control
A-17 PAGE 20 : Delete H13,H20
A-18 PAGE 24 : Add AR23,AR24,AR25,AC36 for ALC269 VA and VB version control
A-19 PAGE 25,32,43,44 : Add Contorl Signal DGPU_PWR_EN to control +VGA_CORE,+3V_GPU,+1.8V_GPU,+1.5V_GPU,+1.0V_GPU Power On/Off
A-20 PAGE 10,25,33,38 : SMBCLK/SMBDATA for Charger and Battery SMBus signals, and SMBCLK2/SMBDATA2 for VGA Thermal Sensor and PCH SMBus signals.
A-21 PAGE 25 : Delete R353
A-22 PAGE 25 : Add MODEL_ID signal to U21 Pin67, and stuff PU resistor R353 10Kohm for MODEL selection
A-23 PAGE 16,26 : Change Fan Controller U2 P/N, and Change LVDS LDO U14 P/N
A-24 PAGE 32 : Add VGA Power and +1.5V_SUS Discharge Circuit
A-25 PAGE 32,43,44 : Add +VGA_CORE,+3V_GPU,+1.5V_GPU,+1.8V_GPU,+1.0V_GPU circuits for Park LP Power
A-26 PAGE 37~42 : Add Park LP circuits
A-27 PAGE 30 : Change PU8 footprint
A-28 PAGE 20 : Add VGA thermal Nut H29, Fan Hole H74 and Modify H12 footprint
A-29 PAGE 29 : Reserve PC39,PC40,PC41,PC43 1uF for Power On/Off Fail issue(Battery Capacity less than 60%)
A-30 PAGE 27 : Change PR95 from 180K to 200K
A-31 PAGE 27 : Change PR98 from 237K to 280K
A-32 PAGE 28 : Change PR148 from 5.1K to 6.8K
A-33 PAGE 30 : Change PR168 from 40.2K to 31.2K
A-34 PAGE 31 : Change PR96 from 10.2K to 12K
A-35 PAGE 32 : Change PR82 from 560 to 1M
A-36 PAGE 32 : Change PR204 from 560 to 1M
A-37 PAGE 33 : Change PD1 & PD2 from ZD3.6V to UDZS5.6BTE-17
A-38 PAGE 43 : Change PR7077 from 10K to 60K, PR7080 from 2K to 12K and PR7095 from 30K to 180K
A-39 PAGE 44 : Change PU7009 & PU7011 from RT9025 to APL5920
A-40 PAGE 29 : Change PQ4 & PQ45 from AOL1448 to RJK03B9DP
A-41 PAGE 29 : Change PQ3, PQ7, PQ41& PQ44 from AOL1718 to RJK03D3DPA
A-42 PAGE 32 : Change PQ7018 from AOL1718 to RJK03D3DPA
A-43 PAGE 32 : Change PC137 & PC152 from CC71004MZ81 to CC71004MZ04

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