

J361Y-SB Rev_V3.06(06/16/2005)

91.3H801.001

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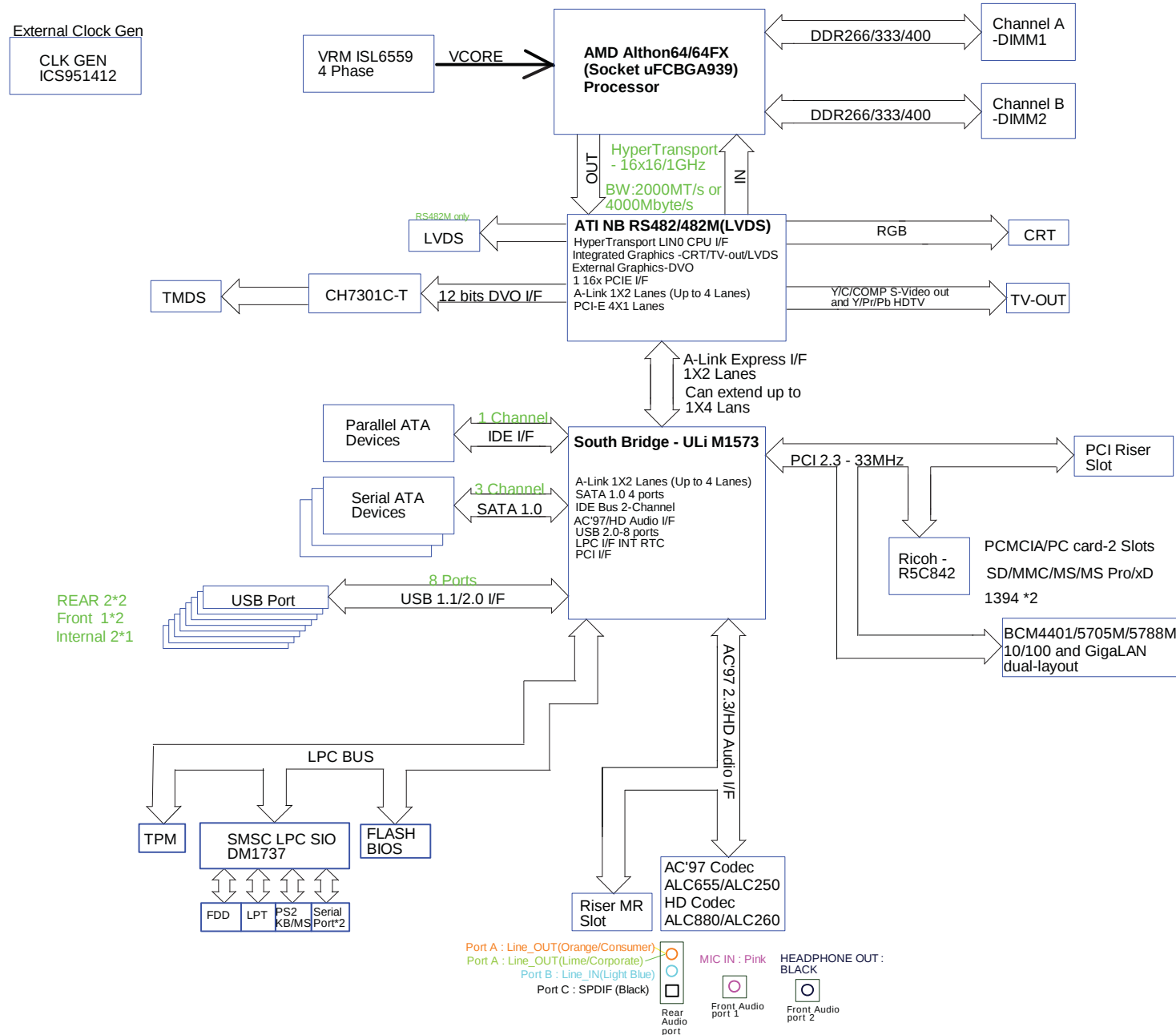
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Sheet 48	ATX 24Pin conn
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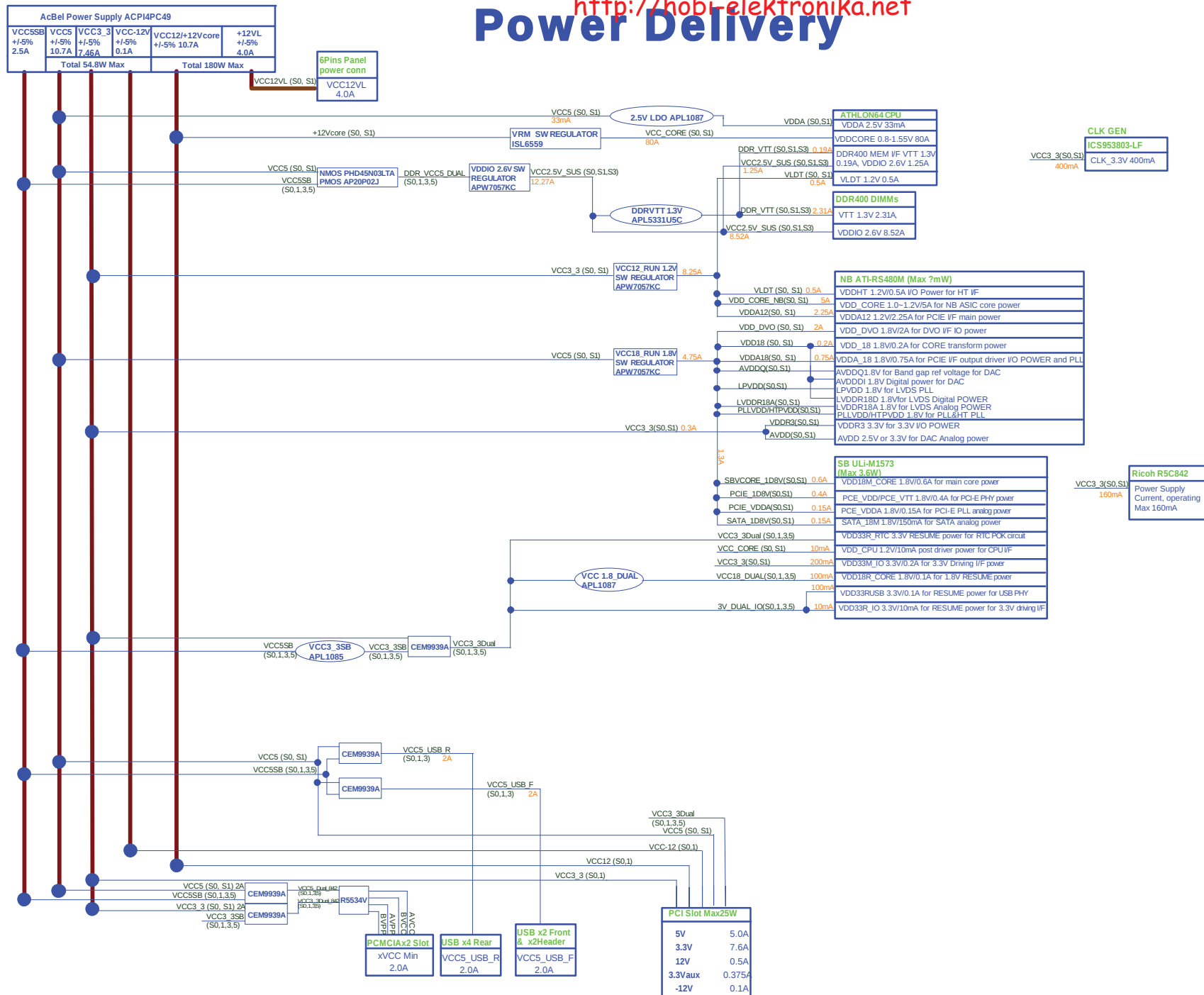
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

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Block Diagram





PCI

Device	IDSEL	GNTJ/REQJ	IRQ	Active Status
R5C842	AD21	PREQJ3PGNTJ3	PIRQJDA,B,C	LOW
PCI RISER	AD19 AD20	PREQJ0PGNTJ0 PREQJ1PGNTJ1	PIRQJAB,C,D PIRQJB,C,D,A	LOW
PCI LAN	AD22	PREQJ4PGNTJ4	PIRQJE	LOW

SMSC DM1737

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
GP10	RST_IDE*		0	MAIN (VCC)	Low
GP11	PCIRST_OUT1	LAN_DISJ	0	AUX (VTR)	Low/Default high
GP12			0	AUX (VTR)	
GP13		SLP_S1_S5_L*	0	AUX (VTR)	Low@S0/ S1/ S3 / High@S4/ S5
GP14	PCIRST_OUT4	SUSLED*	0	AUX (VTR)	Low
GP21	KBDATA		I	MAIN (VCC)	
GP22	KBCLK		I	MAIN (VCC)	
GP27			I	MAIN (VCC)	
GP32	MSDATA		I	MAIN (VCC)	
GP33	MSCLK		I	MAIN (VCC)	
GP36	KBRST*		I	MAIN (VCC)	Low
GP37	A20GATE		I	MAIN (VCC)	
GP40			0	MAIN (VCC)	
GP42	IO_PMES3#		0	AUX (VTR)	PME event output
GP43	IO_PMES5#		0	AUX (VTR)	PME event output
GP50	RI*2		I	MAIN (VCC)	
GP51	DCD*2		I	MAIN (VCC)	
GP52	RXD2		I	MAIN (VCC)	
GP53	TXD2		I	MAIN (VCC)	
GP54	DSR*2		I	MAIN (VCC)	
GP55	RTS*2		I	MAIN (VCC)	
GP56	CTS*2		I	MAIN (VCC)	
GP57	DTR*2		I	MAIN (VCC)	
GP60		TVLED*	0	AUX (VTR)	High / push-pull
GP61		LCDONJ_SIO	0	AUX (VTR)	Low/ S5 wake up event

ATI RS482/482M

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
DFT_GPIO0			I	VDDR3	
DFT_GPIO1	LOAD_ROM_STRAPS#		I	VDDR3	Low
DFT_GPIO2		TV_SWITCH	0	VDDR3	1:0-Video
DFT_GPIO3		D_PLUGDET	I	VDDR3	0: SDV Video connected 1: HDTV_unconnected
DFT_GPIO4			I	VDDR3	
DFT_GPIO5	LOAD_MEM_STRAPS#		I	VDDR3	Low

ULi M1573

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
RUNGPI00		IDE_P	I	VDD33M_IO	High
RUNGPI01			0	VDD33M_IO	LOW
RUNGPI02				VDD33M_IO	
RUNGPI03		MO_DET	I	VDD33M_IO	0: M0 connected 1: M0 unconnected
RUNGPI18	ACB_BITCLK	BOARD_ID_0	I	VDD33M_IO	
RUNGPI11	VOL_UP#	BOARD_ID_1	I	VDD33M_IO	
RUNGPI12	VOL_DOWN#	BOARD_ID_2	I	VDD33M_IO	
RUNGPI13	VOL_MUTE#	BOARD_ID_3	I	VDD33M_IO	
RUNGPI9	CLKRUN#	CRT_TMDS_DISJ	0	VDD33M_IO	HIGH
RUNGPO[13]	CPUHI#	Blueled*	0	VDD33M_IO	HIGH
RUNGPO[16]	IGNNE#	Blueled02*	0	VDD33M_IO	HIGH
RUNGPO[19]	NMI	HDDLED	0	VDD33M_IO	HIGH
RUNGPO[21]	SMI#	Blueled03*	0	VDD33M_IO	HIGH
SATA_GPIO0		LCD_VID0	I	VDD33M_IO	
SATA_GPI1		LCD_VID1	I	VDD33M_IO	
SATA_GPI2		LCD_VID2	I	VDD33M_IO	
SATA_GPI3			I	VDD33M_IO	
SATA_GP00			0	VDD33M_IO	LOW
SATA_GP01		FlashROM_WP	0	VDD33M_IO	High/Default LOW
SATA_GP02			0	VDD33M_IO	LOW
SATA_GP03		PWRLED*	0	VDD33M_IO	LOW
RSMGPI00		USBPWR_Ctrl	0	VDD33R_IO	Consumer: S3->H, S4/S5->L Corporate: S3/S4->H, S5->L
RSMGPI01		ACPILED*	0	VDD33R_IO	HIGH
RSMGPI02		ACPI_S3	0	VDD33R_IO	S3:High
RSMGPI03		842HWSPNDJ	0	VDD33R_IO	High
RSMGPI10	SMBALERT#	IO_PMES3#	I	VDD33R_IO	PME event input
RSMGPI1[0]	SLPBTN#	IO_PMES5#	I	VDD33R_IO	PME event input

<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title GPIO Table			
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Rev. Notes

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DATE	Rev	Description	Page
3/10	SA_V1.0	Release Schematic	
	SA_V1.1	Add Board_ID [3..0] setting	22
		Add PIRQ[EH] pull high	36
		Add CN41	28
		HW strapping setting	13,21,22,23
		Modify Front HP OUT Mute circuit	39
		Two copper pure for VTT fill - at least 100mils wide/Change DDR_VTT_CPU as DDR_VTT	7,8
		Modify Net REFCLK0_1 and REFCLK0_2	24
3/14		Connect ASIC8M_CPU_RST to LDTREST#	47
		Change R92 to 2.4k ohm	17
		Modify DVO_IDCKN and DVO_IDCKP	17
		Modify TMSD HotPlug circuit	17
		Modify TV-out I2C circuit	18
3/15		Modify VDD_DVO power for RS482 revA11	15
		Modify DVO_VREF circuit	17
3/15	SA_V1.2	Change L33	22
		Modify VRM Circuit (Vendor suggestion)	46
		Change M1573 HW strapping resistors to 1K ohm	21
		Change R536 and R538 to 1K ohm and change R554 to 5.1K (Vendor suggestion)	46
		Modify SB&NB POWER Good circuit	47
3/16	SA_V1.3	Modify DLINE circuit	18
		Modify TMSD Hot plug circuit	15
3/16	SA_V1.4	Move R644 and R697 to Page17. Delete R665 and R666	13,17,19
		Delete R669 and R670	18
		Delete TC86	32
		Modify DLINE circuit	18
		Change M1573 to RevA1D	20-23
		Add LAN Disable circuit	37
3/19	SA_V1.5	Delete TC39 for Extra 4 CPU FANSINK screw hole	46
		Change C763 to a small size	40
		Modify FJ's checklist items	
3/21	SA_V1.6	SWAP USB Port	26
	SA_V1.7	SMBCLK and SMBDATA (SIO Page)	28
		Modify SUSLED* circuit	41
		Change R74 and R75 to 8.25k and 82.5 ohm (ATI_RS4X0F4.pdf)	14
		Modify NB_RST* circuit	20
3/22	SA_V1.8	Modify LAN Disable circuit	37
3/23	SA_V1.9	Add 6559 Common Ground	46
	SA_V1.10	Change PCIRST circuit from VCC3_3DUAL driven to VCC3_3SB	
		USE CLKRUN# of M1573(RUNGPO9) to disable CR1 and TMSD	
		Modify GPIO arrangement	
		Add another pair of SM bus dedicate for CLK_GEN and DDR	
3/24	SA_V1.11	Net Swap	
3/25	SA_V1.12	Add Two capacitors for EMI	38
	SA_V1.13	Change Q70 to 3904 NPN BJT	42
3/30	SA_V1.16	Rename Reference and swap nets	
3/31	SA_V1.17	Connect H7 to AGND	
4/06	SA_V1.18	Add CLOCK MAP	50

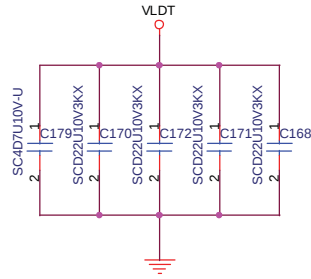
NOTE :

DATE	Rev	Description	Page
0422	SB_V2.0	Modify All SA PIR rework items and FJ GFX_Feedback	
0426	SB_V2.1	Modify R554 and R744 and FJ GFX_Feedback ver.0427	47
0427		Swap ACZ_SDIN0 and ACZ_SDINI at Sb side	23
	SB_V2.2	L_O_R can't be connected with Mute_LG	39
		Add R746/R747/R748	23
		Change C267 to 0.015uF and R418 to 60.4 ohm	44
		Add R749	27
		Modify LAN_RSTJ signal	37
		Remove JF2 and around circuit	21
		Change Pin assignment of CN99	40
		Modify LCD PWRON circuit	37
		Add USB ESD IC	26
		Add COMMON GND for SW regulator	44,45
		Change TC35 to Z20JF	
0505	SB_V2.3	Add common ground near VRD low side MOS	46
		Modify SUSLED circuit	41
		Modify FAN Tach circuit	41
		Modify GPIO assignment for LED function	
		Modify PCI Riser IOSEL	36
		Add FlashRom write protect function	
		Add Two more GPIO pin for IO_PMECS# and IO_PMESS#	
0508	SB_V2.5	Modify USBPWR control circuit	42
		Modify SUSLED circuit	41
		Modify TVON_Plug circuit	41
		Modify All LED circuit	41
		Modify BIOS write protection circuit	27
		Add a pull-up resistor on Mute#	40
		Change R557 to 100K ohm	
0509	SB_V2.6	Modify VDDA_2.5V_CPU Enable circuit	08
		1394 port 0 and port1 swap	
0510	SB_V2.7	Remove Q73 and ACZ_RST_CRL*	40
		Modify All LED circuit	41
		Modify USB POWER controller circuit	42
		Add two 1K ohm between VCC5_USB_F/VCC5USB_R* and GND	42
		Remove D31 and R517. Then change R518 from 1k-ohm to 0ohm and unmount as default.	29
		[ESD for DDC]	17/19
0511	SB_V2.8	Add SLP_S4_H to control USB power	23/42
		Change R775.1 to VCC5	08
		Modify TVON_PLUSE3.jpg	28/41
	SB_V2.9	Change Q55 to 2N7002 and remove R769	41
	SB_V2.10	USE CRT_TMDS_DisJ to do mute function	40
		Change BOM option for Audio function	40
		Reserve 3.3V pull-up for Fansink	41
0512	SB_V2.11	Modify VLDY_EN circuit	45
		Modify USB power control circuit	42
0513	SB_V2.12	Unmount R59	41
0517	SB_V2.13	Change Q105 to FET(2N7002)	40
		Change Board ID	21
		Consumer M/B: Board_ID[3..0] = "0001"	
		Corporate M/B: Board_ID[3..0] = "1000"	
		Small Qty M/B: Board_ID[3..0] = "0010"	
		Change C67 to X7R	16
		Change R512 for Consumer/LCDCP, Change R508 for Corporate	29
		Change C98 and C413 to X5R	32,26
		mount C691 and C692	24
		R13 R14 change to 1Kohm, RN1 change to 1K ohm	28
		U58 U59 U60 change to 83.01293.0AE	26
0524		R129 unmount, L66 change to 63.R0004.151	32,38
0525		R59 R777 change to 0 ohm, Q103 Q15 change to 2N7002	41

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Processor HyperTransport Interface

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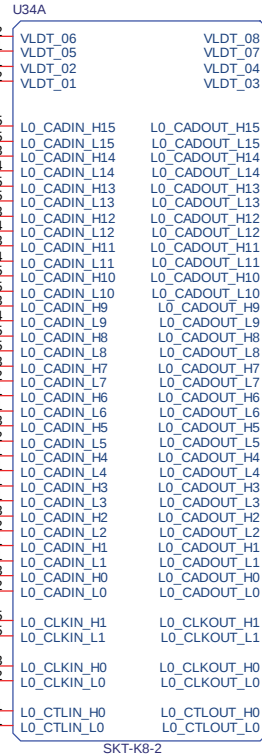


At least 200mils for pure
and 20mils to pin

At least 100mils to Capacitor
and 20mils to pin

12 L0_CADIN_L[0..15] >> L0_CADIN_L[0..15]
12 L0_CADIN_H[0..15] >> L0_CADIN_H[0..15]
20/5/5/20 1"<x<12"

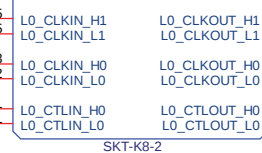
L0_CADIN_H15 R5
L0_CADIN_L15 T5
L0_CADIN_H14 P3
L0_CADIN_L14 P4
L0_CADIN_H13 N5
L0_CADIN_L13 P5
L0_CADIN_H12 M3
L0_CADIN_L12 M4
L0_CADIN_H11 K3
L0_CADIN_L11 K4
L0_CADIN_H10 J5
L0_CADIN_L10 J5
L0_CADIN_H9 K5
L0_CADIN_L9 H3
L0_CADIN_H8 H4
L0_CADIN_L8 H5
L0_CADIN_H7 R3
L0_CADIN_L7 R2
L0_CADIN_H6 N1
L0_CADIN_L6 P1
L0_CADIN_H5 N3
L0_CADIN_L5 N2
L0_CADIN_H4 L1
L0_CADIN_L4 M1
L0_CADIN_H3 J1
L0_CADIN_L3 K1
L0_CADIN_H2 J3
L0_CADIN_L2 J2
L0_CADIN_H1 G1
L0_CADIN_L1 H1
L0_CADIN_H0 G3
L0_CADIN_L0 G2



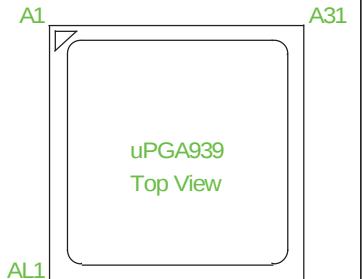
L0_CADOUT_H15 V4
L0_CADOUT_L15 V3
L0_CADOUT_H14 Y5
L0_CADOUT_L14 W5
L0_CADOUT_H13 Y4
L0_CADOUT_L13 Y3
L0_CADOUT_H12 AB5
L0_CADOUT_L12 AA5
L0_CADOUT_H11 AD5
L0_CADOUT_L11 AC5
L0_CADOUT_H10 AD4
L0_CADOUT_L10 AD3
L0_CADOUT_H9 AF5
L0_CADOUT_L9 AF4
L0_CADOUT_H8 AF3
L0_CADOUT_L8 V1
L0_CADOUT_H7 U1
L0_CADOUT_L7 W2
L0_CADOUT_H6 W3
L0_CADOUT_L6 Y1
L0_CADOUT_H5 W1
L0_CADOUT_L5 AA2
L0_CADOUT_H4 AA3
L0_CADOUT_L4 AC2
L0_CADOUT_H3 AC3
L0_CADOUT_L3 AD1
L0_CADOUT_H2 AC1
L0_CADOUT_L2 AE2
L0_CADOUT_H1 AE3
L0_CADOUT_L1 AF1
L0_CADOUT_H0 AE1

L0_CADOUT_H[0..15] >> L0_CADOUT_H[0..15] 12
L0_CADOUT_L[0..15] >> L0_CADOUT_L[0..15] 12
20/5/5/20 1"<x<12"

12 L0_CLKIN_H1 >> L0_CLKIN_H1 L5
12 L0_CLKIN_L1 >> L0_CLKIN_L1 M5
12 L0_CLKIN_H0 >> L0_CLKIN_H0 L3
12 L0_CLKIN_L0 >> L0_CLKIN_L0 L2
12 L0_CTLIN_H0 >> L0_CTLIN_H0 R1
12 L0_CTLIN_L0 >> L0_CTLIN_L0 T1
20/5/5/20 1"<x<12"



L0_CLKOUT_H1 AB4
L0_CLKOUT_L1 AB3
L0_CLKOUT_H0 AB1
L0_CLKOUT_L0 AA1
L0_CTLOUT_H0 U2
L0_CTLOUT_L0 U3
20/5/5/20 1"<x<12"



<Core Design>

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Title Althon64/64FX HT I/F		
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Channel A



Motherboard trace routing : 20/15/20

Motherboard trace routing : 10/10/10

8 7 6 5 4 3 2 1

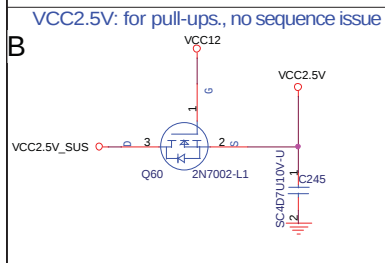
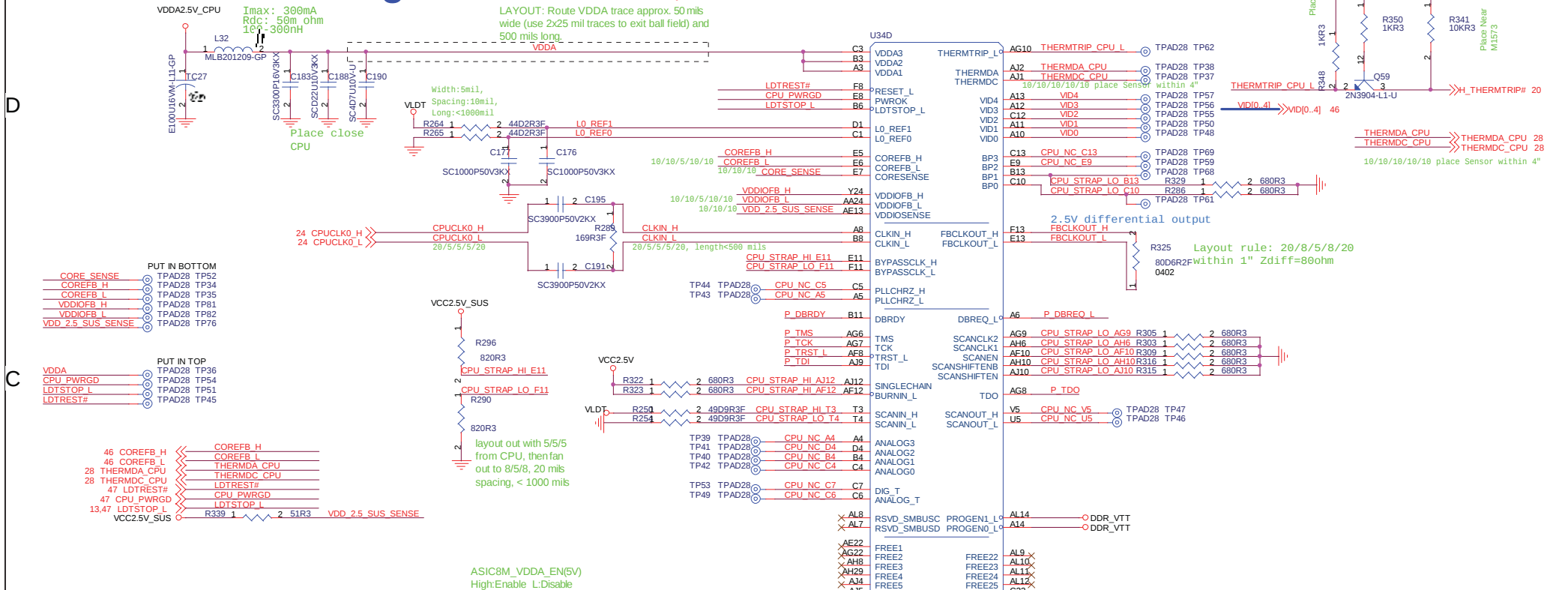
Processor MISC Signals

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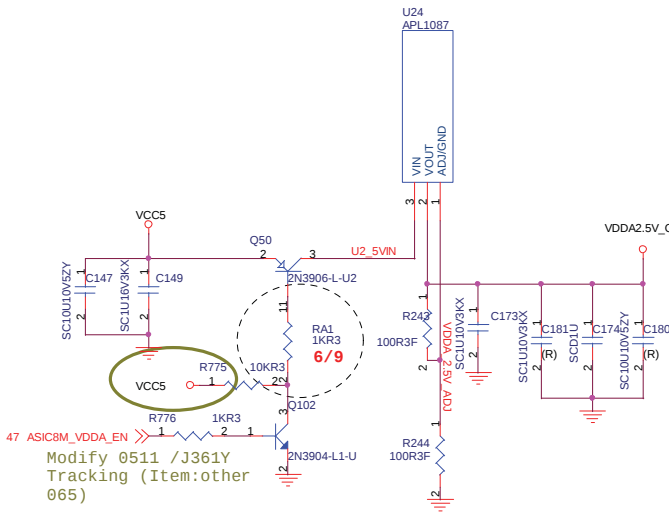
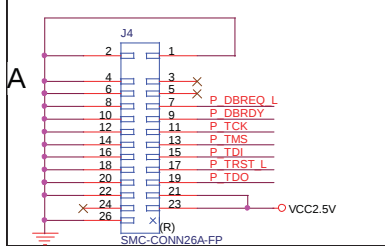
VCC2_5V

VCC3_3

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VDDA2.5V CPU: for PLL



AE22	FREE1		AL9
AG22	FREE2	FREE22	AL10
AH8	FREE3	FREE23	AL11
AH28	FREE4	FREE24	AL12
AJ4	FREE5	FREE25	C22
AJ5	FREE6	FREE26	C28
AJ6	FREE7	FREE27	D8
AJ7	FREE8	FREE28	D11
AJ27	FREE9	FREE29	D12
AJ28	FREE10	FREE30	D29
AK3	FREE11	FREE31	E21
AK4	FREE12	FREE32	E22
AK6	FREE13	FREE33	G15
AK8	FREE14	FREE34	G15
AK8	FREE15	FREE35	N27
AK10	FREE16	FREE36	T26
AK12	FREE17	FREE37	T26
AL3	FREE18	FREE38	U28
AL4	FREE19	FREE39	C11
AL5	FREE20	FREE40	AG15
AL6	FREE21	FREE41	

<Core Design>



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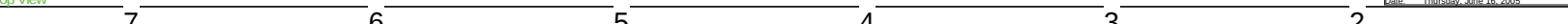
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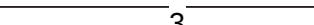
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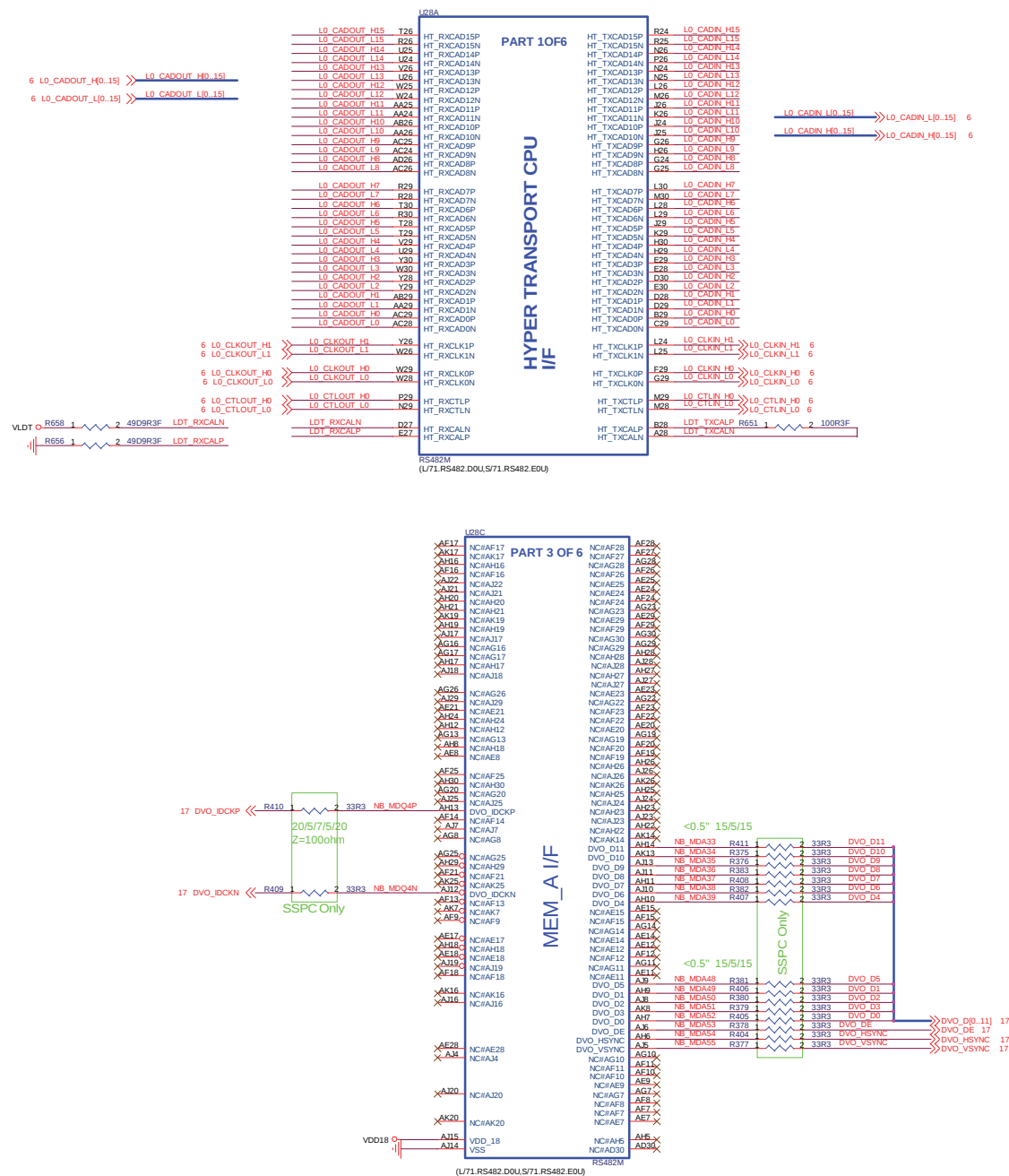
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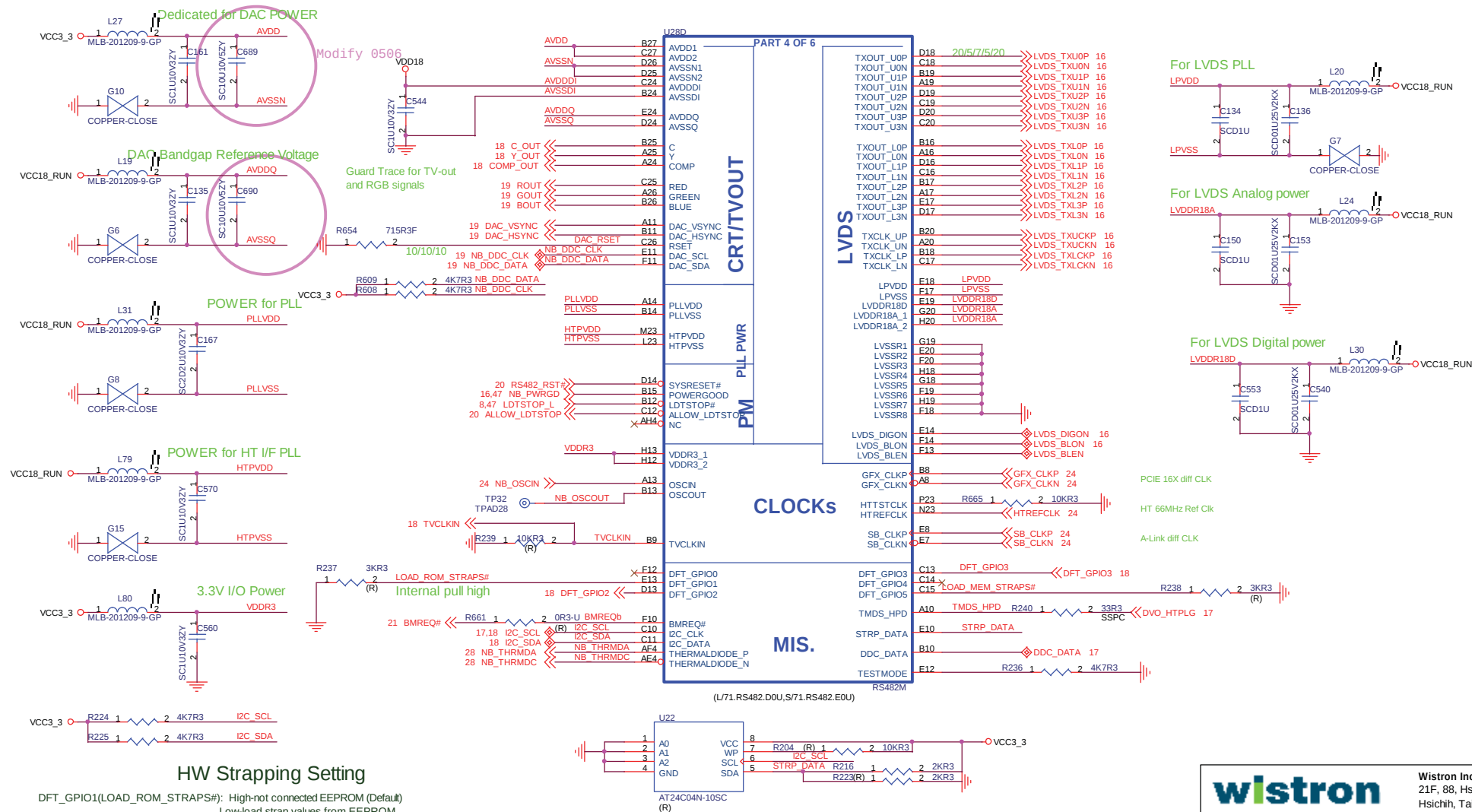
8 DDR Termination

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RS482 ver.A12 PB/P/N 71.RS482.B0U
RS482 ver.A12 LF/F/N 71.RS482.B0U
RS482M ver.A12 PB/P/N 71.RS482.D0U
RS482M ver.A12 LF/P/N 71.RS482.C0U

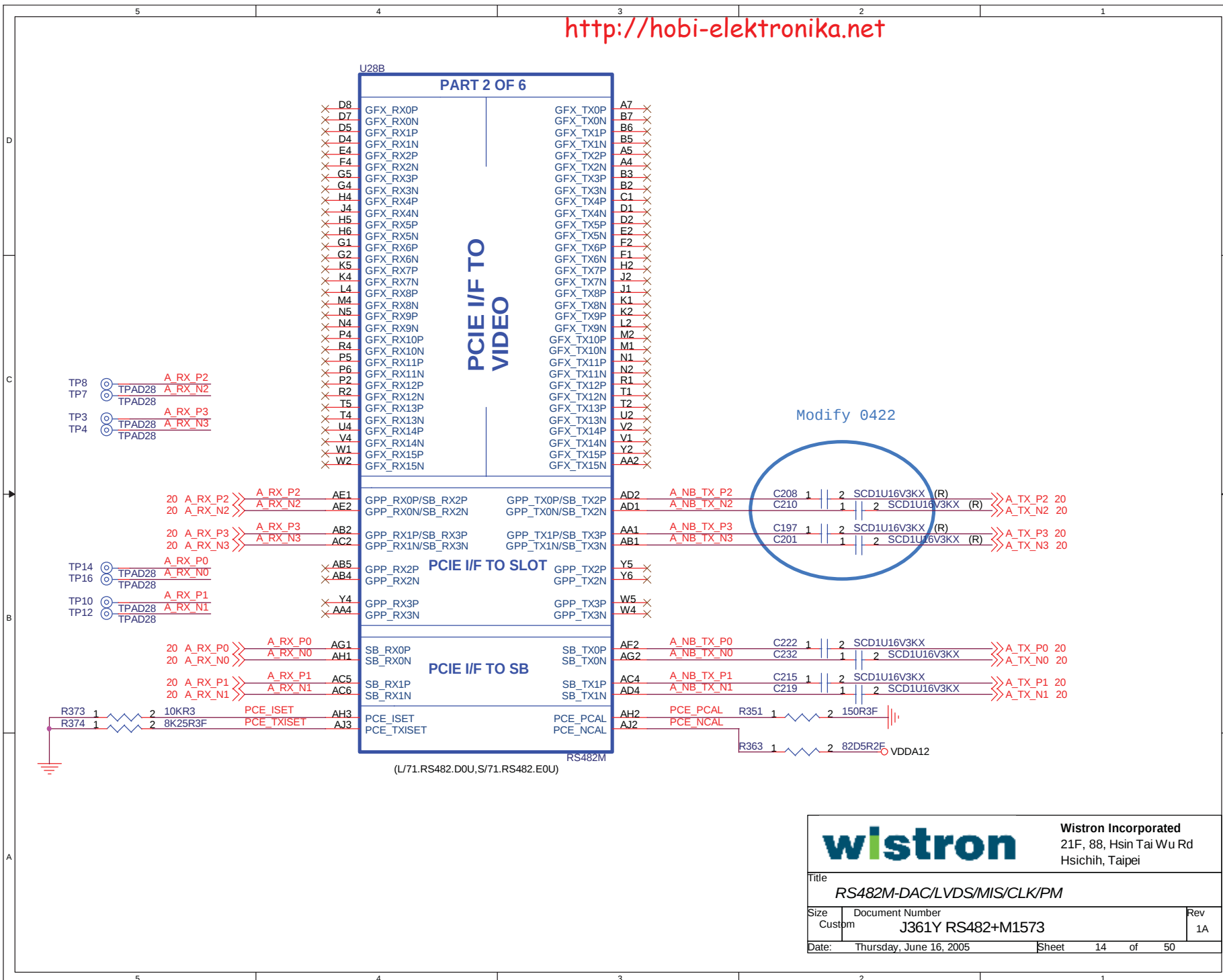


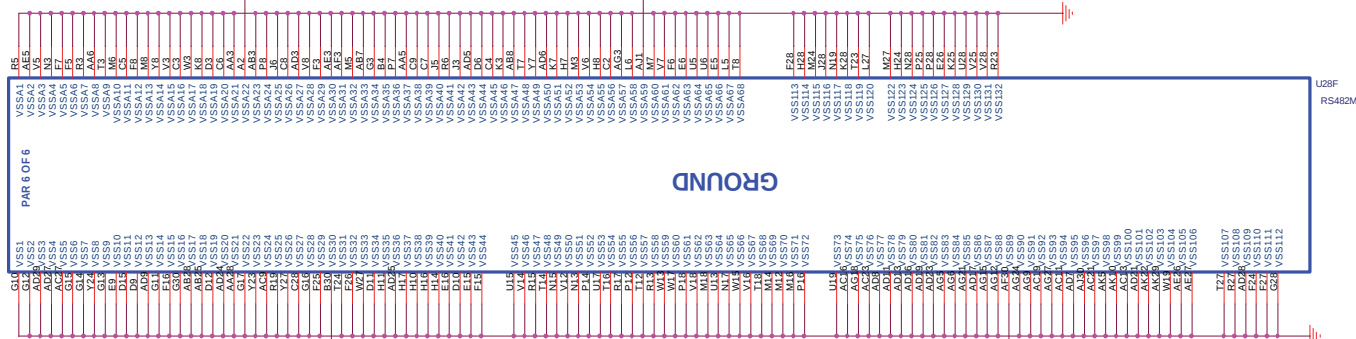
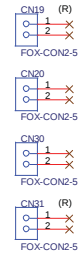
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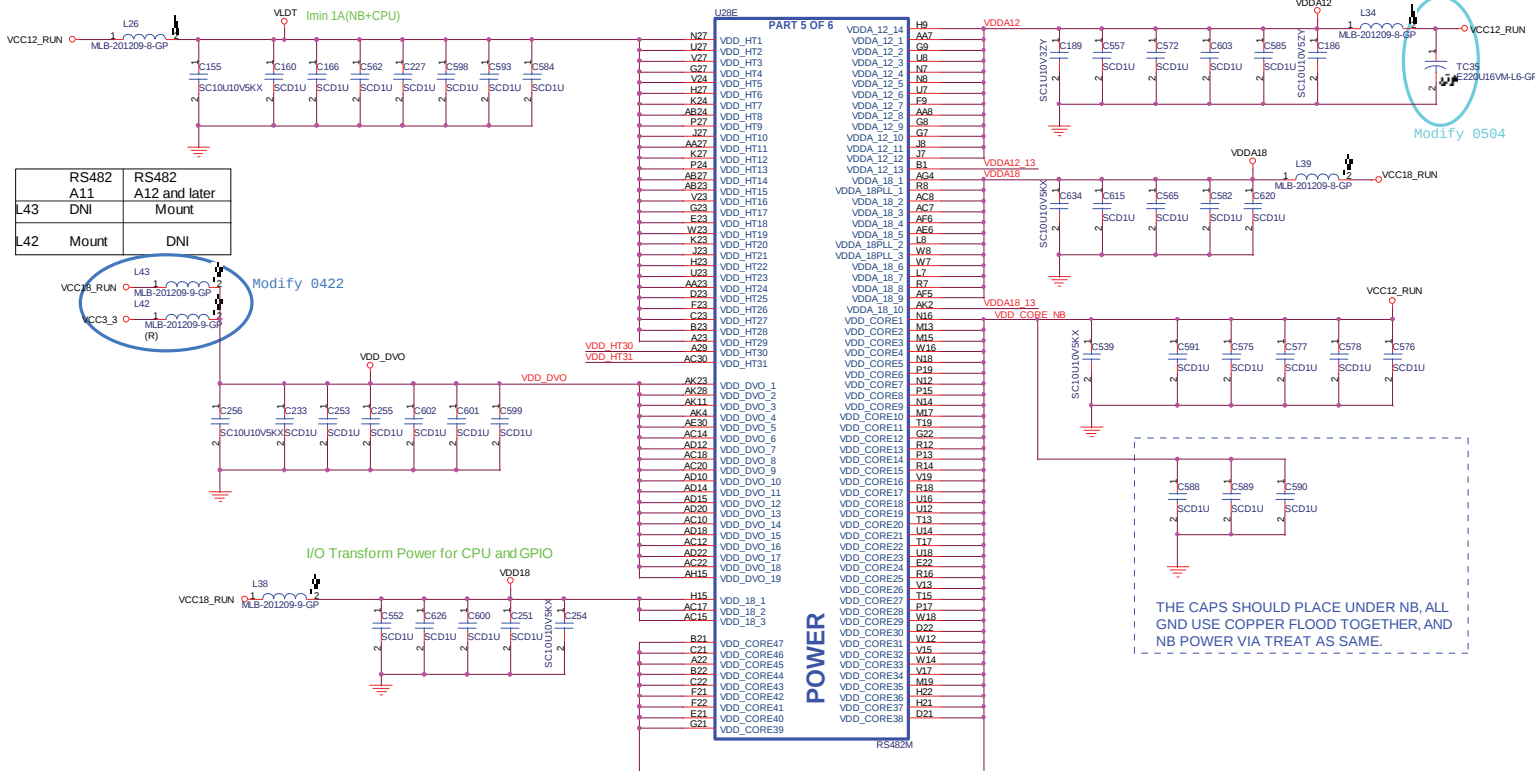
NOTE: Provide access to STRAP_DATA and I2C_SCL pins is MANDATORY.

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Title <i>RS482M-DAC/LVDS/MIS/CLK/PM</i>			
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Power Signal	S0	S1	S3	S4/S5	S6
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
VDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



PUT DECOUPLING CAPS ON THE TOP,
CLOSE TO BALLS.
CONNECT VSSA22,VSSA59, VSS30
,VSS89 to the ground.

THE CAPS SHOULD PLACE UNDER NB, ALL GND USE COPPER FLOOD TOGETHER, AND NB POWER VIA TREAT AS SAME.



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Hsichih, Taipei

Title	RS482M-POWER & GND
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Size	Document Number
Custom	J361Y RS482+M1573

Date: Thursday, June 16, 2005

Date: Thursday, June 20, 2008

<http://hobi-elektronika.net>


$$12 \times 12V / 2.7K = 0.053W$$

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Hsichih, Taipei

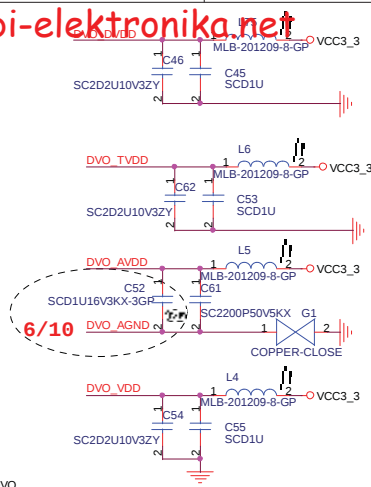
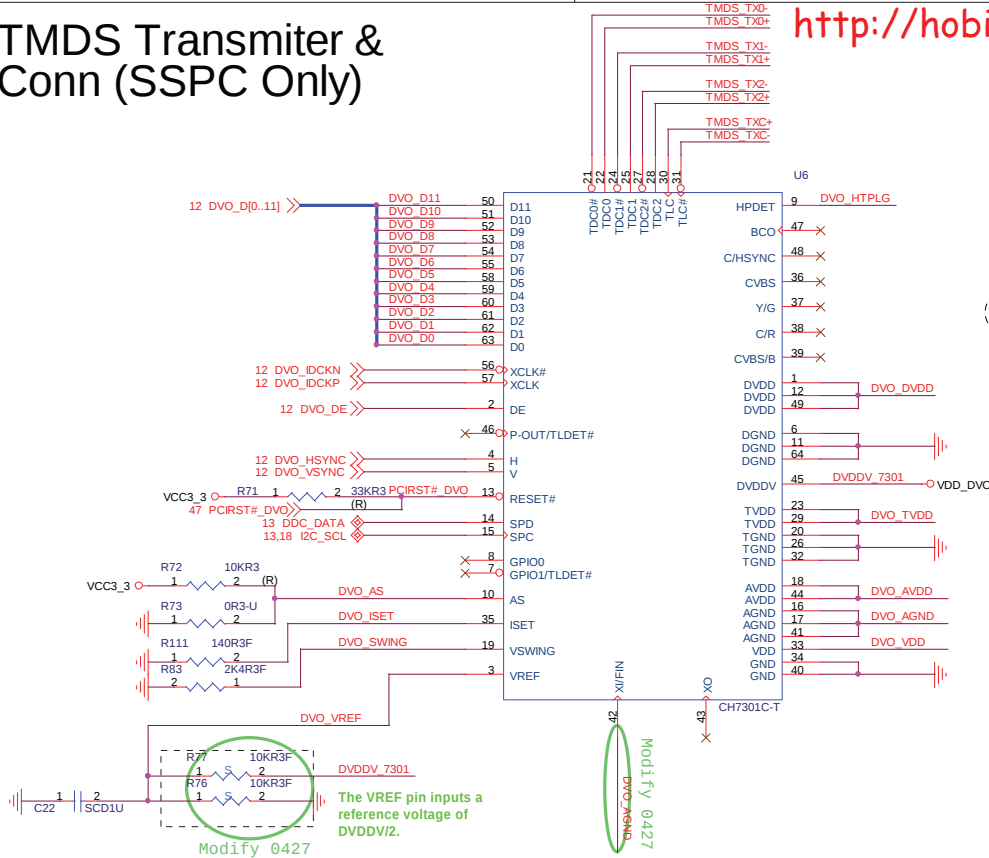
Title

LVDS conn	
Size	Document Number
	J361Y RS482+M1573

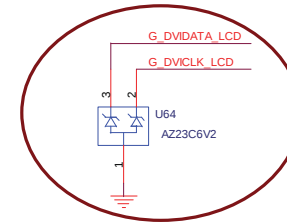
Rev	1A
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TMDS Transmitter & Conn (SSPC Only)

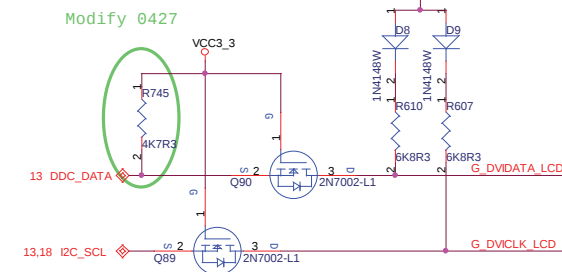
<http://hobi-elektronika.net>



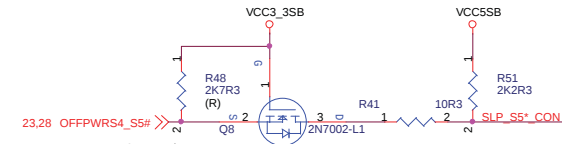
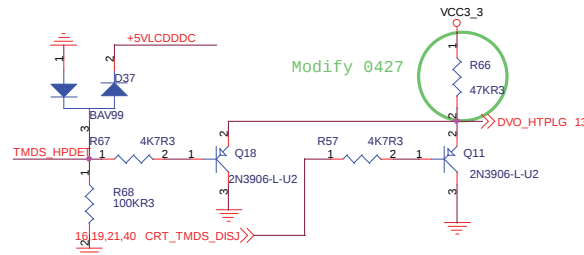
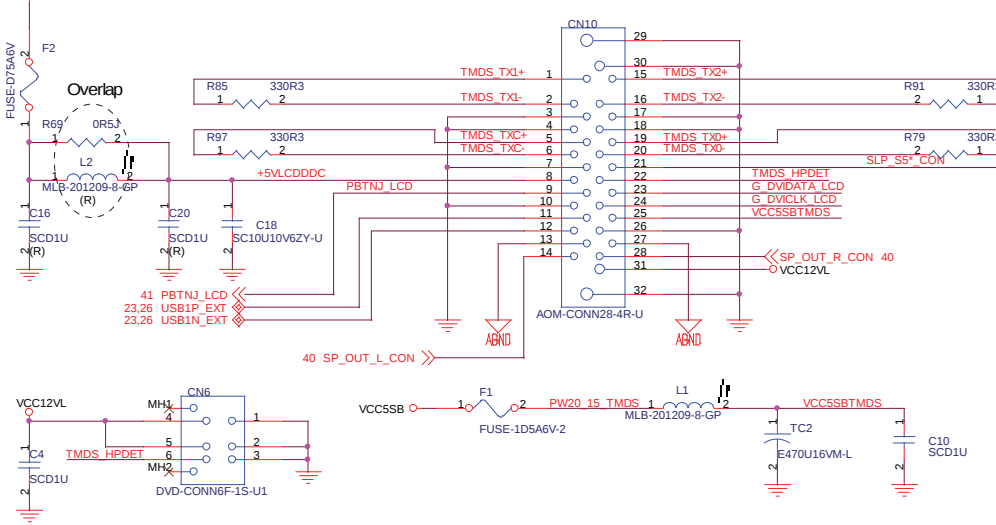
Modify 0510
/J361Y_Tracking (Item
other-064)



Hot Plug detect circuit



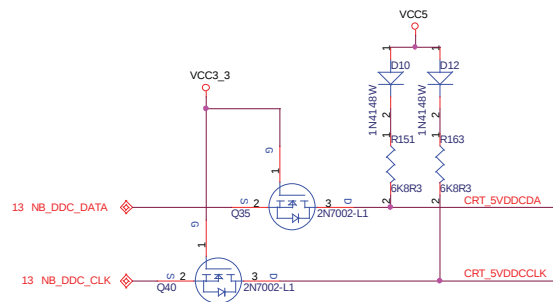
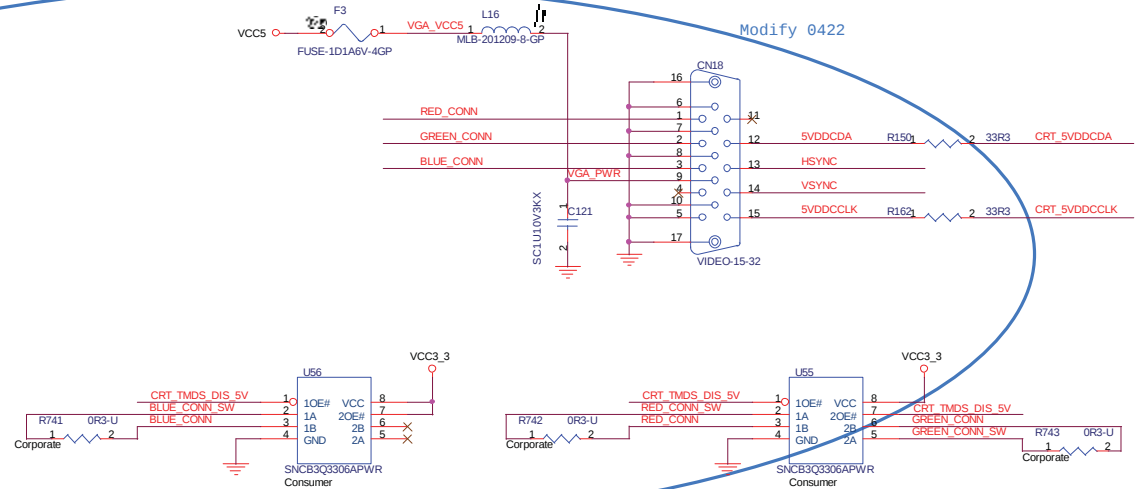
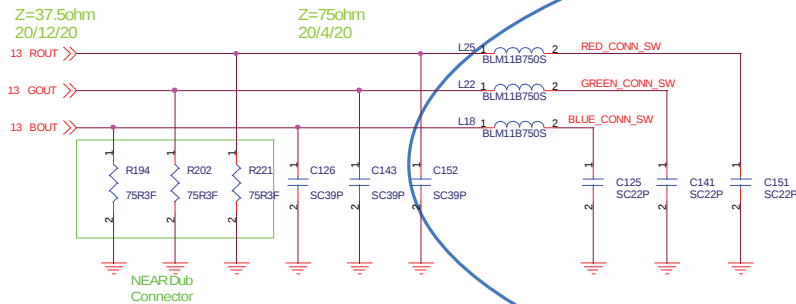
TMDS Conn & PS conn (6 pins)



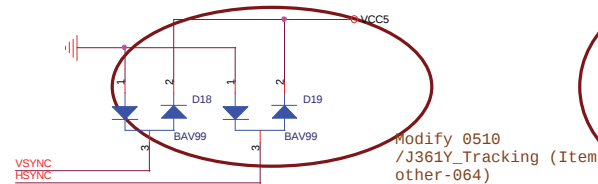
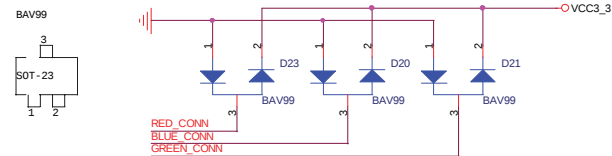
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Title			
TMDS Transmitter & conn			
Size	Document Number	Rev	
Custom	J361Y RS482+M1573	1A	

Video Filter & CRT CONN

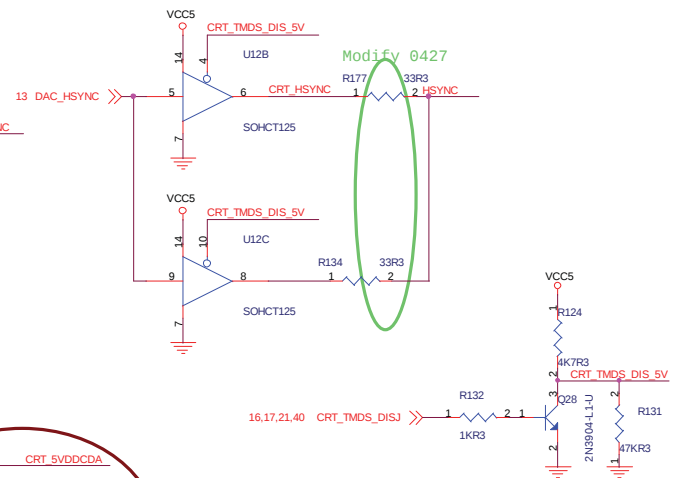
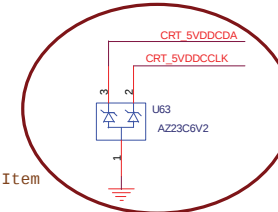
<http://hobi-elektronika.net>



ESD PROTECTION

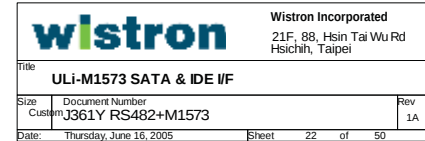


Modify 0510
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 other-064)

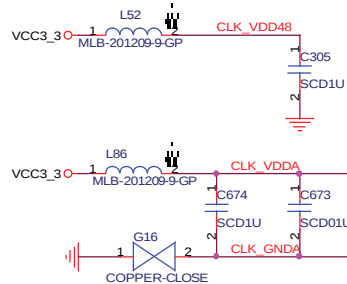


wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
VGA CONN		
Size	Document Number	Rev
Customer	J361Y RS482+M1573	1A
Date	Thursday, June 16, 2005	Sheet 19 of 50

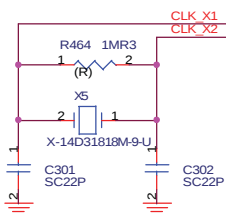








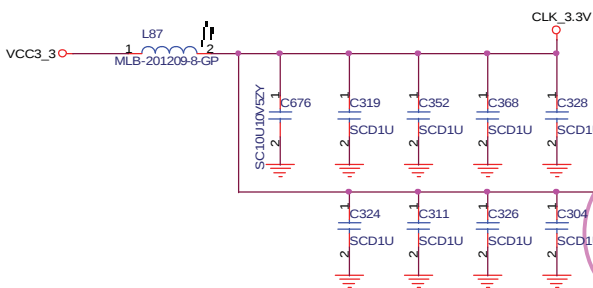
Modify 0506



13 HTREFCLK

21 PCICLK_SB

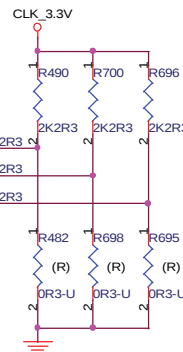
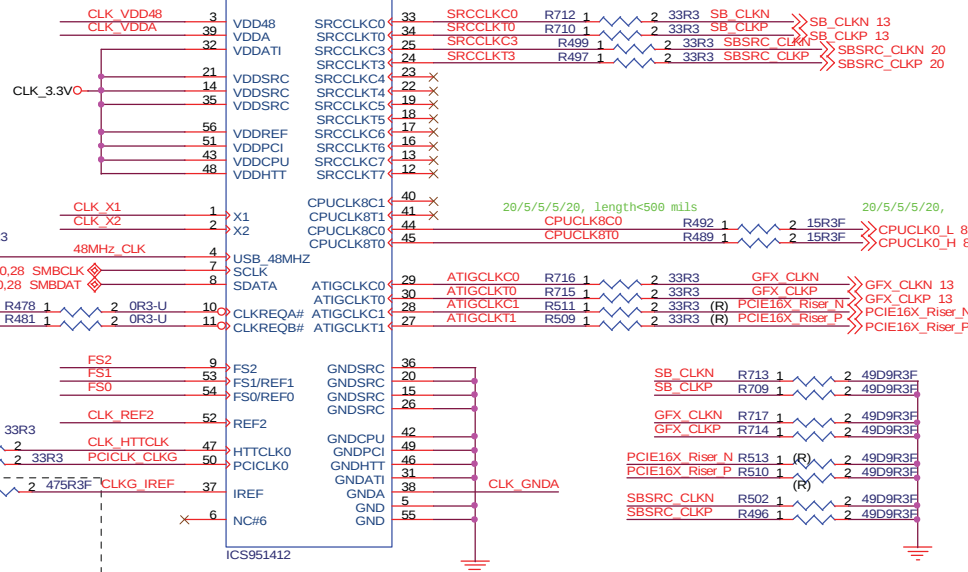
$I_{oh} = 5 \cdot I_{ref}$
(2.32mA)
 $V_{oh} = 0.71V @ 60 ohm$



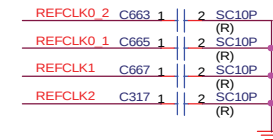
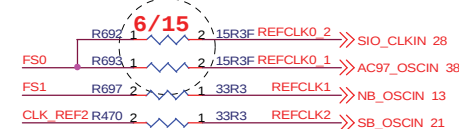
Modify 0506

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



REFCLK0_x: 14.31818MHz for AC97_OSCIN and SIO
REFCLK1: 14.31818MHz for RS482M
REFCLK2: 14.31818MHz for M1573

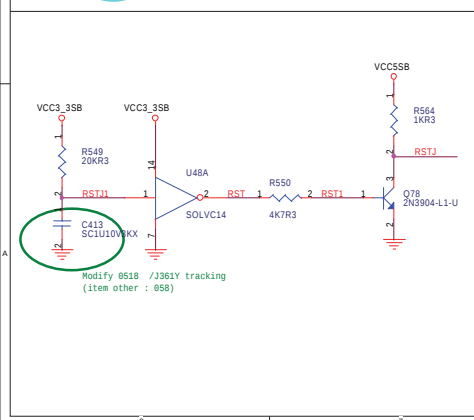
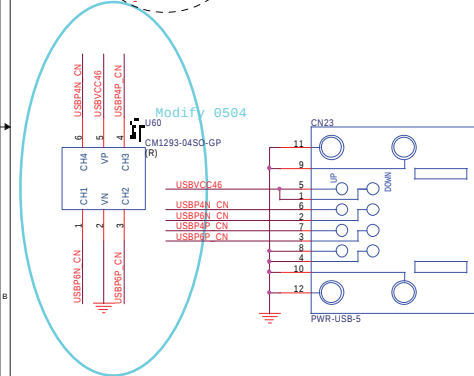
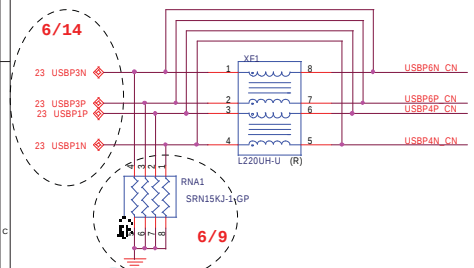
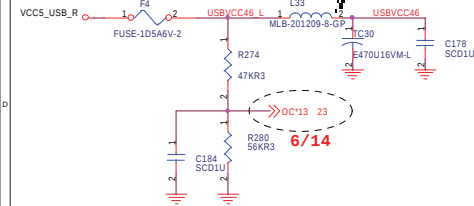


<Core Design>

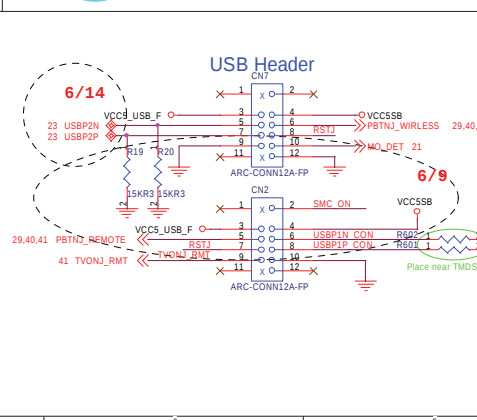
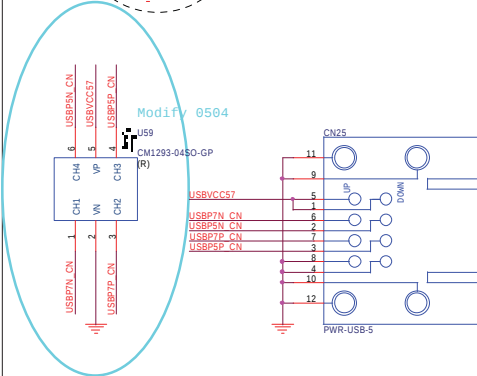
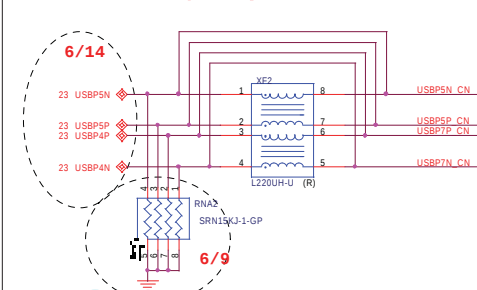
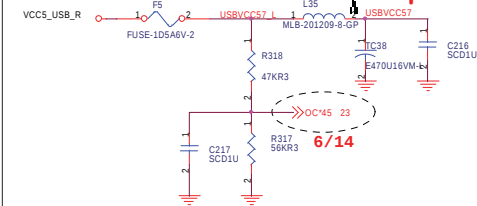
wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CLOCK GENERATOR			
Size	Document Number	Rev	
Custom	J361Y RS482+M1573	1A	
Date:	Thursday, June 16, 2005	Sheet	24 of 50

USB CONN

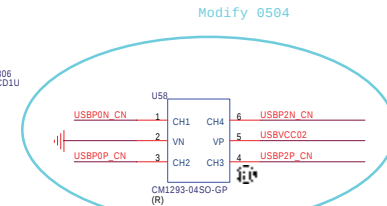
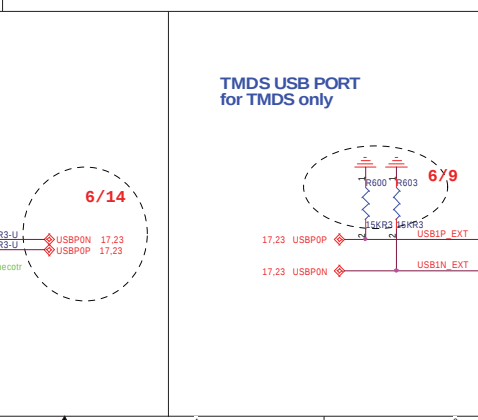
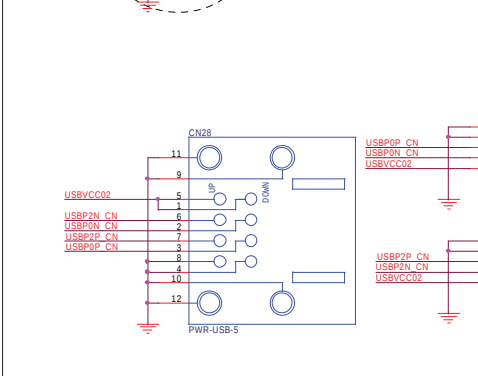
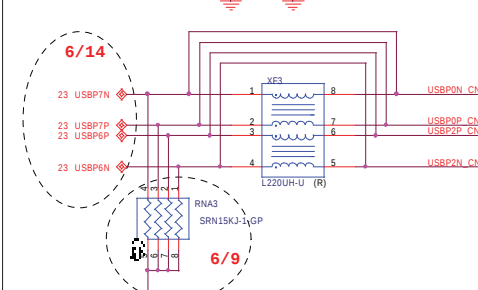
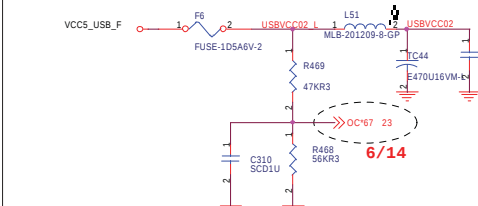
Rear USB CONN 1(Port 4 and Port6)



Rear USB CONN 2(Port5 and Port7)

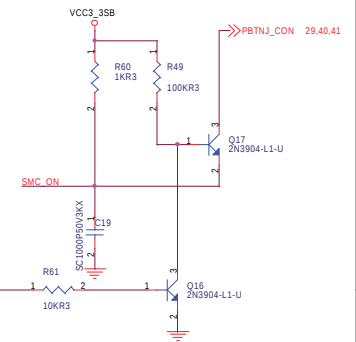


<http://hobi-elektronika.net>



Modify 0504

SMART CARD CIRCUIT

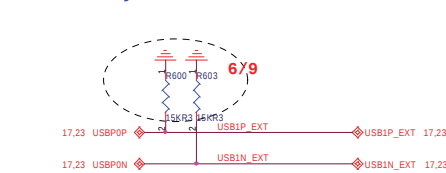


SLP S1, S5 L*:
High@S4, S5

28 SLP_S1_S5_L* >>>

USB Layout Rule : 2017.5/7.5/7.5/20

TMDS USB PORT for TMDS only

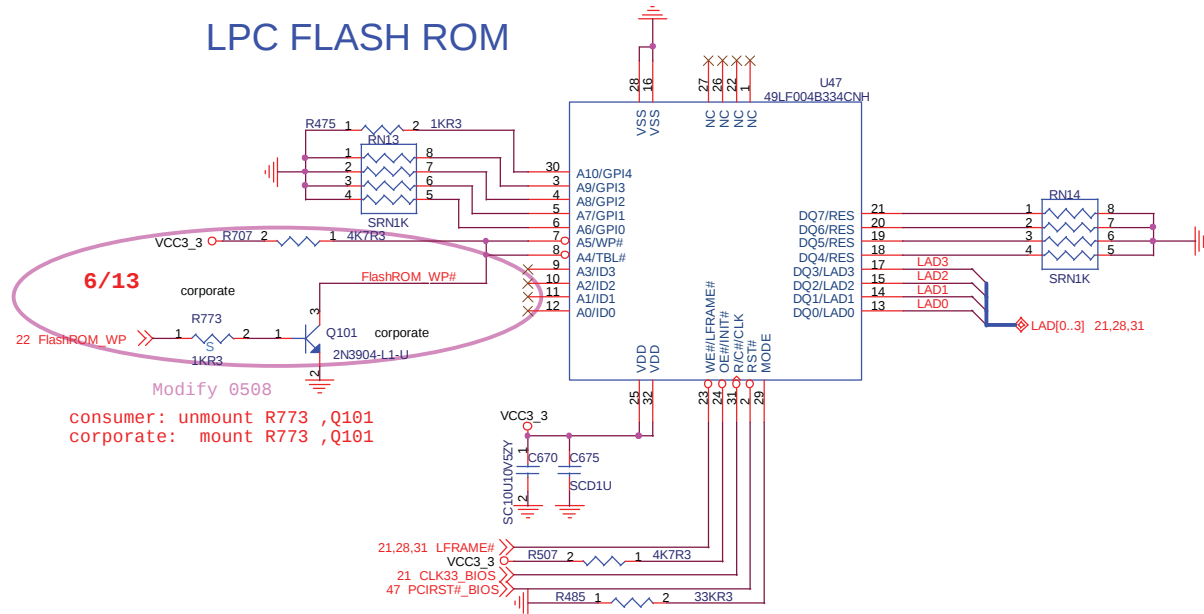


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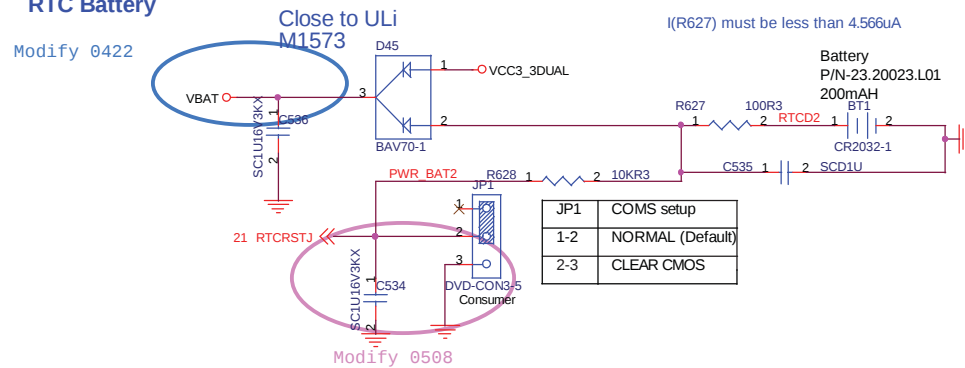
USB CONN			Rev
Size	Document Number	J361Y RS482+M1573	1A
Date	Thursday, June 16, 2005	Sheet 26 of 50	

LPC FLASH ROM



BIOS SCOKET P/N : 62.10061.001

RTC Battery



<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
BIOS/Battery RTC			
Size	Document Number		Rev
Custom	J361Y RS482+M1573		1A
Date:	Thursday, June 16, 2005	Sheet	27 of 50

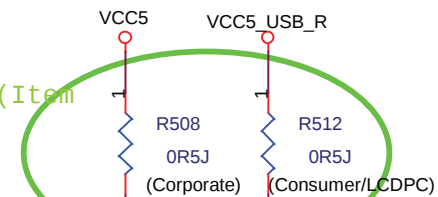
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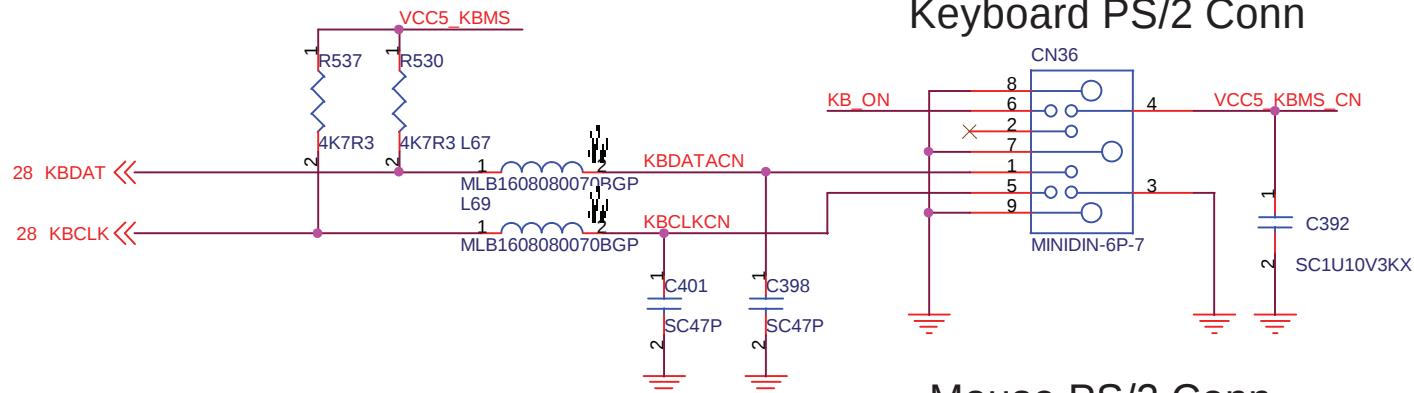
Modify 0510
/J361Y_Tracking (Item
other-063)

Modify 0517
/J361Y_Tracking (Item
other-070)

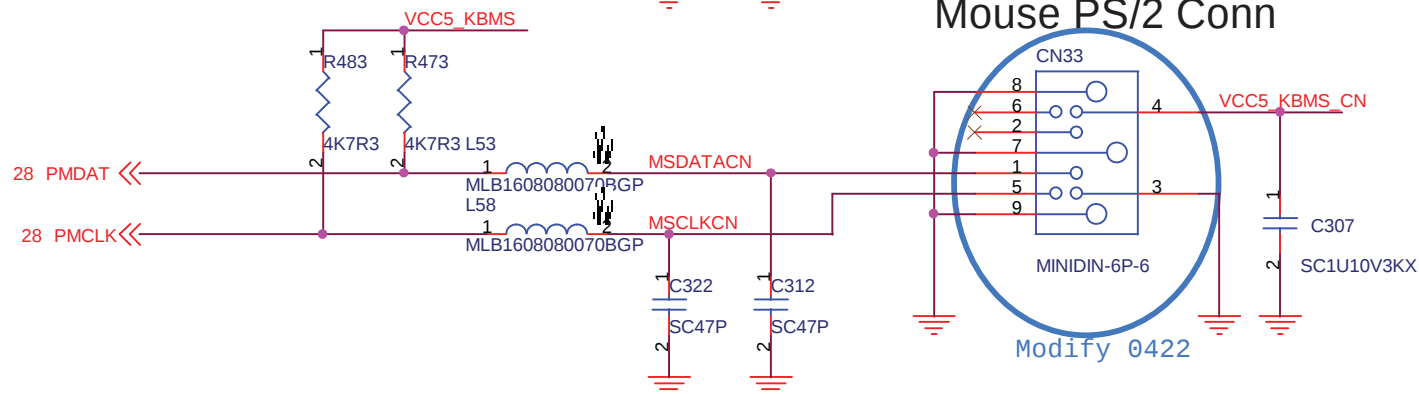
26,40,41 PBTNJ_CON << R518 1 2 0R3-U (R) KB_ON



Keyboard PS/2 Conn



Mouse PS/2 Conn



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

KB/MS PS2 Conn

Size
A

Document Number
J361Y RS482+M1573

Rev
1A

Date: Thursday, June 16, 2005

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28 PP[0..7]	PP[0..7]
28 STROB*	STROB*
28 AUTOFD*	AUTOFD*
28 ERRORP*	ERRORP*
28 PINT*	PINT*
28 SLCTIN*	SLCTIN*
28 PACK*	PACK*
28 BUSYP	BUSYP
28 PE	PE
28 SLCT	SLCT

Pin	Signal
1	RPSTROB*
2	RAUTOF
3	RPP0
4	ERRORP
5	RPP1
6	RPINIT*
7	RPP2
8	RSCLCTN
9	RPP3
10	
11	RPP4
12	
13	RPP5
14	
15	RPP6
16	
17	RPD7
18	
19	PACK*
20	
21	BUSYP
22	
23	PE
24	
25	SLCT
26	

ARC-CONN26A-FP

```

28 DCD*1  <-- DCD*1
28 RI*1   <-- RI*1
28 CTS*1  <-- CTS*1
28 DTR*1  <-- DTR*1
28 RTS*1  <-- RTS*1
28 DSR*1  <-- DSR*1
28 TXD1   <-- TXD1
28 RXD1   <-- RXD1

```

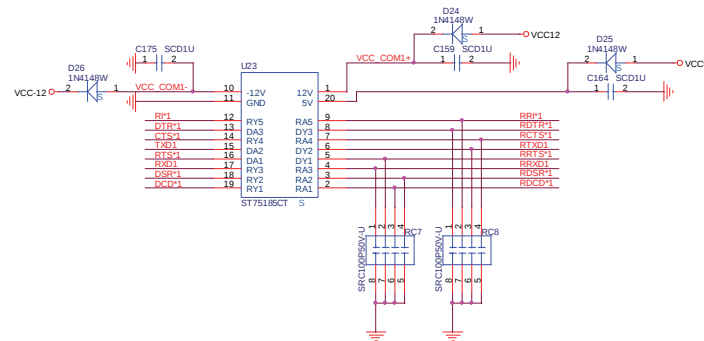


Diagram of the ARC-CONN10A-FP3 connector showing pin connections:

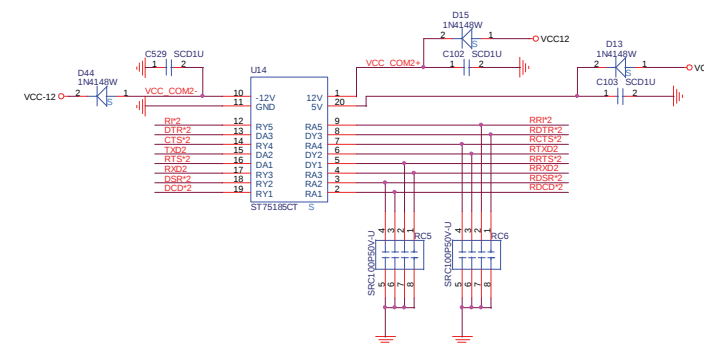
- Pin 1: RDCD*1
- Pin 2: RDSR*1
- Pin 3: RRXD1
- Pin 4: RRTS*1
- Pin 5: RTXD1
- Pin 6: RCTS*1
- Pin 7: RDTR*1
- Pin 8: RRP1
- Pin 9: Ground
- Pin 10: Marked with an X

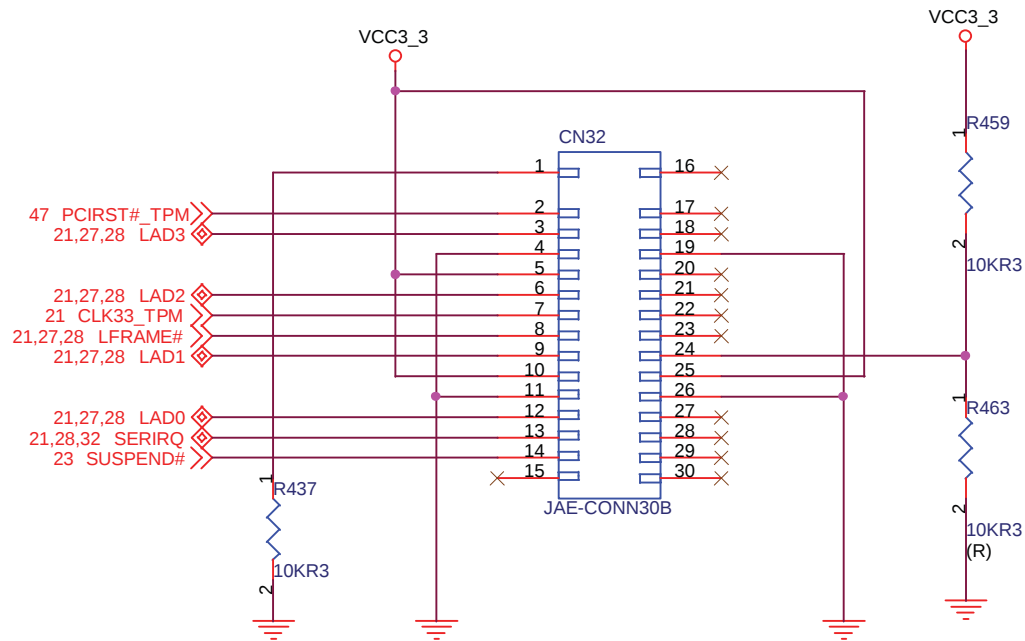
Diagram of the ARC-CONN10A-FP3 connector showing pin connections:

Pin	Signal
1	RDCD*2
2	RDSR*2
3	RRxD2
4	RRTS*2
5	RTxD2
6	RCTS*2
7	RDTR*2
8	RRF2
9	Ground
10	Not connected (X)

Connector Label: CN17
Part Number: ARC-CONN10A-FP3

28 DCD*2	DCD*2
28 RI*2	RI*2
28 CTS*2	CTS*2
28 DTR*2	DTR*2
28 RTS*2	RTS*2
28 DSR*2	DSR*2
28 TXD2	TXD2
28 RXD2	RXD2





<Core Design>



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Hsichih, Taipei

Title

TPM Header

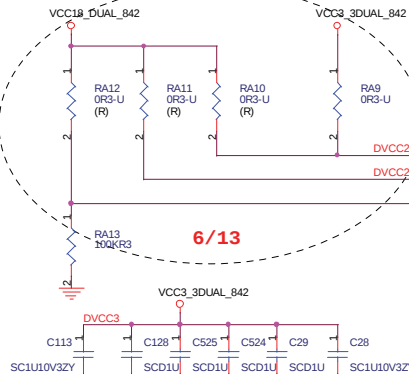
Size
A

Document Number
J361Y RS482+M1573

Rev
1A

Date: Thursday, June 16, 2005

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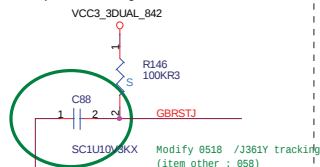
- 21.36,37 AD[0..31] << ADIO[31]
- 21.36,37 C_BEJ[0..3] << C_BEJ[0..3]
- 21.36 PGNTJ3 << PGNTJ3
- 21.36 PREQJ3 << PREQJ3
- 21.36,37 PAR << PAR
- 21.36,37 FRAMEJ << FRAMEJ
- 21.36,37 IRDYJ << IRDYJ
- 21.36,37 TRDYJ << TRDYJ
- 21.36,37 DEVSELJ << DEVSELJ
- 21.36,37 STOPJ << STOPJ
- 36.37 PERRJ << PERRJ
- 21.36,37 SERRJ << SERRJ
- 47 PCIRST#_842 << PCIRST#_842
- 21 CLK33_842 << CLK33_842
- 23.36,37 PME# << PCI_PMEJ
- 21.36 PIRQJA << PIRQJA
- 21.36 PIRQJB << PIRQJB
- 21.36 PIRQJC << PIRQJC
- 21.36 PIRQJD << PIRQJD

Modify 0422

AD21 R108 1 2 33R3 IDSEL 842

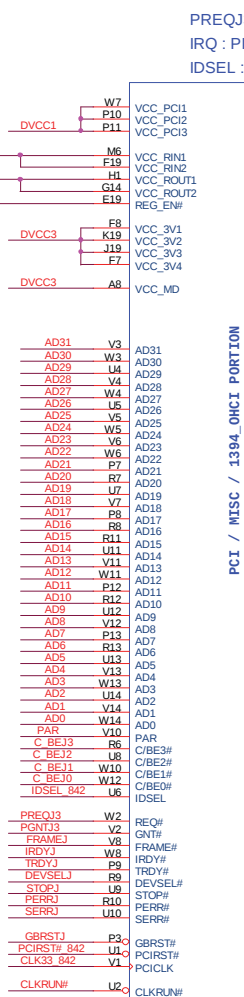
PowerOnReset for VccCore

*An option is available that GBRESET# is wired directly to PCIRST# when not using "wake up from D3" power-management scheme.



CoreLogic CLOCKRUN#

*When do not use, please pull down it thru 100k.



PREQJ3/PGNTJ3
IRQ : PIRQJD,A,B,C
IDSEL : AD21

U7B

AVCC_PHY1/NC#11

VCC_PC12

VCC_PC13

VCC_PC14

VCC_PC15

VCC_PC16

VCC_PC17

VCC_PC18

VCC_PC19

VCC_PC20

VCC_PC21

VCC_PC22

VCC_PC23

VCC_PC24

VCC_PC25

VCC_PC26

VCC_PC27

VCC_PC28

VCC_PC29

VCC_PC30

VCC_PC31

VCC_PC32

VCC_PC33

VCC_PC34

VCC_PC35

VCC_PC36

VCC_PC37

VCC_PC38

VCC_PC39

VCC_PC40

VCC_PC41

VCC_PC42

VCC_PC43

VCC_PC44

VCC_PC45

VCC_PC46

VCC_PC47

VCC_PC48

VCC_PC49

VCC_PC50

VCC_PC51

VCC_PC52

VCC_PC53

VCC_PC54

VCC_PC55

VCC_PC56

VCC_PC57

VCC_PC58

VCC_PC59

VCC_PC60

VCC_PC61

VCC_PC62

VCC_PC63

VCC_PC64

VCC_PC65

VCC_PC66

VCC_PC67

VCC_PC68

VCC_PC69

VCC_PC70

VCC_PC71

VCC_PC72

VCC_PC73

VCC_PC74

VCC_PC75

VCC_PC76

VCC_PC77

VCC_PC78

VCC_PC79

VCC_PC80

VCC_PC81

VCC_PC82

VCC_PC83

VCC_PC84

VCC_PC85

VCC_PC86

VCC_PC87

VCC_PC88

VCC_PC89

VCC_PC90

VCC_PC91

VCC_PC92

VCC_PC93

VCC_PC94

VCC_PC95

VCC_PC96

VCC_PC97

VCC_PC98

VCC_PC99

VCC_PC100

VCC_PC101

VCC_PC102

VCC_PC103

VCC_PC104

VCC_PC105

VCC_PC106

VCC_PC107

VCC_PC108

VCC_PC109

VCC_PC110

VCC_PC111

VCC_PC112

VCC_PC113

VCC_PC114

VCC_PC115

VCC_PC116

VCC_PC117

VCC_PC118

VCC_PC119

VCC_PC120

VCC_PC121

VCC_PC122

VCC_PC123

VCC_PC124

VCC_PC125

VCC_PC126

VCC_PC127

VCC_PC128

VCC_PC129

VCC_PC130

VCC_PC131

VCC_PC132

VCC_PC133

VCC_PC134

VCC_PC135

VCC_PC136

VCC_PC137

VCC_PC138

VCC_PC139

VCC_PC140

VCC_PC141

VCC_PC142

VCC_PC143

VCC_PC144

VCC_PC145

VCC_PC146

VCC_PC147

VCC_PC148

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VCC_PC161

VCC_PC162

VCC_PC163

VCC_PC164

VCC_PC165

VCC_PC166

VCC_PC167

VCC_PC168

VCC_PC169

VCC_PC170

VCC_PC171

VCC_PC172

VCC_PC173

VCC_PC174

VCC_PC175

VCC_PC176

VCC_PC177

VCC_PC178

VCC_PC179

VCC_PC180

VCC_PC181

VCC_PC182

VCC_PC183

VCC_PC184

VCC_PC185

VCC_PC186

VCC_PC187

VCC_PC188

VCC_PC189

VCC_PC190

VCC_PC191

VCC_PC192

VCC_PC193

VCC_PC194

VCC_PC195

VCC_PC196

VCC_PC197

VCC_PC198

VCC_PC199

VCC_PC200

VCC_PC201

VCC_PC202

VCC_PC203

VCC_PC204

VCC_PC205

VCC_PC206

VCC_PC207

VCC_PC208

VCC_PC209

VCC_PC210

VCC_PC211

VCC_PC212

VCC_PC213

VCC_PC214

VCC_PC215

VCC_PC216

VCC_PC217

VCC_PC218

VCC_PC219

VCC_PC220

VCC_PC221

VCC_PC222

VCC_PC223

VCC_PC224

VCC_PC225

VCC_PC226

VCC_PC227

VCC_PC228

VCC_PC229

VCC_PC230

VCC_PC231

VCC_PC232

VCC_PC233

VCC_PC234

VCC_PC235

VCC_PC236

VCC_PC237

VCC_PC238

VCC_PC239

VCC_PC240

VCC_PC241

VCC_PC242

VCC_PC243

VCC_PC244

VCC_PC245

VCC_PC246

VCC_PC247

VCC_PC248

VCC_PC249

VCC_PC250

VCC_PC251

VCC_PC252

VCC_PC253

VCC_PC254

VCC_PC255

VCC_PC256

VCC_PC257

VCC_PC258

VCC_PC259

VCC_PC260

VCC_PC261

VCC_PC262

VCC_PC263

VCC_PC264

VCC_PC265

VCC_PC266

VCC_PC267

VCC_PC268

VCC_PC269

VCC_PC270

VCC_PC271

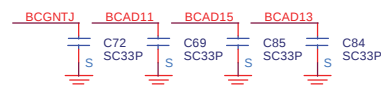
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VCC_PC273

VCC_PC274

CARDBUS / MEDIA CARD PORTION

MDIO10	F10	MDIO10	35
MDIO11	F10	MDIO11	35
MDIO12	F11	MDIO12	35
MDIO13	F12	MDIO13	35
MDIO14/NC	F12	MDIO14	35
MDIO15/NC	F13	MDIO15	35
MDIO16/NC	F14	MDIO16	35
MDIO17/NC	F14	MDIO17	35
MDIO18/NC	E15	MDIO18	35
MDIO19/NC	C16	MDIO19	35



35 MDIO8

35 MDIO9

C9

E9

F9

MDIO07

MDIO08

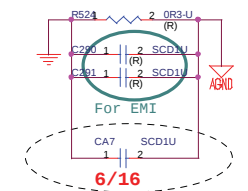
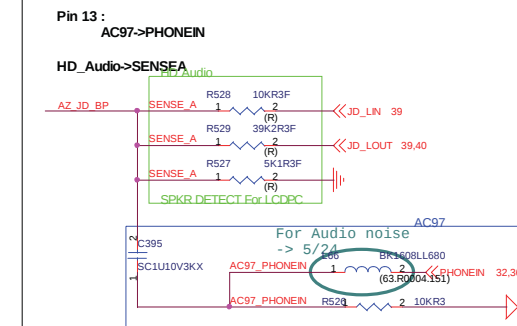
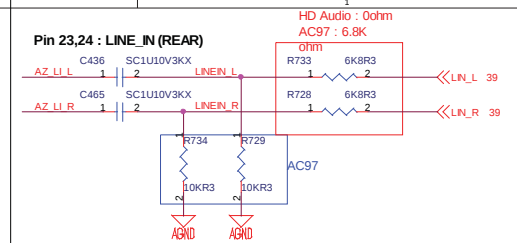
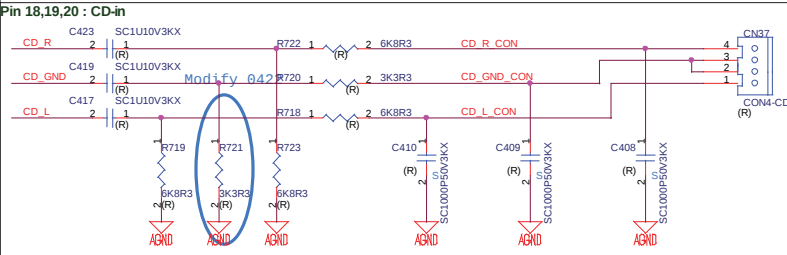
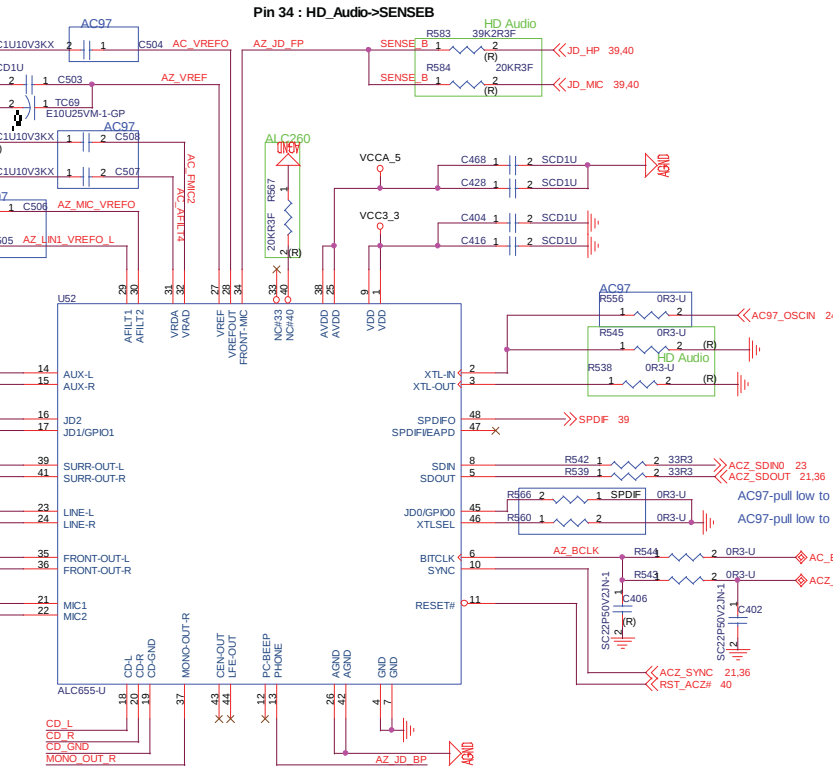
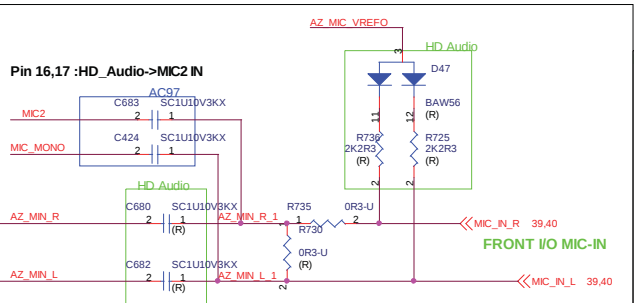
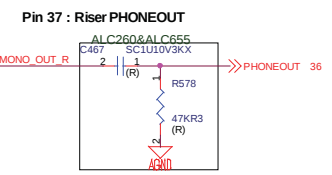
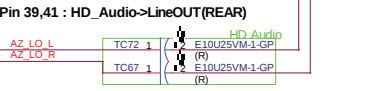
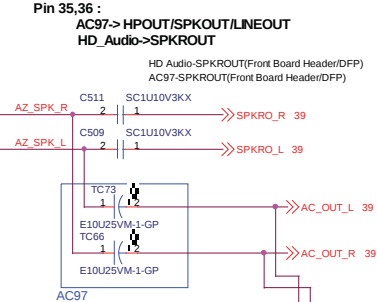
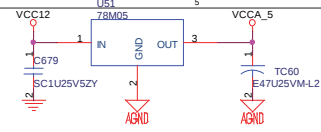
MDIO09



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AC97 Audio Codec :ALC250/ALC655 HD Audio Codec: ALC260/ALC880



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Audio Codec			
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AC97



<http://hobi-elektronika.net>

Front I/O HeadPhone



HD Audio: 0 ohm
AC97 : 33k ohm



— — — — —

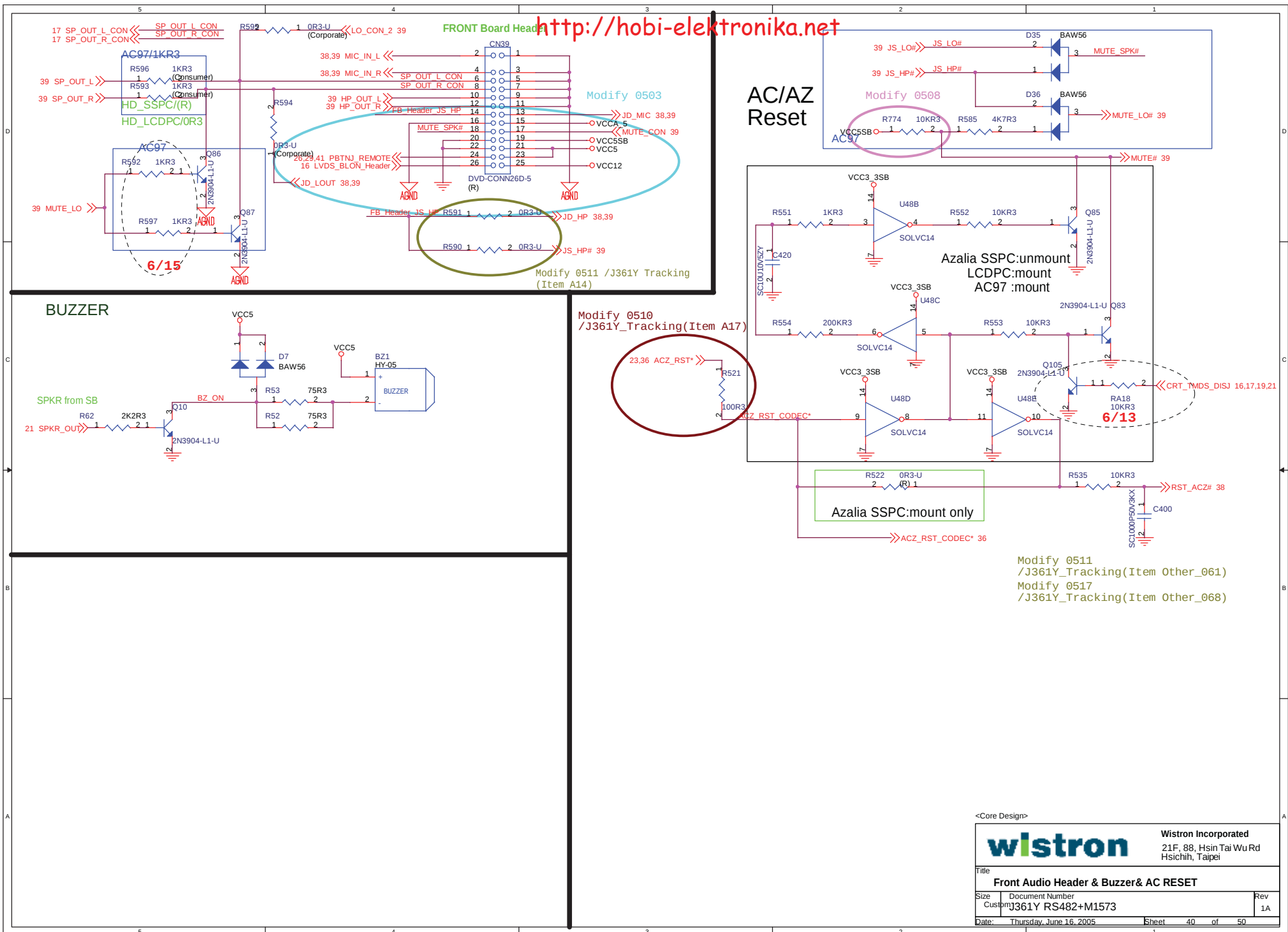
38 JD_LN << JD_LN



Title
AUDIO CONN

AUDIO CONN	
Size	Document Number

Date: Thursday, June 16, 2006



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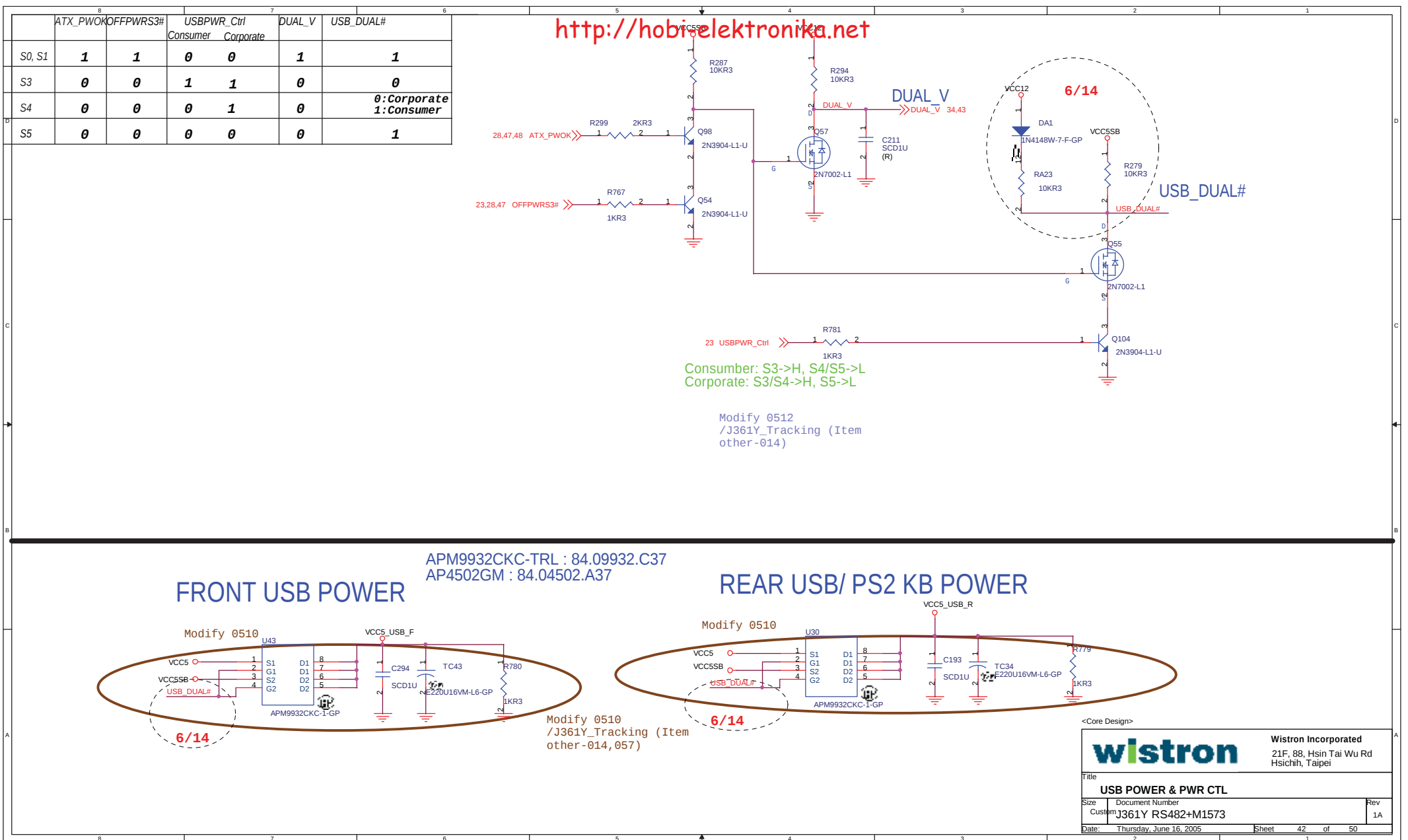
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Front Audio Header & Buzzer & AC RESET

Size Document Number
Custom J361Y RS482+M1573

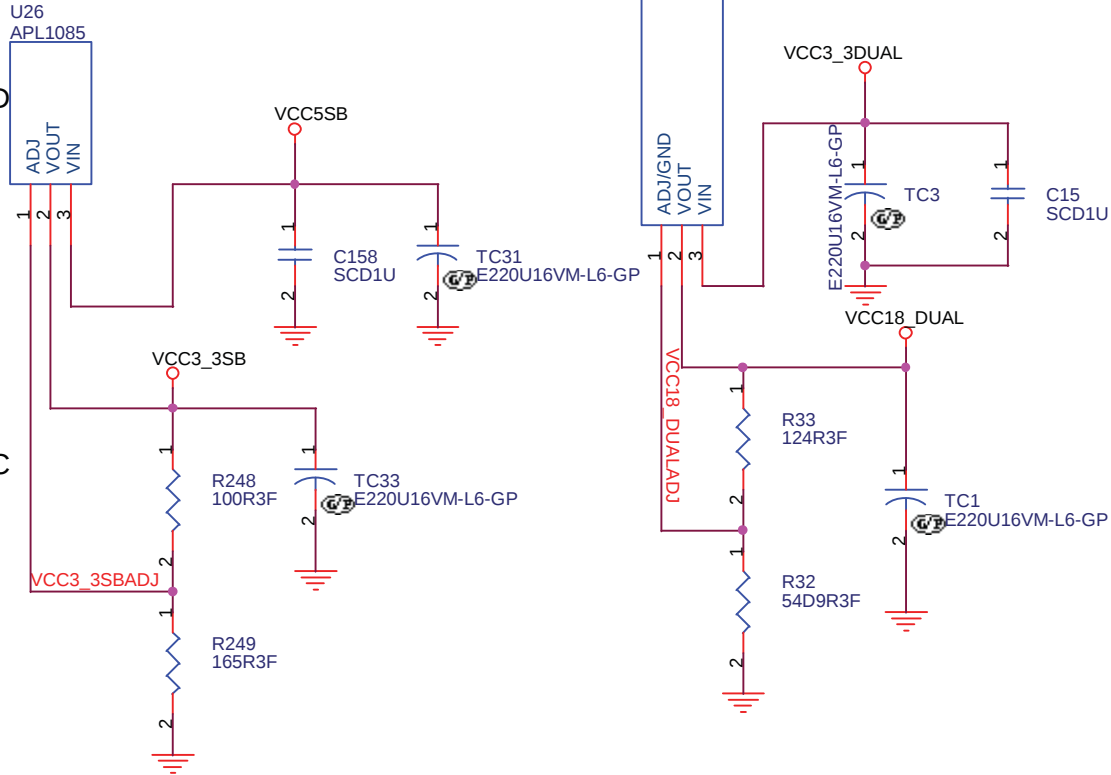
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1A

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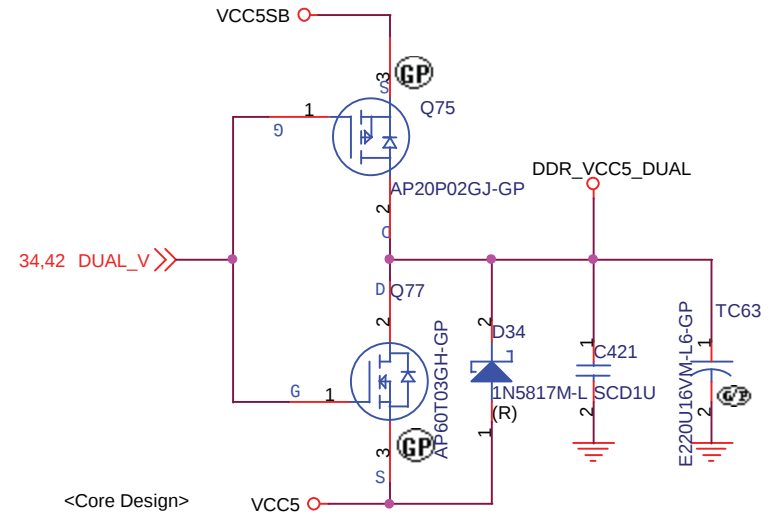


VCC3_3SB



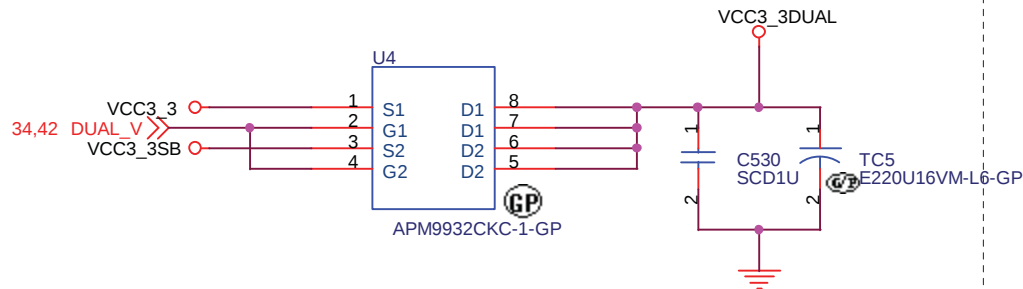
VCC18_DUAL for SB Resume Power

DDR_VCC5_DUAL FOR DDR & Card bus



VCC3_3 DUAL

APM9932CKC-TRL : 84.09932.C37
AP4502GM : 84.04502.A37



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Dual 5V, 3.3V, 1.8V, and 3.3VSB

Size

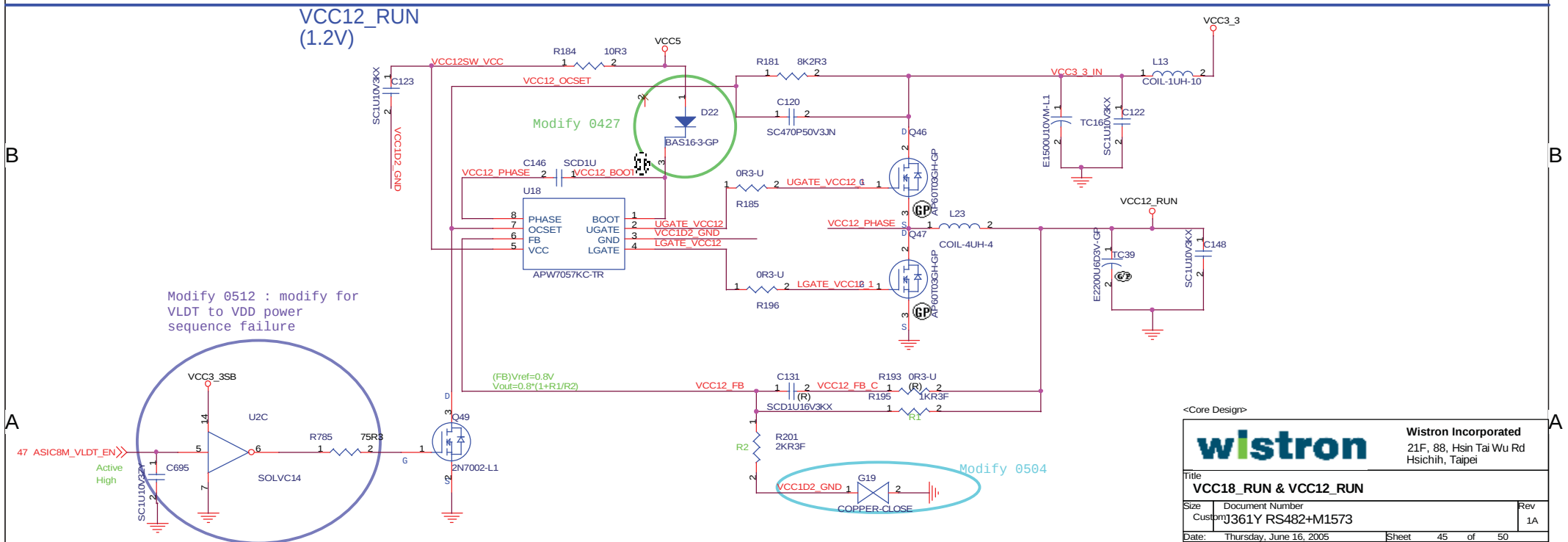
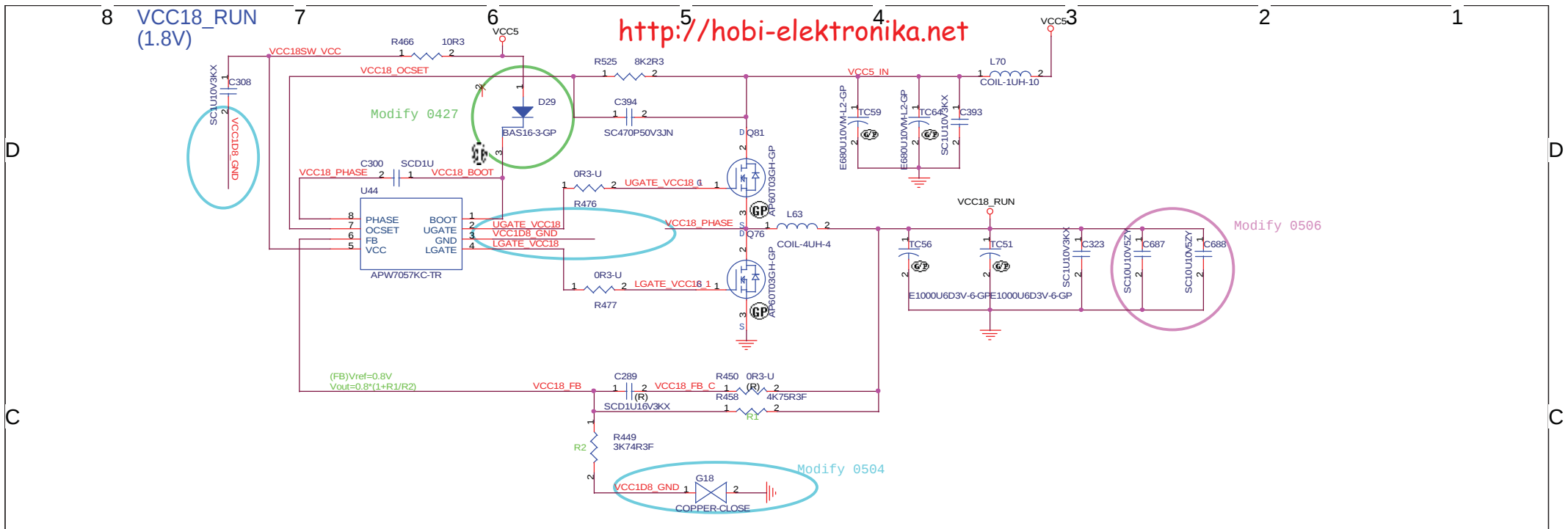
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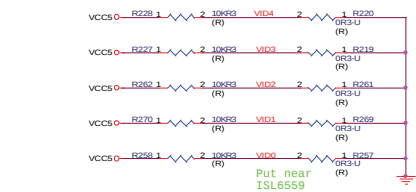
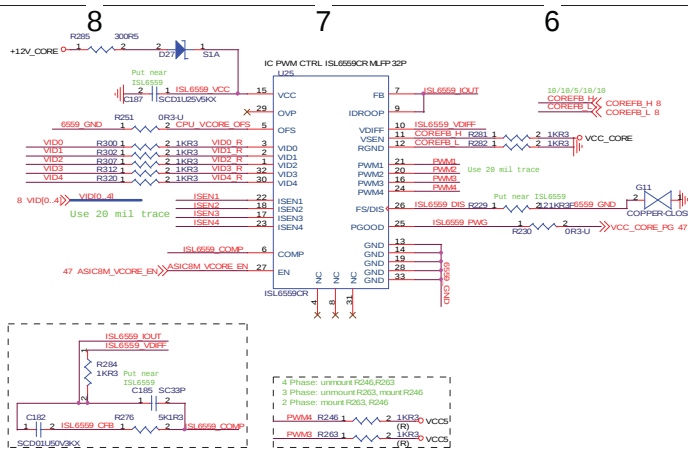
Rev

1A

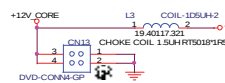
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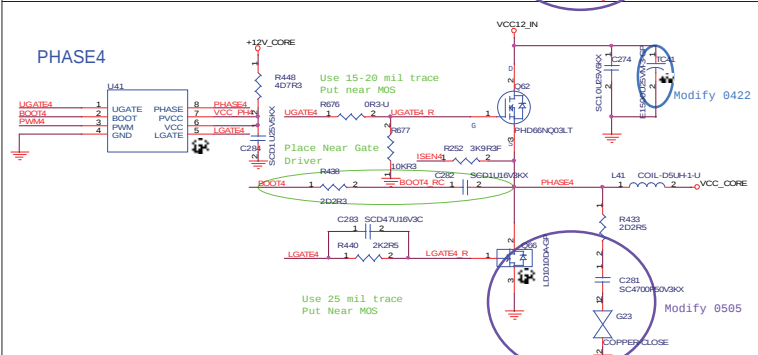
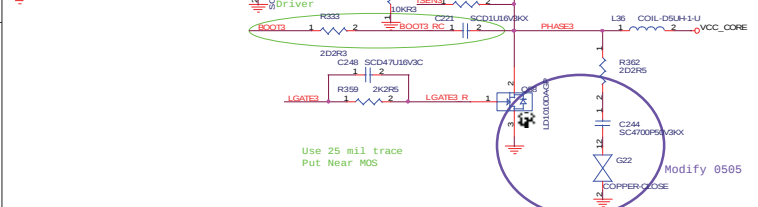
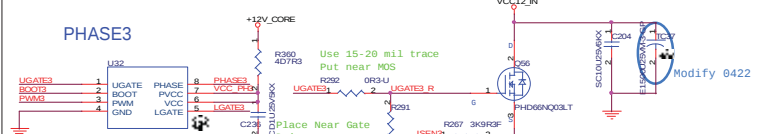
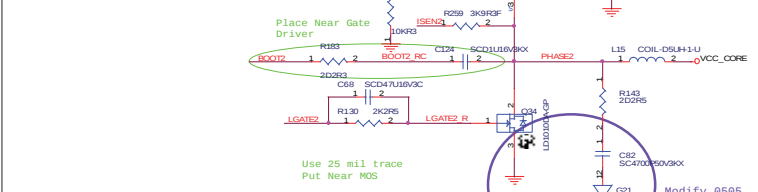
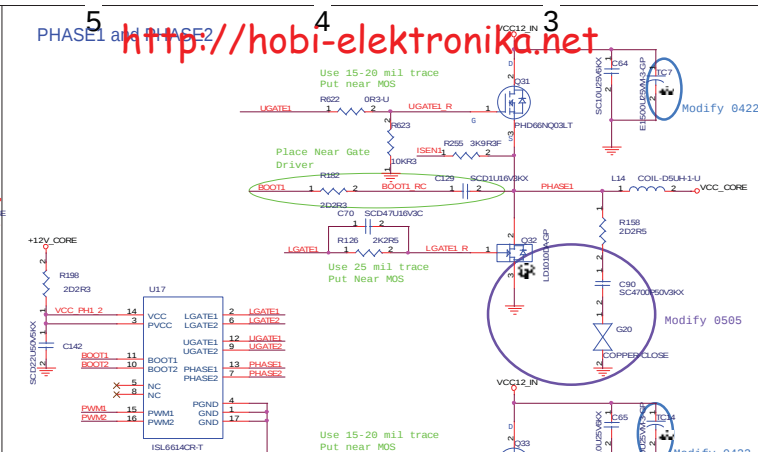
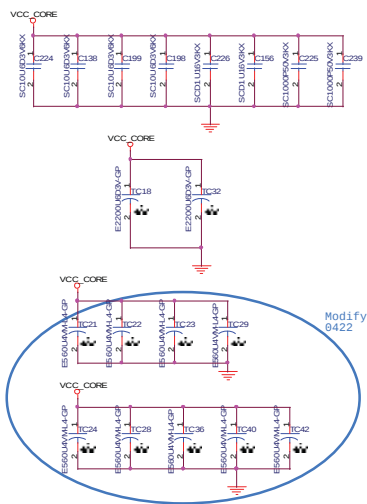




4 pin POWER Connector

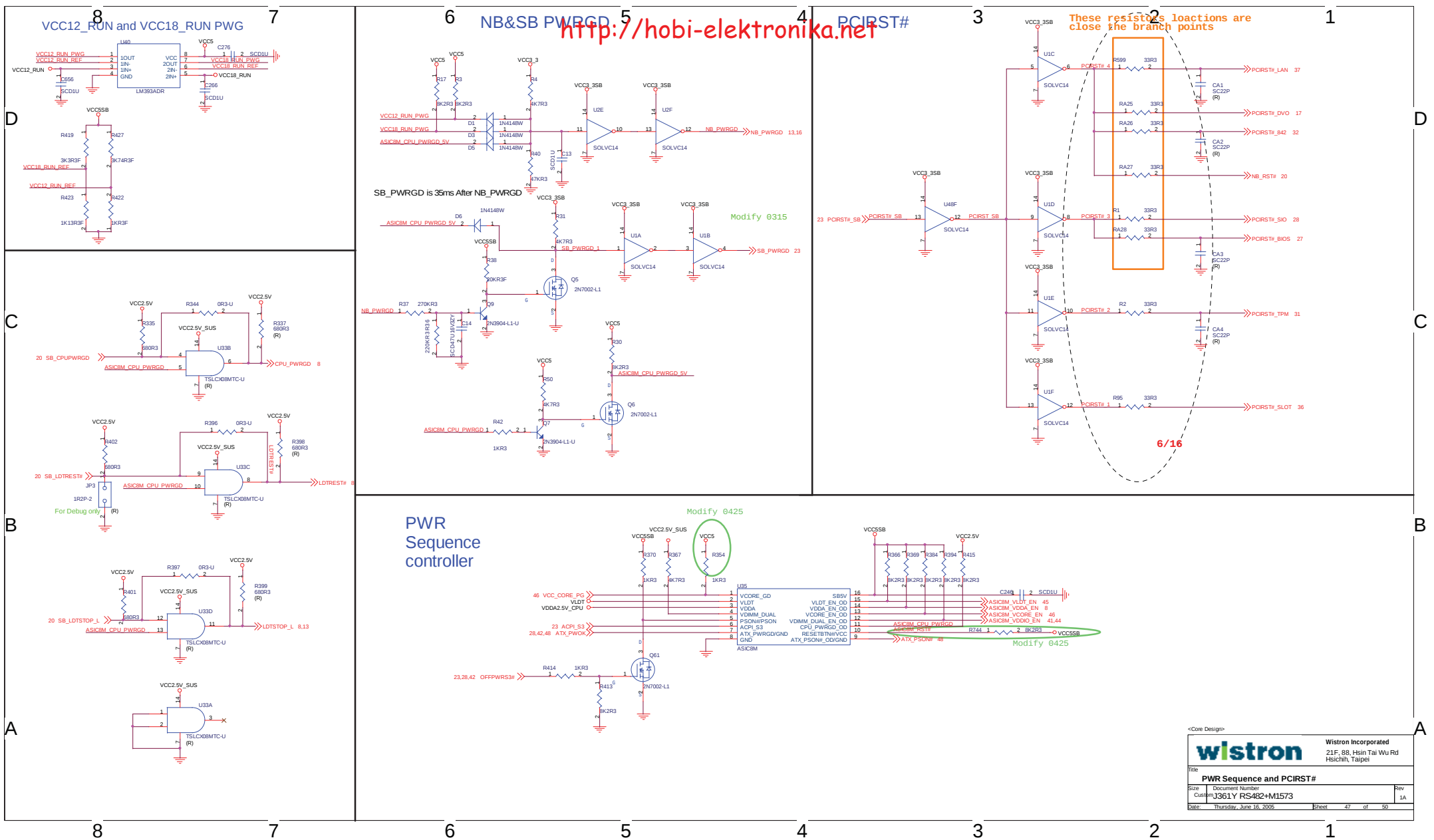


Output Capacitors

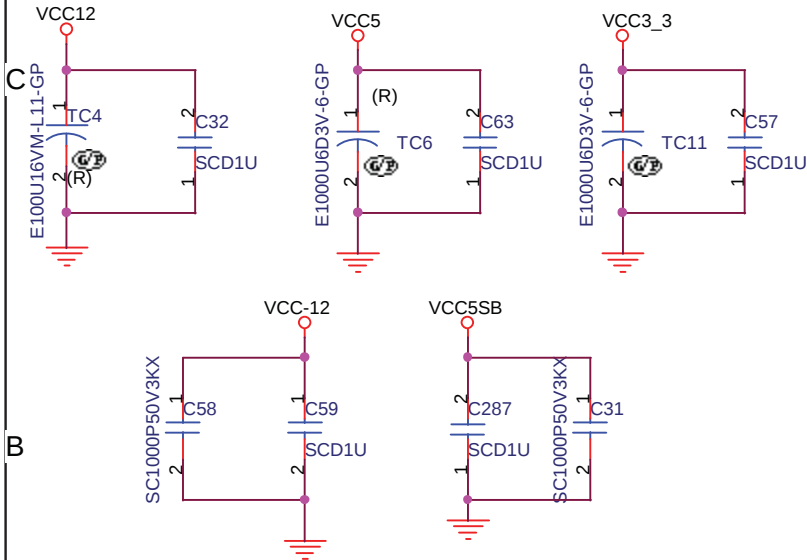
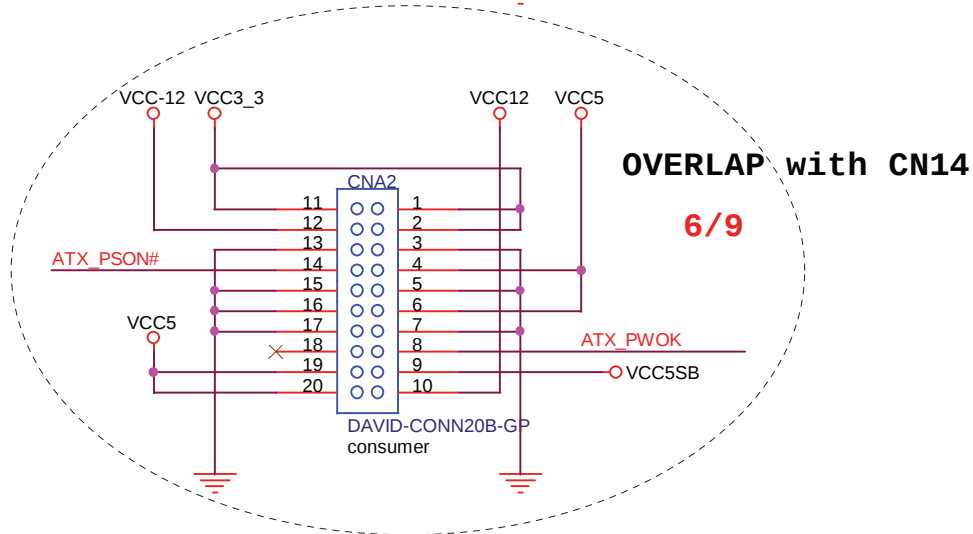
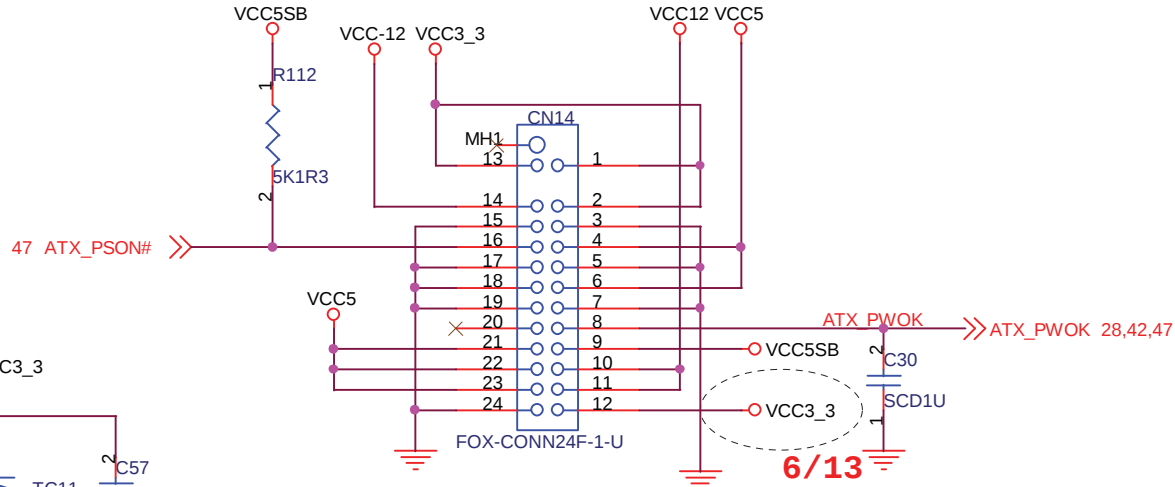
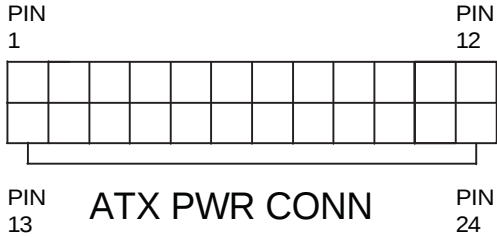


VID Codes

CORE (V)	VID4	VID3	VID2	VID1	VID0
1.550	0	0	0	0	0
1.525	0	0	0	0	1
1.500	0	0	0	1	0
1.475	0	0	0	1	1
1.450	0	0	1	0	0
1.425	0	0	1	0	1
1.400	0	0	1	1	0
1.375	0	0	1	1	1
1.350	0	1	0	0	0
1.325	0	1	0	0	1
1.300	0	1	0	1	0
1.275	0	1	0	1	1
1.250	0	1	1	0	0
1.225	0	1	1	0	1
1.200	0	1	1	1	0
1.175	0	1	1	1	1
1.150	1	0	0	0	0
1.125	1	0	0	0	1
1.100	1	0	0	1	0
1.075	1	0	0	1	1
1.050	1	0	1	0	0
1.025	1	0	1	0	1
1.000	1	0	1	1	0
0.975	1	0	1	1	1
0.950	1	1	0	0	0
0.925	1	1	0	0	1
0.900	1	1	0	1	0
0.875	1	1	0	1	1
0.850	1	1	1	0	0
0.825	1	1	1	0	1
0.800	1	1	1	1	0
OFF	1	1	1	1	1



PWR CONN



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ATX 24Pin conn

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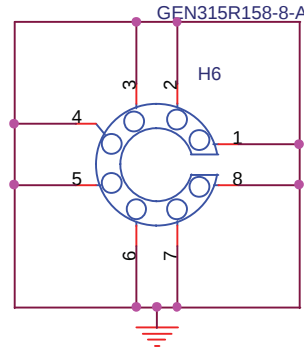
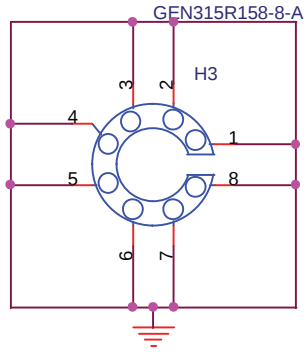
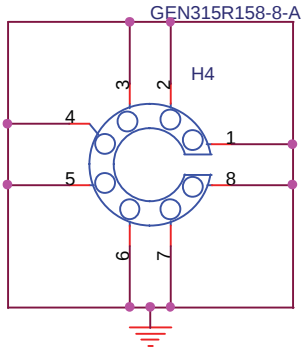
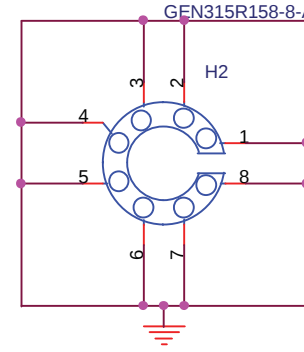
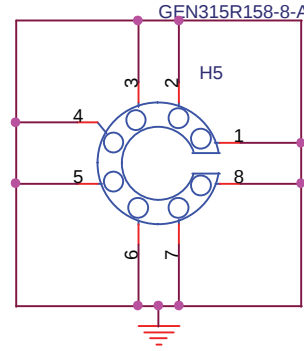
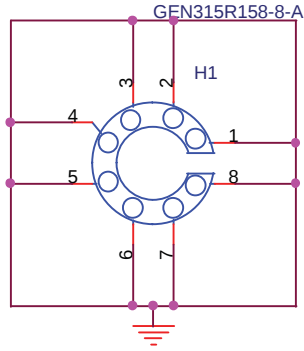
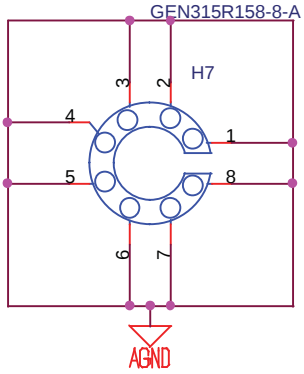
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Screw Hole

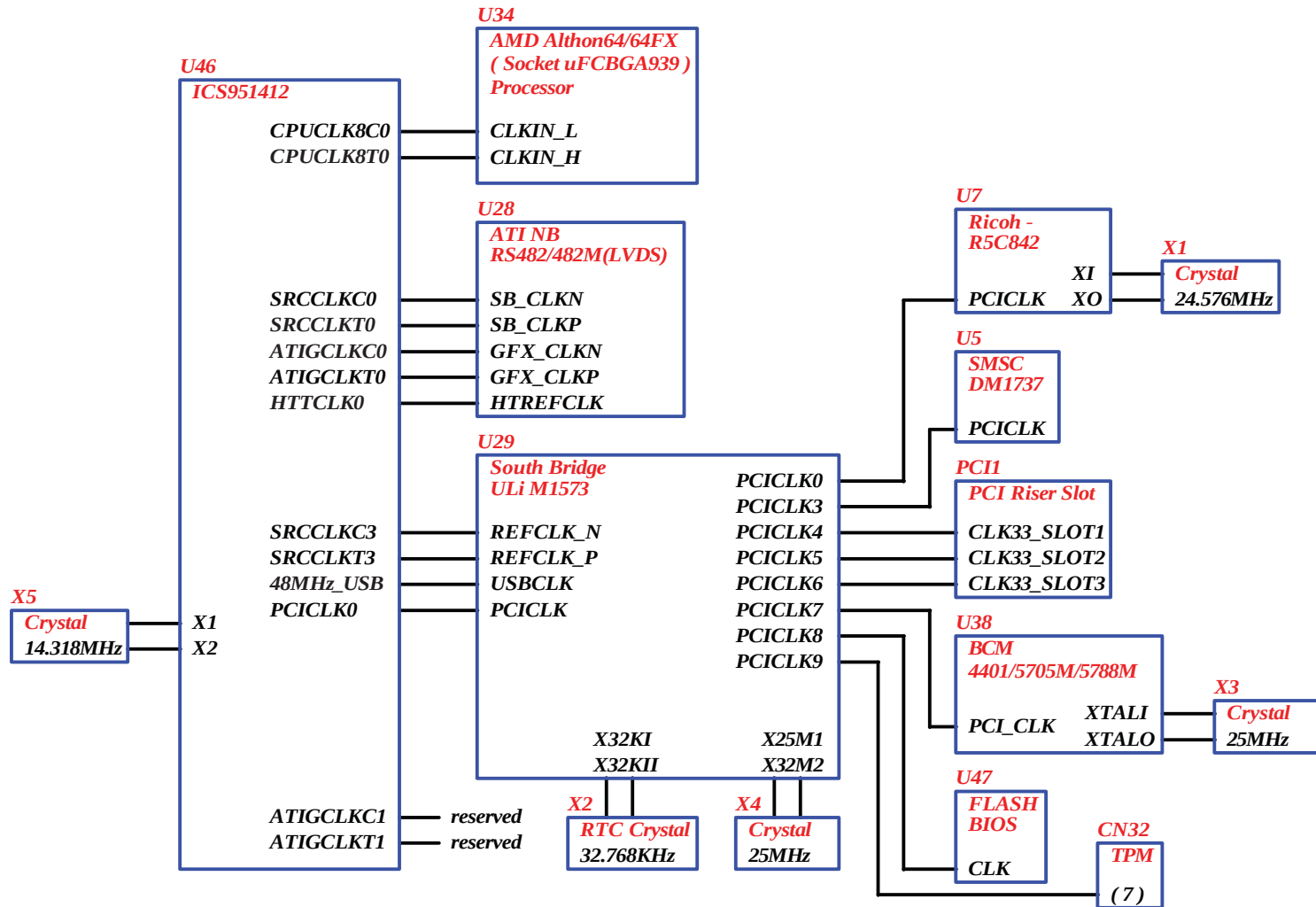
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EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

ATIGCLK Divider Selection

ATIG_Div(3:0)	ATIGCLK(1:0) (MHz)
1 0 0 0	100.00
0 0 1 1	114.29
TBD	133.33
0 0 1 0	160.00

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CLOCK MAP

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