J361Y-SB Rev_V3.06(06/16/2005)
91.3H801.001

Sheet

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Title: **Cover Page**

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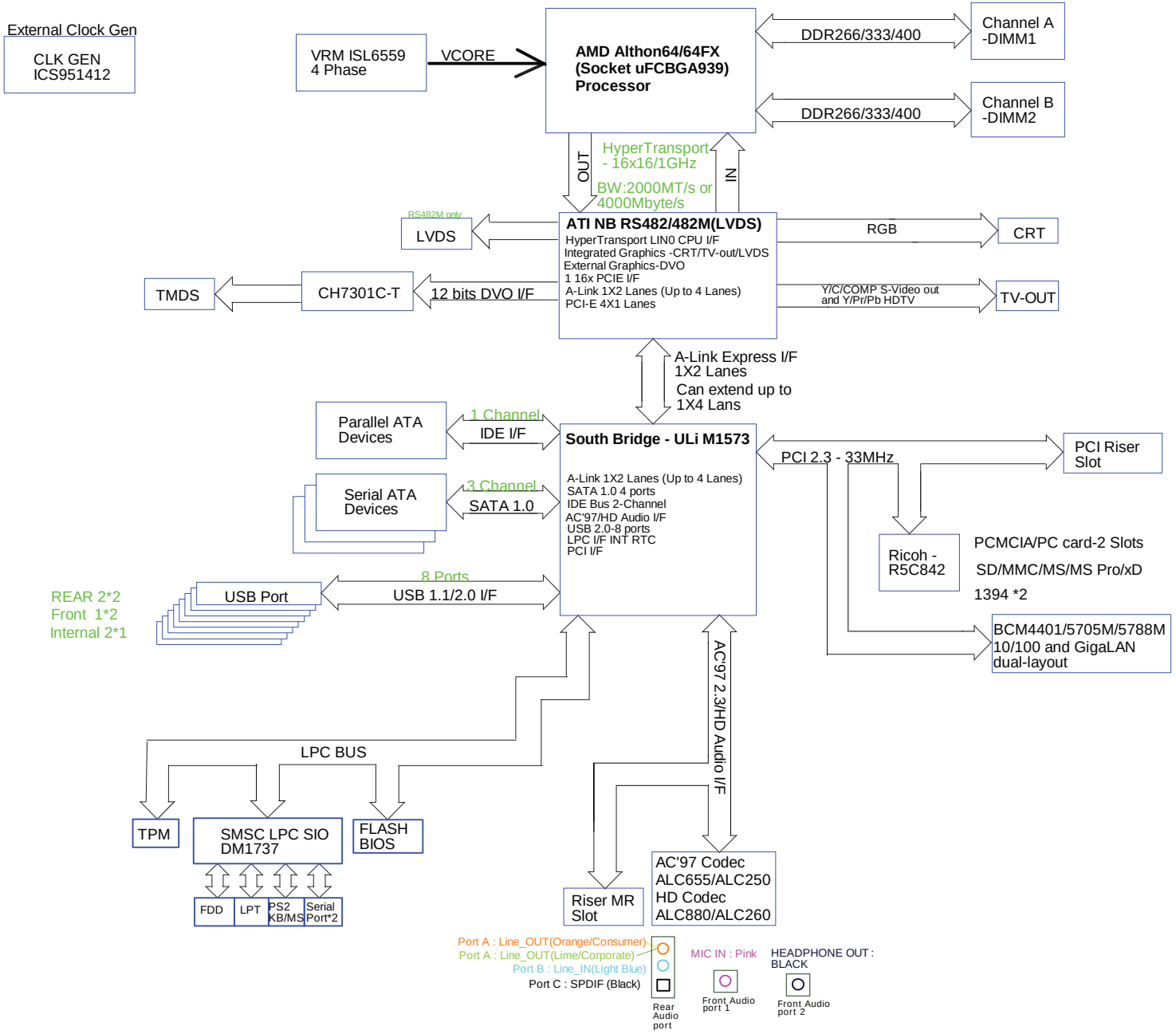
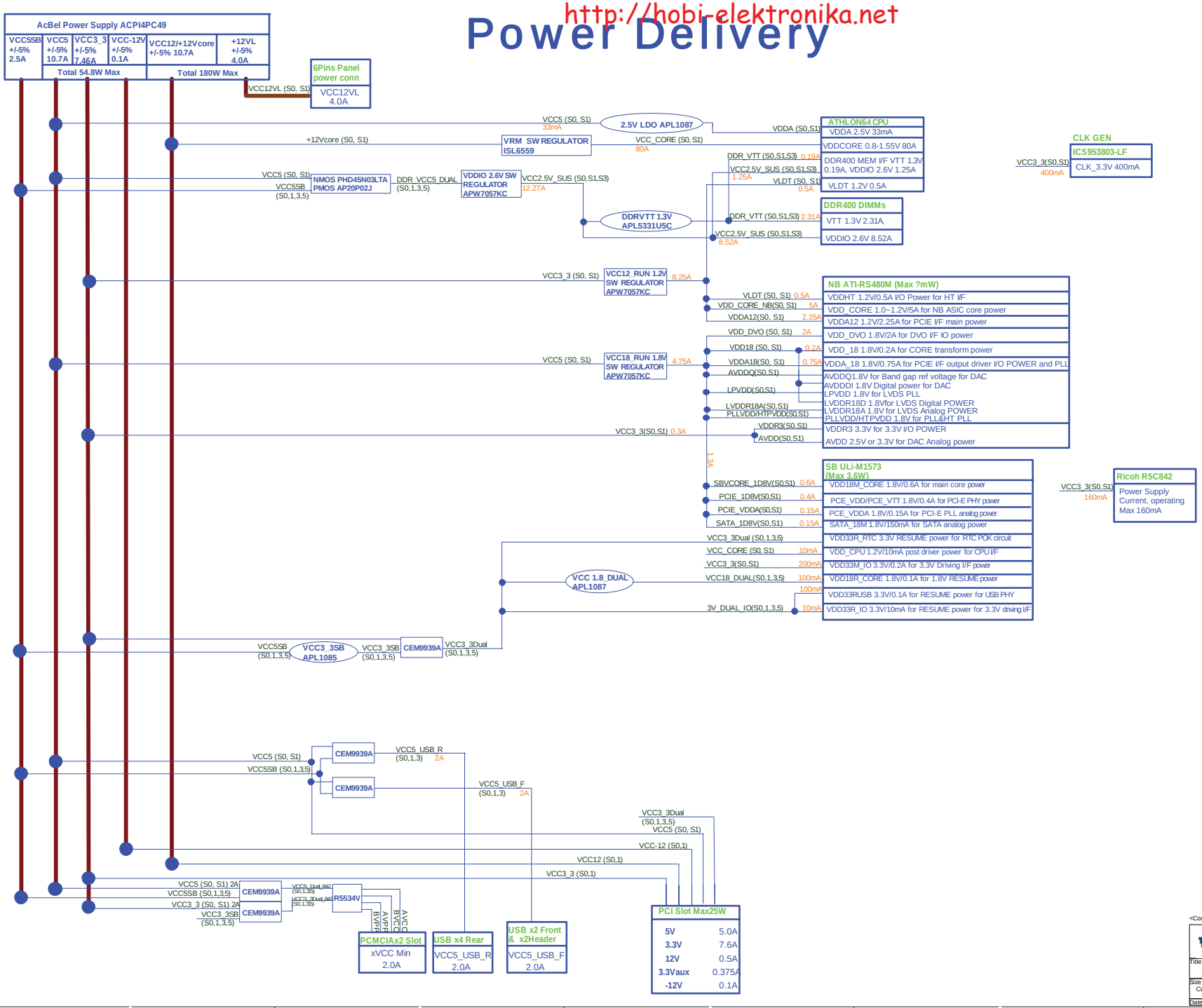
Block Diagram



Power Delivery



PME event output

PCI

Device	IDSEL	GNTJ/REQJ	IRQ	Active Status
R5C842	AD21	PREQJ3/PGNTJ3	PIRQJD,A,B,C	LOW
PCI RISER	AD19 AD20	PREQJ0/PGNTJ0 PREQJ1/PGNTJ1	PIRQJA,B,C,D PIRQJB,C,D,A	LOW
PCI LAN	AD22	PREQJ4/PGNTJ4	PIRQJE	LOW

SMSC DM1737

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
GP10	RST_IDE*		O	MAIN (VCC)	Low
GP11	PCIRST_OUT1	LAN_DISJ	O	AUX (VTR)	Low/Default high
GP12			O	AUX (VTR)	
GP13		SLP_S1_S5_L*	O	AUX (VTR)	Low@S0/ S1/ S3 / High@S4/ S5
GP14	PCIRST_OUT4	SUSLED*	O	AUX (VTR)	Low
GP21	KBDATA		I	MAIN (VCC)	
GP22	KBCLK		I	MAIN (VCC)	
GP27			I	MAIN (VCC)	
GP32	MSDATA		I	MAIN (VCC)	
GP33	MSCLK		I	MAIN (VCC)	
GP36	KBRST*		I	MAIN (VCC)	Low
GP37	A20GATE		I	MAIN (VCC)	
GP40			O	MAIN (VCC)	
GP42	IO_PMES3#		O	AUX (VTR)	PME event output
GP43	IO_PMES5#		O	AUX (VTR)	PME event output
GP50	RI*2		I	MAIN (VCC)	
GP51	DCD*2		I	MAIN (VCC)	
GP52	RXD2		I	MAIN (VCC)	
GP53	TXD2		I	MAIN (VCC)	
GP54	DSR*2		I	MAIN (VCC)	
GP55	RTS*2		I	MAIN (VCC)	
GP56	CTS*2		I	MAIN (VCC)	
GP57	DTR*2		I	MAIN (VCC)	
GP60		TVLED*	O	AUX (VTR)	High / push-pull
GP61		LCDONJ_SIO	O	AUX (VTR)	Low/ S5 wake up event

ATI RS482/482M

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
DFT_GPIO0			I	VDDR3	
DFT_GPIO1	LOAD_ROM_STRAPS#		I	VDDR3	Low
DFT_GPIO2		TV_SWITCH	O	VDDR3	1:D-Video 0:S-Video
DFT_GPIO3		D_PLUGDET	I	VDDR3	0: HDTV connected 1: HDTV unconnected
DFT_GPIO4			I	VDDR3	
DFT_GPIO5	LOAD_MEM_STRAPS#		I	VDDR3	Low

ULi M1573

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
RUNGPIO0		IDE_P	I	VDD33M_IO	High
RUNGPIO1			O	VDD33M_IO	LOW
RUNGPIO2				VDD33M_IO	
RUNGPIO3		MO_DET	I	VDD33M_IO	0: MO connected 1: MO unconnected
RUNGPI18	ACB_BITCLK	BOARD_ID_0	I	VDD33M_IO	
RUNGPI11	VOL_UP#	BOARD_ID_1	I	VDD33M_IO	
RUNGPI12	VOL_DOWN#	BOARD_ID_2	I	VDD33M_IO	
RUNGPI13	VOL_MUTE#	BOARD_ID_3	I	VDD33M_IO	
RUNGPI9	CLKRUN#	CRT_TMDS_DISJ	O	VDD33M_IO	HIGH
RUNGPO[13]	CPUHI#	Blueled*	O	VDD33M_IO	HIGH
RUNGPO[16]	IGNNE#	Blueled02*	O	VDD33M_IO	HIGH
RUNGPO[19]	NMI	HDDLED	O	VDD33M_IO	HIGH
RUNGPO[21]	SMI#	Blueled03*	O	VDD33M_IO	HIGH
SATA_GPI0		LCD_VID0	I	VDD33M_IO	
SATA_GPI1		LCD_VID1	I	VDD33M_IO	
SATA_GPI2		LCD_VID2	I	VDD33M_IO	
SATA_GPI3			I	VDD33M_IO	
SATA_GPO0			O	VDD33M_IO	LOW
SATA_GPO1		FlashROM_WP	O	VDD33M_IO	High/Default LOW
SATA_GPO2			O	VDD33M_IO	LOW
SATA_GPO3		PWRLED*	O	VDD33M_IO	LOW
RSMGPIO0		USBPWR_Ctrl	O	VDD33R_IO	Consumer: S3->H, S4/S5->L Corporate: S3/S4->H, S5->L
RSMGPIO1		ACPILED*	O	VDD33R_IO	HIGH
RSMGPIO2		ACPI_S3	O	VDD33R_IO	S3:High
RSMGPIO3		842HWSPNDJ	O	VDD33R_IO	High
RSMGPI10	SMBALERT#	IO_PMES3#	I	VDD33R_IO	PME event input
RSMGPIL[0]	SLPBTN#	IO_PMES5#	I	VDD33R_IO	PME event input

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Title: GPIO Table

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Rev. Notes

DATE	Rev	Description	Page
3/10	SA_V1.0	Release Schematic	
	SA_V1.1	Add Board_ID_[3..0] setting	22
		Add PIRQ#[E:H] pull high	36
		Add CN41	28
		HW strapping setting	13,21,22,23
		Modify Front HP OUT Mute circuit	39
		Two copper pure for VTT fill - at least 100mils wide/Change DDR_VTT_CPU as DDR_VTT	7,8
		Modify Net REFCLK0_1 and REFCLK0_2	24
3/14		Connect ASIC8M_CPU_RST to LDTRST#	47
		Change R92 to 2.4K ohm	17
		Modify DVO_IDCKN and DVO_IDCKP	17
		Modify TMDS HotPlug circuit	17
		Modify TV-out I2C circuit	18
3/15		Modify VDD_DVO power for RS482 revA11	15
		Modify DVO_VREF circuit	17
3/15	SA_V1.2	Change L33	22
		Modify VRM Circuit (Vendor suggestion)	46
		Change M1573 HW strapping resistors to 1K ohm	21
		Change R536 and R538 to 1K ohm and change R554 to 5.1K (Vendor suggestion)	46
		Modify SB&NB POWER Good circuit	47
3/16	SA_V1.3	Modify DLINE circuit	18
		Modify TMDS Hot plug circuit	15
3/16	SA_V1.4	Move R664 and R97 to Page17. Delete R665 and R666	13,17,19
		Delete R669 and R670	18
		Delete TC86	32
		Modify DLINE circuit	18
		Change M1573 to RevA1D	20-23
		Add LAN Disable circuit	37
3/19	SA_V1.5	Delete TC39 for Extra 4 CPU FANSINK screw hole	46
		Change C763 to a small size	40
		Modify FJ's checklist items	
3/21	SA_V1.6	SWAP USB Port	26
	SA_V1.7	SMBCLK and SMBDATA (SIO Page)	28
		Modify SUSLED* circuit	41
		Change R74 and R75 to 8.25K and 82.5 ohm (ATI PA_RS4X0F4.pdf	14
		Modify NB_RST* circuit	20
3/22	SA_V1.8	Modify LAN Disable circuit	37
3/23	SA_V1.9	Add 6559_Common Ground	46
	SA_V1.10	Change PCIRST circuit from VCC3_3DUAL driven to VCC3_3SB	
		USE CLKRUN# of M1573(RUNGPO9) to disable CRT and TMDS	
		Modify GPIO arrangement	
		Add another pair of SM bus dedicate for CLK GEN and DDR	
3/24	SA_V1.11	Net Swap	
3/25	SA_V1.12	Add Two capacitors for EMI	38
	SA_V1.13	Change Q70 to 3904 NPN BJT	42
3/30	SA_V1.16	Rename Reference and swap nets	
3/31	SA_V1.17	Connect H7 to AGND	
4/06	SA_V1.18	Add CLOCK MAP	50

NOTE :

DATE	Rev	Description	Page
0422	SB_V2.0	Modify All SA P/R rework items and FJ GFX_Feedback	
0426	SB_V2.1	Modify R354 and R744 and FJ GFX Feedback ver.0427	47
0427		Swap ACZ_SDIN0 and ACZ_SDIN1 at SB side	23
	SB_V2.2	LO_R can't be connected with Mute_LO.	39
		Add R746/R747/R748	23
		Change C257 to 0.018uF and R418 to 60.4 ohm	44
		Add R749	27
		Modify LAN_RSTJ signal	37
		Remove JP2 and around circuit	21
		Change Pin assignment of CN39	40
		Modify LCD PWRON circuit	37
		Add USB ESD IC	26
		Add COMMON GND for SW regulator	44,45
		Change TC35 to 220uF	
0505	SB_V2.3	Add common ground near VRD low side MOS	46
		Modify SUSLED circuit	41
		Modify FAN Tach circuit	41
		Modify GPIO assignment for LED function	
		Modify PCI Riser IDSEL	36
		Add FlashRom_write protect function	
		Add Two more GPIO pin for IO_PMES3# and IO_PMES5#	
0508	SB_V2.5	Modify USBPWR control circuit	42
		Modify SUSLED circuit	41
		Modify TVON_Plug circuit	41
		Modify All LED circuit	41
		Modify BIOS write protection circuti	27
		Add a pull-up resistor on Mute#	40
		Change R557 to 100K ohm	
0509	SB_V2.6	Modify VDDA_2.5V_CPU Enable circuit	08
		1394 port 0 and port1 swap	
0510	SB_V2.7	Remove Q73 and ACZ_RST_CRL*	40
		Modify All LED circuit	41
		Modify USB POWER controller circuit	42
		Add two 1K ohm between VCC5_USB_F"/VCC5USB_R" and GND	42
		Remove D31 and R517. Then change R518 from 1k-ohm to 0ohm and unmount as default.	29
		[ESD for DDC]	17/19
0511	SB_V2.8	Add SLP_S4_H to control USB power	23/42
		Change R775.1 to VCC5	08
		Modify TVON_PLUSE3.jpg	28/41
	SB_V2.9	Change Q55 to 2N7002 and remove R768	41
	SB_V2.10	USE CRT_TMDS_DISJ to do mute function	40
		Change BOM option for Audio function	40
		Reserve 3.3V pull-up for Fansink	41
0512	SB_V2.11	Modify VLDT_EN circuit	45
		Modify USB power control circuit	42
0513	SB_V2.12	Unmount R8	41
0517	SB_V2.13	Change Q105 to FET(2N7002)	40
		Change Board ID — Consuemr M/B: Board_ID[3..0] = "0001"; Corporate M/B: Board_ID[3..0] = "1000"; Small Qty M/B: Board_ID[3..0] = "0010"	21
		Change C67 to X7R	16
		Change R512 for Consumer/LCDPC ,Change R508 for Corporate	29
		Change C88 and C413 to X5R	32 26
		mount C691 and C692	24
		R13 R14 change to 1Kohm , RN1 change to 1K ohm	28
		U58 U59 U60 change to 83.01293.0AE	26
0524		R129 unmount, L66 change to 63.R0004.151	32 38
0525		R59 R777 change to 0 ohm, Q103 Q15 change to 2N7002	41

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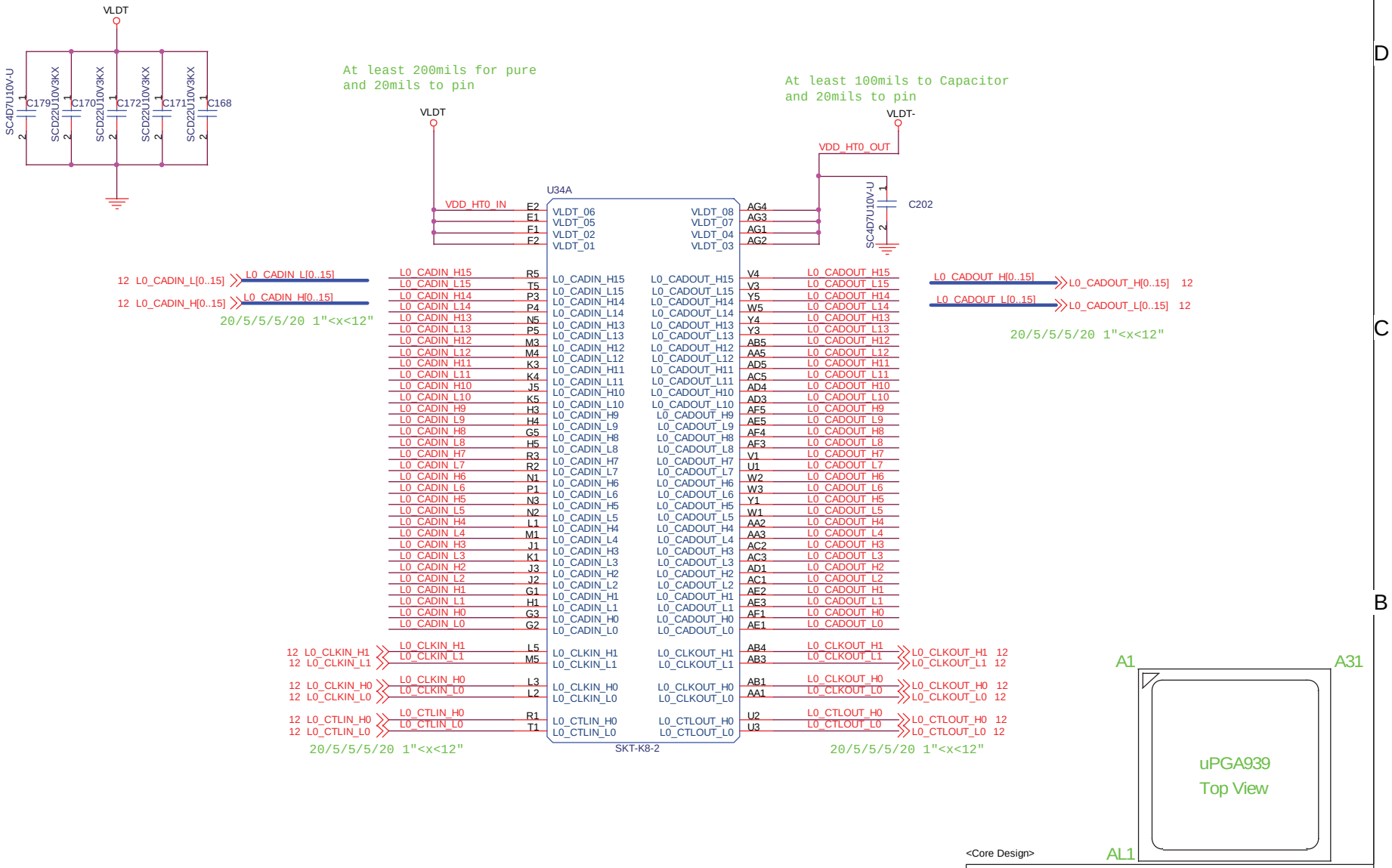
Processor HyperTransport Interface



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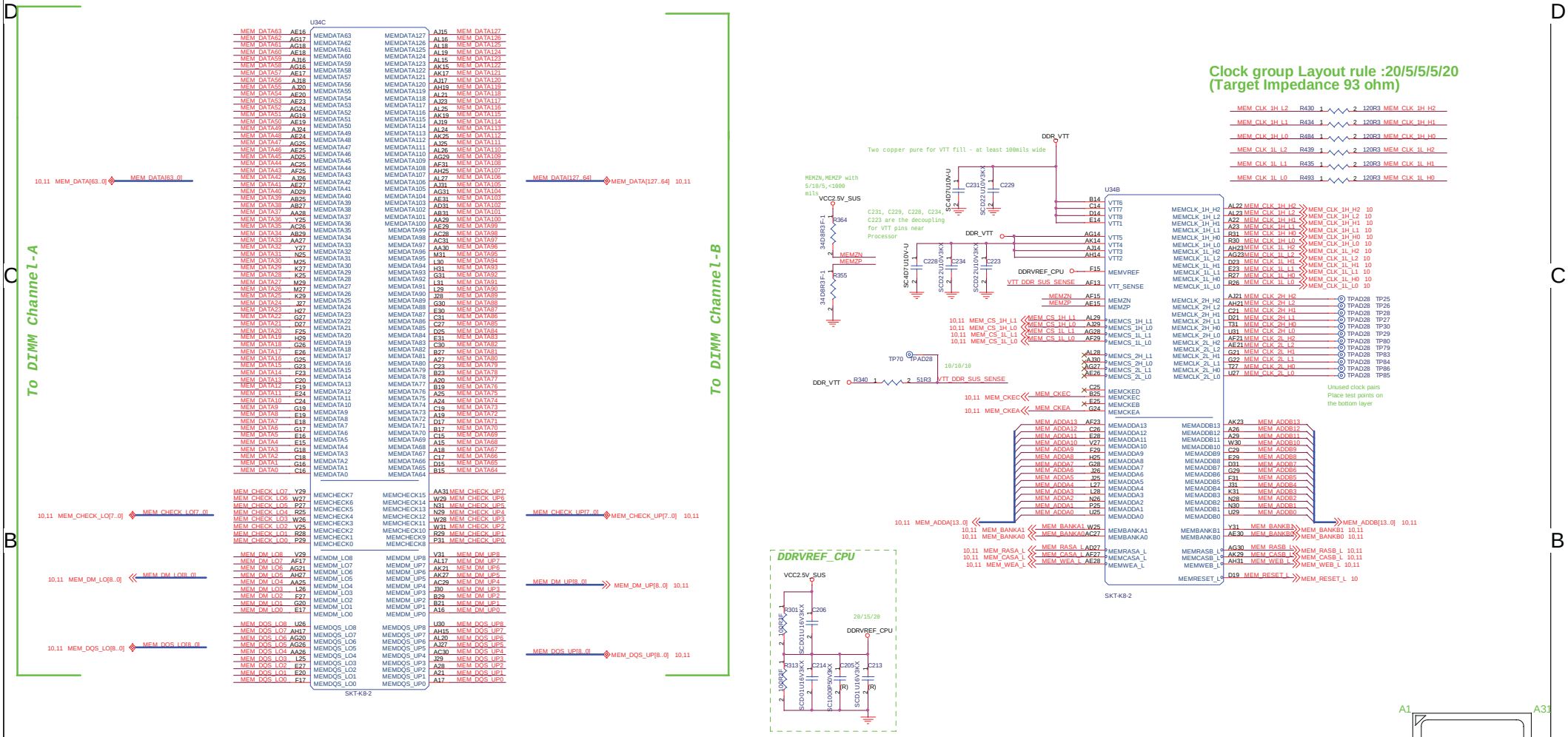
Processor DDR Memory Interface



Data/DM/CHECK group Layout rule : (Target Impedance 45 ohm)

Break in/out : 15/5/15

Motherboard trace routing : 10/10/10

DQS group Layout rule : (Target Impedance 35 ohm)

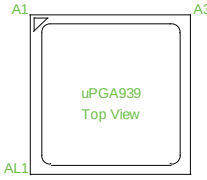
Break in/out : 20/5/20

Motherboard trace routing : 20/15/20

Address/Command group Layout rule : (Target Impedance 45 ohm)

Break in/out : 15/5/15

Motherboard trace routing : 10/10/10



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Processor MISC Signals

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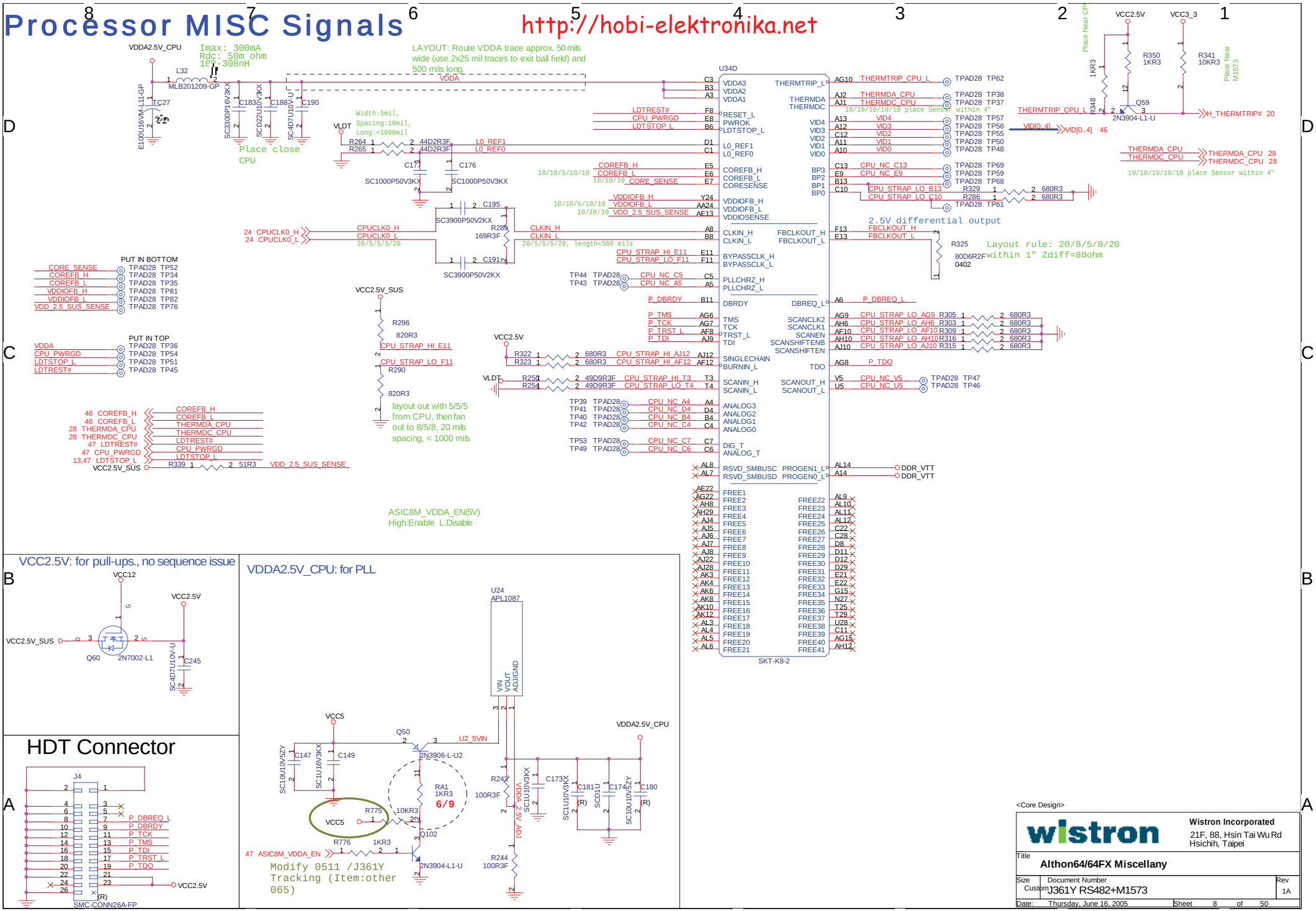

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Processor POWER & Ground

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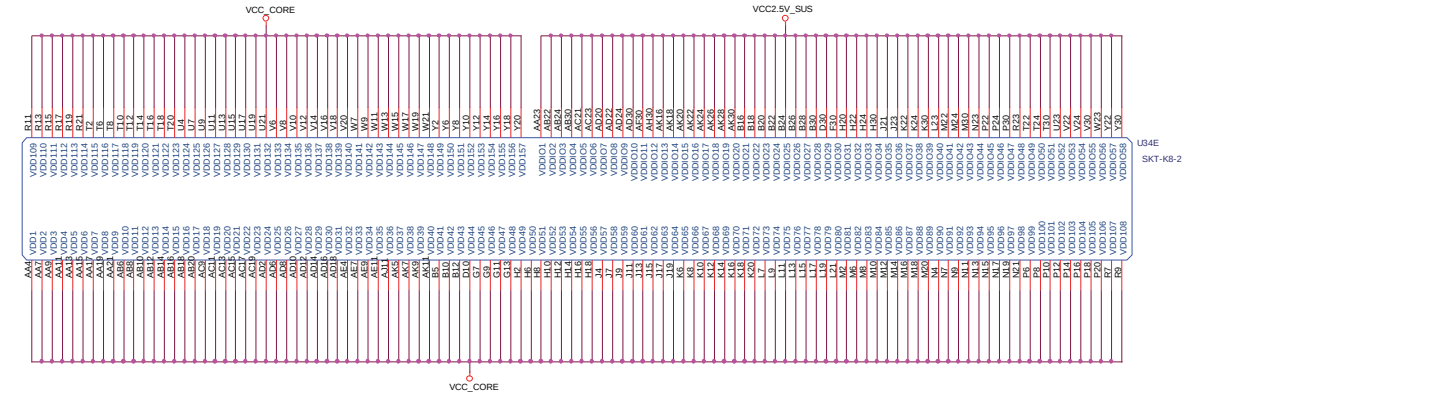
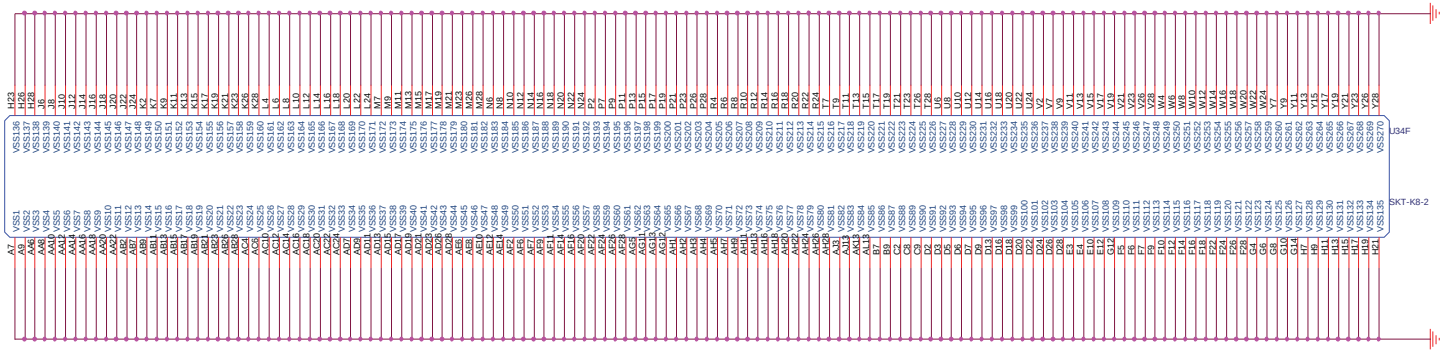
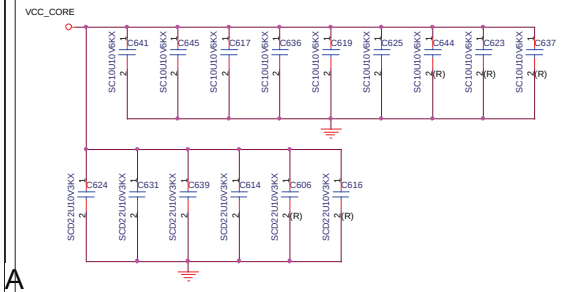


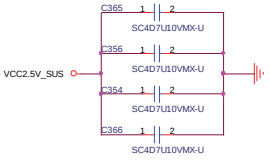


VCC_Core decoupling - Bottom Layer under CPU socket

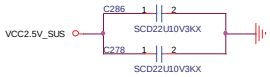


VDDIO Decoupling

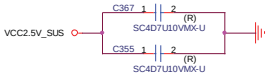
TOP Layer between CPU and DIMMs



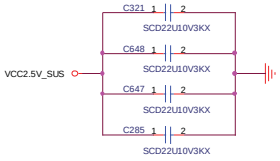
TOP Layer near CPU socket side

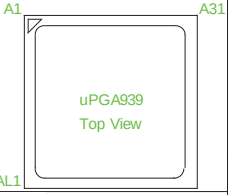


Bottom Layer between CPU and DIMMs



Bottom Layer under CPU socket





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DIMM Slots

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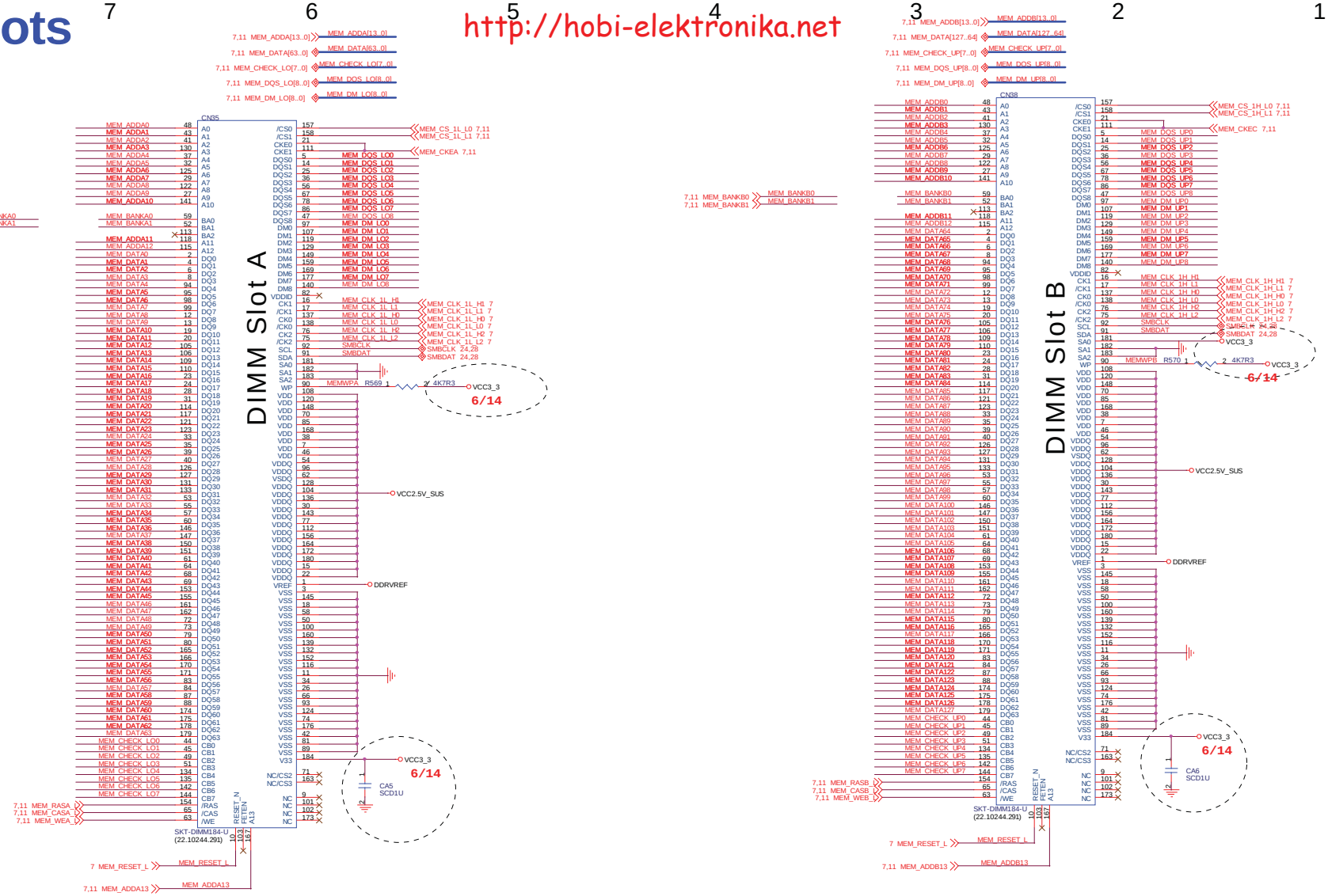


Data/DM/CHECK group Layout rule :

Break in/out : 15/5/15

Motherboard trace routing : 10/10/10

Address/Command group Layout rule :

Break in/out : 15/5/15

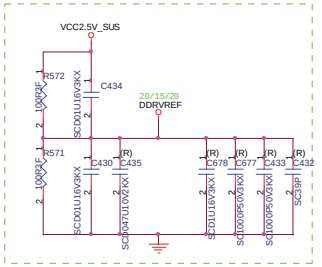
Motherboard trace routing : 10/10/10

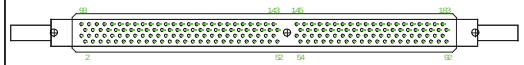
DQS group Layout rule :

Break in/out : 20/5/20

Motherboard trace routing : 20/15/20

Clock group Layout rule :20/5/5/5/20





DDR Socket

Top View

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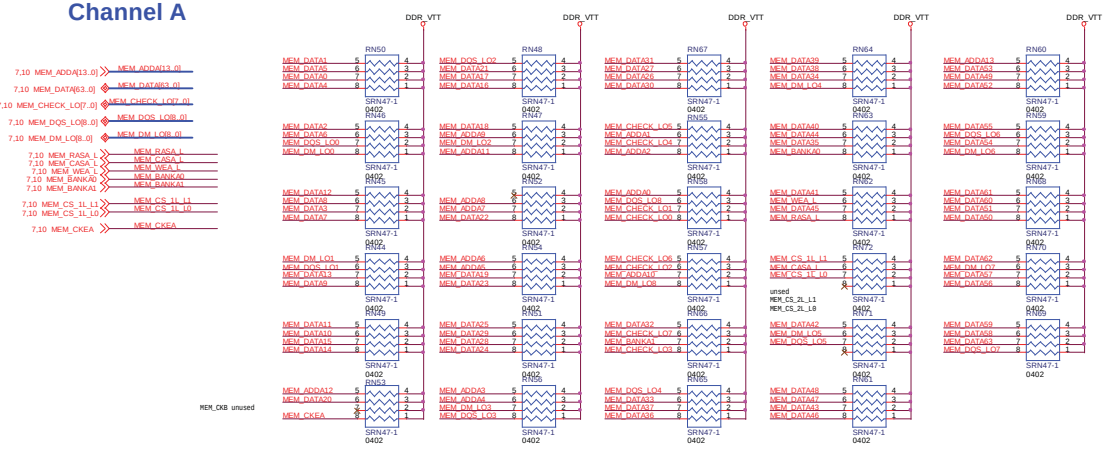
DDR Termination

Data/DM/CHECK group Layout rule :
Break in/out : 15/5/15
Motherboard trace routing : 10/10/10

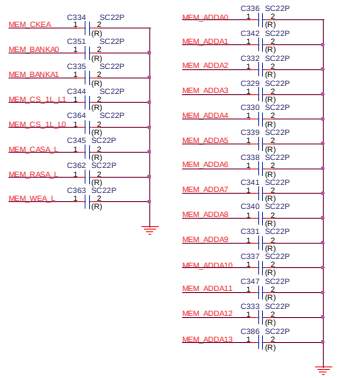
Address/Command group Layout rule :
Break in/out : 15/5/15
Motherboard trace routing : 10/10/10

DQS group Layout rule :
Break in/out : 20/5/20
Motherboard trace routing : 20/15/20

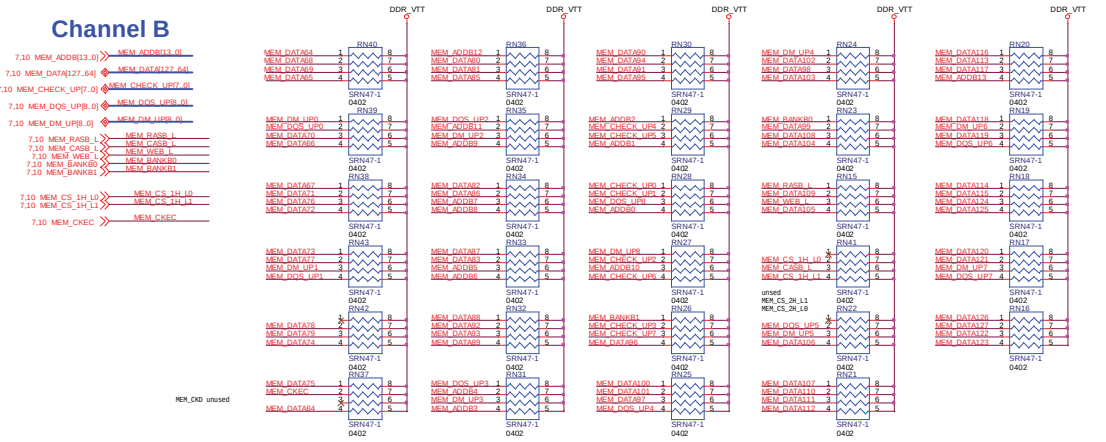
Channel A



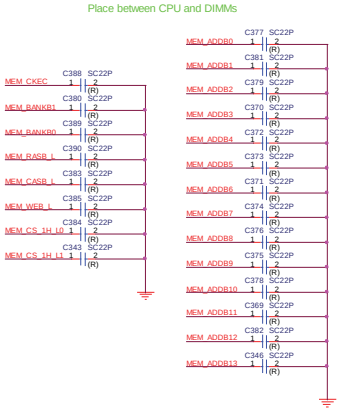
Place between CPU and DIMMs

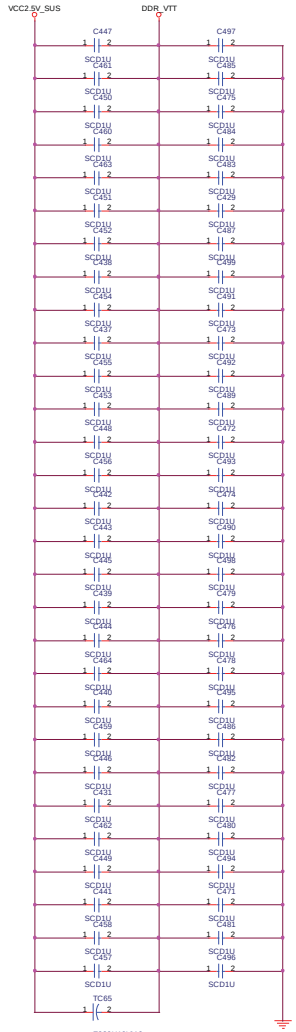


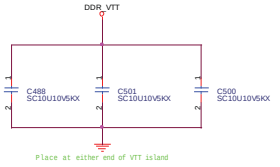
Channel B



Place between CPU and DIMMs







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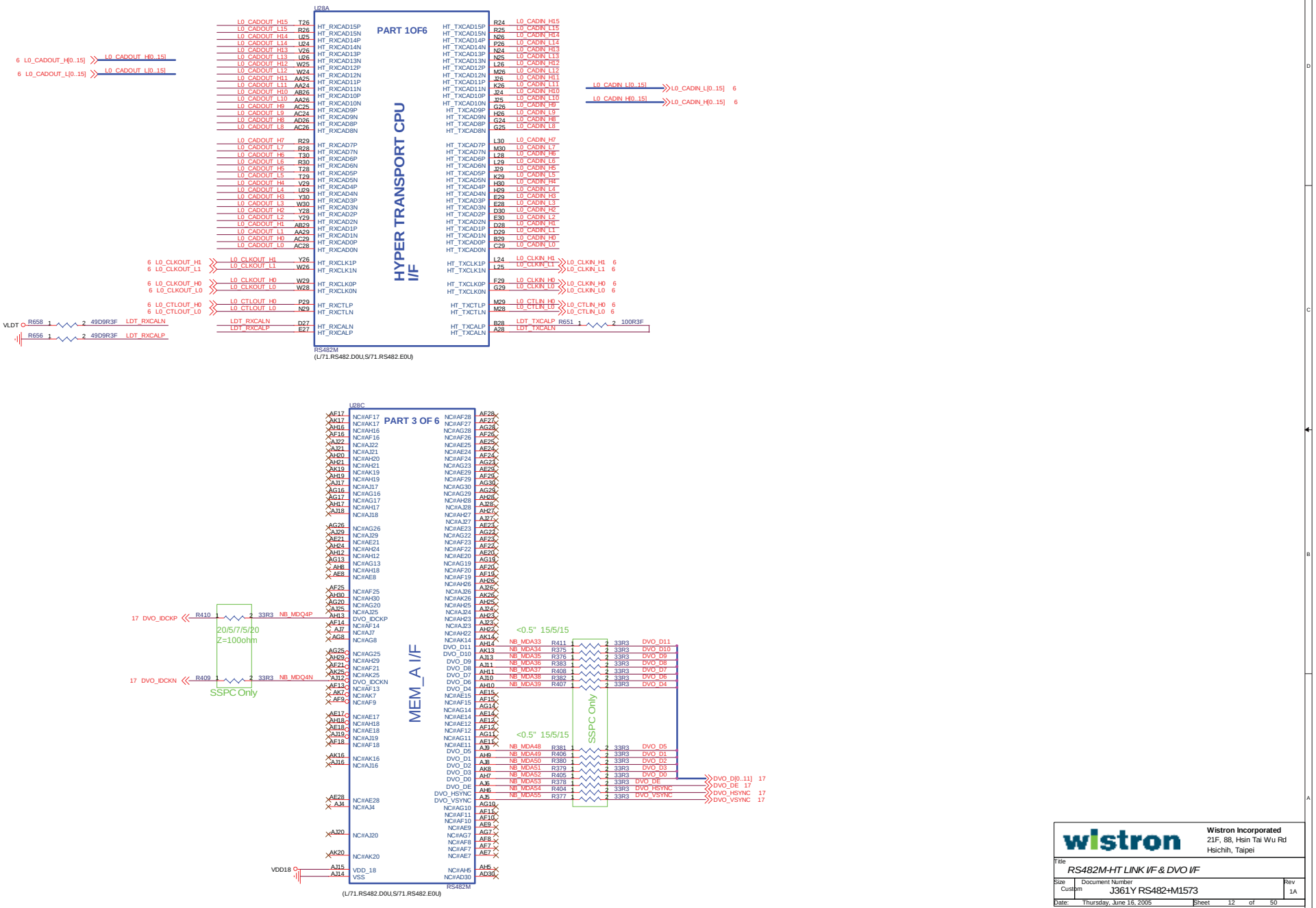
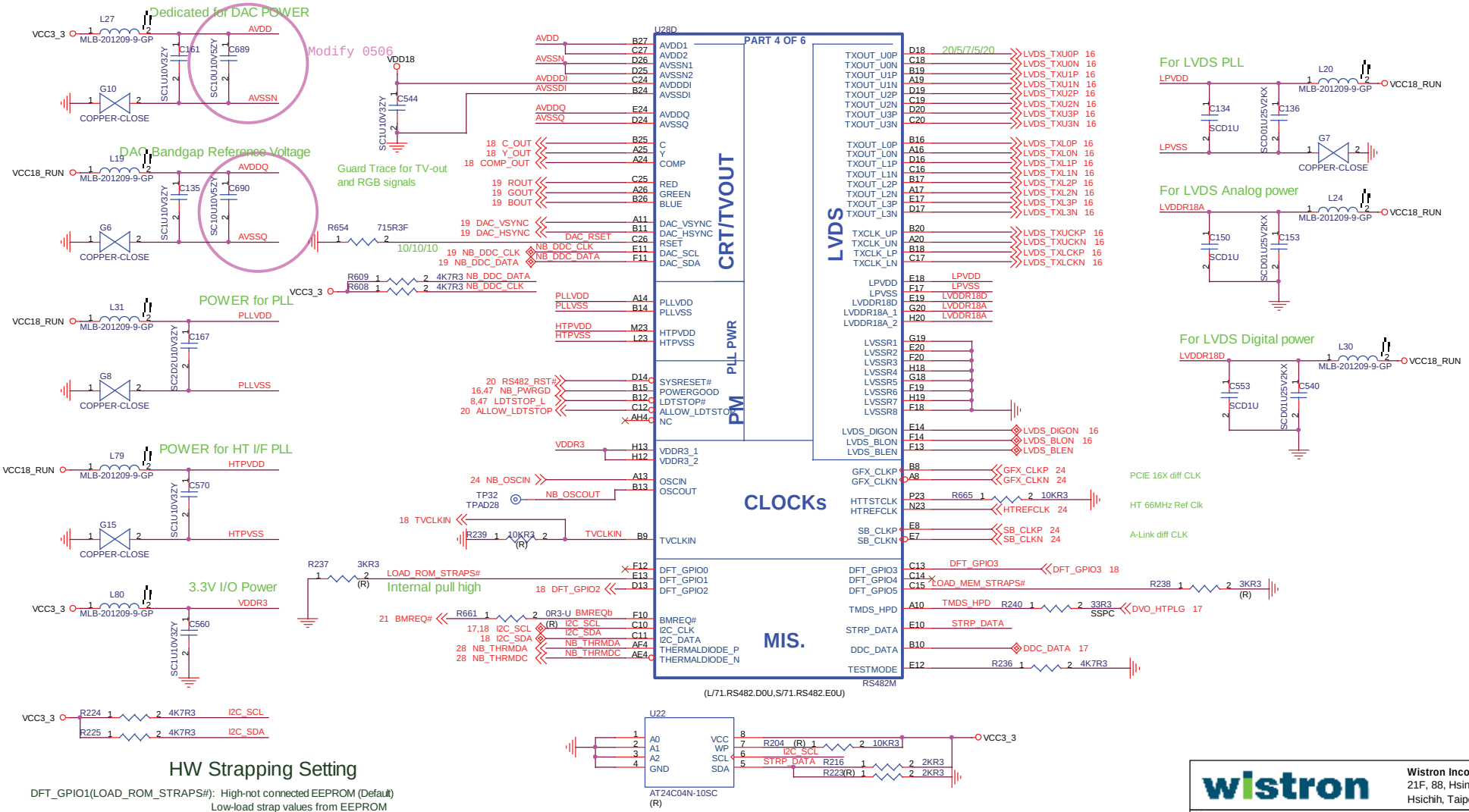
NB/RS482M HT IF & DVO Bus

RS482 ver.A12 PB_P/N 71.RS482.D0U
RS482 ver.A12 LF_P/N 71.RS482.C0U
RS482M ver.A12 PB_P/N 71.RS482.D0U
RS482M ver.A12 LF_P/N 71.RS482.C0U



NB/RS482M DAC/LVDS/CLK/PM



HW Strapping Setting

DFT_GPIO1(LOAD_ROM_STRAPS#): High-not connected EEPROM (Default)
Low-load strap values from EEPROM

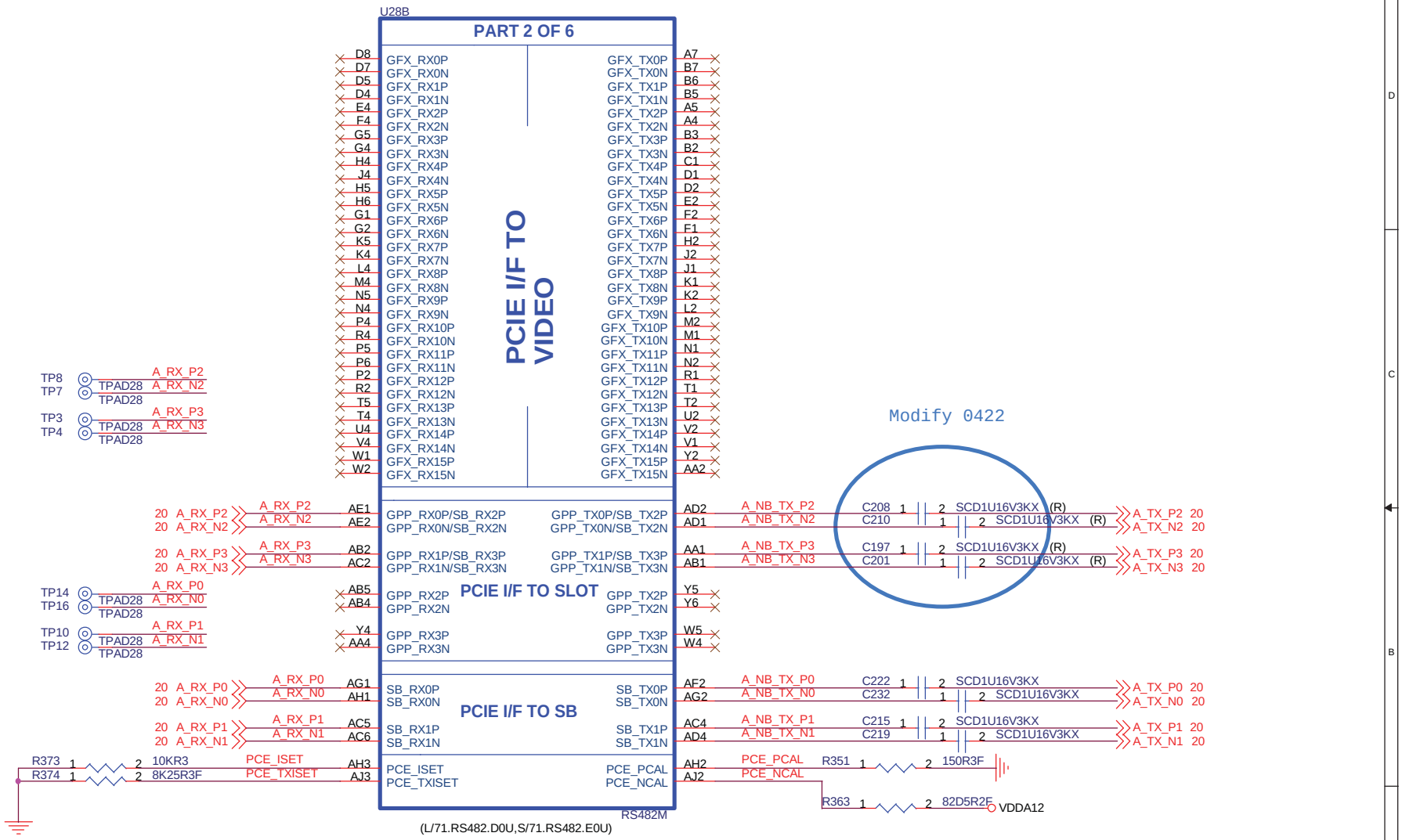
DFT_GPIO2(HT_Width_Override): High-8 bit link (default)
Low-for testing only

DFT_GPIO[4..3](Overrides HT Freq): 11-200MHz(Default)

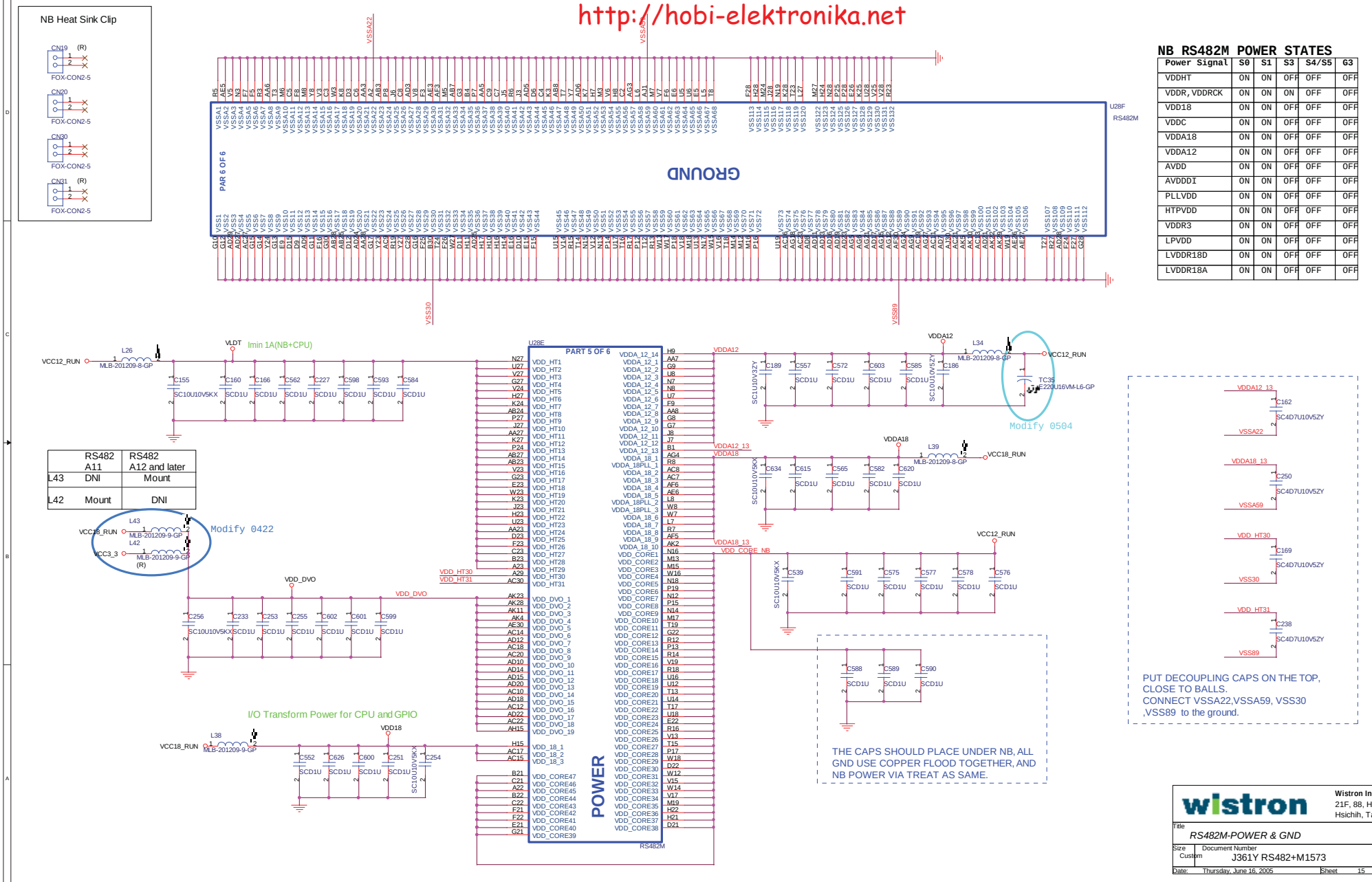
DFT_GPIO5(LOAD_MEM_STRAPS#): 0-capture DVO pins for debug bus straps.
1-Use Default Values

NOTE: Provide access to STRAP_DATA and I2C_SCL pins is MANDATORY.

Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	*RS482M-DAC/LVDS/MIS/CLK/PM*
Size: Custom	Document Number: J361Y RS482+M1573 Rev: 1A
Date: Thursday, June 16, 2005	Sheet 13 of 50



wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	*RS482M-DAC/LVDS/MIS/CLK/PM*	
Size: Custom	Document Number: J361Y RS482+M1573	Rev: 1A
Date: Thursday, June 16, 2005	Sheet 14 of 50	



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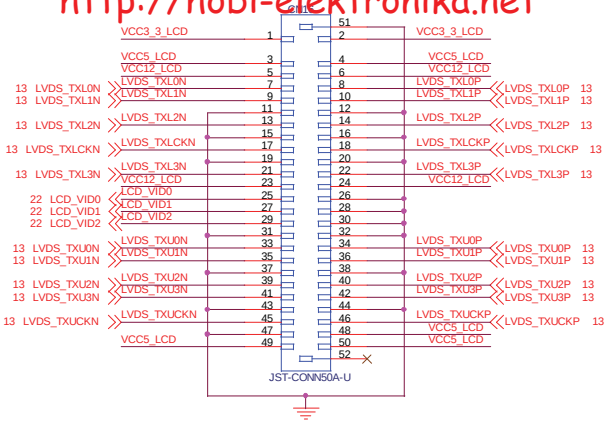
Hsichih, Taipei

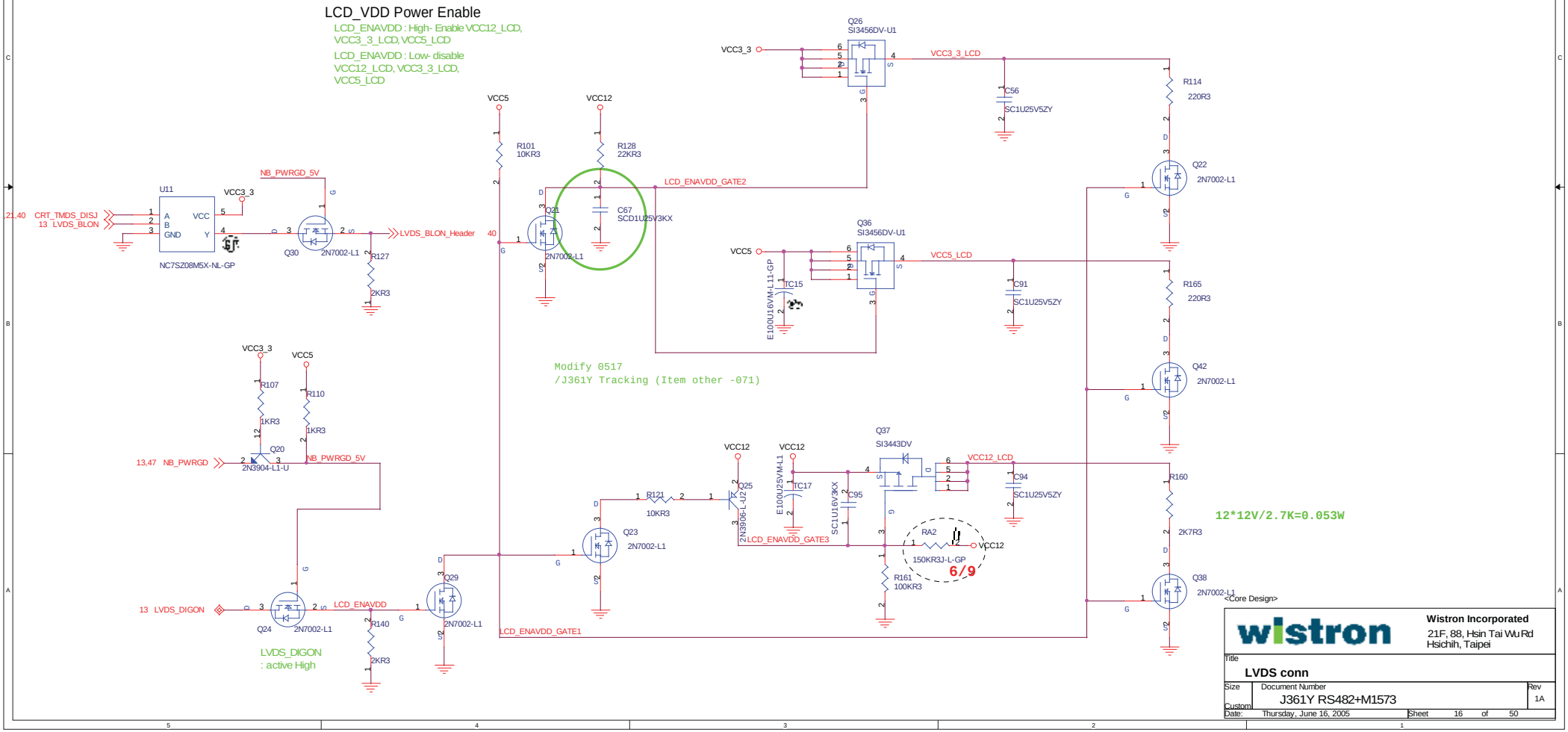
Title: *RS482M-POWER & GND*

Size: Custom | Document Number: J361Y RS482+M1573 | Rev: 1A

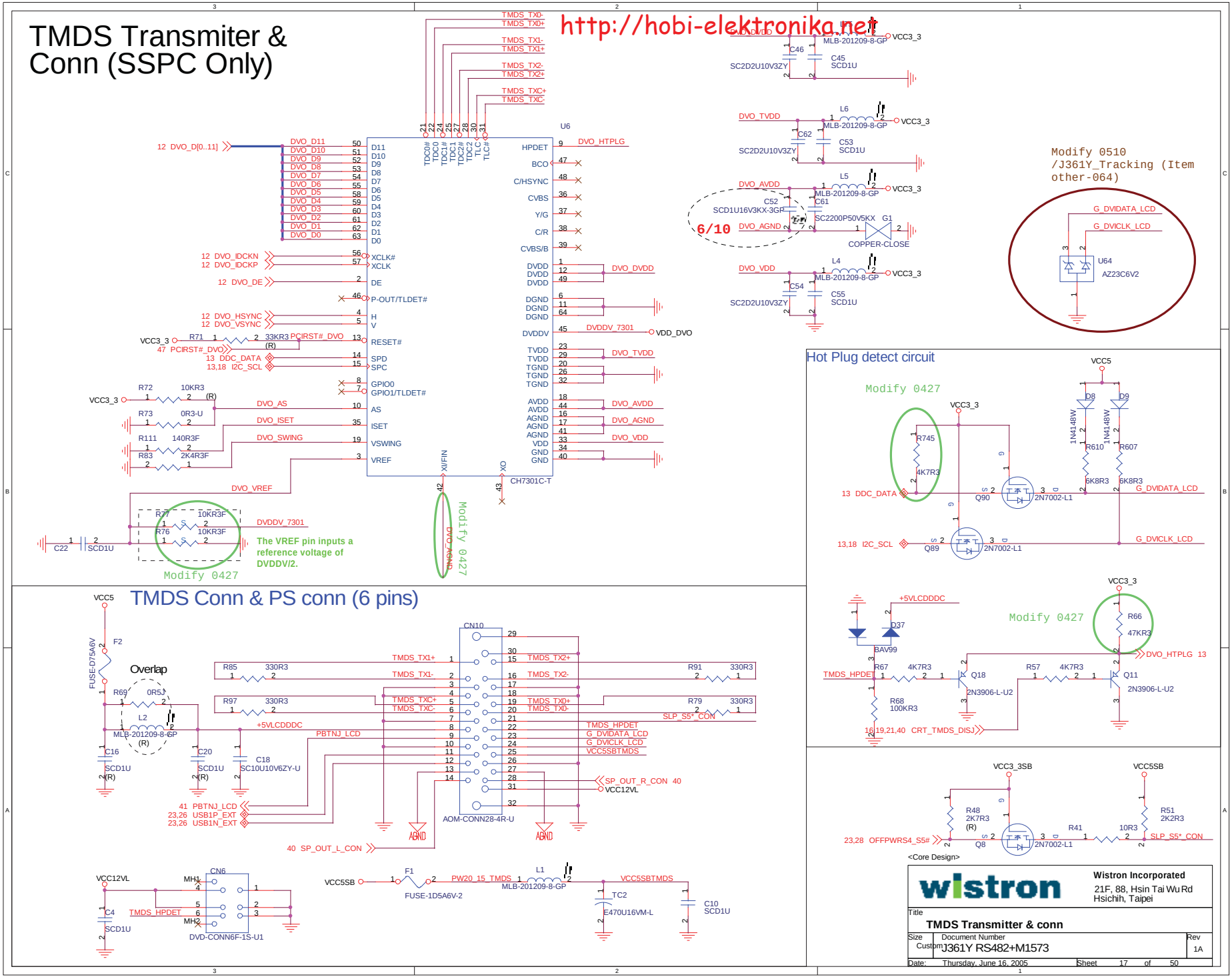
Date: Thursday, June 16, 2005 | Sheet 15 of 50

LVDS header (LCDPC Only)





TMDS Transmiter & Conn (SSPC Only)



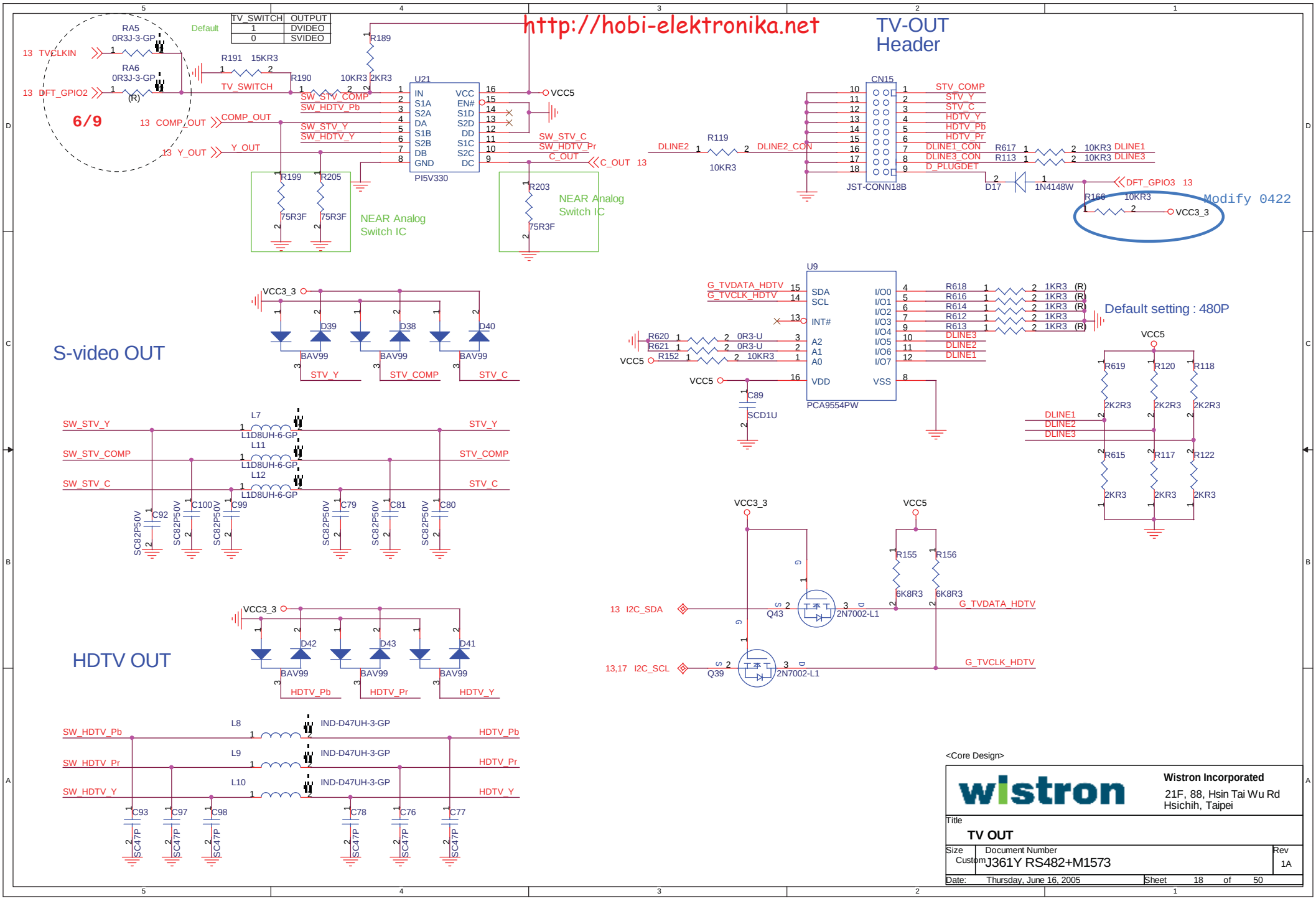
Modify 0510 /J361Y_Tracking (Item other-064)

Hot Plug detect circuit

TMDS Conn & PS conn (6 pins)

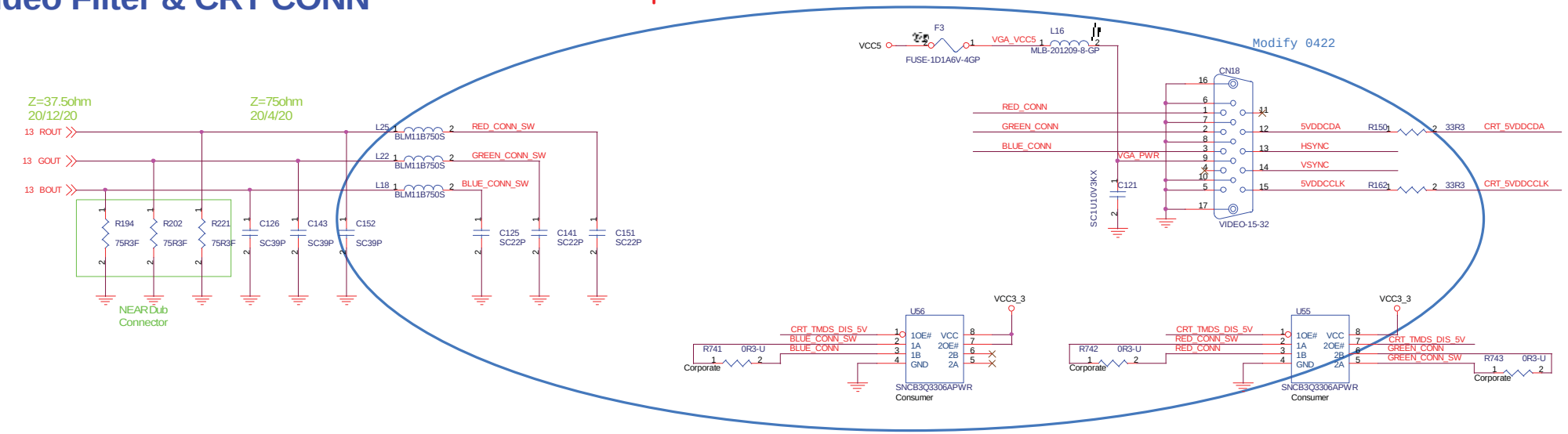
<Core Design>

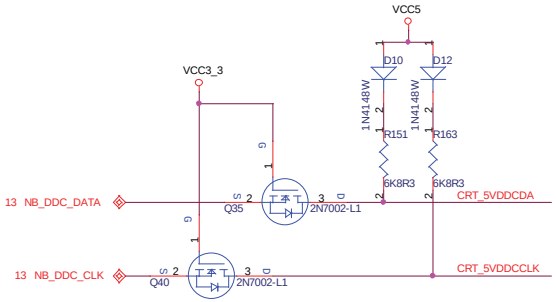
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: TMDS Transmitter & conn		
Size: Custom	Document Number: J361Y RS482+M1573	Rev: 1A
Date: Thursday, June 16, 2005	Sheet 17 of 50	

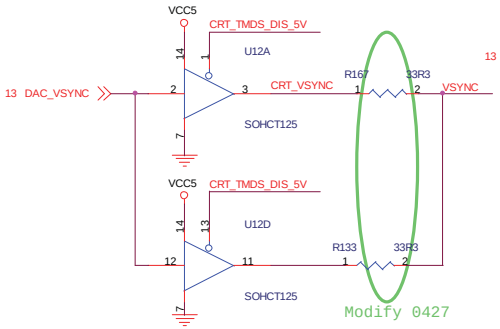


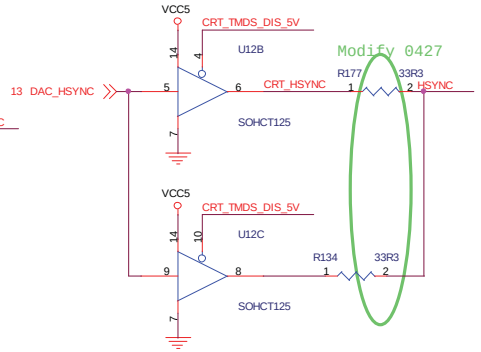
Video Filter & CRT CONN

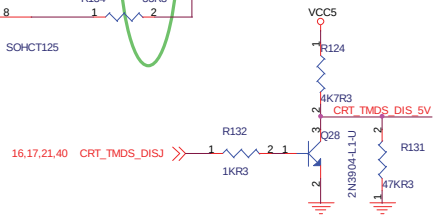
http://hobi-elektronika.net



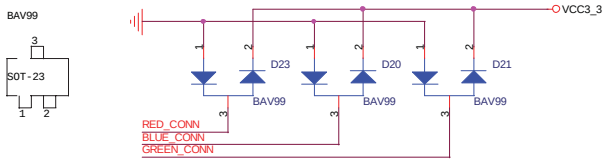


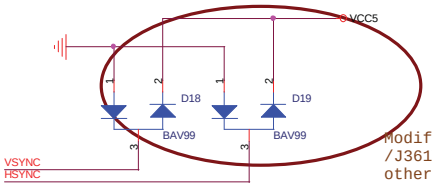


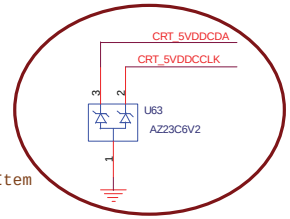




ESD PROTECTION







<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA CONN

Size: Custom | Document Number: J361Y RS482+M1573 | Rev: 1A

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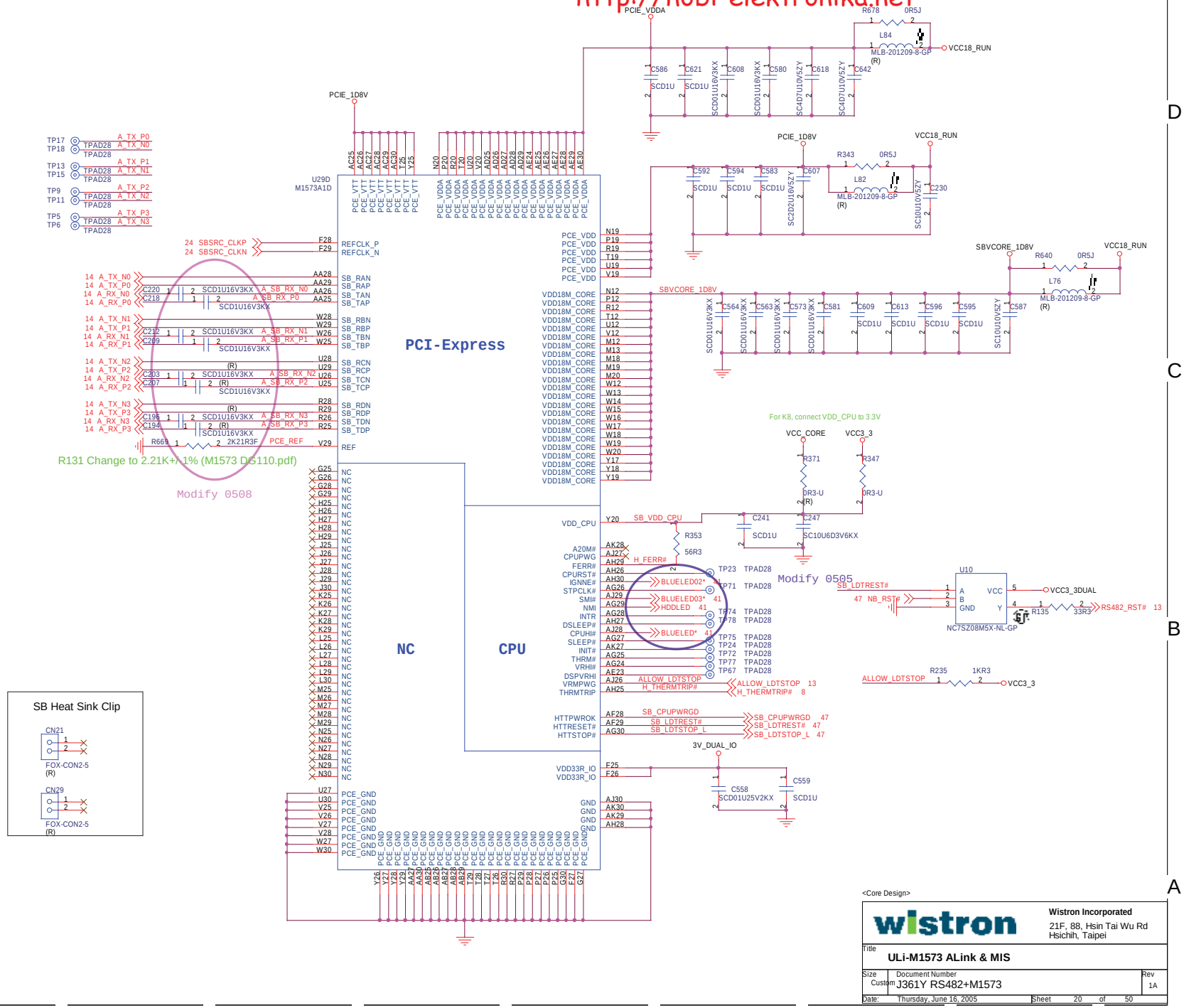

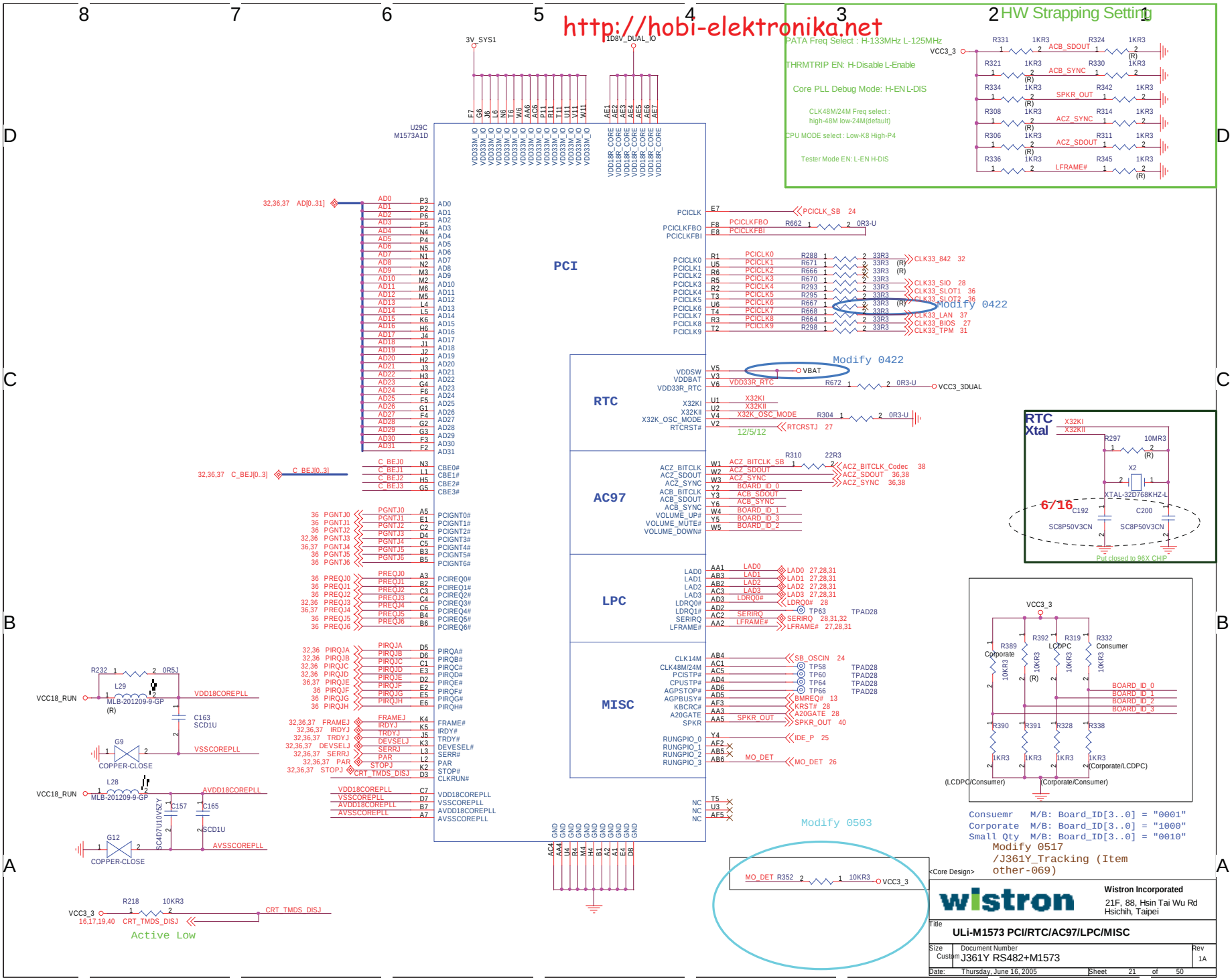

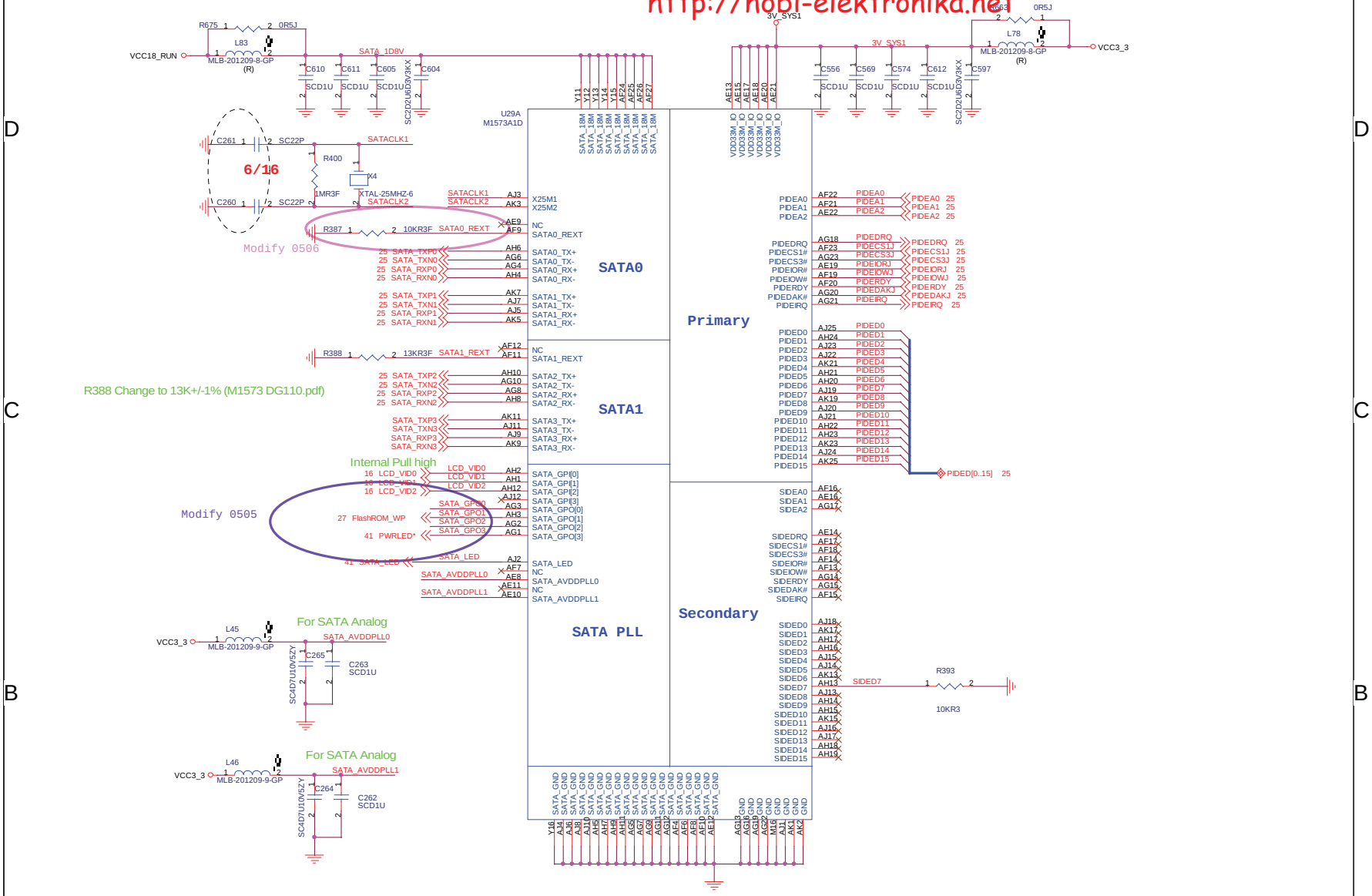

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: ULi-M1573 SATA & IDE I/F

Size: Custom | Document Number: J361Y RS482+M1573 | Rev: 1A

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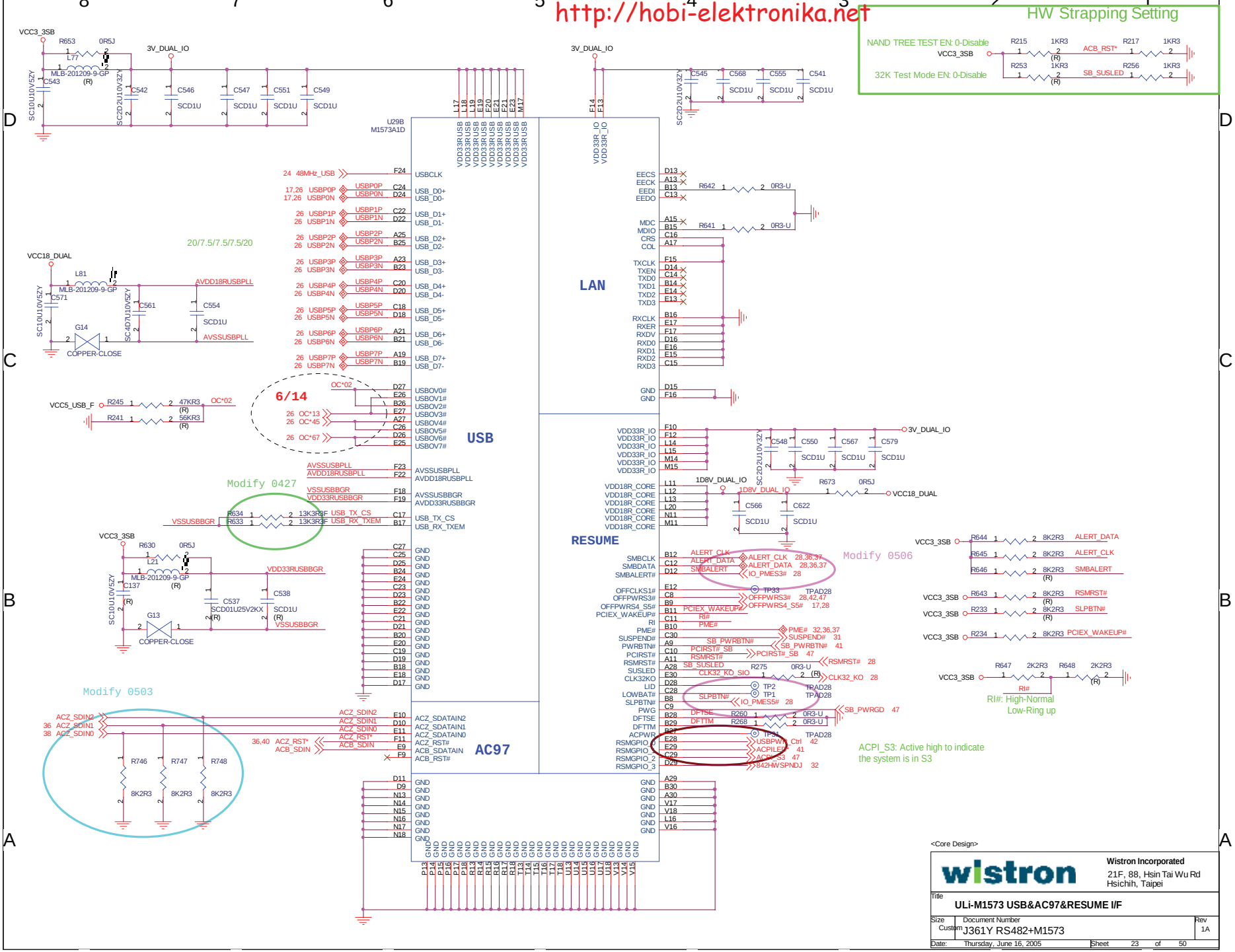

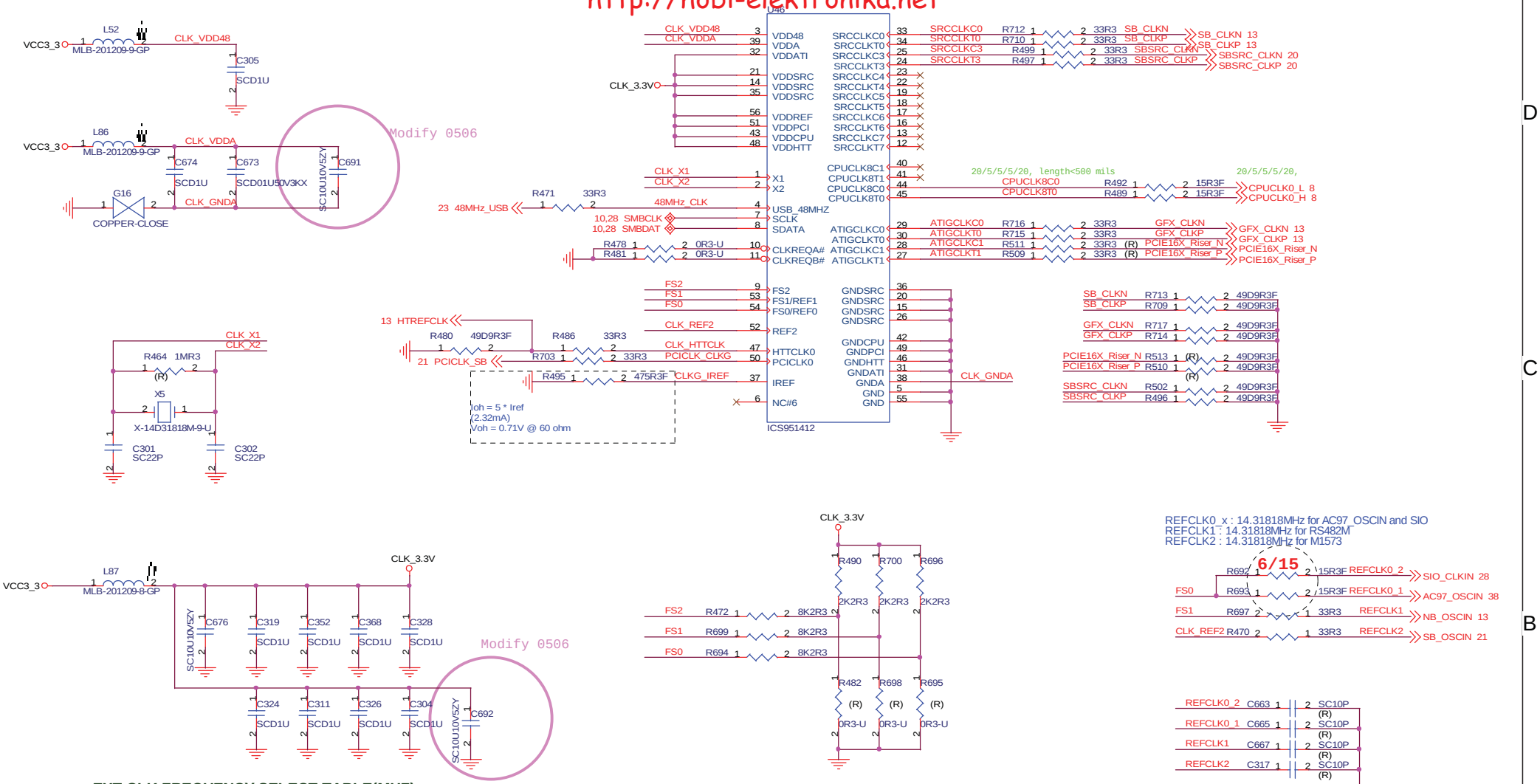

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
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Title: CLOCK GENERATOR

Size: Custom | Document Number: J361Y RS482+M1573 | Rev: 1A

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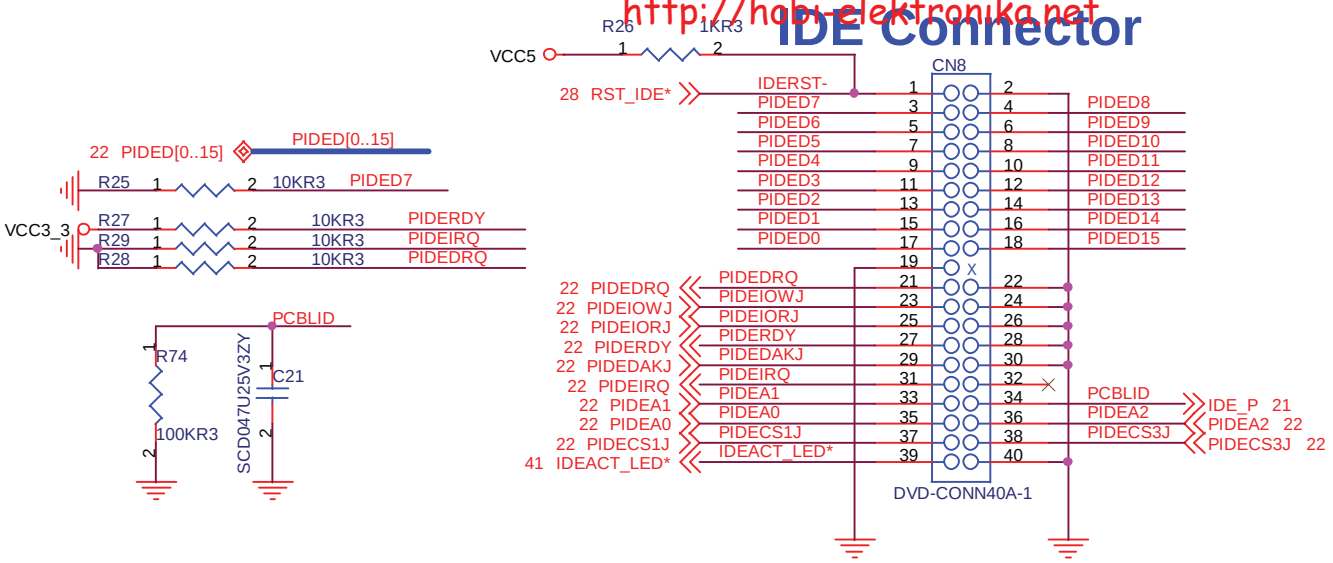
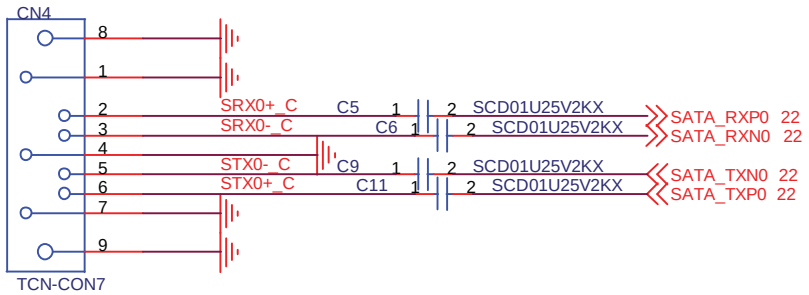
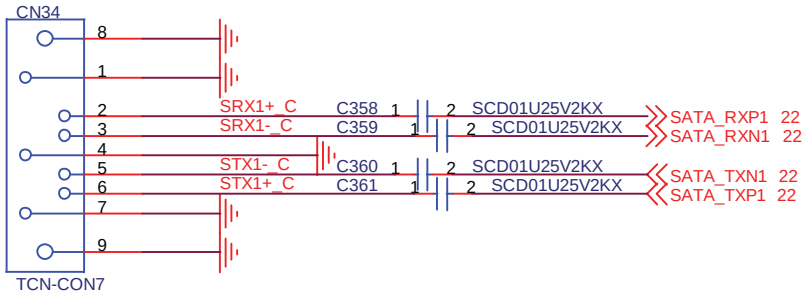
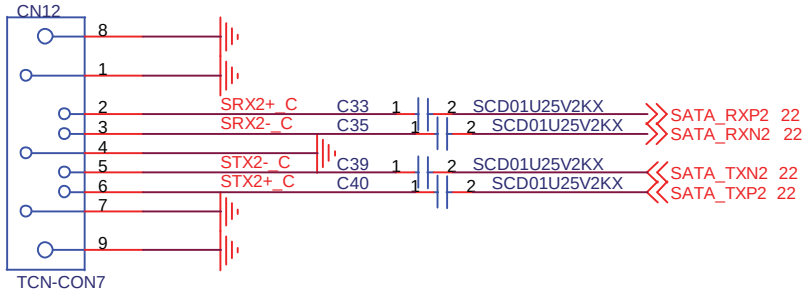
IDE Connector



SATA Connector







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Hsichih, Taipei

Title: IDE and SATA CONN

Size	Document Number	Rev
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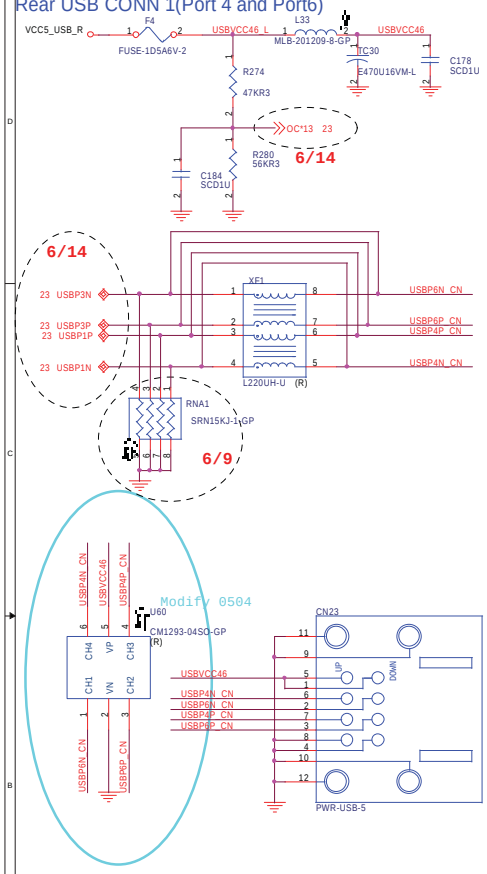
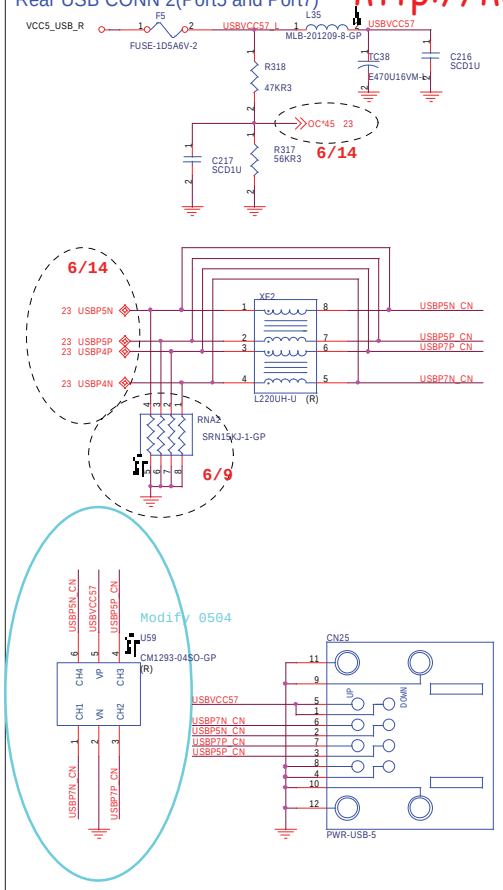
USB CONN

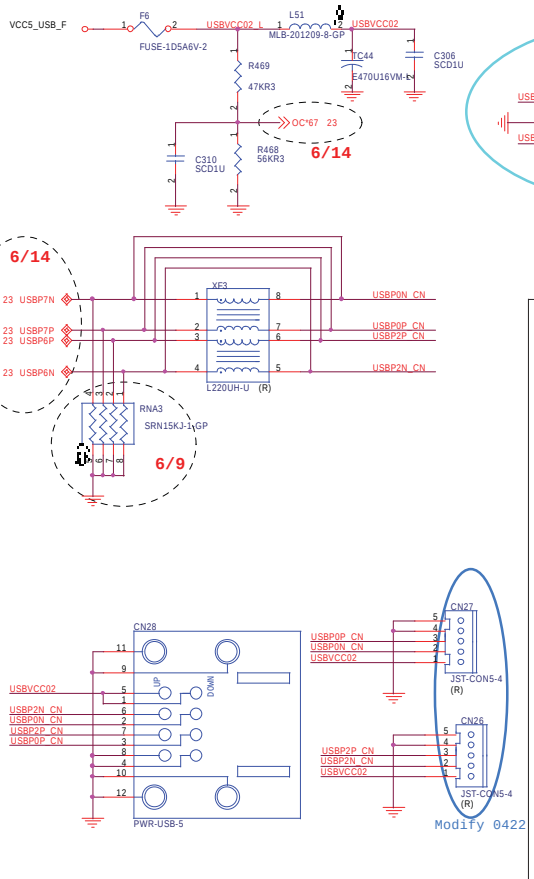
Rear USB CONN 1(Port 4 and Port6)



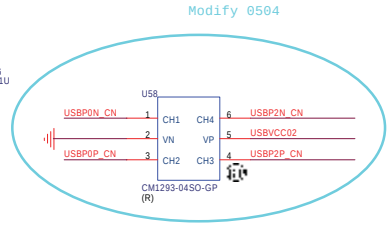
Rear USB CONN 2(Port5 and Port7)



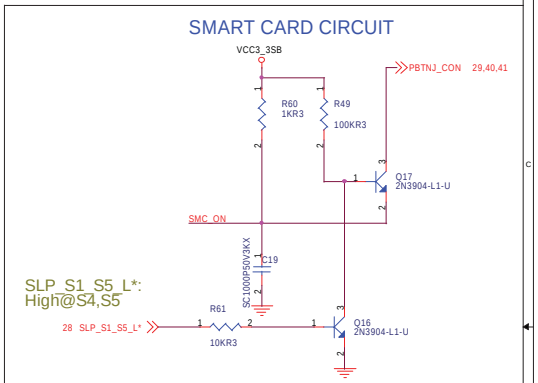
Front USB CONN(Port 1and Port2)



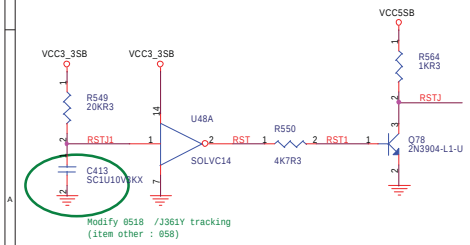
Modify 0504



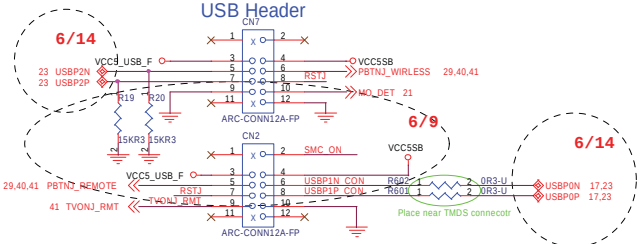
SMART CARD CIRCUIT



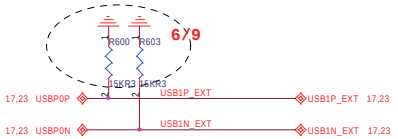
USB Layout Rule : 20/7.5/7.5/7.5/20



USB Header



TMDS USB PORT for TMDS only



<Core Design>

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Title: USB CNT

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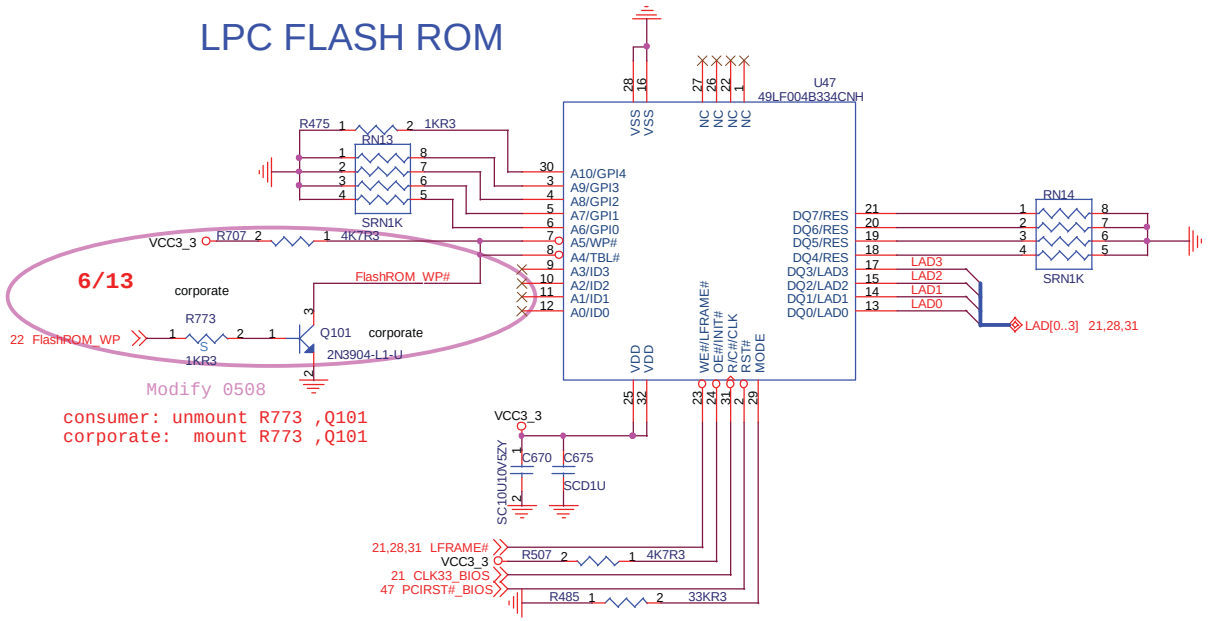
LPC FLASH ROM



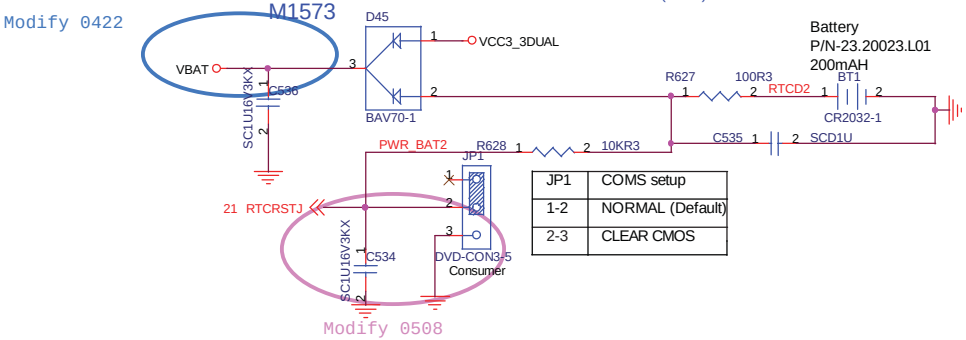
BIOS SCOKET P/N : 62.10061.001

RTC Battery

Modify 0422

Close to ULi M1573

I(R627) must be less than 4.566uA



JP1	COMS setup
1-2	NORMAL (Default)
2-3	CLEAR CMOS

<Core Design>

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Hsichih, Taipei

Title: **BIOS/Battery RTC**

Size	Document Number	Rev
Custom	J361Y RS482+M1573	1A

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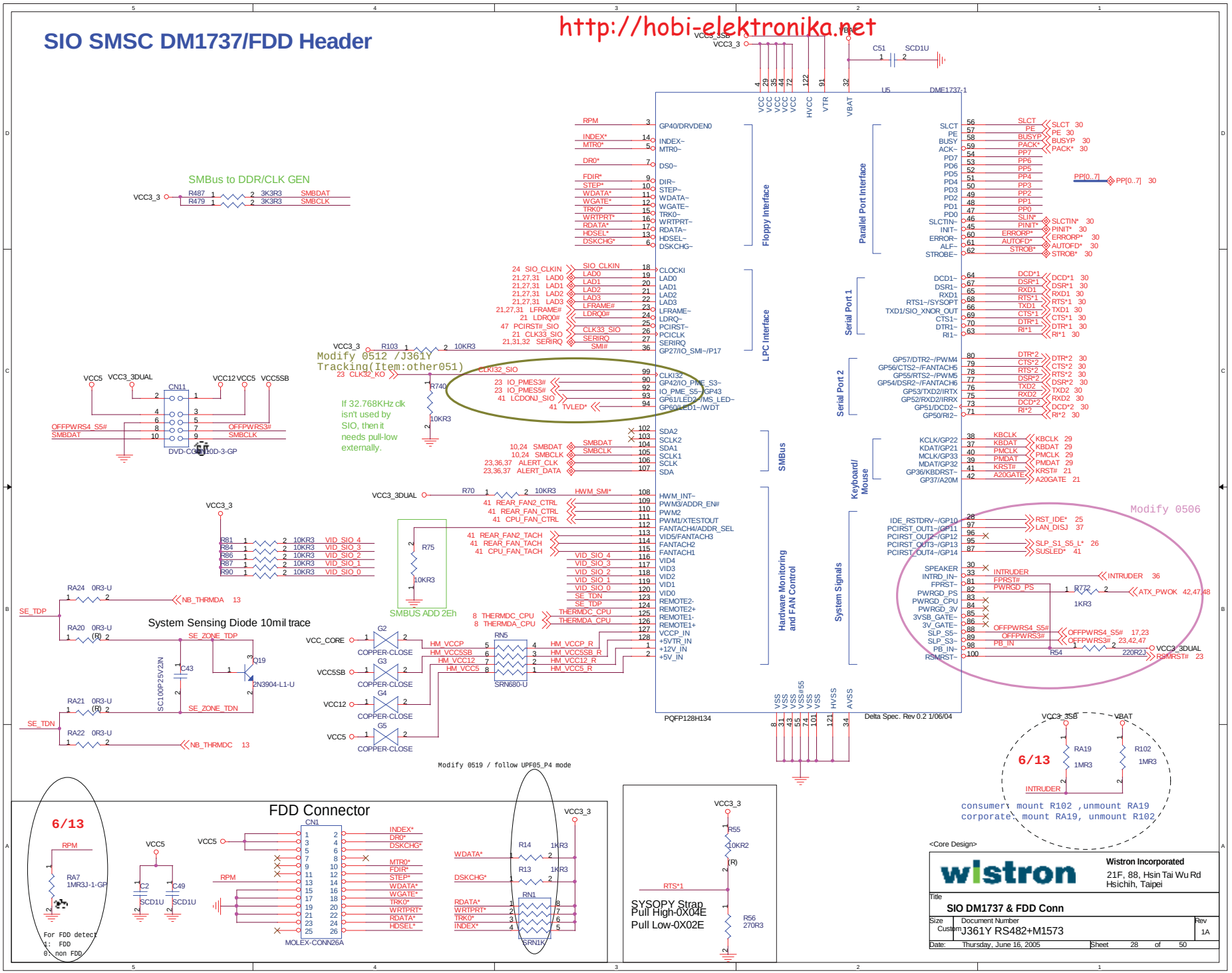
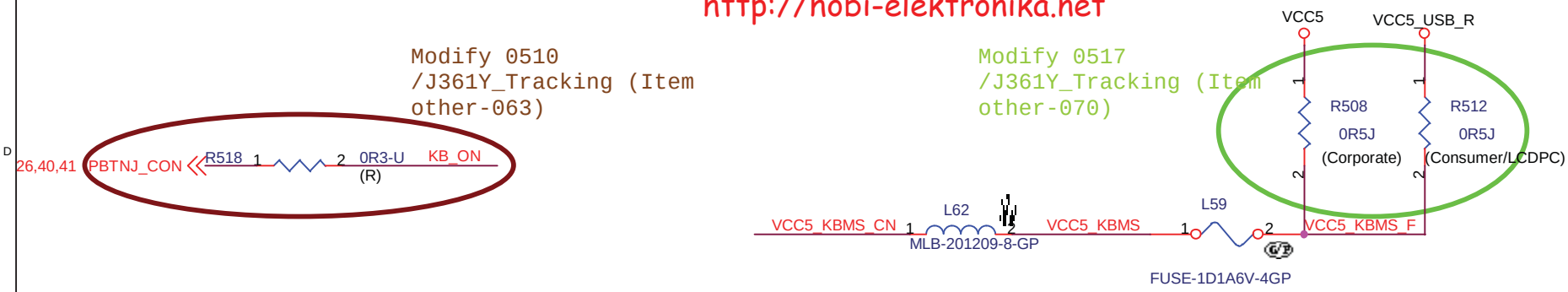
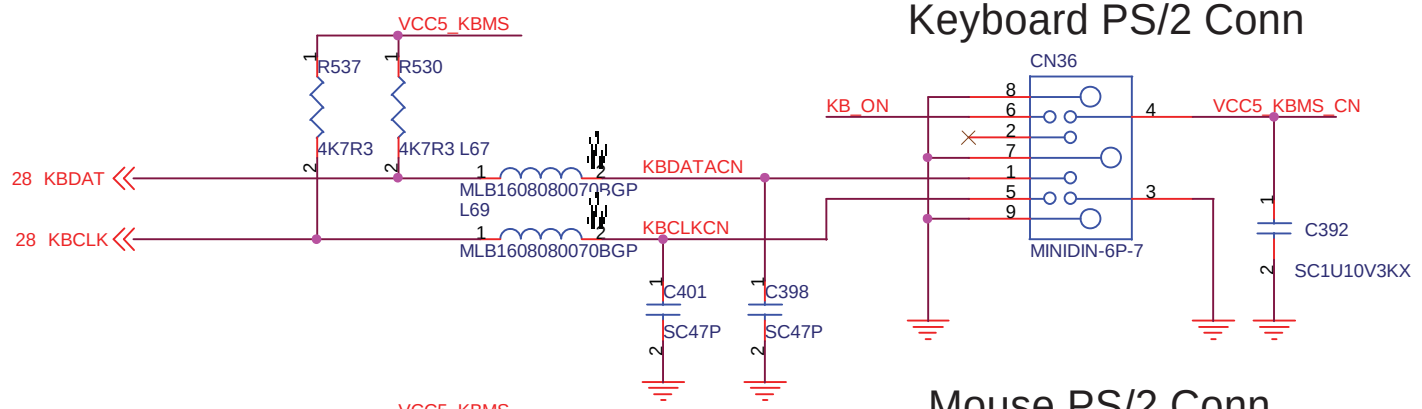


Modify 0510
/J361Y_Tracking (Item
other-063)

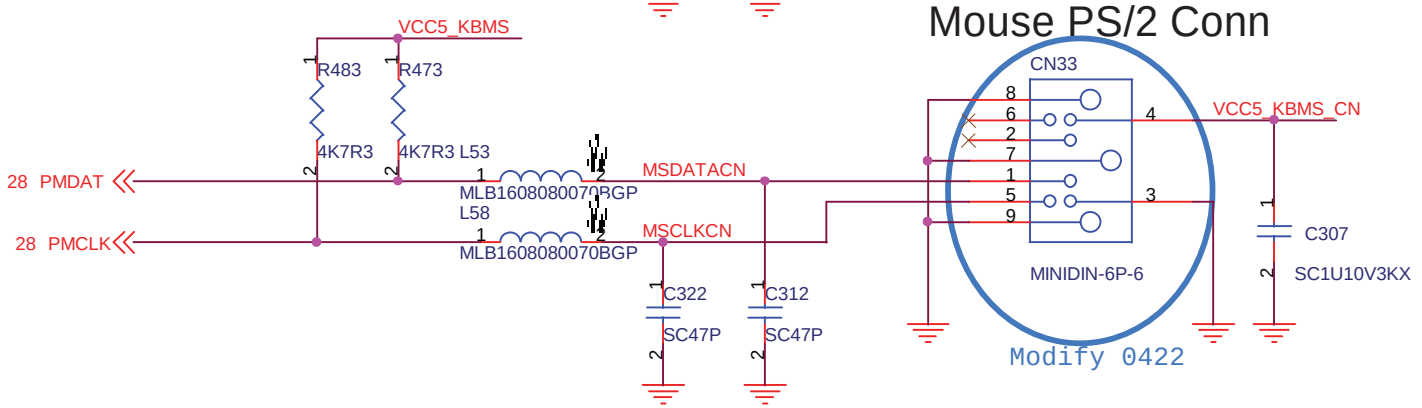
Modify 0517
/J361Y_Tracking (Item
other-070)



Keyboard PS/2 Conn



Mouse PS/2 Conn



Modify 0422

<Core Design>

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Hsichih, Taipei

Title: **KB/MS PS2 Conn**

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A	J361Y RS482+M1573	1A

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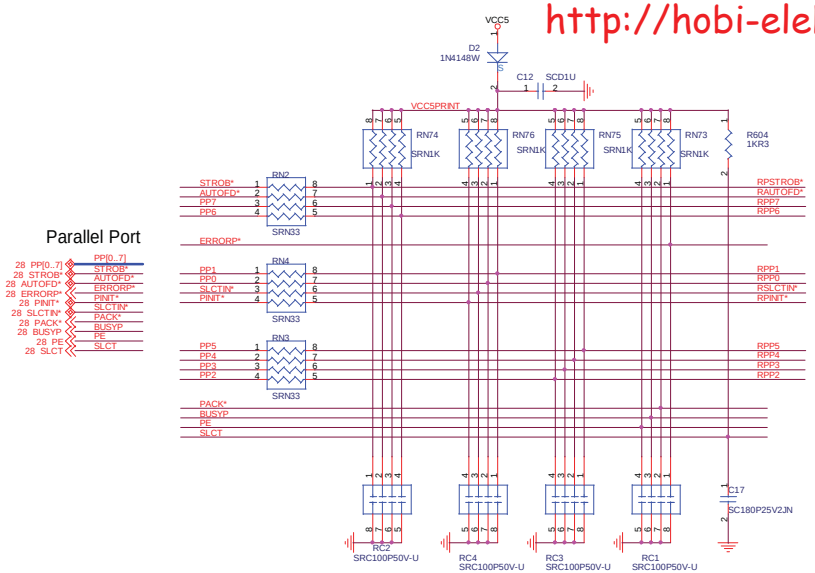

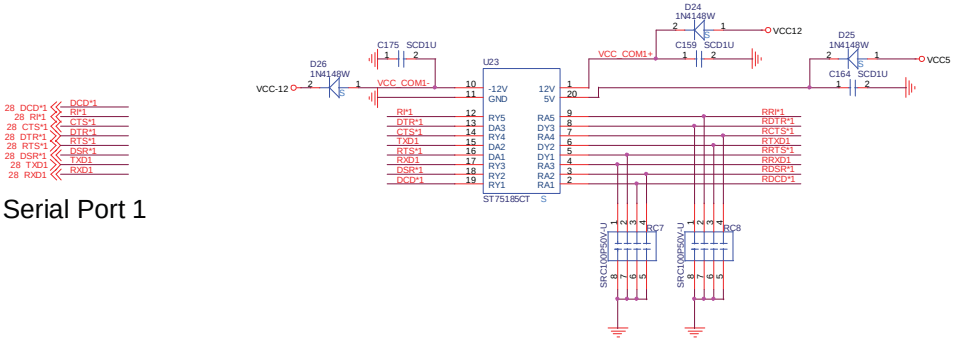

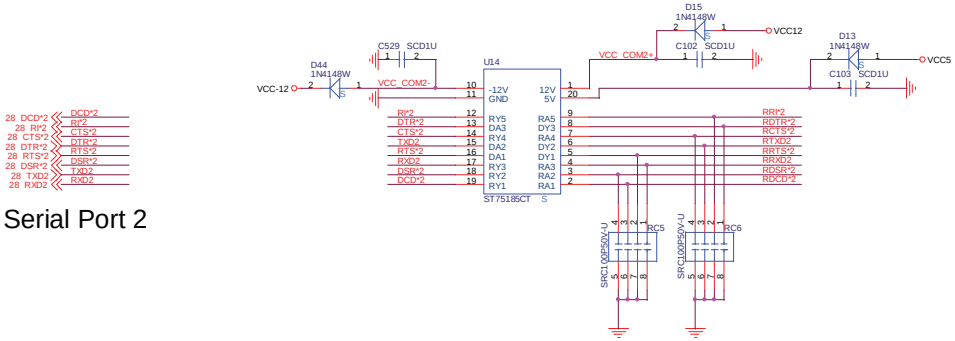

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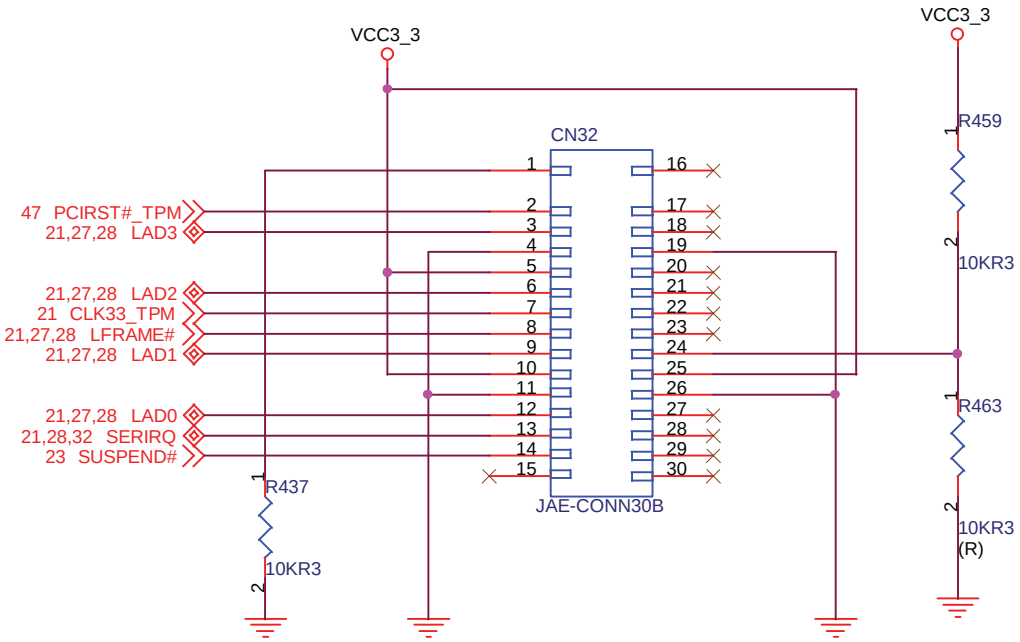
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: COM/PRINTER PORT

Size: C | Document Number: J361Y RS482+M1573 | Rev: 1A

Date: Thursday, June 16, 2005 | Sheet 30 of 50



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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
TPM Header

Size	Document Number	Rev
A	J361Y RS482+M1573	1A

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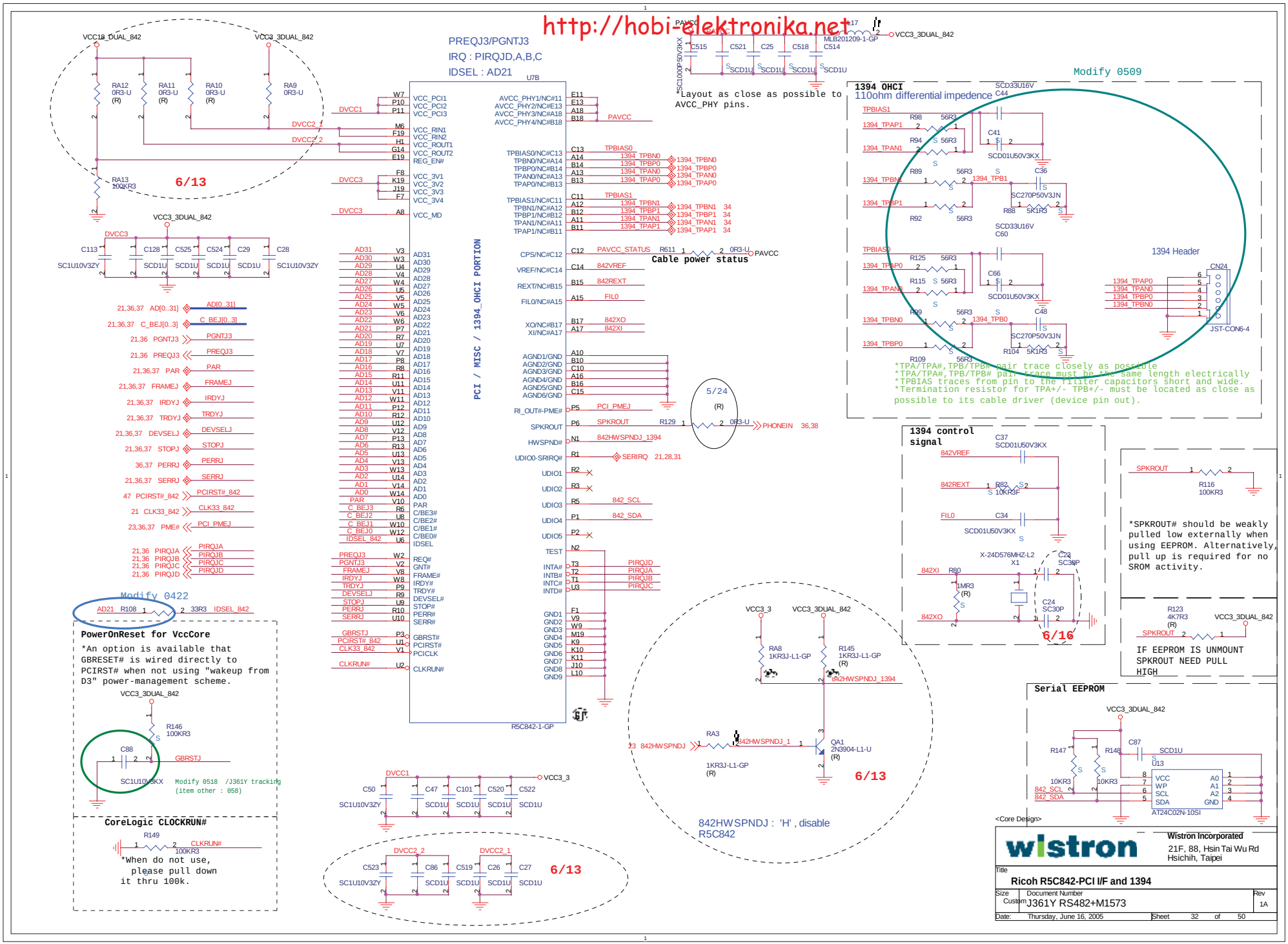

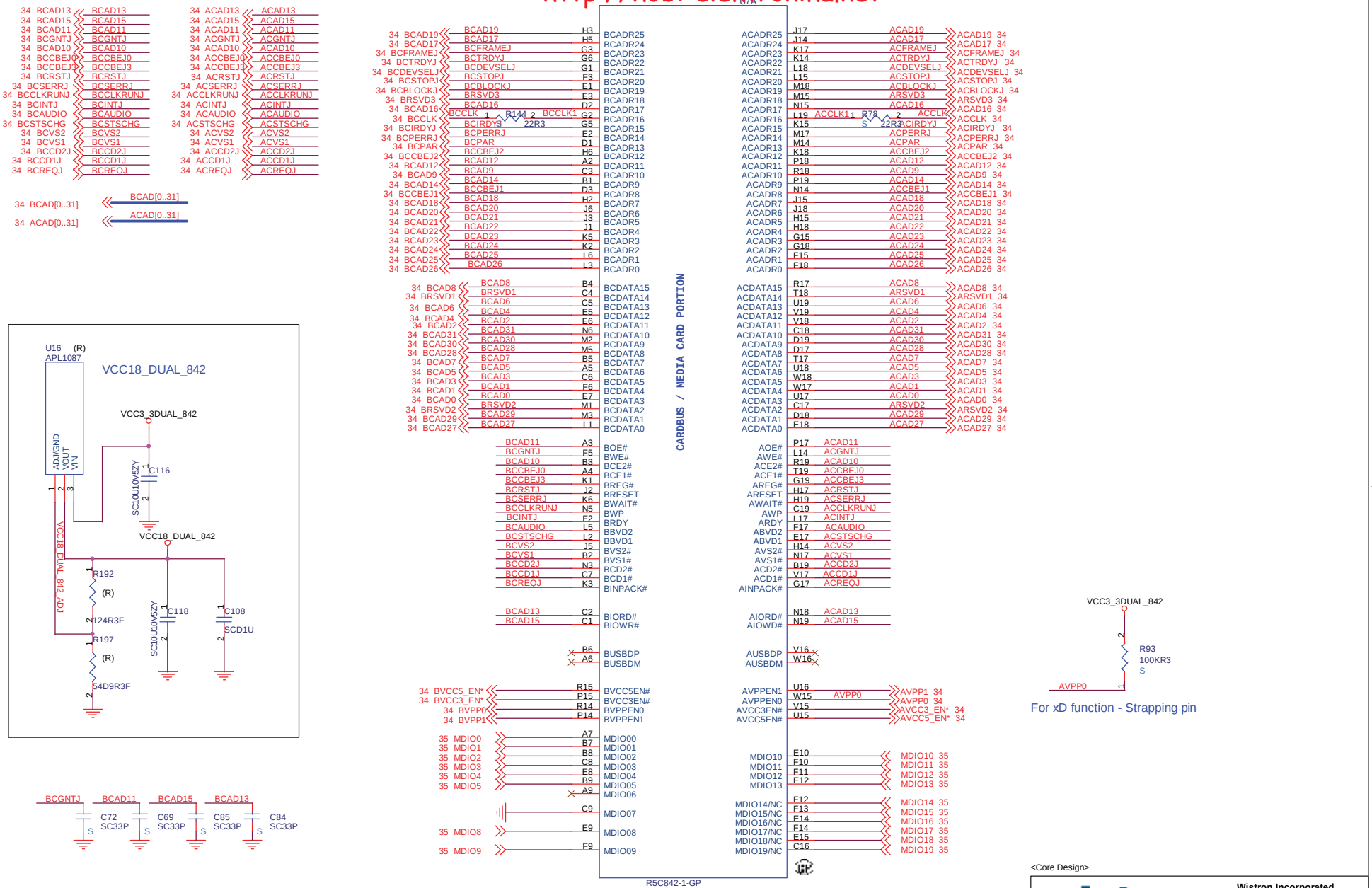

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Ricoh R5C842-MDIO I/F and CB I/F

Size	Document Number	Rev
Custom	J361Y RS482+M1573	1A

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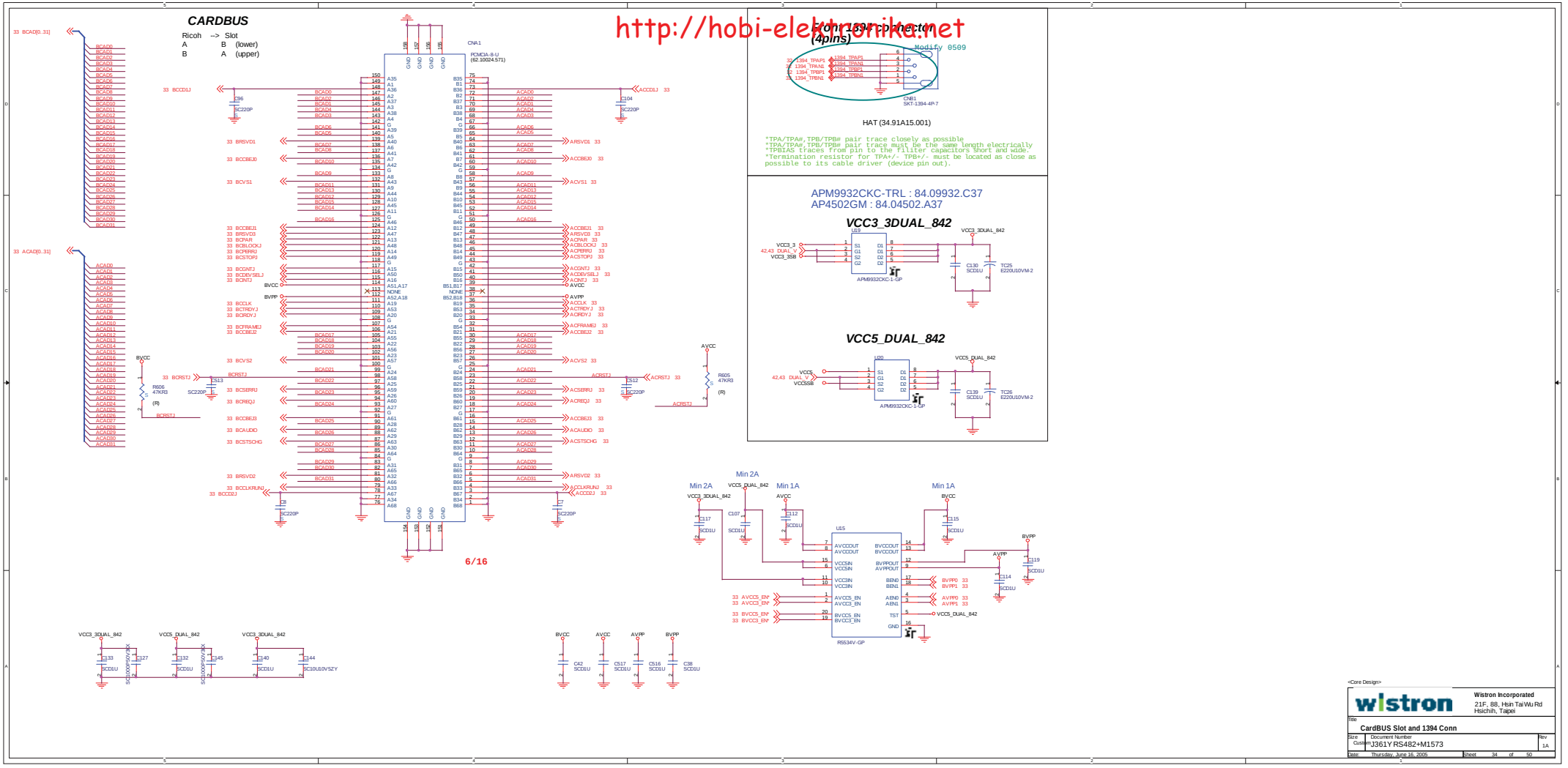

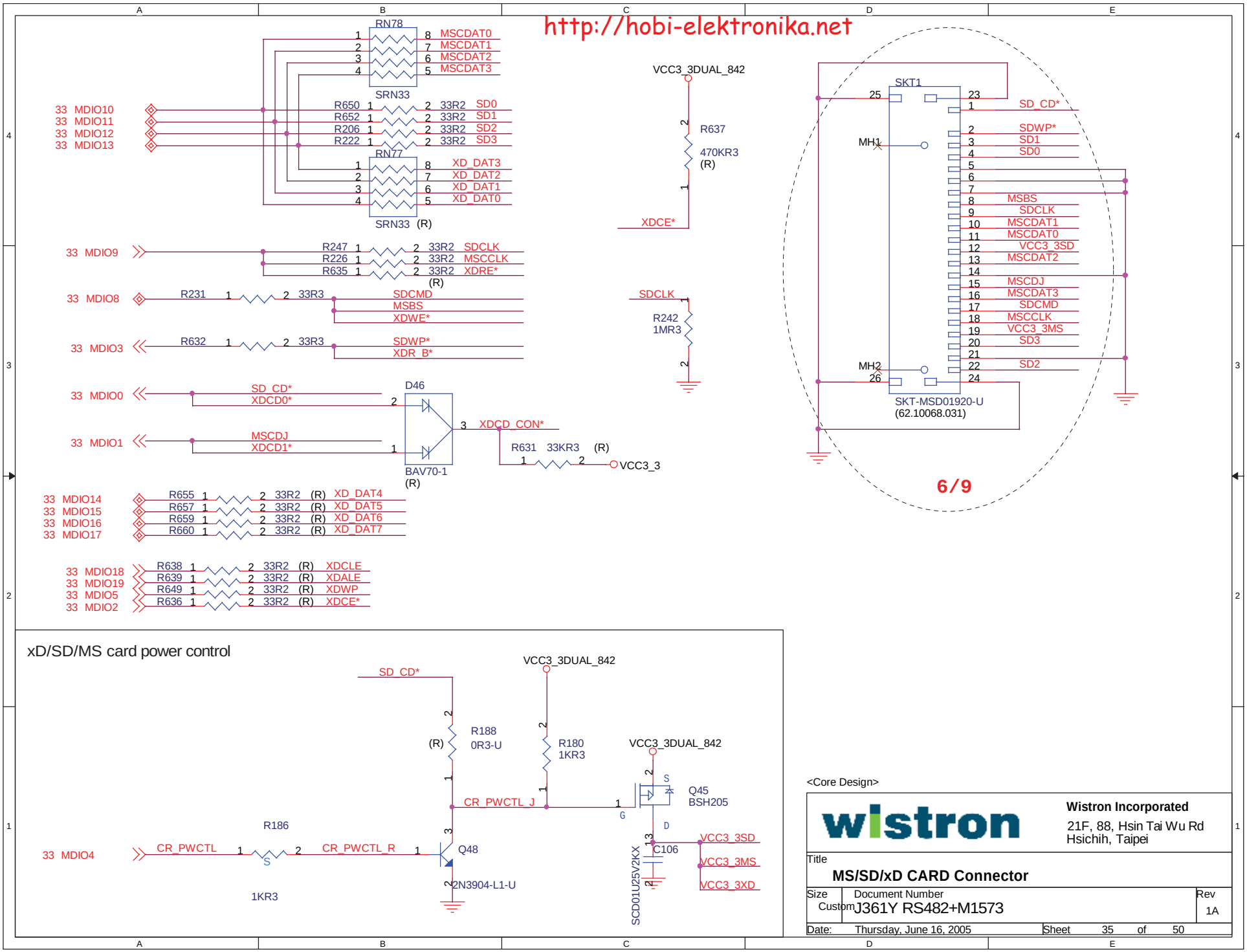

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **MS/SD/xD CARD Connector**

Size	Document Number	Rev
Custom	J361Y RS482+M1573	1A

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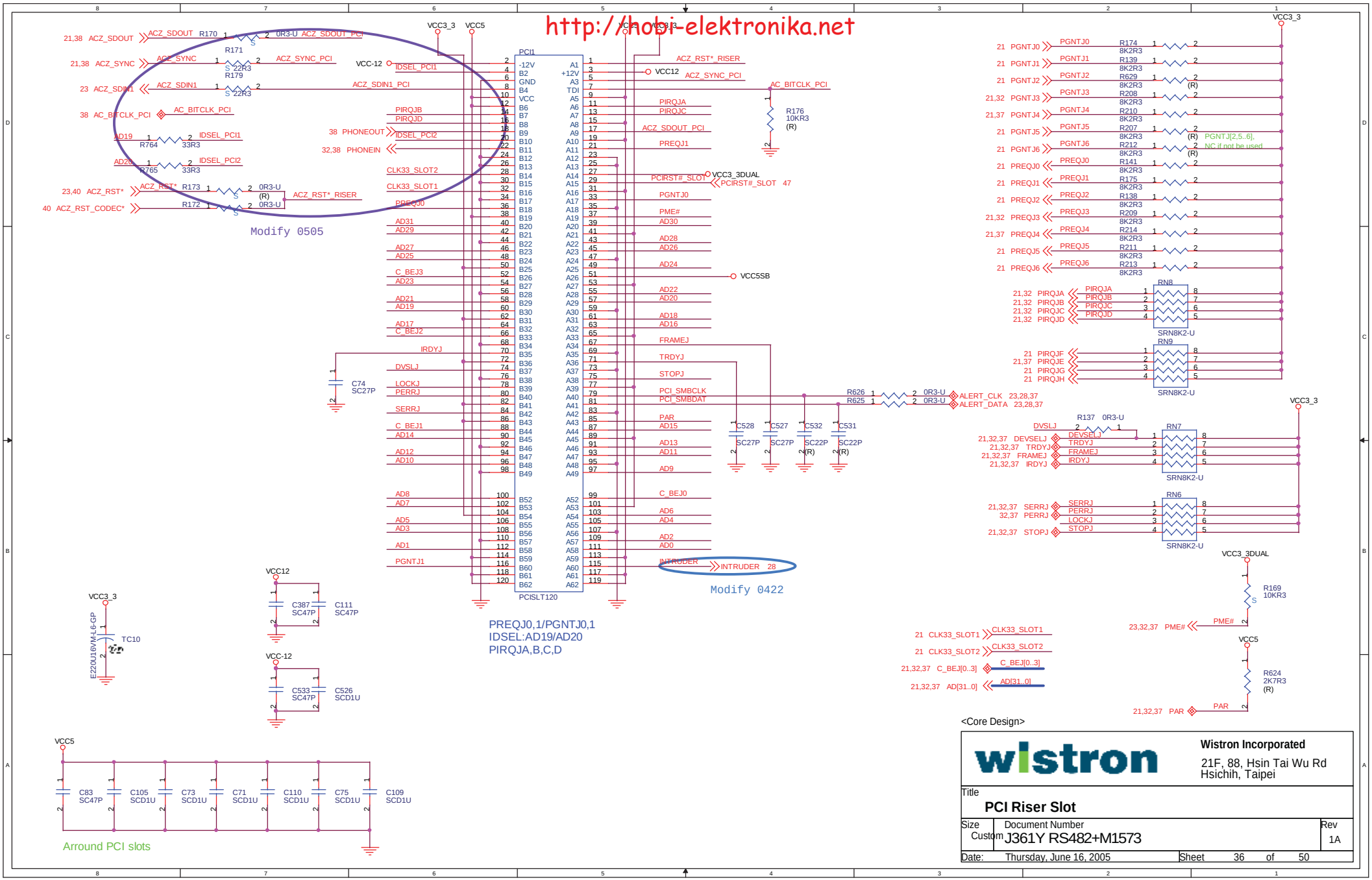
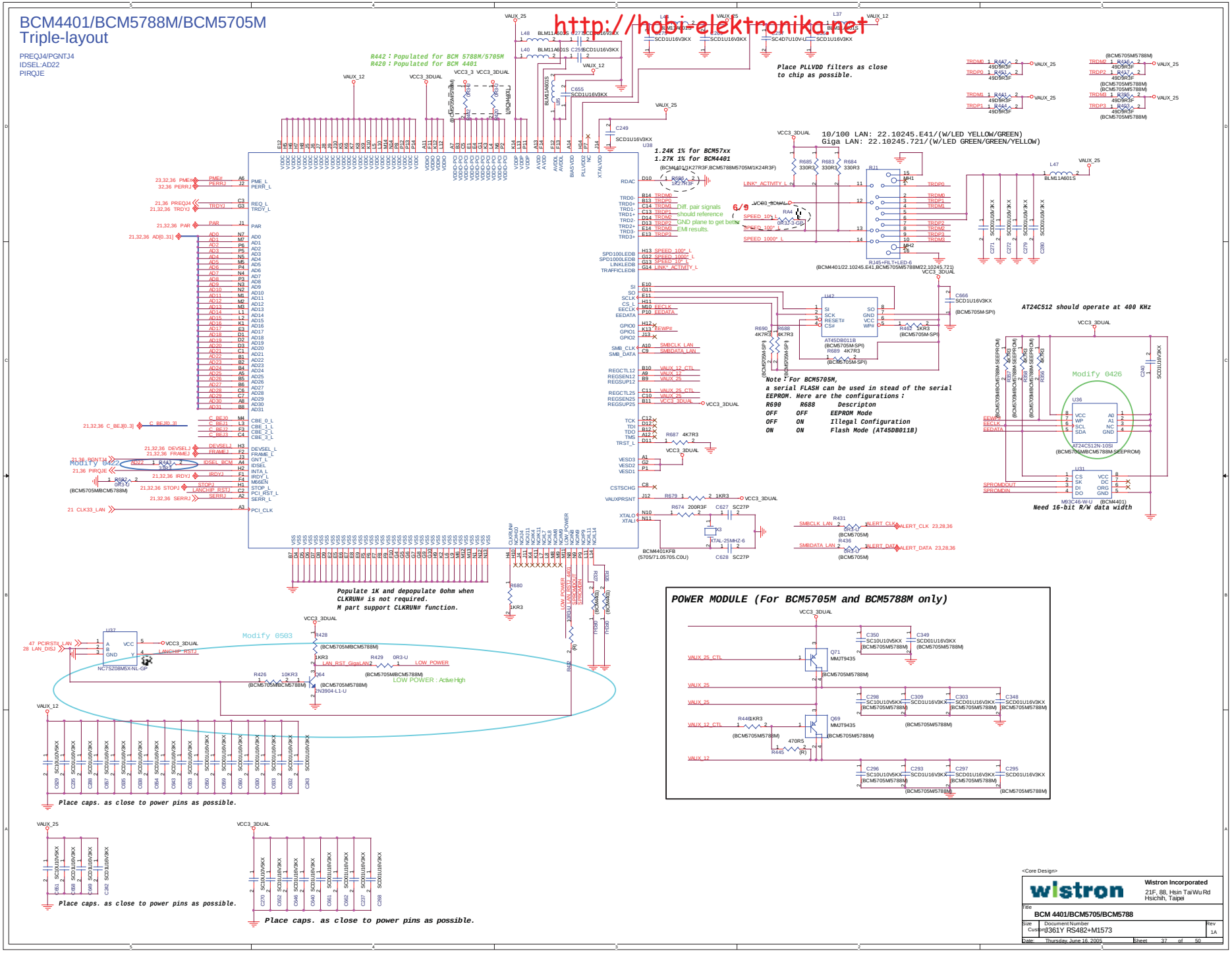
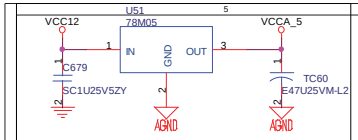
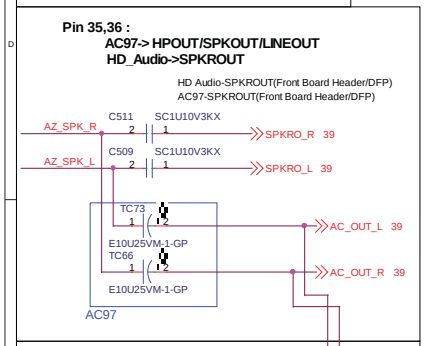
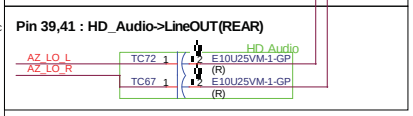


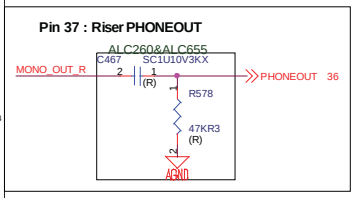


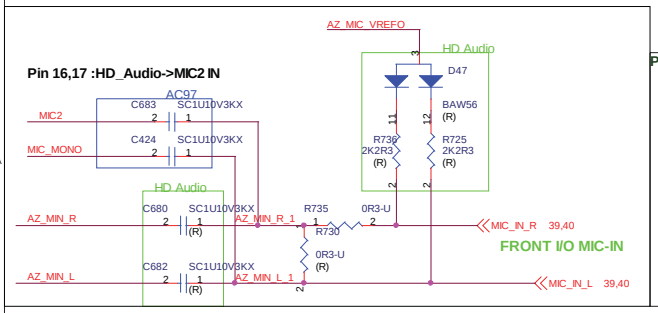
AC97 Audio Codec :ALC250/ALC655
HD Audio Codec: ALC260/ALC880

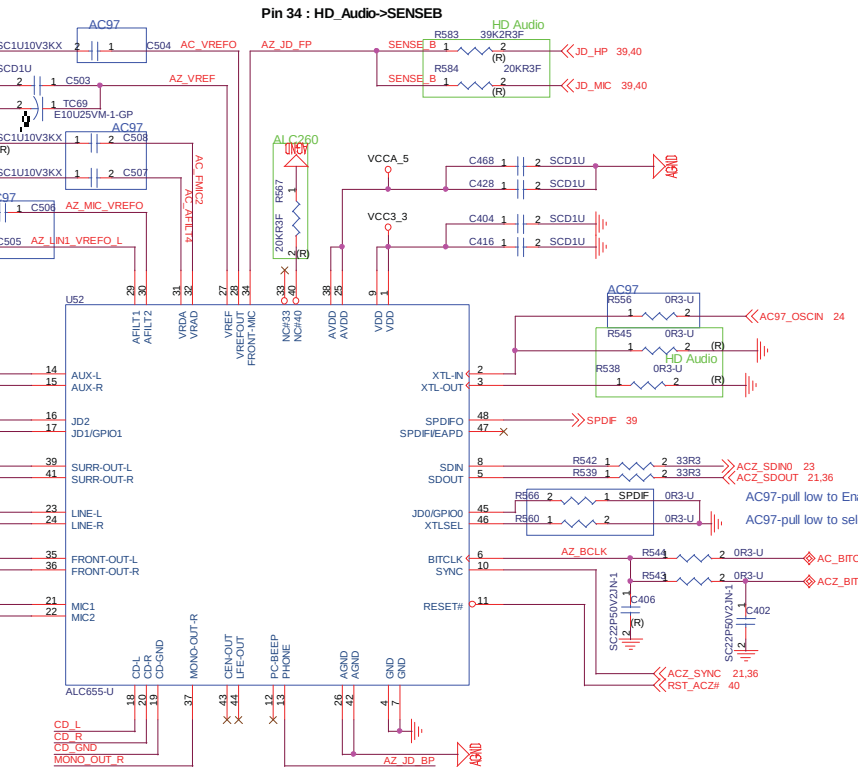


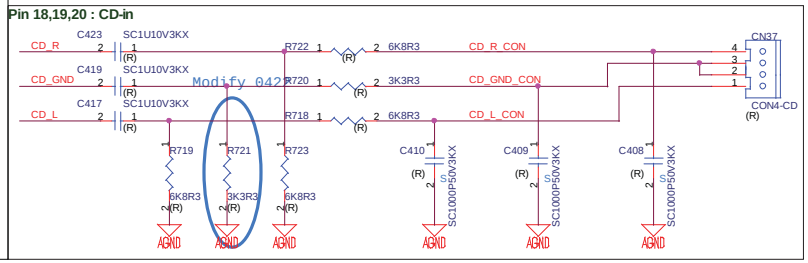


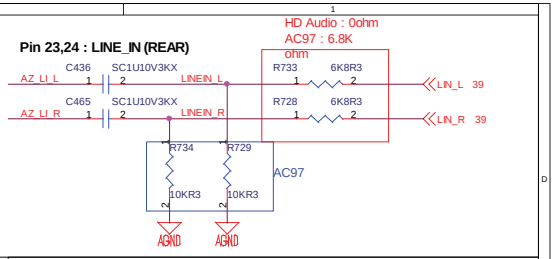


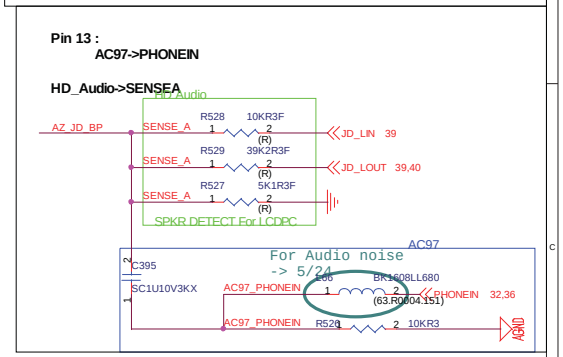


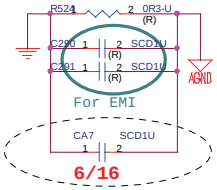












<Core Design>
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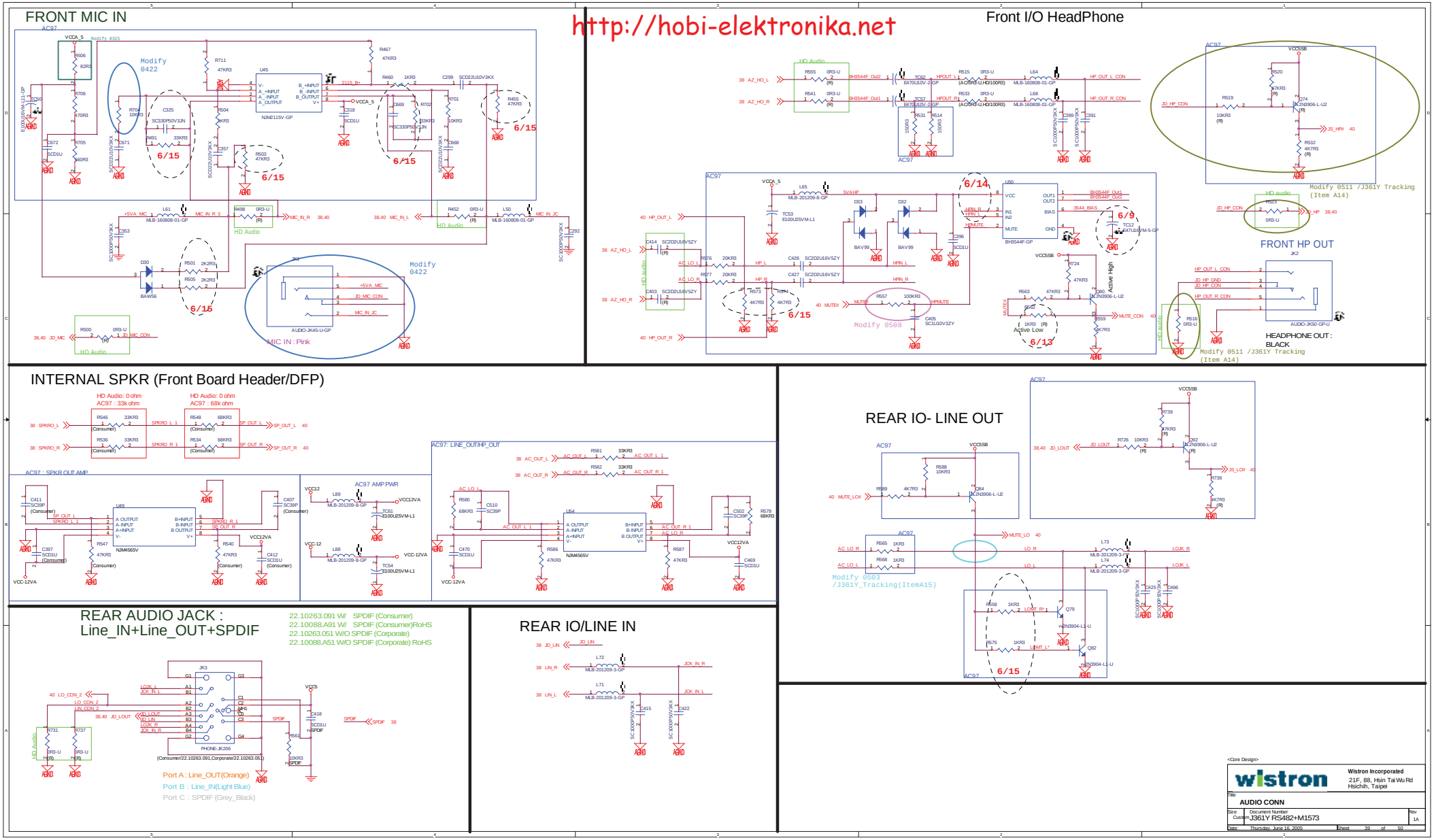
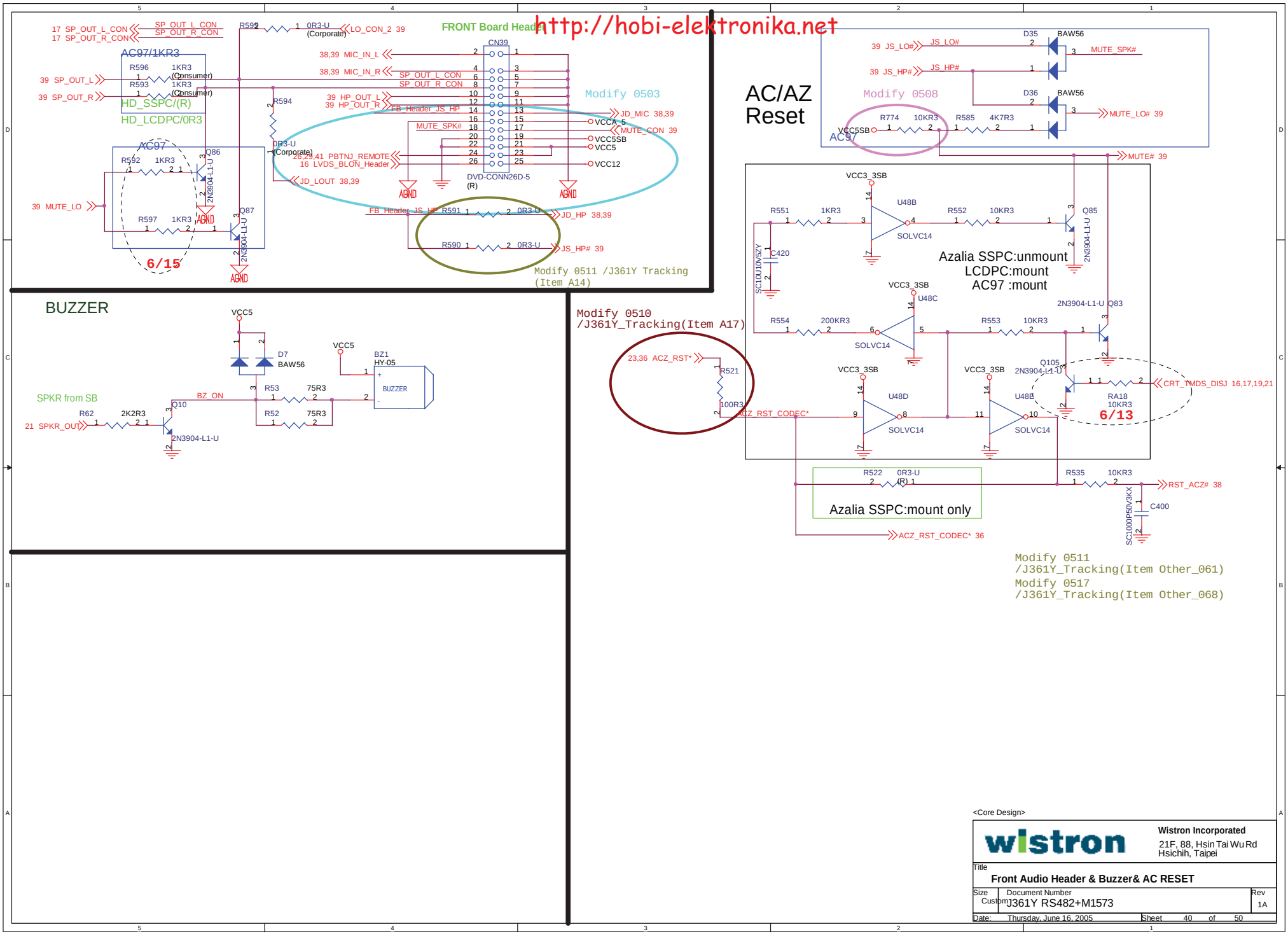
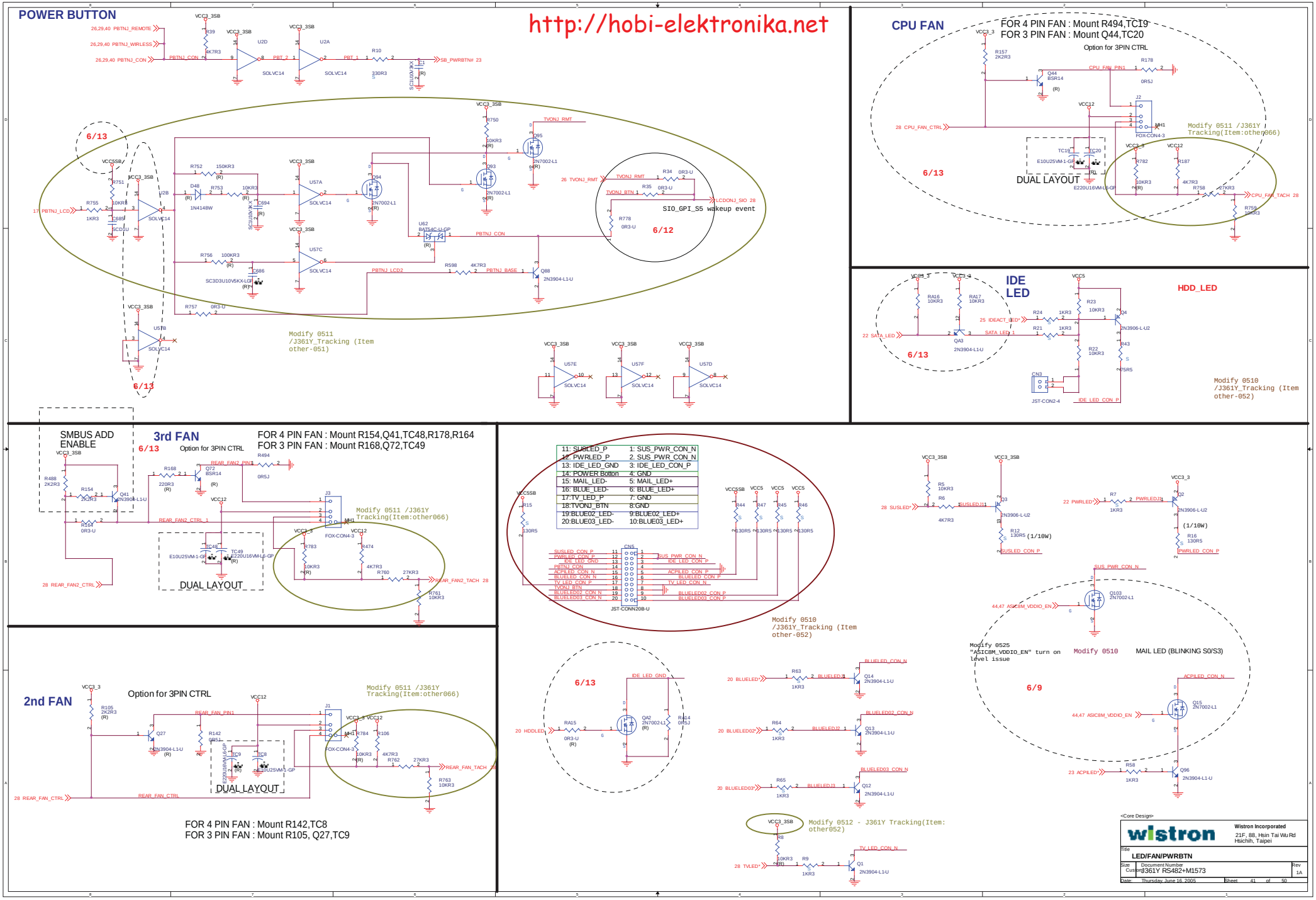
Hsichih, Taipei

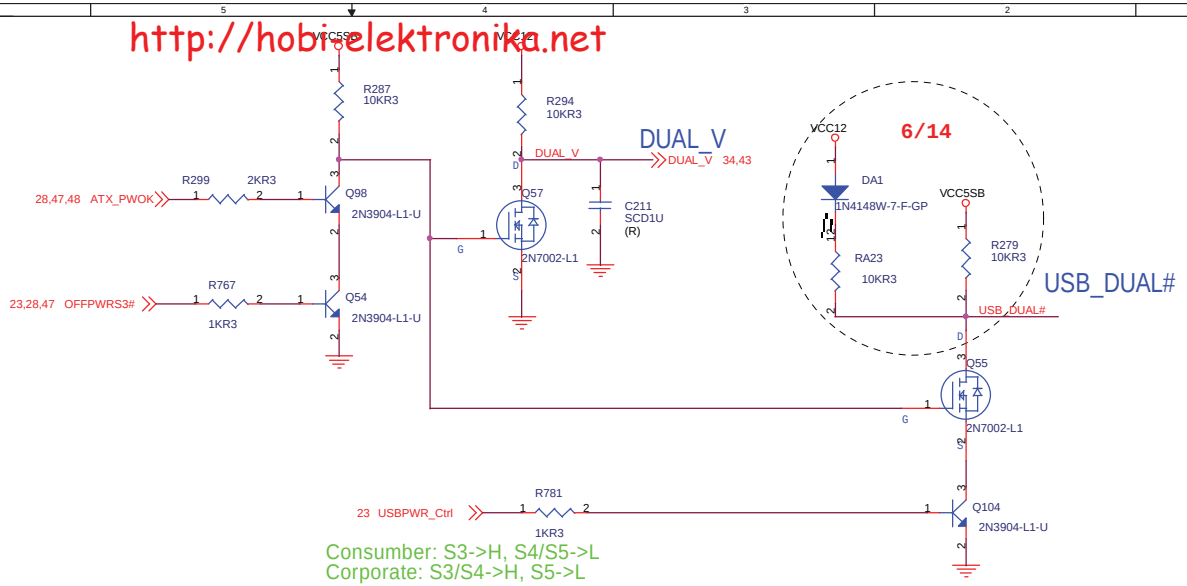
Title: Audio Codec
Size: Custom | Document Number: J361Y RS482+M1573 | Rev: 1A
Date: Thursday, June 16, 2005 | Sheet 38 of 50





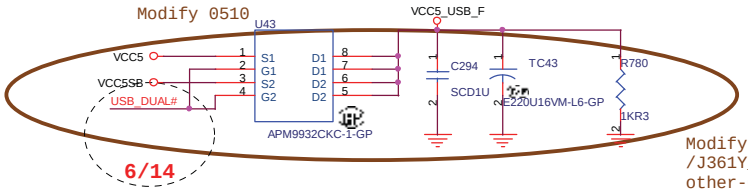


	ATX_PWOK	OFFPWRS3#	USBPWR_Ctrl Consumer	USBPWR_Ctrl Corporate	DUAL_V	USB_DUAL#
S0, S1	1	1	0	0	1	1
S3	0	0	1	1	0	0
S4	0	0	0	1	0	0:Corporate 1:Consumer
S5	0	0	0	0	0	1



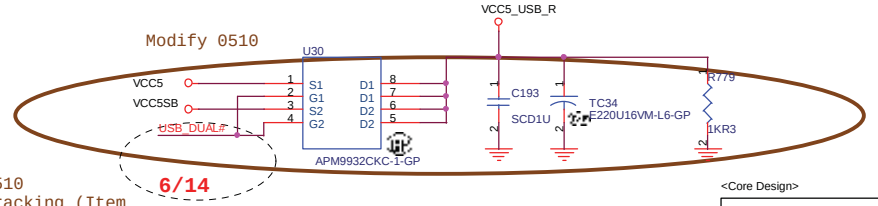
APM9932CKC-TRL : 84.09932.C37
AP4502GM : 84.04502.A37

FRONT USB POWER



Modify 0510 /J361Y_Tracking (Item other-014,057)

REAR USB/ PS2 KB POWER



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Title: USB POWER & PWR CTL

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VCC3_3SB

U26
APL1085
ADJ
VOUT
VIN

VCC5SB
C158 SCD1U
TC31 E220U16VM-L6-GP
VCC3_3SB
R248 100R3F
TC33 E220U16VM-L6-GP
VCC3_3SBADJ
R249 165R3F

VCC1.8_DUAL for SB Resume Power

U3
APL1087
ADJ/GND
VOUT
VIN

VCC3_3DUAL
E220U16VM-L6-GP
TC3
C15 SCD1U
VCC18_DUAL
VCC18_DUALADJ
R33 124R3F
TC1 E220U16VM-L6-GP
R32 54D9R3F

DDR_VCC5_DUAL FOR DDR & Card bus

VCC5SB
Q75
AP20P02GJ-GP
DDR_VCC5_DUAL
34,42 DUAL_V
Q77
AP60T03GH-GP
D34
1N5817M-L (R)
C421 SCD1U
TC63 E220U16VM-L6-GP
VCC5
<Core Design>

VCC3_3 DUAL

APM9932CKC-TRL : 84.09932.C37
AP4502GM : 84.04502.A37

VCC3_3DUAL
U4
VCC3_3
34,42 DUAL_V
VCC3_3SB
S1 G1 S2 G2
D1 D1 D2 D2
APM9932CKC-1-GP
C530 SCD1U
TC5 E220U16VM-L6-GP

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Title	Dual 5V, 3.3V, 1.8V, and 3.3VSB
Size A	Document Number J361Y RS482+M1573 Rev 1A
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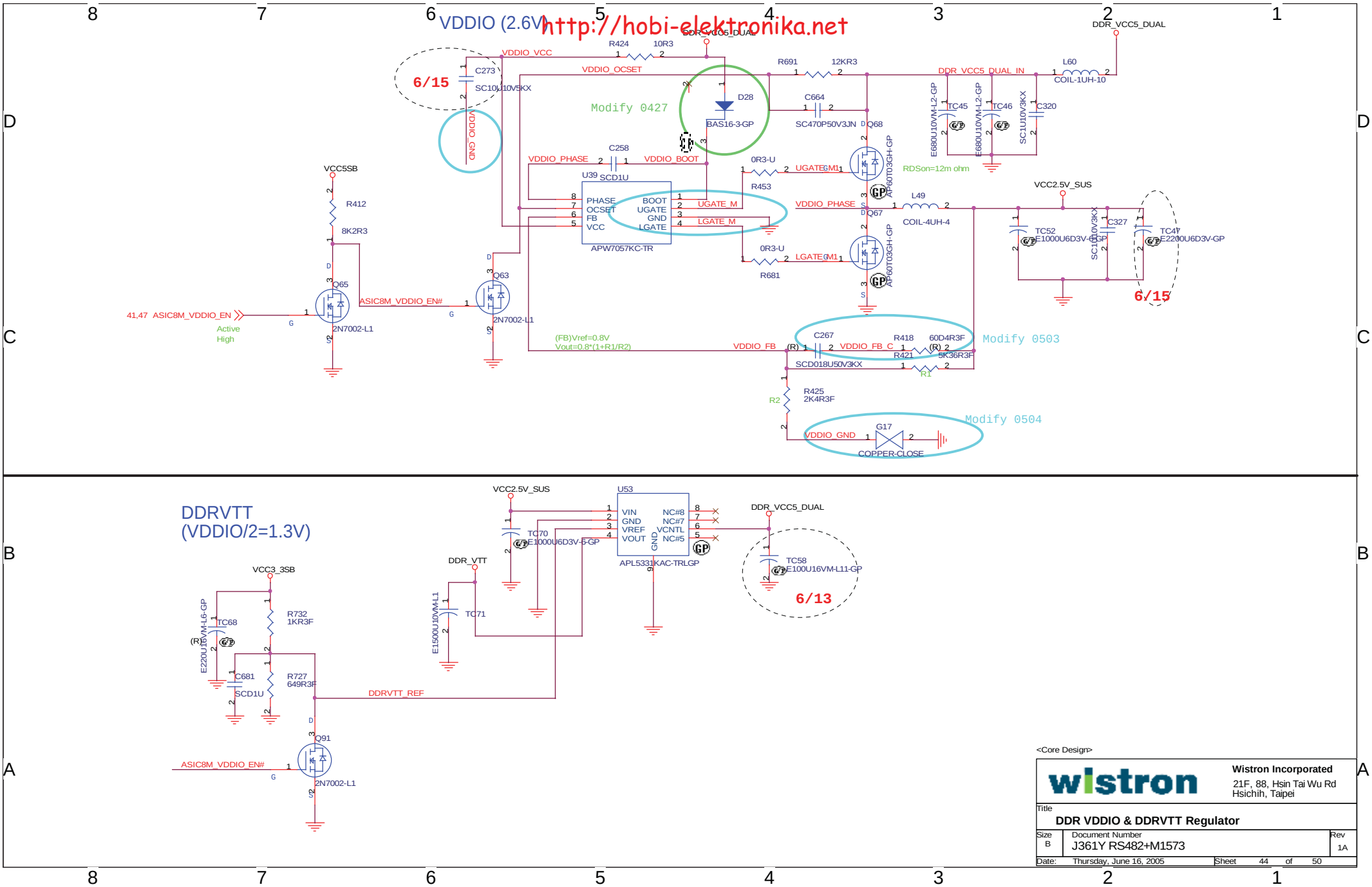
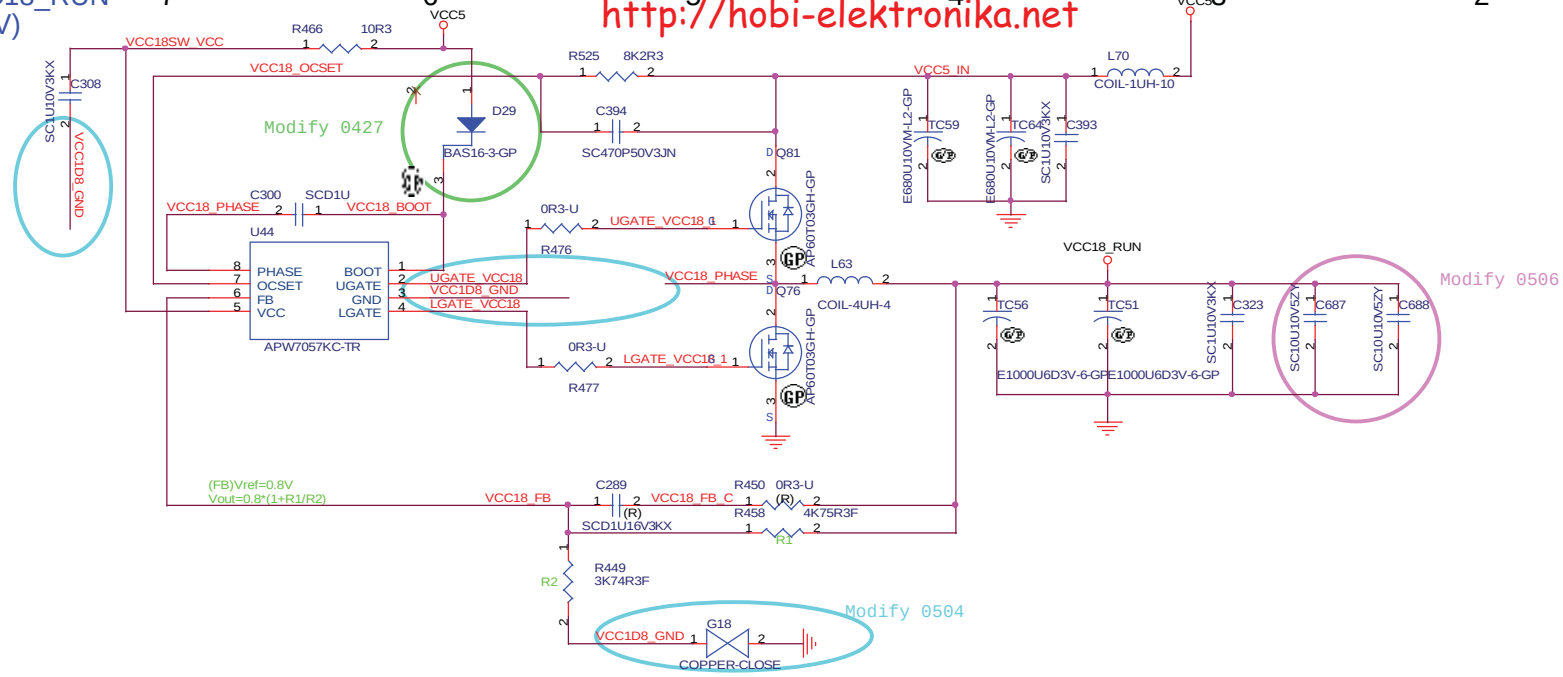
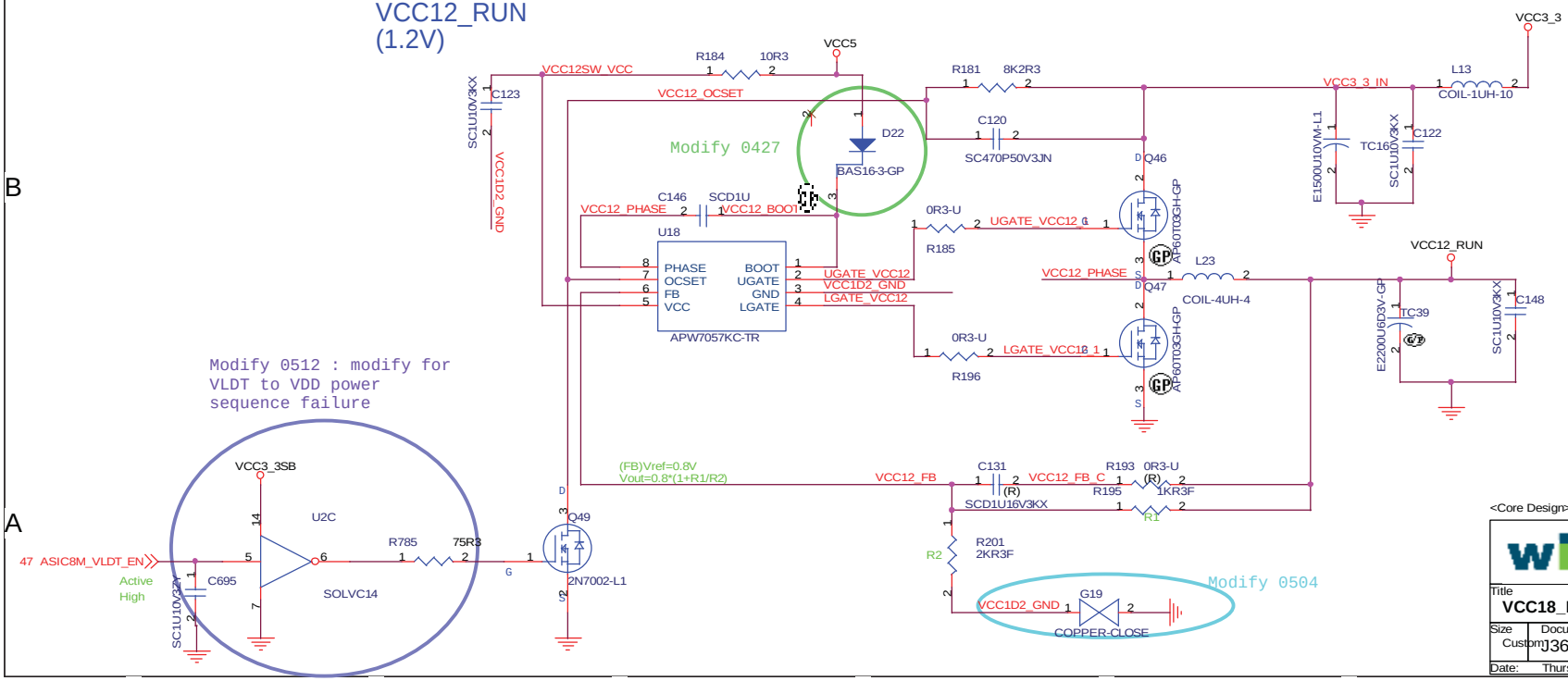


VCC18_RUN (1.8V)



VCC12_RUN (1.2V)



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Hsichih, Taipei

Title: **VCC18_RUN & VCC12_RUN**

Size	Document Number	Rev
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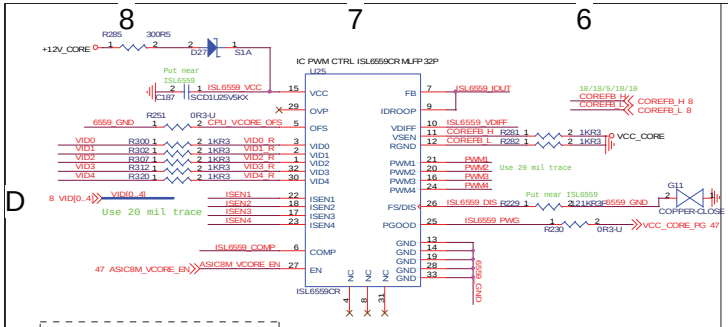
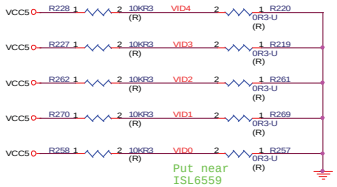
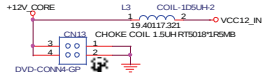
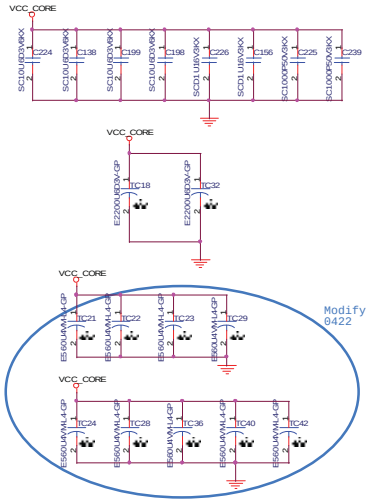




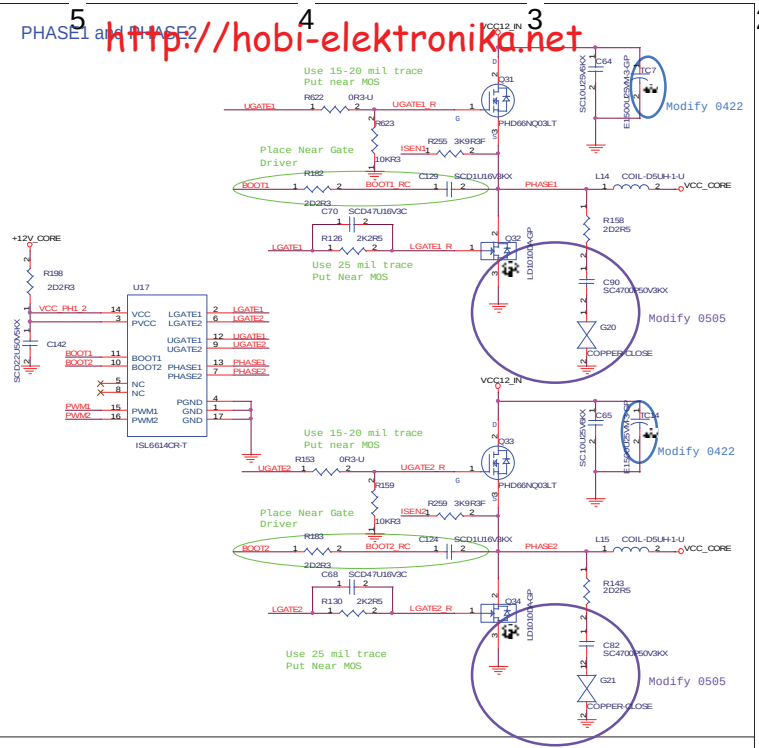
4 pin POWER Connector



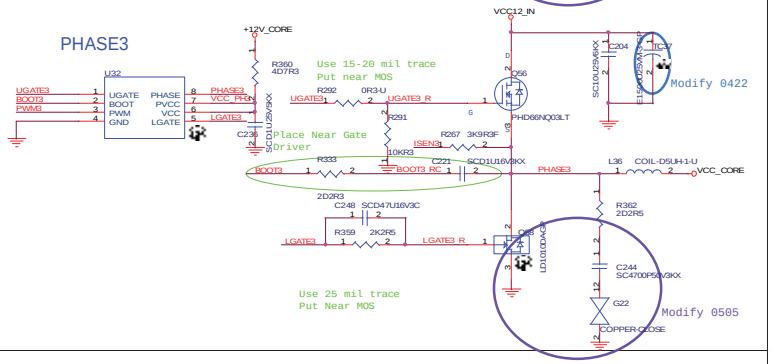
Output Capacitors



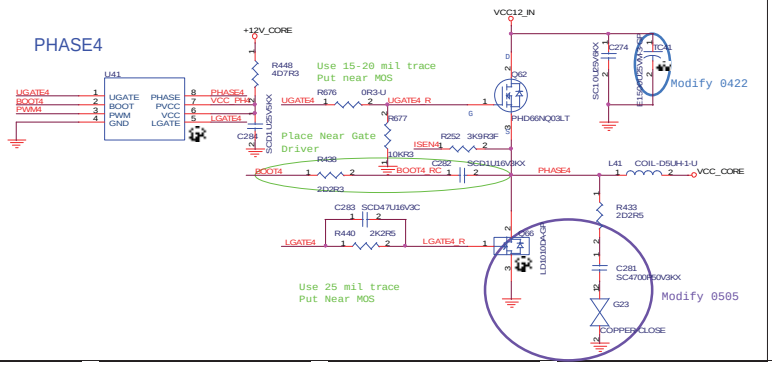
PHASE1 and PHASE2



PHASE3



PHASE4



VID Codes

CORE (V)	VID4	VID3	VID2	VID1	VID0
1.550	0	0	0	0	0
1.525	0	0	0	0	1
1.500	0	0	0	1	0
1.475	0	0	0	1	1
1.450	0	0	1	0	0
1.425	0	0	1	0	1
1.400	0	0	1	1	0
1.375	0	0	1	1	1
1.350	0	1	0	0	0
1.325	0	1	0	0	1
1.300	0	1	0	1	0
1.275	0	1	0	1	1
1.250	0	1	1	0	0
1.225	0	1	1	0	1
1.200	0	1	1	1	0
1.175	0	1	1	1	1
1.150	1	0	0	0	0
1.125	1	0	0	0	1
1.100	1	0	0	1	0
1.075	1	0	0	1	1
1.050	1	0	1	0	0
1.025	1	0	1	0	1
1.000	1	0	1	1	0
0.975	1	0	1	1	1
0.950	1	1	0	0	0
0.925	1	1	0	0	1
0.900	1	1	0	1	0
0.875	1	1	0	1	1
0.850	1	1	1	0	0
0.825	1	1	1	0	1
0.800	1	1	1	1	0
OFF	1	1	1	1	1

<Core Design>

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Title: VCORE(ISL6559)

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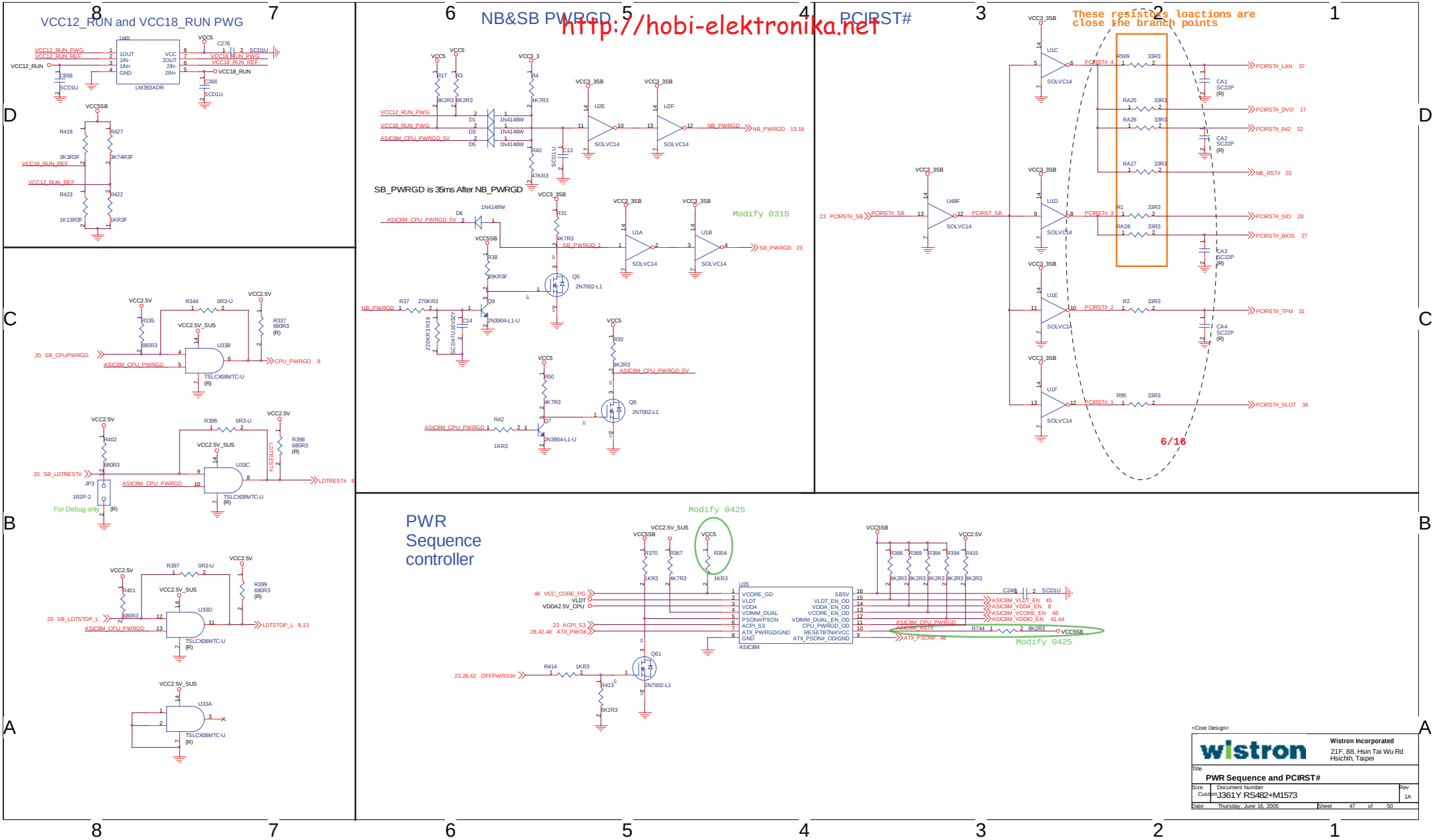
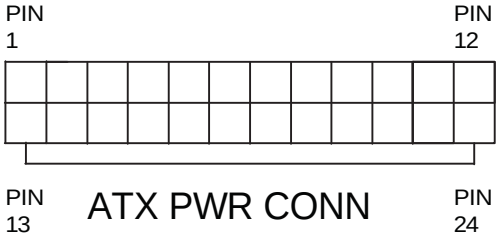
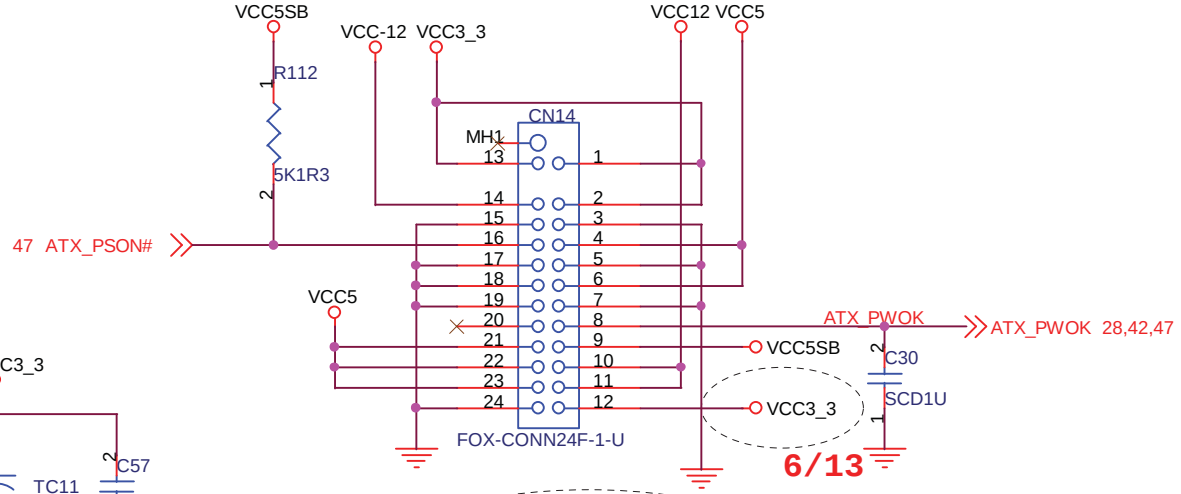
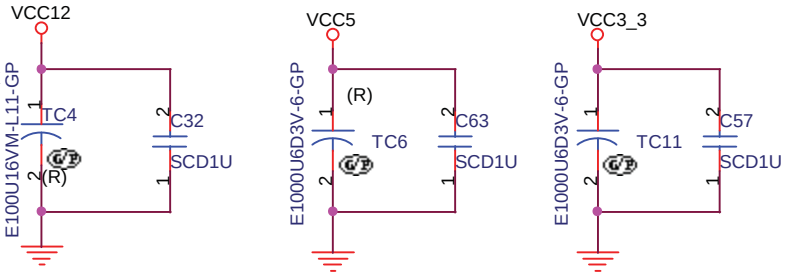


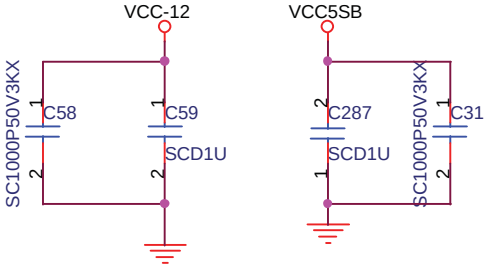
PWR CONN

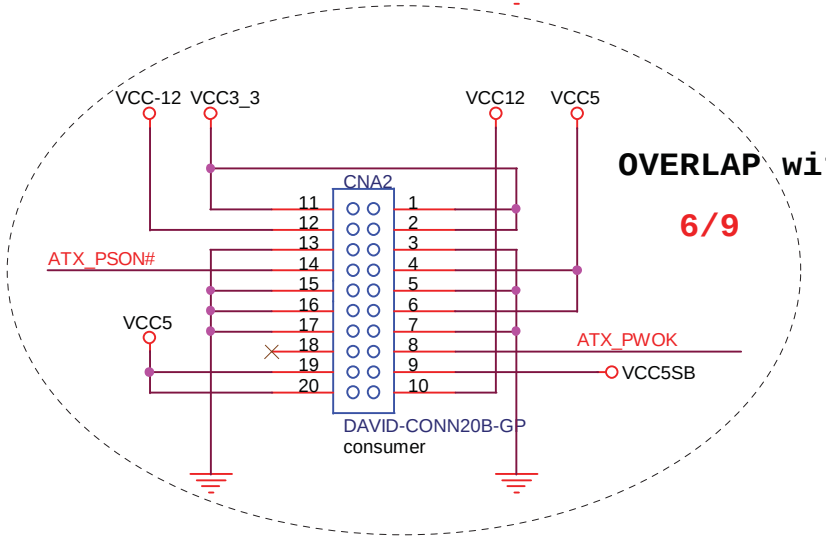
http://hobi-elektronika.net











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Title	ATX 24Pin conn
Size: A	Document Number: J361Y RS482+M1573
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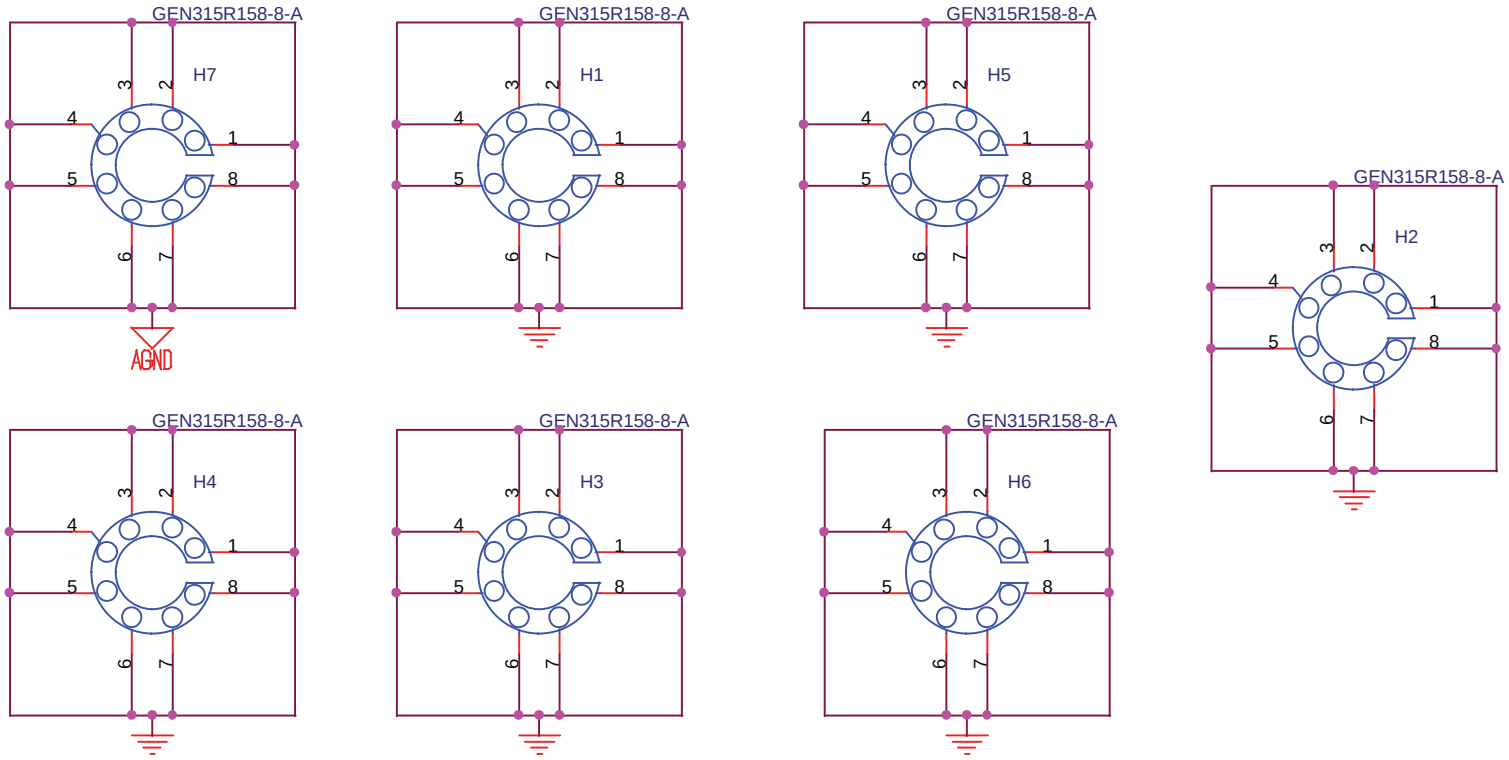

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Title
Screw Hole

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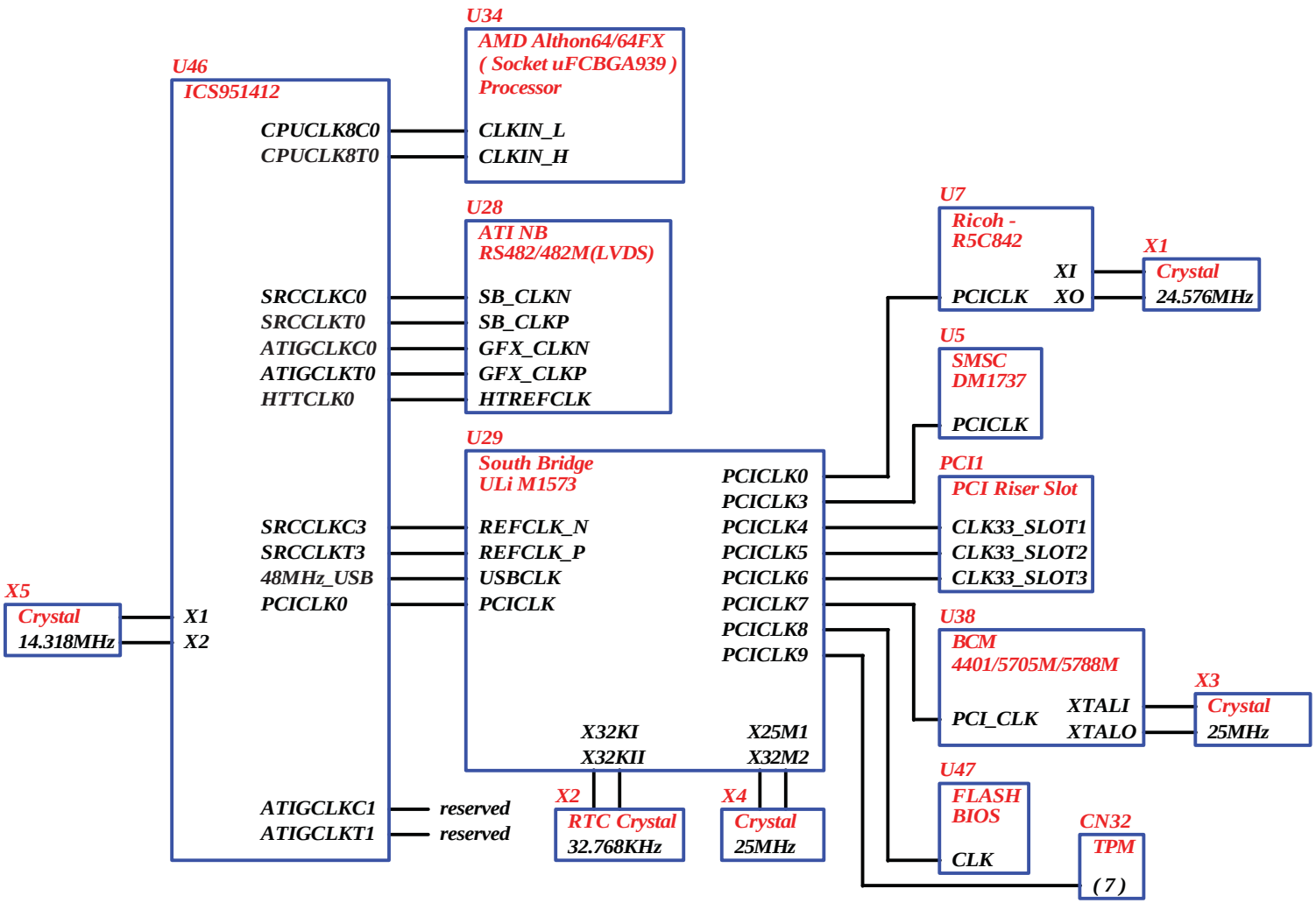

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

ATIGCLK Divider Selection

ATIG_Div(3:0)	ATIGCLK(1:0) (MHz)
1 0 0 0	100.00
0 0 1 1	114.29
TBD	133.33
0 0 1 0	160.00

<Core Design>

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Title: CLOCK MAP

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