VB161AX (Ginger) Main Board 0.1

Index

System Block

Version History

Version	Date	Description
00	Jul-20-'02	Initial

Power Block

USB CHANEL

PCIINT#	Device
USB1	System -1
USB2	P-R1
USB3	System-2
USB4	PR -2
USB5	Bluetooth
USB6	Bay

PCI REQ#/GNT#

REQ#/GNT#	Device
REQ#0	PCMCIA
REQ#1	IEEE1394
REQ#2	Unused
REQ#3	On Board LAN
REQ#4	Mini PCI
REQ#5	Unused

PCI INTERRUPT

PCIINT#	Device	
INT#0	PCIC	USB#1 / IDE
INT#1	PCIC	SMbus/AC-97
INT#2	Mini-PCI	USB#3
INT#3	Mini-PCI	USB#2
INT#4	On Board LAN	
INT#5	IEEE1394	
INT#6	Unused	
INT#7	Unused	

SMBus

SMBCNT[2:0]	Device
0,0,0	DIMM SLOT-0/1
0,0,1	PMU
0,1,0	PLL
0,1,1	ADM1030

PCI BUS NUMBER = #0

IDSEL	Dev.ID	Device
AD16	00h	GMCH(HOST/DRAM BRIDGE)
AD17	01h	GMCH(AGP BRIDGE)
AD18	02h	Unused
	1Dh	ICH4-M (USB2.0/USB1.1)
	1Eh	ICH4-M(Hub I/F to PCI Bridge)
	1Fh	ICH4-M(LPC,IDE,SMbus,AC-97)

PCI BUS NUMBER = #2

IDSEL	Dev.ID	Device
AD24	08h	Reserved for ICH4 (Internal LAN)
AD25	09h	OnBoard LAN
AD26	0Ah	PCIC
AD28	0Ch	On Board LAN
AD29	0Dh	MiniPCI
AD30	0Eh	IEEE1394
AD31	0Fh	Unused

Design Rquirement documents

DWG#	Description
A5CP149522-XX	Ginger A/W requirement
A1CP134338-XX	Common H/W specification of mobile platform

Rev.	Date	Design	Check	Appr.	Description
Design	02/05/07	Konaka Ohgomi	Check	Fuchida	Appr. Fukuyo

TITLE: VB161AX MAIN

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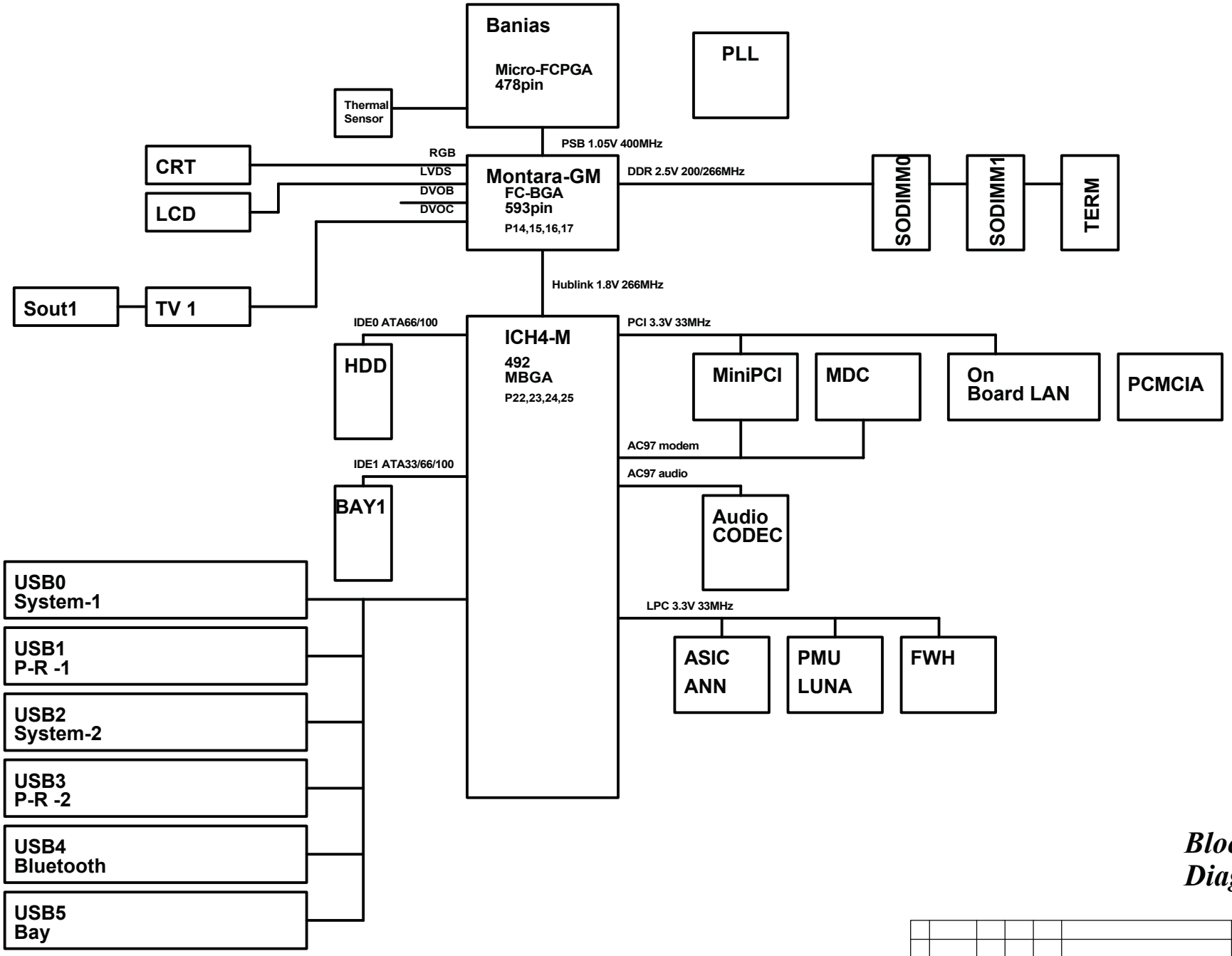
system block diagram



Block Diagram

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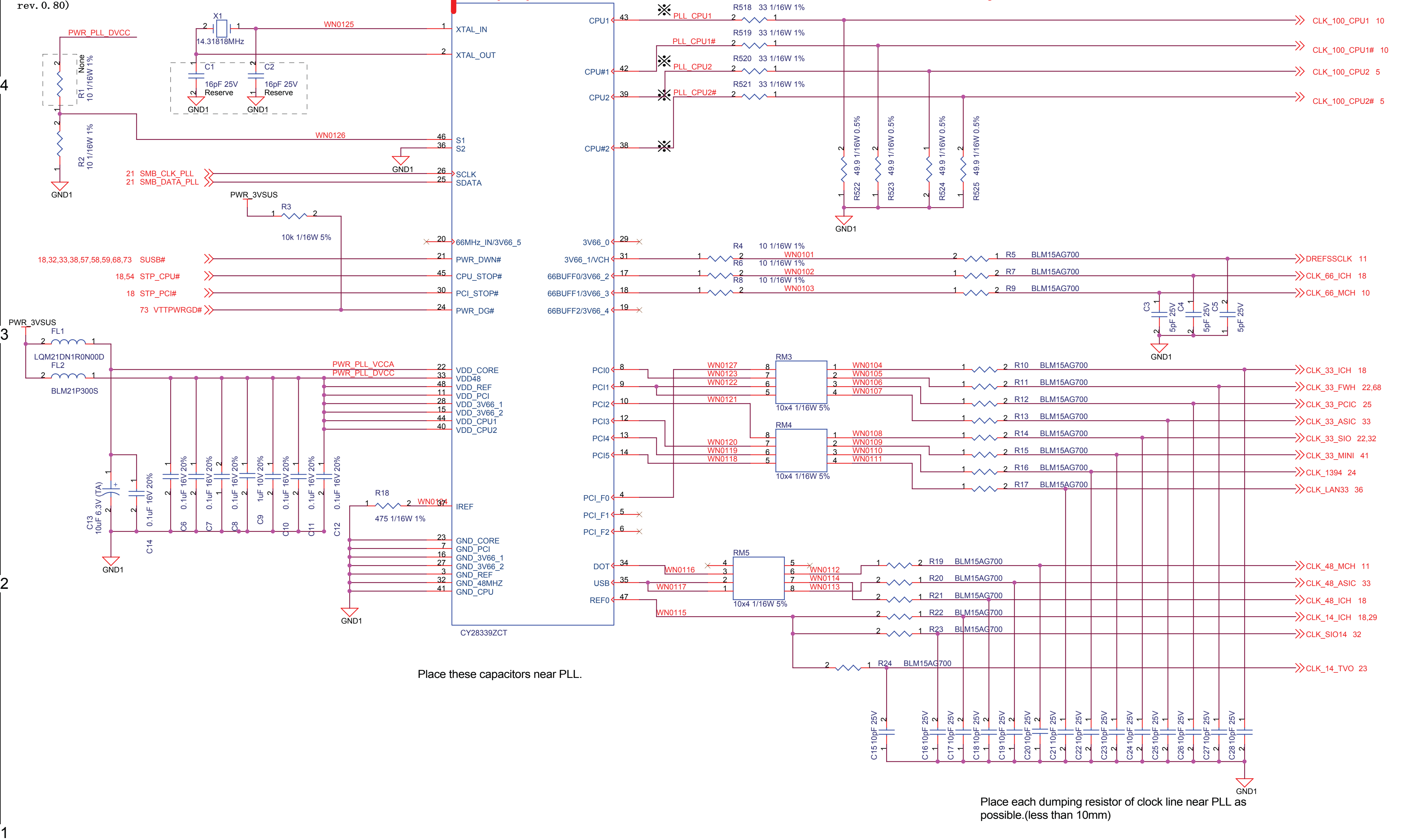
Place cyrstal within 500mils of Clk_TITAN
(by ALMADOR-M CHIPSET/MOBILE TUALATIN
PROCESSOR
CUSTMER REFERENCE BOARD SCHEMATICS
rev.0.80)

NOTE
These resistor limits use the PLL.
(No same as Almador requirements)



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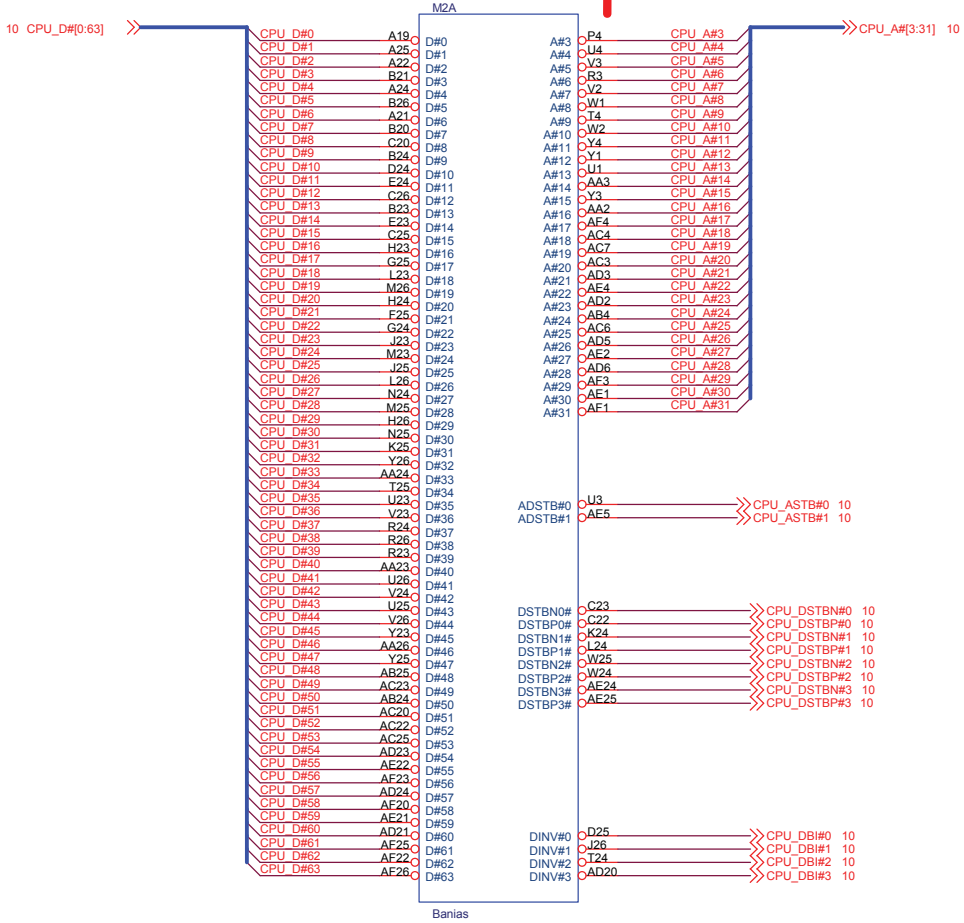
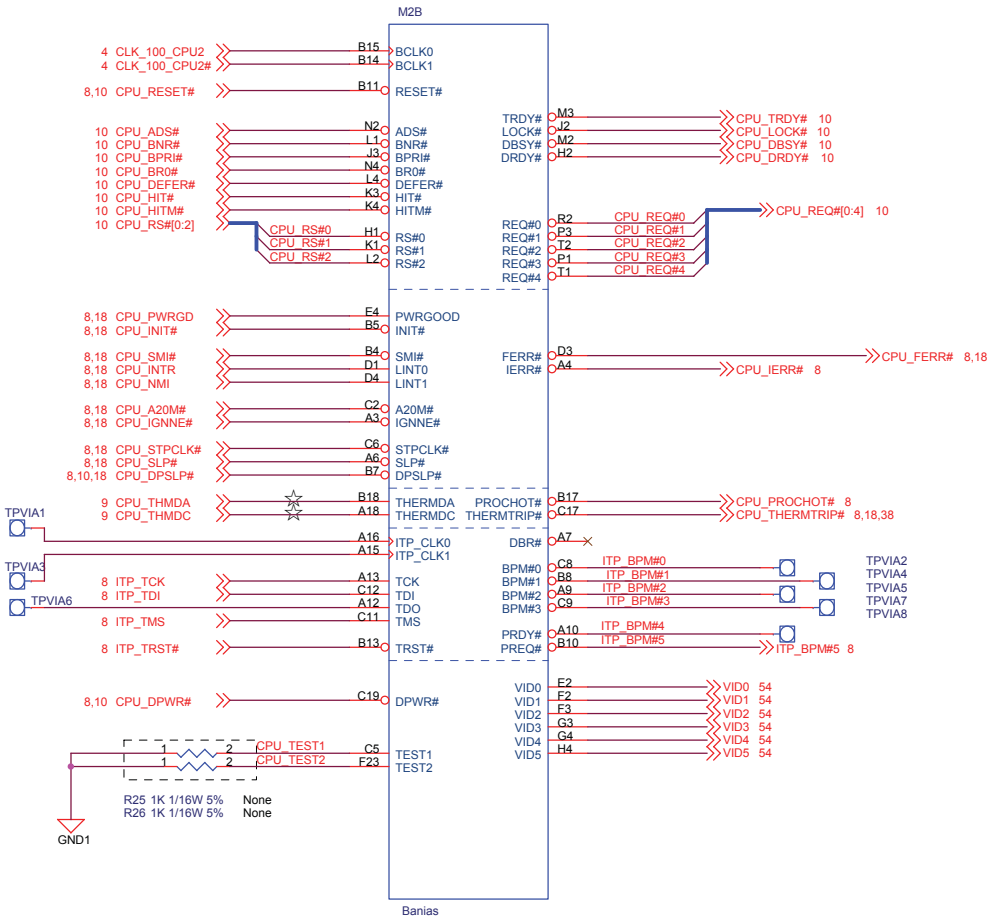
PLL





CPU_ASTB#0, CPU_ASTB#1はそれぞれの両側をGND1にて囲うこと
Guard CPU_ASTB#0, CPU_ASTB#1 with GND1 respectively.

CPU_DSTBx#[0:3]は各ペアごとに両側をGND1にて囲うこと
Each CPU_DSTBx#[0:3] strobe pear should be guarded with GND1 respectively.

☆印の付いた信号線(CPUTHMDA,CPUTHMDC)は、
GND1で両側をガードすること
(12ページ参照)

CPUTHMDA, CPUTHMDC with☆
is guraded with GND1

BANIAS_1

CPU 1 of 3

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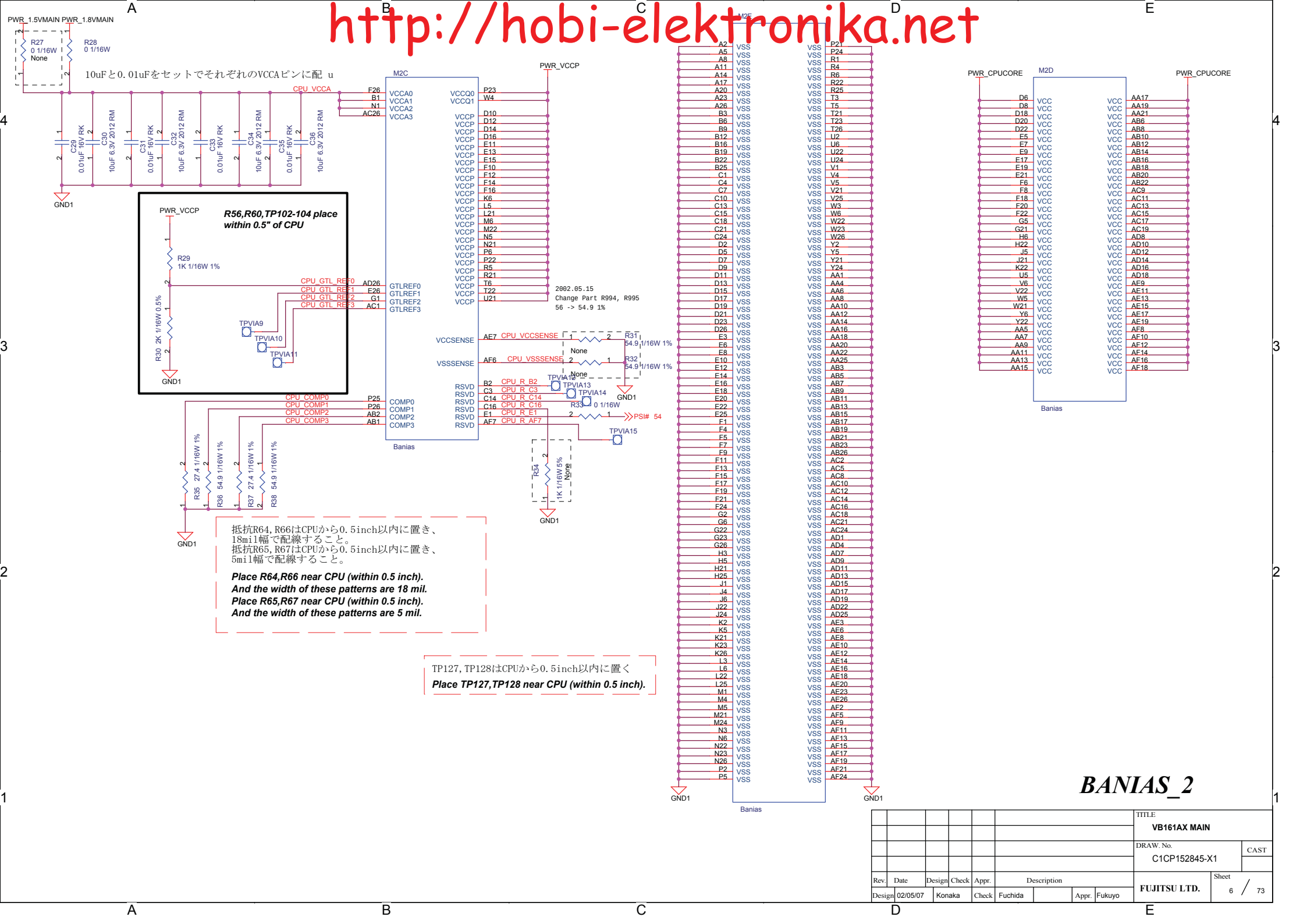

M3

BANIAS

PWR_CPUCORE

C37 0.22uF 10V FZ
C38 0.22uF 10V FZ
C39 0.22uF 10V FZ
C40 0.22uF 10V FZ
C41 0.22uF 10V FZ
C42 0.22uF 10V FZ
C43 0.22uF 10V FZ
C44 0.22uF 10V FZ
C45 0.22uF 10V FZ
C46 0.22uF 10V FZ
C47 0.22uF 10V FZ
C48 0.22uF 10V FZ
C49 0.22uF 10V FZ
C50 0.22uF 10V FZ
C51 0.22uF 10V FZ
C52 0.22uF 10V FZ

GND1

C57 10uF 6.3V 2012 RM
C58 10uF 6.3V 2012 RM
C59 10uF 6.3V 2012 RM
C60 10uF 6.3V 2012 RM
C61 10uF 6.3V 2012 RM
C62 10uF 6.3V 2012 RM
C63 10uF 6.3V 2012 RM
C64 10uF 6.3V 2012 RM
C65 10uF 6.3V 2012 RM
C66 10uF 6.3V 2012 RM
C67 10uF 6.3V 2012 RM
C68 10uF 6.3V 2012 RM
C69 10uF 6.3V 2012 RM
C70 10uF 6.3V 2012 RM
C71 10uF 6.3V 2012 RM
C72 10uF 6.3V 2012 RM

GND1

Sand pit ciucuit!

C73 0.1uF 10V RK
C74 0.1uF 10V RK
C75 0.1uF 10V RK
C76 0.1uF 10V RK
R39 10 1/16W 5%
R40 10 1/16W 5%
R41 10 1/16W 5%
R42 10 1/16W 5%

GND1

本回路ブロックは、CPU周囲のPWR_CPU内層べの４辺に均等に配置すること。

PWR_VCCP

C79 0.1uF 10V RK
C80 0.1uF 10V RK
C81 0.1uF 10V RK
C82 0.1uF 10V RK
C83 0.1uF 10V RK
C84 0.1uF 10V RK
C85 0.1uF 10V RK
C86 0.1uF 10V RK
C87 10uF 6.3V 2012 RM
C88 10uF 6.3V 2012 RM

GND1

CPU Socket
Primary Side

12 x 150uF

CPU Socket
Secondary Side

4x 2.2uF

11x 2.2uF

図中のコンデンサはCPUVCC供給側に配置すること。

CPU
PassC

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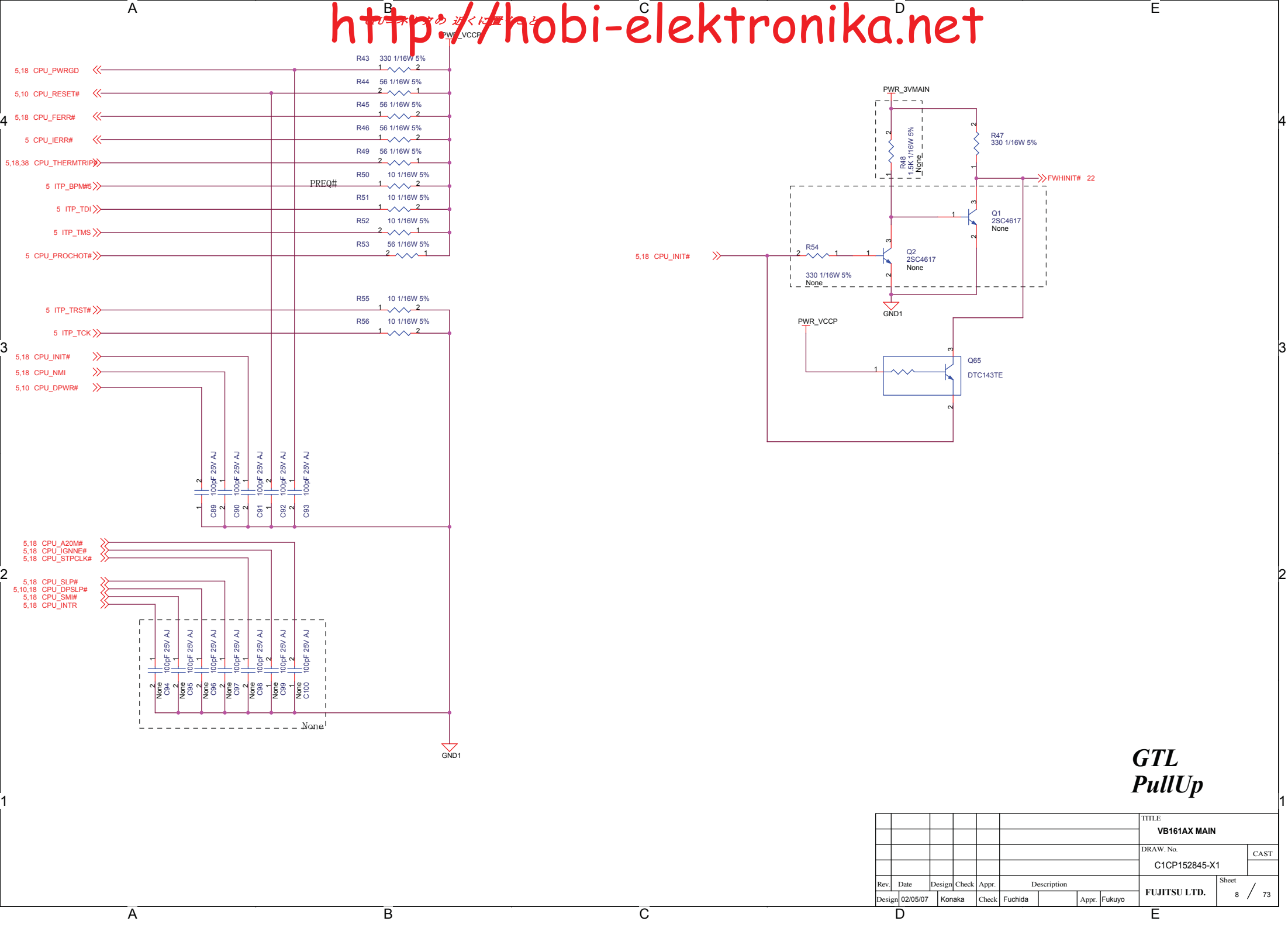

GTL PullUp

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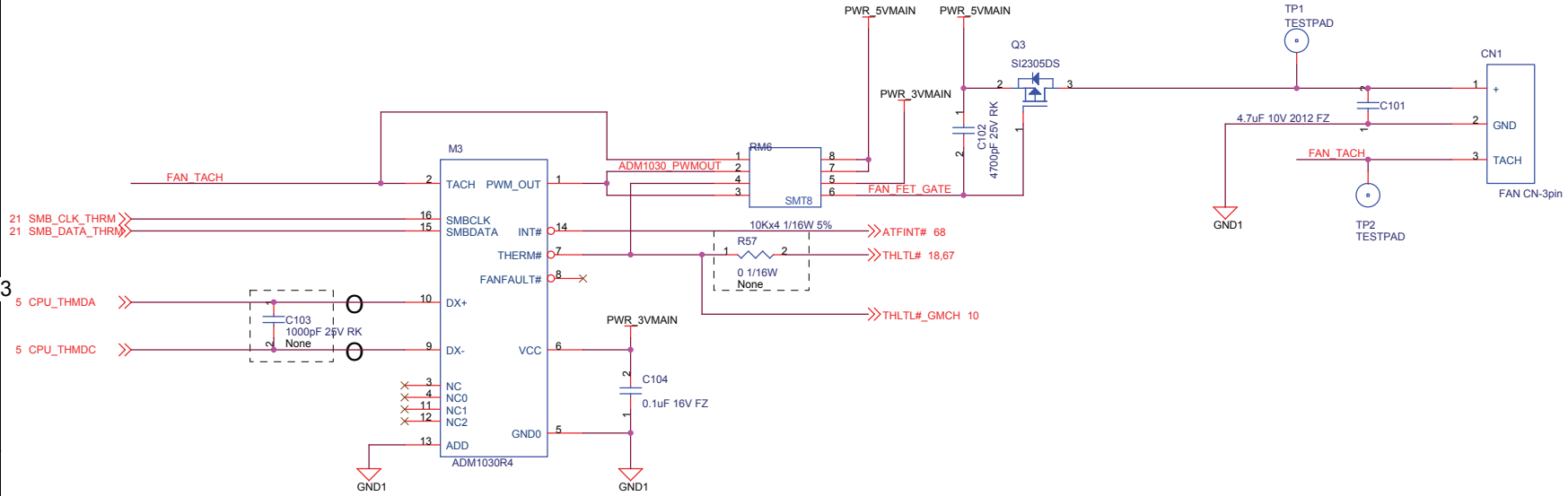

これらの部品はCPUの近くに配置すること。
Place each component near CPU.

CPU_THMDA, CPU_THMDCのパターンが最短になるよう、
ADM1030(M5)は、CPUの近傍に配置すること。

Place ADM1030(M5) near CPU(M3) to control
CPU_THMDA,CPU_THMDC patterns as short
as possible.

CPU_THMDA, CPU_THMDC両端に入っているコンデンサ
C108(1000pF)は、ADM1030(M5)の直近に配置すること。
Place and C108(1000pF) nearest ADM1030(M5).

○印の付いた信号線(CPU_THMDA,CPU_THMDC)は、
GND1で両側をガードすること
（下図参照）
Guard these signals(CPU_THMDA,CPU_THMDC) that marked "O"
at the both sides by GND1 pattern.
(Look at follow figure.)

10mil
10mil
10mil
10mil

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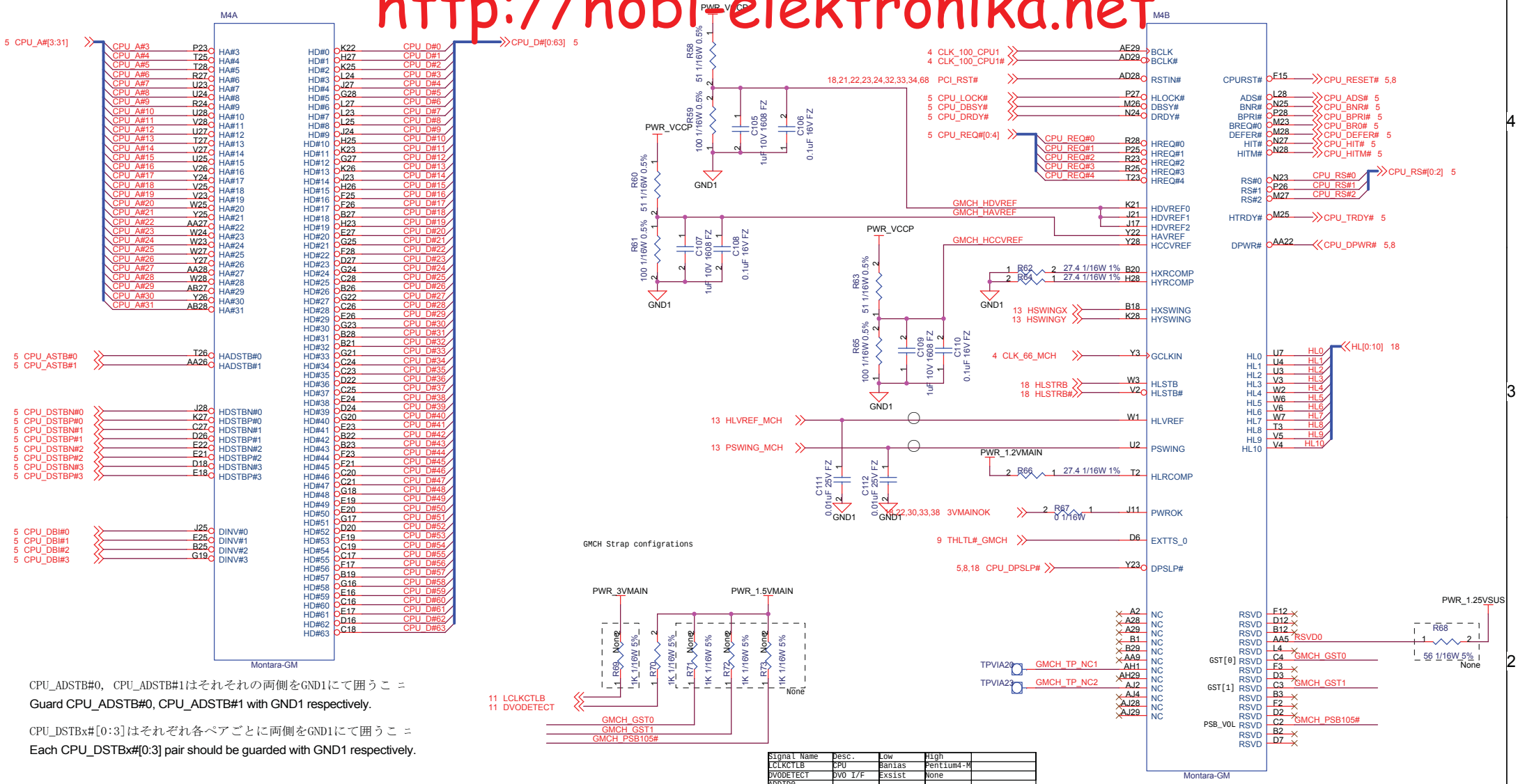

CPU_ADSTB#0, CPU_ADSTB#1はそれぞれの両側をGND1にて囲うこと
Guard CPU_ADSTB#0, CPU_ADSTB#1 with GND1 respectively.

CPU_DSTBx#[0:3]はそれぞれ各ペアごとに両側をGND1にて囲うこと
Each CPU_DSTBx#[0:3] pair should be guarded with GND1 respectively.

Signal Name	Desc.	Low	High	
LCLKCTLB	CPU	Banias	Pentium4-M	
DVODETECT	DVO I/F	Exsist	None	
ADDID0				
ADDID1				
ADDID2				
ADDID3				
ADDID4				
ADDID5				
ADDID6				
GST0	00 : FSB=400MHz/Mem=133MHz/Gfx=200/DDR=1.2			
GST1	01 : FSB=400MHz/Mem=100MHz/Gfx=200/DDR=1.2			
PSB105#	PSB VCC	PSB=1.05V	REserved	

○のついた信号線は 25mil 以上の太さで配線し、左右と下をベタの GND 線で囲むこと。
The width of signals that are marked "O" must be more than 25 mil and guard the both sides, the top and the bottom of them by GND1 pattern.

抵抗R164,R165はGMCH(M78)から0.5inch以内に置き 15mil幅以上で配線すること。
Place R164,R165 near MCH(M6) (within 0.5 inch). And the width of these patterns are more than 15 mil.

コンデンサC754はGMCH(M78)の近傍に配置すること
Place C754 near GMCH(M78)

HLSTRB/HLSTRB#ペアは両側をGND1にて囲うこと
HLSTRB/HLSTRB# pear should be guarded with GND1.

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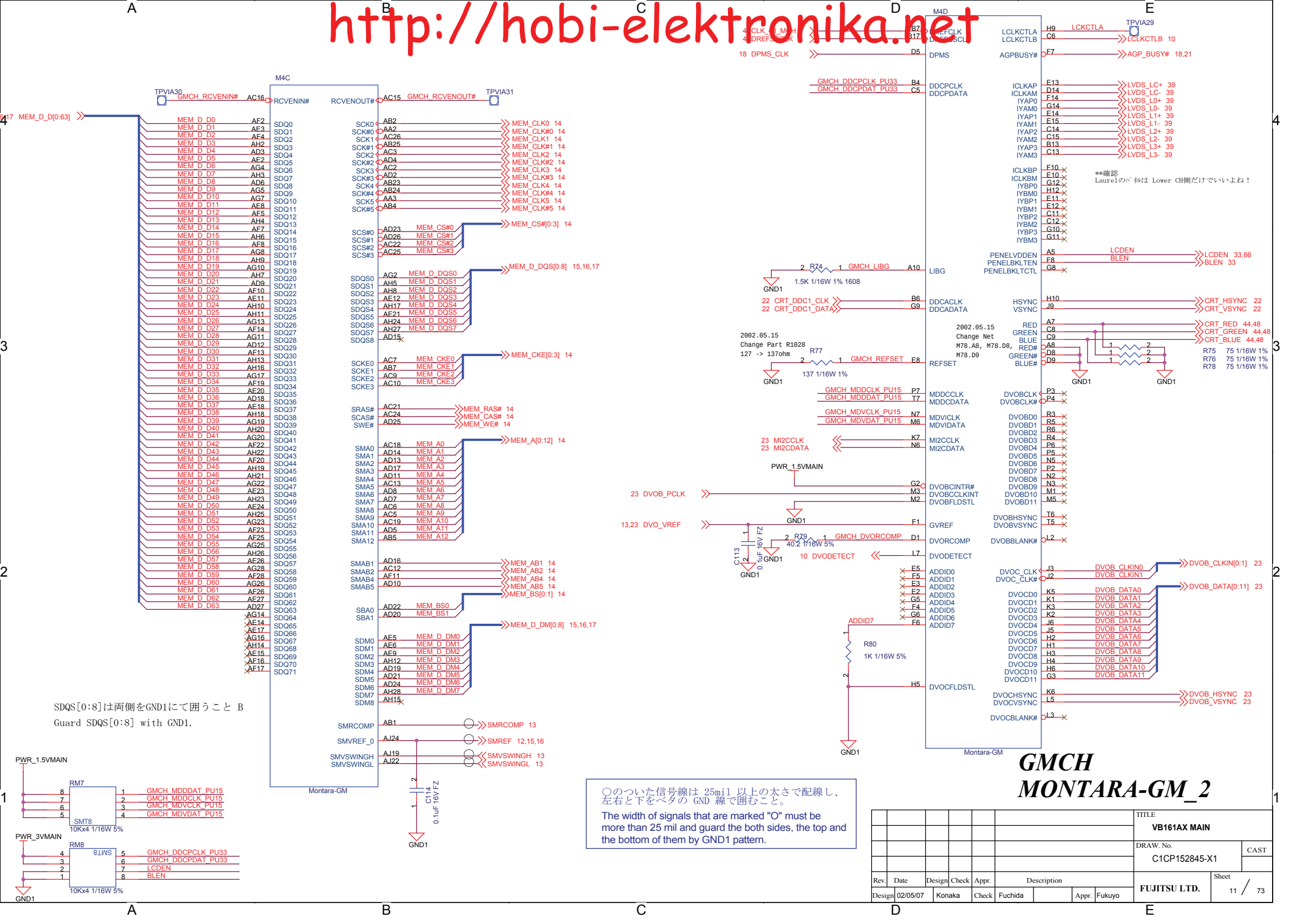

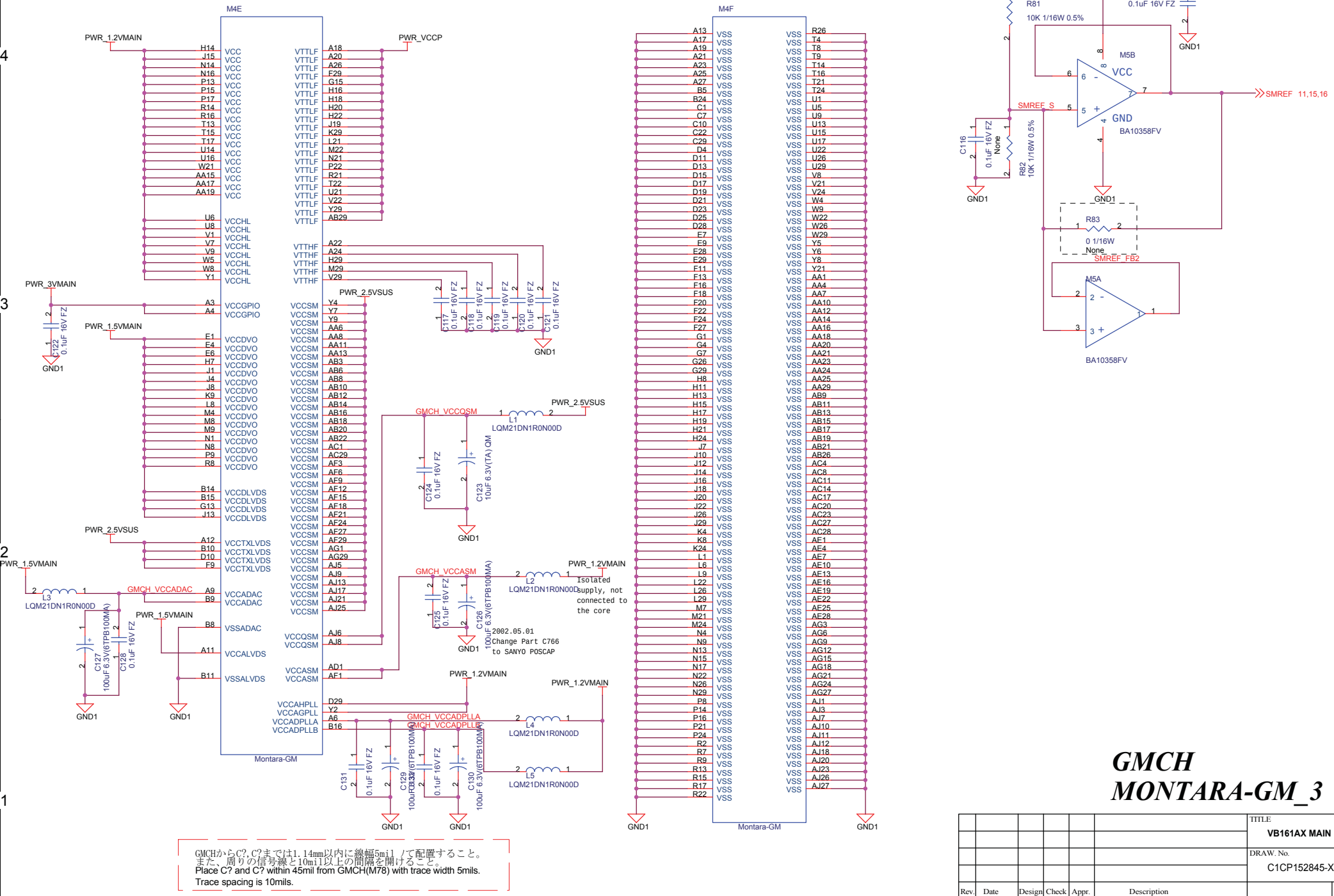

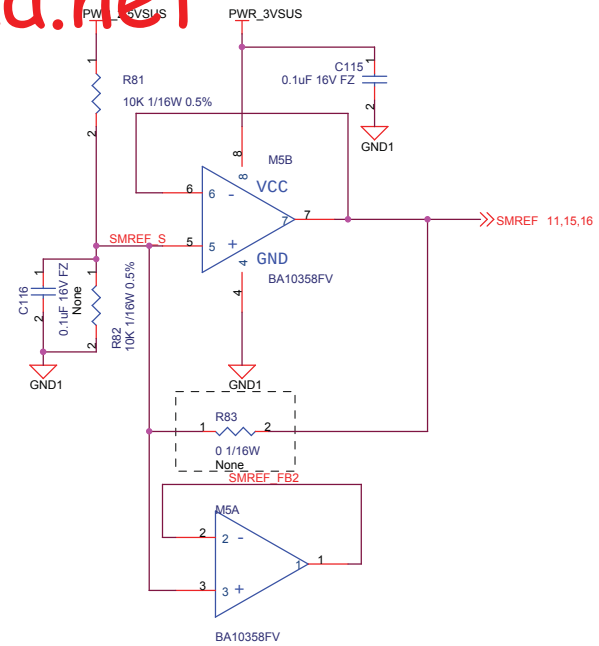

GMCH
MONTARA-GM_3

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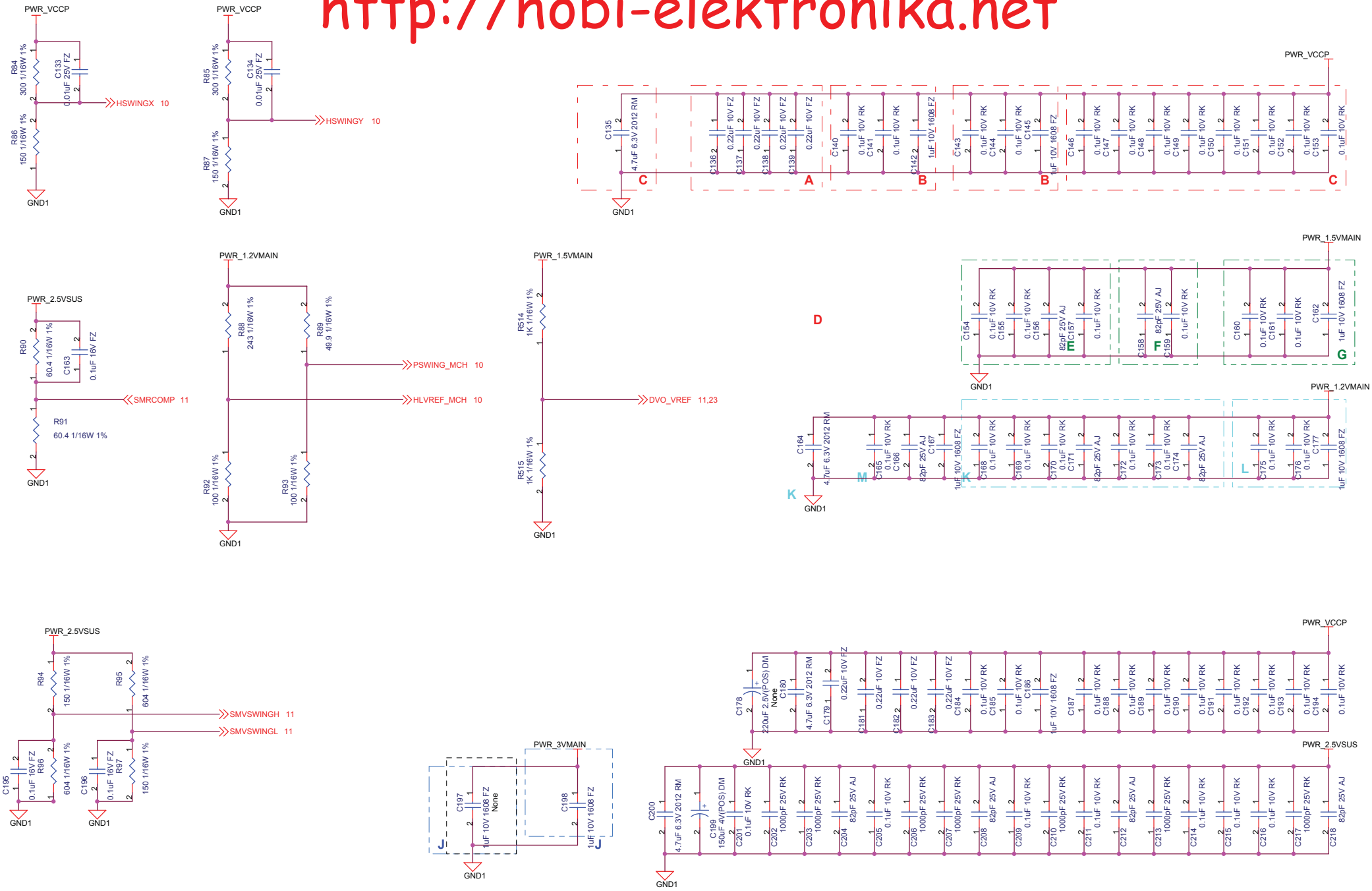

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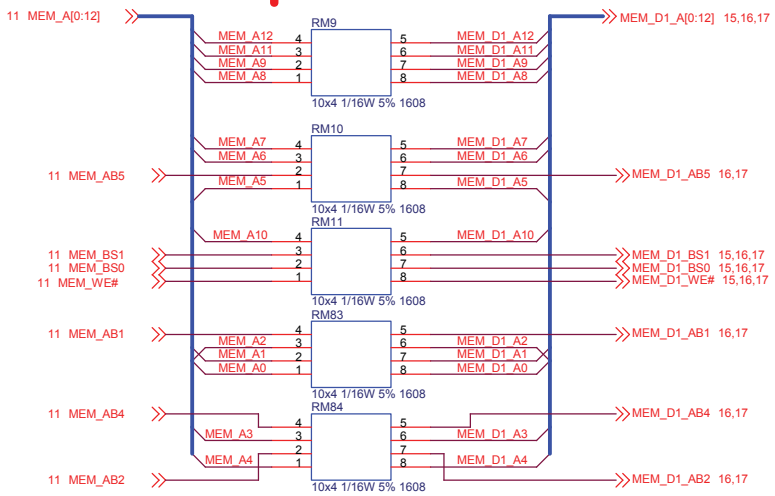

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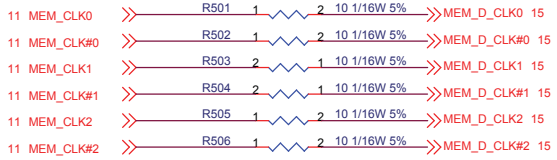

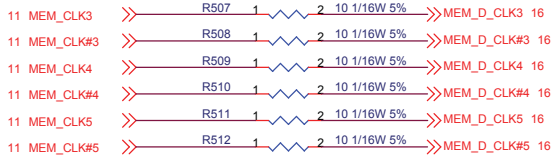

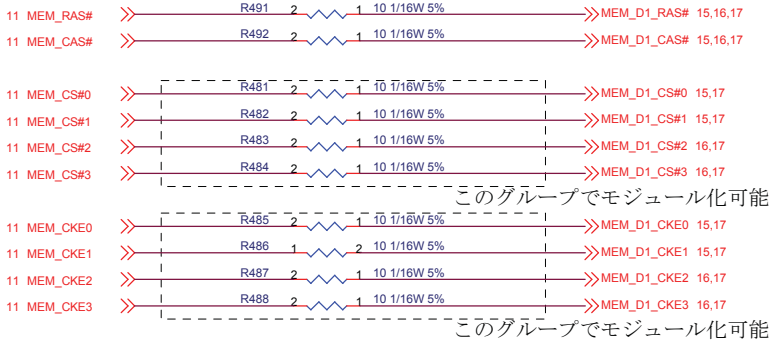

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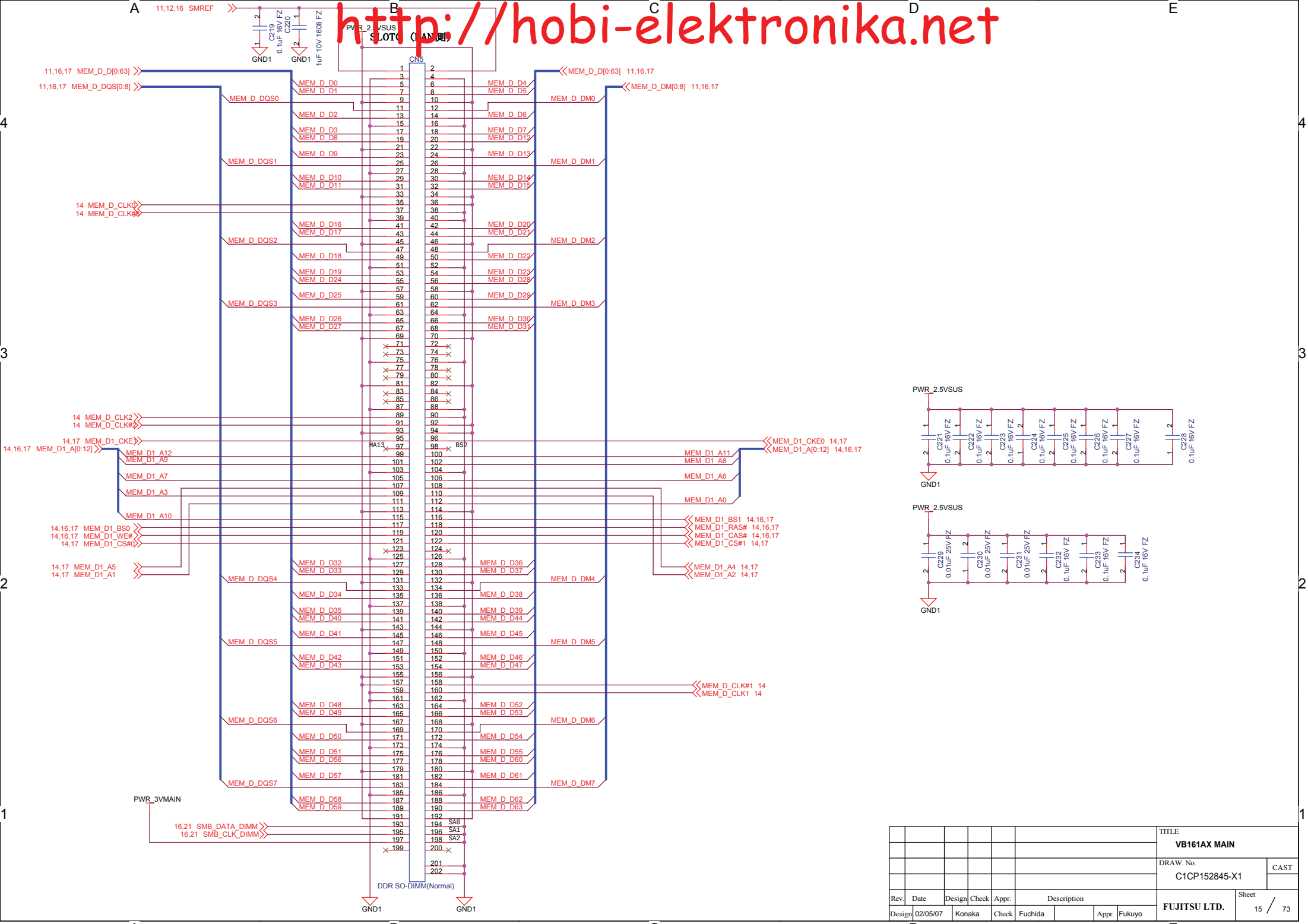

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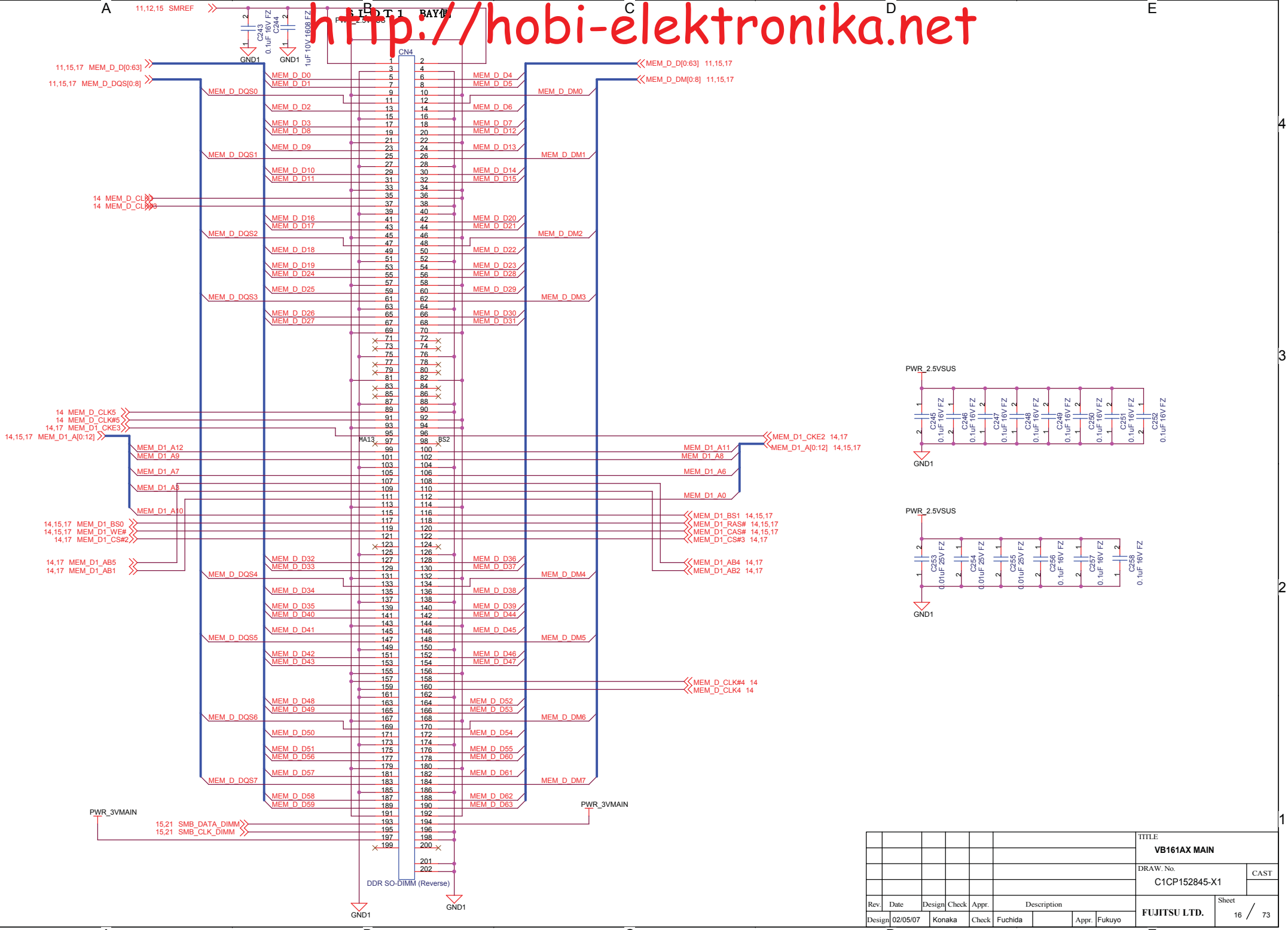

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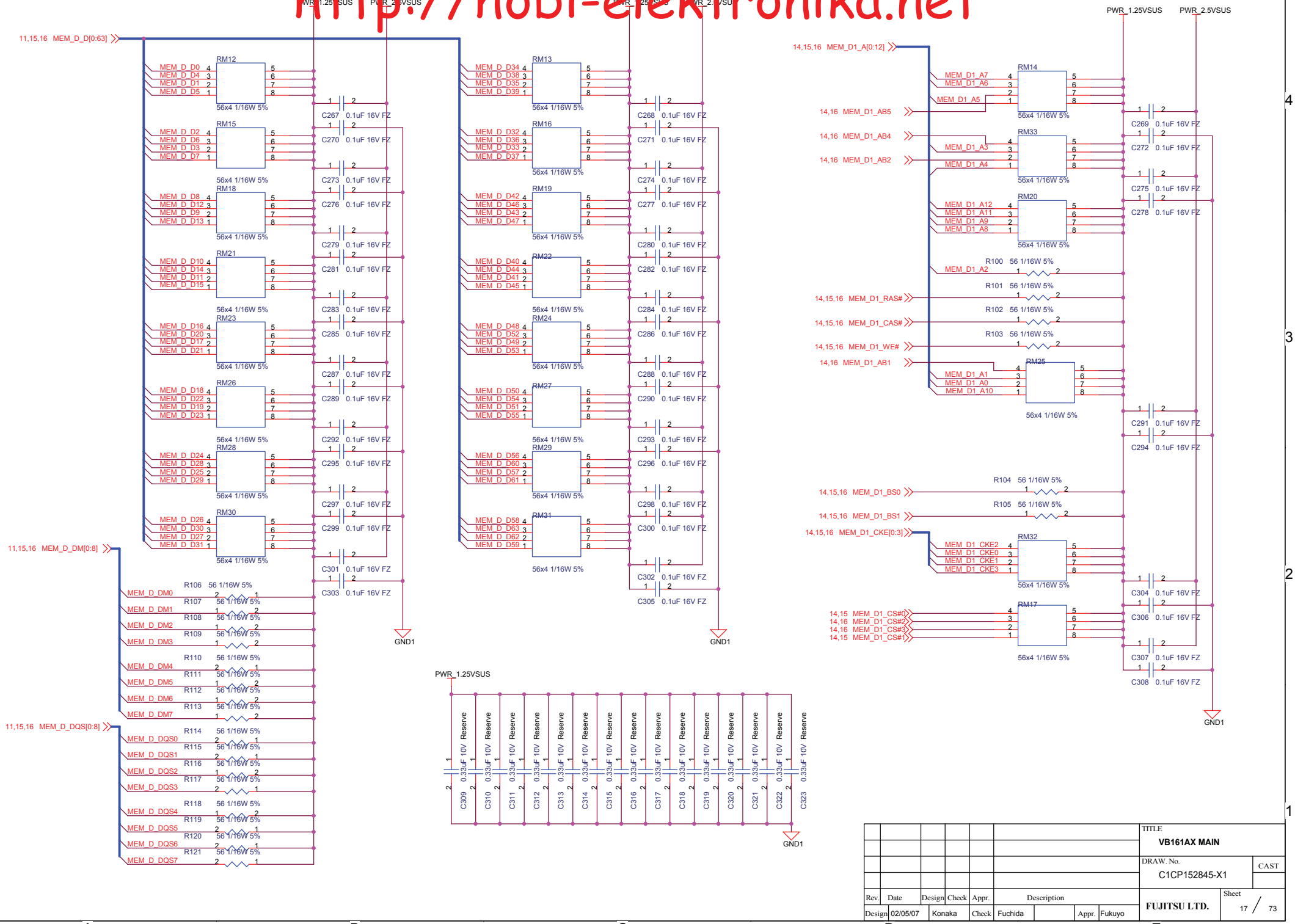

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○の付いた信号線は 20mil 以上の太さで配線し A
左上下をその GND 線で囲うこと
The width of signals that marked "O" must be
more than 25 mil and guard the both sides, the top and
the bottom of them by GND1 pattern.

HLSTRB/HLSTRB# ペアは両側をGND1にて囲うこと
HLSTRB/HLSTRB# pair should be guarded with GND1.

<<CL2の配置について>>
RTCRST#ではデータがクリアできないため、
RTCVCCをGNDに落とす仕様を継続して採用。

<<CL2 arrangement>>
RTCRST# does not clear data in RTC well.
Reset pin is connected to RTCVCC in this
case.

A23:USBBIAS/B23 USBBIAS#は平行伝送路とし、抵抗PAD上で接続すること。

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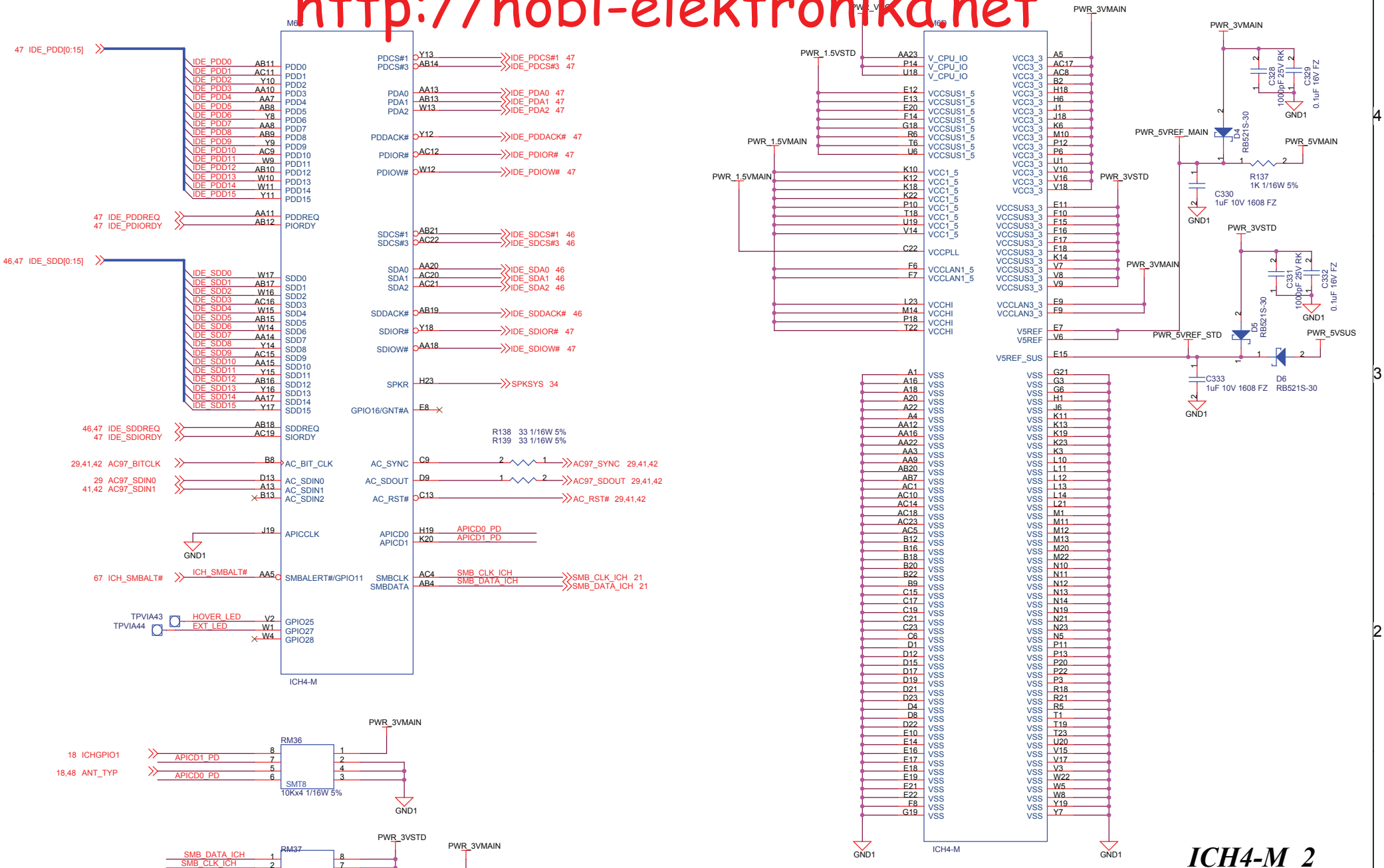

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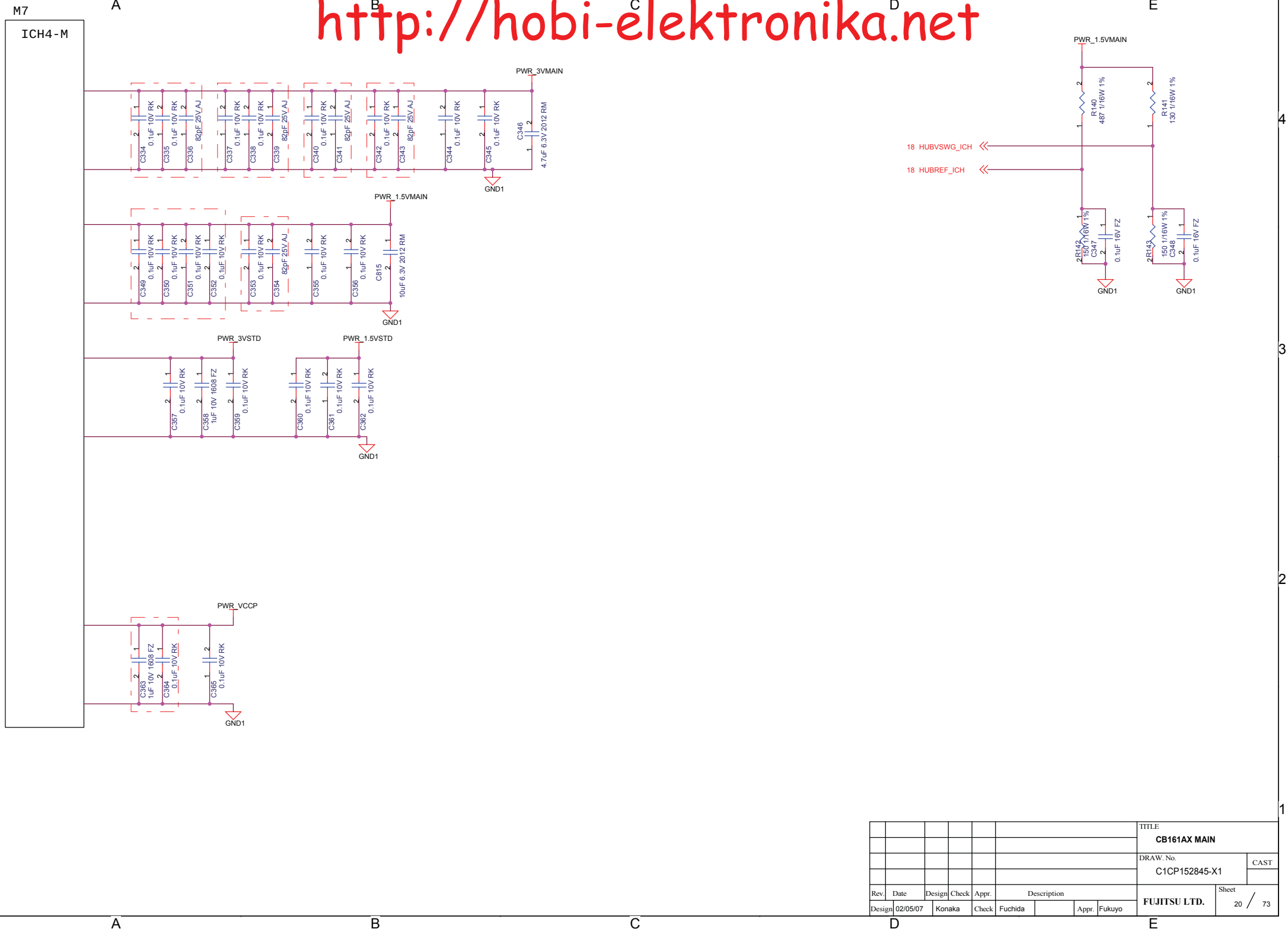

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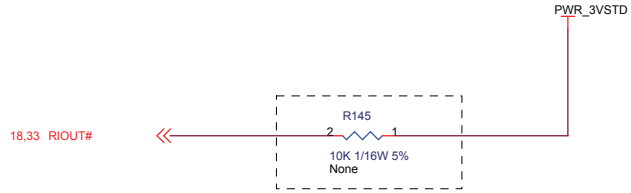

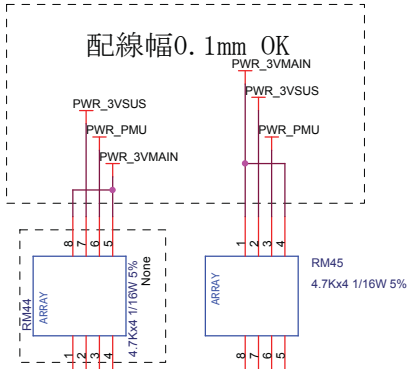

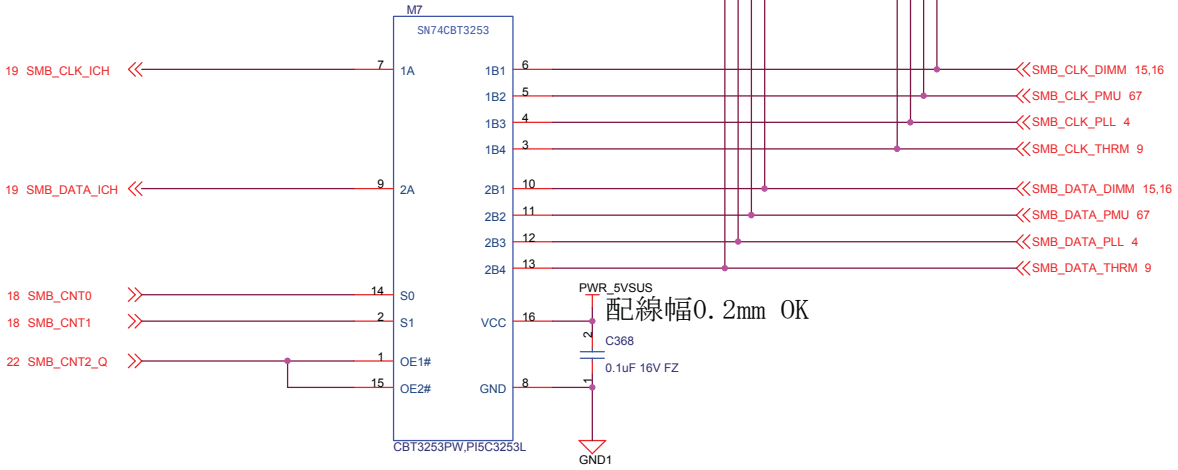

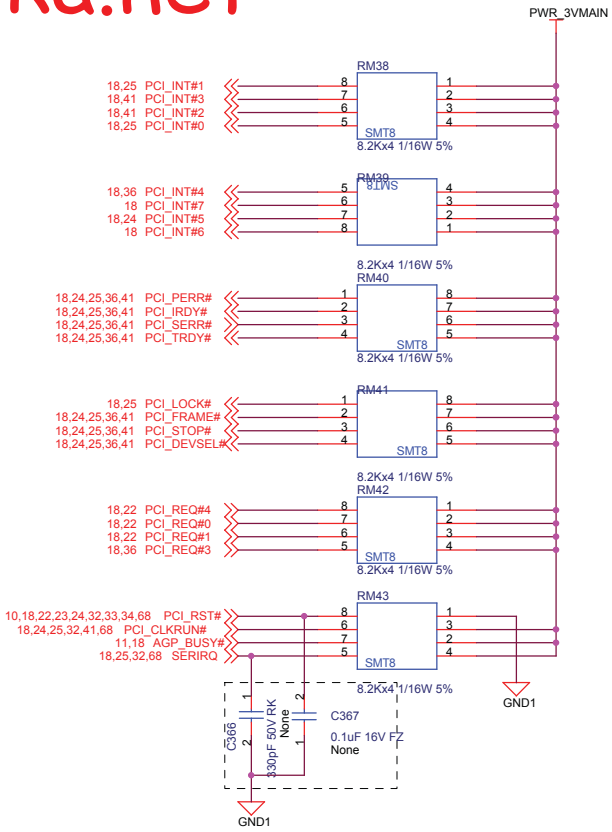

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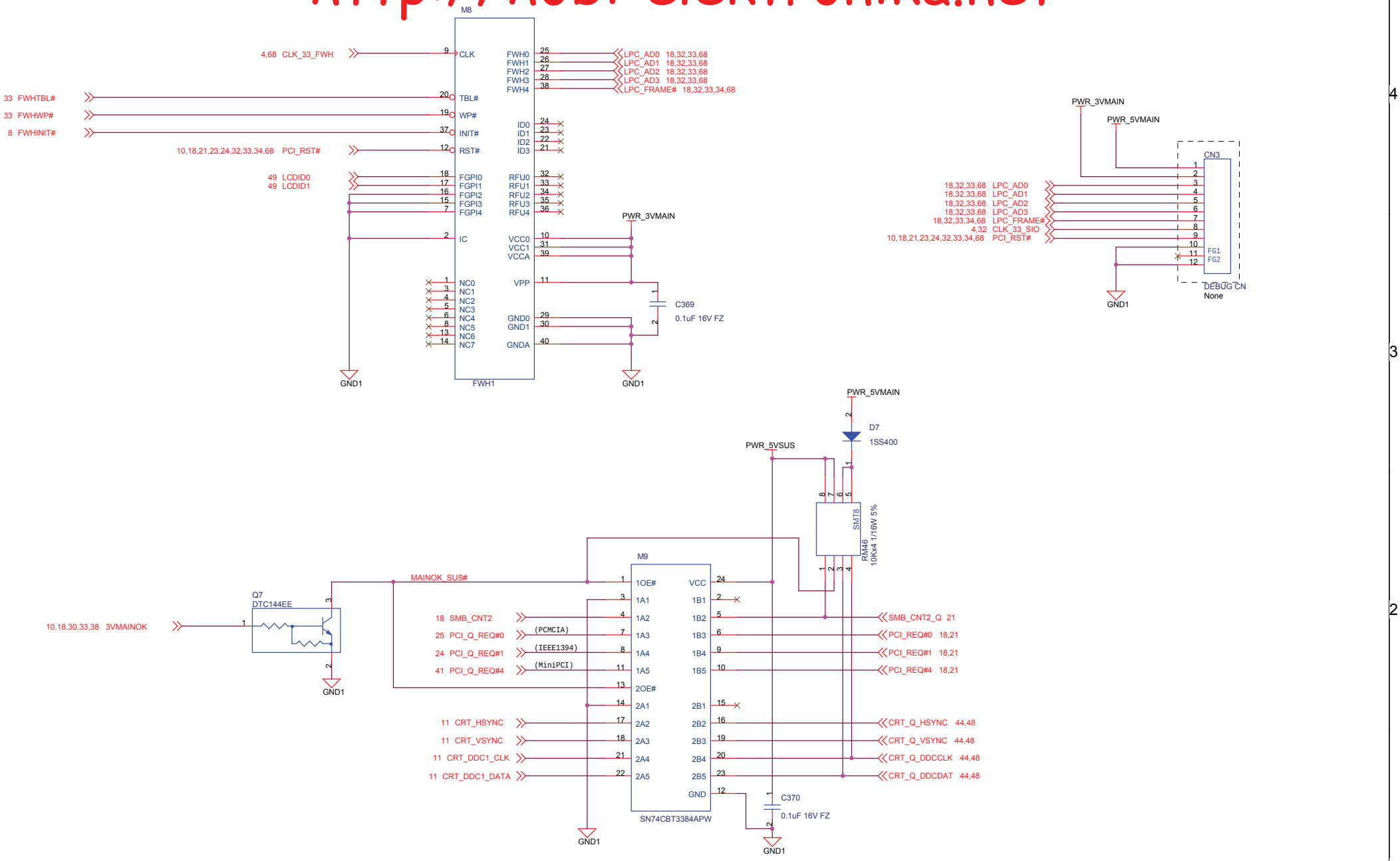

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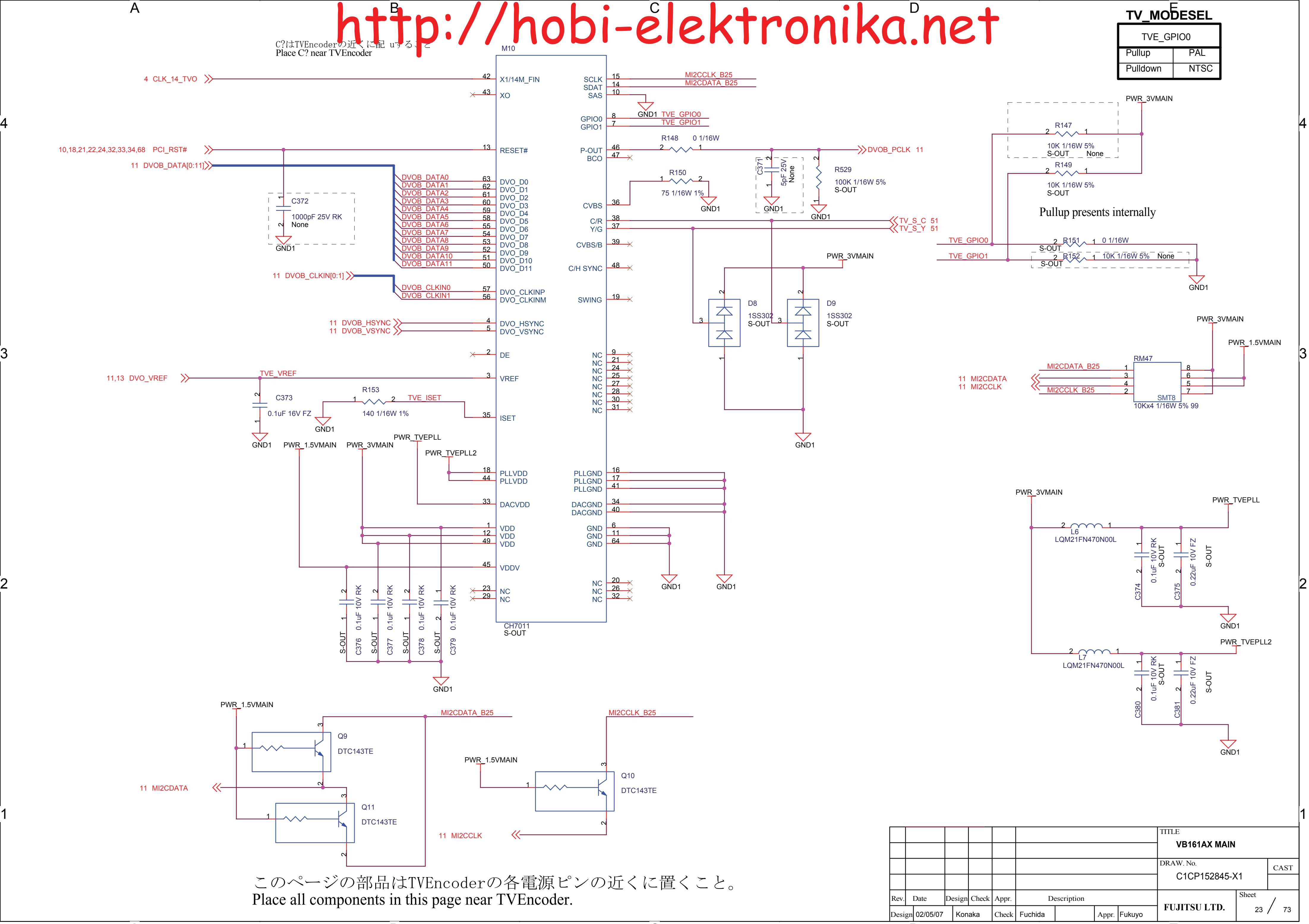
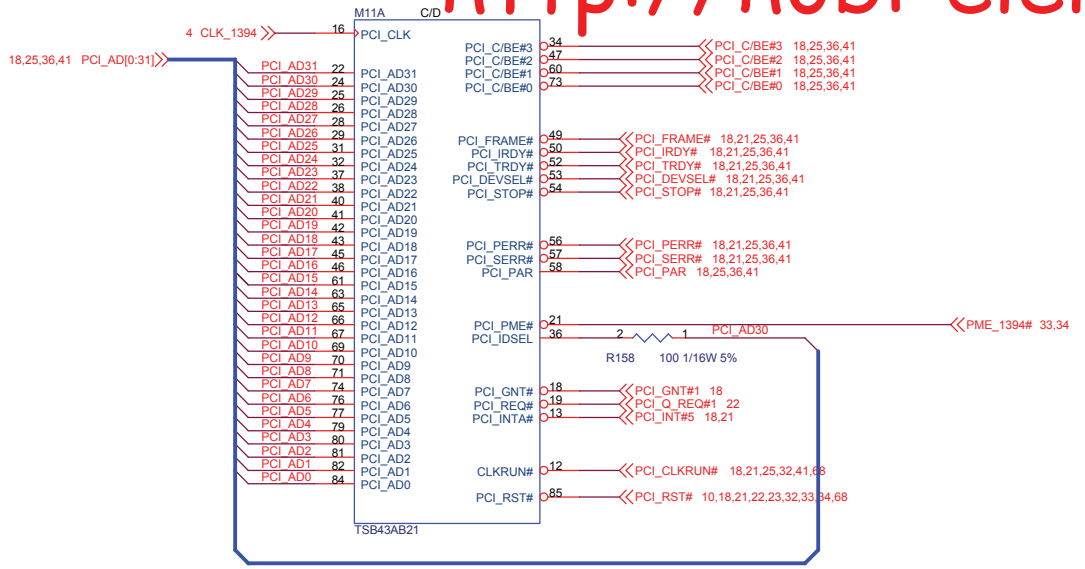
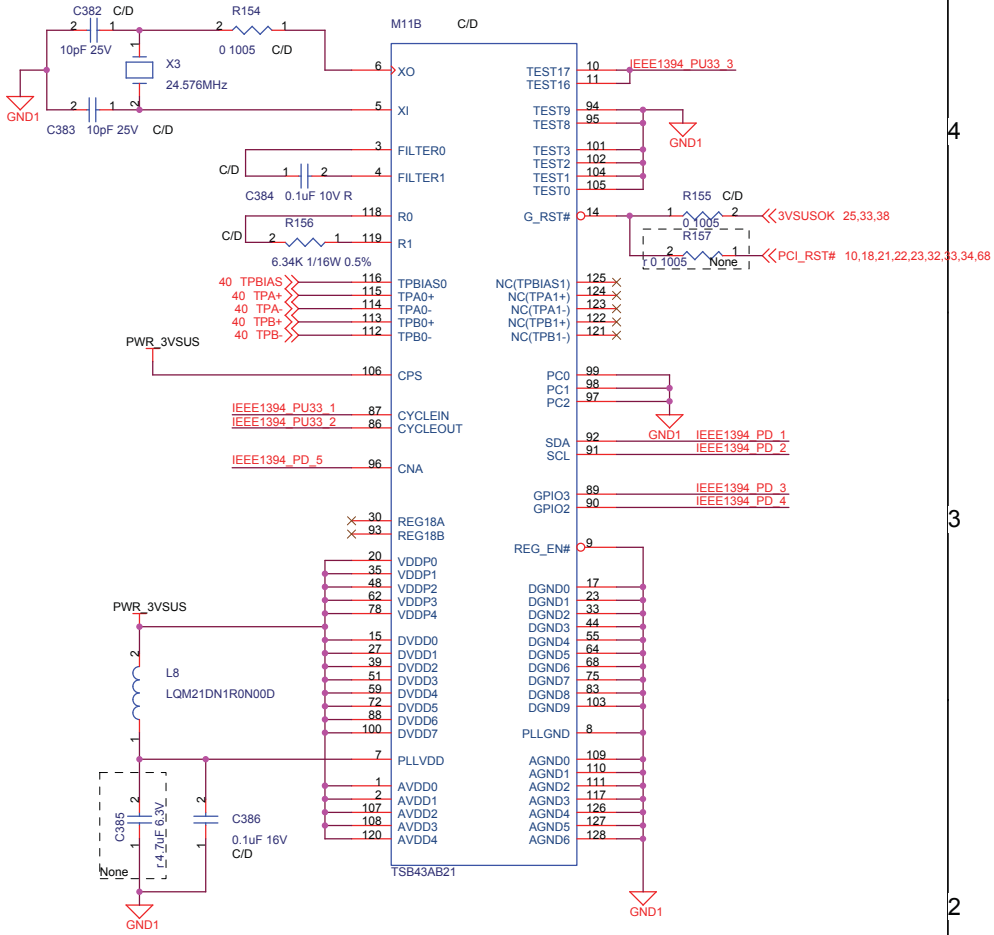
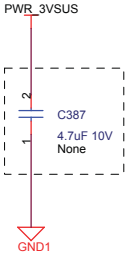
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		


TV_MODESEL
TVE_GPIO0
Pullup PAL
Pulldown NTSC
C?はTVEncoderの近くに配置すること
Place C? near TVEncoder
M10
4 CLK_14_TVO
X1/14M_FIN
XO
SCLK
SDAT
SAS
MI2CCLK_B25
MI2CDATA_B25
GND1
TVE_GPIO0
TVE_GPIO1
GPIO0
GPIO1
10,18,21,22,24,32,33,34,68 PCI_RST#
RESET#
P-OUT
BCO
R148 0 1/16W
DVOB_PCLK 11
11 DVOB_DATA[0:11]
DVOB_DATA0
DVOB_DATA1
DVOB_DATA2
DVOB_DATA3
DVOB_DATA4
DVOB_DATA5
DVOB_DATA6
DVOB_DATA7
DVOB_DATA8
DVOB_DATA9
DVOB_DATA10
DVOB_DATA11
DVO_D0
DVO_D1
DVO_D2
DVO_D3
DVO_D4
DVO_D5
DVO_D6
DVO_D7
DVO_D8
DVO_D9
DVO_D10
DVO_D11
C372
1000pF 25V RK
None
R150
75 1/16W 1%
C371
5pF 25V
None
R529
100K 1/16W 5%
S-OUT
CVBS
C/R
Y/G
CVBS/B
C/H SYNC
SWING
TV_S_C 51
TV_S_Y 51
PWR_3VMAIN
R147
10K 1/16W 5%
S-OUT None
R149
10K 1/16W 5%
S-OUT
Pullup presents internally
TVE_GPIO0
TVE_GPIO1
R151 0 1/16W
R152 10K 1/16W 5% None
11 DVOB_CLKIN[0:1]
DVOB_CLKIN0
DVOB_CLKIN1
DVO_CLKINP
DVO_CLKINM
D8
1SS302
S-OUT
D9
1SS302
S-OUT
11 DVOB_HSYNC
11 DVOB_VSYNC
DVO_HSYNC
DVO_VSYNC
DE
NC
PWR_1.5VMAIN
RM47
MI2CDATA_B25
MI2CCLK_B25
11 MI2CDATA
11 MI2CCLK
SMT8
10Kx4 1/16W 5% 99
11,13 DVO_VREF
TVE_VREF
VREF
C373
0.1uF 16V FZ
R153
140 1/16W 1%
TVE_ISET
ISET
PWR_TVEPLL
PWR_TVEPLL2
PLLVDD
PLLGND
DACVDD
DACGND
VDD
GND
VDDV
C376
C377
C378
C379
0.1uF 10V RK
S-OUT
CH7011
S-OUT
PWR_3VMAIN
PWR_TVEPLL
L6
LQM21FN470N00L
C374
0.1uF 10V RK
C375
0.22uF 10V FZ
S-OUT
PWR_TVEPLL2
L7
LQM21FN470N00L
C380
0.1uF 10V RK
C381
0.22uF 10V FZ
PWR_1.5VMAIN
Q9
DTC143TE
MI2CDATA_B25
11 MI2CDATA
Q11
DTC143TE
Q10
DTC143TE
MI2CCLK_B25
11 MI2CCLK
このページの部品はTVEncoderの各電源ピンの近くに置くこと。
Place all components in this page near TVEncoder.

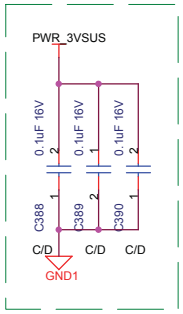
TITLE	VB161AX MAIN				
DRAW. No.	C1CP152845-X1	CAST			
Rev.	Date	Design	Check	Appr.	Description
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo
FUJITSU LTD.	Sheet 23 / 73				



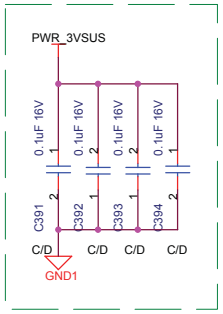




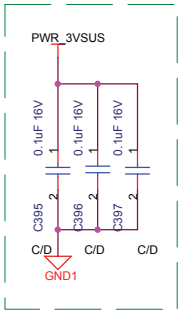
下記のコンデンサはTSB43AA21の
VDDPxピン近傍に配置

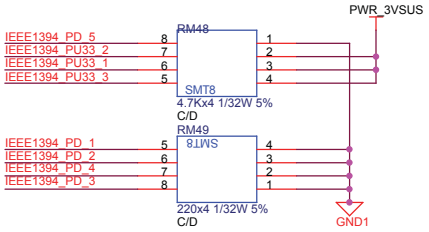


下記のコンデンサはTSB43AA21の
AVDDxピン近傍に配置



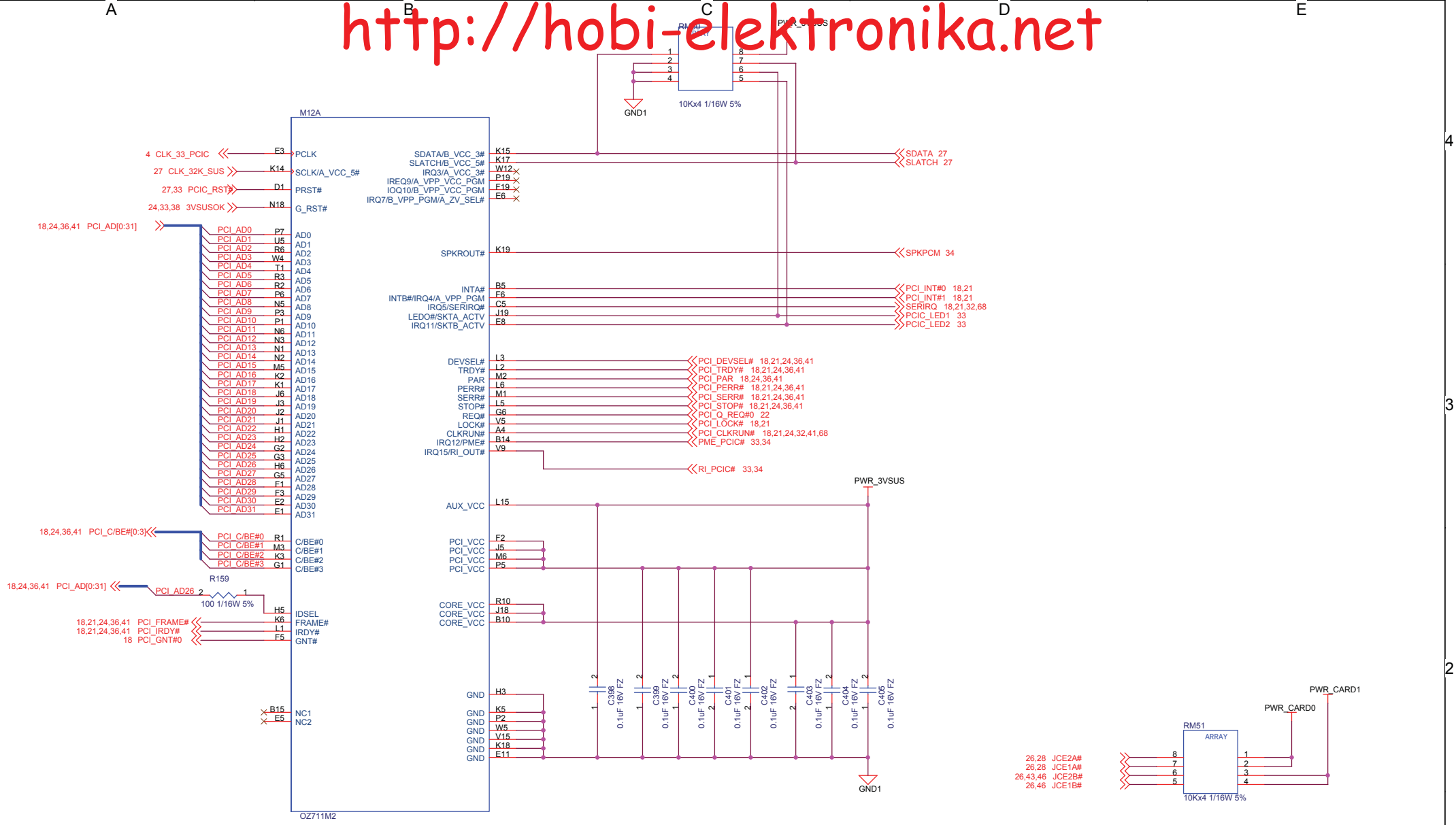
下記のコンデンサはTSB43AA21の
DVDDxピン近傍に配置





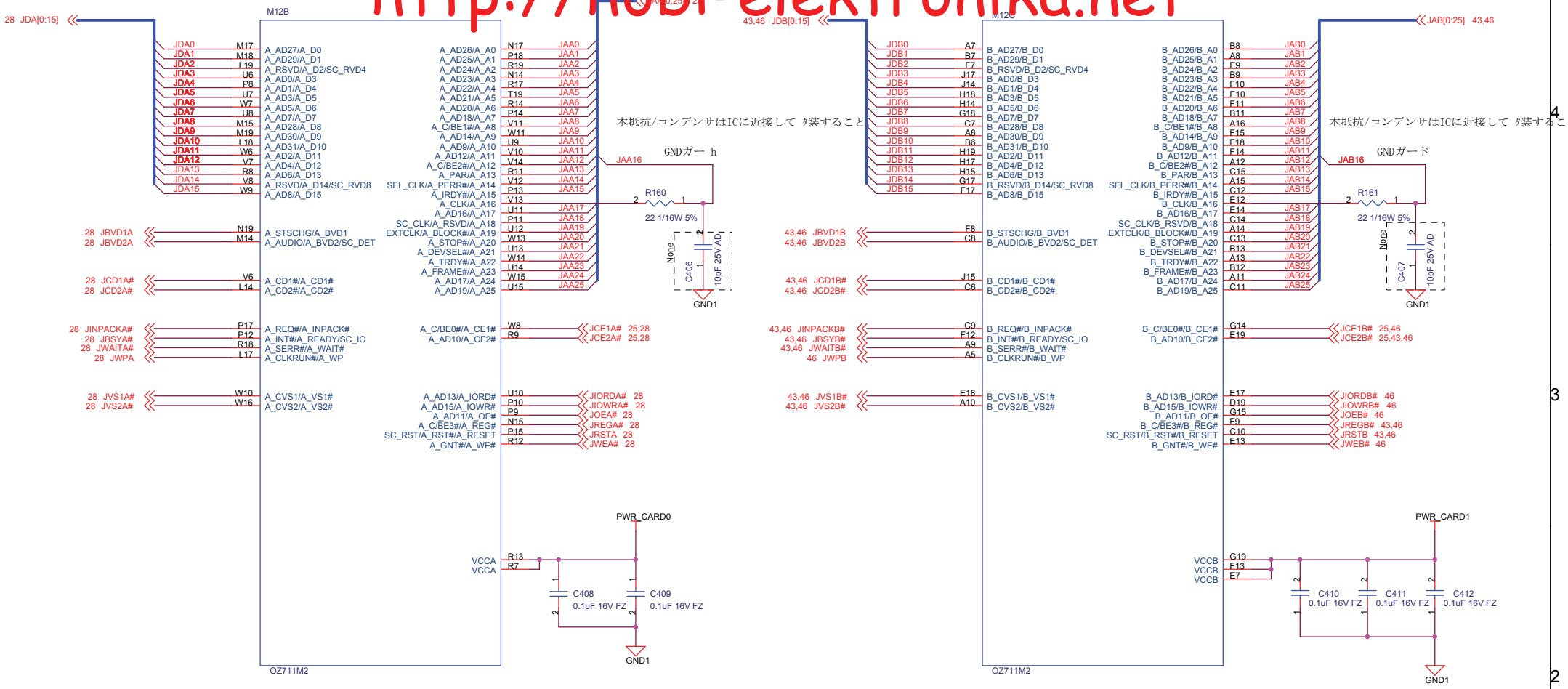
IEEE1394

								TITLE	VB161AX MAIN
								DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet 24 / 73
Design	02/05/07	Konaka	Check	Fuchida		Appr.	Fukuyo		

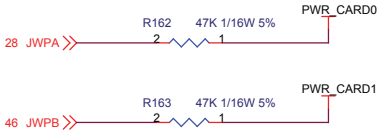


PCIC-1[O2Micro-Tarzan]

						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 25 / 73
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		

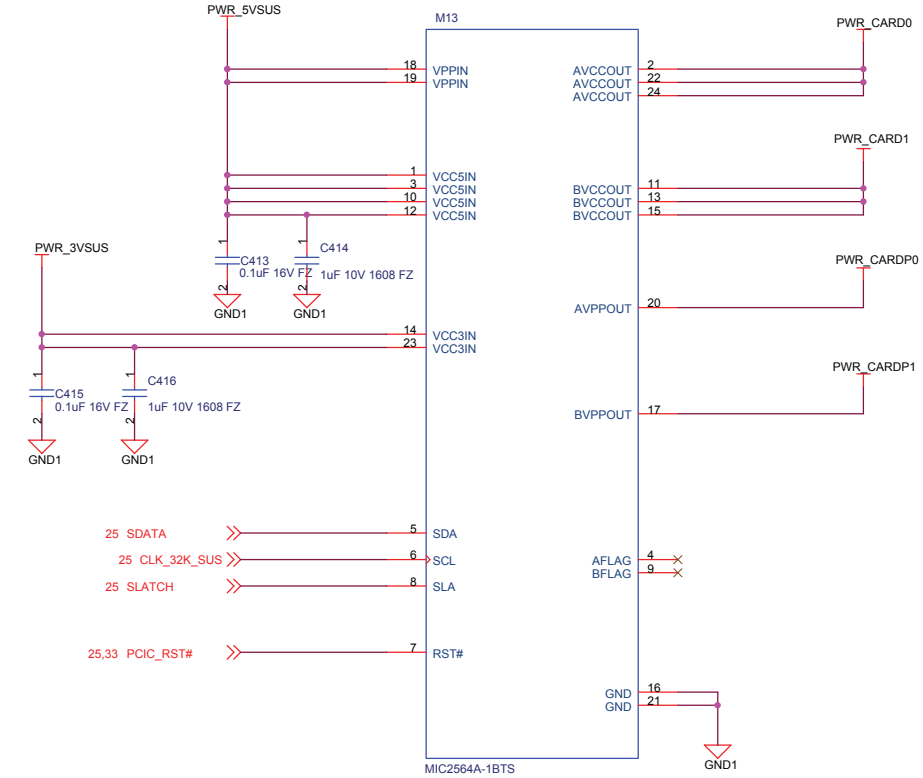


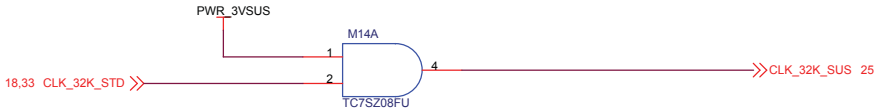
【注意 z
JAA16, JAB16はCardBus時クロック信号になるのでGND1にてガードを行うこと。

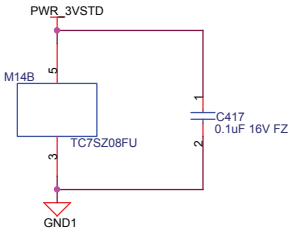


PCIC-2[O2Micro-Tarzan]

						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description		
Design	02/05/07	Konaka	Check	Fuchida	Appr.	Fukuyo	FUJITSU LTD. Sheet 26 / 73

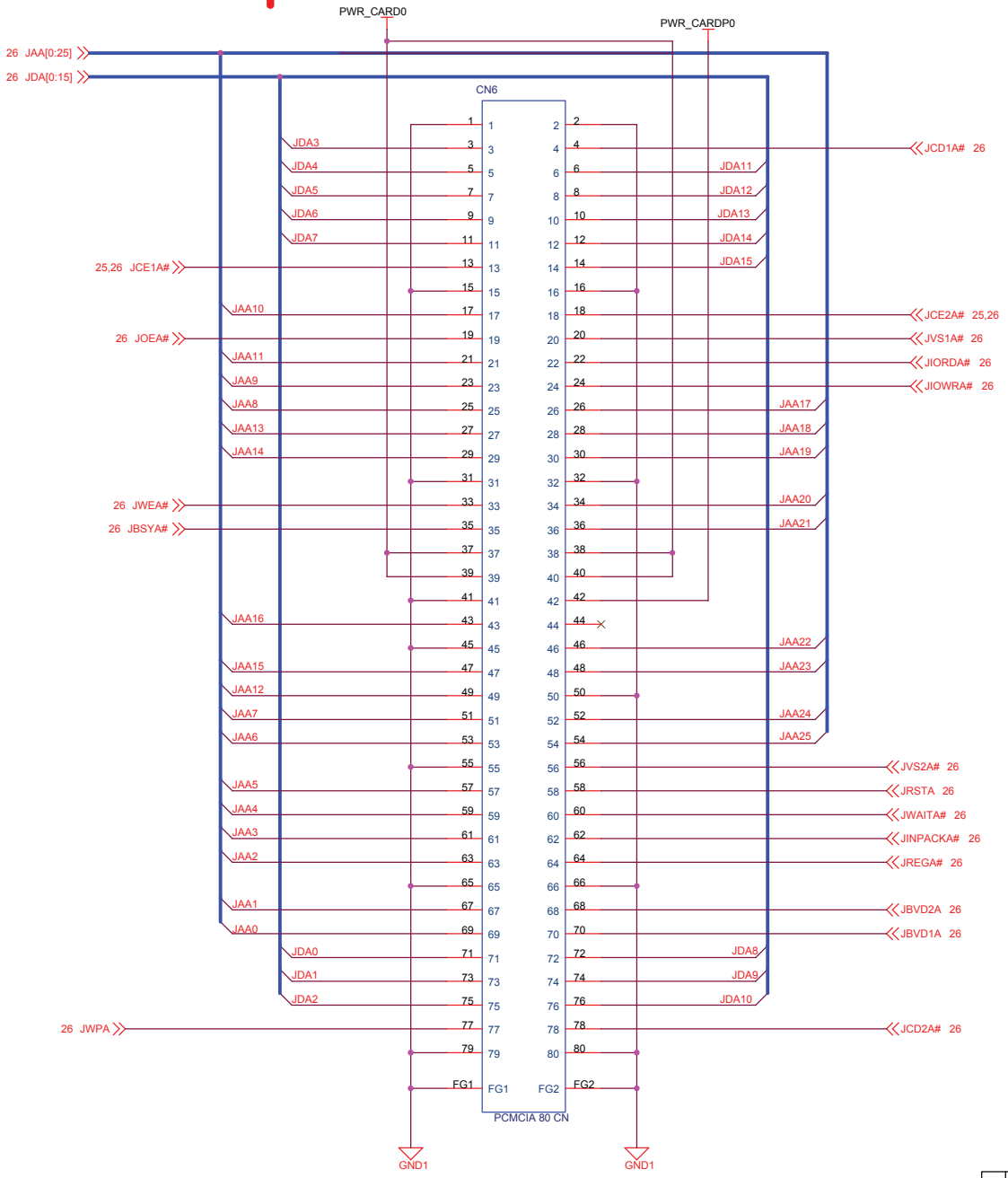




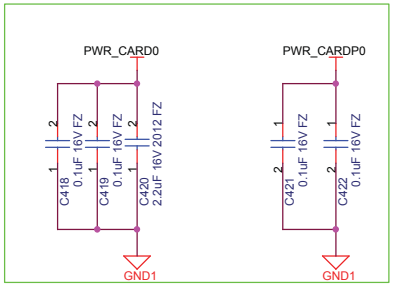


PCIC POW

								TITLE	VB161AX MAIN
								DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet 27 / 73
Design	02/05/07	Konaka	Check	Fuchida		Appr.	Fukuyo		



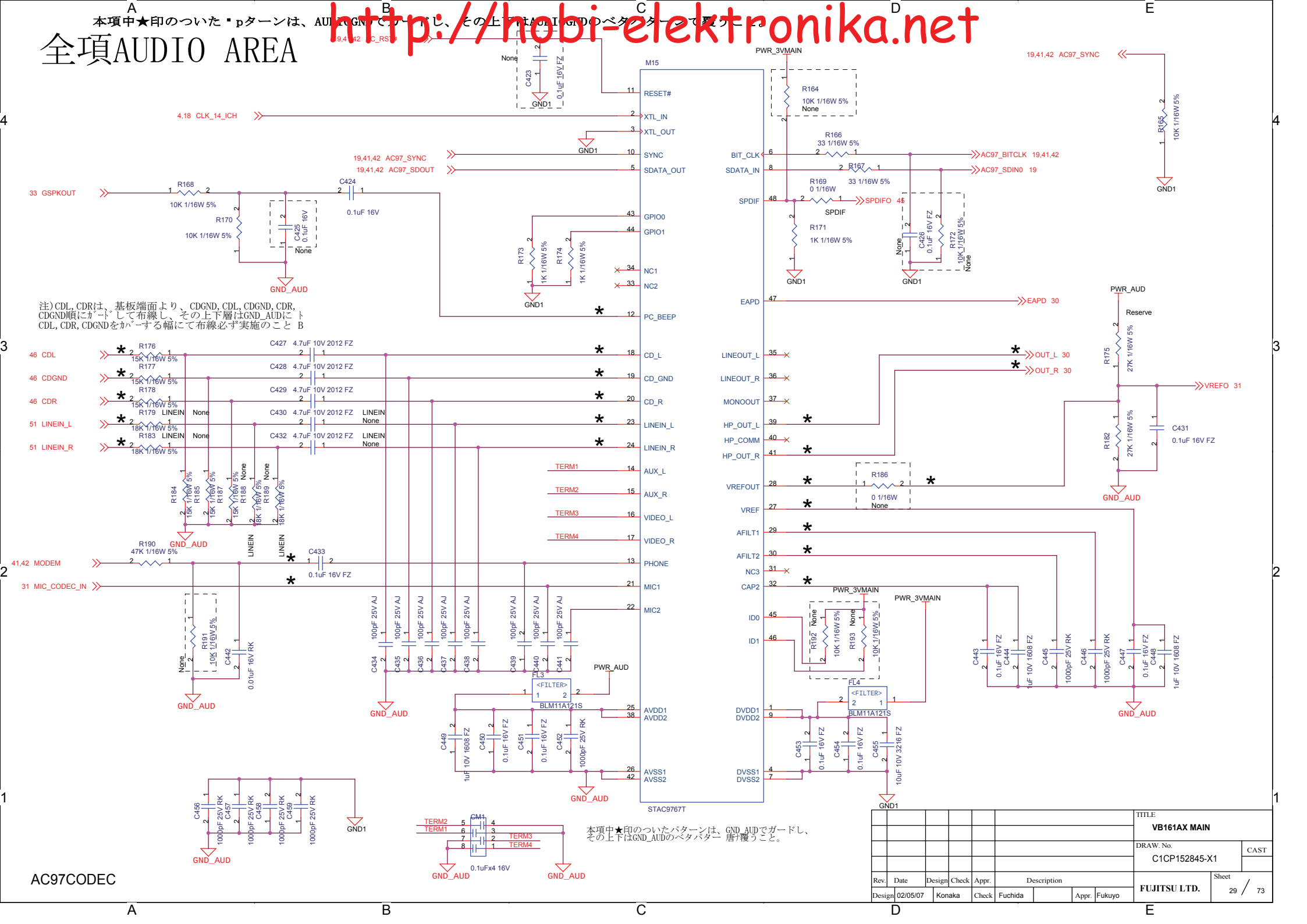
コネクタ電源ピンの近傍に配置



						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description		
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo	FUJITSU LTD.	Sheet 28 / 73

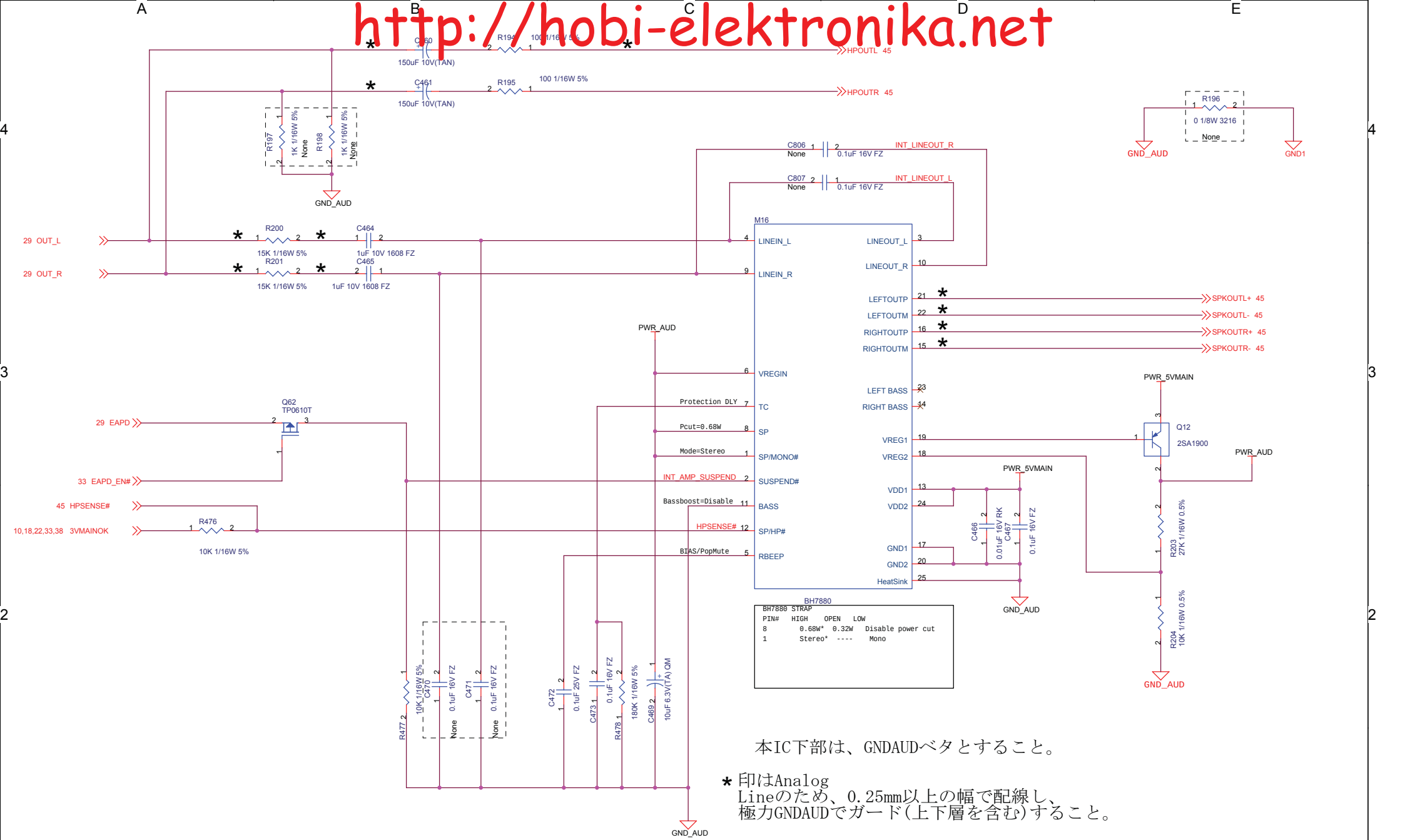
本項中★印のついた・pターンは、AUDIO GNDでガードし、その上下はAUDIO GNDのベタパターンで覆うこと。

全項AUDIO AREA



						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1
							CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 29 / 73
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		

AC97CODEC



本IC下部は、GNDAUDベタとすること。

＊印はAnalog
Lineのため、0.25mm以上の幅で配線し、
極力GNDAUDでガード(上下層を含む)すること。

Rev.	Date	Design	Check	Appr.	Description
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo

TITLE: VB161AX MAIN
DRAW. No.: C1CP152845-X1
CAST
FUJITSU LTD.
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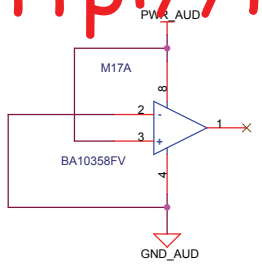

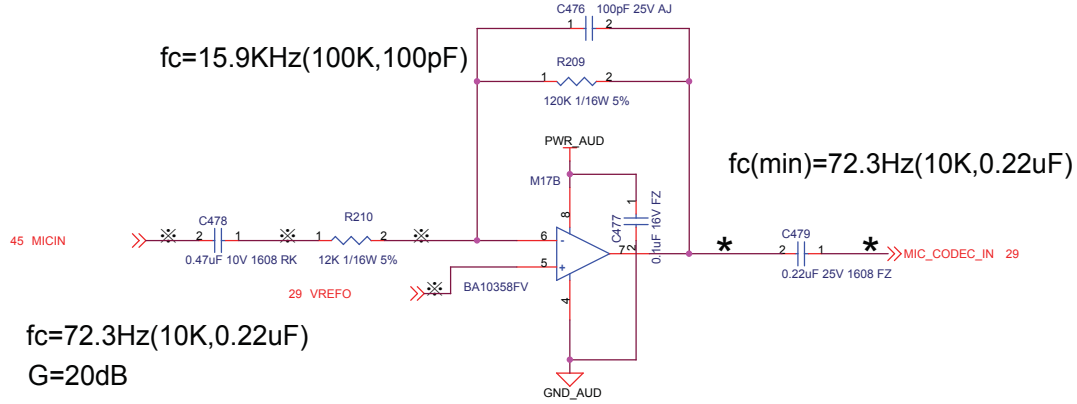

MIC AMP

Rev.	Date	Design	Check	Appr.	Description
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo

TITLE: VB161AX MAIN

DRAW. No.: C1CP152845-X1 CAST

FUJITSU LTD.

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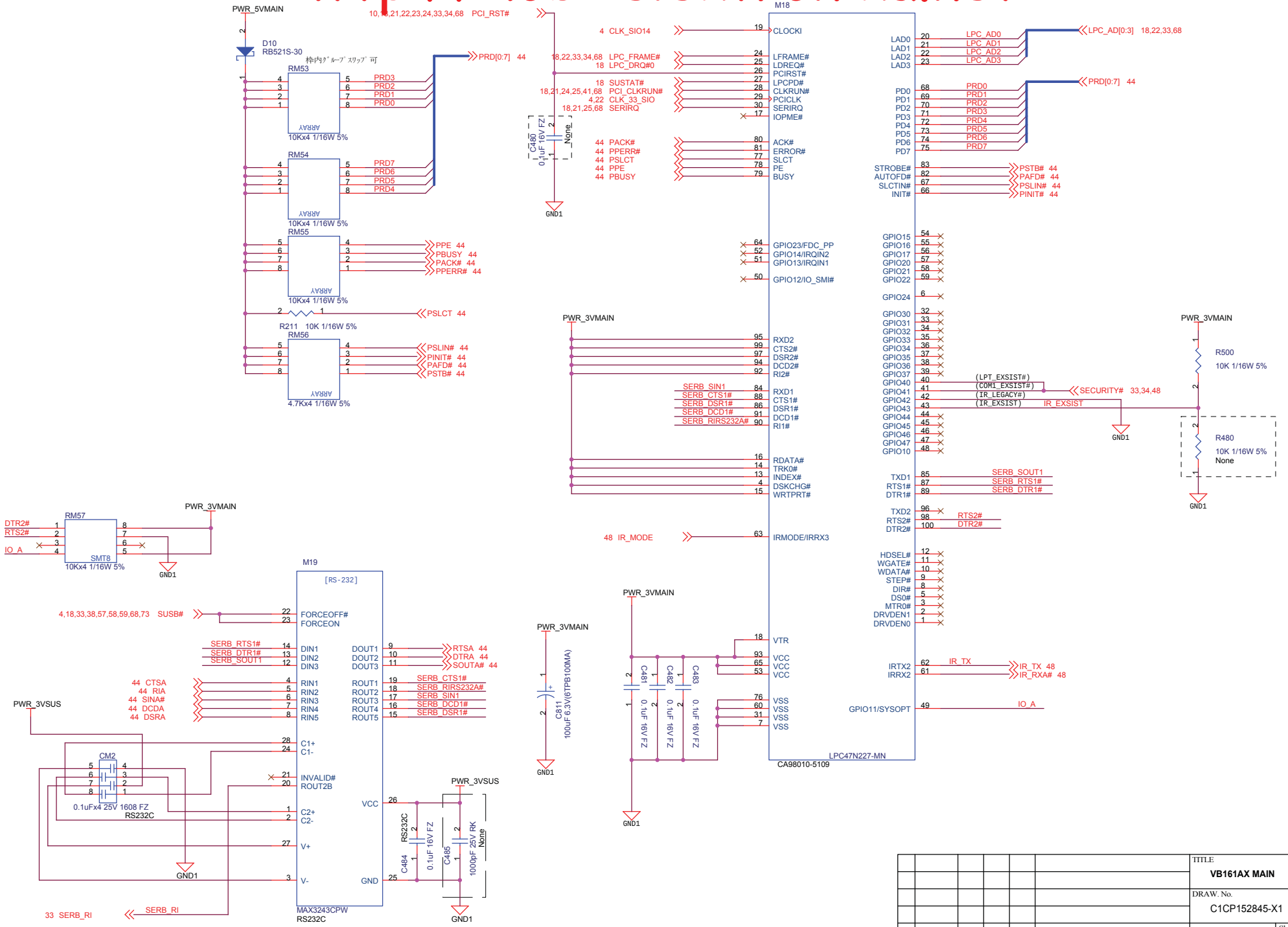
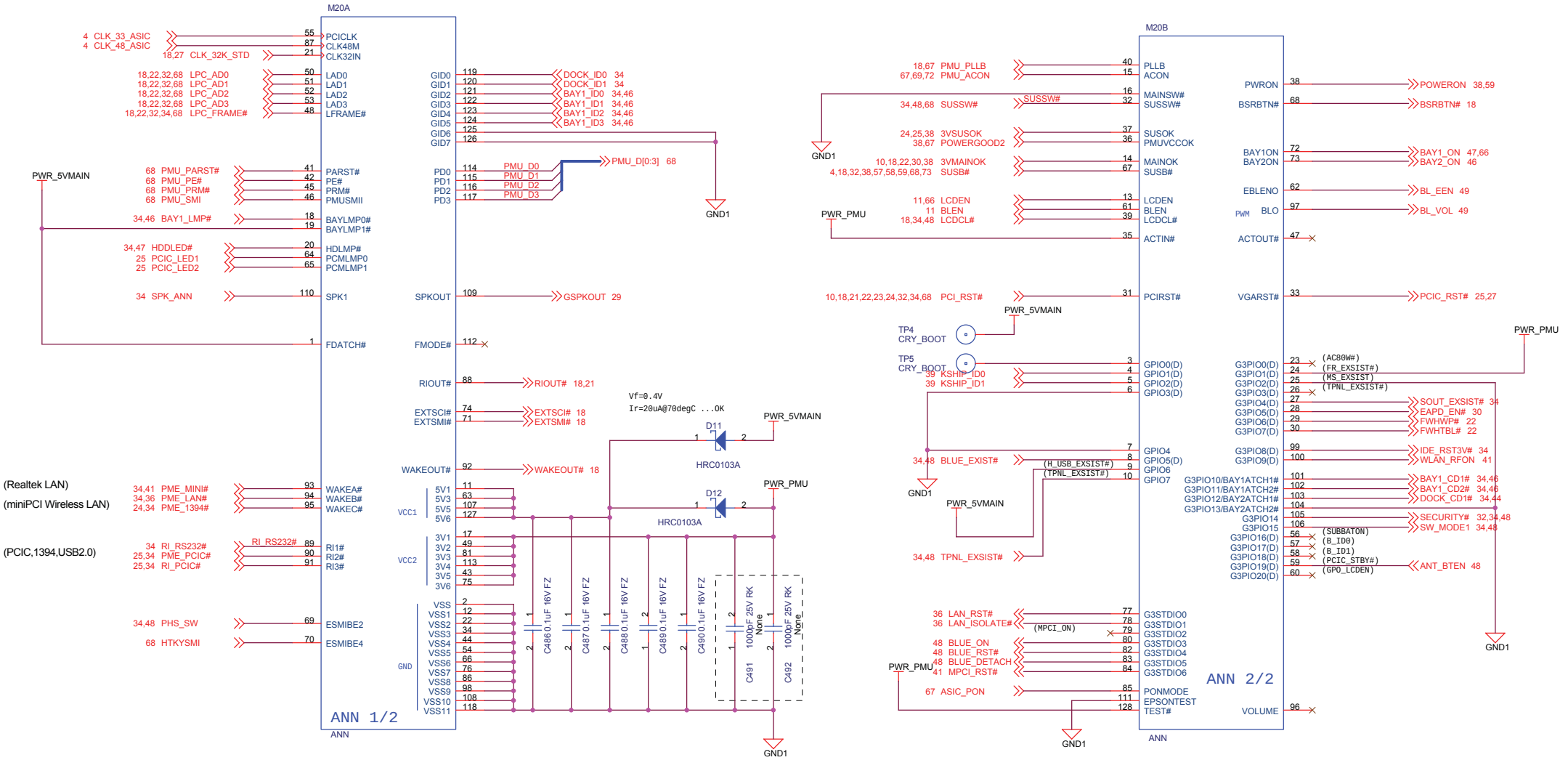
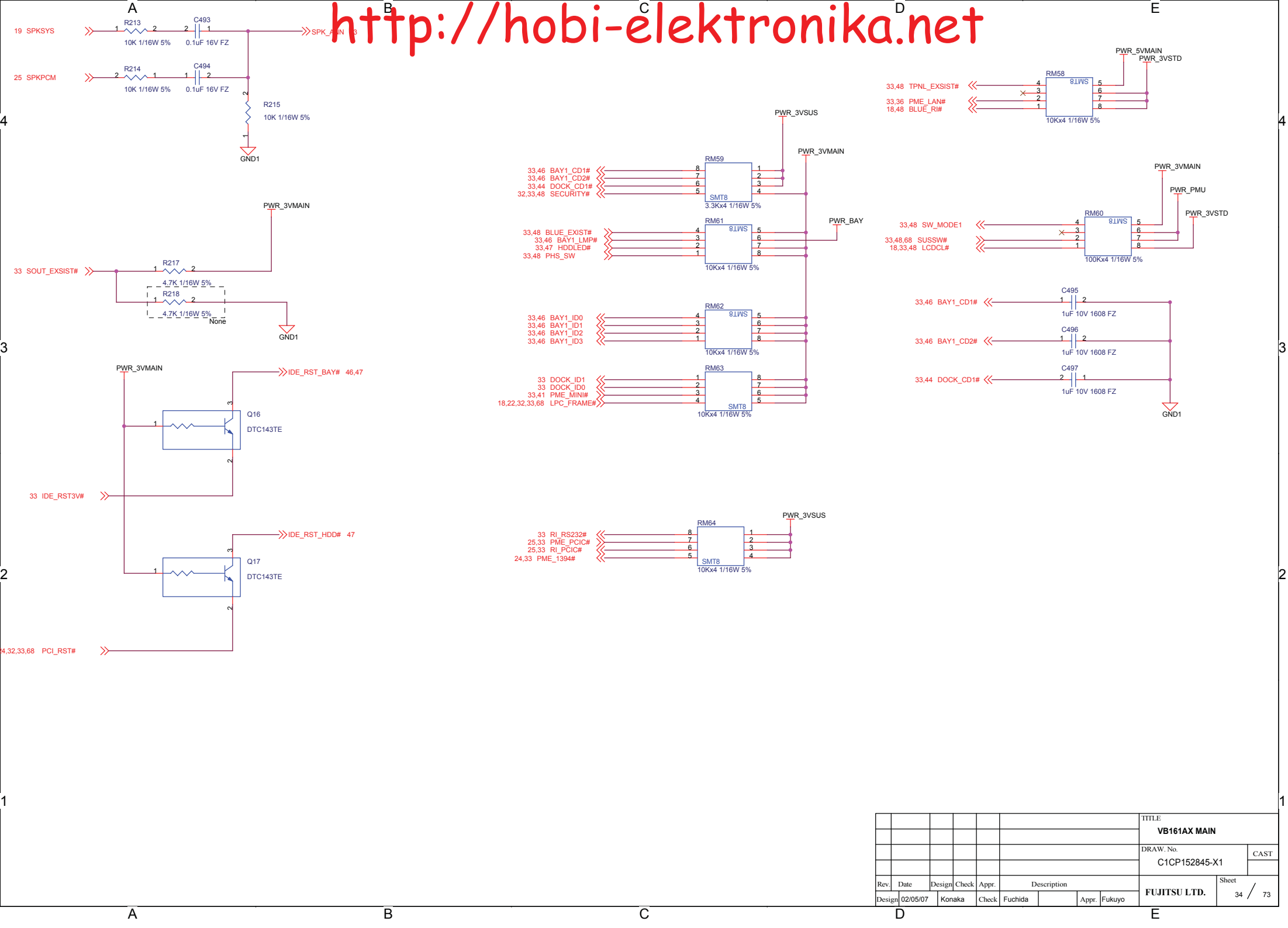


							TITLE	VB161AX MAIN
							DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description			
Design	02/05/07	Konaka	Check	Fuchida		Appr. Fukuyo	FUJITSU LTD.	Sheet 32 / 73

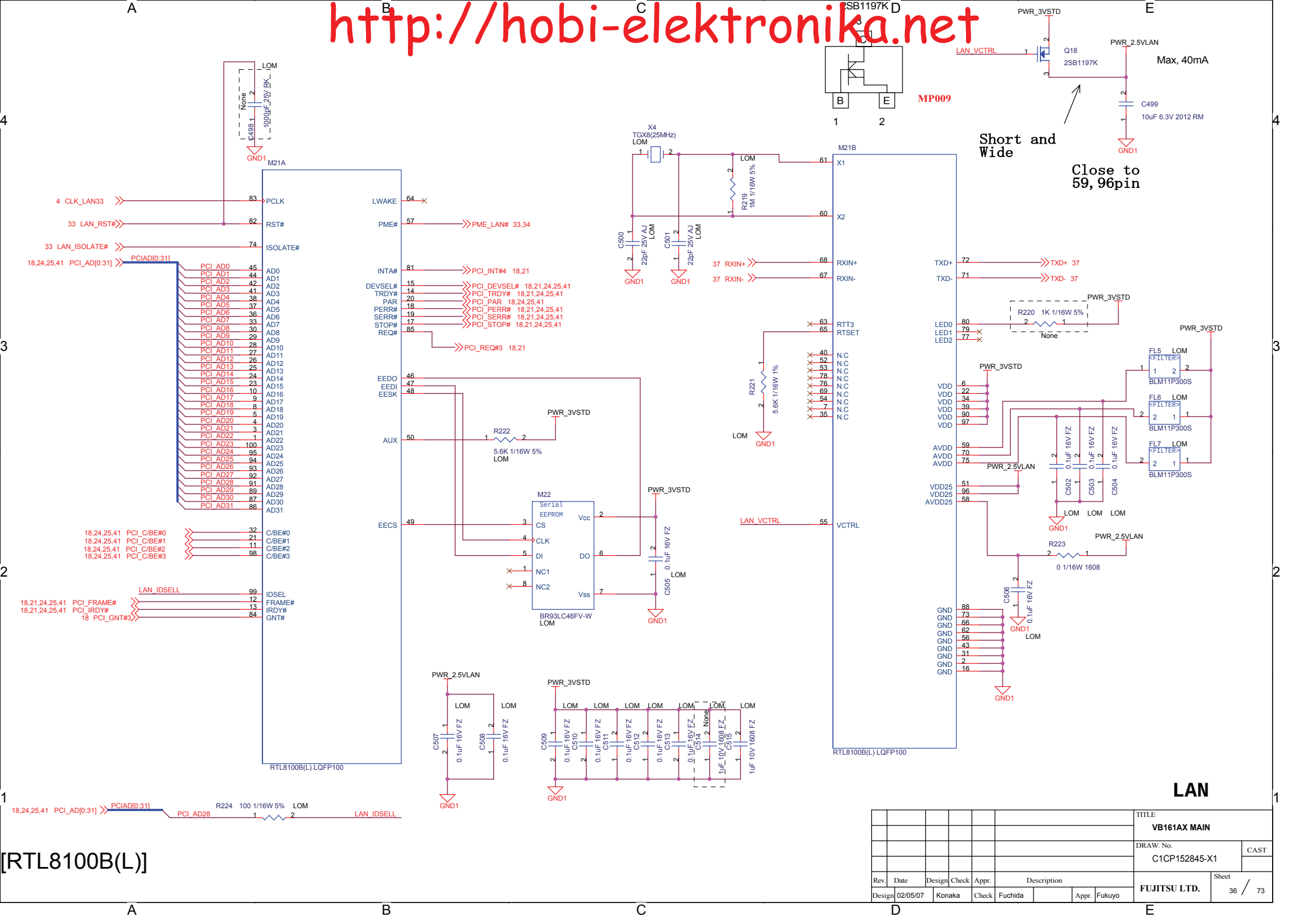


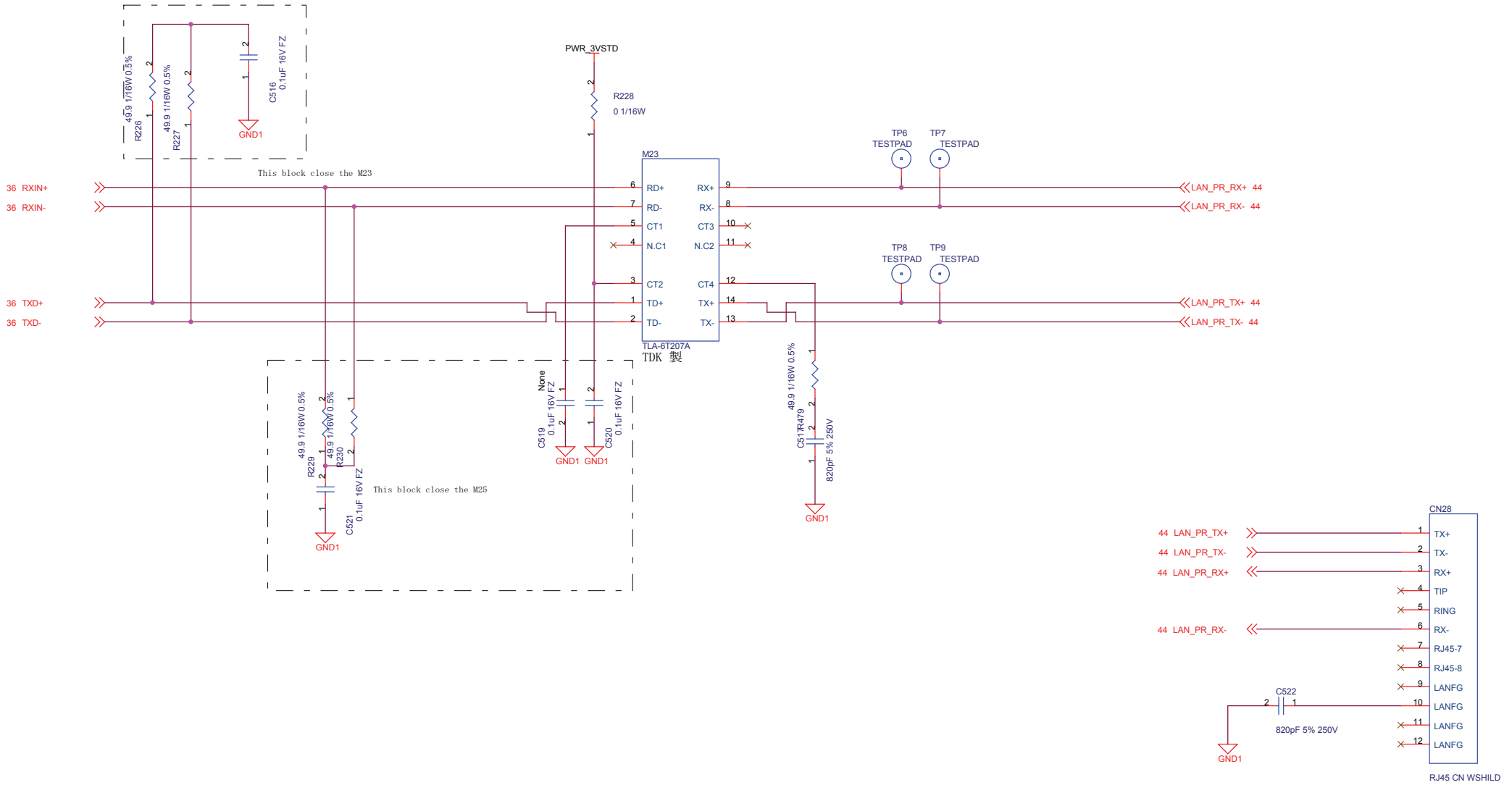
[ASIC ANN]

						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1
							CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 33 / 73
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		

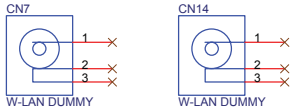


						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description		
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo	FUJITSU LTD.	Sheet 34 / 73



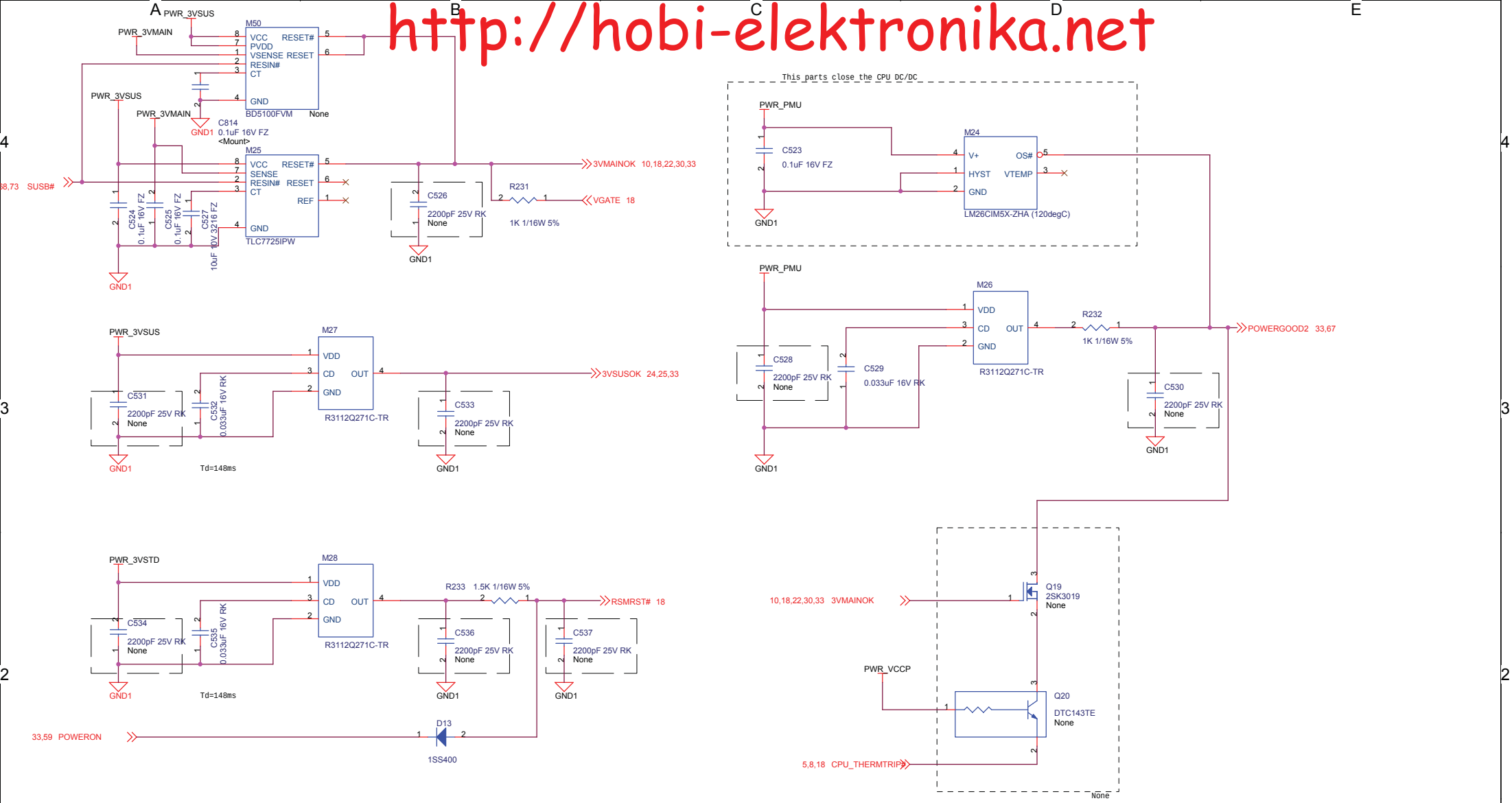


※02 NET接続変更



LAN

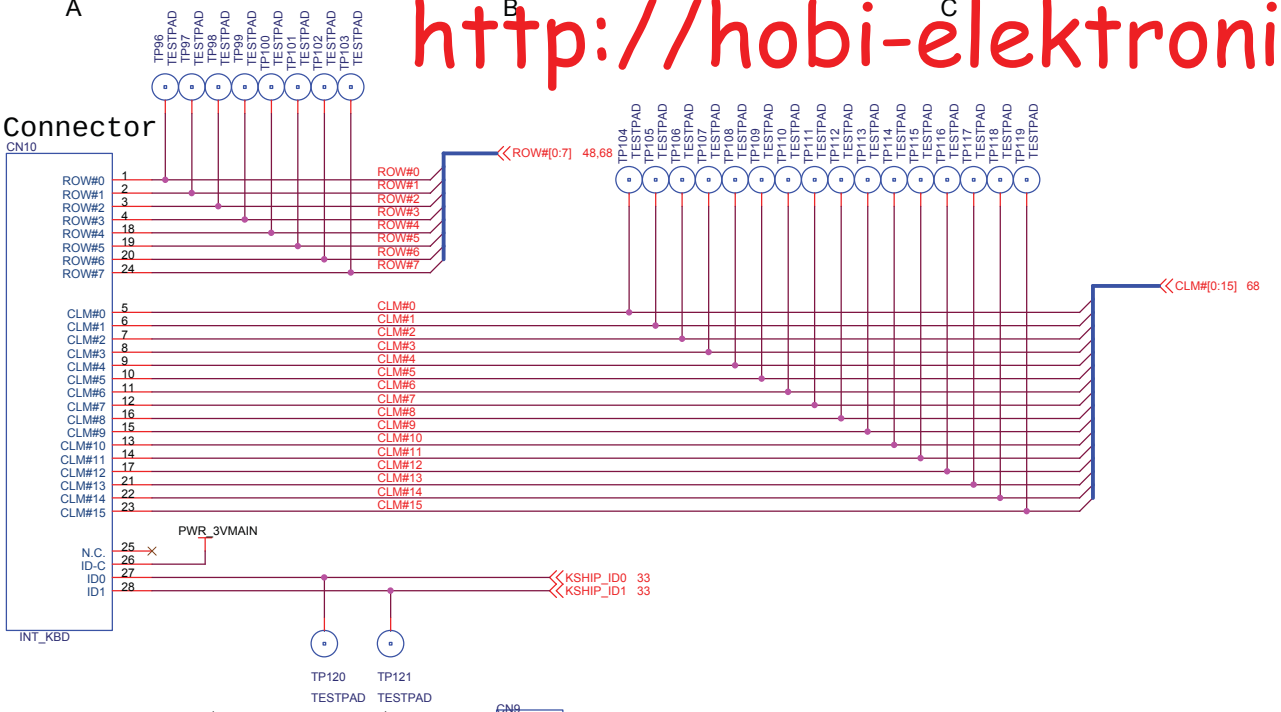
							TITLE	VB161AX MAIN
							DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description		Sheet	37 / 73
Design	02/05/07	Konaka	Check	Fuchida		Appr. Fukuyo	FUJITSU LTD.	



Fujitsu
Proprietary & Confidential

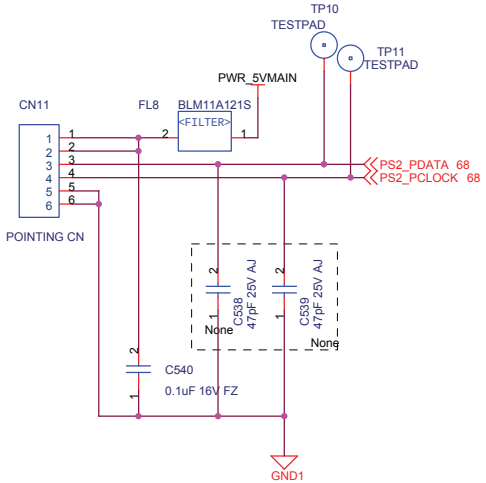
						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 38 / 73
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		

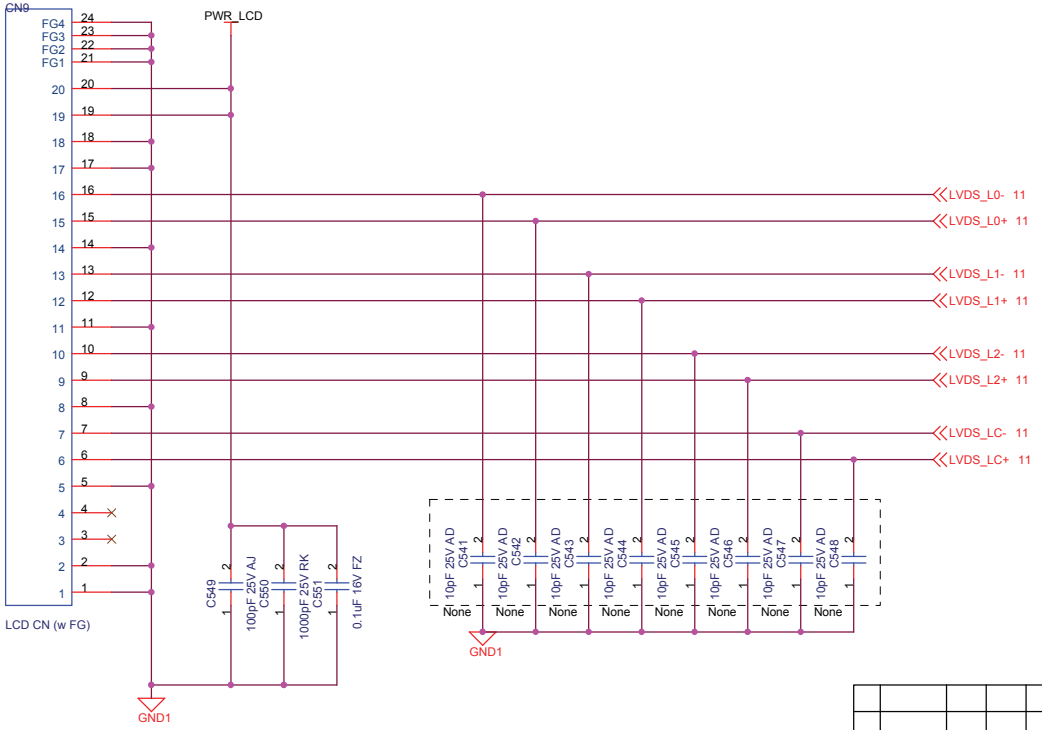
KeyBoard Connector

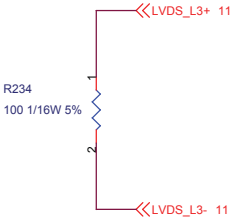


Keyboard Strap (N86C-7664-0203-E)
ID1:ID0 (KBC Side)

JP	1	1
US	1	0
UK	0	1







Pullup for IDE

						TITLE	VB161AX MAIN
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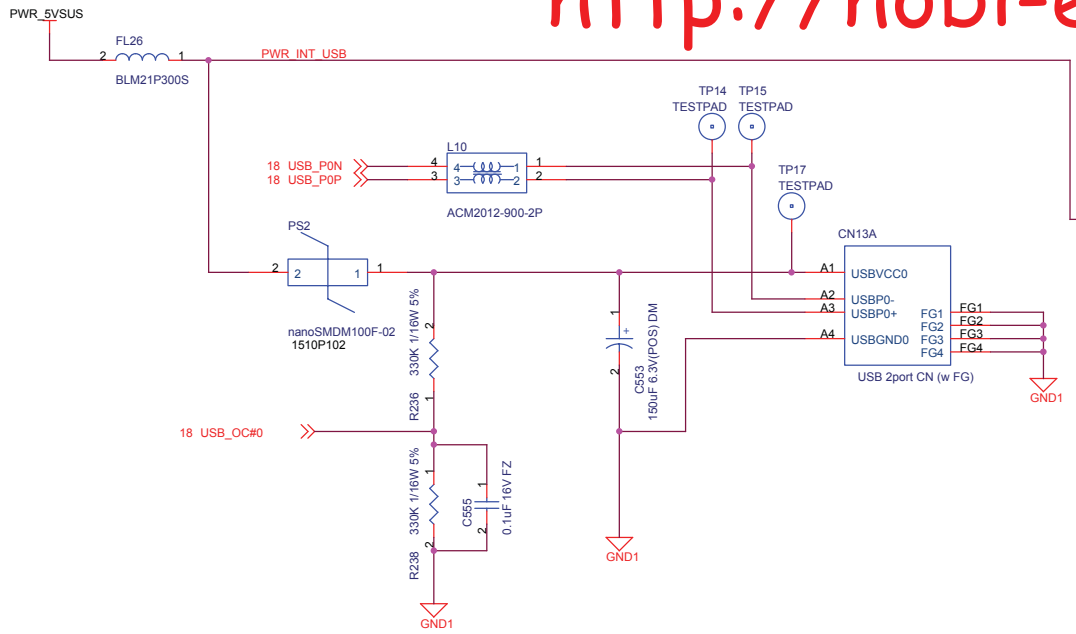
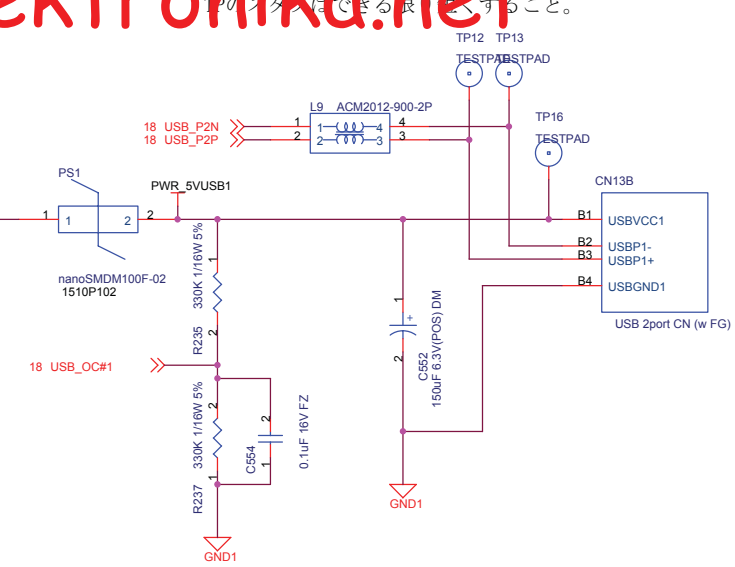
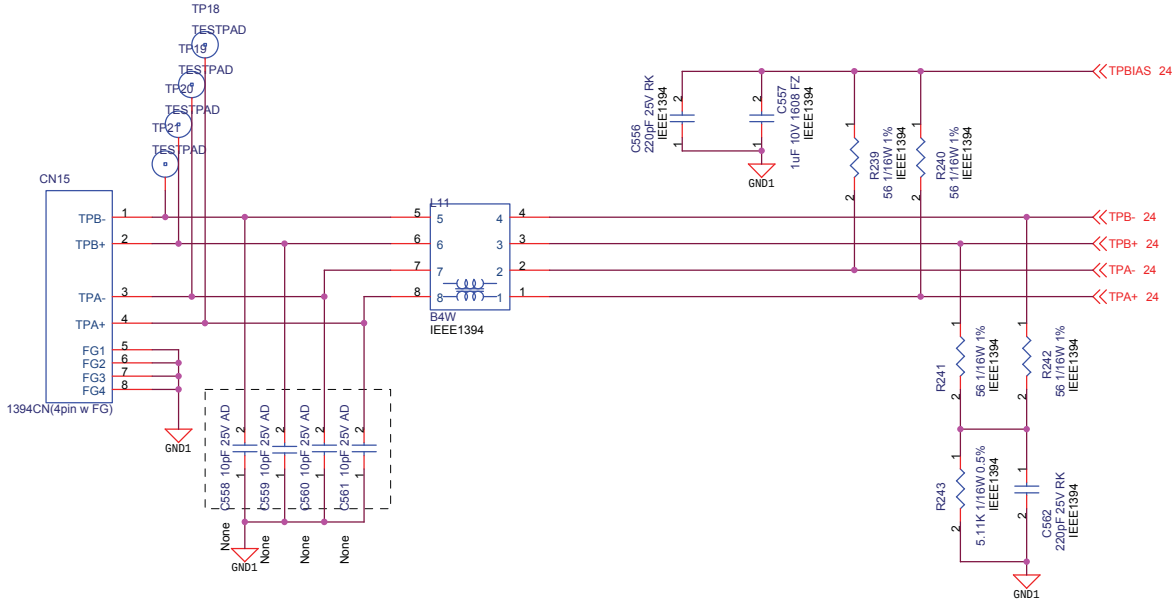
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		

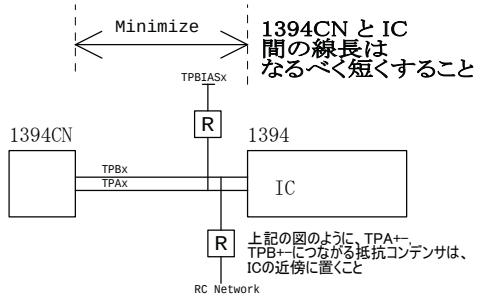
コモンモードコイル(L5,L6)はUSBコネクタの近傍（7mm以内)に配置すること。
TPのスタブはできる限り短くすること。





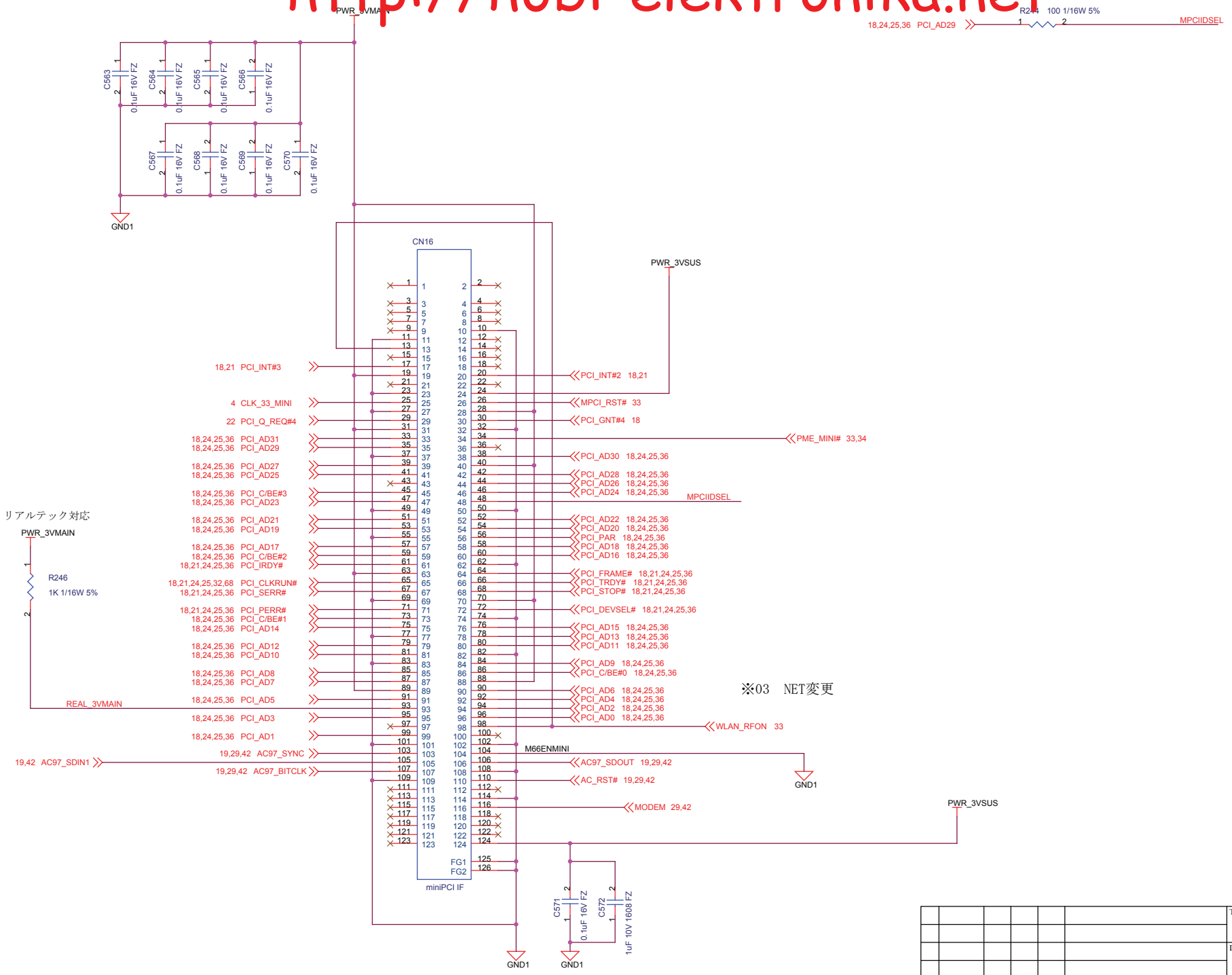
TPのスタブはできる限り短くすること。





I/O CN

						TITLE	VB161AX MAIN
						DRAW. No.	C1CP152845-X1 CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 40 / 73
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo		



MiniPCI CN

Rev.	Date	Design	Check	Appr.	Description
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo

TITLE: VB161AX MAIN

DRAW. No.: C1CP152845-X1

CAST

FUJITSU LTD.

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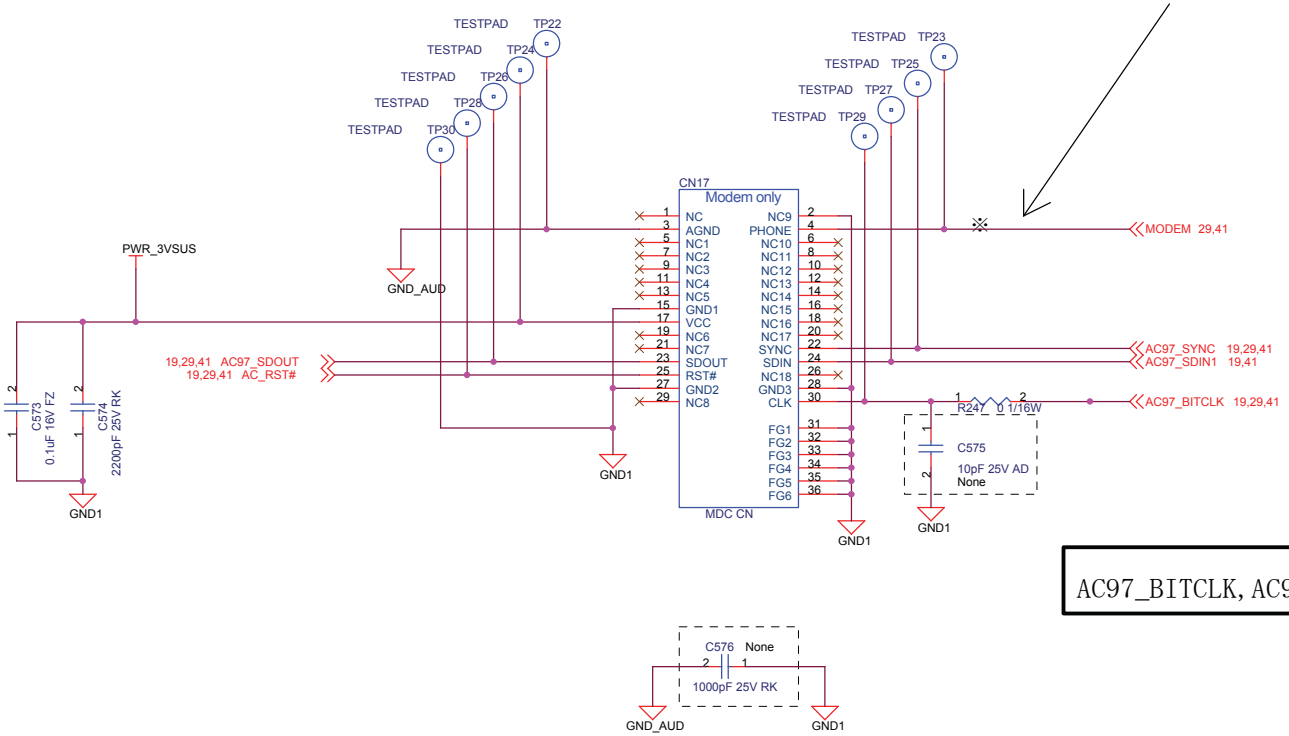
※印は微小なAnalogLineのため、GNDAUDでガード
(上下層を含む)すること。パターン幅 最小でかまいません。



AC97_BITCLK,AC97_RESET#はGND1でガードすること。

モジュールの固定用ネジ穴はGND１に接続する。

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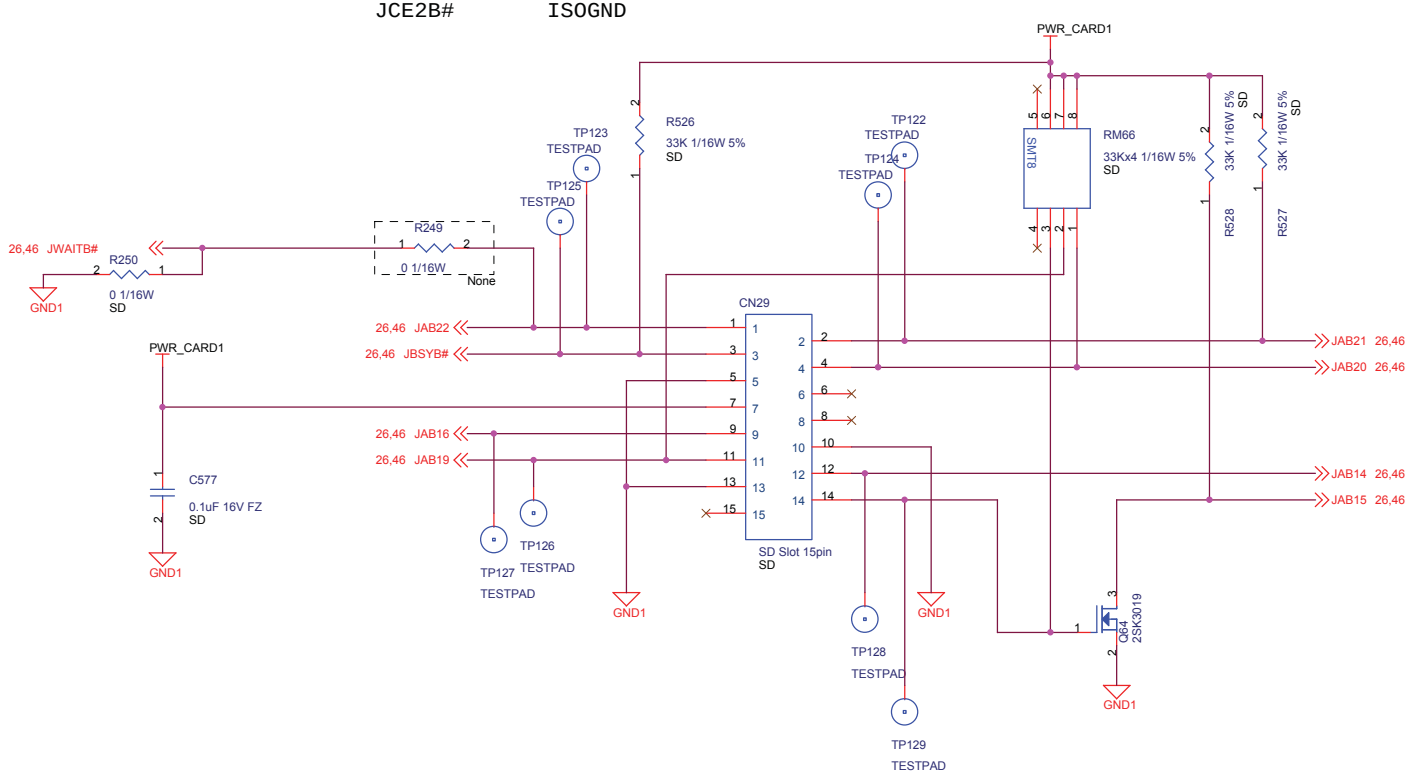
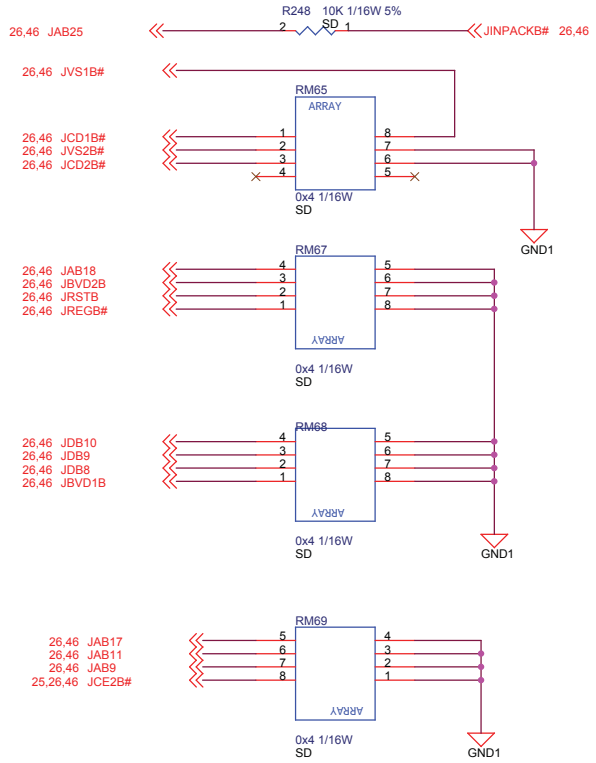
```
MISC
JWAITB#        SQRY3
JAB22           MC_CD#

JAB25           SQRYDR
JINPACKB#    SQRYDRX or SQRY4
JCD1B#         B_CCD1#
JVS1B#         B_CVS1
JCD2B#         B_CCD2#
JVS2B#         B_CVS2
JAB18           SQRY1
JRSTB          SQRY2
JREGB#        SQRY5
JBVD2B        SQRY6
JBVD1B        SQRY7
JDB8            SQRY8
JDB9            SQRY9
JDB10           SQRY10
JAB17          ISOGND
JAB11          ISOGND
JAB9           ISOGND
JCE2B#        ISOGND
```

```
SD I/F
JAB14      SD_DATA1
JAB19      SD_DATA0
JAB16      SD_CLK/MS_CLK
JAB20      SD_CMD
JBSYB#    SD_DATA3
JAB21      SD_DATA2
JAB15      MC_WP#
```


PWR_CARD1
R526
33K 1/16W 5%
SD
TP123
TESTPAD
TP125
TESTPAD
TP122
TESTPAD
TP124
TESTPAD
RM66
33Kx4 1/16W 5%
SD
SW18
R528
R527
26,46 JWAITB#
R250
0 1/16W
SD
GND1
R249
0 1/16W
None
CN29
26,46 JAB22
26,46 JBSYB#
JAB21 26,46
JAB20 26,46
JAB14 26,46
JAB15 26,46
SD Slot 15pin
SD
PWR_CARD1
C577
0.1uF 16V FZ
SD
26,46 JAB16
26,46 JAB19
TP126
TESTPAD
TP127
TESTPAD
TP128
TESTPAD
TP129
TESTPAD
Q64
2SK3019



[SD SLOT]

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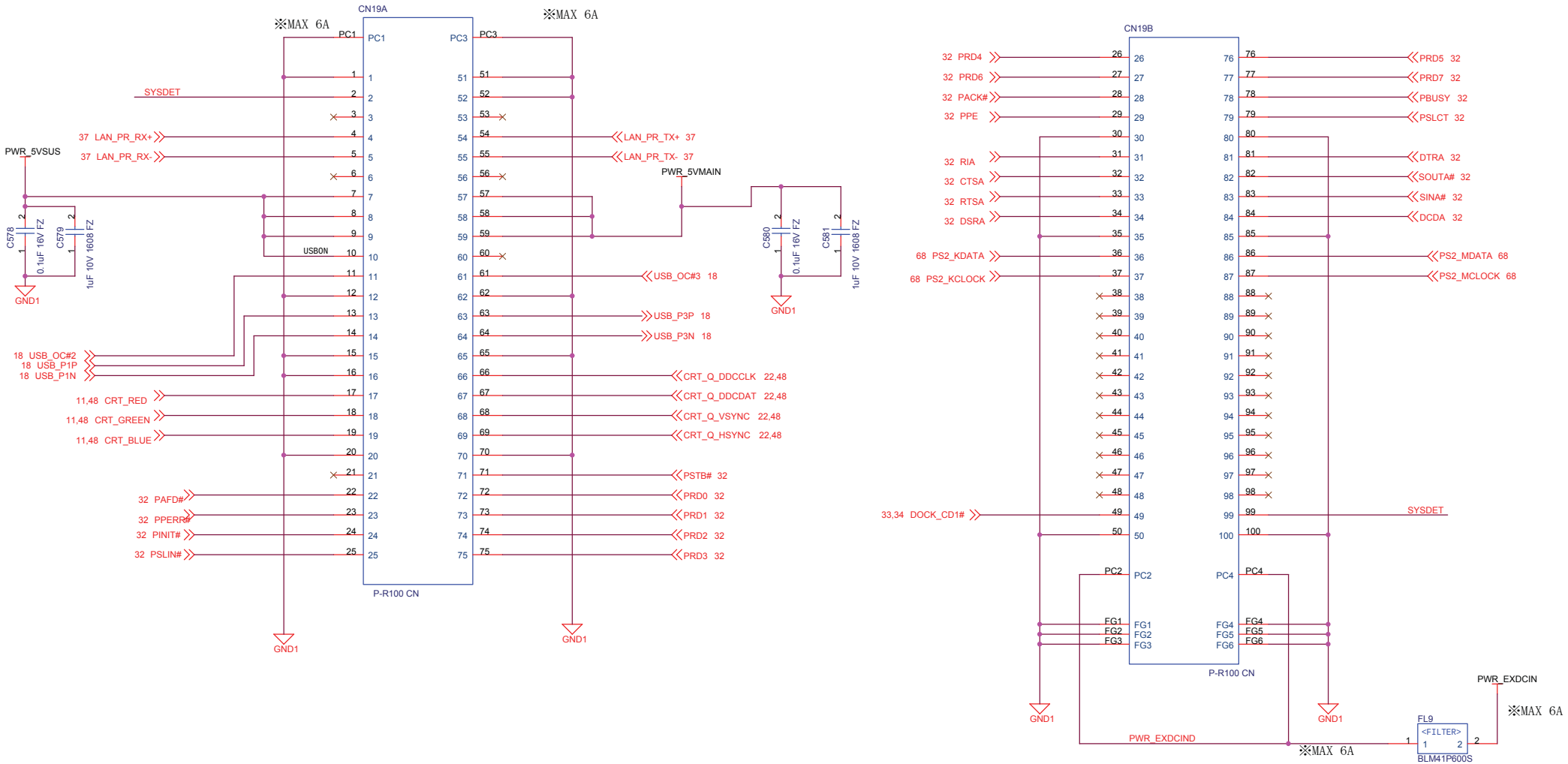
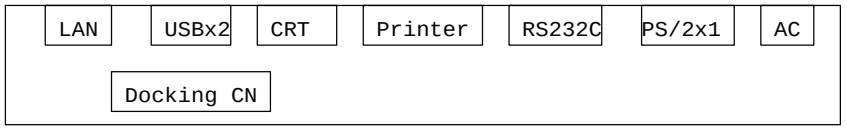


Port replicator Layout



P-R CN

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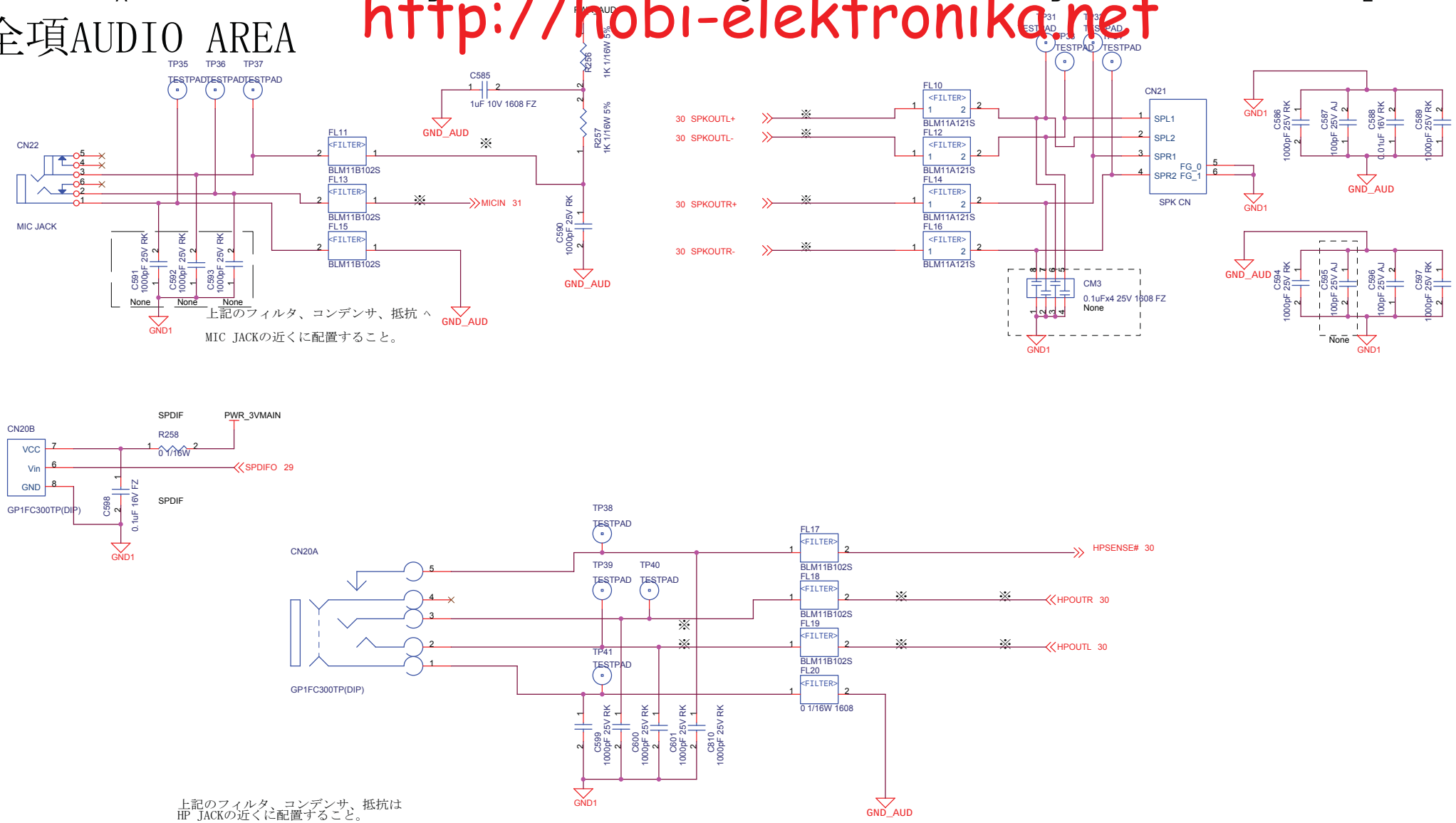
全項AUDIO AREA



上記のフィルタ、コンデンサ、抵抗 ヘ
MIC JACKの近くに配置すること。

上記のフィルタ、コンデンサ、抵抗は
HP JACKの近くに配置すること。

本ページ中に記載されているフィルタ(FLxx)はそれぞれ接 ア
されているコネクタの近くに配置し、フィルターコネクタ間の z
線は非常に短く配線すること。
The filters in this page (refered with FLxx) have to be placed near each connector connecting to respective filters. The traces between connector and filter have to be short as much as possible.

本項中※印のついたパターンは、AUDIOGND ナガードし、その上下はAUDIOGNDのベタパターンで覆うこと。 りた、Mxの下の基板面およびその下の層には、ディジタル系の信号線を配線しないこと。
The traces marked with ※ have to be guarded both side and both adjacent layer with AUDIOGND. Underneath Mx on surface layer and in one more internal layer don't allow digital traces to be run.

Audio CN

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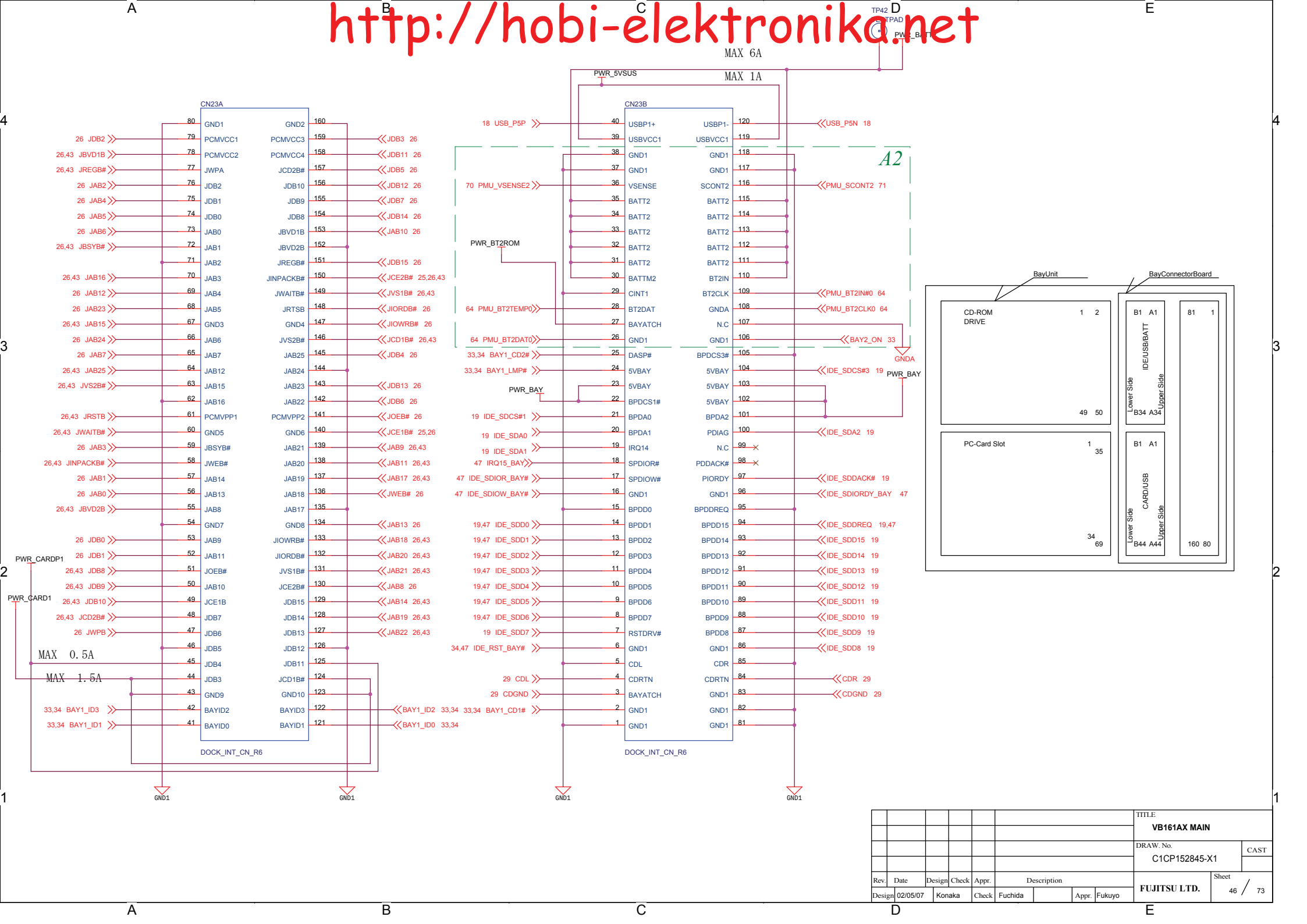

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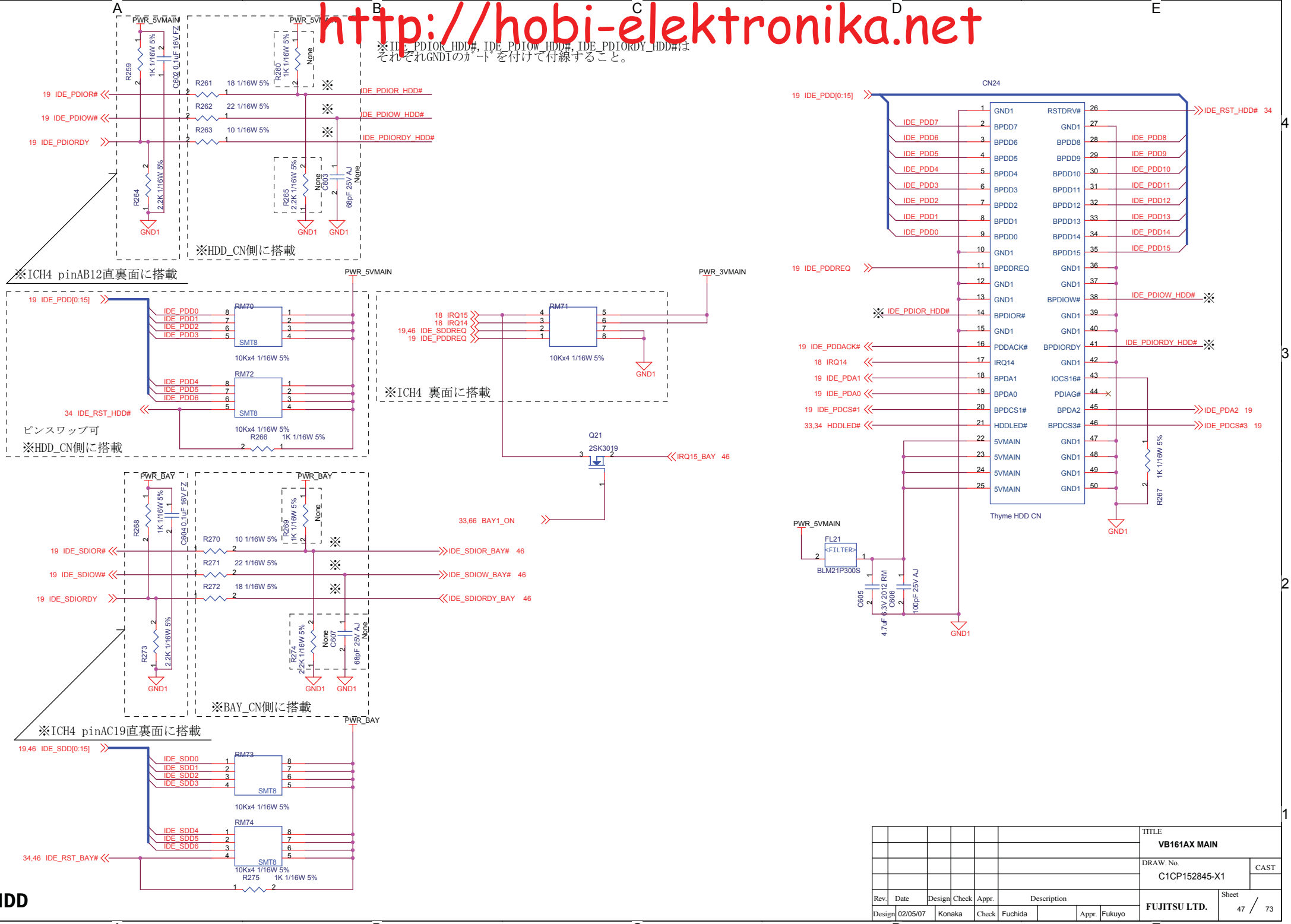
※IDE_PDIOR_HDD#,IDE_PDIOW_HDD#,IDE_PDIORDY_HDD#は
それぞれGND1のｶﾟﾄﾞを付けて付線すること。



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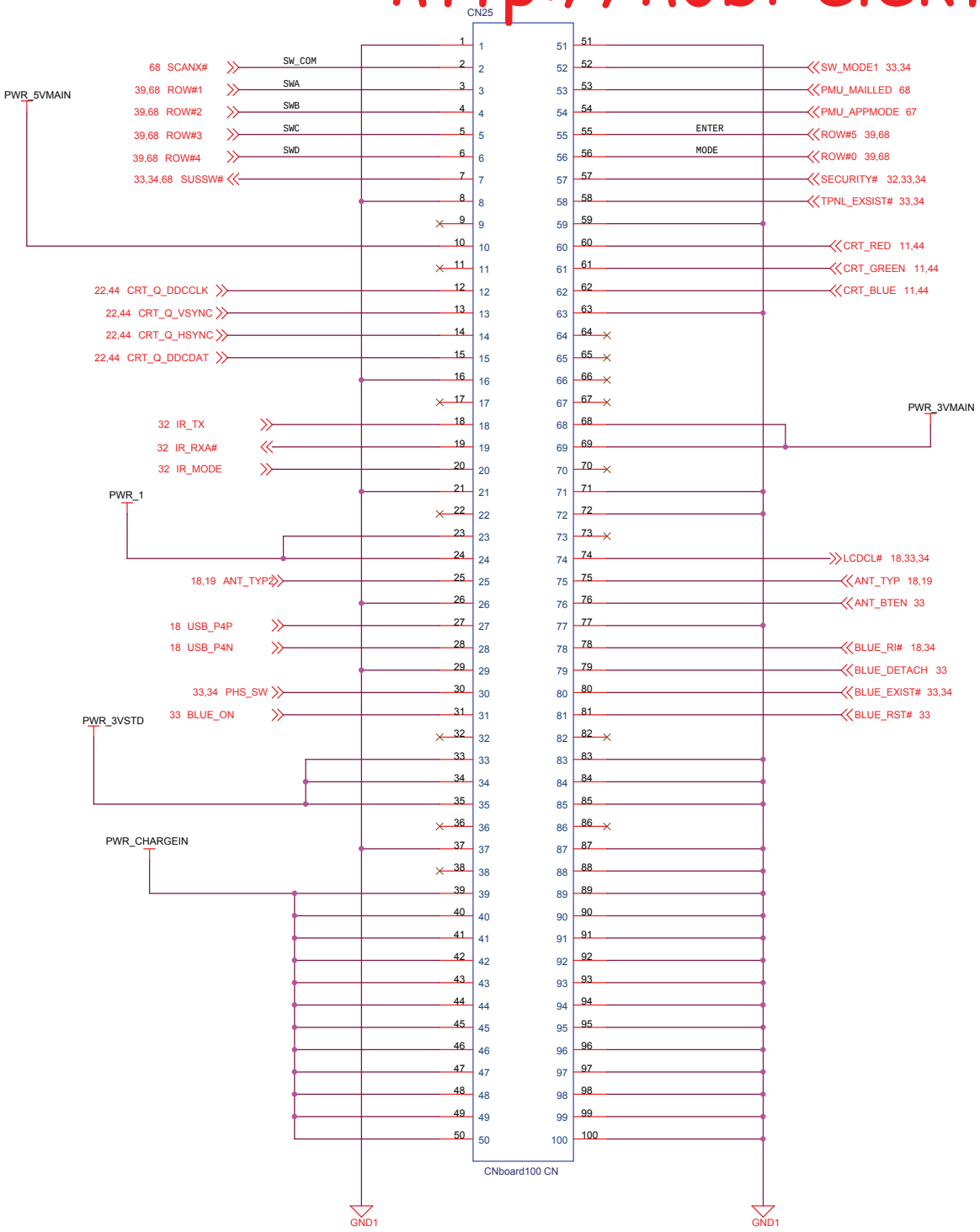

CN Board

							TITLE	VB161AX MAIN
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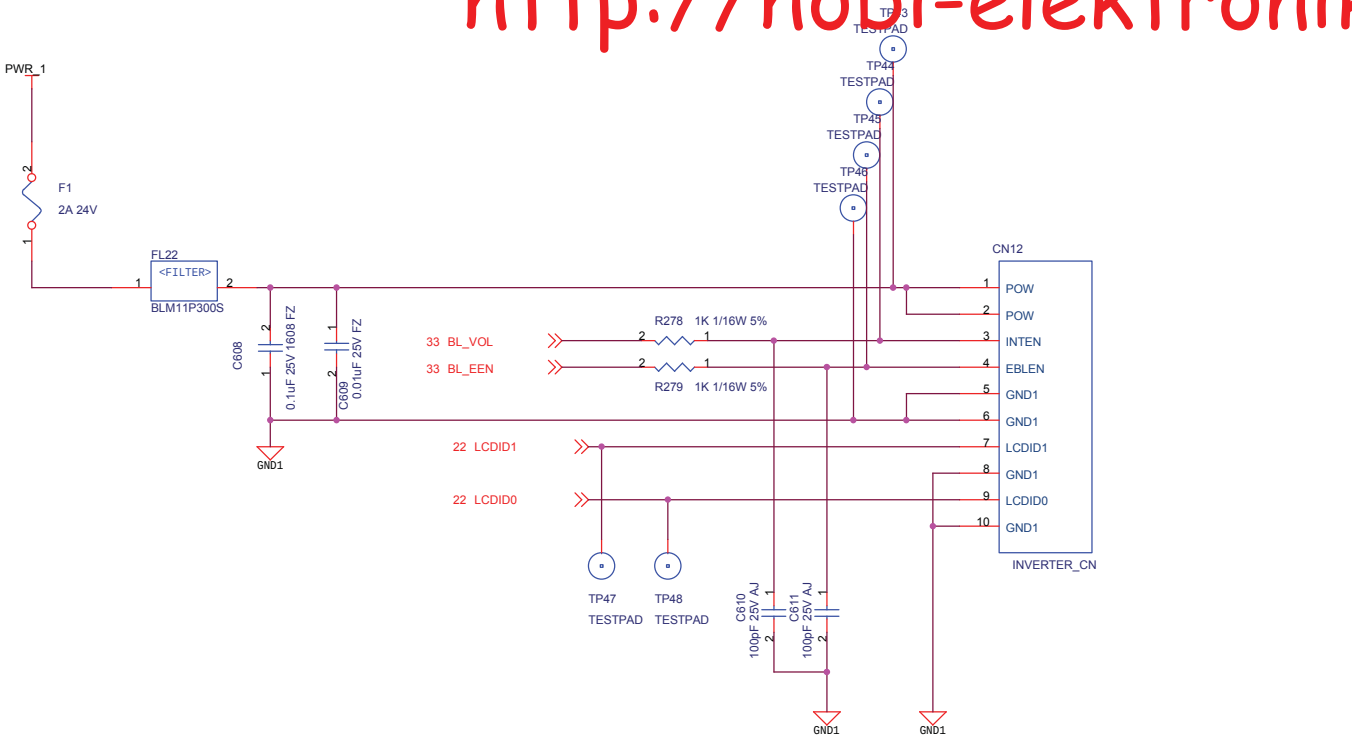

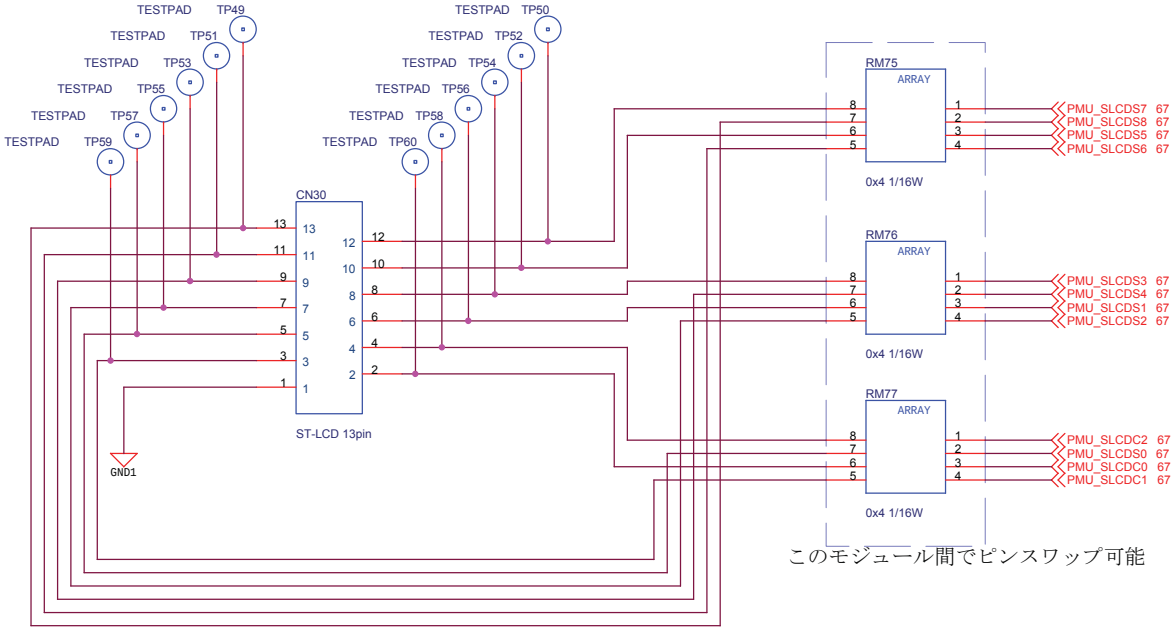

このモジュール間でピンスワップ可能

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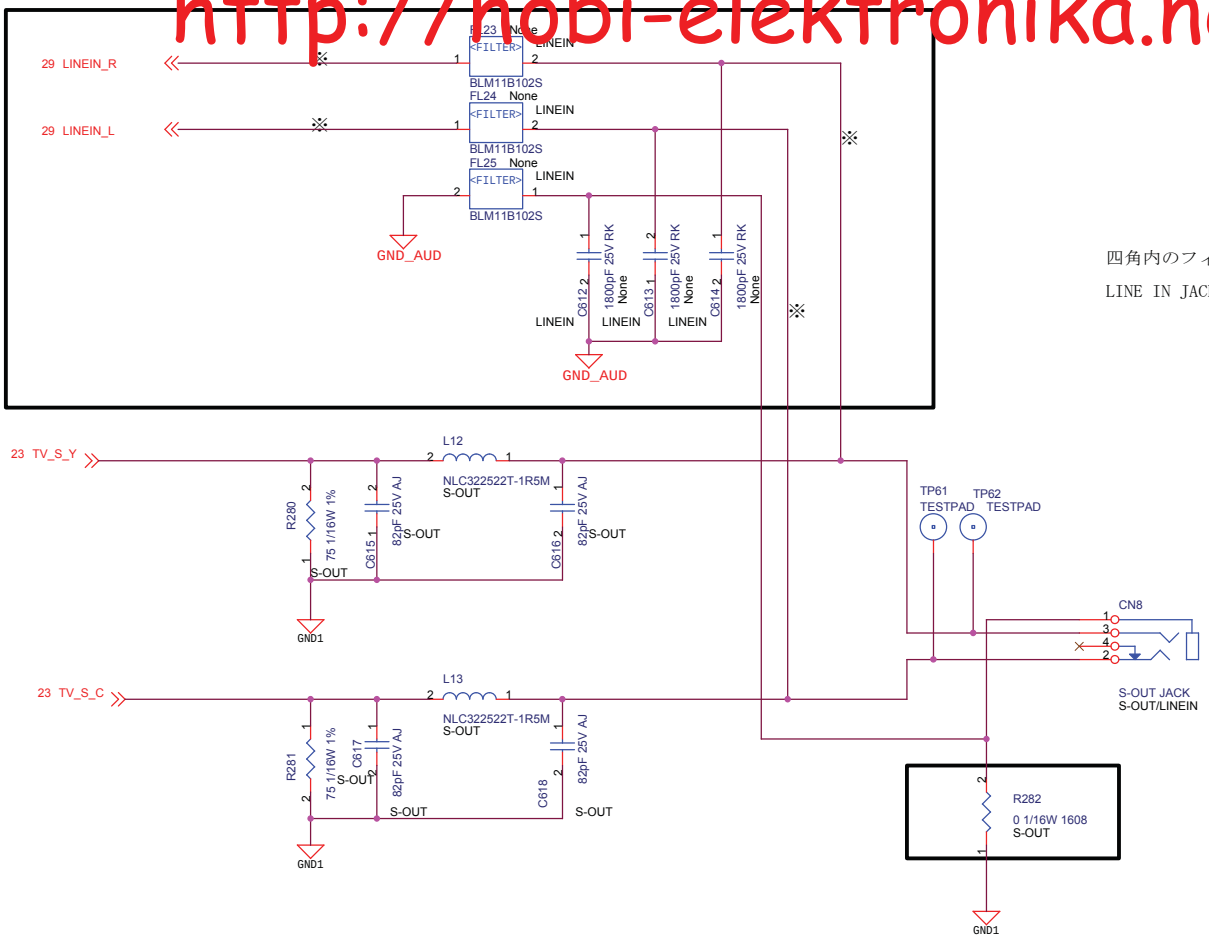

四角内のフィルタ、コンデンサ、抵抗は
LINE IN JACKの近くに配置すること。

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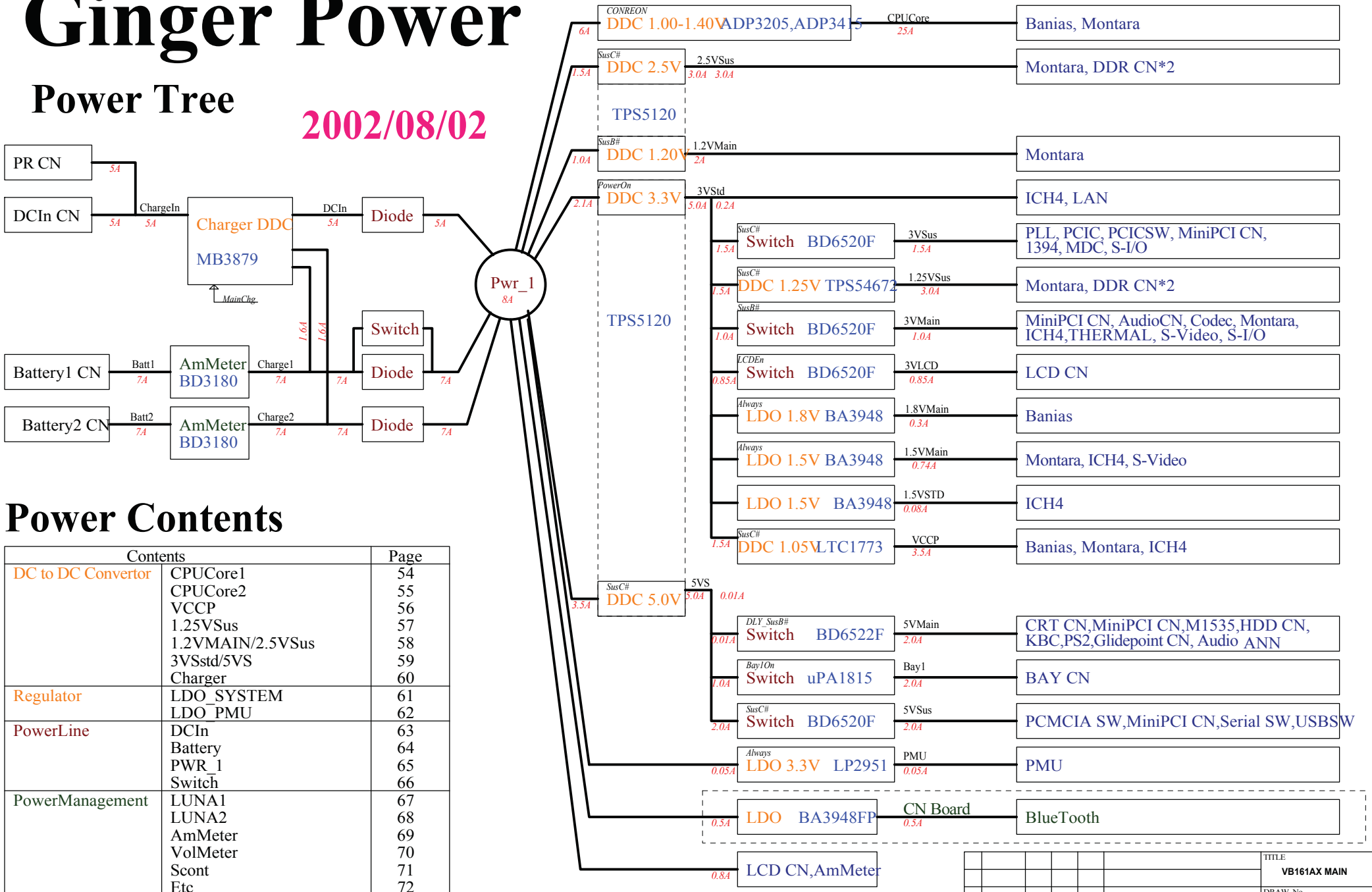
DDC ; DC to DC Convertor

Ginger Power

Power Tree

2002/08/02



Power Contents

Power/ TopPage

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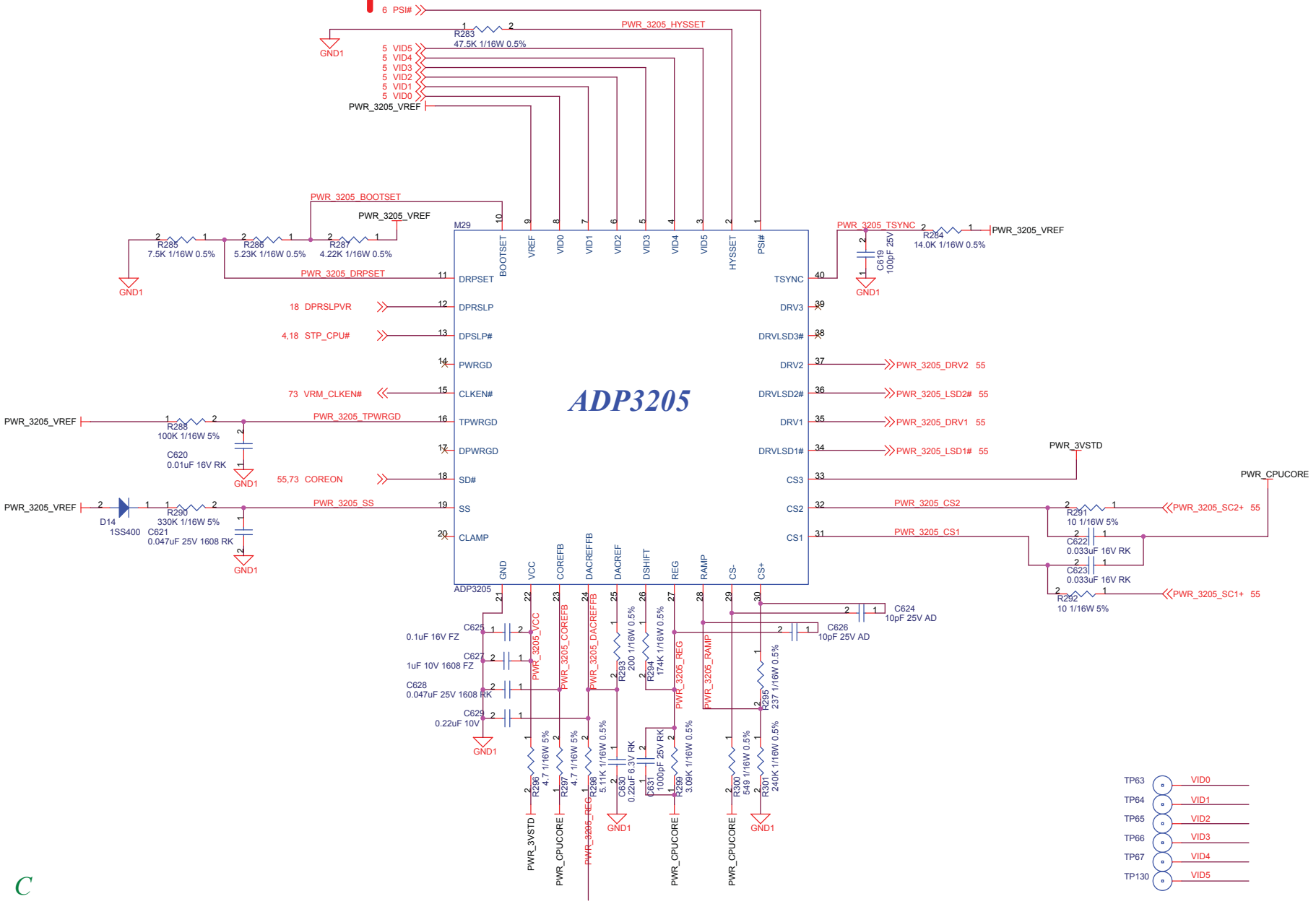

Power/ DDC/ CPUCore 1

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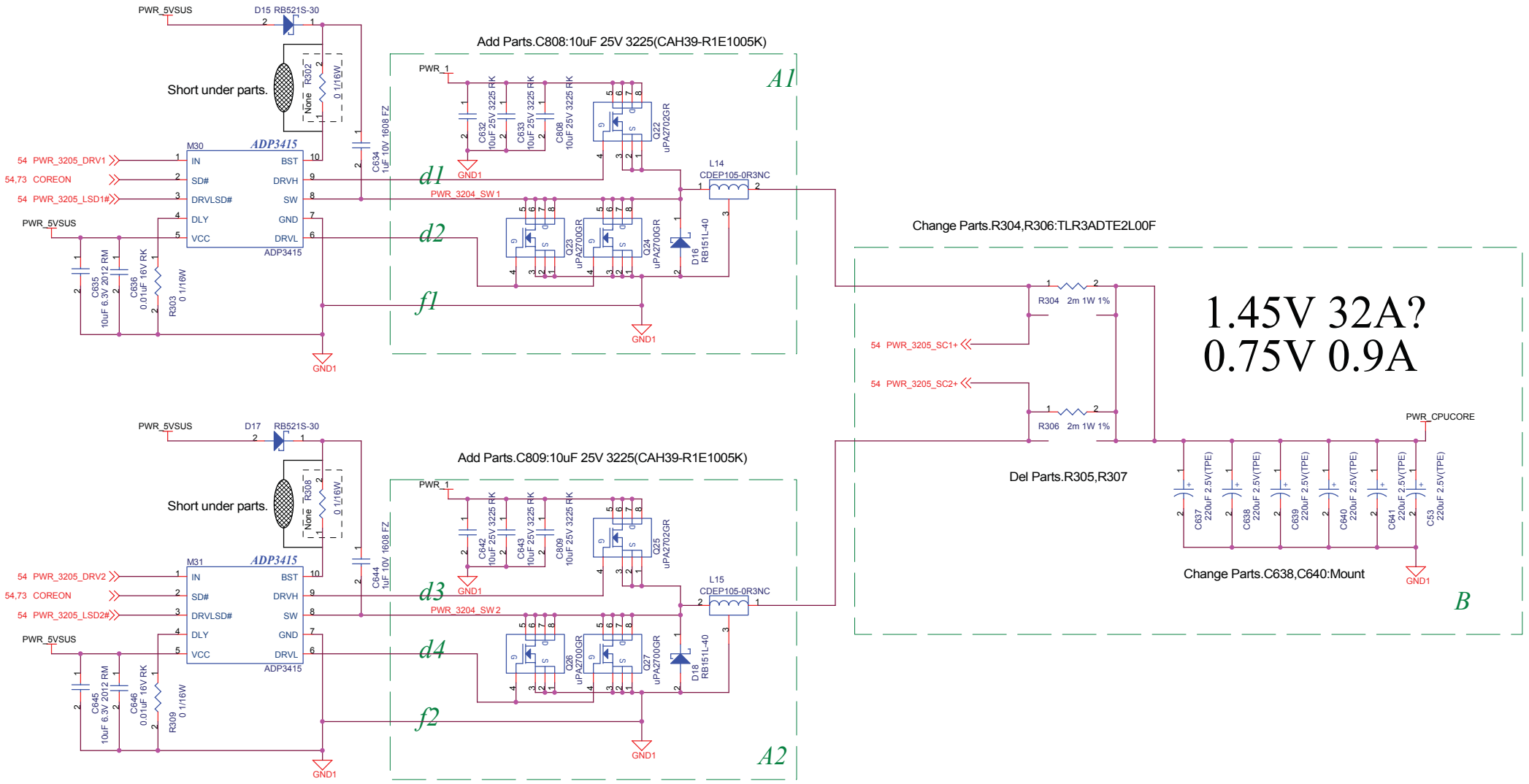

Power/ DDC/ CPUCore2

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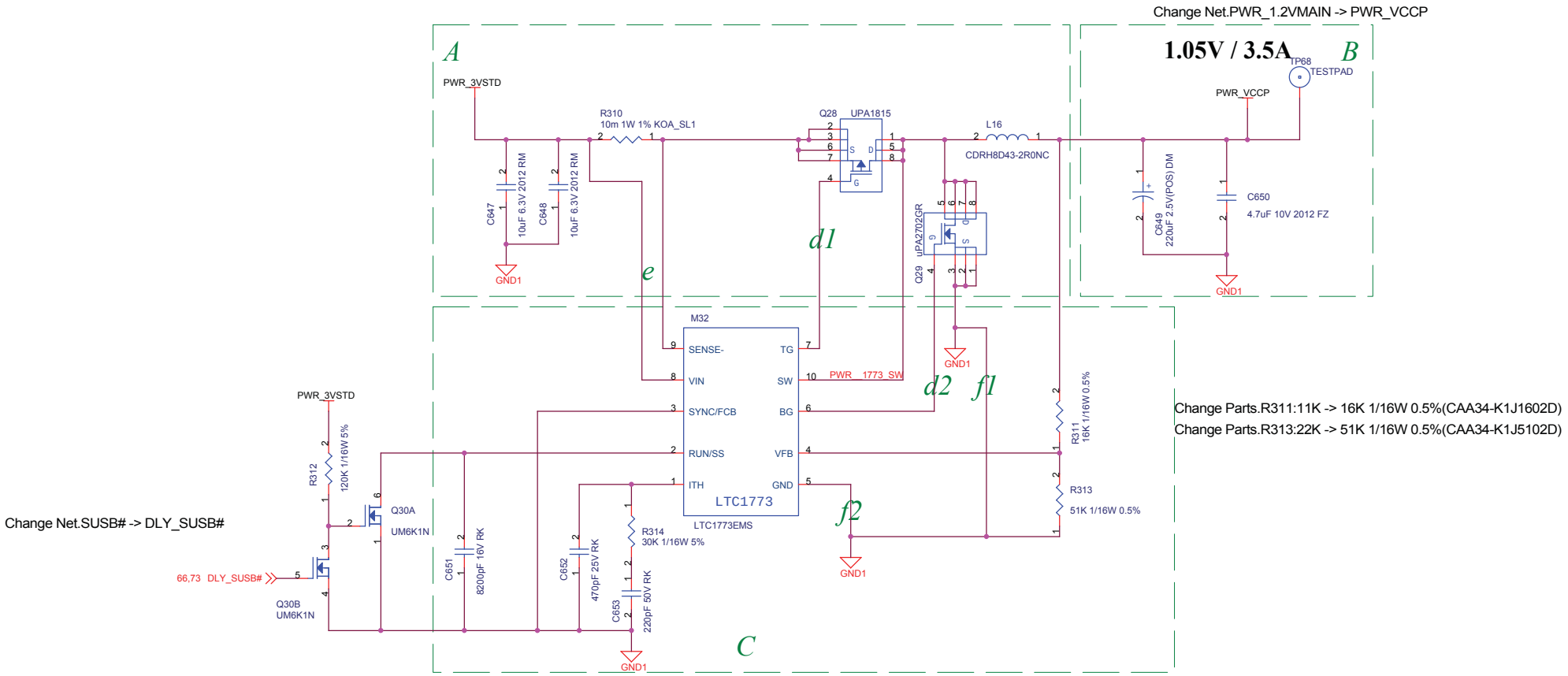
Change Net.PWR_1.2VMAIN -> PWR_VCCP



Change Net.SUSB# -> DLY_SUSB#

Change Parts.R311:11K -> 16K 1/16W 0.5%(CAA34-K1J1602D)
Change Parts.R313:22K -> 51K 1/16W 0.5%(CAA34-K1J5102D)

Power/ DDC/ VCCP

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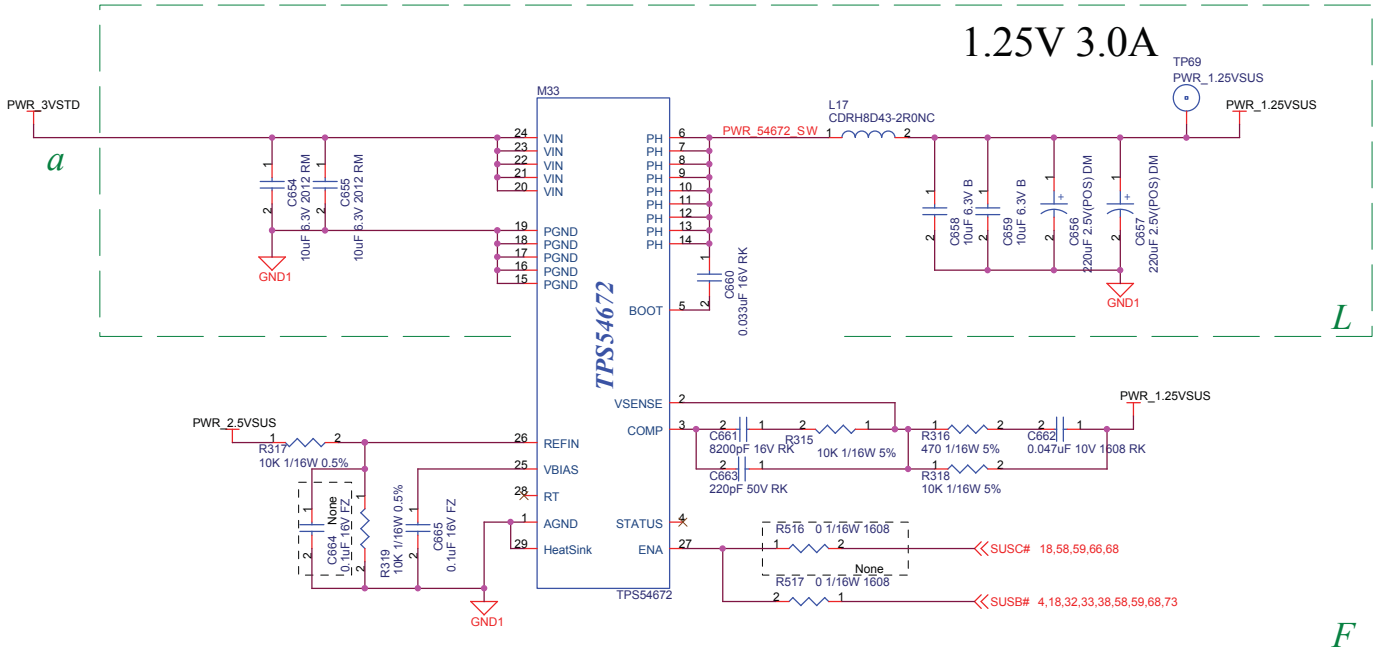

Power/ DDC/ 1.25VSus

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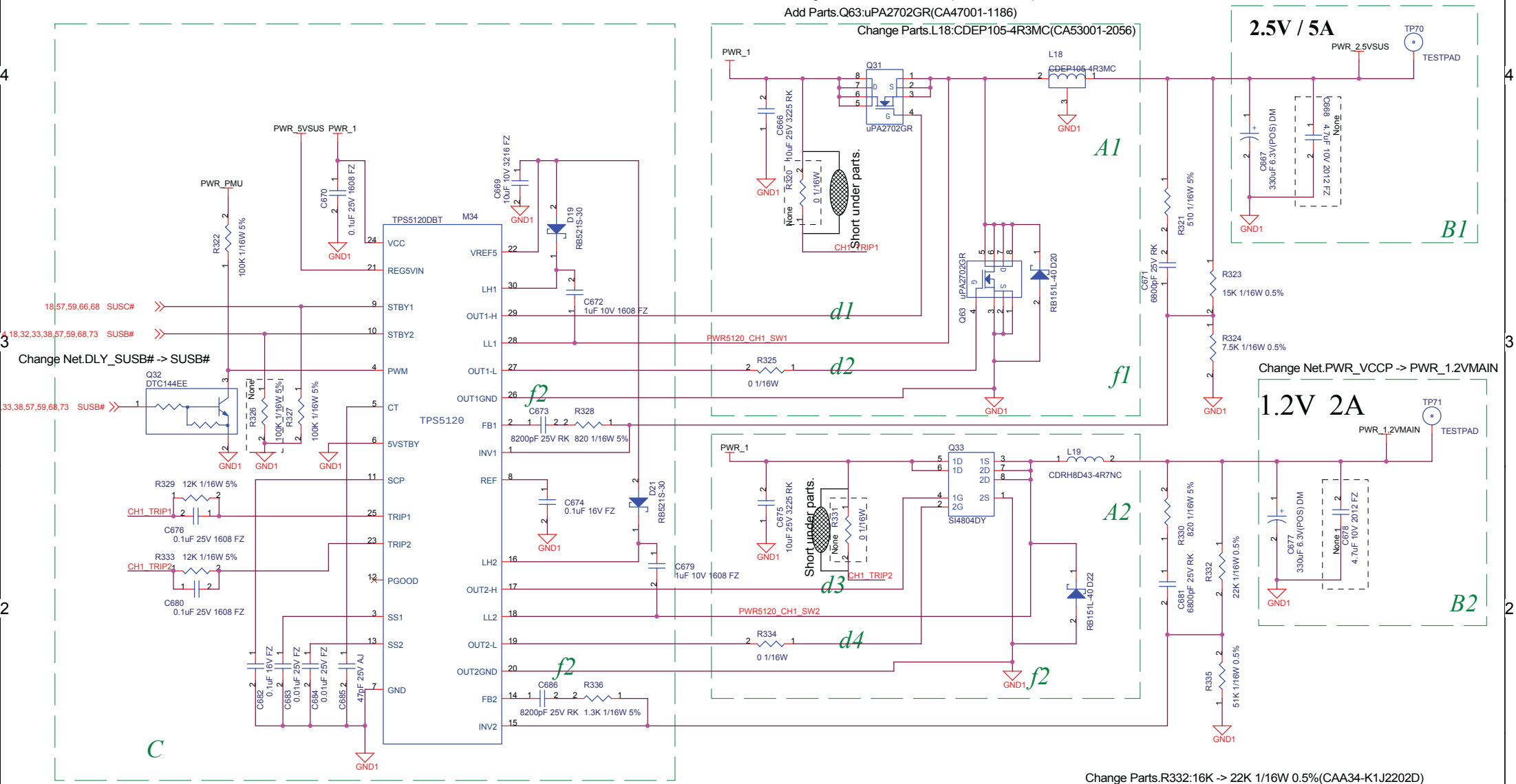
Change Parts.Q31:uPA2702GR(CA47001-1186)
Add Parts.Q63:uPA2702GR(CA47001-1186)
Change Parts.L18:CDEP105-4R3MC(CA53001-2056)



Change Parts.R332:16K -> 22K 1/16W 0.5%(CAA34-K1J2202D)
Change Parts.R335:68K -> 51K 1/16W 0.5%(CAA34-K1J5102D)

Power/ DDC/ 2.5VSUS/1.2VMAIN

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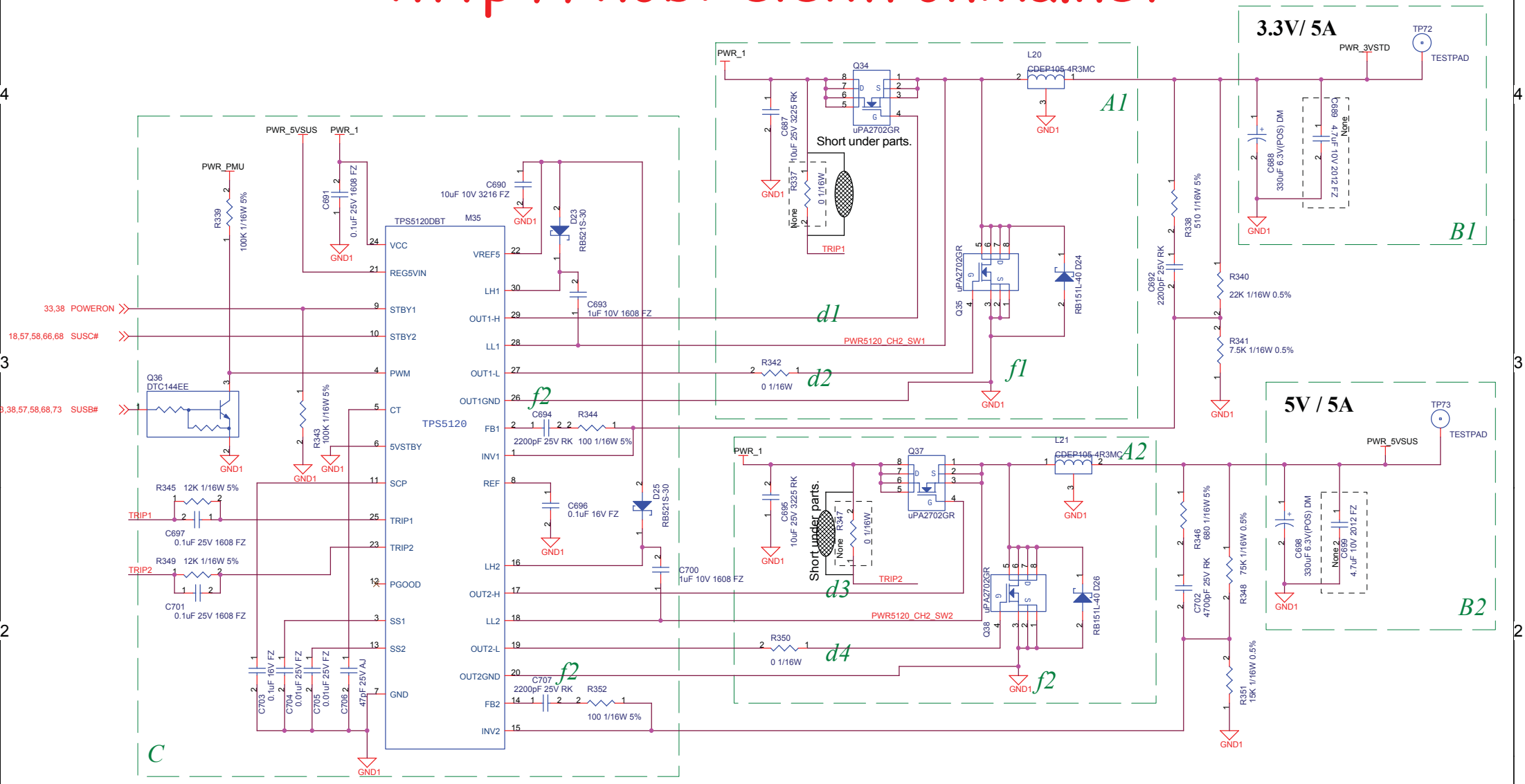

Power/ DDC/ 3VStr,5VS

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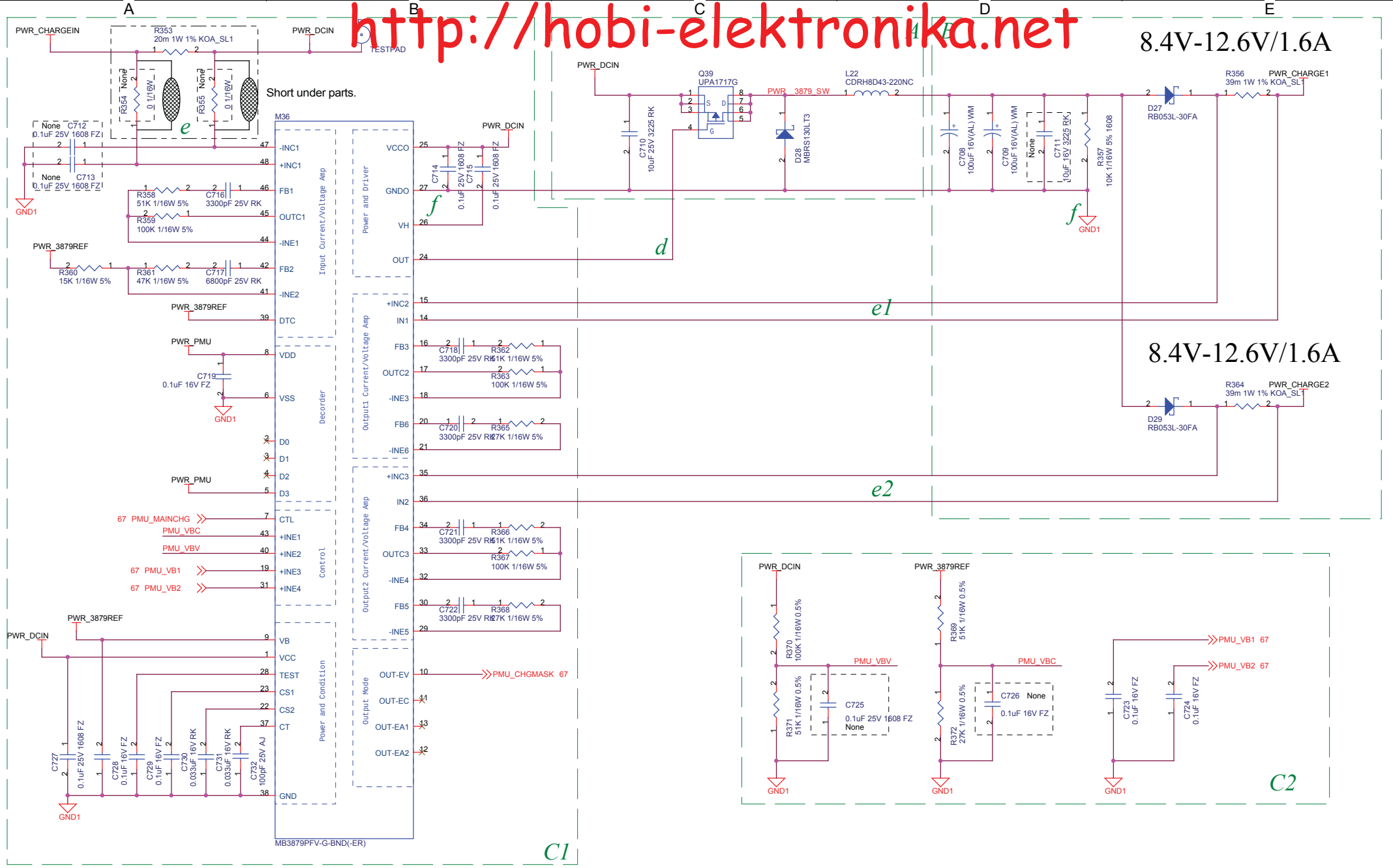

Power/ DDC/ Charger

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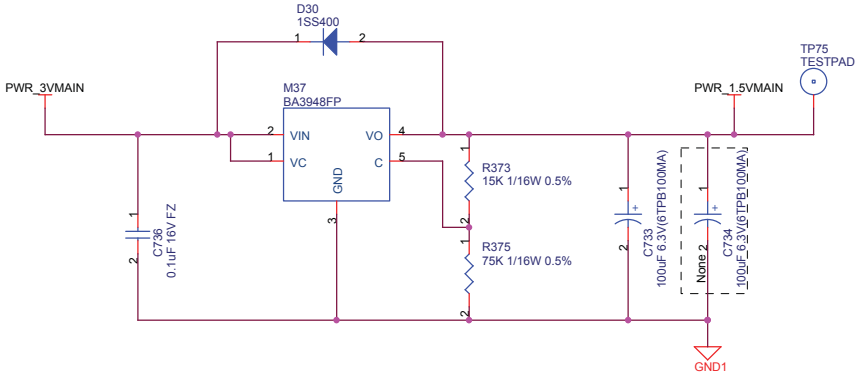
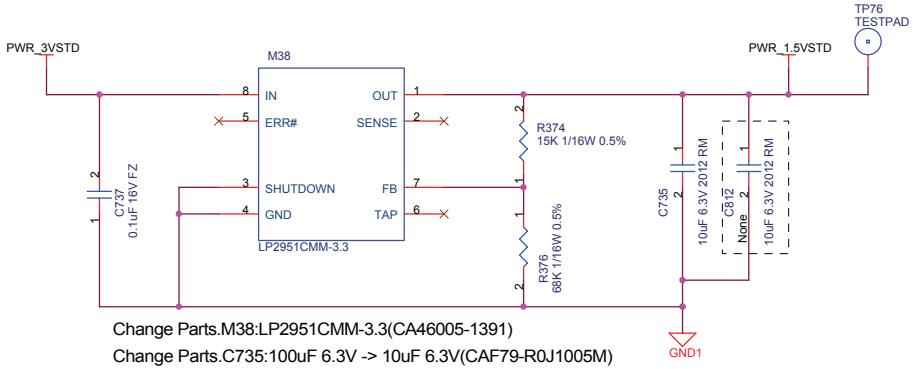
1.5V 0.74A

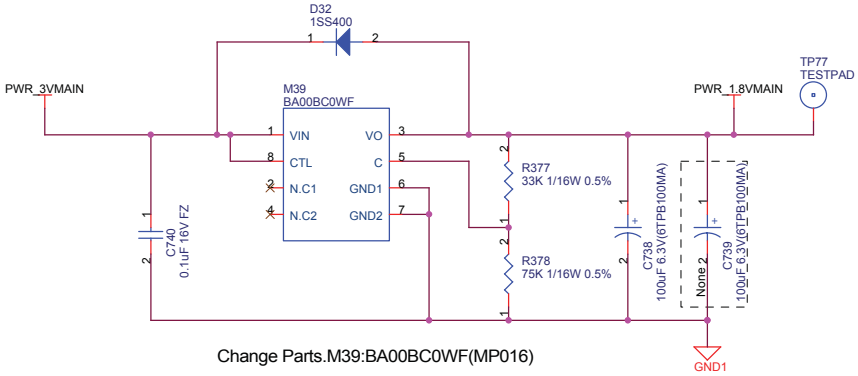


1.5V 0.08A



Change Parts.M38:LP2951CMM-3.3(CA46005-1391)
Change Parts.C735:100uF 6.3V -> 10uF 6.3V(CAF79-R0J1005M)
Add Parts.C812:10uF 6.3V(CAF79-R0J1005M)Reserve
Change Parts.R376:75K -> 68K 1/16W 0.5%(CAA34-K1J6802D)

1.8V 0.3A



Change Parts.M39:BA00BC0WF(MP016)

Power/ LDO/ System

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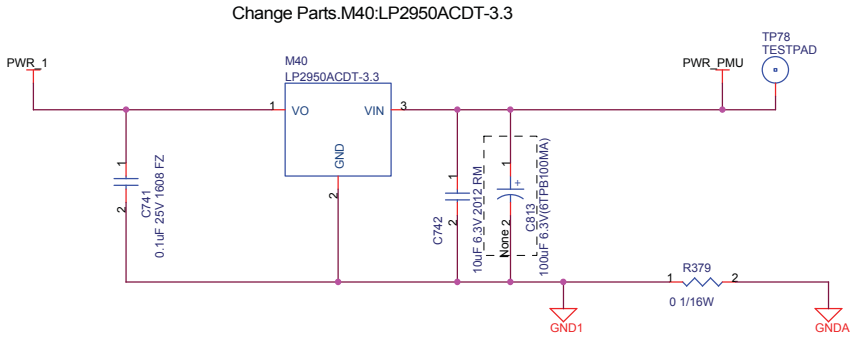

3.3V 50mA

Power/ LDO/ PMU

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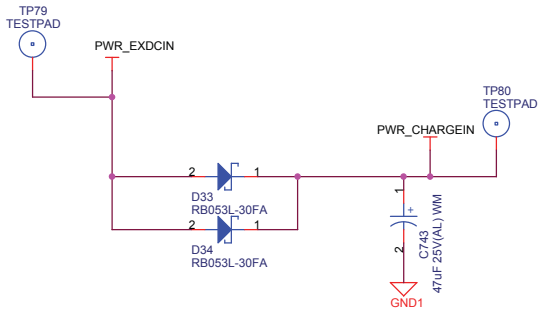

Power/ Node/ DCIn

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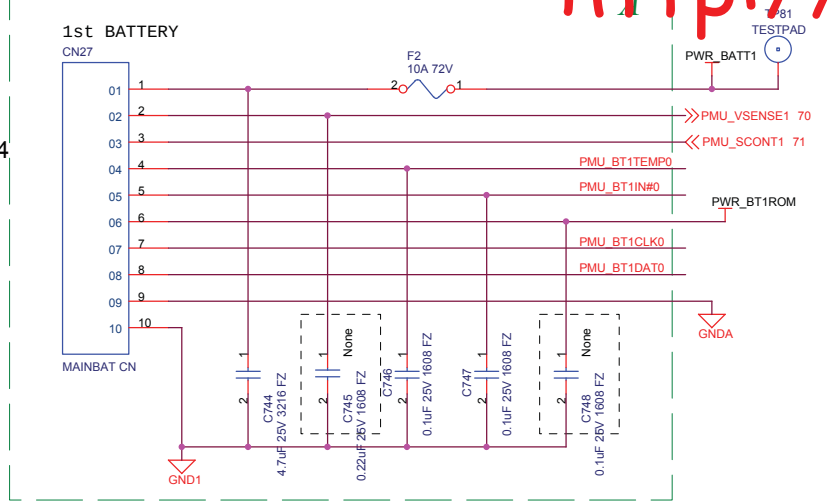

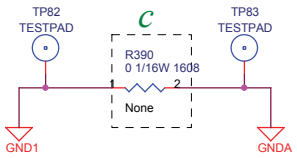

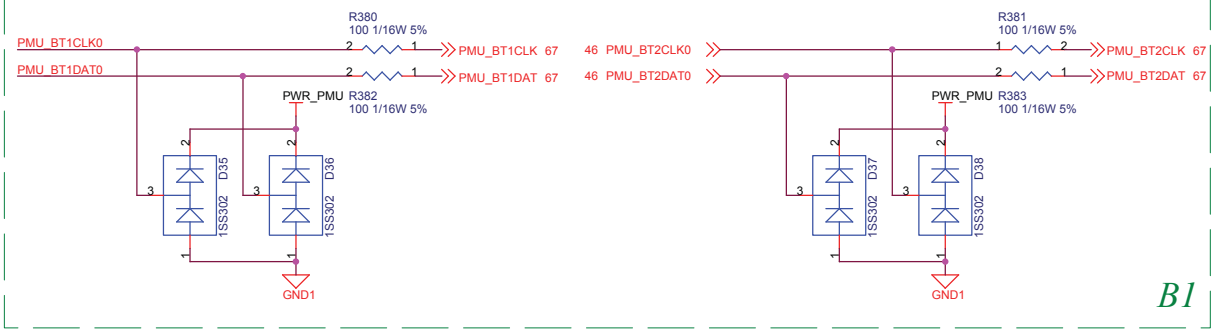

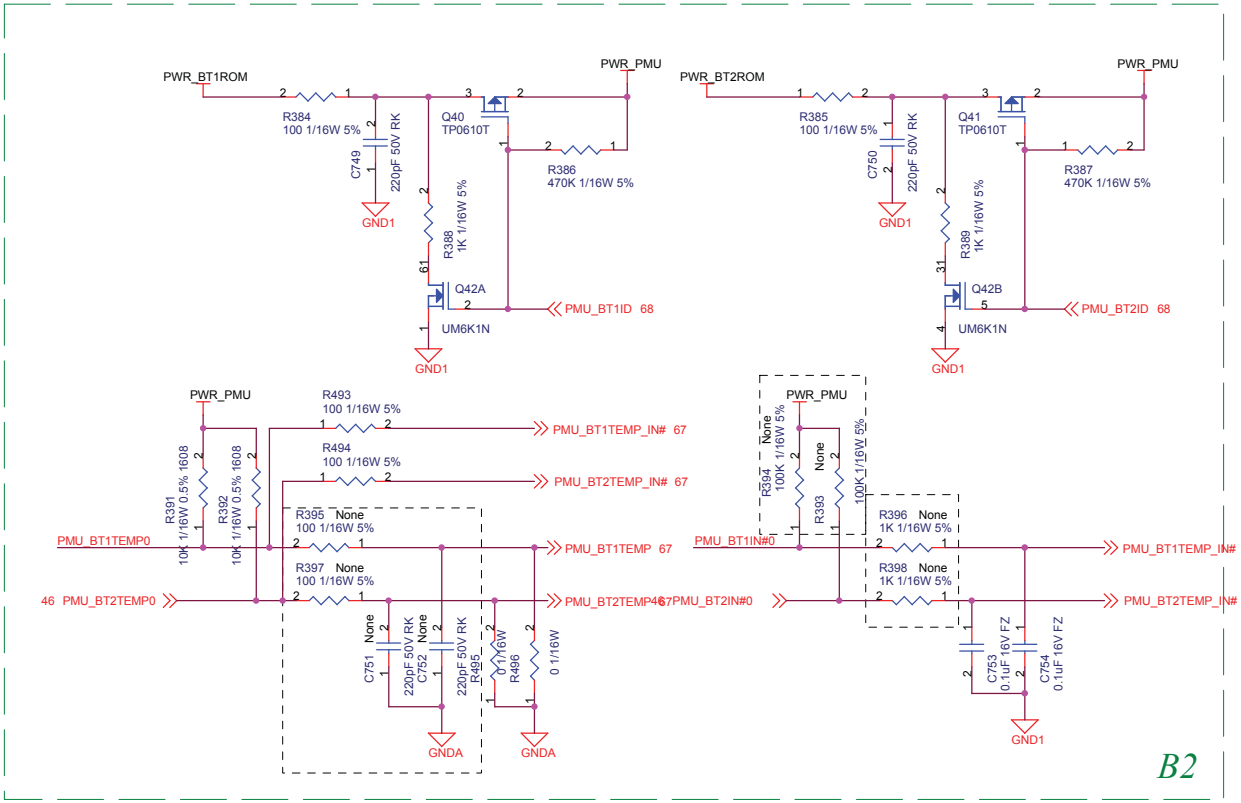

Power/ Node/ Battery

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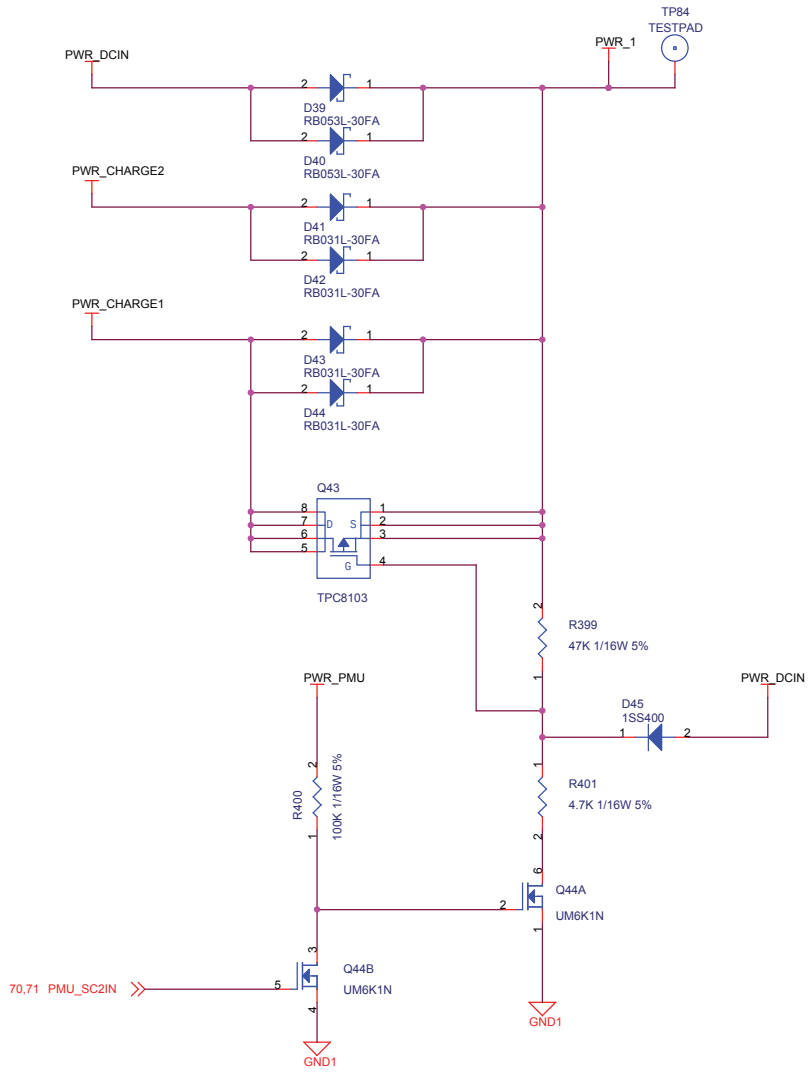

Power/ Node/ PWR_1

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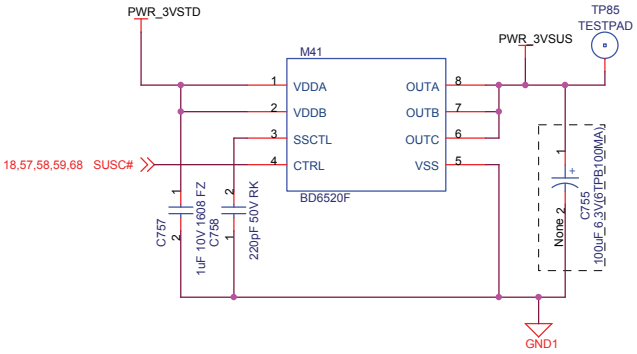
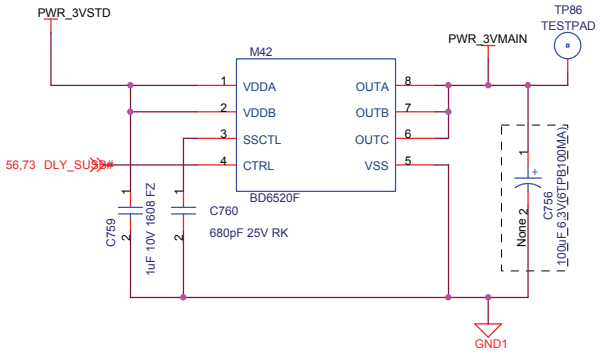
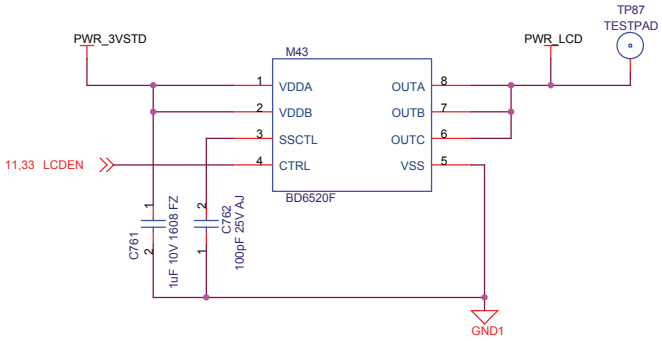
3.3V 2.0A



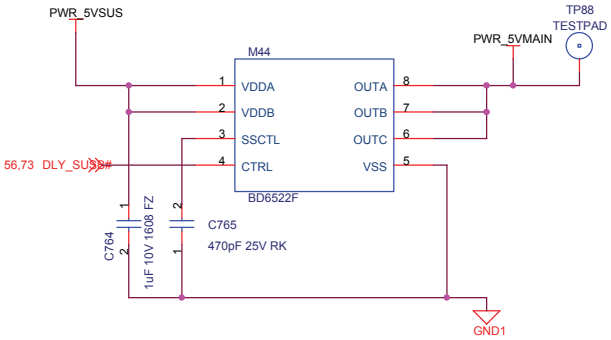
3.3V 2.0A



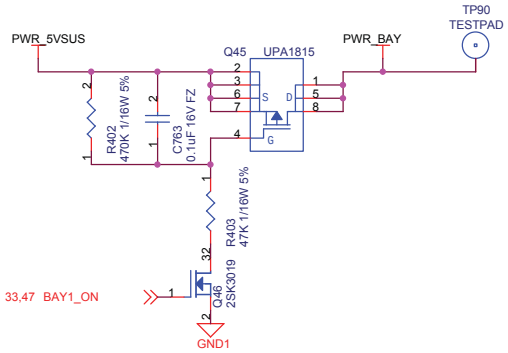
3.3V 1.0A



5.0V 2.0A



5.0V 2.0A



Power/ Node/ Swicth

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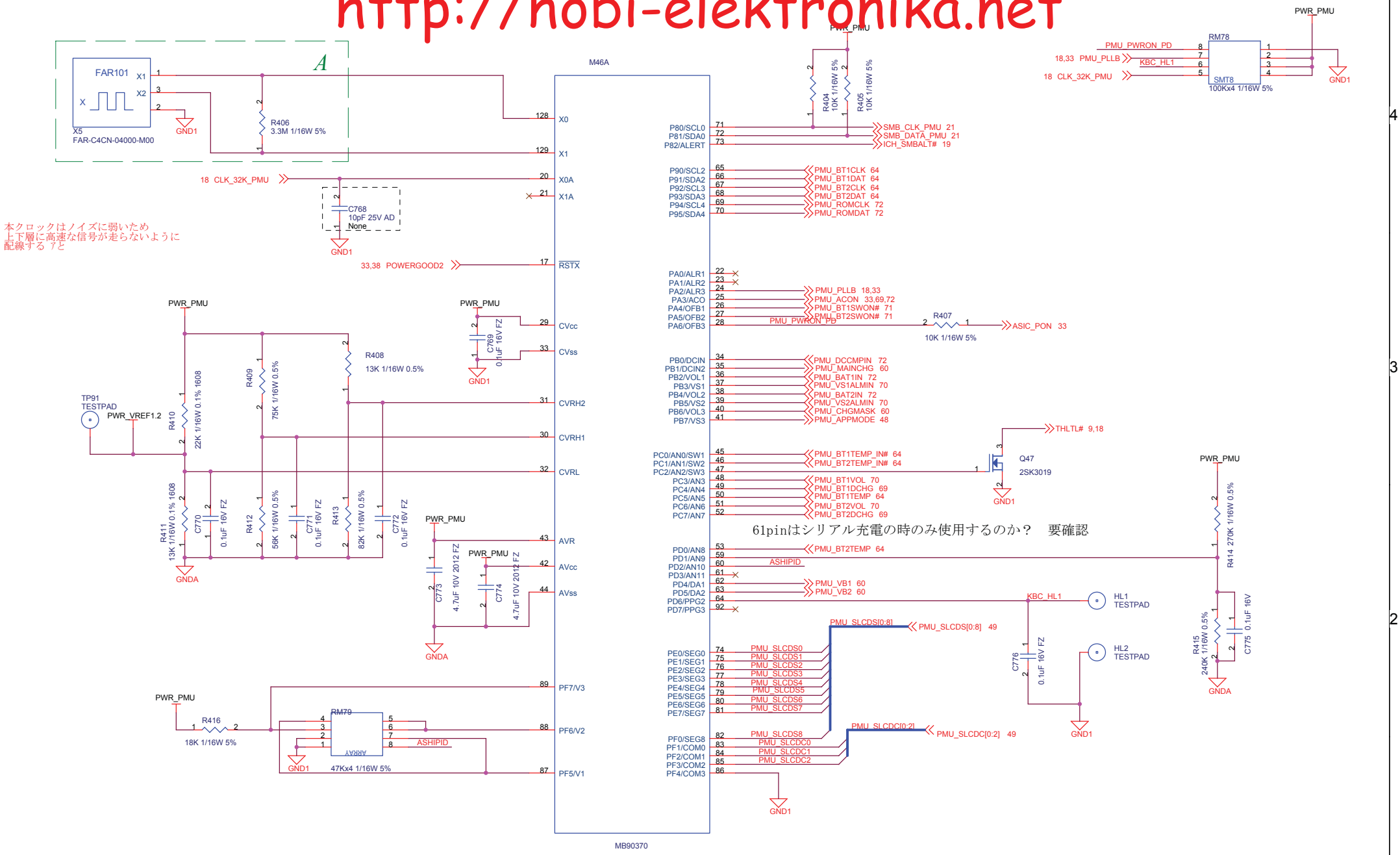
Rev.	Date	Design	Check	Appr.	Description		
Design	02/05/07	Konaka	Check	Fuchida	Appr. Fukuyo	FUJITSU LTD.	Sheet 66 / 73



Power/ PMU/ LUNA1

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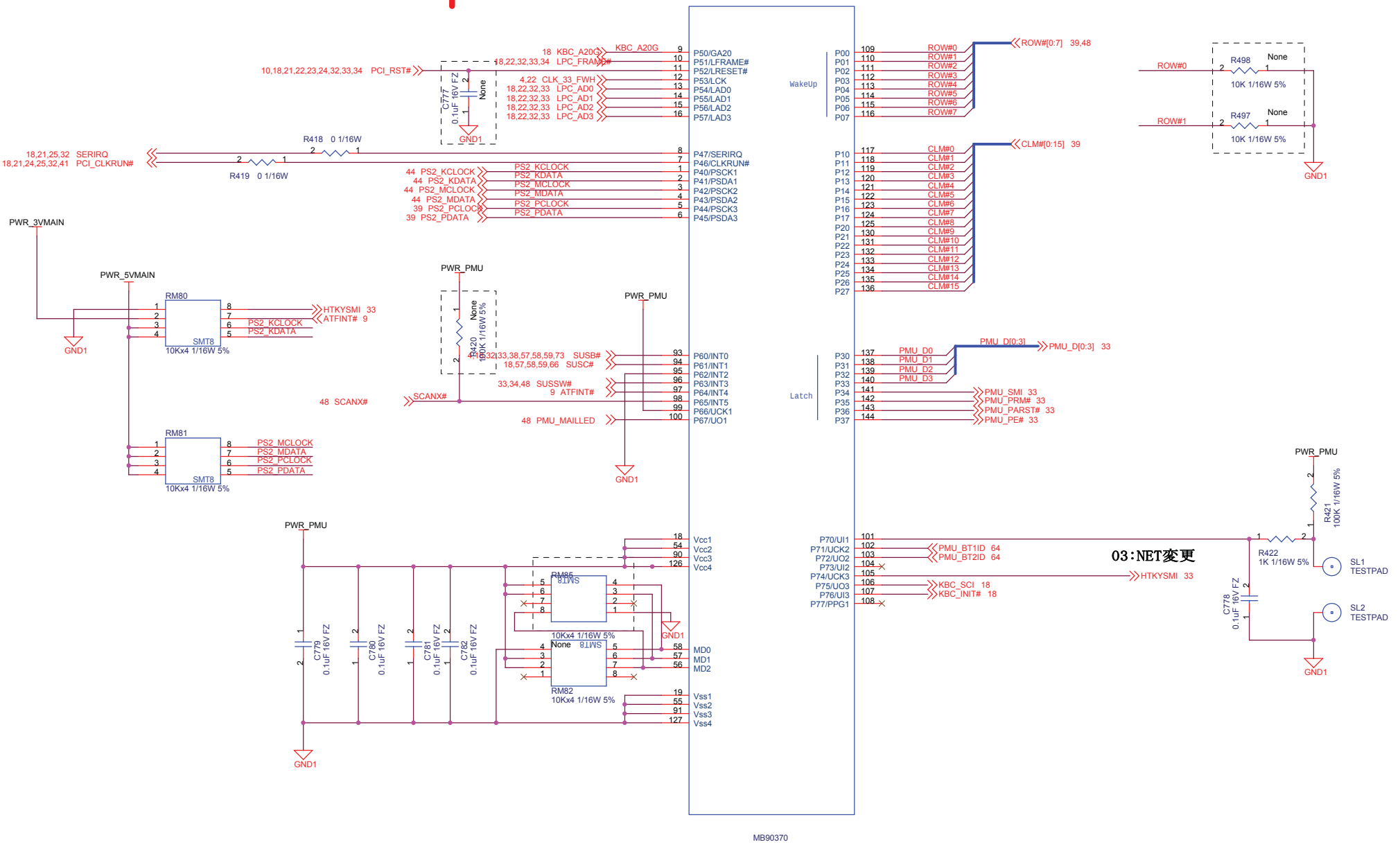

本ページの抵抗・コンデンサはM38867付近に配置すること。
パスコンについてはM38867の電源ピンに対して均等になるように配置分散し、
電源ピンまでのリード長を最大限短くなるようレイアウトすること。

Power/ PMU/ LUNA2

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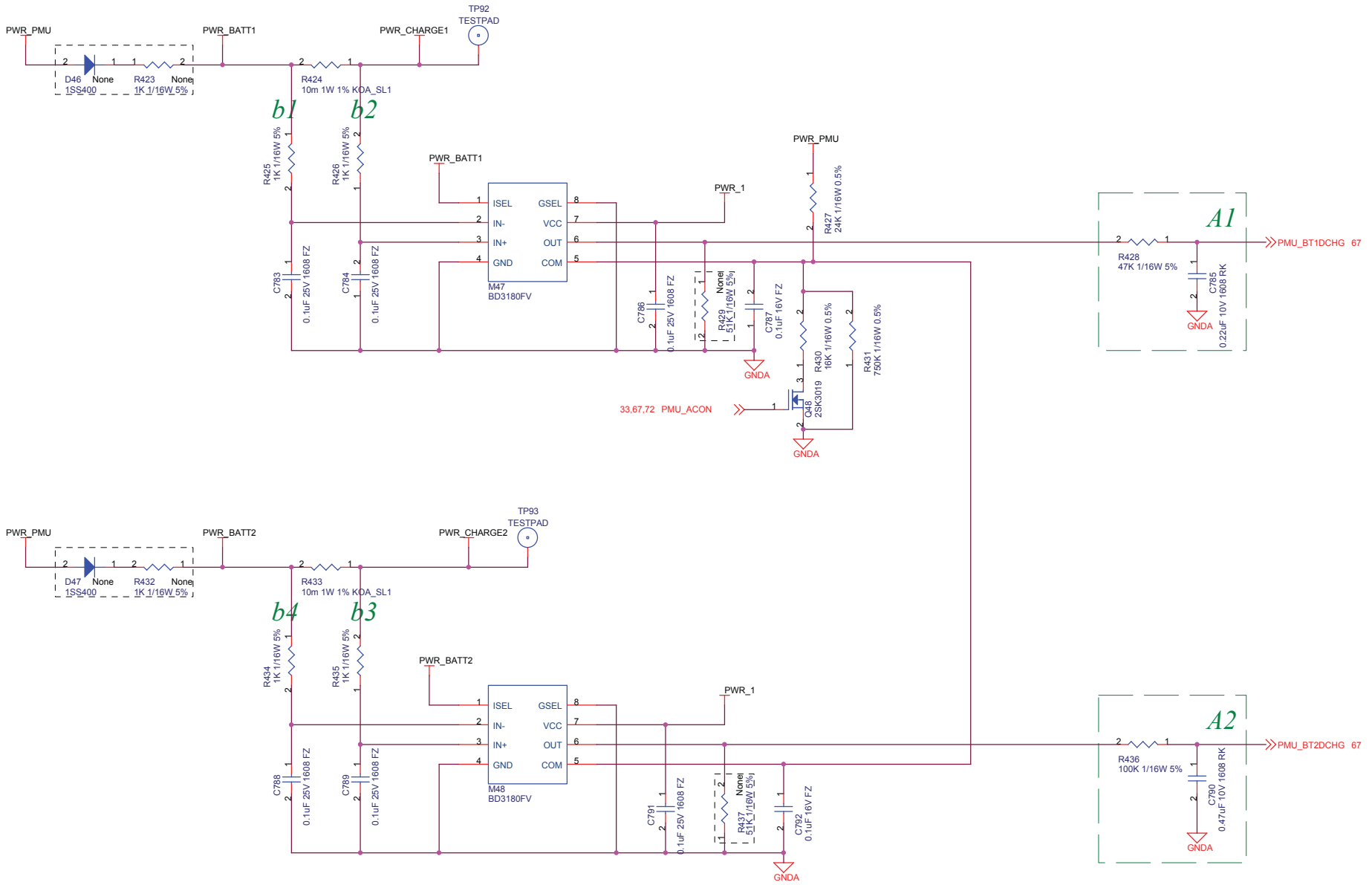

Power/ PMU/ AmMeter

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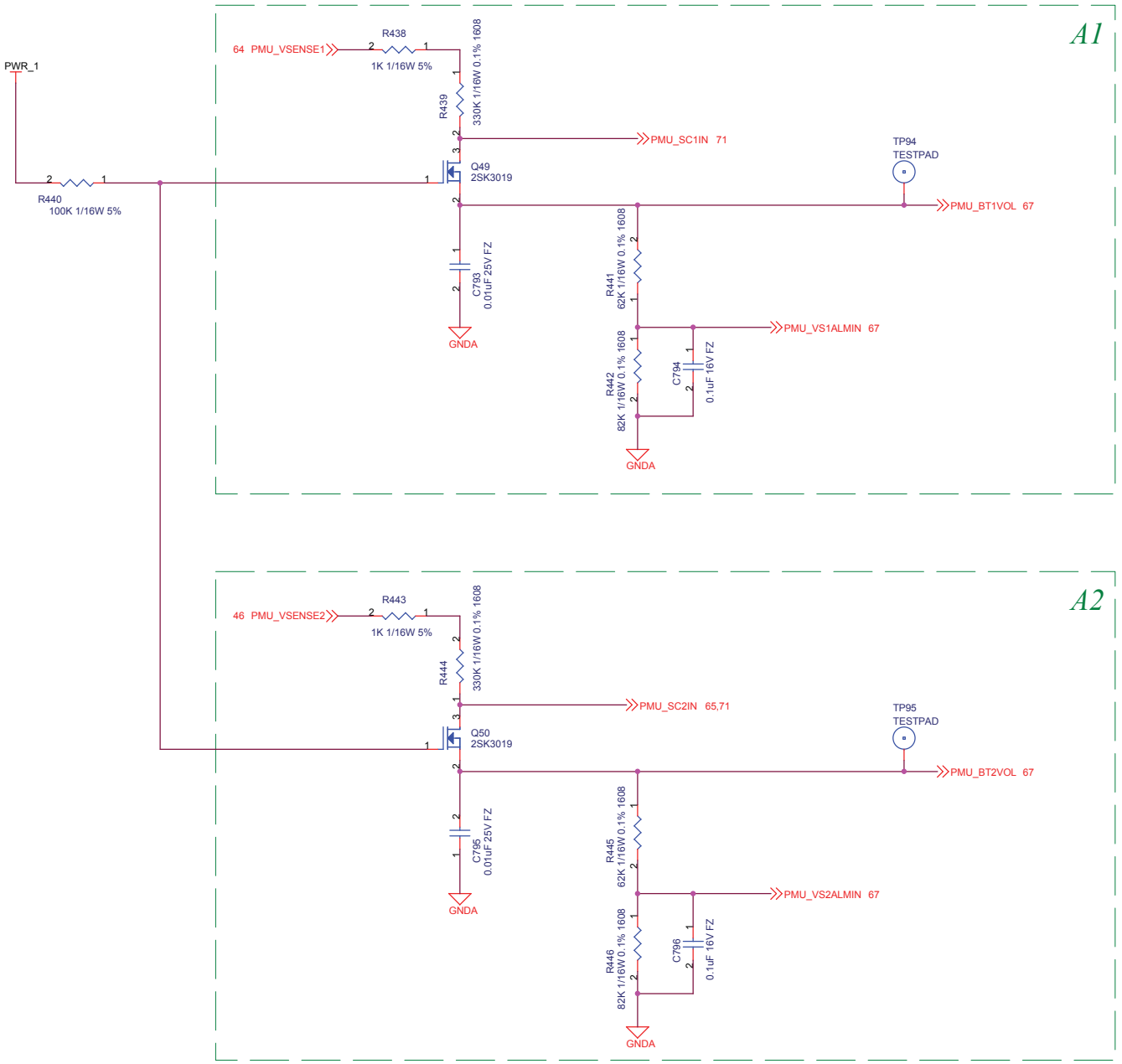

Power/ PMU/ VolMeter

Rev.	Date	Design	Check	Appr.	Description				
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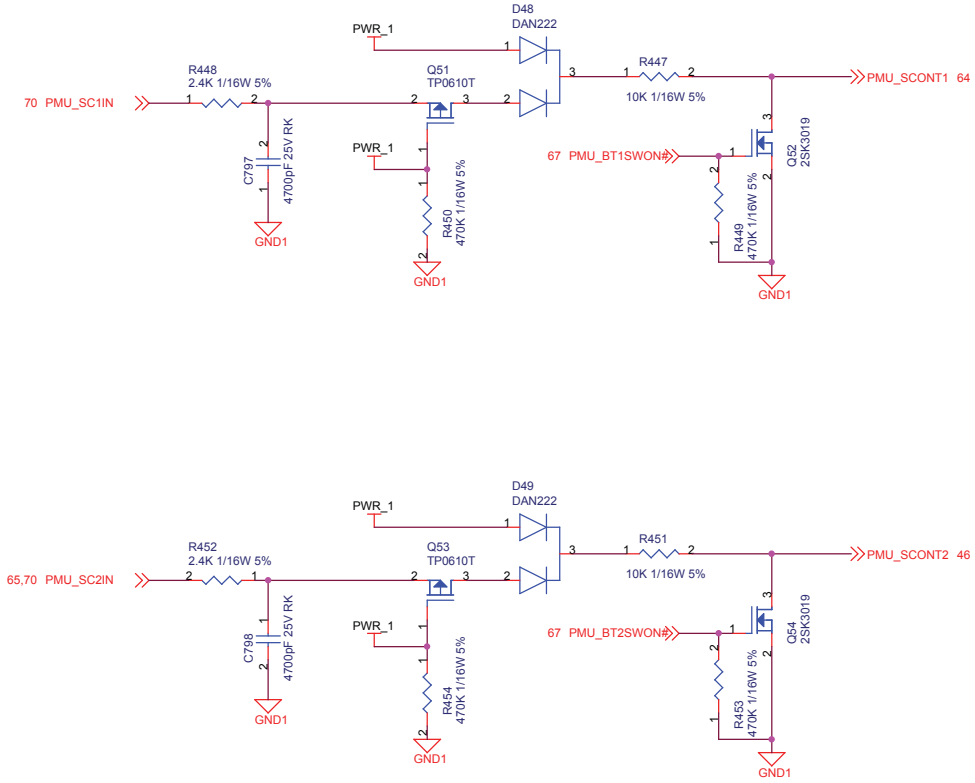

Power/ PMU/ Scont

Rev.	Date	Design	Check	Appr.	Description				
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TITLE: VB161AX MAIN

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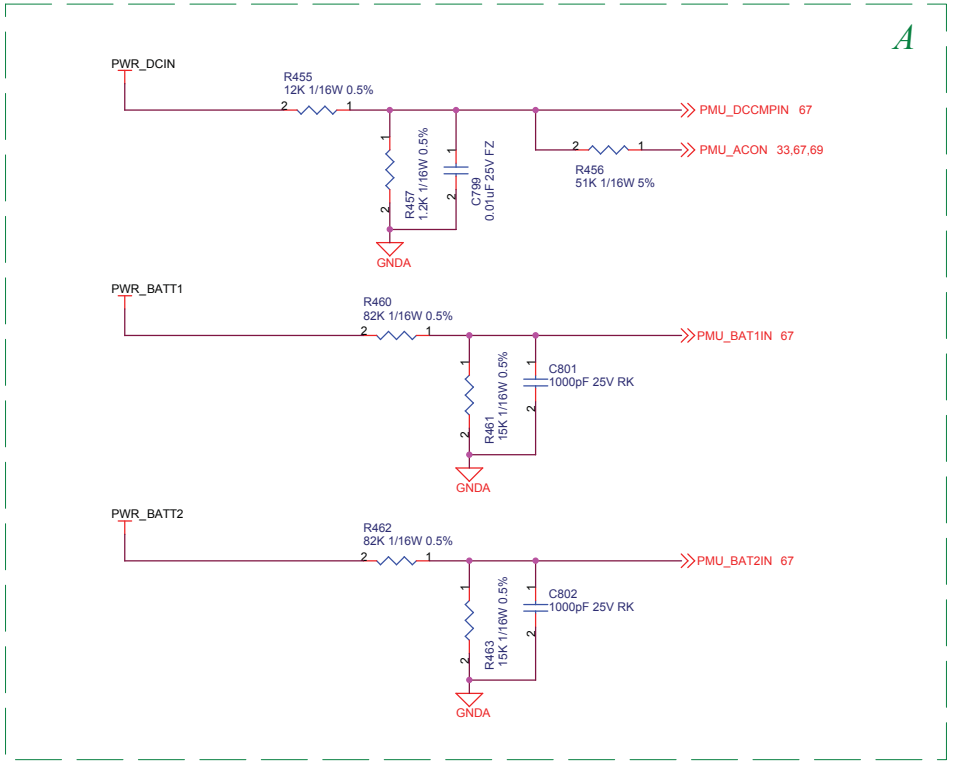

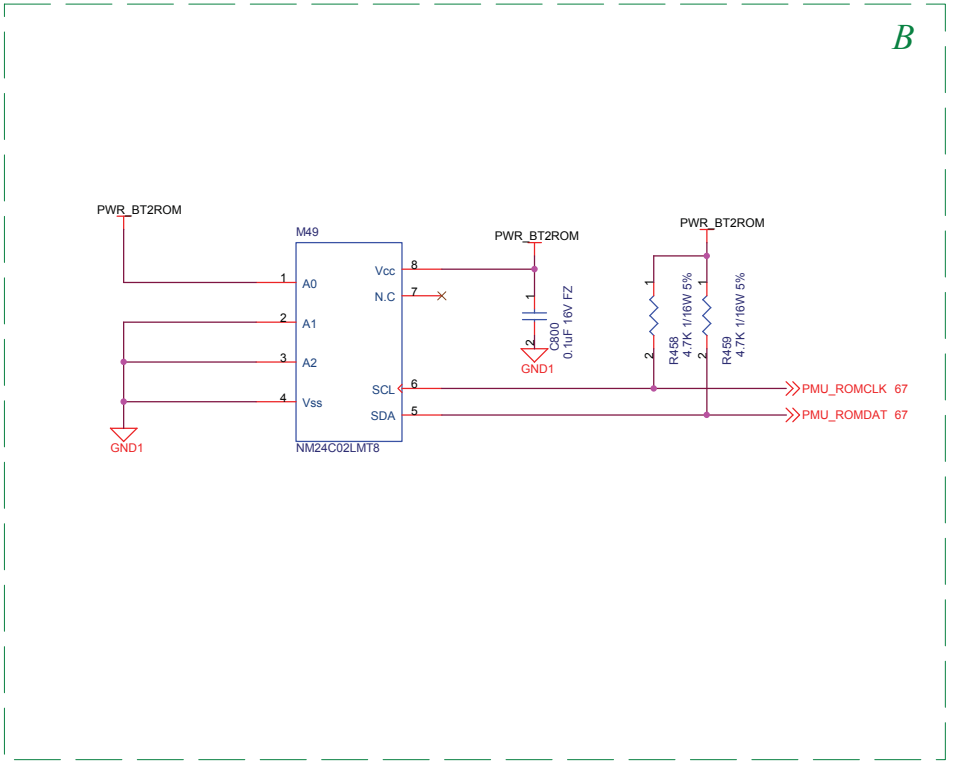

Power/ PMU/ Etc1

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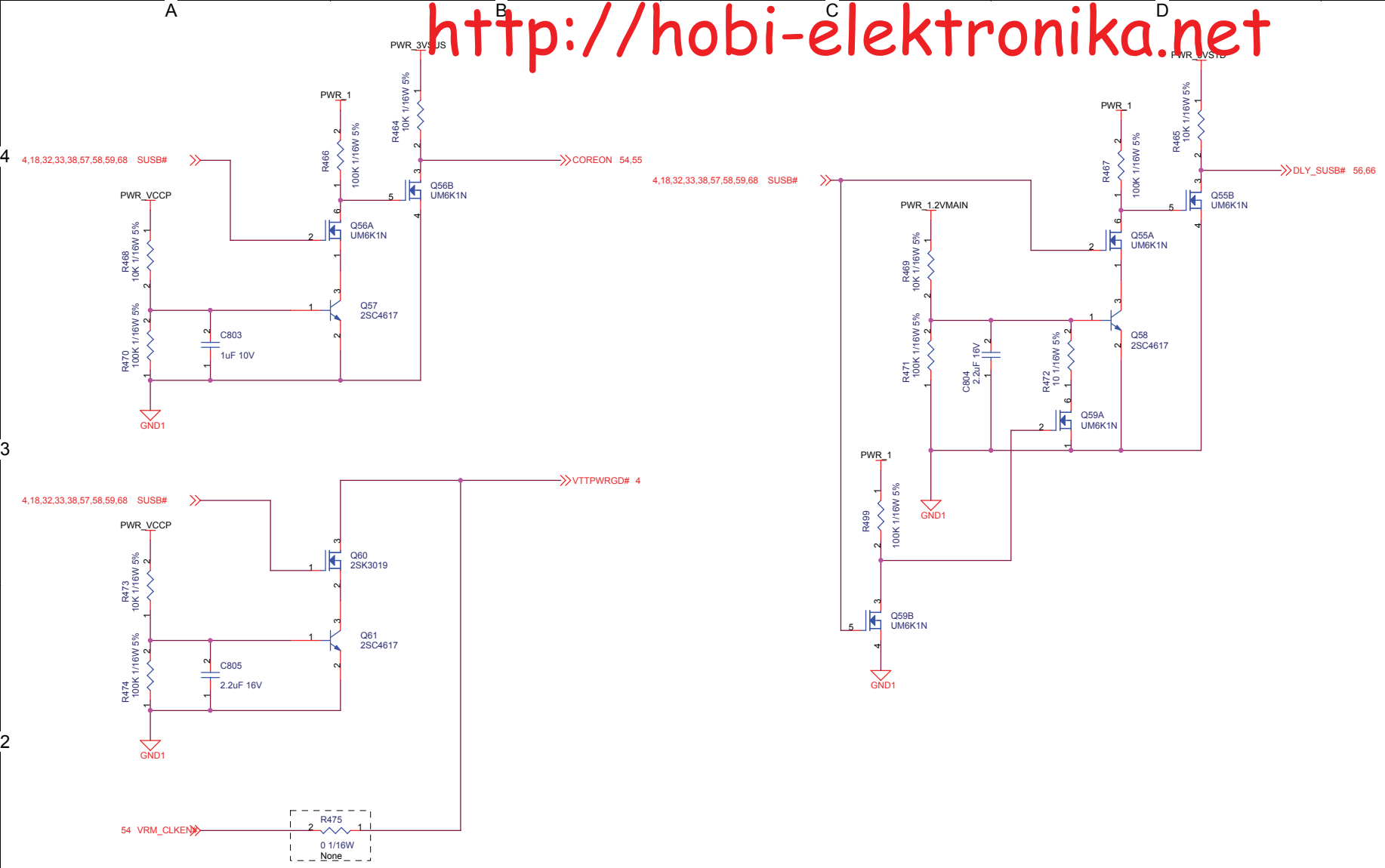

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