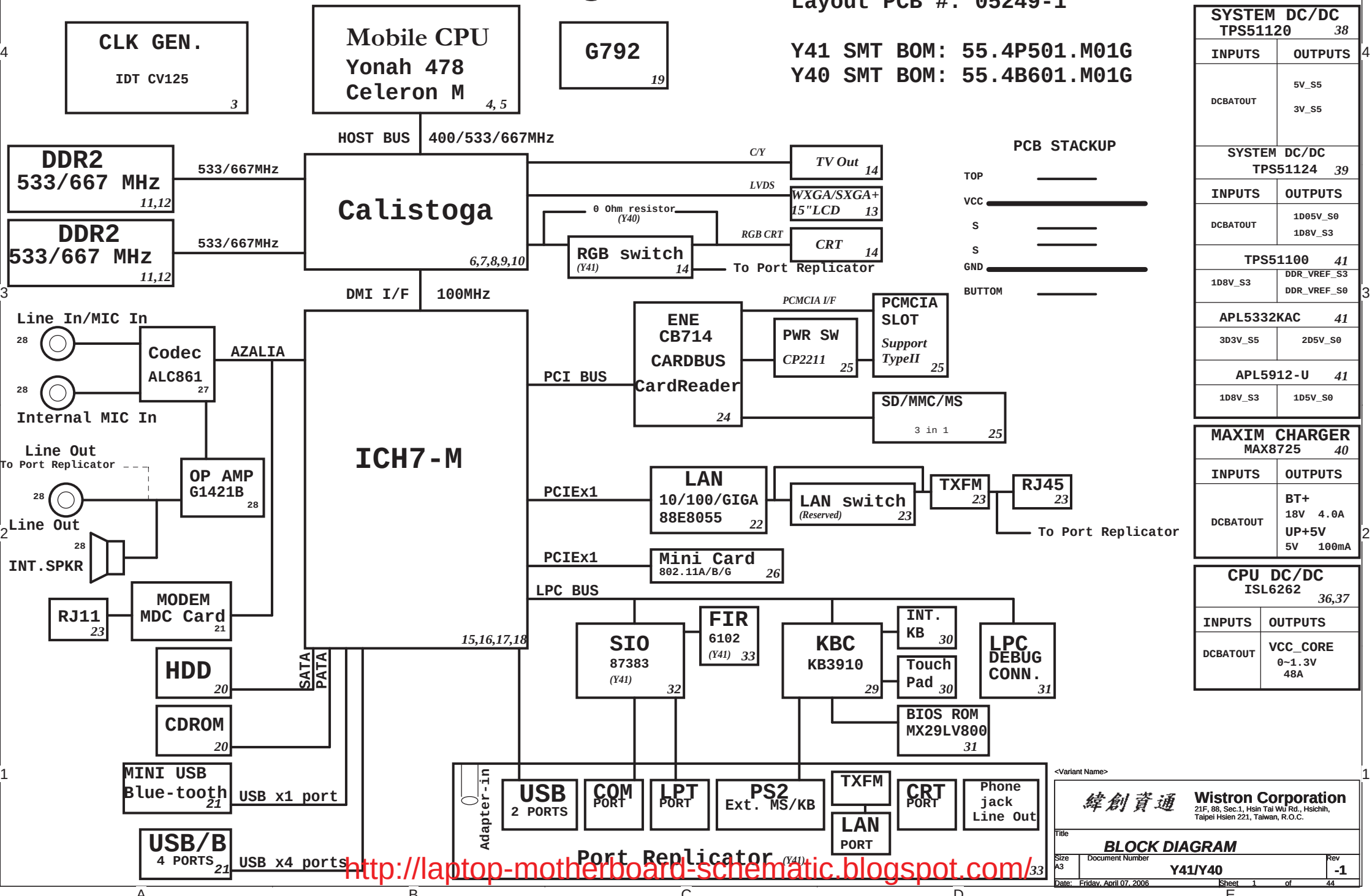
Y41/Y40 Block Diagram

Project code: 91.4P501.001
PCB P/N : 48.4P501.011
Layout PCB #: 05249-1

Y41 SMT BOM: 55.4P501.M01G
Y40 SMT BOM: 55.4B601.M01G



SYSTEM DC/DC TPS51120 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC TPS51124 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 41	
1D8V_S3	DDR_VREF_S3 DDR_VREF_S0

APL5332KAC 41	
3D3V_S5	2D5V_S0

APL5912-U 41	
1D8V_S3	1D5V_S0

MAXIM CHARGER MAX8725 40	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 36,37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Friday, April 07, 2006 Sheet 1 of 44

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 24

	IDSEL	INT -> PIRQ	REQ/GNT
CB714	22	A->G, B->E,	0

Device SSID/SVID

Device	SSID	SVID
LAN 88E8055	10C1	1734
Codec ALC861	10C1	1734

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

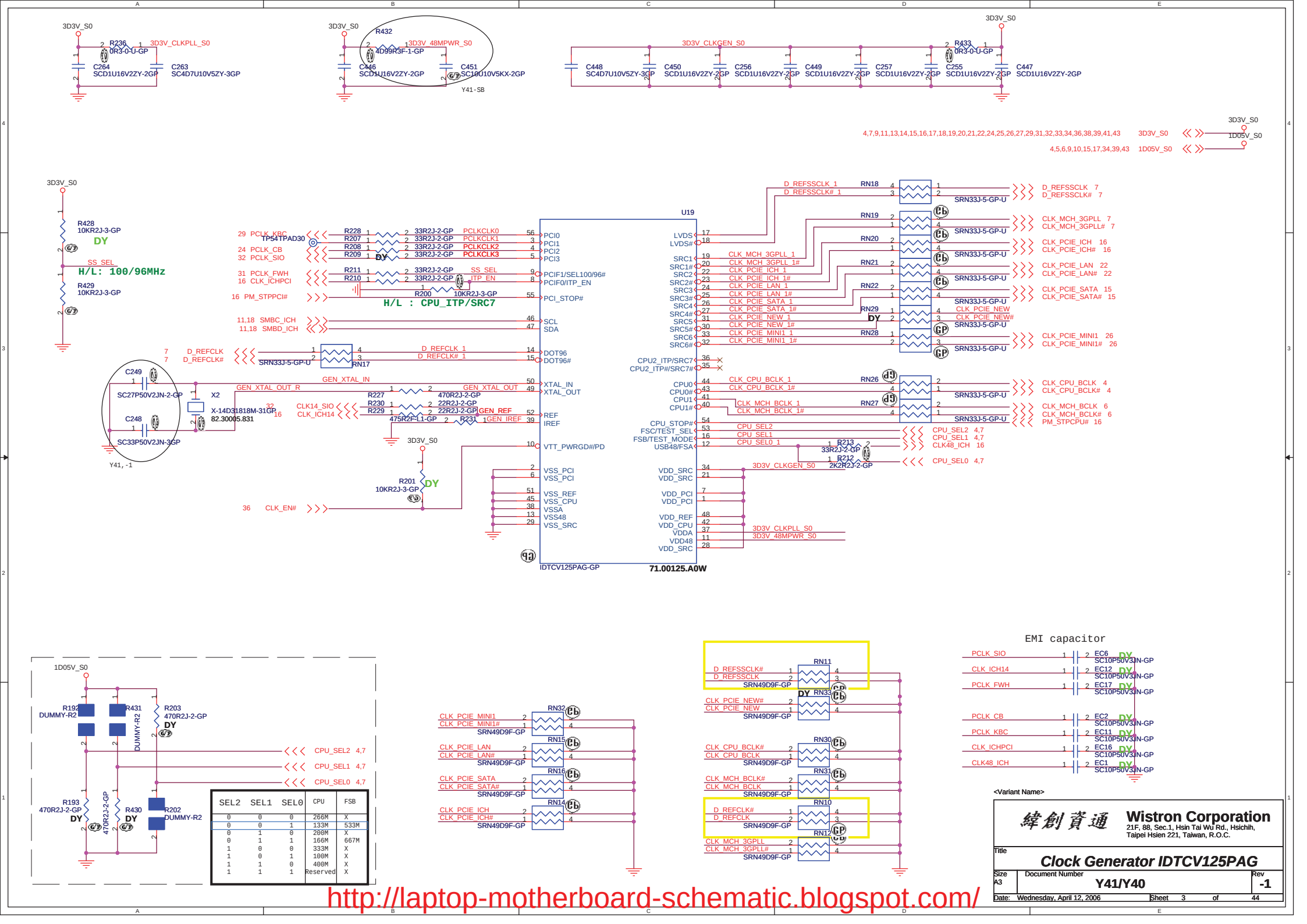
<Variant Name>

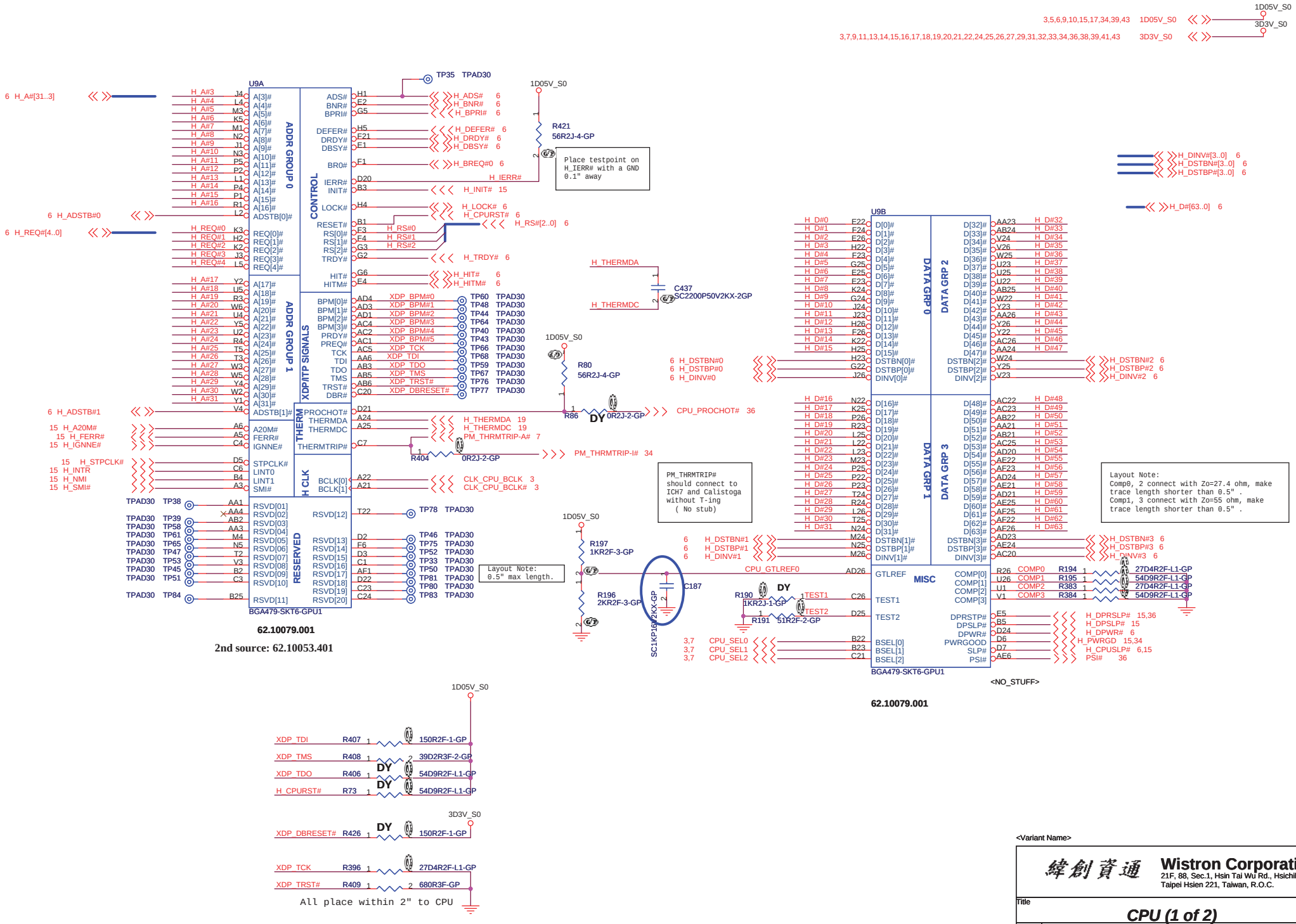
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Friday, April 07, 2006 | Sheet 2 of 44





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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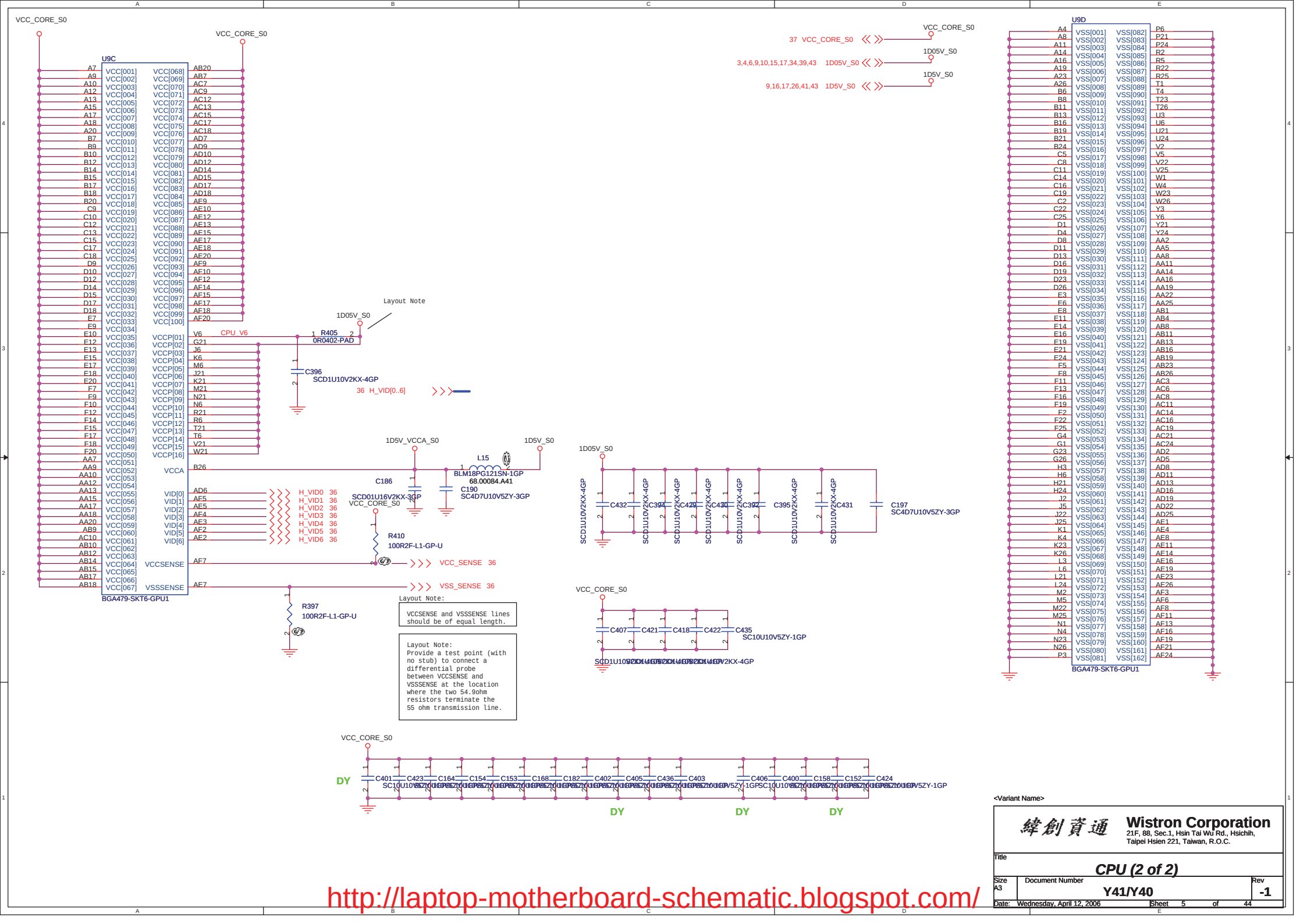
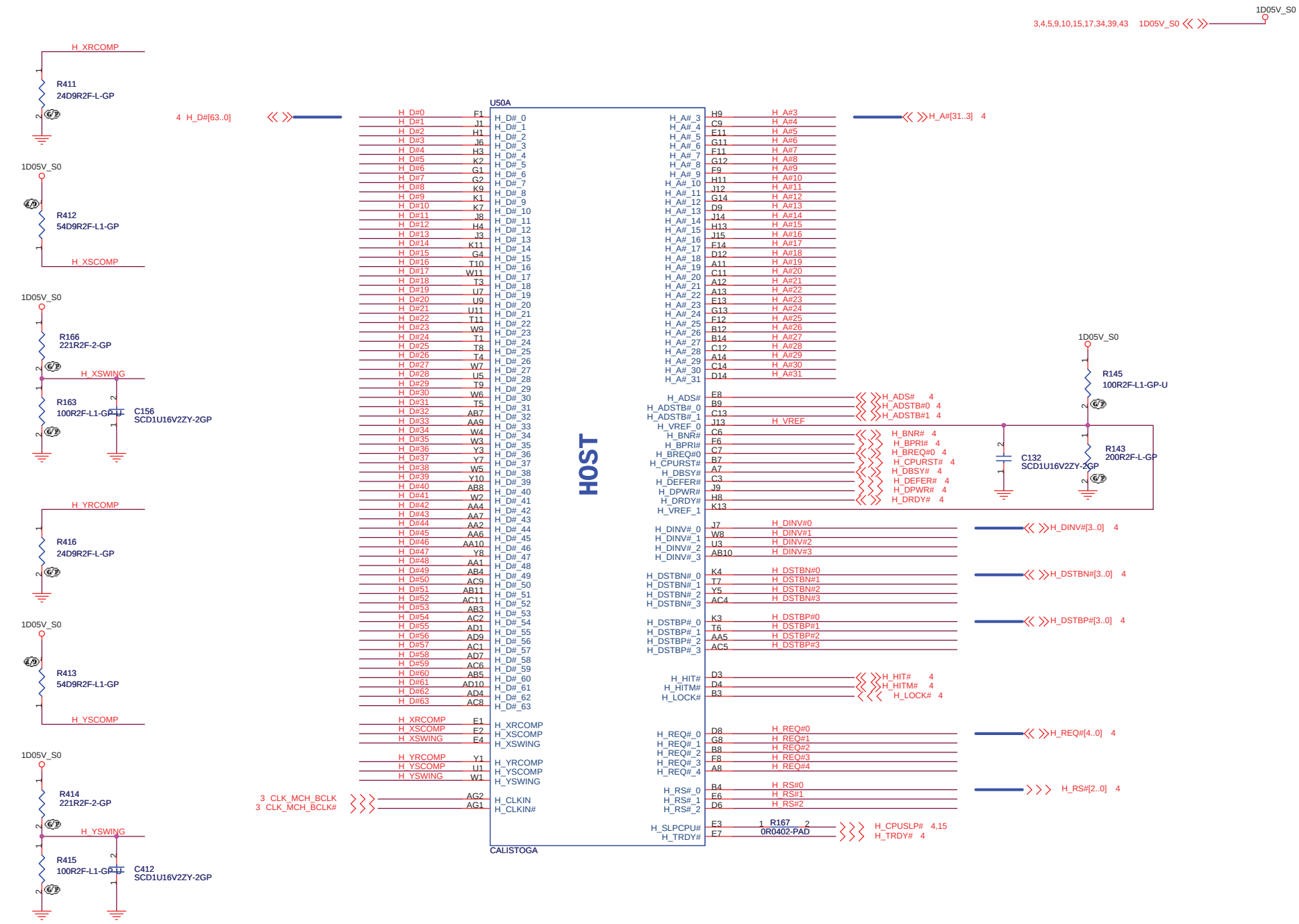
Title: CPU (1 of 2)

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 4 of 44





Place them near to the chip (< 0.5")

<Variant Name>

緯創資通 **Wistron Corporation**
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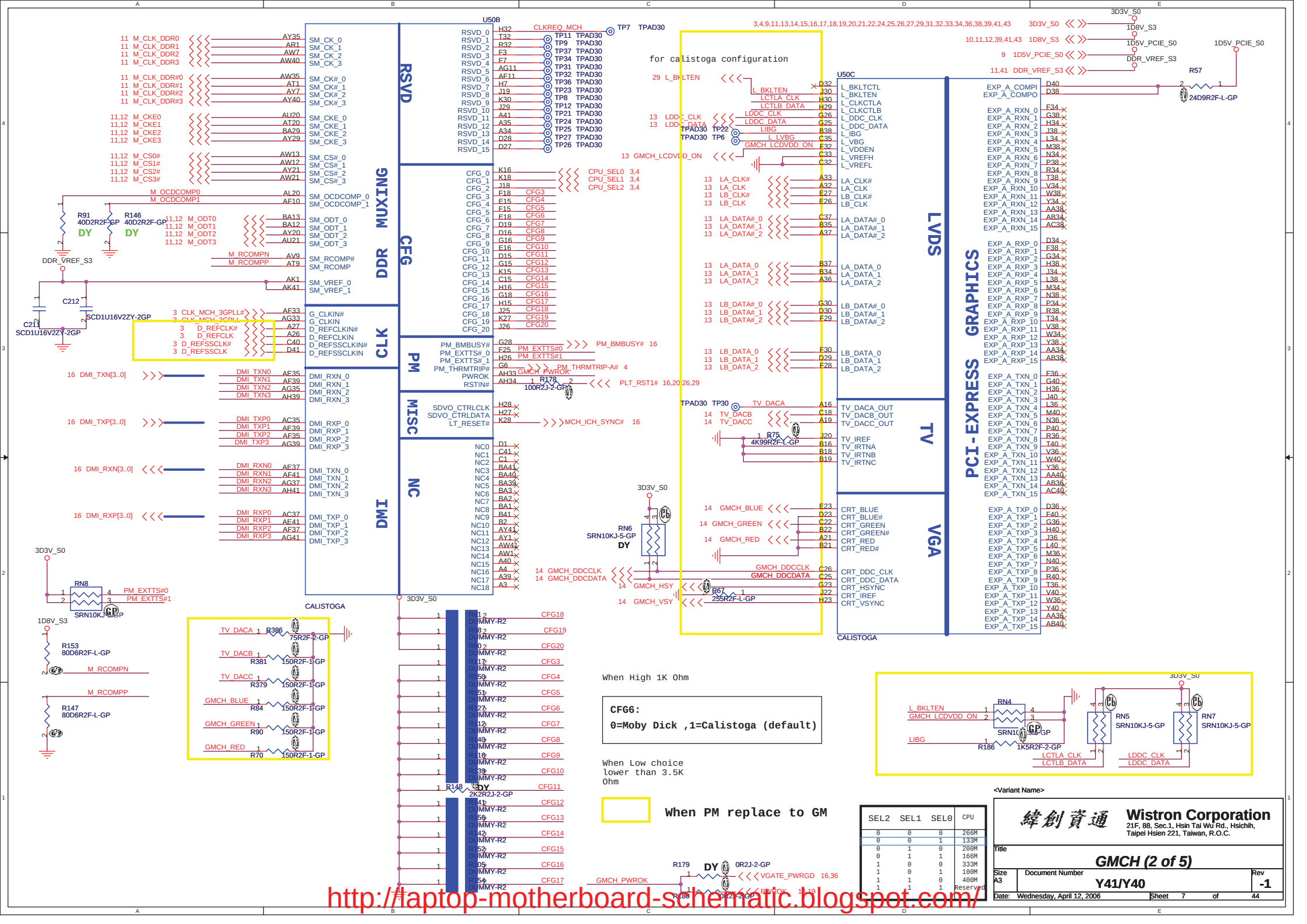
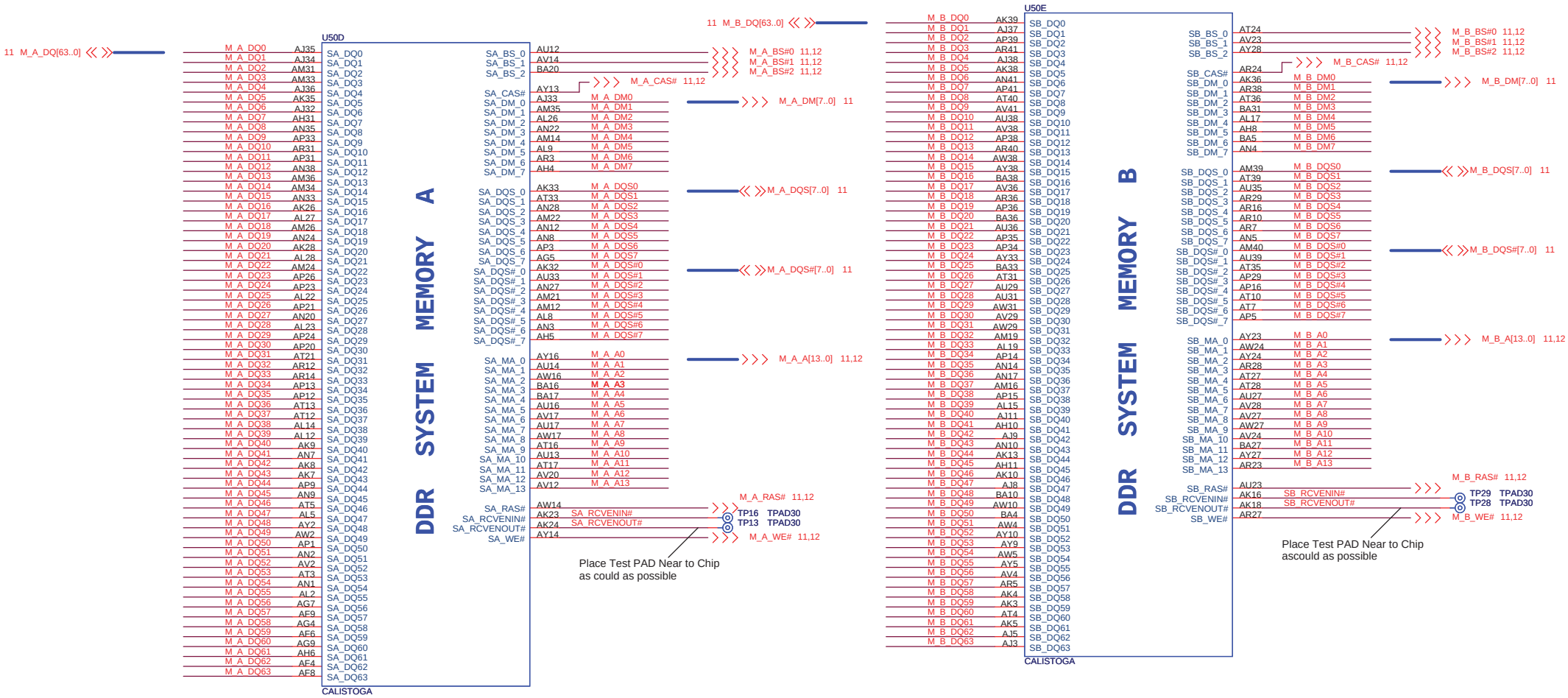
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 6 of 44


RSVD
DDR MUXING
CFG
CLK
PM
MISC
NC
DMI
U50B
U50C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
for calistoga configuration
When High 1K Ohm
CFG6:
0=Moby Dick ,1=Calistoga (default)
When Low choice lower than 3.5K Ohm
When PM replace to GM
SEL2 SEL1 SEL0 CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 7 of 44
<Variant Name>
http://laptop-motherboard-schematic.blogspot.com/



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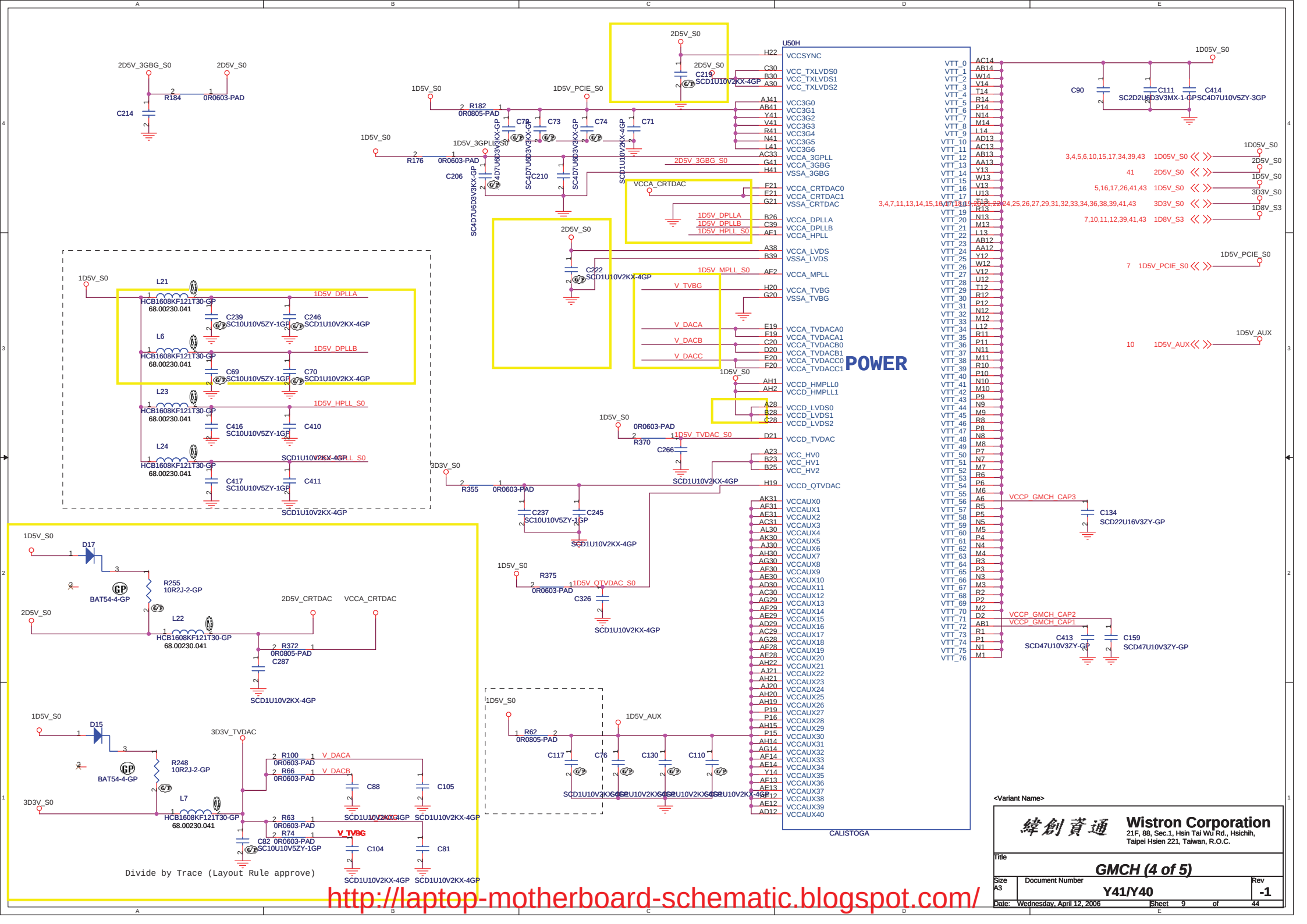
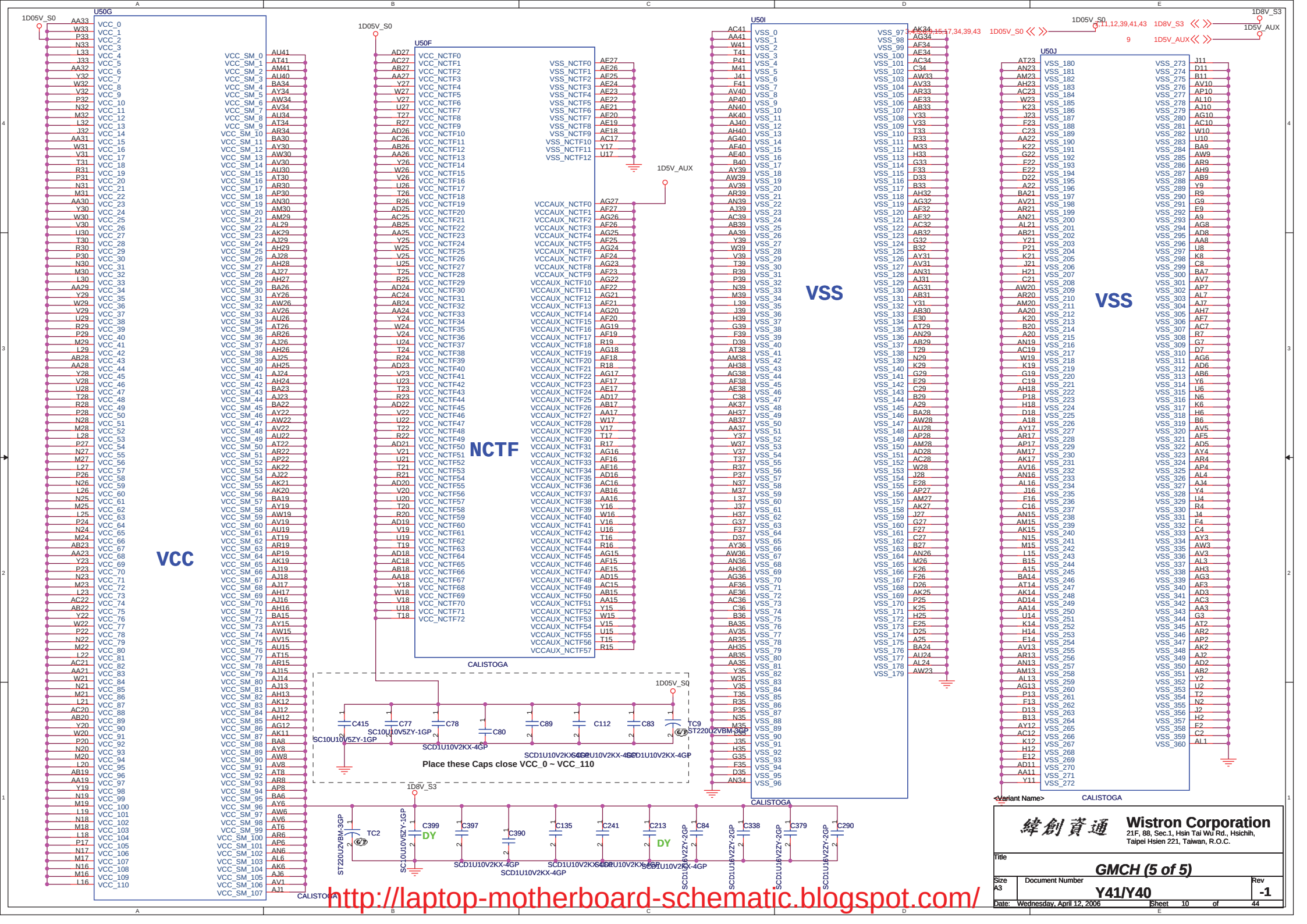
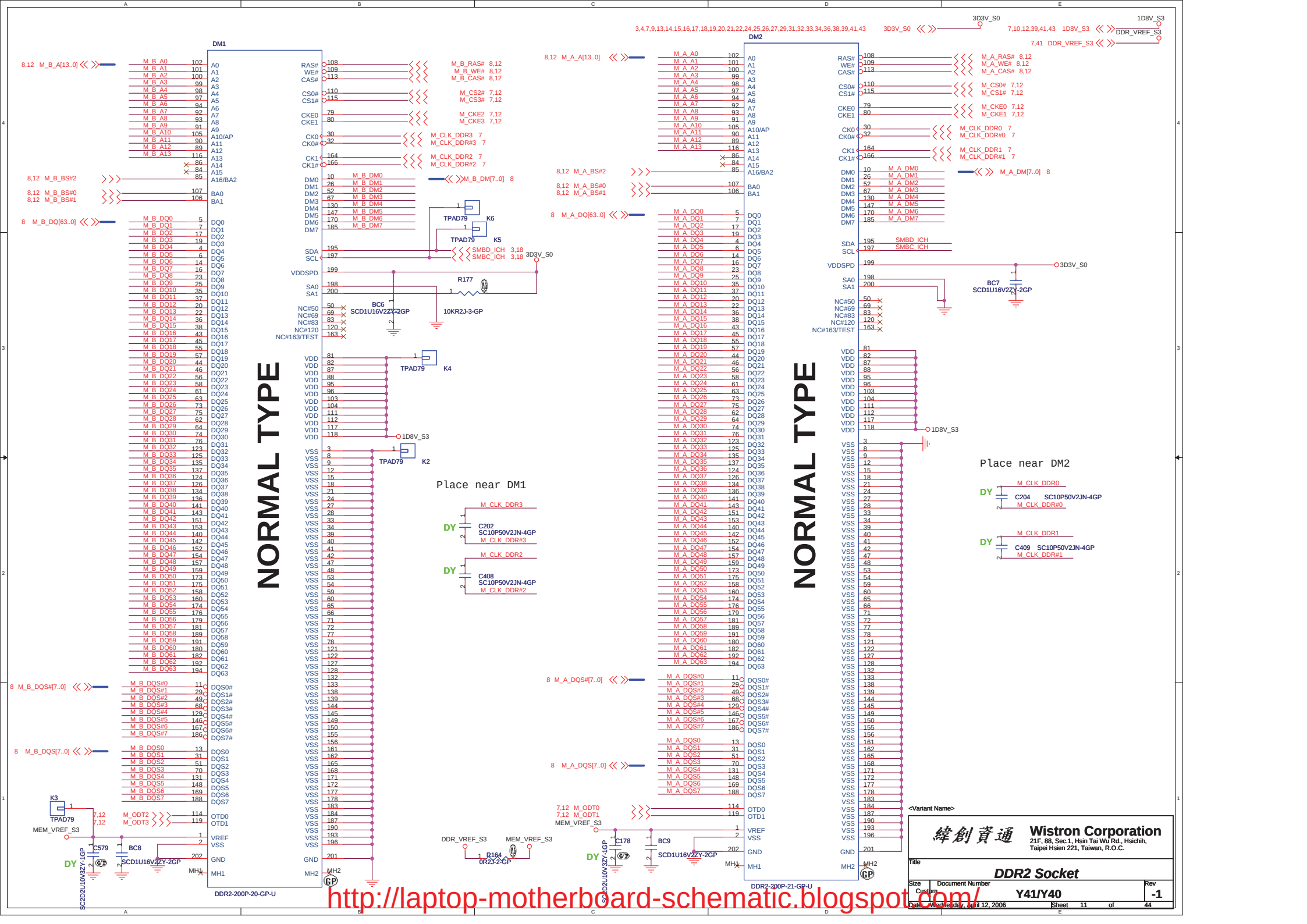
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GMCH (3 of 5)***	
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 8 of 44	


U50H
CALISTOGA
POWER
2D5V_S0
1D5V_S0
3D3V_S0
1D05V_S0
1D5V_PCIE_S0
1D5V_AUX
1D8V_S3
2D5V_3GBG_S0
1D5V_3GPLL_S0
VCCA_CRTDAC
1D5V_DPLLA
1D5V_DPLLB
1D5V_HPLL_S0
1D5V_MPLL_S0
V_TVBG
V_DACA
V_DACB
V_DACC
1D5V_TVDAC_S0
1D5V_QTVDAC_S0
3D3V_TVDAC
2D5V_CRTDAC
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
Divide by Trace (Layout Rule approve)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size A3
Document Number
Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 9 of 44
http://laptop-motherboard-schematic.blogspot.com/





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Socket

Size: Custom | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 11 of 44

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN13 SRN56J-5-GP
- M_CKE2 7,11
- M_B_BS#2 8,11
- M_B_A12
- M_B_A9

M_A_A[13..0] 8,11

M_B_A[13..0] 8,11

R389 56R2J-4-GP
R387 56R2J-4-GP
R367 56R2J-4-GP M_A_A9
R368 56R2J-4-GP M_B_A8
- M_ODT1 7,11
- M_ODT3 7,11

RN42 SRN56J-5-GP
- M_B_A5
- M_B_A3
- M_B_A1
- M_B_A10

RN48 SRN56J-5-GP
- M_B_A13
- M_ODT2 7,11
- M_CS2# 7,11
- M_B_RAS# 8,11

RN44 SRN56J-5-GP
- M_B_BS#1 8,11
- M_B_A0
- M_B_A2
- M_B_A4

RN41 SRN56J-5-GP
- M_B_A6
- M_B_A7
- M_B_A11
- M_CKE3 7,11

RN46 SRN56J-5-GP
- M_B_BS#0 8,11
- M_B_WE# 8,11
- M_CS3# 7,11
- M_B_CAS# 8,11

RN47 SRN56J-5-GP
- M_A_A13
- M_ODT0 7,11
- M_CS0# 7,11
- M_A_RAS# 8,11

RN43 SRN56J-5-GP
- M_A_BS#1 8,11
- M_A_A0
- M_A_A2
- M_A_A4

RN49 SRN56J-5-GP
- M_A_BS#0 8,11
- M_A_WE# 8,11
- M_A_CAS# 8,11
- M_CS1# 7,11

RN40 SRN56J-5-GP
- M_CKE0 7,11
- M_A_BS#2 8,11
- M_A_A12
- M_A_A8

RN25 SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11
- M_CKE1 7,11

RN45 SRN56J-5-GP
- M_A_A5
- M_A_A3
- M_A_A1
- M_A_A10

Decoupling Capacitor

1D8V_S3
- 7,10,11,39,41,43 1D8V_S3
- DDR_VREF_S0
- 41,43 DDR_VREF_S0

DDR_VREF_S0

Put decap near power(0.9V) and pull-up resistor

C216 SCD1U16V2ZY-2GP DY
C228 SCD1U16V2ZY-2GP
C223 SCD1U16V2ZY-2GP
C384 SCD1U16V2ZY-2GP
C231 SCD1U16V2ZY-2GP
C294 SCD1U16V2ZY-2GP
C296 SCD1U16V2ZY-2GP DY
C385 SCD1U16V2ZY-2GP
C252 SCD1U16V2ZY-2GP
C375 SCD1U16V2ZY-2GP
C240 SCD1U16V2ZY-2GP

C229 SCD1U16V2ZY-2GP DY
C382 SCD1U16V2ZY-2GP
C377 SCD1U16V2ZY-2GP
C227 SCD1U16V2ZY-2GP
C361 SCD1U16V2ZY-2GP
C220 SCD1U16V2ZY-2GP
C224 SCD1U16V2ZY-2GP
C371 SCD1U16V2ZY-2GP DY
C226 SCD1U16V2ZY-2GP
C230 SCD1U16V2ZY-2GP
C254 SCD1U16V2ZY-2GP

1D8V_S3

Place these Caps near DM1

C86 SC2D2U6D3V3MX-1-GP
C92 SC2D2U6D3V3MX-1-GP
C108 SC2D2U6D3V3MX-1-GP
C123 SC2D2U6D3V3MX-1-GP
C131 SC2D2U6D3V3MX-1-GP

C267 SCD1U16V2ZY-2GP DY
C247 SCD1U16V2ZY-2GP DY
C383 SCD1U16V2ZY-2GP DY
C324 SCD1U16V2ZY-2GP

1D8V_S3

Place these Caps near DM2

C116 SC2D2U6D3V3MX-1-GP
C79 SC2D2U6D3V3MX-1-GP
C133 SC2D2U6D3V3MX-1-GP
C96 SC2D2U6D3V3MX-1-GP
C85 SC2D2U6D3V3MX-1-GP

C308 SCD1U16V2ZY-2GP DY
C253 SCD1U16V2ZY-2GP DY
C376 SCD1U16V2ZY-2GP DY
C381 SCD1U16V2ZY-2GP

<Variant Name>

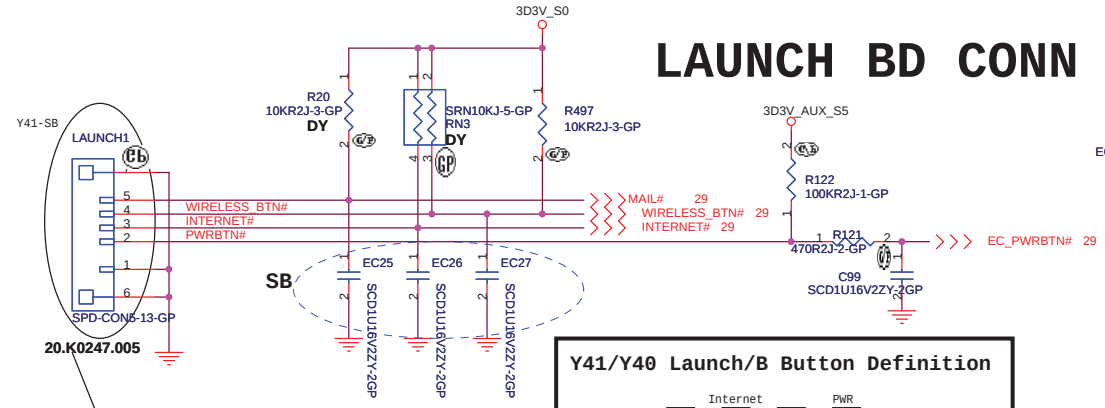
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size: A3 | Document Number: Y41/Y40 | Rev: -1

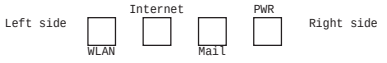
Date: Wednesday, April 12, 2006 | Sheet 12 of 44

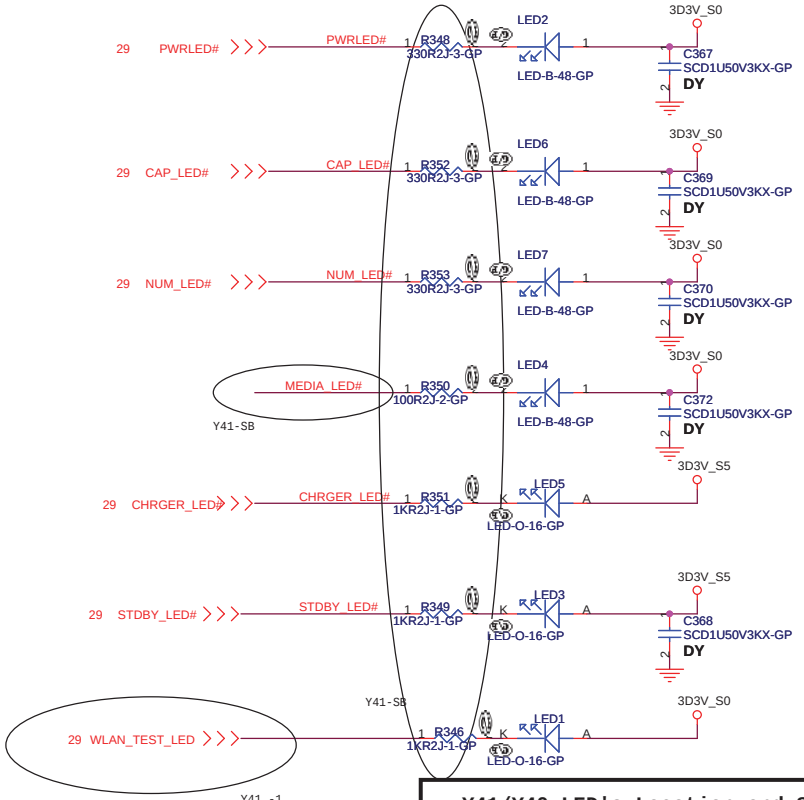
LAUNCH BD CONN



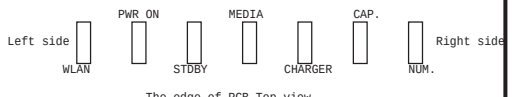
The pin1 of M/B side connects
the pin5 of Launch/B side.

Y41/Y40 Launch/B Button Definition

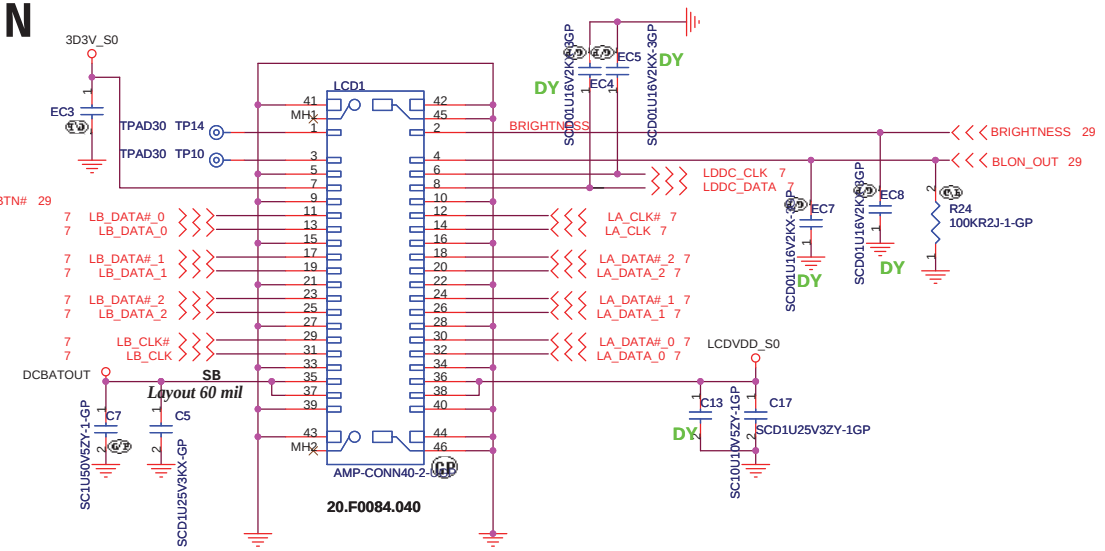


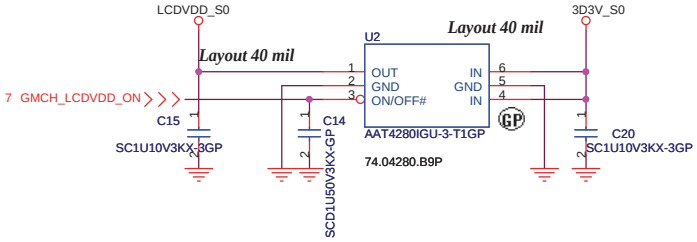


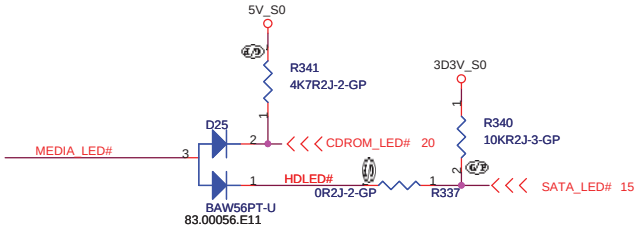
Y41/Y40 LED's Location and Sequence

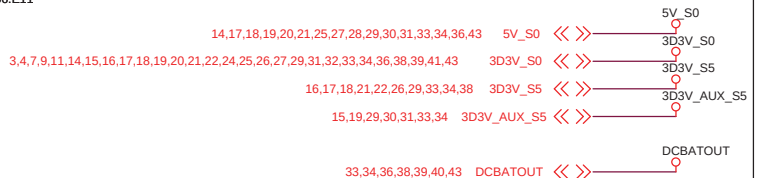


LCD/INVERTER









<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD / LAUNCH / LEDs

Size: Custom | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 13 of 44

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

CRT_RED_SYS
CRT_GREEN_SYS
CRT_BLUE_SYS
R183 150R2F-1-GP
R181 150R2F-1-GP
R171 150R2F-1-GP
L30 FCB1608CF-GP
L27 FCB1608CF-GP
L31 FCB1608CF-GP
L28 FCB1608CF-GP
L32 FCB1608CF-GP
L29 FCB1608CF-GP
C565 SC1D8P50V2CC-GP
C566 SC1D8P50V2CC-GP
C567 SC1D8P50V2CC-GP
C184 SC1D8P50V2CC-GP
C180 SC1D8P50V2CC-GP
C169 SC1D8P50V2CC-GP
CRT_R
CRT_G
CRT_B

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V_S0
D18 CH751H-40PT
RN50 SRN4K7J-8-GP
C420 SCD01U16V2KX-3GP
5V_CRT_S0
CRT1
VIDEO-15-42-GP-U
20.20378.015
C419 SC100P50V2JN-3GP
C147 SC22P50V2JN-4GP
C404 SC100P50V2JN-3GP
C155 SC22P50V2JN-4GP
DAT_DDC1_5
JVGA_HS
JVGA_VS
CLK_DDC1_5

Hsync & Vsync level shift

33 GMCH_HSY_DOCK
7 GMCH_HSY
7 GMCH_VSY
33 GMCH_VSY_DOCK
R160 0R2J-2-GP Y40_DY
R159 47R2J-2-GP
R158 47R2J-2-GP
R157 0R2J-2-GP Y40_DY
HSYNC_4
VSYNC_4
U10A
U10B
TSAHCT125PW-GP
CRT_HSYNC1
CRT_VSYNC1
R162 0R2J-2-GP
R161 0R2J-2-GP
JVGA_HS
JVGA_VS
C160 SCD1U16V2ZY-2GP

For System CRT

DDC_CLK & DATA level shift

3D3V_S0
RN51 SRN4K7J-8-GP
Y41,-1
Y41-SB
7 GMCH_DDCDATA
7 GMCH_DDCCLK
R498 0R2J-2-GP Y40_DY DAT_DDC1_5
R499 0R2J-2-GP Y40_DY CLK_DDC1_5
GMCH_DDCDATA_DOCK 33
GMCH_DDCCLK_DOCK 33
2SK3019-N-2GP Q28
2SK3019-N-2GP Q27

23,29,33 DOCK_IN#
R241 2K2R2F-GP
Q26 DTC115EE-2-GP
Q25 DTC115EE-2-GP
R187 4K7R2F-GP
VGA_SYS_ON#
U47 U49 U48 SNCB3Q3306APWRGP
C576 C577 C578 SCD1U16V2ZY-2GP
R294 R289 R328 0R2J-2-GP
CRT_RED_SYS
CRT_GREEN_SYS
CRT_BLUE_SYS
GMCH_RED
GMCH_GREEN
GMCH_BLUE
CRT_RED_DOCK 33
CRT_GREEN_DOCK 33
CRT_BLUE_DOCK 33

TV OUT CONN

7 TV_DACC
7 TV_DACB
C193 SC33P50V3JN-GP
C243 SC33P50V3JN-GP
L16 MLB201209-0150A-GP
L18 MLB201209-0150A-GP
R204 150R2F-1-GP
R226 150R2F-1-GP
C200 SC6P50V2CN-1GP
C205 SC6P50V2CN-1GP
C238 SC6P50V2CN-1GP
C217 SC6P50V2CN-1GP
CRMA_1
LUMA_1
TVOUT1
MINDIN4-29-GP
Reverse type

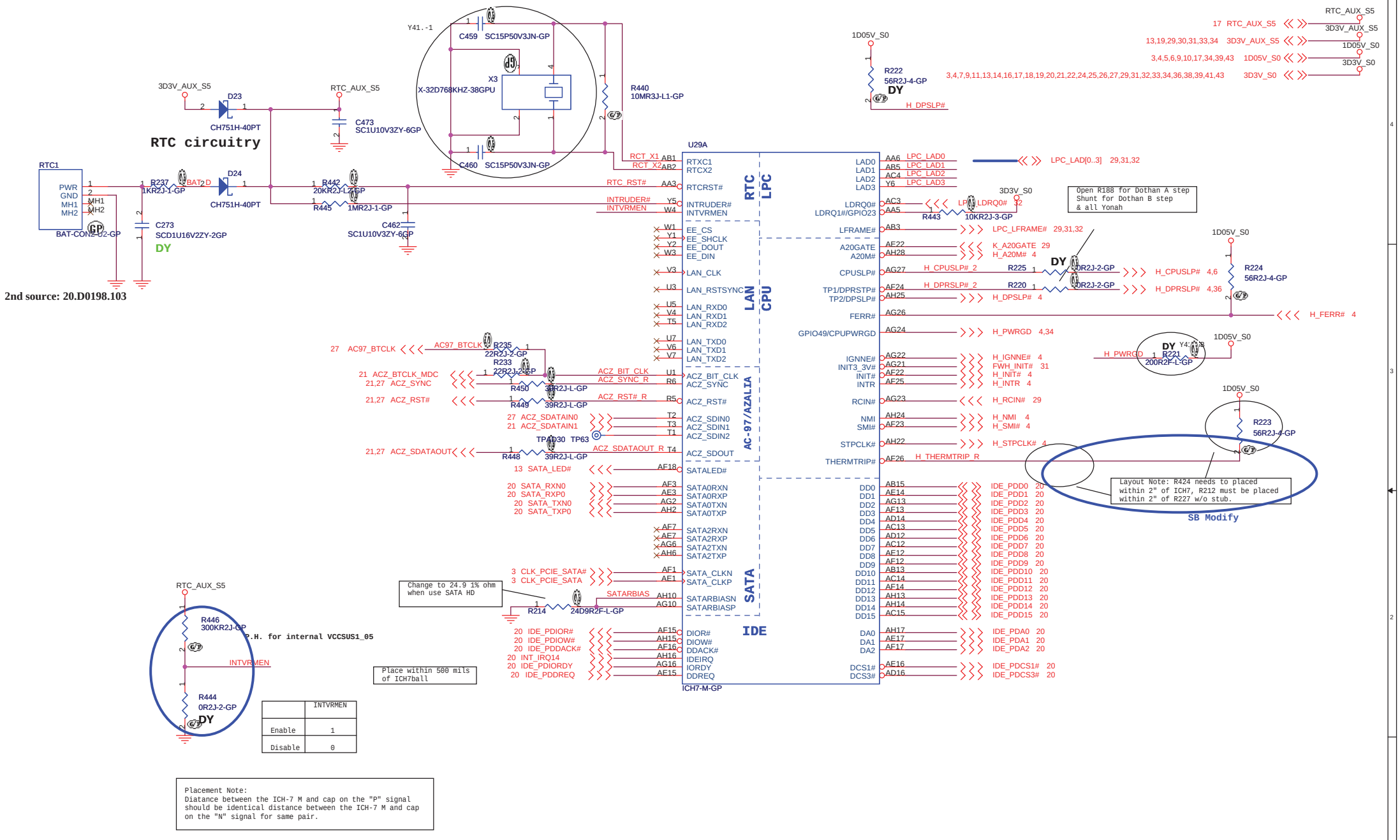
D22 D19 BAV99PT-GP-U
D16 D14 D13 BAV99PT-GP-U
LUMA_1
CRMA_1
CRT_R
CRT_G
CRT_B
TVout

13,17,18,19,20,21,25,27,28,29,30,31,33,34,36,43 5V_S0
2,4,7,9,11,13,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Y41/Y40
Rev: -1
Date: Friday, May 26, 2006
Sheet 14 of 44



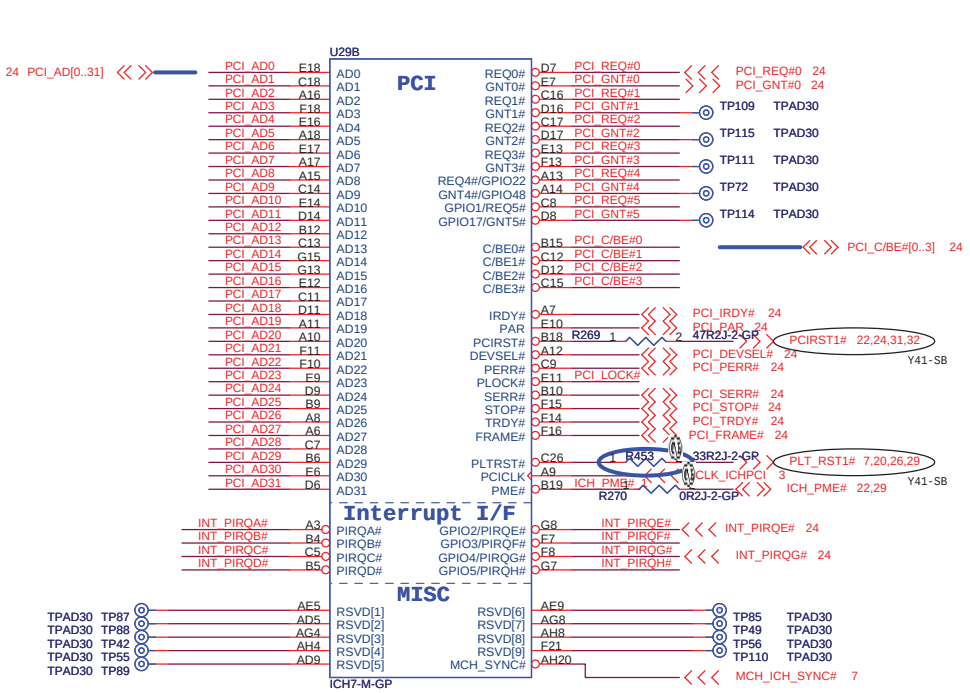
<variant_name>

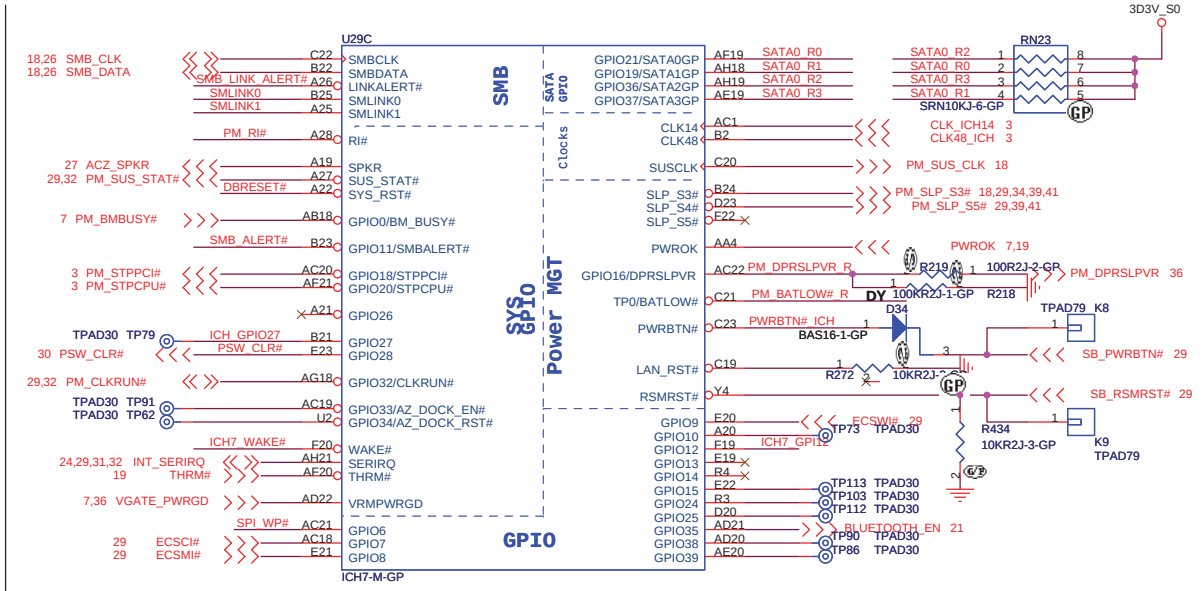
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

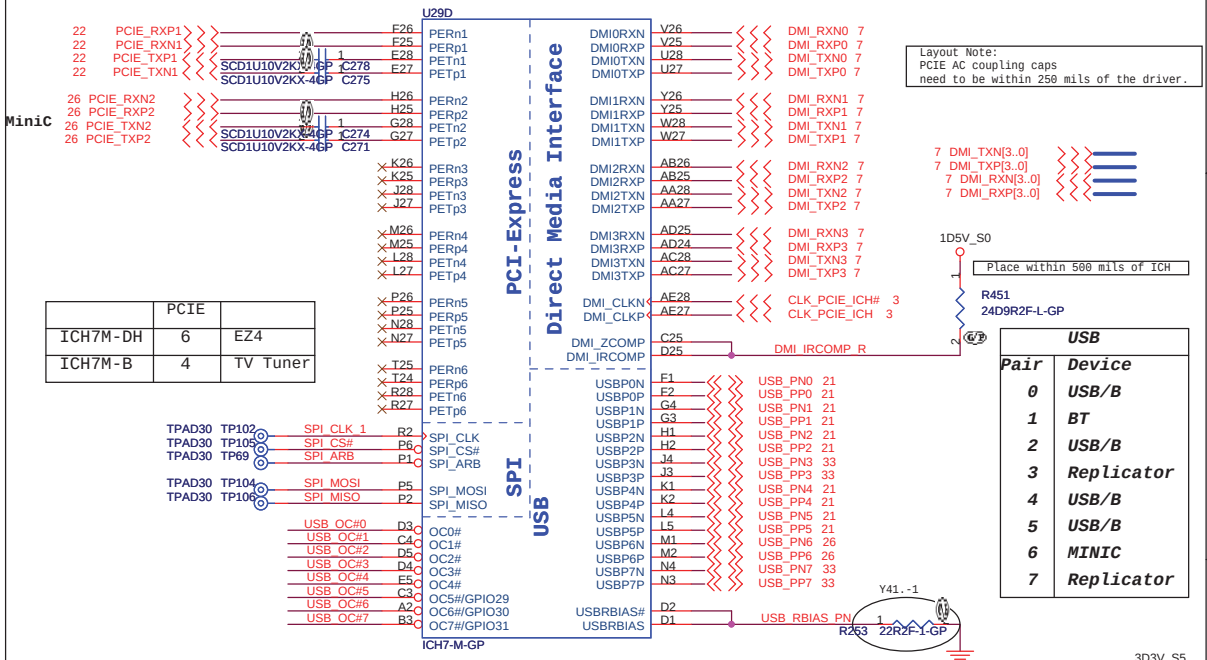
Title: ICH7-M (1 of 4)

Size: A3 | Document Number: Y41/Y40 | Rev: -1

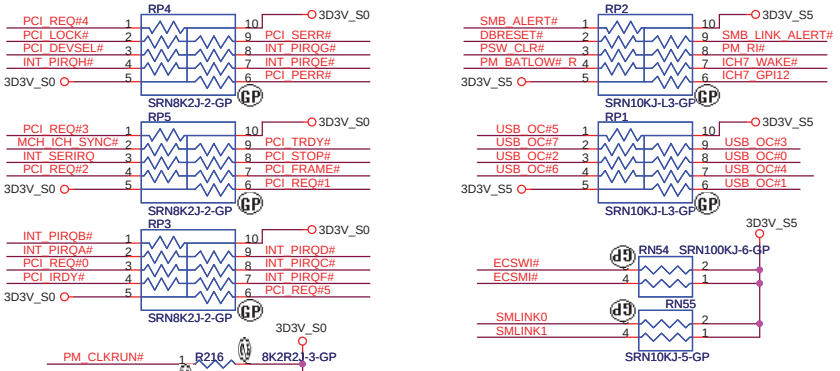
Date: Wednesday, April 12, 2006 | Sheet 15 of 44

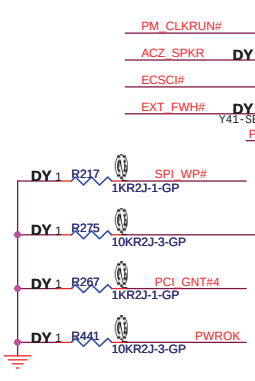






ICH7 Pullups





Default:H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

T=22ms

Boot from various source

	PCIE	
ICH7M-DH	6	EZ4
ICH7M-B	4	TV Tuner

USB	
Pair	Device
0	USB/B
1	BT
2	USB/B
3	Replicator
4	USB/B
5	USB/B
6	MINIC
7	Replicator

Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

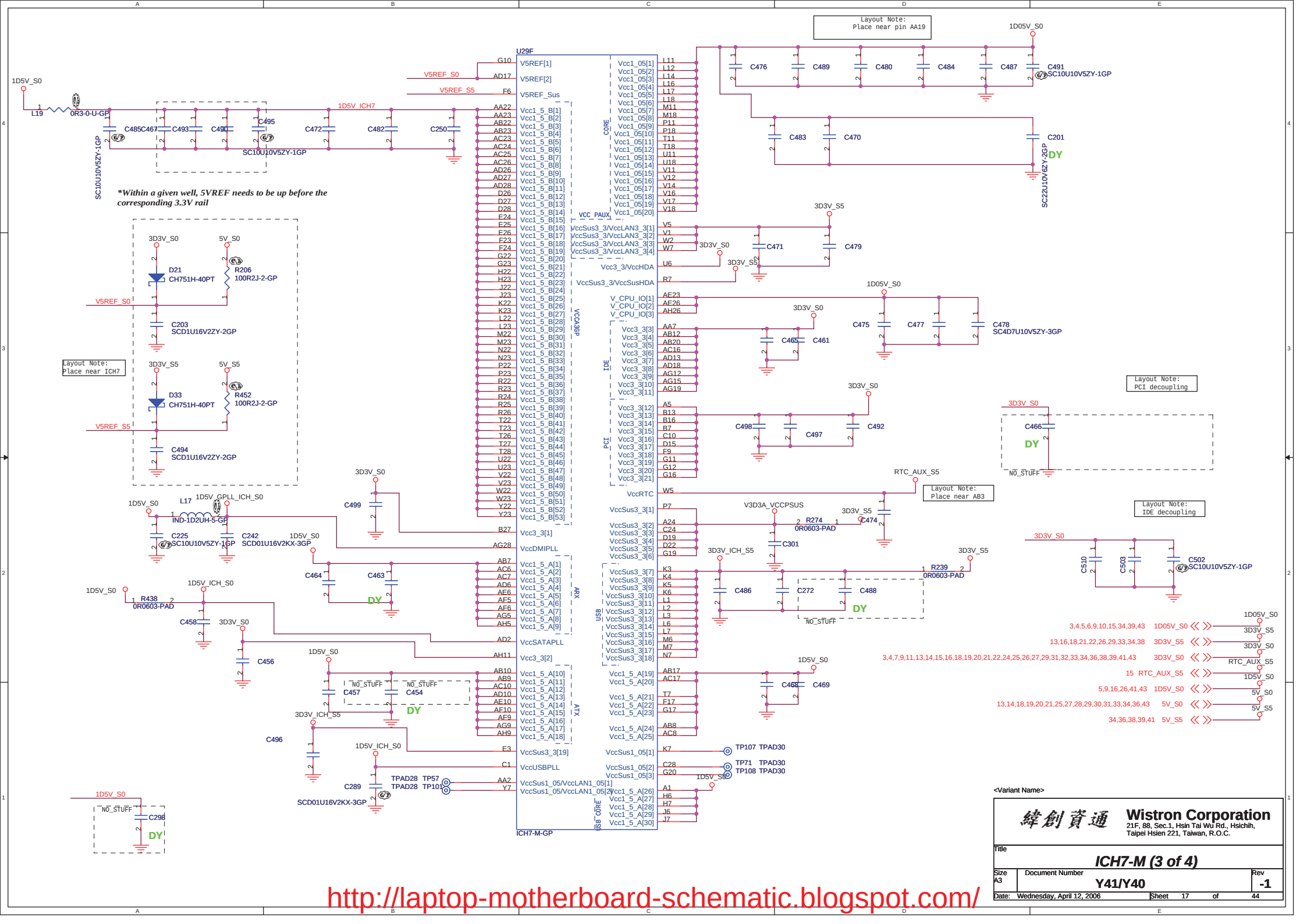
<Variant Name>

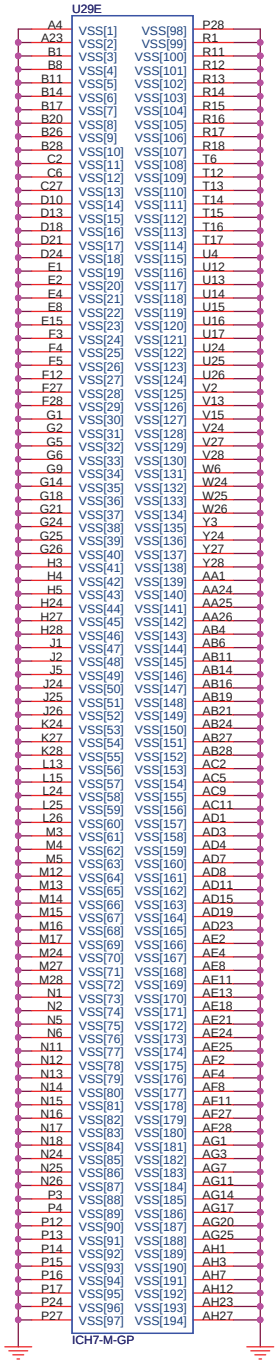
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

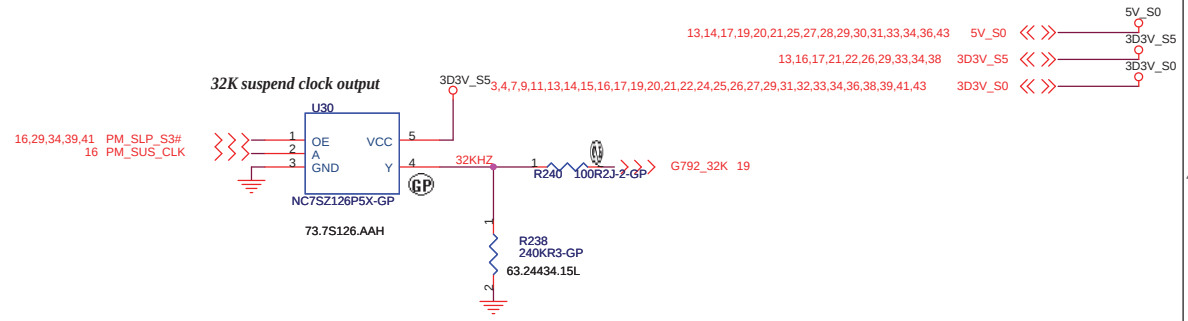
Title: ICH7-M (2 of 4)

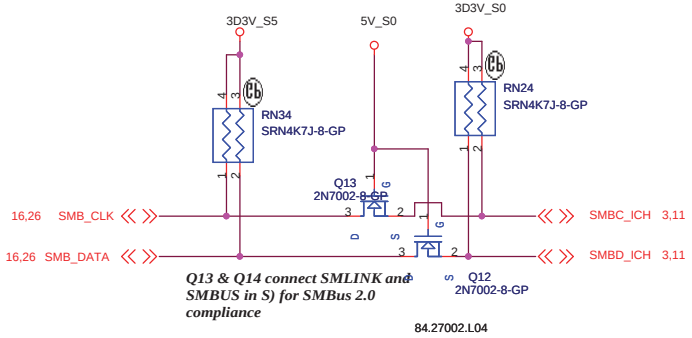
Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 16 of 44


U29F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: PCI decoupling
Layout Note: Place near AB3
Layout Note: IDE decoupling
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
Y41/Y40
Rev
-1
Date: Wednesday, April 12, 2006
Sheet 17 of 44
http://laptop-motherboard-schematic.blogspot.com/



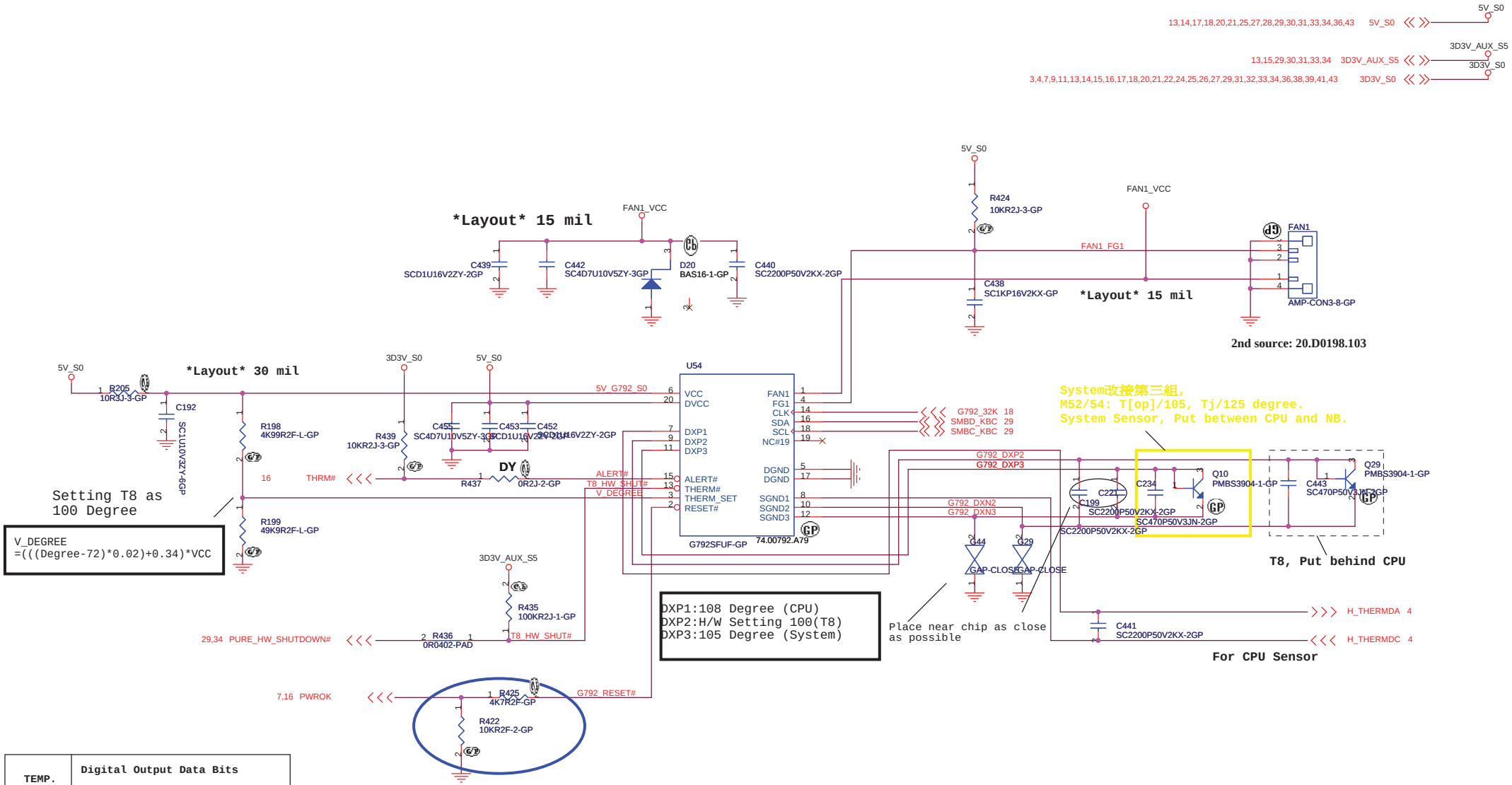




<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH7-M (4 of 4)/ODD	
Size A3	Document Number Y41/Y40	Rev -1
Date: Wednesday, April 12, 2006	Sheet 18 of 44	



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

<Variant Name>

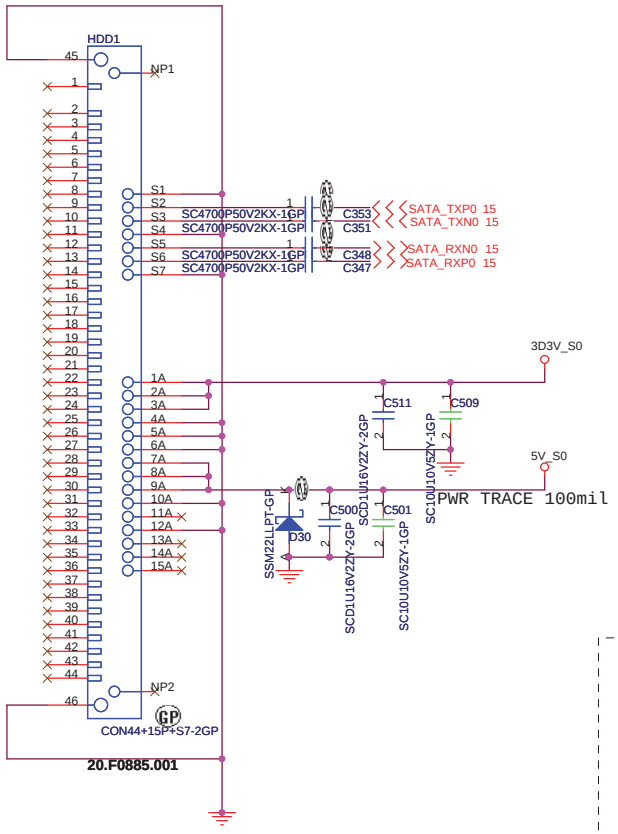
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

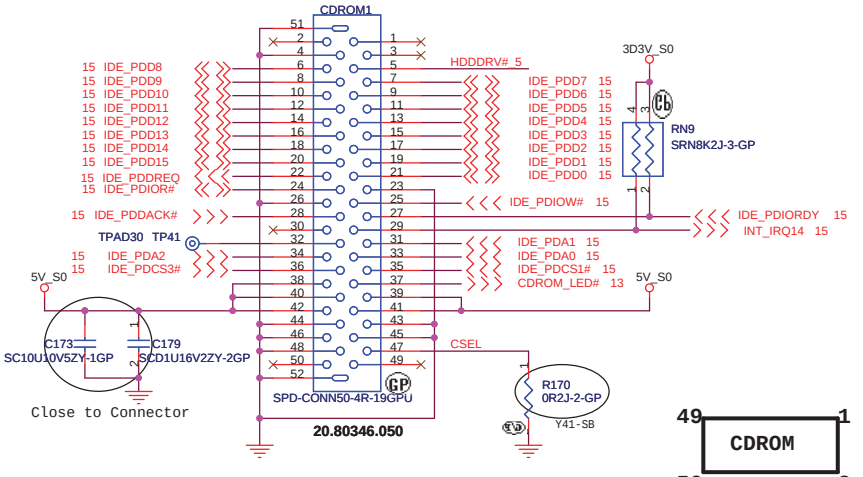
Size: Custom | Document Number: Y41/Y40 | Rev: -1

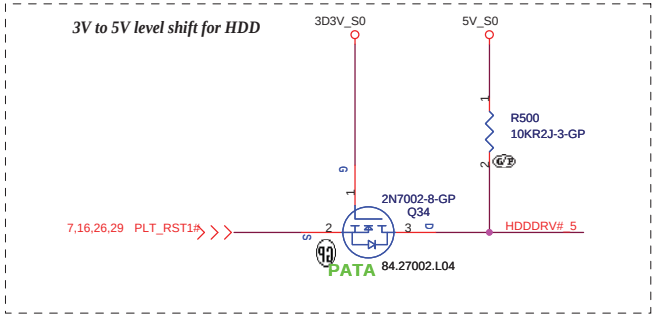
Date: Wednesday, April 12, 2006 | Sheet 19 of 44

SATA Connector



CDROM Connector





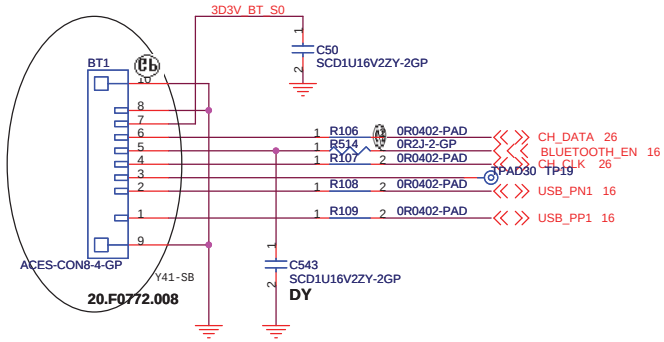
<Variant Name>

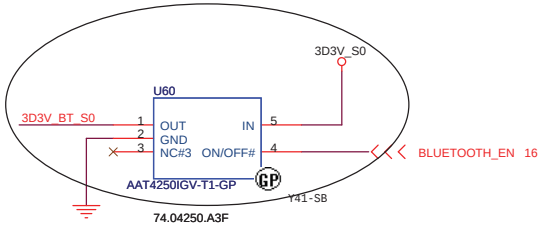
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

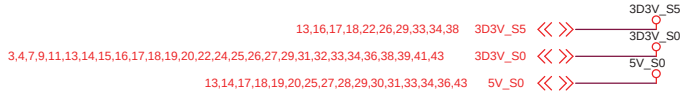
Title: SATA/PATA HDD ULi-M5285

Size: A3 | Document Number: Y41/Y40 | Rev: -1

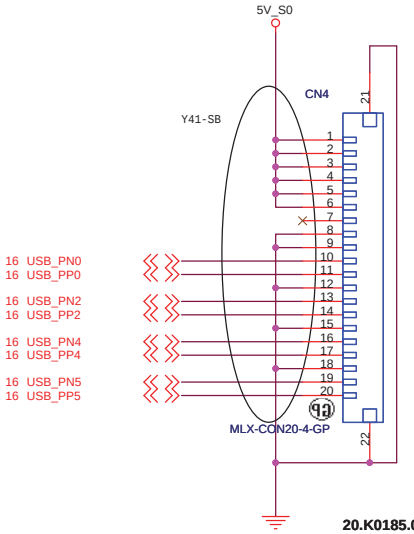
Date: Wednesday, April 12, 2006 | Sheet 20 of 44





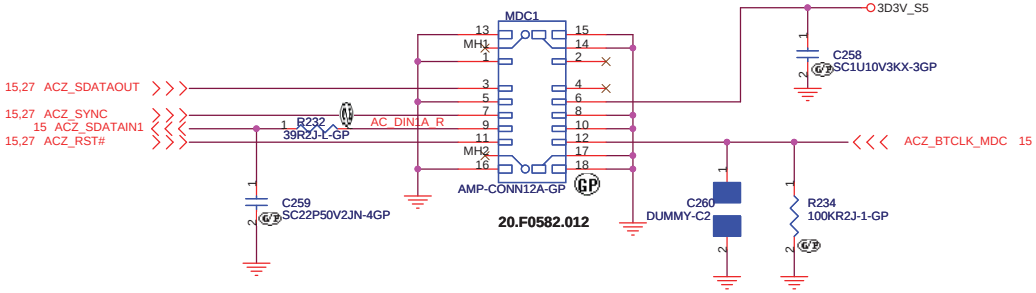


USB PORT



Cable length = 120mm.

MDC 1.5 CONN



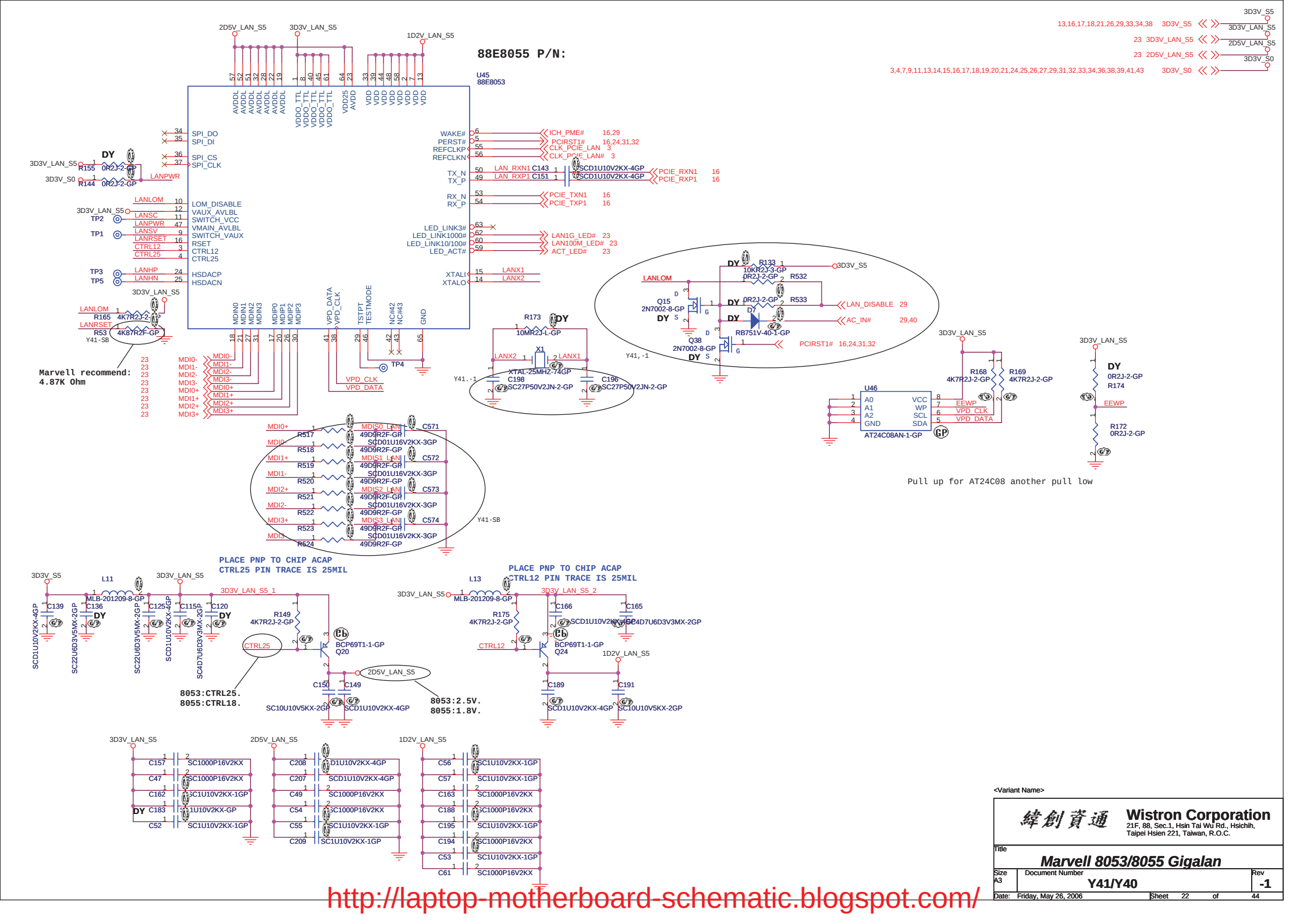
<Variant Name>

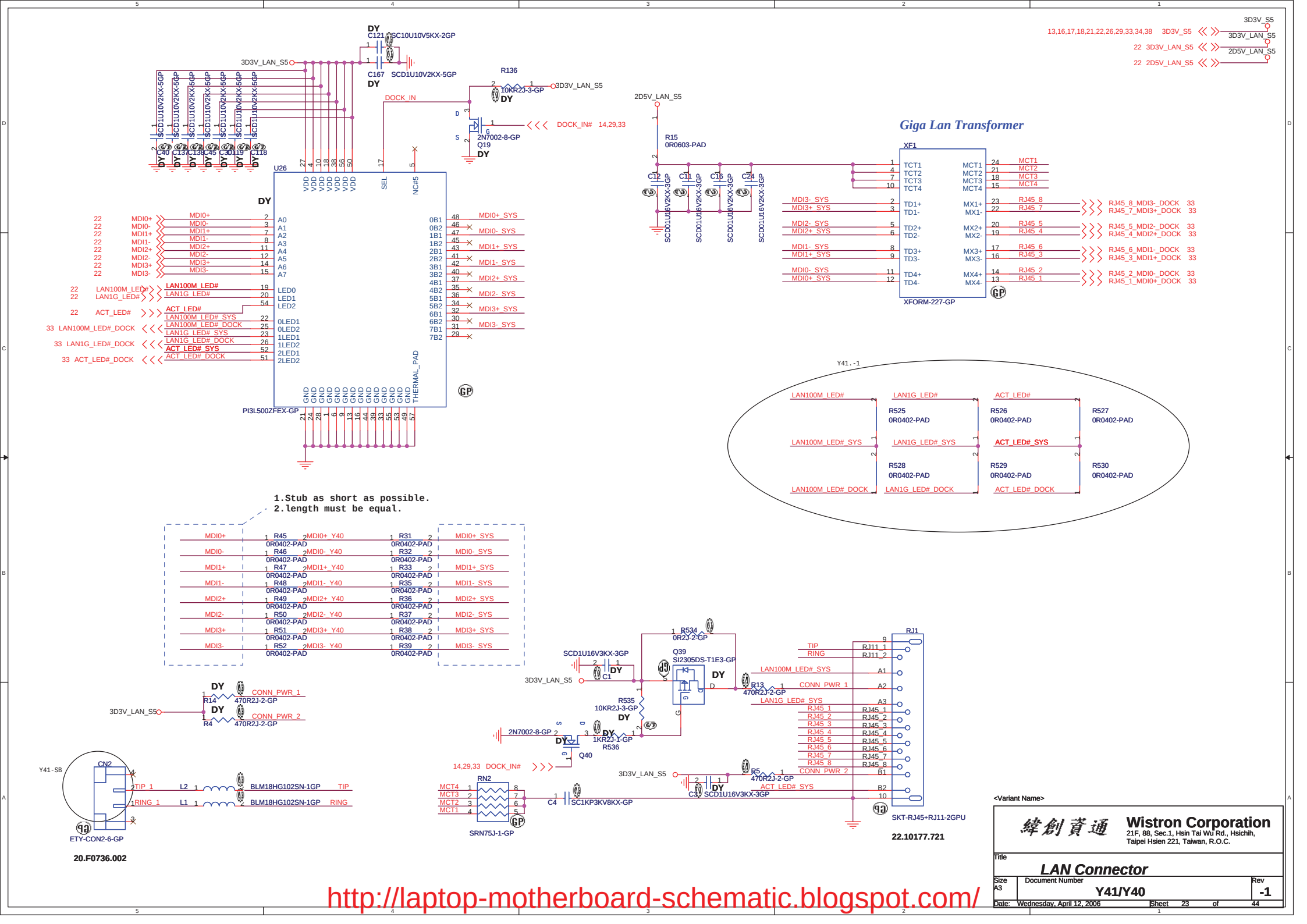
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

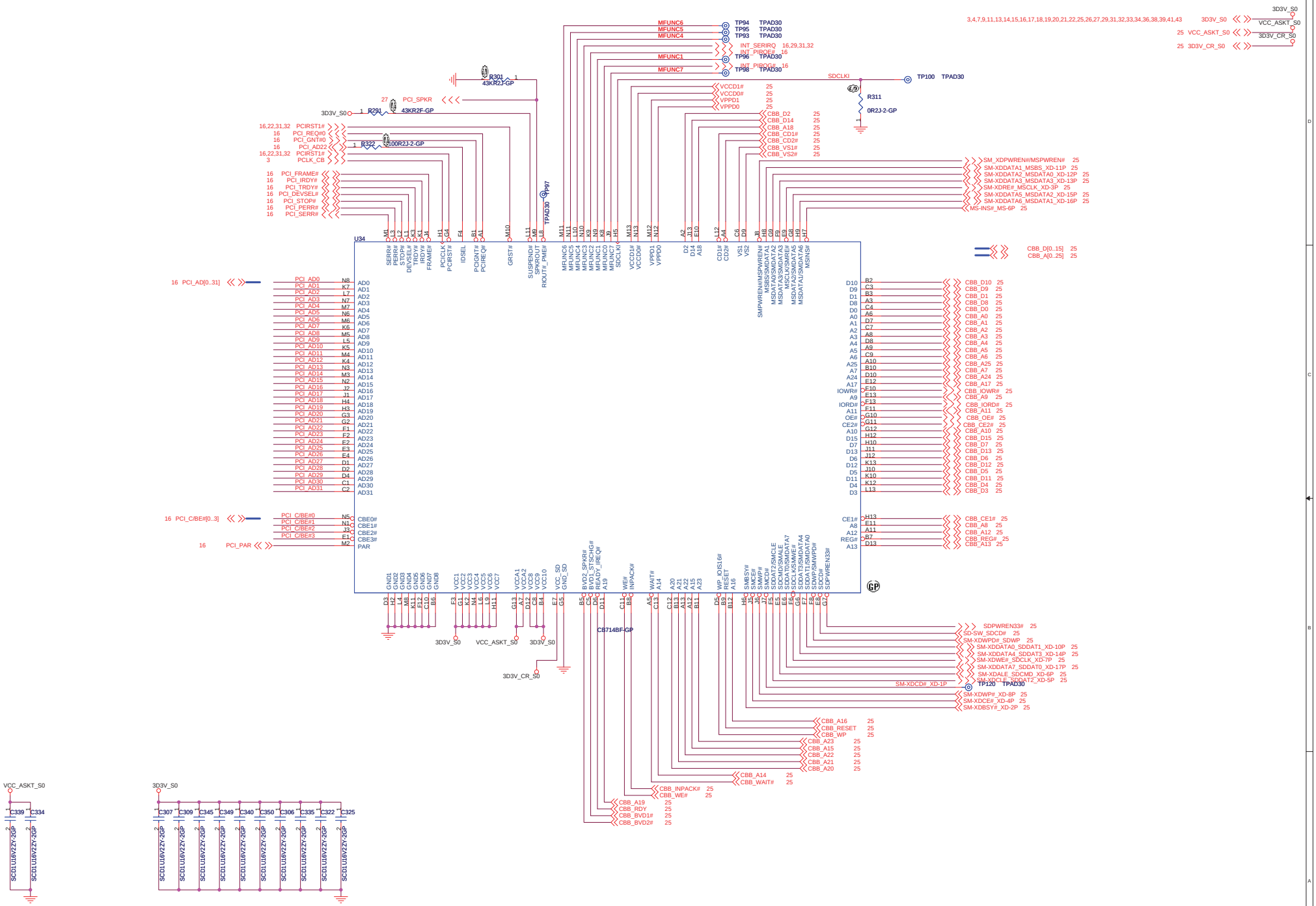
Title: USB and MDC I/F

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 21 of 44


88E8055 P/N:
U45
88E8053
Marvell recommend:
4.87K Ohm
Pull up for AT24C08 another pull low
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Marvell 8053/8055 Gigalan
Y41/Y40
-1
Friday, May 26, 2006
http://laptop-motherboard-schematic.blogspot.com/


Giga Lan Transformer
1.Stub as short as possible.
2.length must be equal.
U26
PI3L500ZFEX-GP
XF1
XFORM-227-GP
Y41.-1
CN2
ETY-CON2-6-GP
20.F0736.002
RN2
SRN75J-1-GP
RJ1
SKT-RJ45+RJ11-2GPU
22.10177.721
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN Connector
Y41/Y40
Wednesday, April 12, 2006
http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CardBus CB714**

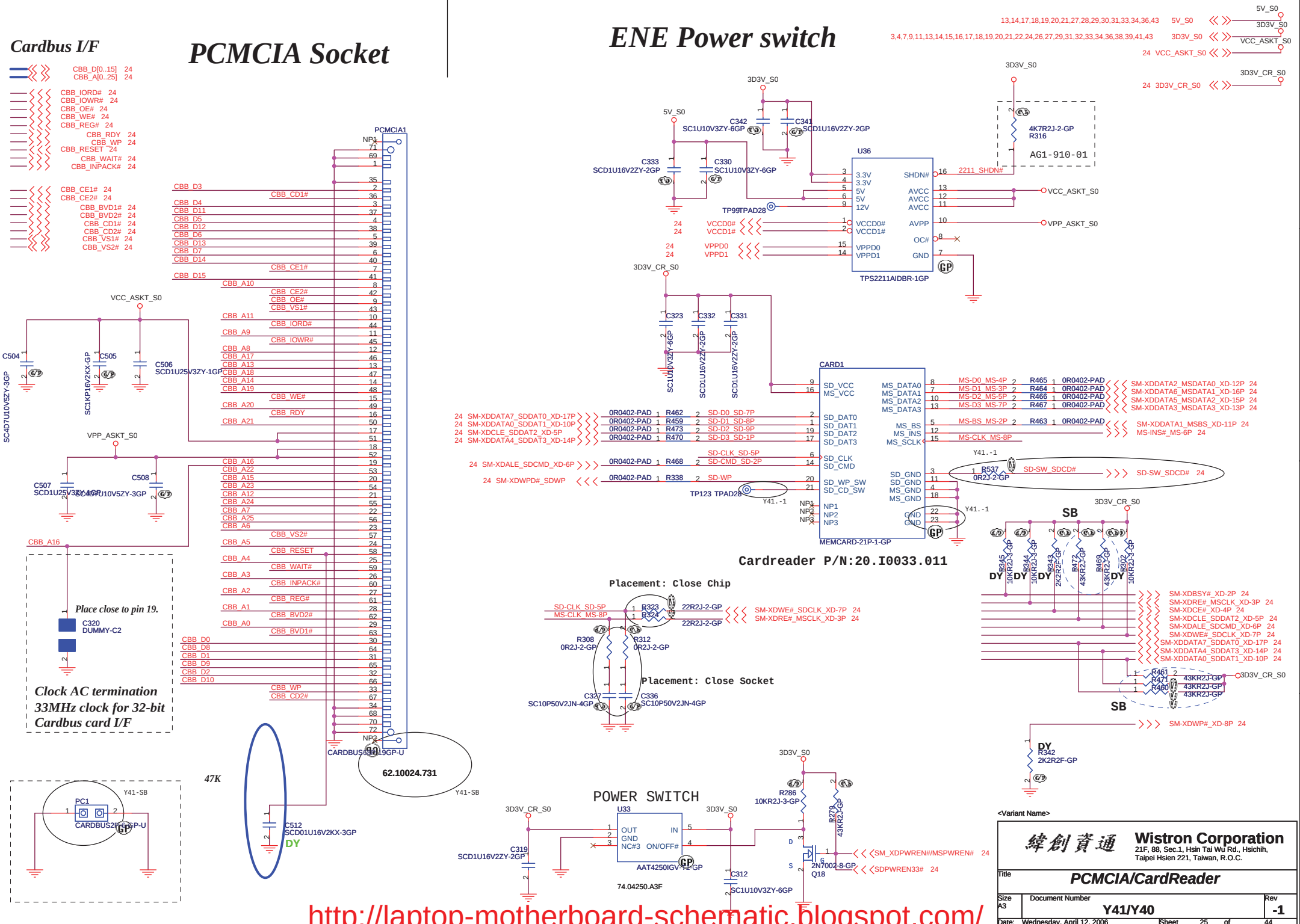
Size	Document Number	Rev
C	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 24 of 44

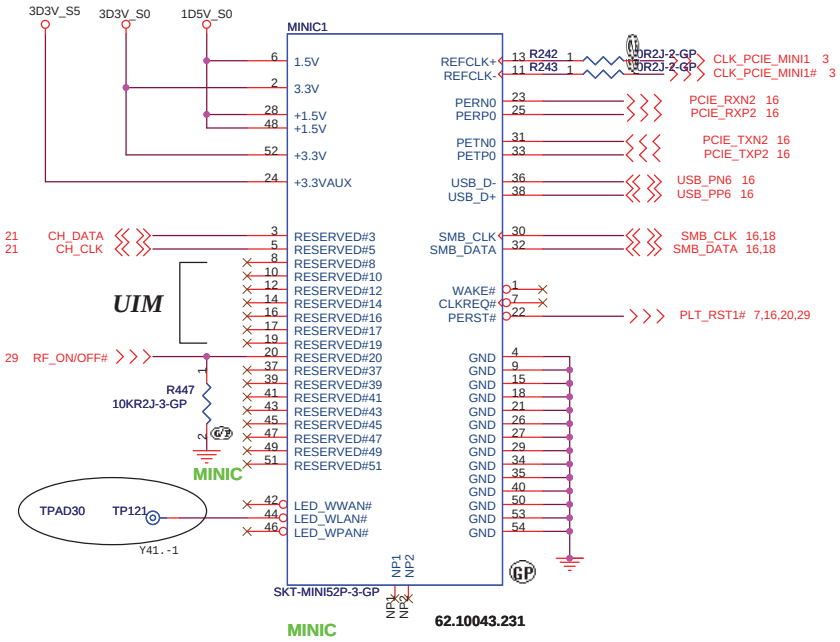
Cardbus I/F

PCMCIA Socket

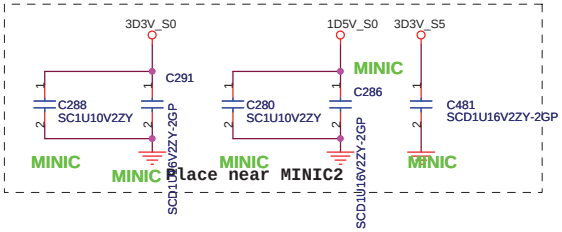
ENE Power switch



Mini Card Connector



Change part to P/N:62.10043.241



3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

13,16,17,18,21,22,29,33,34,38 3D3V_S5

24,25 3D3V_CR_S0

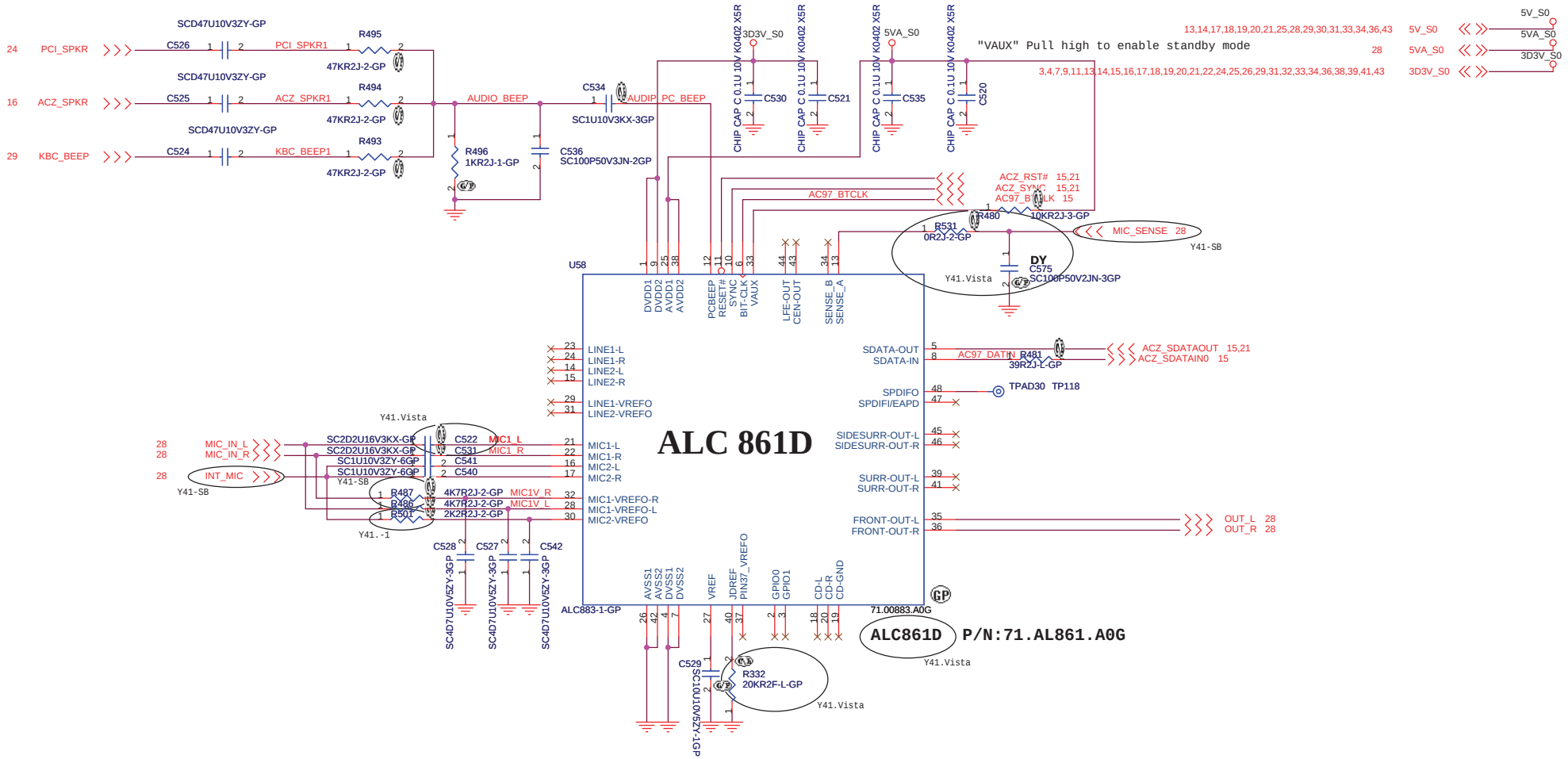
5,9,16,17,41,43 1D5V_S0

3D3V_S0
3D3V_S5
3D3V_CR_S0
1D5V_S0

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

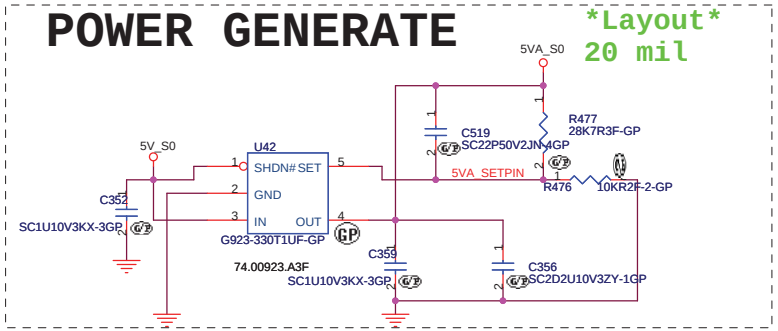
Title	***MINI CARD***	
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 26 of 44	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<Variant Name>

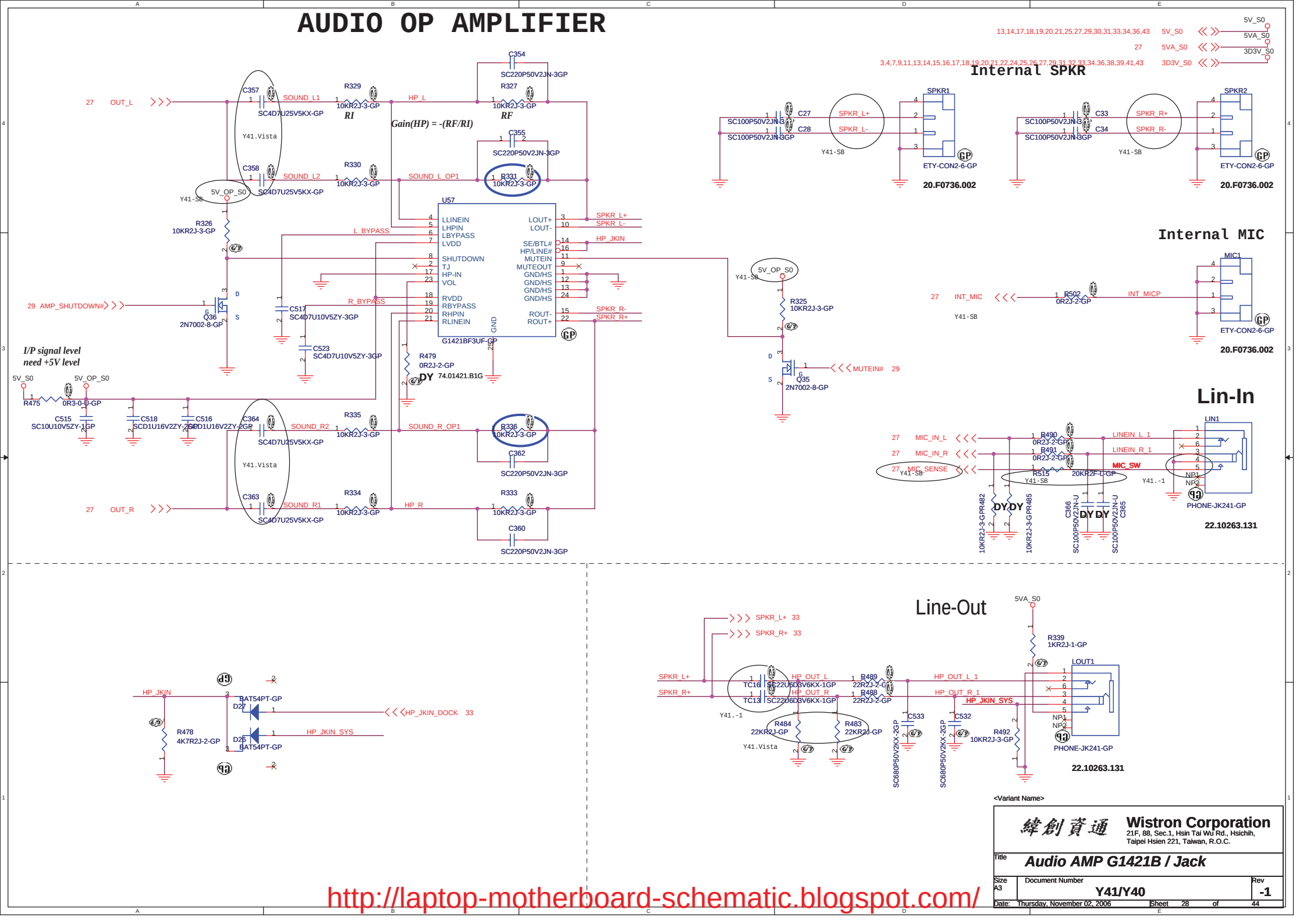
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC861

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Thursday, November 02, 2006 | Sheet 27 of 44

AUDIO OP AMPLIFIER



http://laptop-motherboard-schematic.blogspot.com/

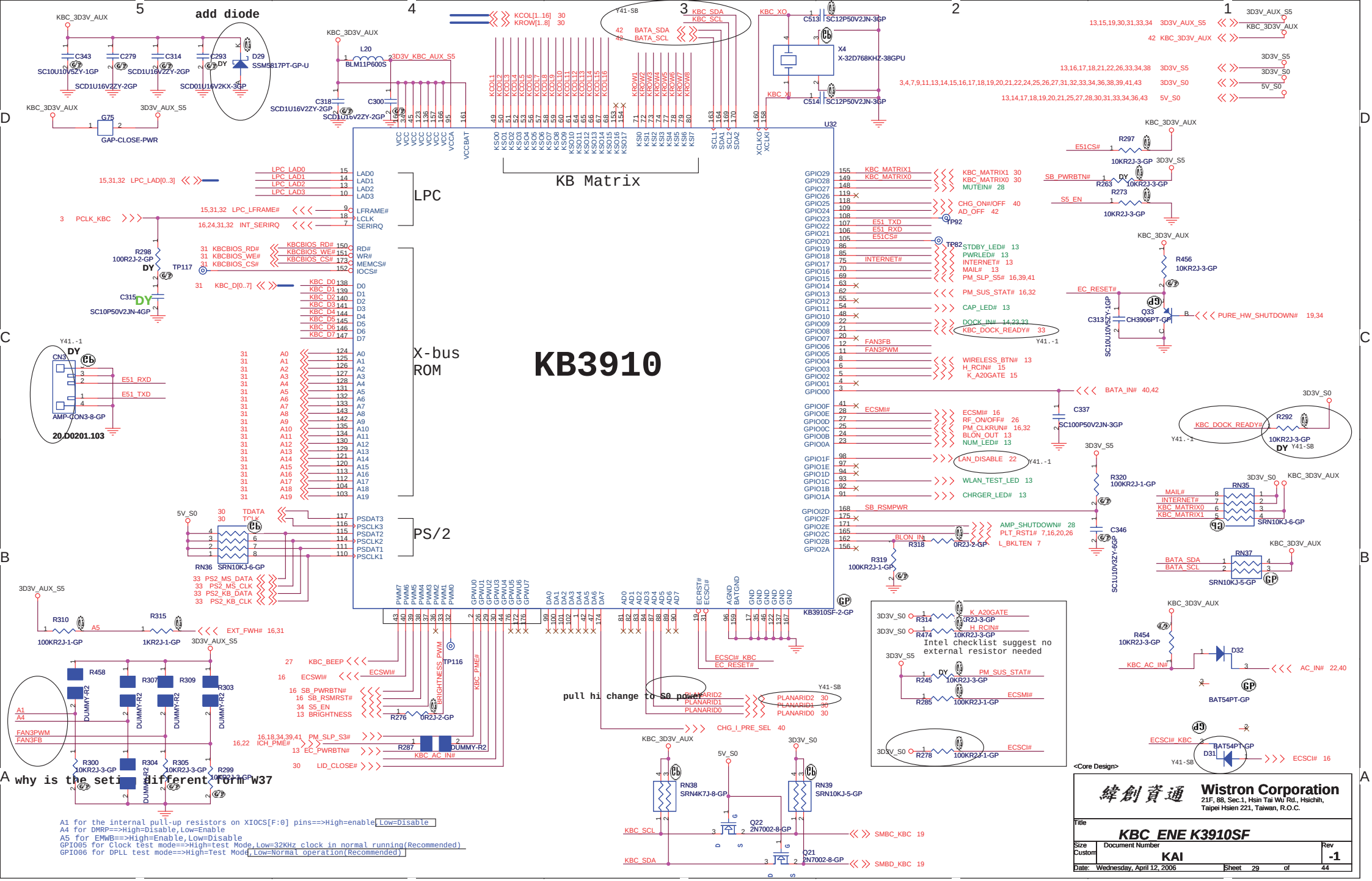
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio AMP G1421B / Jack

Size: A3 | Document Number: Y41/Y40 | Rev: -1

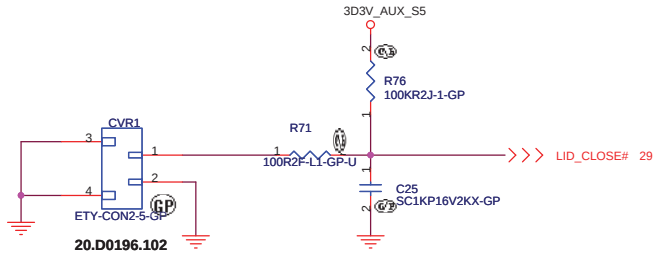
Date: Thursday, November 02, 2006 | Sheet 28 of 44

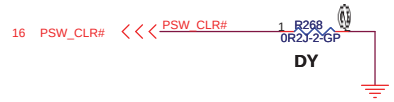
<Variant Name>



Internal KeyBoard Connector

COVER SWITCH

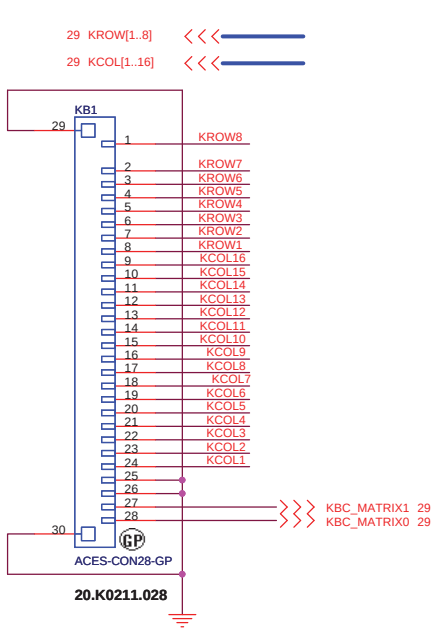




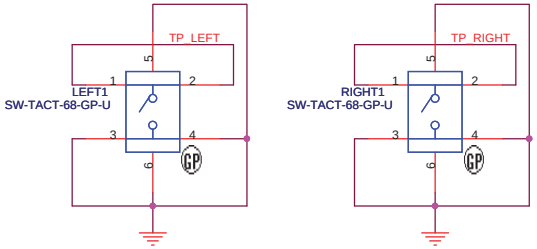
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

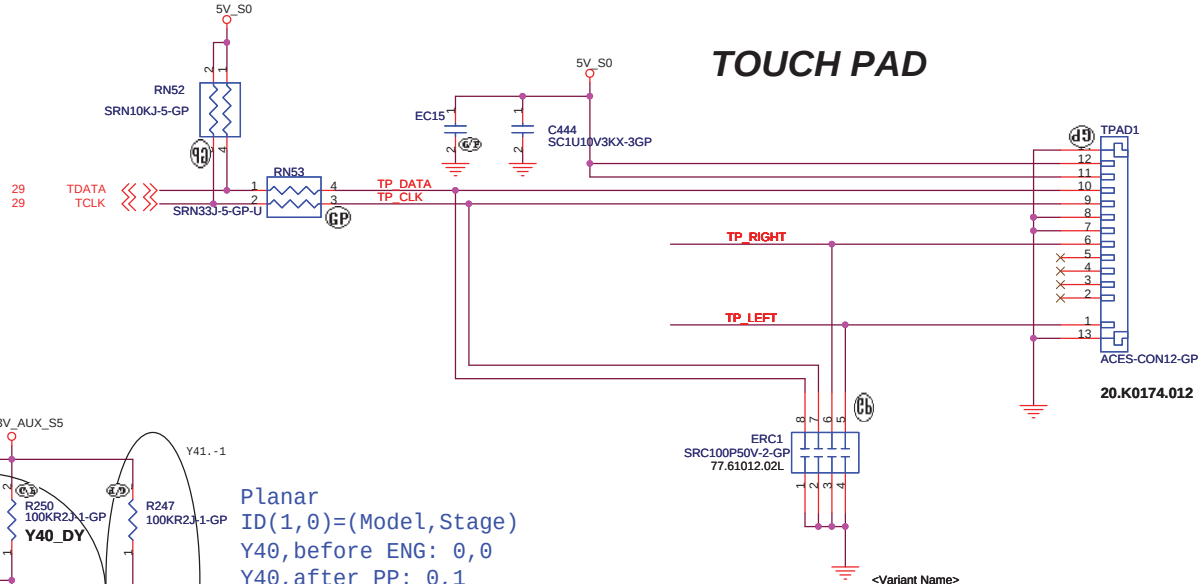
	Low Active
PSW_CLR#	1 - 5 ON

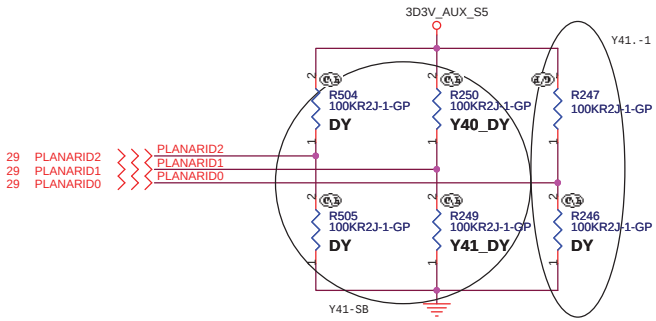


SCROLL KEY



TOUCH PAD





Planar
ID(1,0)=(Model,Stage)
Y40,before ENG: 0,0
Y40,after PP: 0,1
Y41,before ENG: 1,0
Y41,after PP: 1,1

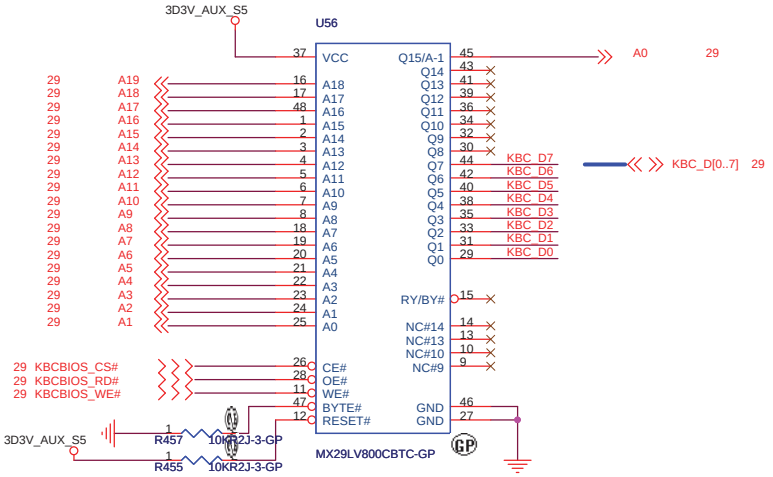
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

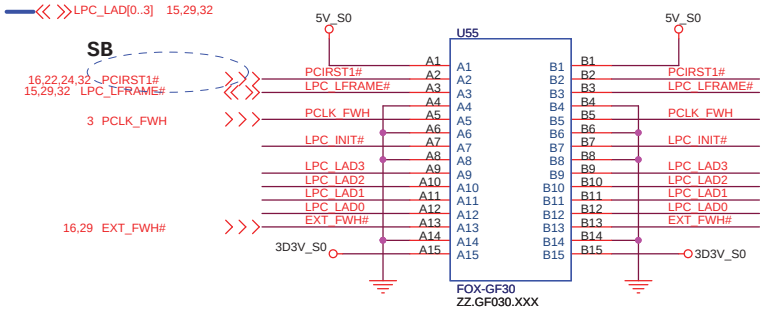
Title: KEYBOARD/TOUCHPAD

Size: A3 | Document Number: Y41/Y40 | Rev: -1

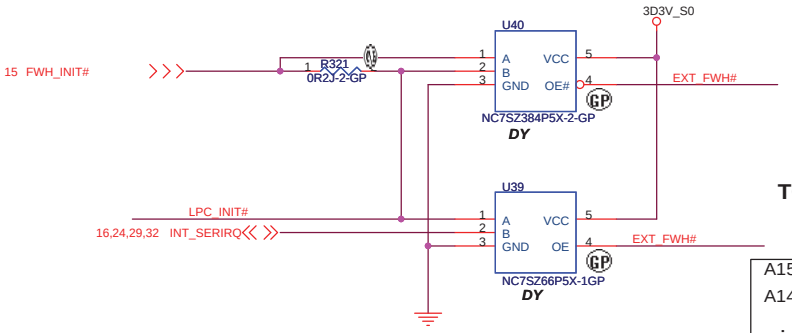
Date: Wednesday, April 12, 2006 | Sheet 30 of 44



GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

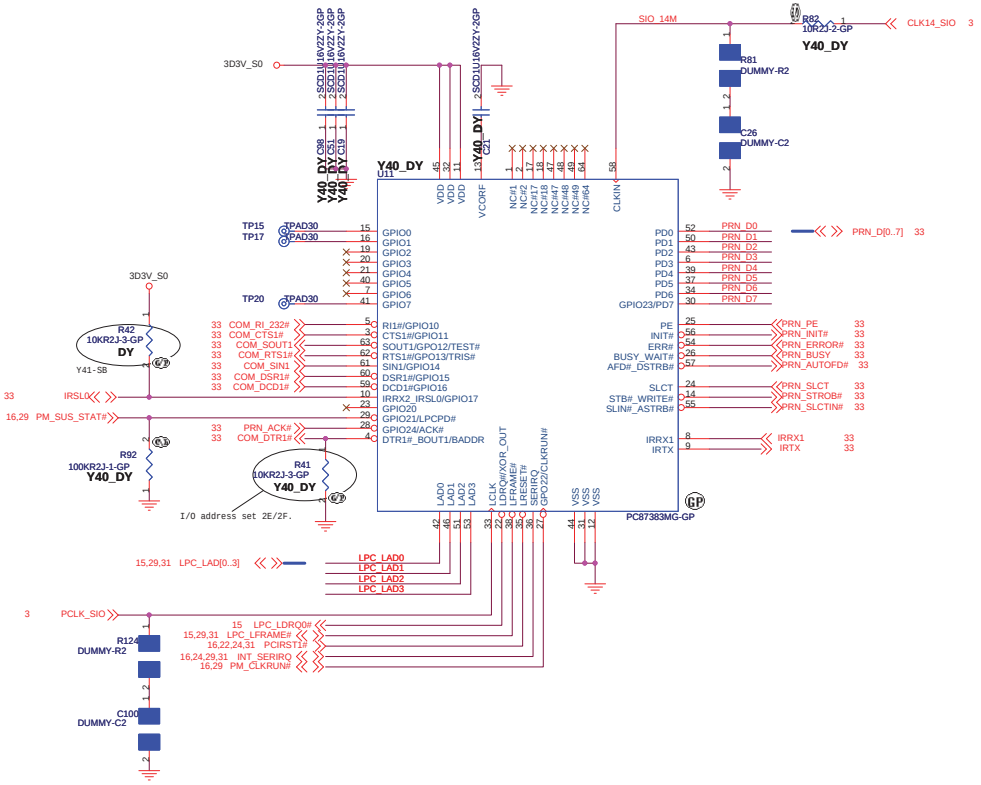


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***BIOS : SPI/Debug***		
Size A3	Document Number **Y41/Y40**		Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 31 of 44		



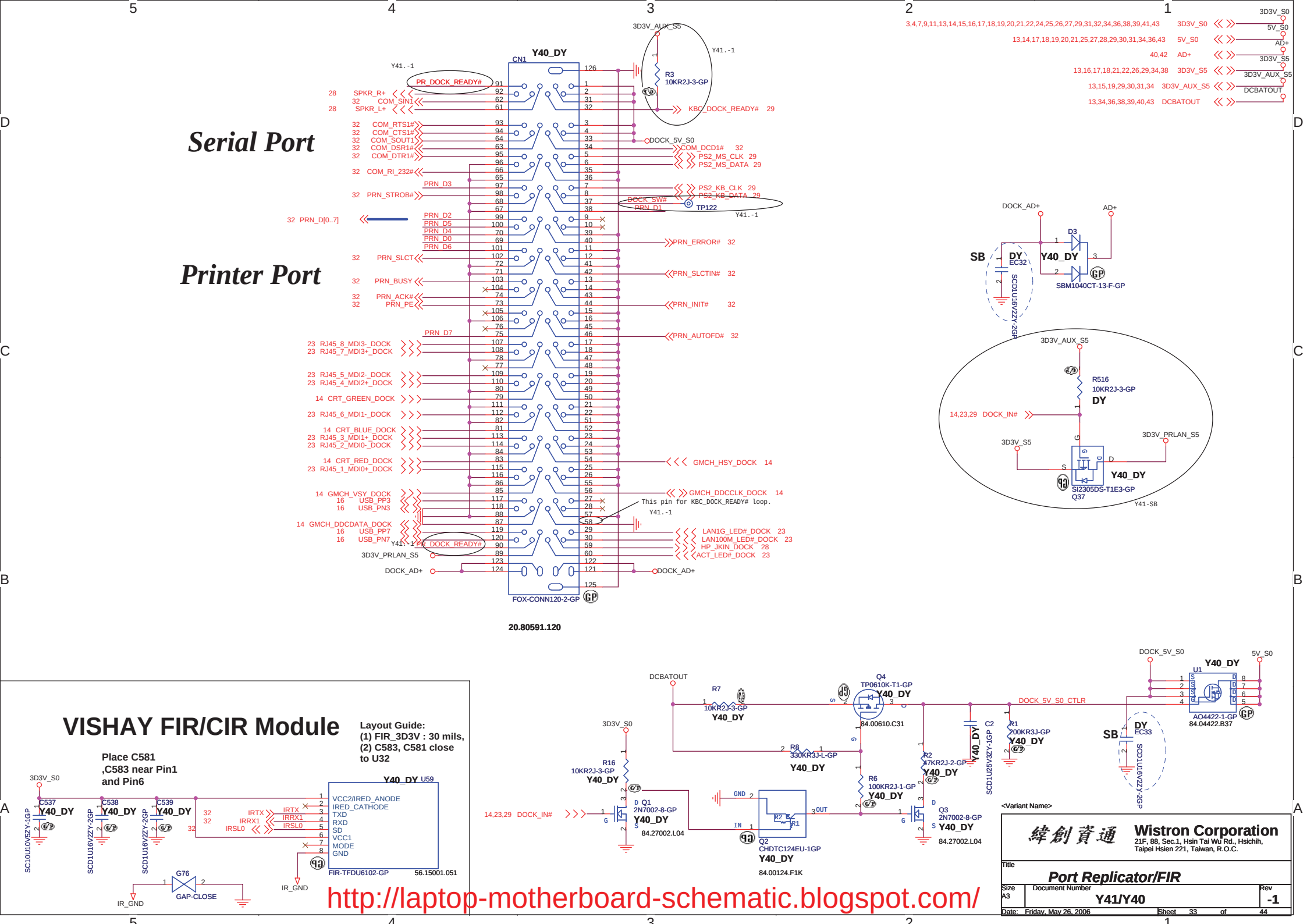
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

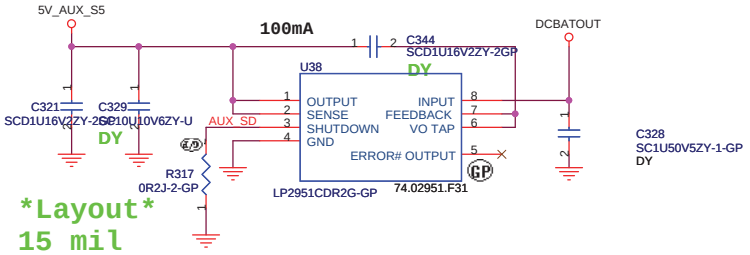
Title: SIO PC87383-VS

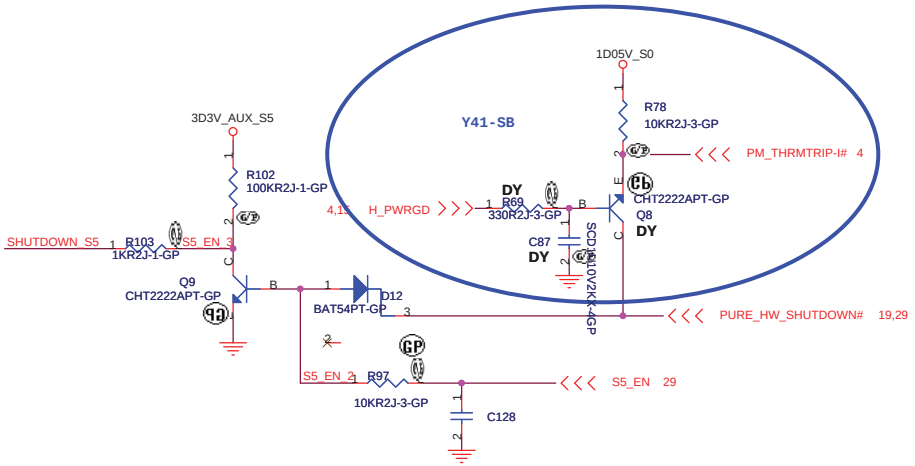
Size: C | Document Number: Y41/Y40 | Rev: -1

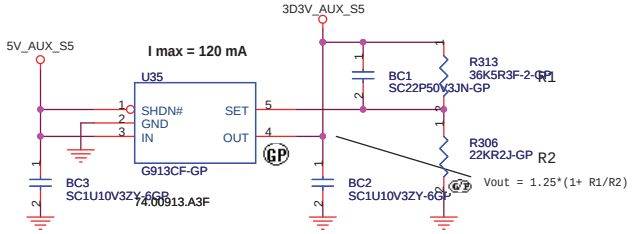
Date: Wednesday, April 12, 2006 | Sheet 32 of 44

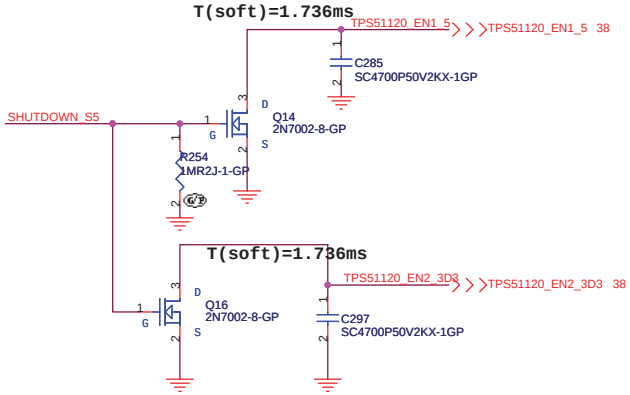


Aux Power

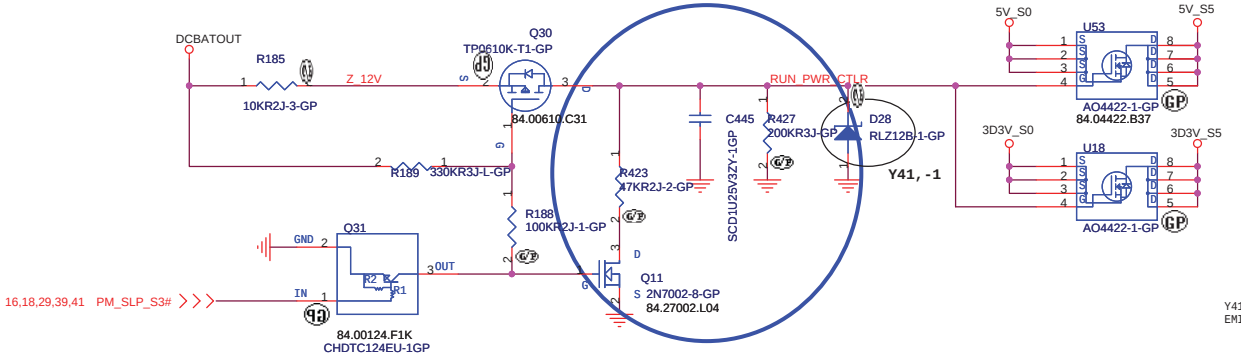


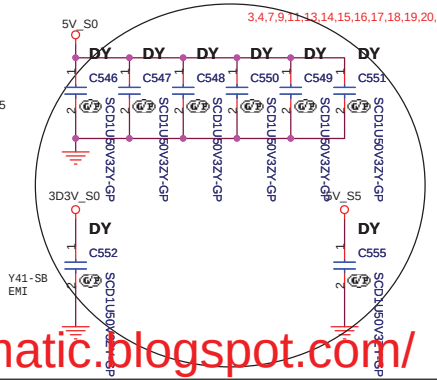


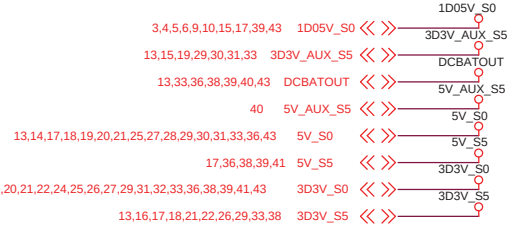




Run Power







<Variant Name>

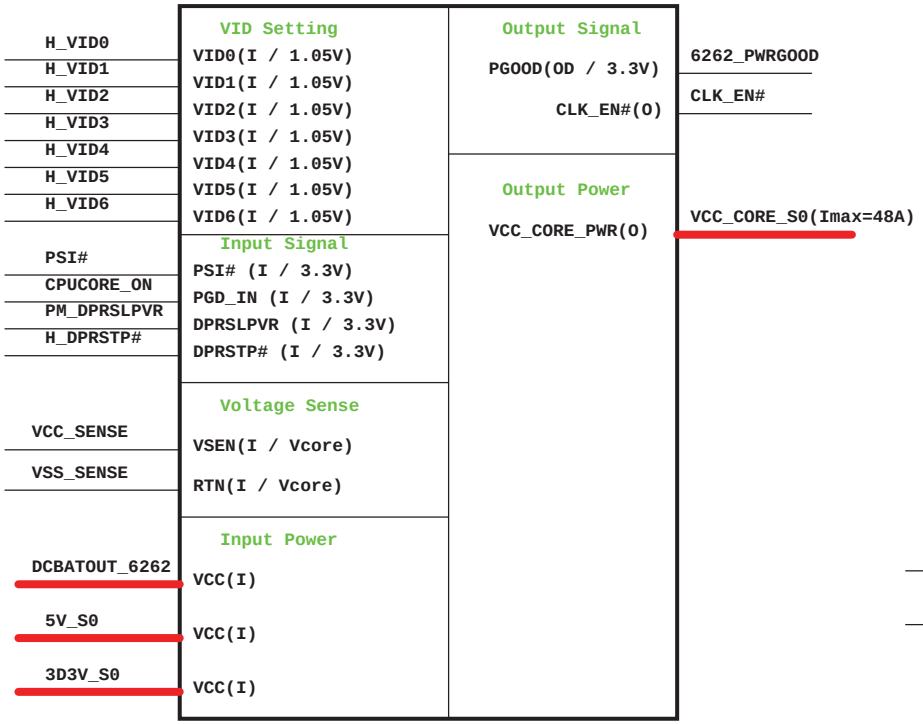
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN and AUX POWER

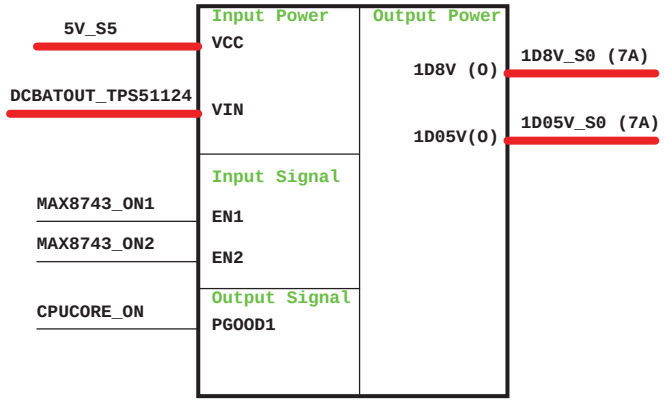
Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 34 of 44

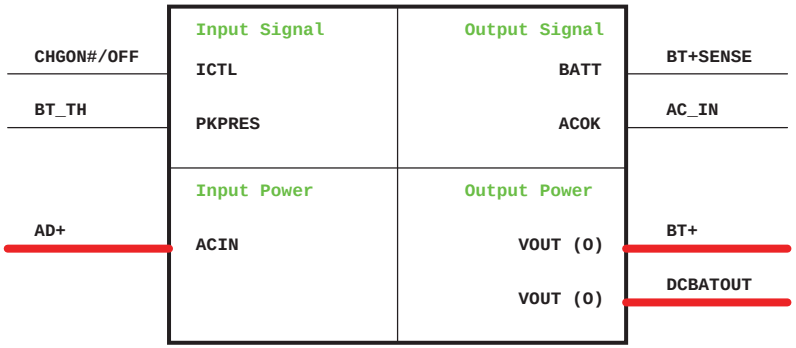
CPU_CORE
Intersil ISL6262



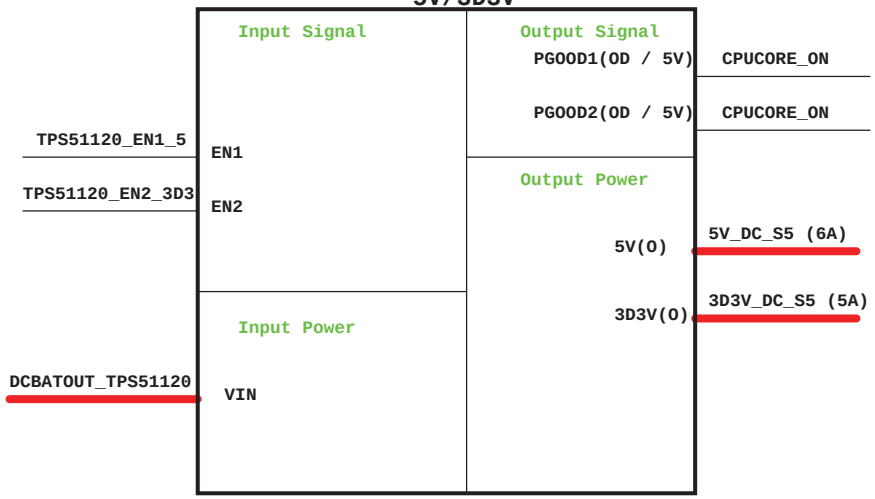
MAX8743
1D8V/1D05V



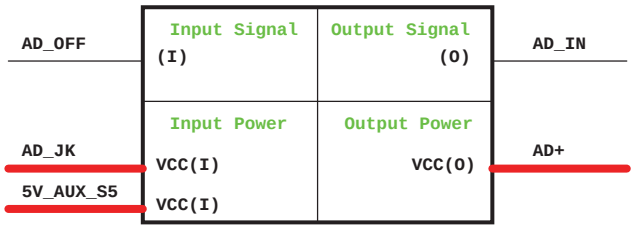
Charger Max8725



TPS51120
5V/3D3V



Adapter



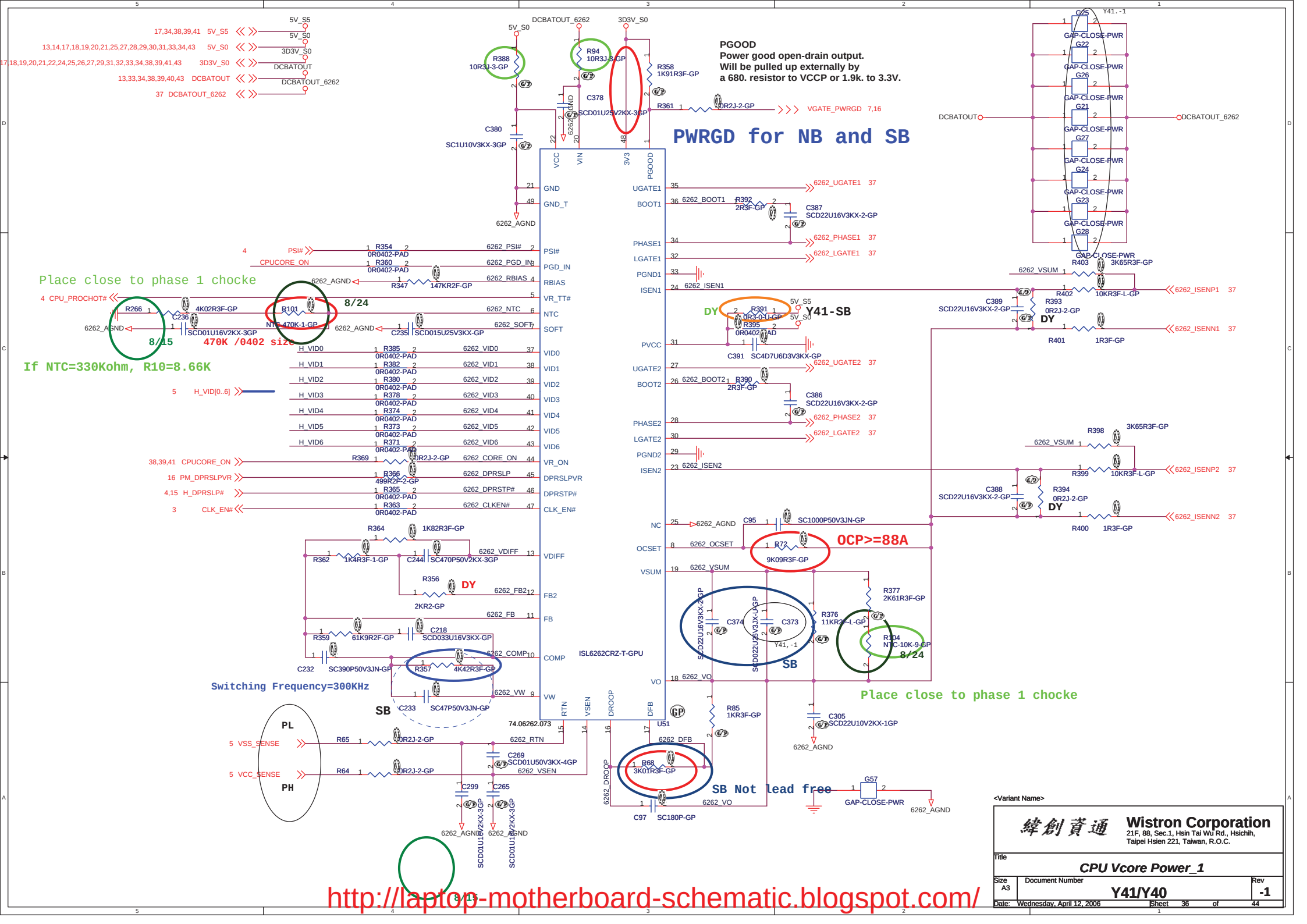
<Variant Name>

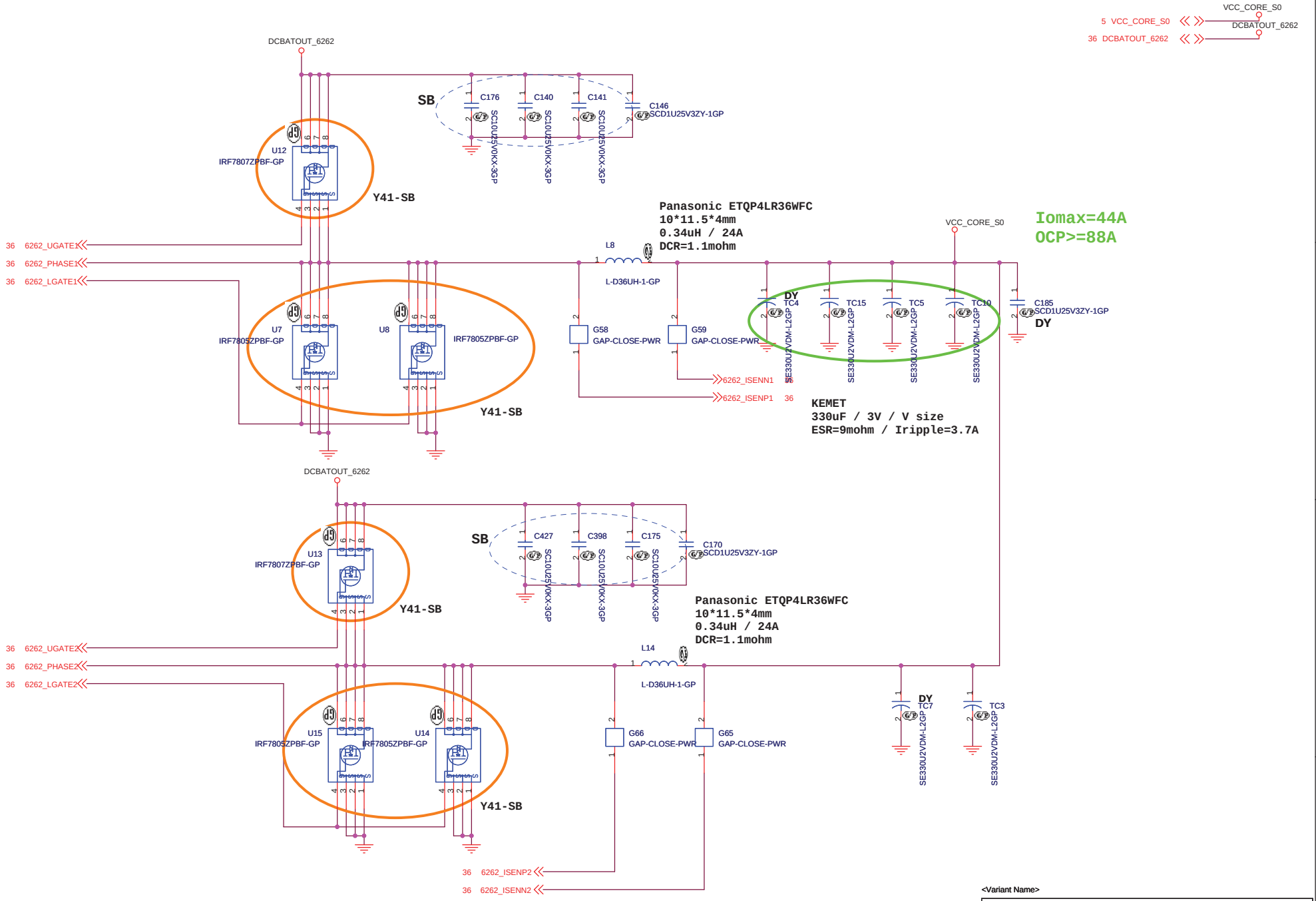
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Friday, April 07, 2006 | Sheet 35 of 44

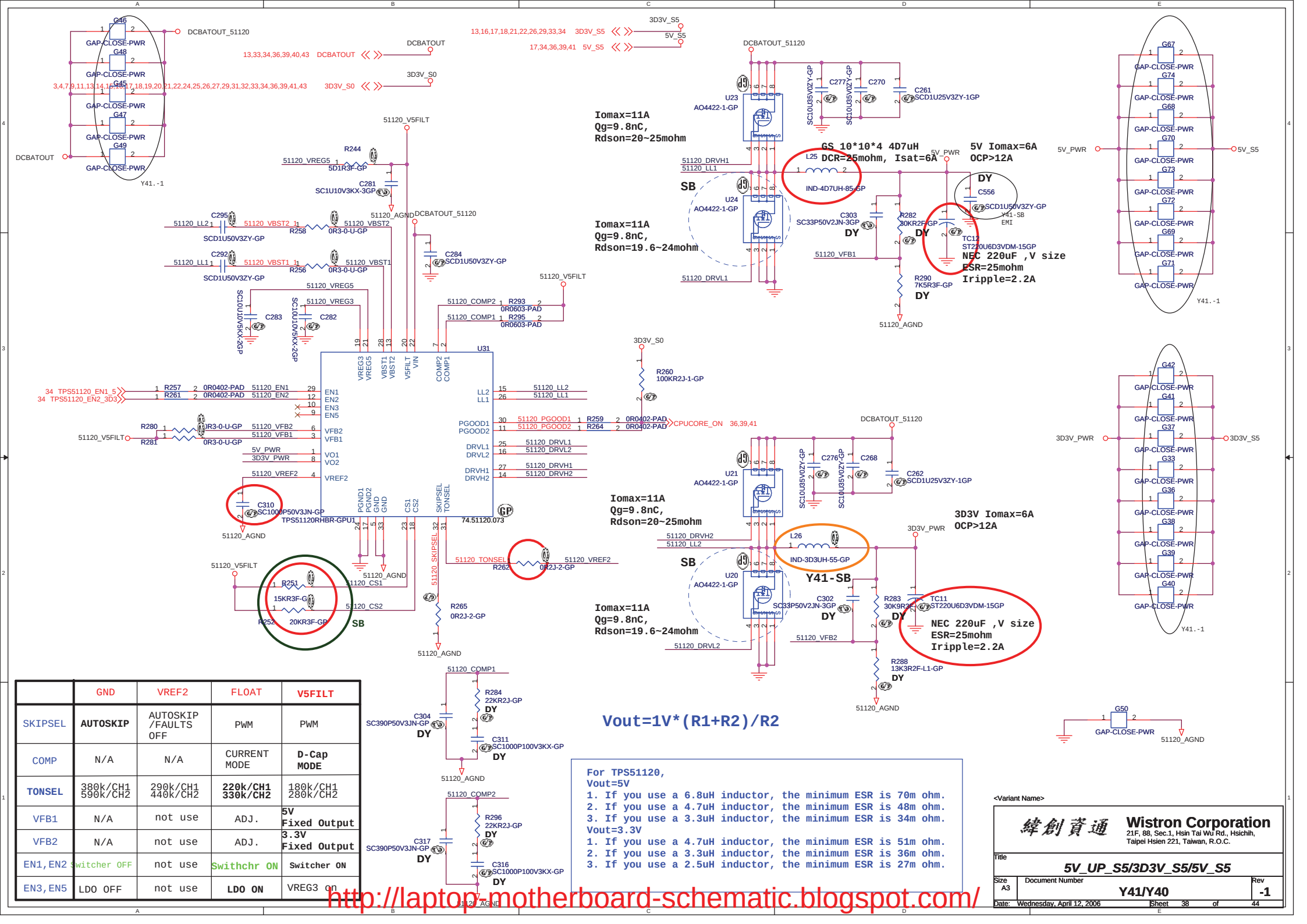

PWRGD for NB and SB
PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
Y41-SB
DY
8/24
8/15
470K /0402 size
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
Switching Frequency=300KHz
OCP>=88A
SB
SB Not lead free
ISL6262CRZ-T-GPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
Y41/Y40
Wednesday, April 12, 2006
http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU Vcore Power_2*	
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 37 of 44	



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1, EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3, EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use 2.5uH inductor, the minimum ESR is 27m ohm.

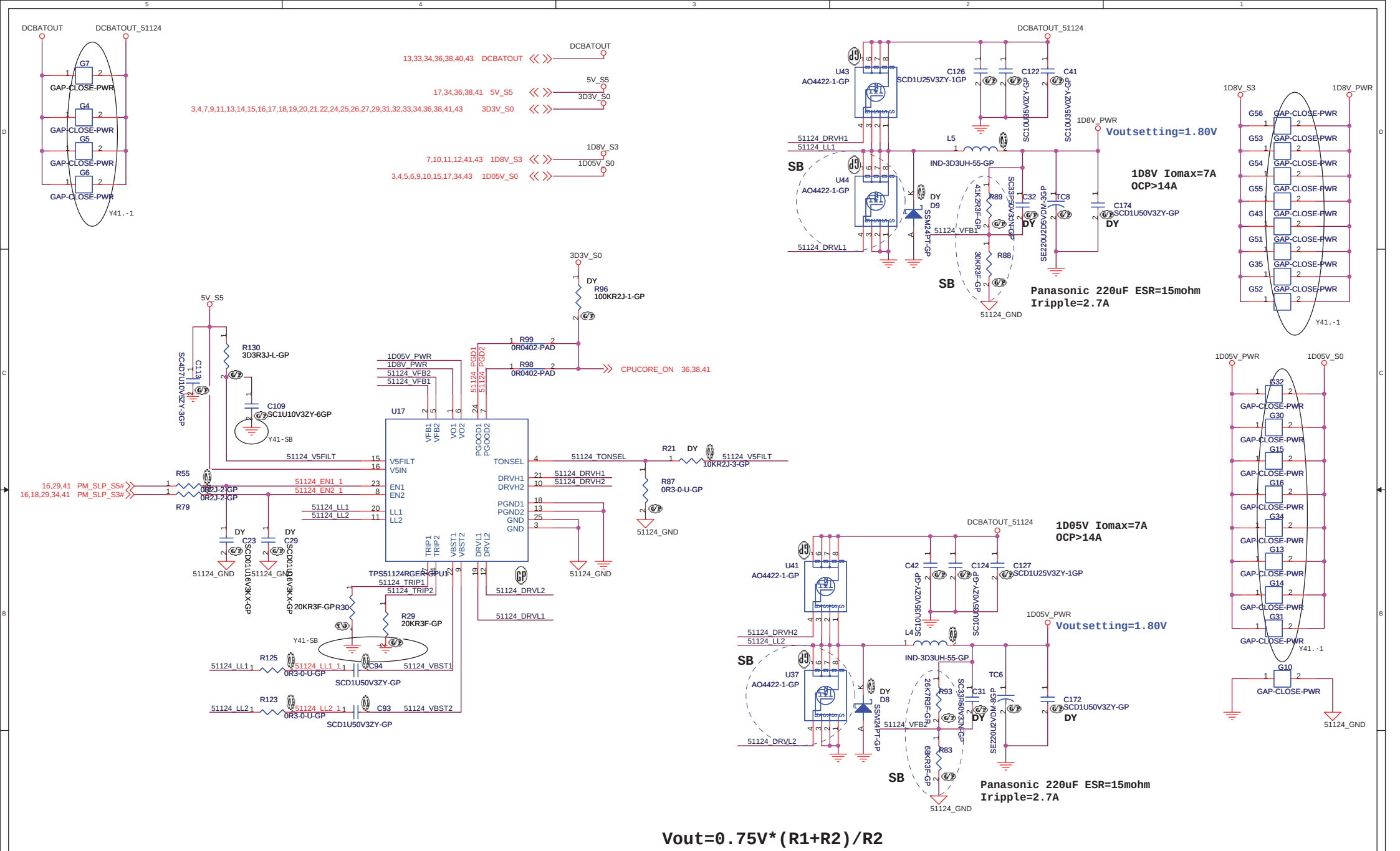
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_UP_S5/3D3V_S5/5V_S5

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 38 of 44



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

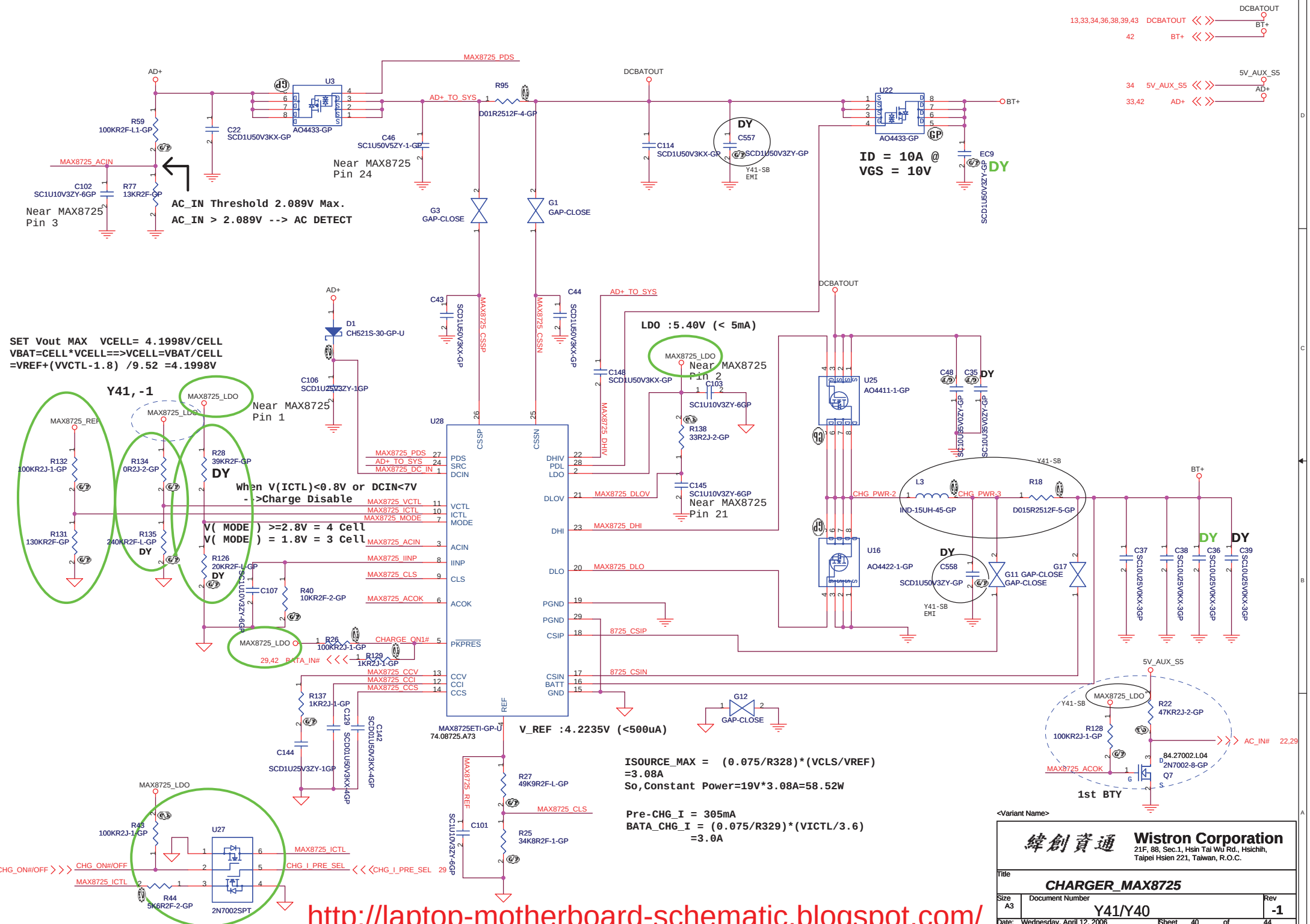
<Variant Name>

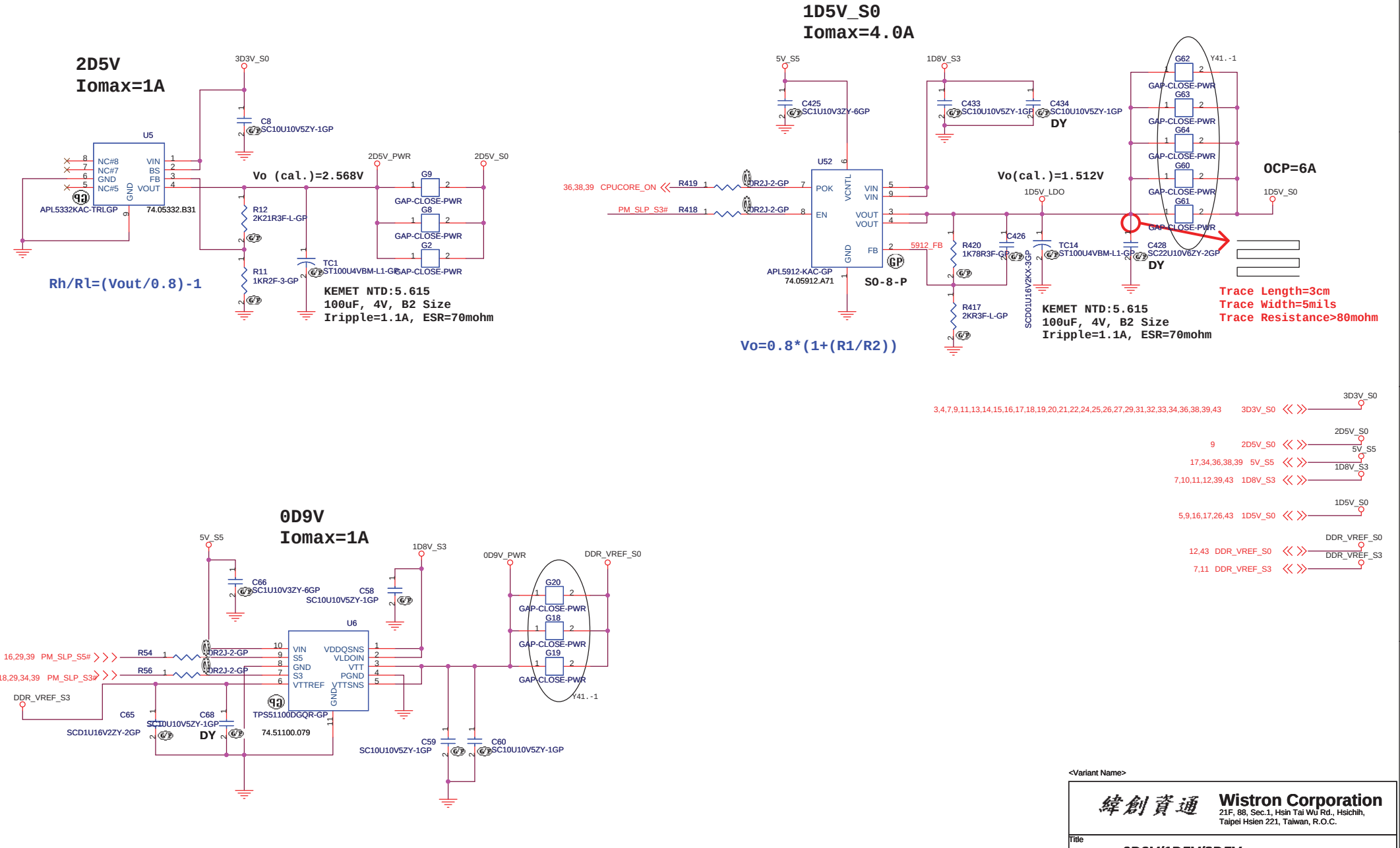
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Friday, May 26, 2006 | Sheet 39 of 44


SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
Y41,-1
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
LDO :5.40V (< 5mA)
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R328)*(VCLS/VREF)
=3.08A
So,Constant Power=19V*3.08A=58.52W
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R329)*(VICTL/3.6)
=3.0A
ID = 10A @
VGS = 10V
1st BTY
MAX8725_PDS
MAX8725_ACIN
MAX8725_LDO
MAX8725_REF
MAX8725_ICTL
MAX8725_IINP
MAX8725_CLS
MAX8725_ACOK
MAX8725_CCV
MAX8725_CCI
MAX8725_CCS
MAX8725_DLOV
MAX8725_DHI
MAX8725_CSSP
MAX8725_CSSN
MAX8725_DHIV
MAX8725_REF
MAX8725_CLS
AD+_TO_SYS
MAX8725_DC_IN
CHARGE_ON1#
CHG_ON#/OFF
CHG_I_PRE_SEL
BATA_IN#
8725_CSIP
8725_CSIN
DCBATOUT
BT+
5V_AUX_S5
AC_IN#
U3 AO4433-GP
U22 AO4433-GP
U25 AO4411-1-GP
U16 AO4422-1-GP
U27 2N7002SPT
U28 MAX8725ETI-GP-U 74.08725.A73
D1 CH521S-30-GP-U
Q7 84.27002.L04 2N7002-8-GP
L3 IND-15UH-45-GP
R59 100KR2F-L1-GP
R95 D01R2512F-4-GP
R28 39KR2F-GP
R132 100KR2J-1-GP
R134 0R2J-2-GP
R131 130KR2F-GP
R135 240KR2F-L-GP
R126 20KR2F-L-GP
R40 10KR2F-2-GP
R26 100KR2J-1-GP
R129 1KR2J-1-GP
R137 1KR2J-1-GP
R27 49K9R2F-L-GP
R25 34K8R2F-1-GP
R43 100KR2J-1-GP
R44 5K6R2F-2-GP
R138 33R2J-2-GP
R145 SC1U10V3ZY-6GP
R18 D015R2512F-5-GP
R22 47KR2J-2-GP
R128 100KR2J-1-GP
C22 SCD1U50V3KX-GP
C46 SC1U50V5ZY-1-GP
C114 SCD1U50V3KX-GP
C557 SCD1U50V3ZY-GP
EC9 SCD1U50V3ZY-GP
C102 SC1U10V3ZY-6GP
C106 SCD1U25V3ZY-1GP
C43 SCD1U50V3KX-GP
C44 SCD1U50V3KX-GP
C148 SCD1U50V3KX-GP
C103 SC1U10V3ZY-6GP
C107 SC1U10V3ZY-6GP
C144 SCD1U25V3ZY-1GP
C129 SCD01U50V3KX-4GP
C142 SCD01U50V3KX-4GP
C101 SC1U10V3ZY-6GP
C48 SC10U35V0ZY-GP
C35 SC10U35V0ZY-GP
C558 SCD1U50V3ZY-GP
C37 SC1U25V0KX-3GP
C38 SC1U25V0KX-3GP
C36 SC1U25V0KX-3GP
C39 SC1U25V0KX-3GP
G3 GAP-CLOSE
G1 GAP-CLOSE
G12 GAP-CLOSE
G11 GAP-CLOSE
G17 GAP-CLOSE
Y41-SB EMI
Near MAX8725 Pin 1
Near MAX8725 Pin 2
Near MAX8725 Pin 3
Near MAX8725 Pin 21
Near MAX8725 Pin 24
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER_MAX8725
Y41/Y40
-1
Wednesday, April 12, 2006
40
44
http://laptop-motherboard-schematic.blogspot.com/

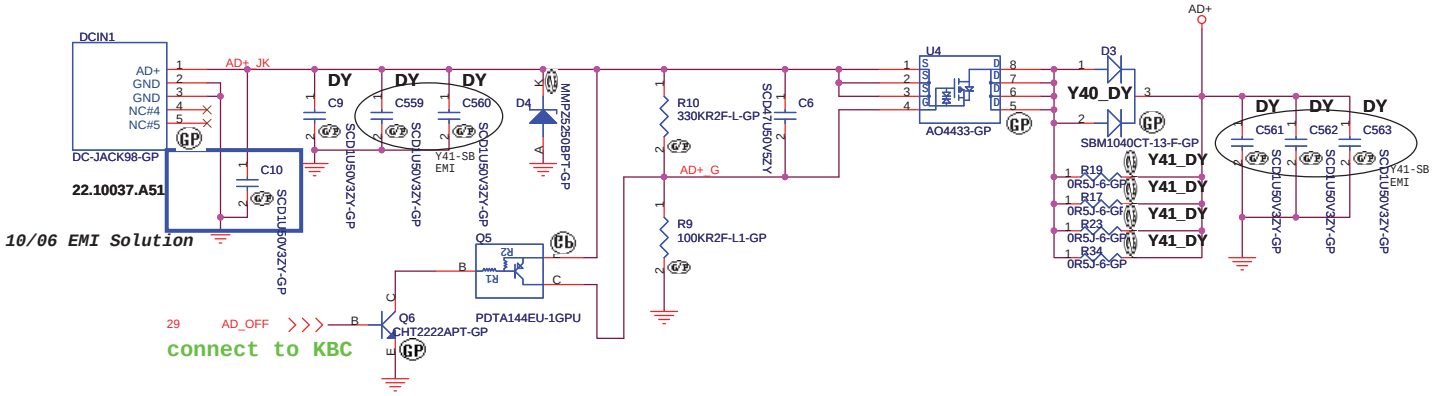


<Variant Name>

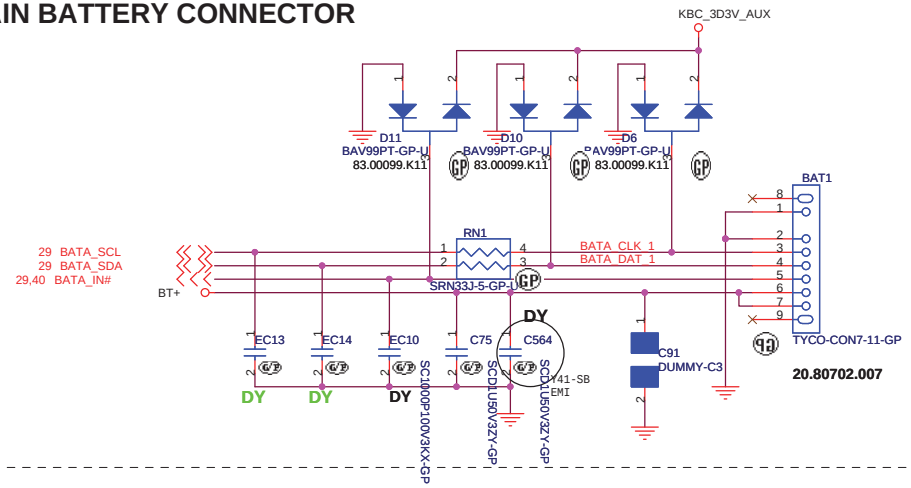
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	0D9V/1D5V/2D5V	
Size A3	Document Number Y41/Y40	Rev -1
Date: Wednesday, April 12, 2006	Sheet 41 of 44	

ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



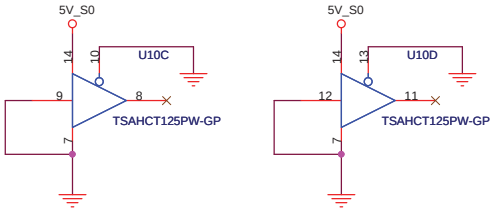
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 42 of 44



3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41 3D3V_S0 — 3D3V_S0

13,14,17,18,19,20,21,25,27,28,29,30,31,33,34,36 5V_S0 — 5V_S0

13,33,34,36,38,39,40 DCBATOUT — DCBATOUT

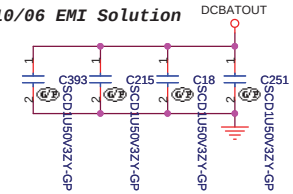
7,10,11,12,39,41 1D8V_S3 — 1D8V_S3

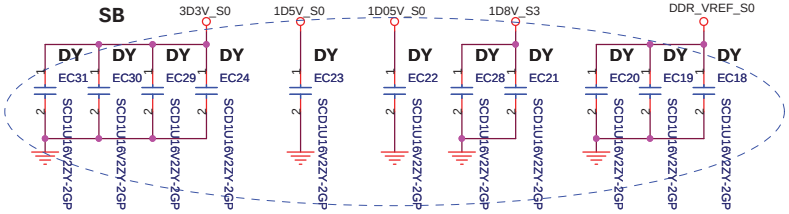
3,4,5,6,9,10,15,17,34,39 1D05V_S0 — 1D05V_S0

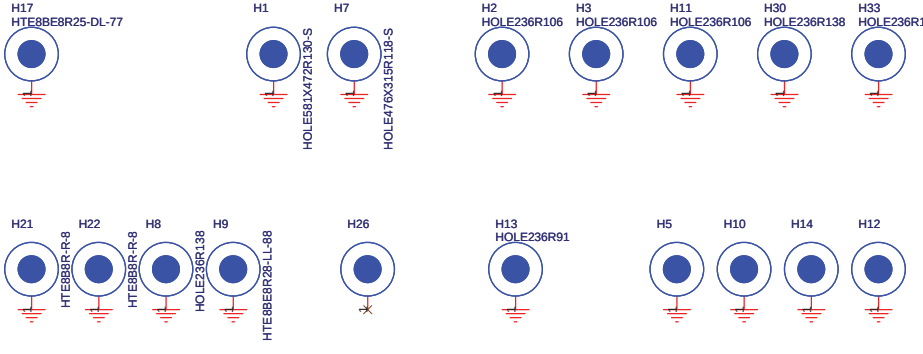
5,9,16,17,26,41 1D5V_S0 — 1D5V_S0

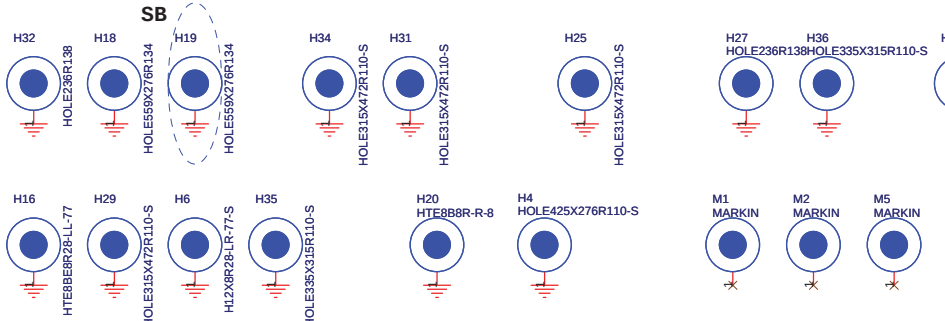
12,41 DDR_VREF_S0 — DDR_VREF_S0

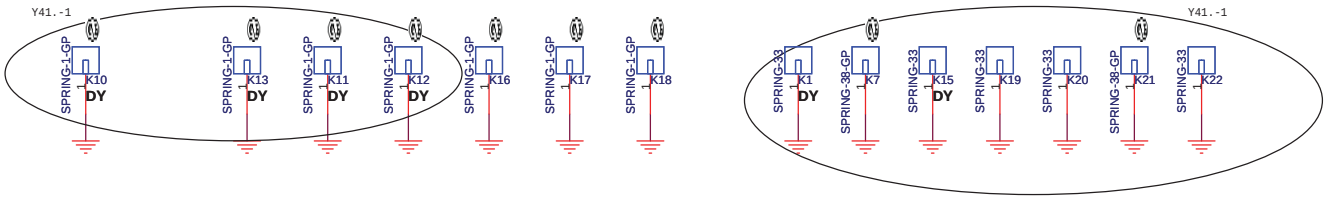
10/06 EMI Solution











<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SPRING & BOSS & EMI**

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 43 of 44

PRT modification list for Layout:

MINIC1, 62.10043.241
CDROM1, 20.80338.050
CN1, 20.80591.120
U9, 62.10079.001
U45, 71.88055.A03
U58, 71.AL861.00G

PRT modification list for Y41/Y41 BOM:

FAN1, 20.F0714.003
MINIC1, 62.10043.241
LAUNCH1, 20.K0196.005
U36, 74.02211.B39
U45, 71.88055.A03
U58, 71.AL861.00G
XF1, 68.2410S.30B
D2,D3 83.10R04.E87(Y41)
U50, 71.945GM.B0U
U29, 71.ICH7M.C0U
LCD1, 20.F0853.040
C6, 78.47494.41L
C280,C288, 78.10593.4FL
78.10221.2F1 <> 78.10221.2FL

H32, 34.46I14.001
H27, 34.46I14.001
H18, 34.46I14.001
H14, 34.4B604.001
H10, 34.4B604.001
H30, 34.4B601.001
H33, 34.4B601.001
H5, 34.4B602.001
H8, 34.4B603.001

Del K2~K6,K8,K9

Change parts to meet vista as below:
78.22521.5BL; 2.2uF 16V 0603 X5R; C522,C531.(Original:78.10593.4BL,1uF)
78.47521.51L(SCH改78.47522.51L); 4.7uF 16V 0805 X5R; C363,C364,C357,C358.(Original:78.22591.41L,2.2uF)
63.22334.1DL; 22K Ohm F 0402; R483,R484.(Original:63.10234.1DL,1K Ohm)
C575 Dummy.(Original:78.10134.1FL,100pF)
64.20025.6DL; 20K Ohm F 0402; R332.(Original:64.51015.6DL,5.1K Ohm)
63.R0034.1DL; 0 Ohm J 0402; R531.(Original:63.47034.1DL,47 Ohm)
71.AL861.A0G; ALC861-VD; U58.(Original:71.AL861.00G,ALC861)

Daughter Board information:

LAUNCH/B Layout Revision: 05572-1.
LAUNCH/B PCB P/N: 48.4P502.011

USB/B Layout Revision: 05573-1.
USB/B PCB P/N: 48.4P503.011

Port Replicator/B Layout Revision: 05579-1.
Port replicator/B PCB P/N: 48.4P504.011

Key part list:

Modification list:

<Variant Name>

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Title: Remark

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, December 06, 2006 Sheet 44 of 44