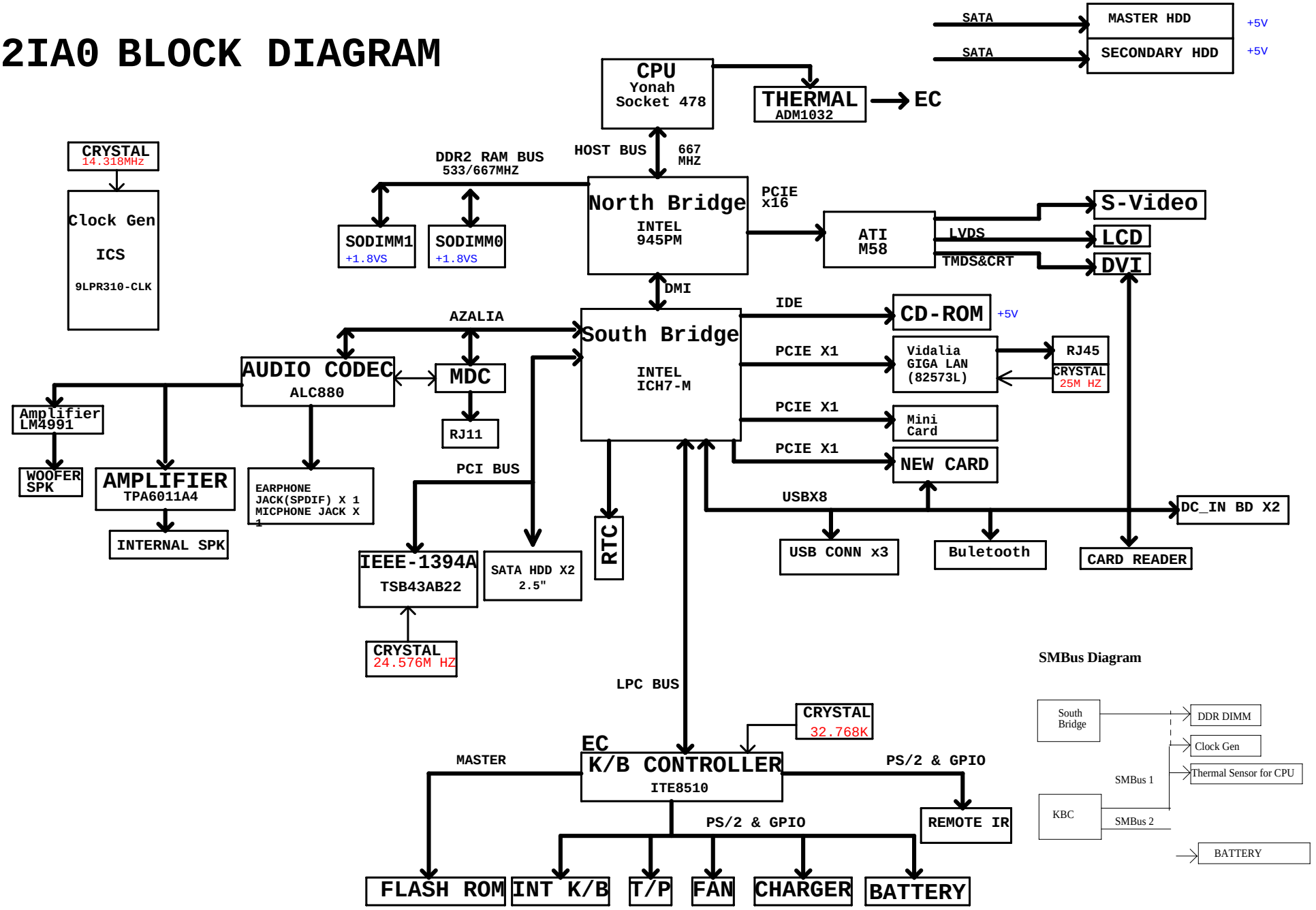
Model : P72IA0

Intel Yonah CPU + 945PM / ICH7-M Chipset

Revision History		
	09/2005	RA
	10/2005	RB

UNIWILL COMPUTER CORP.			
Title: P72IA0			
Size	Document Number: 3220 INDEX		Rev: B
Date: Wednesday, October 19, 2005	Sheet 1 of 33		

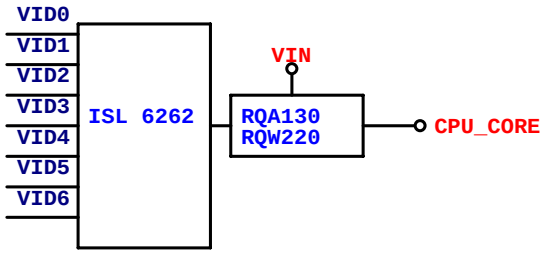
P72IA0 BLOCK DIAGRAM

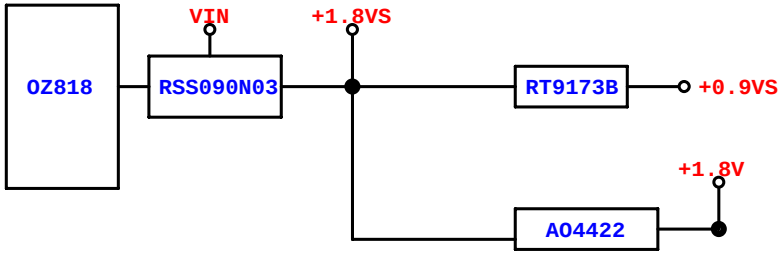


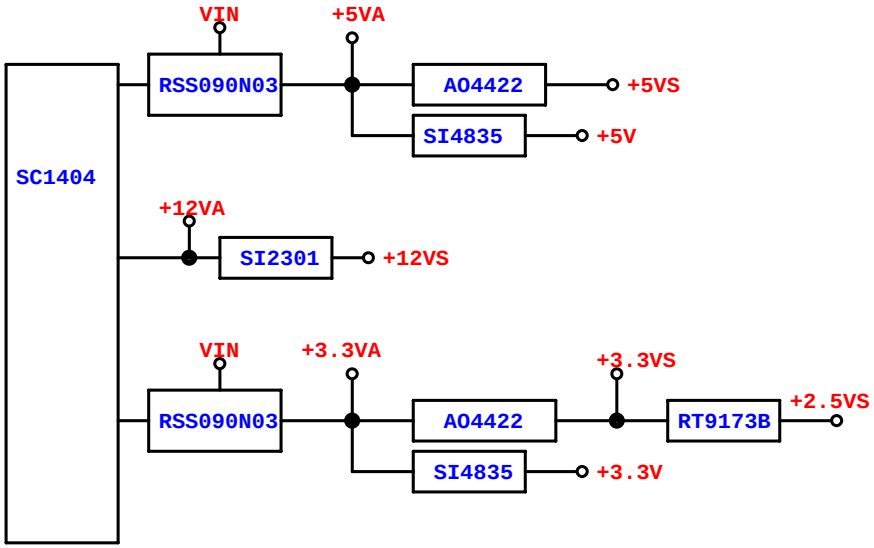
SMBus Diagram

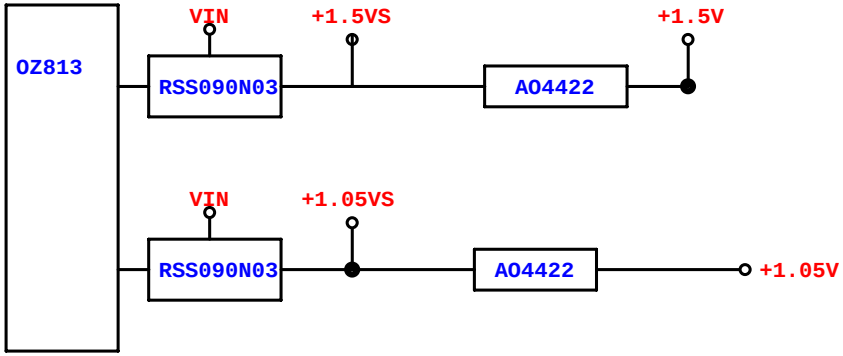
UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size	Document Number: 3220 SYSTEM BLOCK DIAGRAM	Rev B
Date: Wednesday, October 19, 2005	Sheet 2 of 33	

POWER BLOCK DIAGRAM

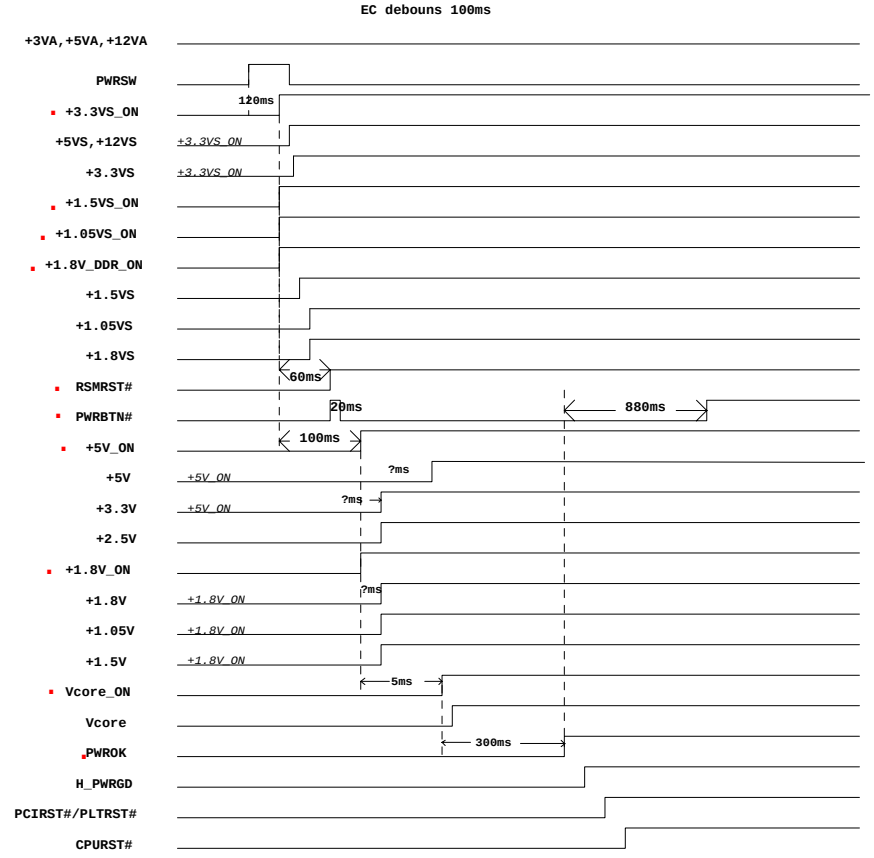








POWER Sequence



▪ EC Control Pin

UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size: C	Document Number: 3220 POWER DIAGRAM	Rev: B
Date: Wednesday, October 19, 2005	Sheet 3 of 33	

ICH6-M GPIO

GPI0	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GPO18	PM_STPPCI_ICH#
GPO19	
GPO20	PM_STPCPU_ICH#
GPO21	TPM_EN
GPO23	
GPIO24	
GPIO25	
GPIO26	SATA0_GP
GPIO27	
GPIO28	
GPIO29	PNLSW1
GPIO30	PNLSW2
GPIO31	PNLSW0
GPIO32	PM_CLKRUN#
GPIO33	
GPIO34	

ITE8510E GPIO

GPCF0	RF_SW#
GPCF1	SILENT#/
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#
GPCF7	BROWSER#
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	***VOLMAX***
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	TP_DISABLE
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	CELERON_VO_DET
GPB1	CPPE#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	***NA***
GPE1	CPU_BSEL0
GPE2	***NA***
GPE3	***NA***
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	EC_PREST#
GPA0	BTL_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO

GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1
GPC4	SB_ALERT#2
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	***NA***

CPU

	CPU CORE(V)	ICC(mA)	W	TEMP(℃)
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_GMCH_CORE	266	0.452	

ICH6-M

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

ITE8510E

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	300	1	70

CLOCK GENERATOR

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	180	0.594	70

ALC880

VCC	ICC(mA)	W	TEMP(℃)
+3.3V(DVDD)	71	0.234	70

TPA6011A4

VCC	ICC(mA)	W	TEMP(℃)
3.3V	30	0.099W	85

ADM1032

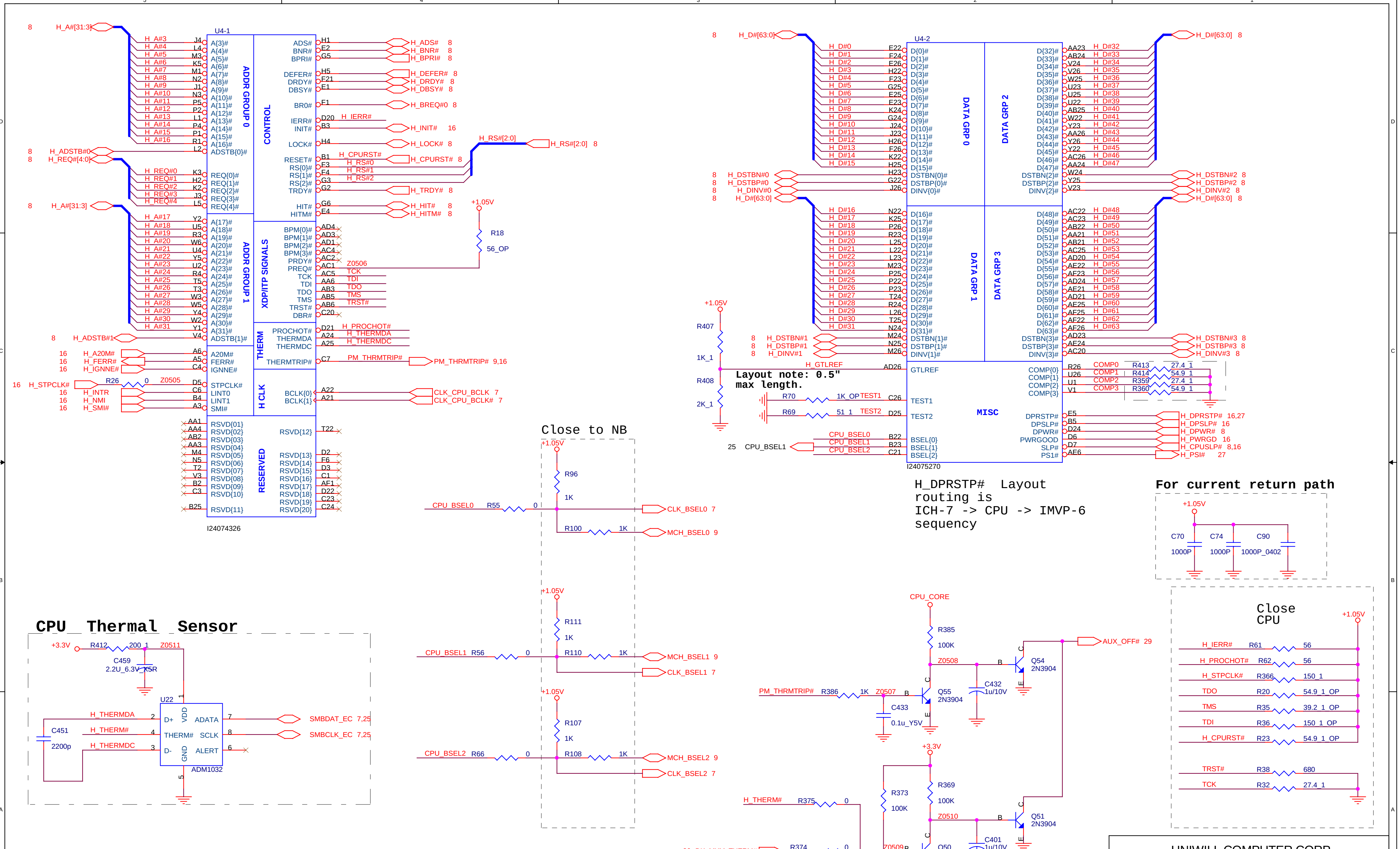
VCC	ICC	W	TEMP(℃)
+3.3V	170uA	0.56mW	150

UNIWILL COMPUTER CORP.

Title: P72IA0

Size: C | Document Number: 3220 | GPIO & POWER CONSU | Rev: B

Date: Wednesday, October 19, 2005 | Sheet 4 of 33



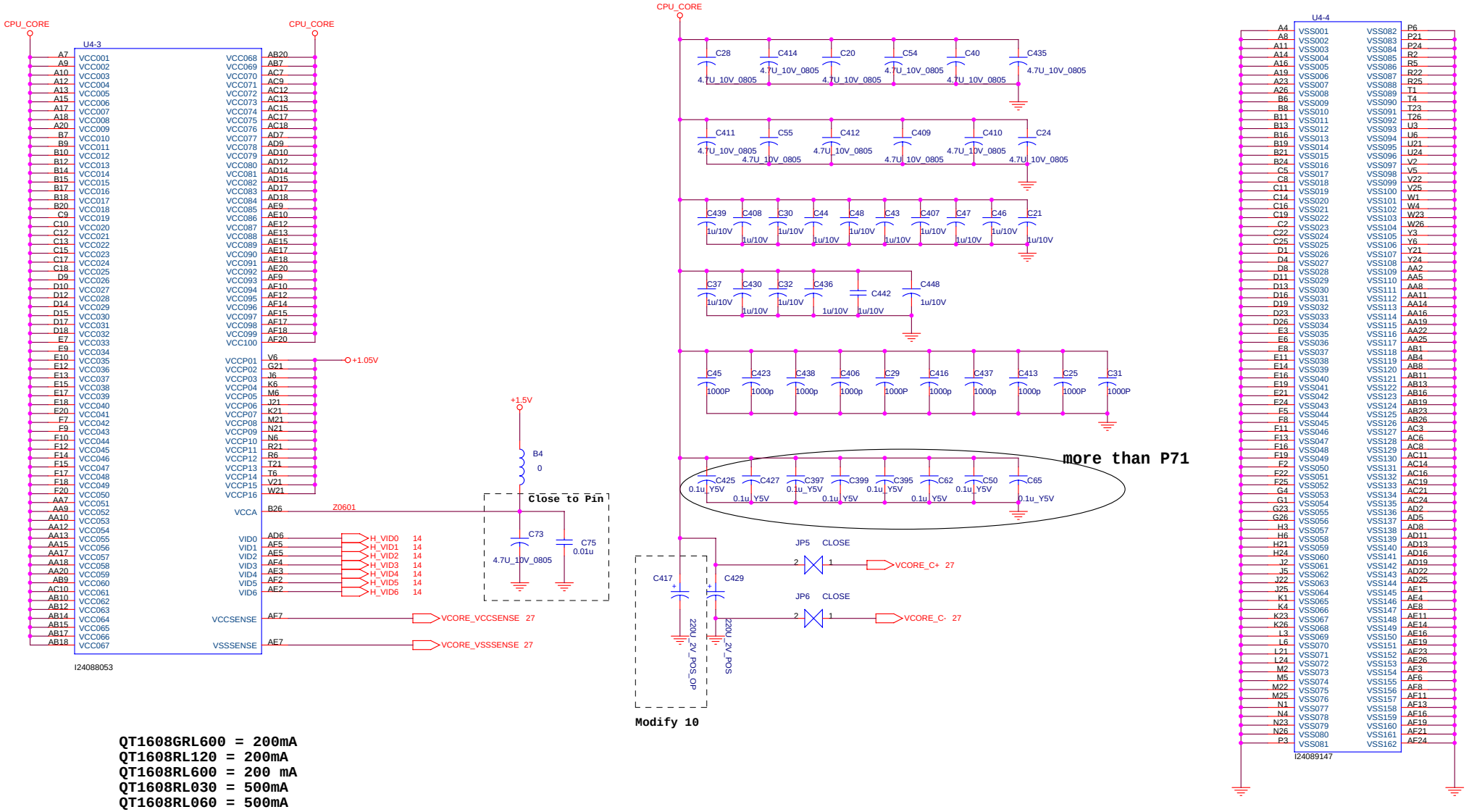
	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

UNIWILL COMPUTER CORP.

Title: P72IA0

Size: 3220 | Document Number: CPU Yonah-1/2 | Rev: B

Date: Wednesday, October 19, 2005 | Sheet 5 of 33

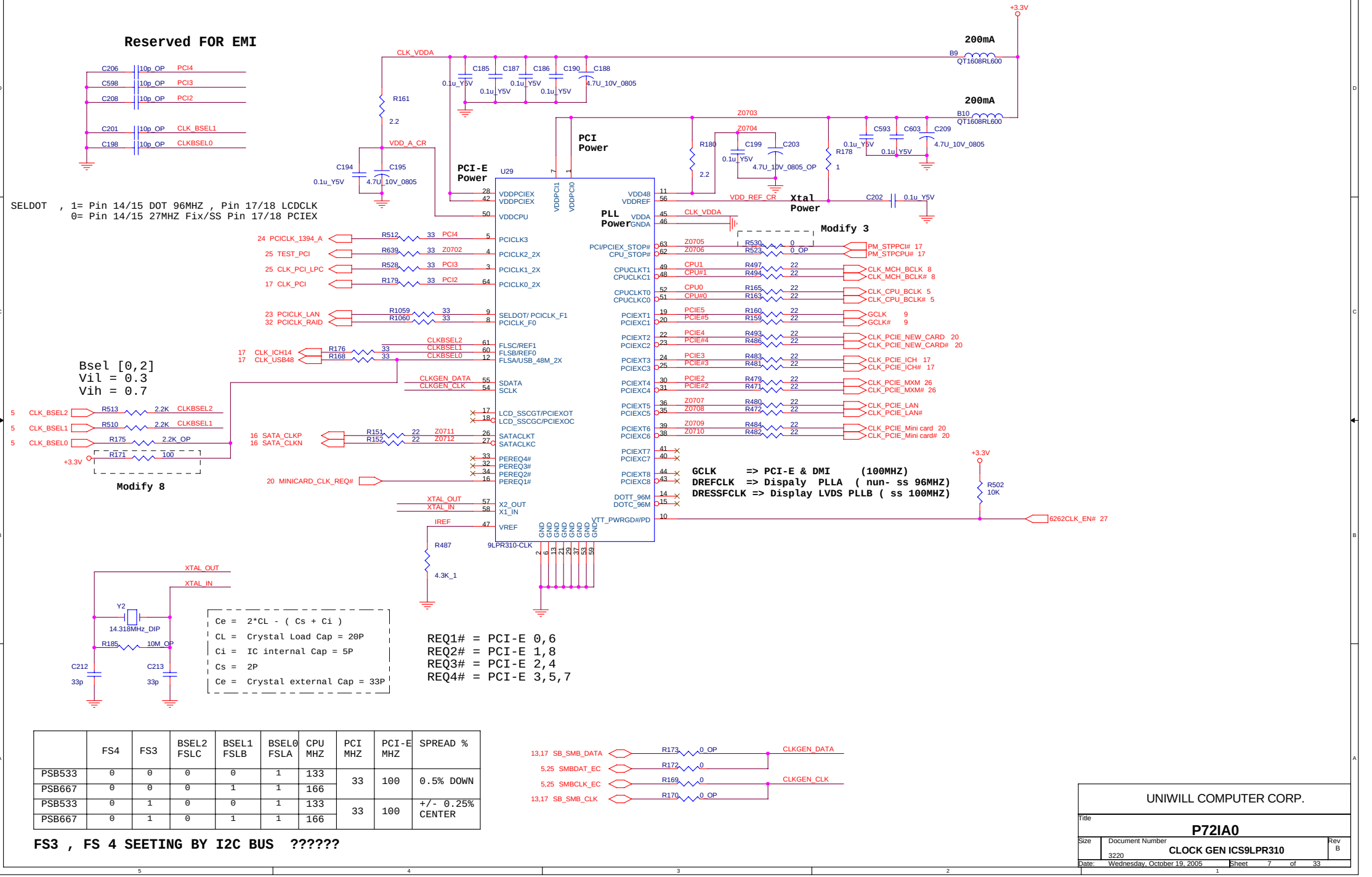


UNIWILL COMPUTER CORP.

Title: **P72IA0**

Size	Document Number	Rev
	3220 **CPU Yonah-2/2**	B

Date: Wednesday, October 19, 2005 Sheet 6 of 33



	FS4	FS3	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ	SPREAD %
PSB533	0	0	0	0	1	133	33	100	0.5% DOWN
PSB667	0	0	0	1	1	166			
PSB533	0	1	0	0	1	133	33	100	+/- 0.25% CENTER
PSB667	0	1	0	1	1	166			

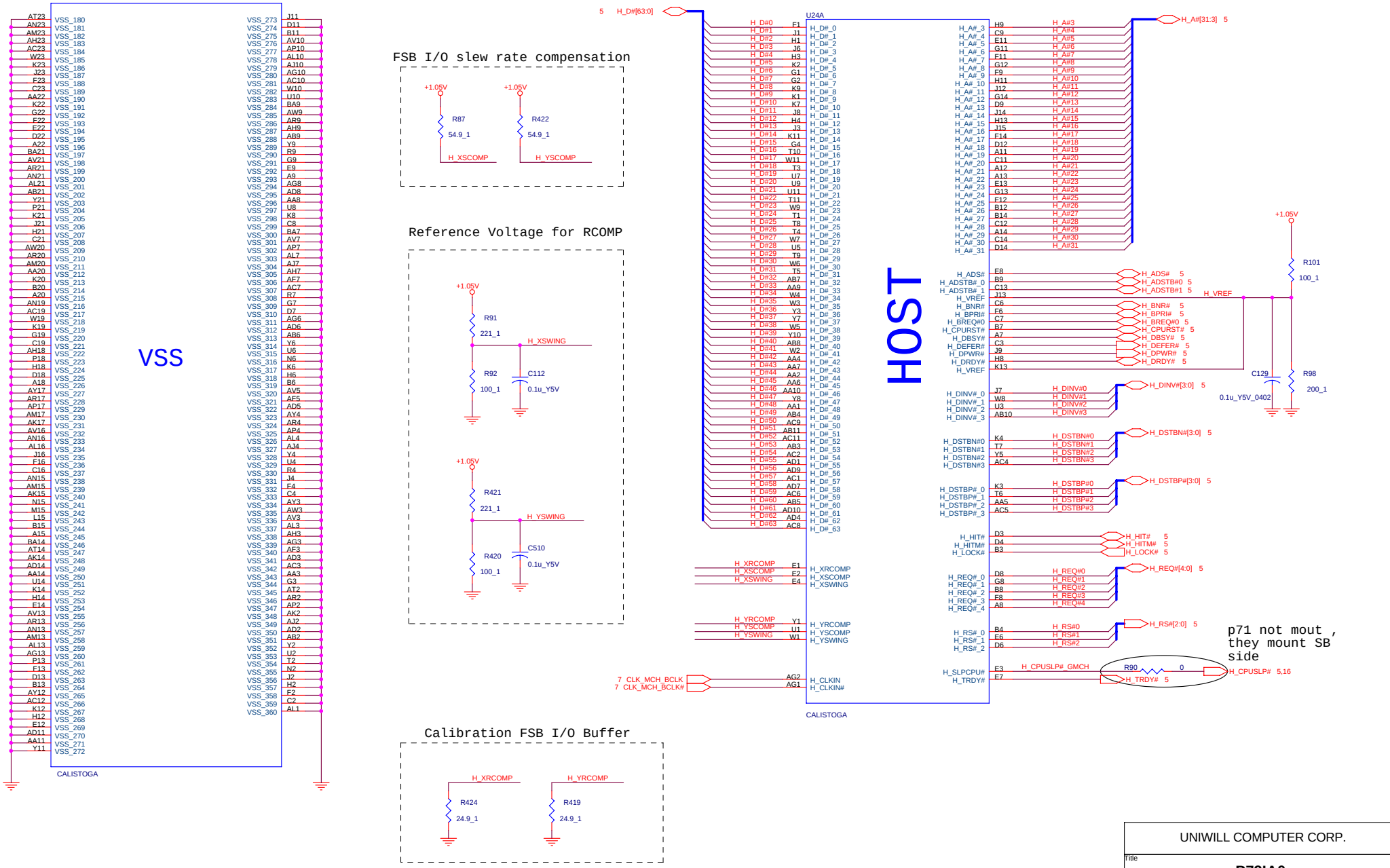
FS3 , FS 4 SEETING BY I2C BUS ??????

UNIWILL COMPUTER CORP.

Title: **P72IA0**

Size | Document Number: 3220 **CLOCK GEN ICS9LPR310** | Rev B

Date: Wednesday, October 19, 2005 | Sheet 7 of 33



UNIWILL COMPUTER CORP.

Title

P72IA0

Size	Document Number	Rev
	NB_945PM-1/5	B
	3220	

Date: Wednesday, October 19, 2005 Sheet 8 of 33

U24B

DMI
DMI_RXP[3:0] → DMI_RXP3 AG41, DMI_RXP2 AF37, DMI_RXP1 AE41, DMI_RXP0 AC37
DMI_RXN[3:0] → DMI_RXN3 AH41, DMI_RXN2 AG37, DMI_RXN1 AF41, DMI_RXN0 AE37
DMI_TXP[3:0] → DMI_TXP3 AG39, DMI_TXP2 AF35, DMI_TXP1 AE39, DMI_TXP0 AC35
DMI_TXN[3:0] → DMI_TXN3 AH39, DMI_TXN2 AG35, DMI_TXN1 AF39, DMI_TXN0 AE35
DMI_TXP_3, DMI_TXP_2, DMI_TXP_1, DMI_TXP_0
DMI_TXN_3, DMI_TXN_2, DMI_TXN_1, DMI_TXN_0
DMI_RXP_3, DMI_RXP_2, DMI_RXP_1, DMI_RXP_0
DMI_RXN_3, DMI_RXN_2, DMI_RXN_1, DMI_RXN_0

NC
NC18 A3, NC17 A39, NC16 A4, NC15 A40, NC14 AW1, NC13 AW41, NC12 AY1, NC11 AY41, NC10 B2, NC9 B41, NC8 BA1, NC7 BA2, NC6 BA3, NC5 BA39, NC4 BA40, NC3 BA41, NC2 C1, NC1 C41, NC0 D1

MISC
CLK_REQ# H32 — Z0907 — R117 0_OP — +1.5V
LT_RESET# K28 — NB_SYNC# 17
SDVO_CTRLDATA H27
SDVO_CTRLCLK H28

Asserted to control the raw PCI-E clock

Asserted to synchronize with ICH on fault

PM
RSTIN# AH34 — Z0911 — R157 100 — PLT_RST# 17,19,20,25,26
PWROK AH33 — DELAY_VR_PWRGOOD — DELAY_VR_PWRGOOD 17
PM_THRMTRIP# G6 — ICH7_THRMTRIP#
PM_EXTTS#_1 H26 — PM_EXTTS#1 — R112 0 — D6 BAT54 — PM_DPRSLPVR 17,27
PM_EXTTS#_0 F25 — PM_EXTTS#0 — A — C — EXTTS#0 14,25
PM_BMBUSY# G28 — BM_BUSY# 17

GHCH integrated graphics busy

CLK
R468 0 Z0901 D41
R470 0 Z0902 C40
R438 0 Z0906 A26
R441 0 Z0912 A27
GCLK AG33
GCLK# AF33
D_REFSSCLKIN, D_REFSSCLKIN#, D_REFCLKIN, D_REFCLKIN#, G_CLKIN, G_CLKIN#

DDR MUXING
M_VREF_MCH → SM_VREF_1 AK41, SM_VREF_0 AK1
M_RCOMPP → SM_RCOMP AT9
M_RCOMPN → SM_RCOMP# AV9
SM_ODT_3 AU21, SM_ODT_2 AY20, SM_ODT_1 BA12, SM_ODT_0 BA13
13,14 MB_ODT3, 13,14 MB_ODT2, 13,14 MA_ODT1, 13,14 MA_ODT0
M_OCDCOMP1 → SM_OCDCOMP_1 AF10
M_OCDCOMP0 → SM_OCDCOMP_0 AL20
as short as possible
R97, R106, 40.2_1_OP, 40.2_1_OP
SM_CS#_3 AW21, SM_CS#_2 AY21, SM_CS#_1 AW12, SM_CS#_0 AW13
13,14 MB_CS#3, 13,14 MB_CS#2, 13,14 MA_CS#1, 13,14 MA_CS#0
SM_CKE_3 AY29, SM_CKE_2 BA29, SM_CKE_1 AT20, SM_CKE_0 AU20
13,14 MB_CKE3, 13,14 MB_CKE2, 13,14 MA_CKE1, 13,14 MA_CKE0
SM_CK#_3 AY40, SM_CK#_2 AY7, SM_CK#_1 AT1, SM_CK#_0 AW35
13 MB_CK#3, 13 MB_CK#4, 13 MA_CK#1, 13 MA_CK#0
SM_CK_3 AW40, SM_CK_2 AW7, SM_CK_1 AR1, SM_CK_0 AY35
13 MB_CK3, 13 MB_CK4, 13 MA_CK1, 13 MA_CK0

CFG
CFG_20 J26, CFG_19 K27 — CFG19 12
CFG_18 J25 — CFG18 12
CFG_17 H15, CFG_16 G18 — CFG16 12
CFG_15 H16, CFG_14 C15, CFG_13 K15 — Z0903 — R104 1K_OP, CFG_12 G15 — Z0904 — R105 1K_OP, CFG_11 D15, CFG_10 E16
CFG_9 G16 — CFG9 12
CFG_8 D16, CFG_7 D19, CFG_6 F18
CFG_5 F15 — CFG5 12
CFG_4 E15, CFG_3 F18
CFG_2 J18 — MCH_BSEL2 5
CFG_1 K18 — MCH_BSEL1 5
CFG_0 K16 — MCH_BSEL0 5

Base on RSTIN#

RSVD
RSVD_13 D27, RSVD_12 D28, RSVD_11 A34, RSVD_10 A35, RSVD_9 A41, RSVD_8 J19, RSVD_7 H7, RSVD_6 AF11, RSVD_5 AG11, RSVD_4 F7, RSVD_3 F3, RSVD_2 R32, RSVD_1 T32

+1.05V — C196 1000P

CALISTOGA

U24C

LVDS
L_BKLTCTL D32, L_BKLTEN J30, L_CLKCTLA H30, L_CLKCTLB H29, L_DDC_CLK G26, L_DDC_DATA G25, L_IBG B38, L_VBG C35, L_VDDEN F32, L_VREFH C33, L_VREFL C32
LA_CLK# A33, LA_CLK A32, LB_CLK# E27, LB_CLK E26
LA_DATA#_0 C37, LA_DATA#_1 B35, LA_DATA#_2 A37
LA_DATA_0 B37, LA_DATA_1 B34, LA_DATA_2 A36
LB_DATA#_0 G30, LB_DATA#_1 D30, LB_DATA#_2 F29
LB_DATA_0 F30, LB_DATA_1 D29, LB_DATA_2 F28

TV
+1.5V
TV_DACA_OUT A16, TV_DACB_OUT C18, TV_DACC_OUT A19
TV_IREF J20, TV_IRTNA B16, TV_IRTNB B18, TV_IRTNC B19
O/A
TV_DCONSEL0 K30, TV_DCONSEL1 J29

VGA
+1.05V
CRT_BLUE E23, CRT_BLUE# D23, CRT_GREEN C22, CRT_GREEN# B22, CRT_RED A21, CRT_RED# B21
CRT_DDC_CLK C26, CRT_DDC_DATA C25, CRT_HSYNC G23, CRT_IREF J22, CRT_VSYNC H23

PCI-EXPRESS GRAPHICS
EXP_A_COMPI D40 — PEG_COMP — R469 24.9_1 — +1.5V
EXP_A_COMPO D38
EXP_A_RXN_0 F34, EXP_A_RXN_1 G38, EXP_A_RXN_2 H34, EXP_A_RXN_3 J38, EXP_A_RXN_4 L34, EXP_A_RXN_5 M38, EXP_A_RXN_6 N34, EXP_A_RXN_7 P38, EXP_A_RXN_8 R34, EXP_A_RXN_9 T38, EXP_A_RXN_10 V34, EXP_A_RXN_11 W38, EXP_A_RXN_12 Y34, EXP_A_RXN_13 AA38, EXP_A_RXN_14 AB34, EXP_A_RXN_15 AC38 — PEG_RXN[15..0] 26
EXP_A_RXP_0 D34, EXP_A_RXP_1 F38, EXP_A_RXP_2 G34, EXP_A_RXP_3 H38, EXP_A_RXP_4 J34, EXP_A_RXP_5 L38, EXP_A_RXP_6 M34, EXP_A_RXP_7 N38, EXP_A_RXP_8 P34, EXP_A_RXP_9 R38, EXP_A_RXP_10 T34, EXP_A_RXP_11 V38, EXP_A_RXP_12 W34, EXP_A_RXP_13 Y38, EXP_A_RXP_14 AA34, EXP_A_RXP_15 AB38 — PEG_RXP[15..0] 26
EXP_A_TXN_0 F36, EXP_A_TXN_1 G40, EXP_A_TXN_2 H36, EXP_A_TXN_3 J40, EXP_A_TXN_4 L36, EXP_A_TXN_5 M40, EXP_A_TXN_6 N36, EXP_A_TXN_7 P40, EXP_A_TXN_8 R36, EXP_A_TXN_9 T40, EXP_A_TXN_10 V36, EXP_A_TXN_11 W40, EXP_A_TXN_12 Y36, EXP_A_TXN_13 AA40, EXP_A_TXN_14 AB36, EXP_A_TXN_15 AC40 — PEG_TXN[15..0] 26
EXP_A_TXP_0 D36, EXP_A_TXP_1 F40, EXP_A_TXP_2 G36, EXP_A_TXP_3 H40, EXP_A_TXP_4 J36, EXP_A_TXP_5 L40, EXP_A_TXP_6 M36, EXP_A_TXP_7 N40, EXP_A_TXP_8 P36, EXP_A_TXP_9 R40, EXP_A_TXP_10 T36, EXP_A_TXP_11 V40, EXP_A_TXP_12 W36, EXP_A_TXP_13 Y40, EXP_A_TXP_14 AA36, EXP_A_TXP_15 AB40 — PEG_TXP[15..0] 26

CALISTOGA

GCLK => PCI-E & DMI (100MHZ)
DREFCLK => Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

SDVODATA has internal pull down
0= no DVO device
1= DVO device present
SDVOCLK has internal pull down .

Only Base on Discreted VGA

VCCA_DPLLA , VCCA_DPLLB => NC
DREF_CLKP / DREF_SSCLKP = GND
DREF_CLKN / DREF_SSCLKN = GND

VCCA_DPLLA , VCCA_DPLLB =>1.5V
DREF_CLKP / DREF_SSCLKP = 1.5V
DREF_CLKN / DREF_SSCLKN = GND

CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	533
1	1	0	667

CFG20 (IPD) => 1= Only SDVO or PCI-E
0 = SDVO and PCI-E

CFG7 (IPU) => 1= Mobility CPU
0 = Reverse

+1.8VS
R89 150_1, R88 150_1
0.05A, M_VREF_MCH
C169 0.1u_Y5V, C105 0.1u_Y5V

+1.8VS
R95 80.6_1 — M_RCOMPN
R94 80.6_1 — M_RCOMPP

For MEN bus throttling
+3.3V
R114 10K — PM_EXTTS#1
R115 10K — PM_EXTTS#0 — PM_EXTTS#0 13
Check with S/W

Reserve for NB THRMTRIP# (O/D Vccp)
IPU — ICH7_THRMTRIP# — C D5 A — BAT54_OP — PM_THRMTRIP# 5,16

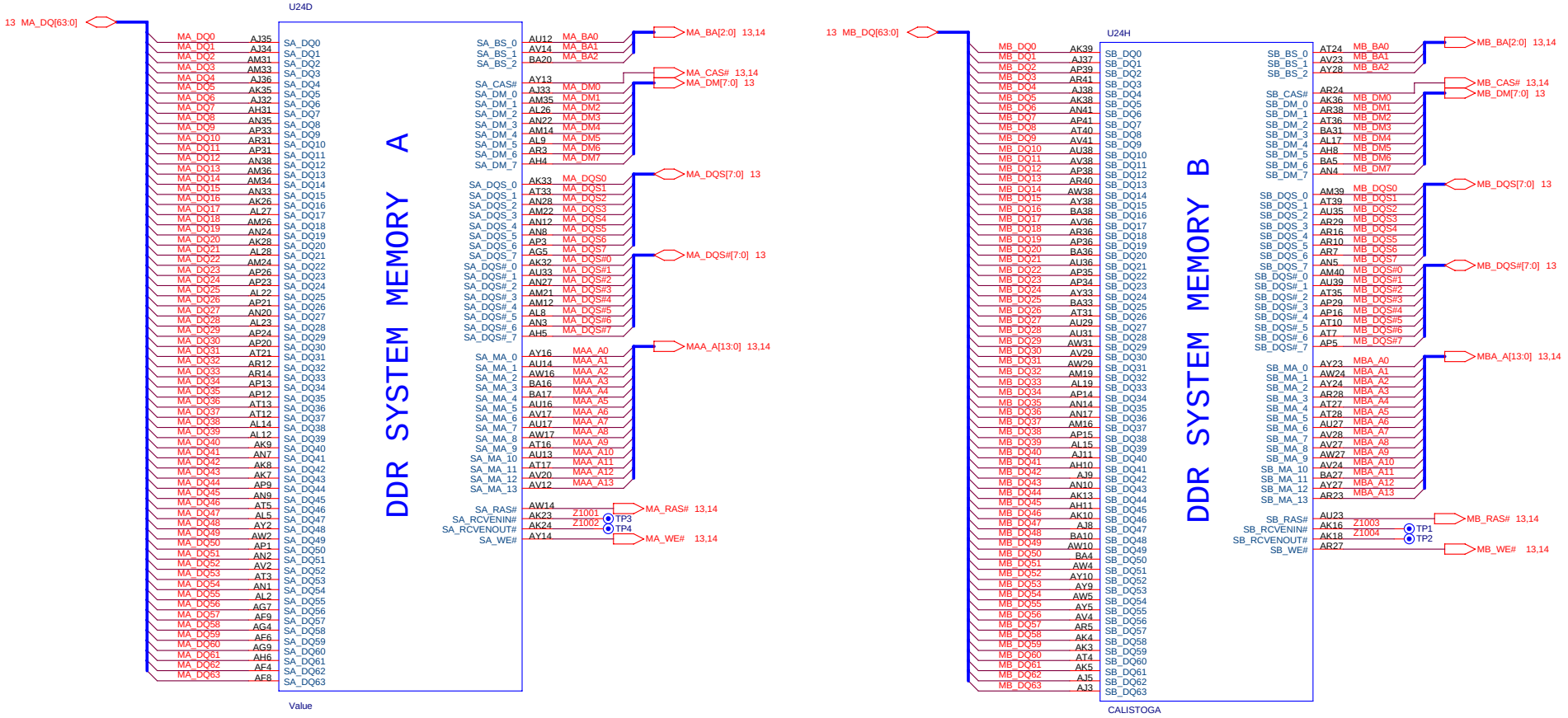
Colse to NB
DELAY_VR_PWRGOOD — C193 0.1u_Y5V

UNIWILL COMPUTER CORP.

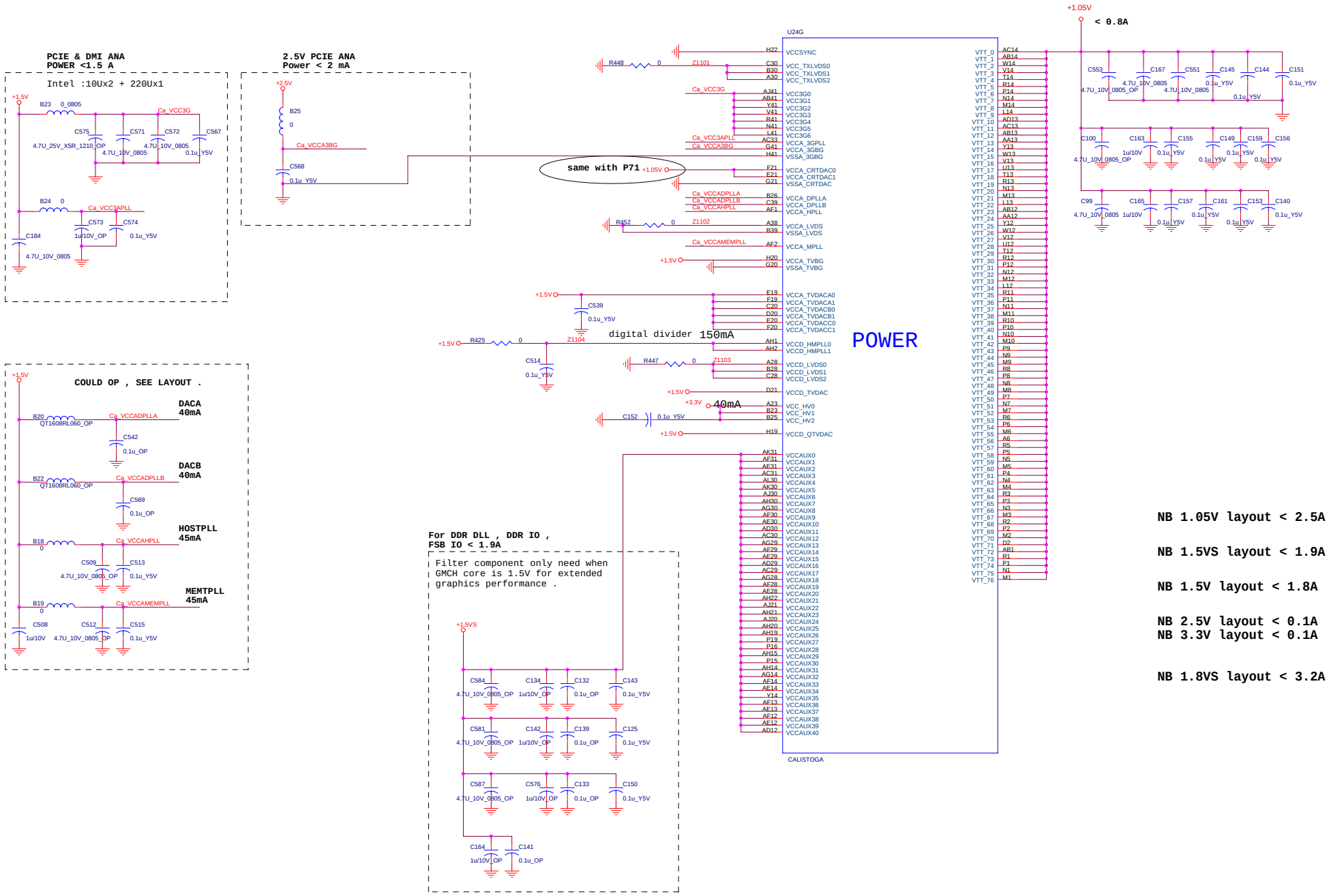
Title: **P72IA0**

Size | Document Number: 3220 **NB NB DDRCLK_VGA_PCIEXPR-2/5** | Rev B

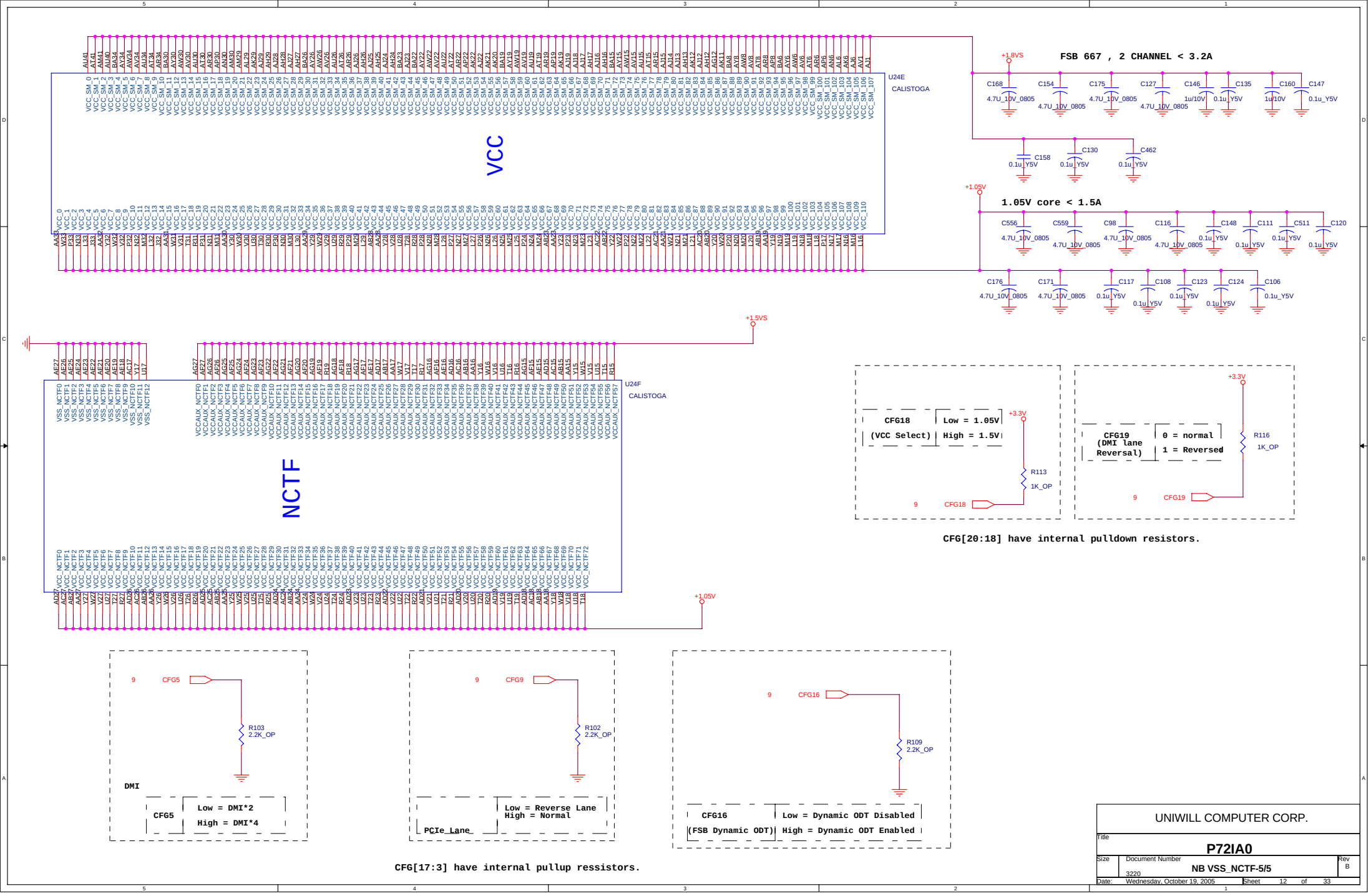
Date: Wednesday, October 19, 2005 | Sheet 9 of 33



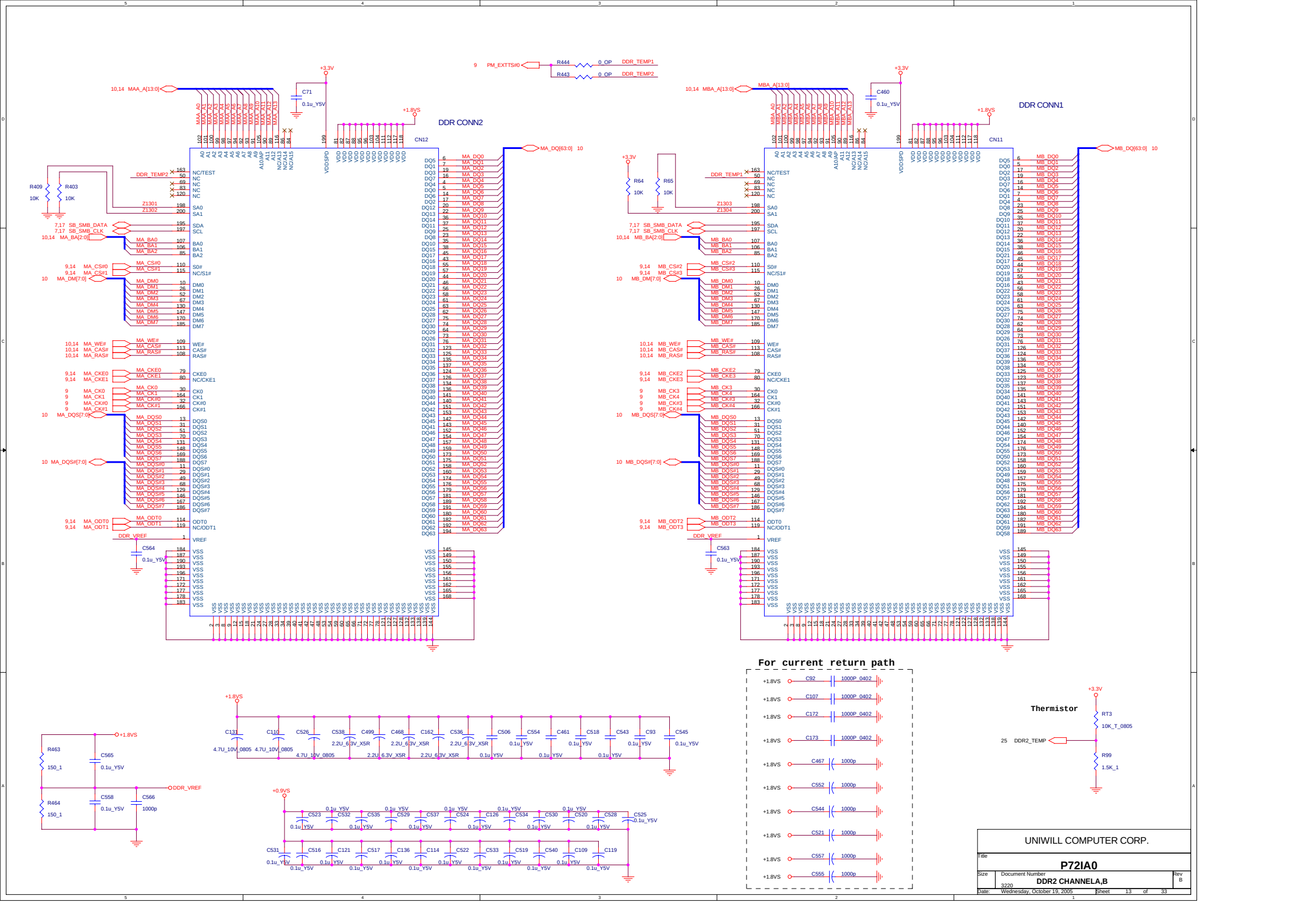
UNIWILL COMPUTER CORP.		
Title	P72IA0	
Size	Document Number 3220 NB DDR_MEM SYSTEM-3/5	Rev B
Date: Wednesday, October 19, 2005	Sheet 10 of 33	



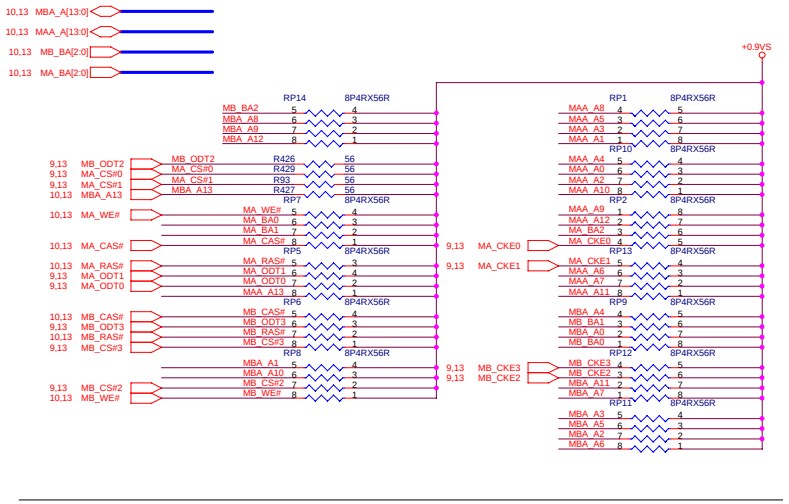
UNIWILL COMPUTER CORP.		
Title	P72IA0	
Size	Document Number 3220	Rev B
	NB POWER-4/5	
Date: Wednesday, October 19, 2005	Sheet 11 of 33	



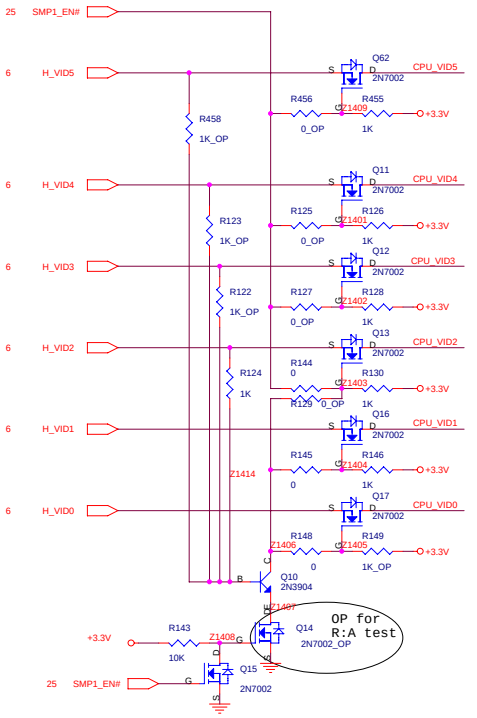
UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size	Document Number: NB VSS_NCTF-5/5	Rev: B
	3220	
Date: Wednesday, October 19, 2005	Sheet 12 of 33	

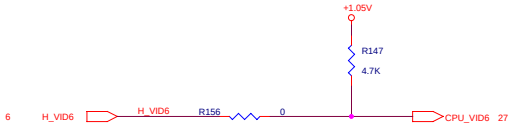

DDR CONN2
DDR CONN1
For current return path
Thermistor
UNIWILL COMPUTER CORP.
P72IA0
DDR2 CHANNELA,B
3220
Wednesday, October 19, 2005
Sheet 13 of 33

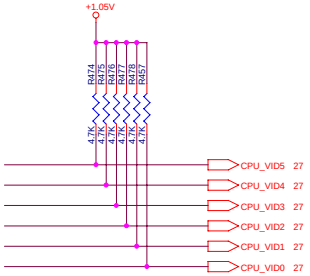
SMART POWER



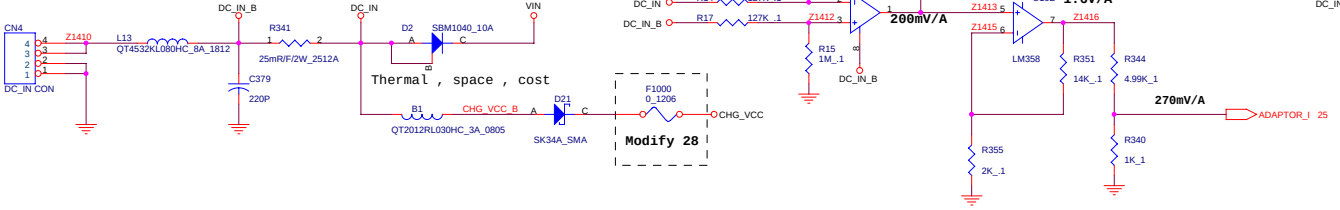
VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

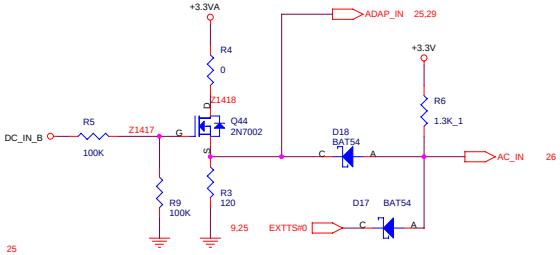




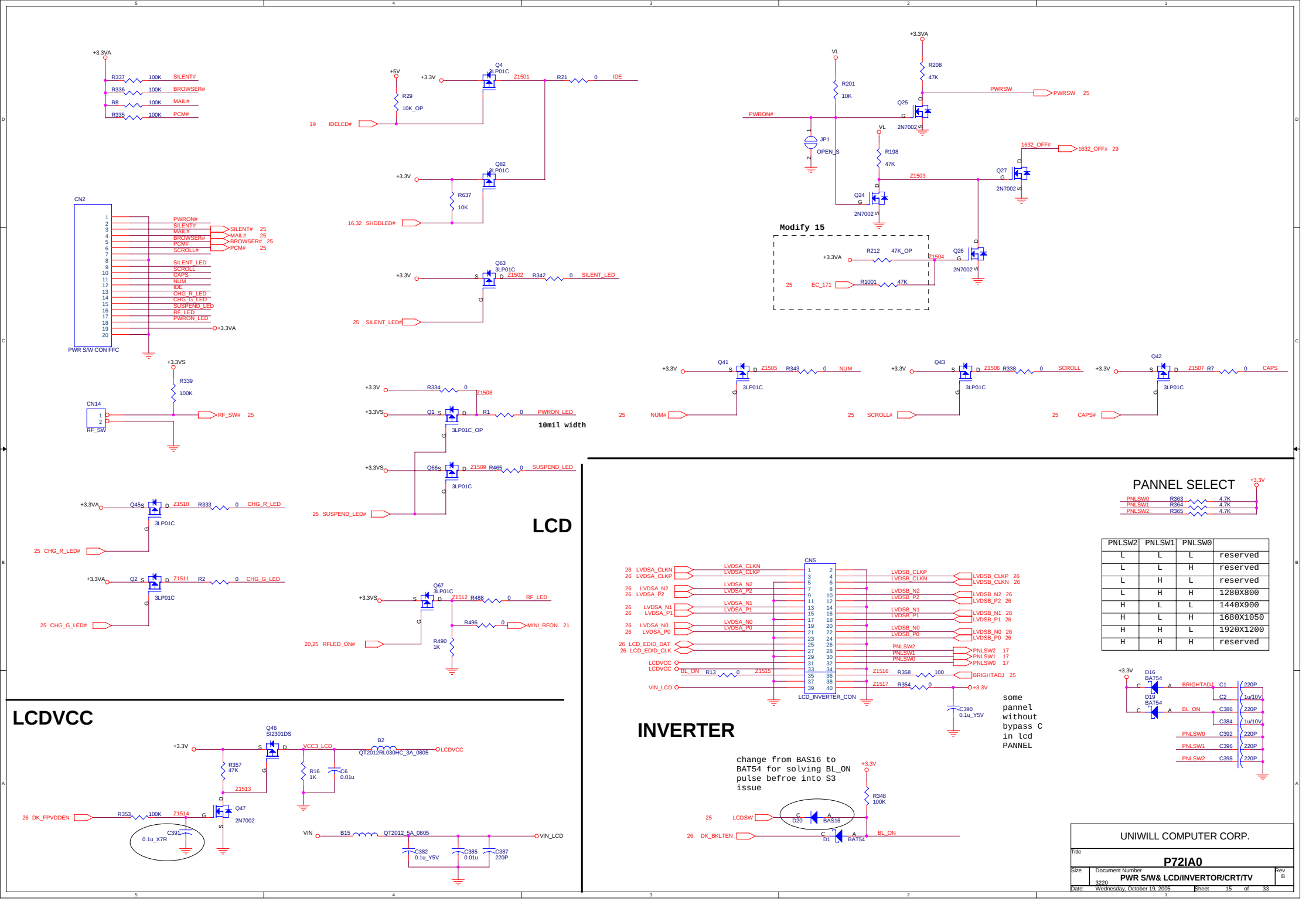


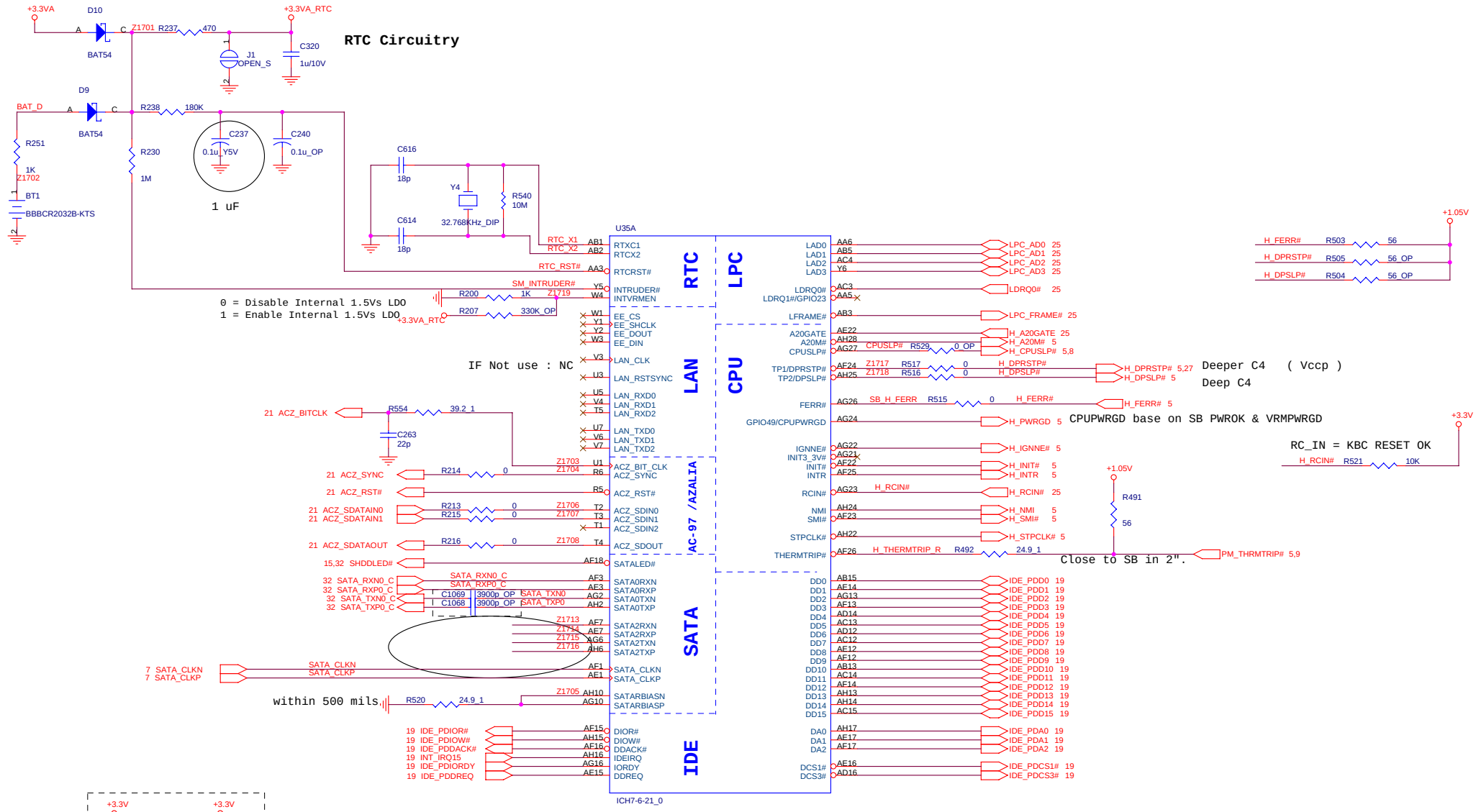
DC IN



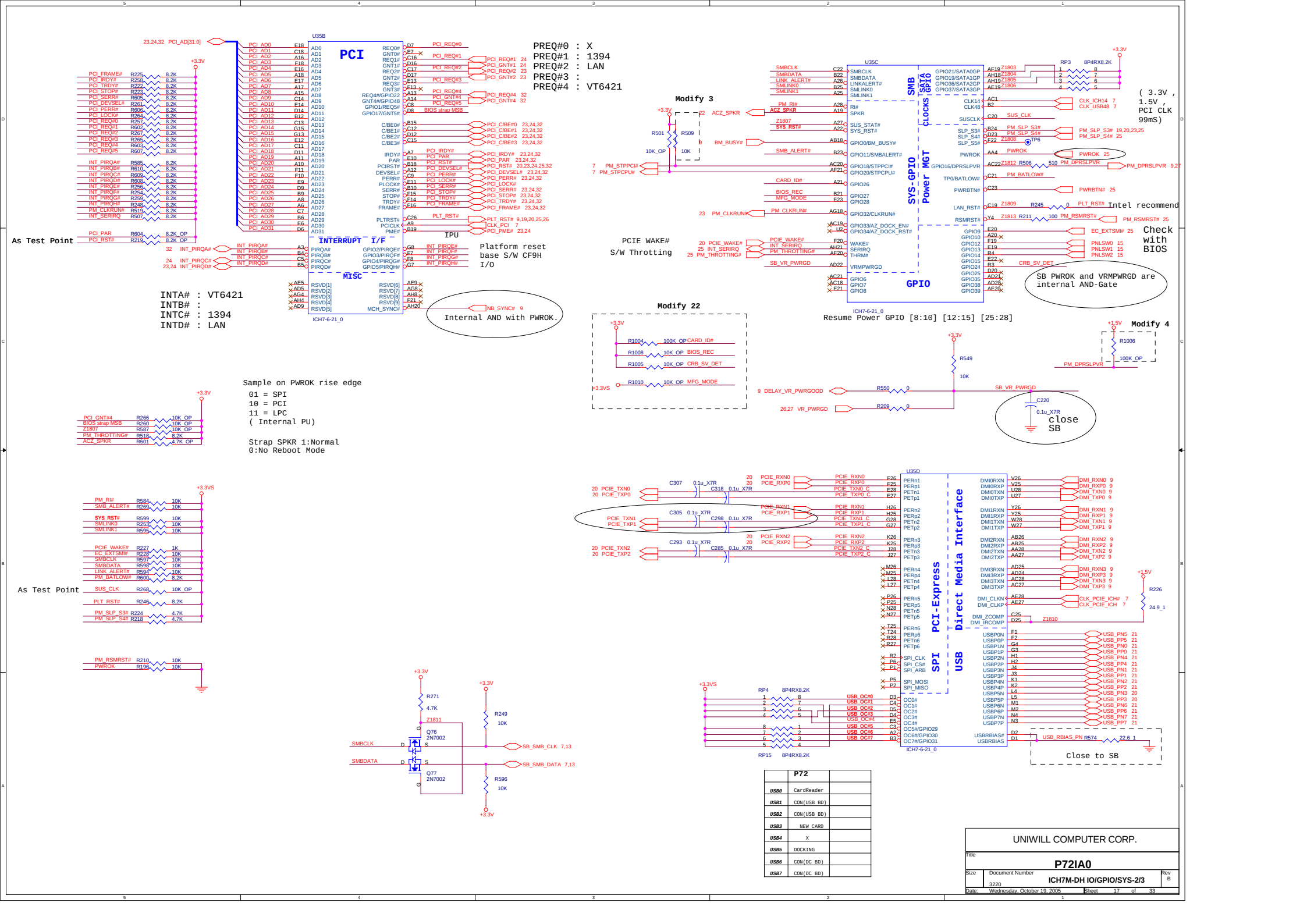


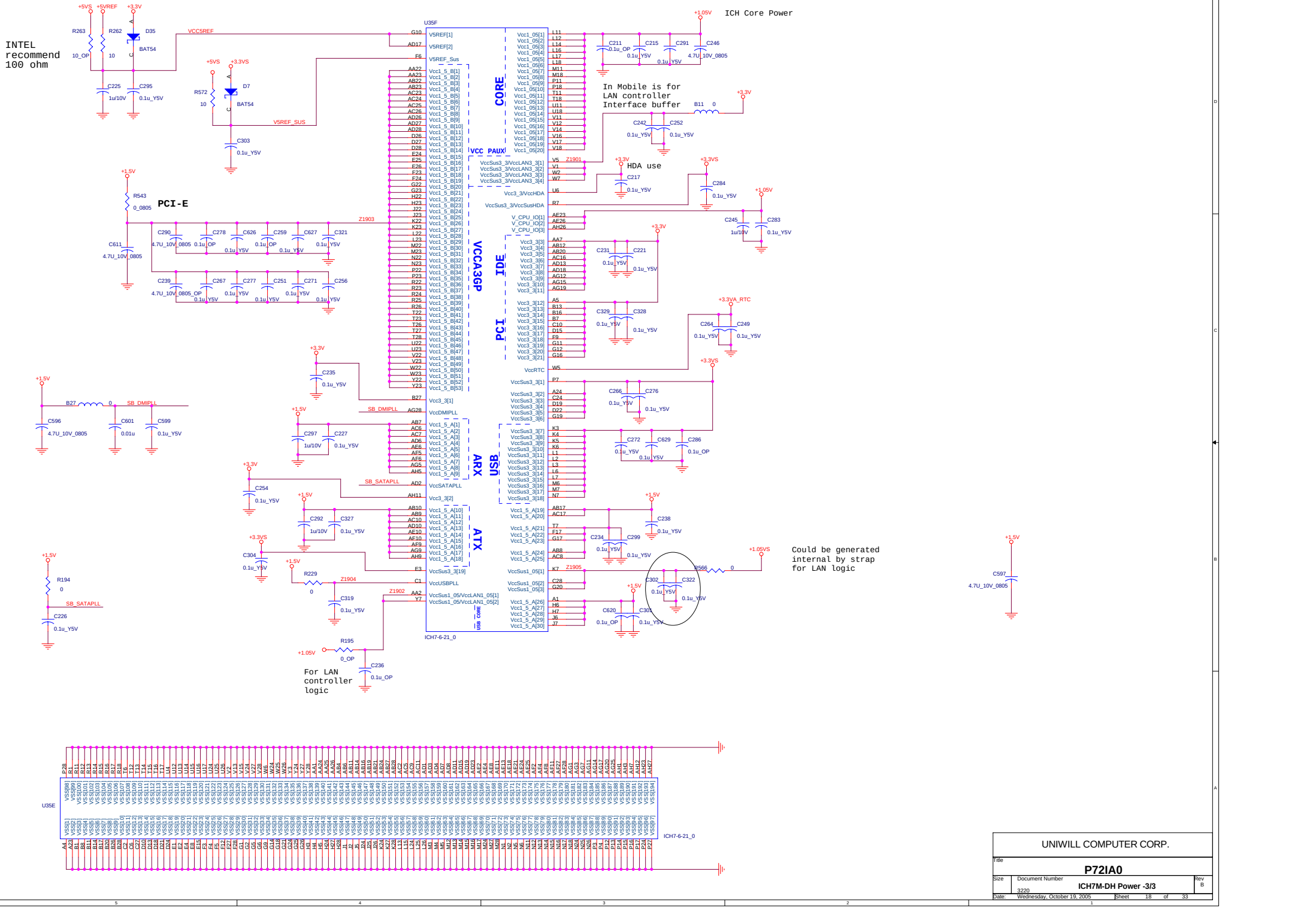
UNIWILL COMPUTER CORP.			
Title: P72IA0			
Size	Document Number: 3220 Termination / Smart Power/DC IN		Rev B
Date: Wednesday, October 19, 2005	Sheet 14 of 33		


+3.3VA
R337 100K SILENT#
R336 100K BROWSER#
R8 100K MAIL#
R335 100K PCM#
CN2
PWRON#
SILENT#
MAIL#
BROWSER#
PCM#
SCROLL#
SILENT_LED
SCROLL
CAPS
NUM
IDE
CHG_R_LED
CHG_G_LED
SUSPEND_LED
RF_LED
PWRON_LED
+3.3VA
PWR S/W CON FFC
+3.3VS
R339 100K
CN14
RF_SW# 25
RF_SW
+5V
+3.3V
Q4 2LP01C Z1501 R21 0 IDE
R29 10K_OP
19 IDELED#
Q82 2LP01C
R637 10K
16,32 SHDDLED#
Q63 3LP01C Z1502 R342 0 SILENT_LED
25 SILENT_LED#
VL
R201 10K
R208 47K
PWRSW PWRSW 25
Q25 2N7002
PWRON#
JP1 OPEN_S
R198 47K
1632_OFF# 1632_OFF# 29
Z1503
Q27 2N7002
Q24 2N7002
Modify 15
R212 47K_OP
Z1504
Q26 2N7002
25 EC_171
R1001 47K
Q41 3LP01C Z1505 R343 0 NUM
25 NUM#
Q43 3LP01C Z1506 R338 0 SCROLL
25 SCROLL#
Q42 3LP01C Z1507 R7 0 CAPS
25 CAPS#
R334 0 Z1508
Q1 3LP01C_OP R1 0 PWRON_LED
10mil width
Q66 3LP01C Z1509 R465 0 SUSPEND_LED
25 SUSPEND_LED#
Q45 3LP01C Z1510 R333 0 CHG_R_LED
25 CHG_R_LED#
Q2 3LP01C Z1511 R2 0 CHG_G_LED
25 CHG_G_LED#
Q67 3LP01C Z1512 R488 0 RF_LED
R496 0 MINI_RFON 21
20,25 RFLED_ON#
R490 1K
LCD
PANNEL SELECT
PNLSW0 R363 4.7K
PNLSW1 R364 4.7K
PNLSW2 R365 4.7K
PNLSW2 PNLSW1 PNLSW0
L L L reserved
L L H reserved
L H L reserved
L H H 1280X800
H L L 1440X900
H L H 1680X1050
H H L 1920X1200
H H H reserved
CN5
LVDSA_CLKN
LVDSA_CLKP
LVDSA_N2
LVDSA_P2
LVDSA_N1
LVDSA_P1
LVDSA_N0
LVDSA_P0
LCD_EDID_DAT
LCD_EDID_CLK
LCDVCC
BL_ON R13 0 Z1515
VIN_LCD
LVDSB_CLKP
LVDSB_CLKN
LVDSB_N2
LVDSB_P2
LVDSB_N1
LVDSB_P1
LVDSB_N0
LVDSB_P0
PNLSW2
PNLSW1
PNLSW0
Z1516 R358 100 BRIGHTADJ 25
Z1517 R354 0 +3.3V
C390 0.1u_Y5V
LCD_INVERTER_CON
INVERTER
some pannel without bypass C in lcd PANNEL
change from BAS16 to BAT54 for solving BL_ON pulse befroe into S3 issue
25 LCDSW
26 DK_BKLTEN
D20 BAS16
D1 BAT54
R348 100K
BL_ON
D16 BAT54
D19 BAT54
BRIGHTADJ C1 220P
C2 1u/10V
BL_ON C386 220P
C384 1u/10V
PNLSW0 C392 220P
PNLSW1 C396 220P
PNLSW2 C398 220P
LCDVCC
Q46 SI2301DS
VCC3_LCD
B2 QT2012RL030HC_3A_0805 LCDVCC
R357 47K
Z1513
R16 1K
C6 0.01u
26 DK_FPVDDEN
R353 100K Z1514
Q47 2N7002
C391 0.1u_X7R
VIN
B15 QT2012_5A_0805 VIN_LCD
C382 0.1u_Y5V
C385 0.01u
C387 220P
UNIWILL COMPUTER CORP.
Title
P72IA0
Size
Document Number
PWR S/W& LCD/INVERTOR/CRT/TV
3220
Rev B
Date: Wednesday, October 19, 2005
Sheet 15 of 33



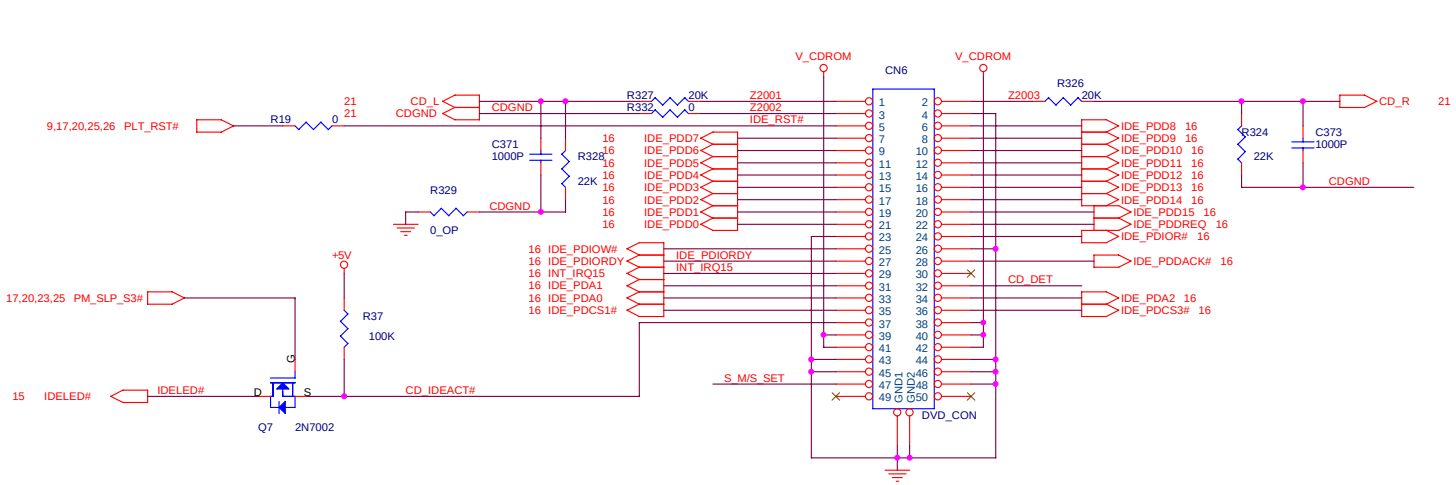
UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size	Document Number: SB ICH7M-DH -1/3	Rev: B
	3220	
Date: Wednesday, October 19, 2005	Sheet 16 of 33	

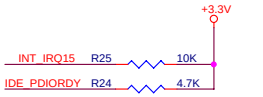

PREQ#0 : X
PREQ#1 : 1394
PREQ#2 : LAN
PREQ#3 :
PREQ#4 : VT6421
Modify 3
PCIE WAKE#
S/W Throtting
Modify 22
Resume Power GPIO [8:10] [12:15] [25:28]
Modify 4
(3.3V , 1.5V , PCI CLK 99mS)
Intel recommend
Check with BIOS
SB PWROK and VRMPWRGD are internal AND-Gate
INTA# : VT6421
INTB# :
INTC# : 1394
INTD# : LAN
Internal AND with PWROK.
Platform reset base S/W CF9H I/O
Sample on PWROK rise edge
01 = SPI
10 = PCI
11 = LPC
(Internal PU)
Strap SPKR 1:Normal
0:No Reboot Mode
As Test Point
As Test Point
close SB
Close to SB
UNIWILL COMPUTER CORP.
P72IA0
ICH7M-DH IO/GPIO/SYS-2/3
Wednesday, October 19, 2005



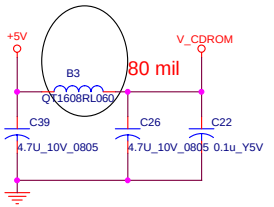
UNIWILL COMPUTER CORP.			
Title	P72IA0		
Size	Document Number 3220	ICH7M-DH Power -3/3	Rev B
Date: Wednesday, October 19, 2005	Sheet 18 of 33		

CR-ROM



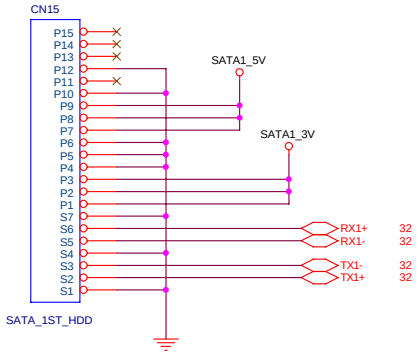


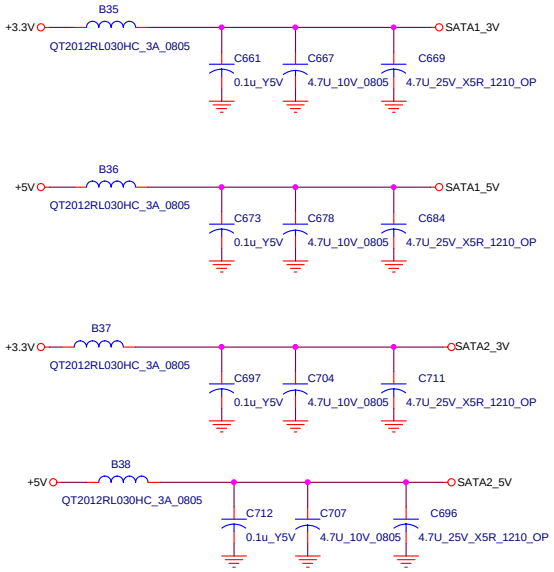
500mA Bead => 80 mils trace ?

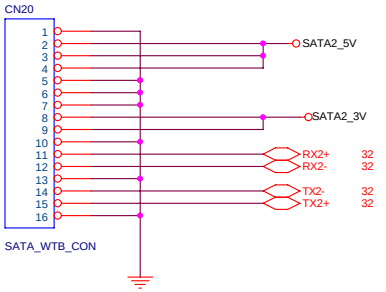


CSEL : Master = 0 / Slave = 1

HDD





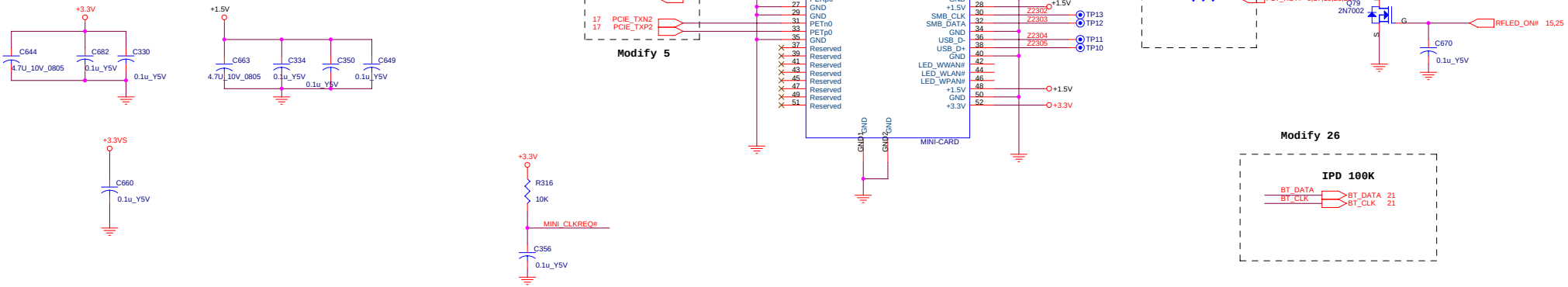


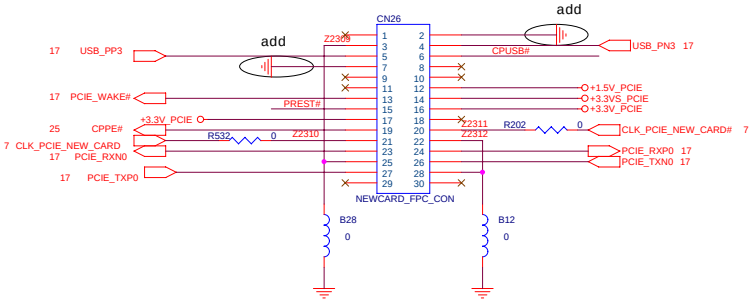
UNIWILL COMPUTER CORP.		
Title: **P72IA0**		
Size	Document Number: **HDD / CD-ROM CONN** 3220	Rev B
Date: Wednesday, October 19, 2005	Sheet 19 of 33	

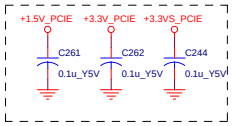
MINI CARD CONN

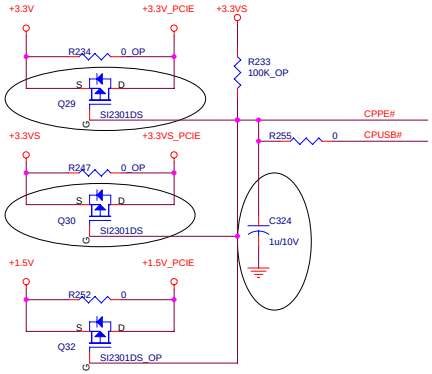
Intel PRO/Wireless 2100 LAN

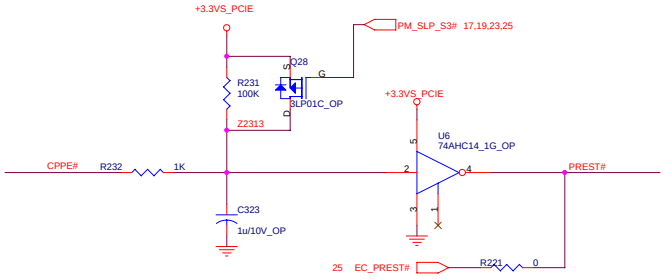
PIN11	LED_WLAN_LINK	Hi(3.3V) Low(0V)	Solid ON 1 flash/3 sec LED OFF	Associated AP Not Associated with an AP Power OFF or RF_Kill active
PIN12	LED_WLAN_ACT	Hi(3.3V) Low(0V)	Rapid Blinking Slow Blinking LED OFF	Passing data traffic to AP Beacon traffic to Ap Power OFF or not activity or RF_Kill active
PIN13	HW_RadioXMIT_OFF#	Hi(3.3V) Low(0V)	Enable Disable	Radio transmitter is ON Radio transmitter turn off



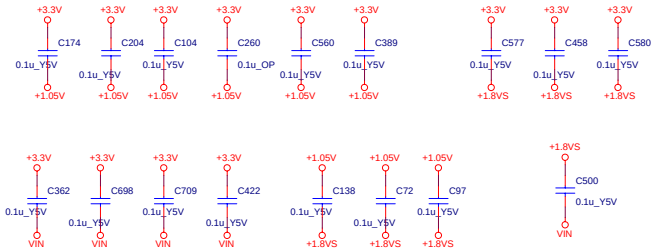






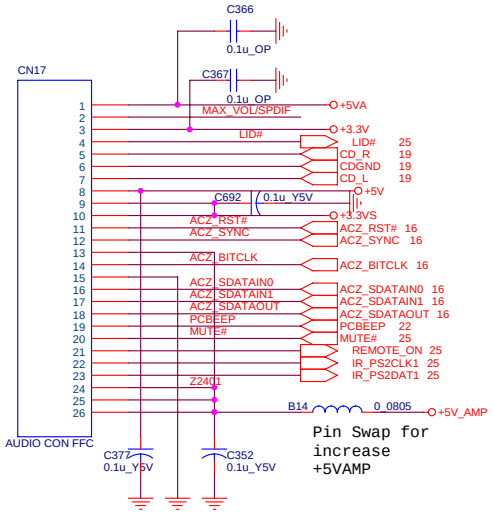


FOR EMI

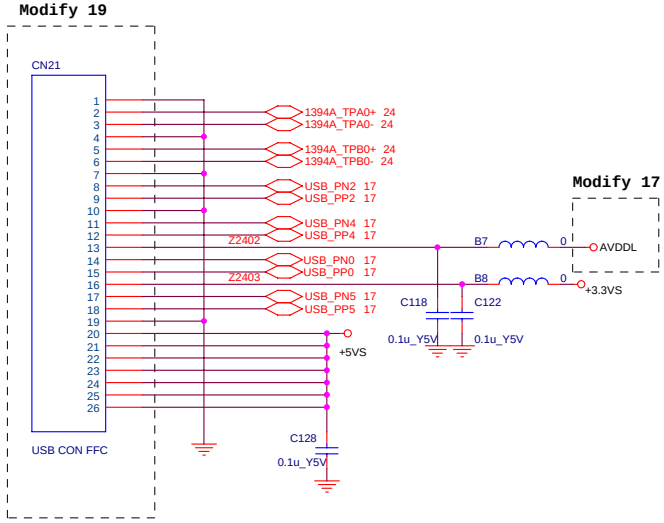


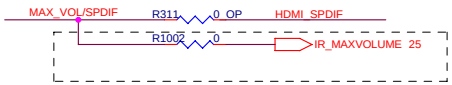
COULD DEL

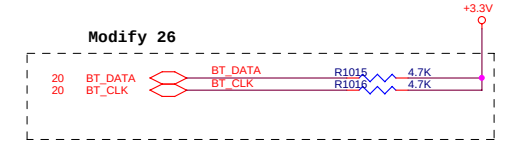
UNIWILL COMPUTER CORP.			
Title: P72IA0			
Size	Document Number: 3220	Wireless / New Card / EMI	Rev: B
Date: Wednesday, October 19, 2005	Sheet 20 of 33		

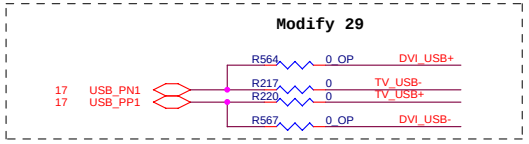


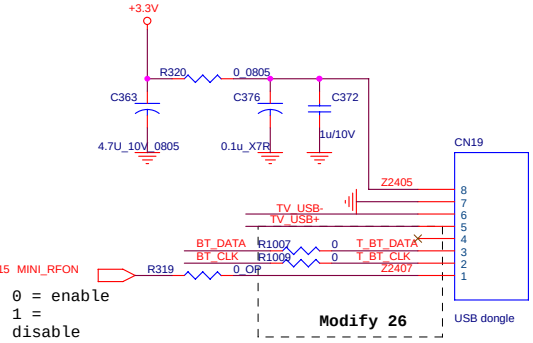
Pin Swap for increase +5VAMP



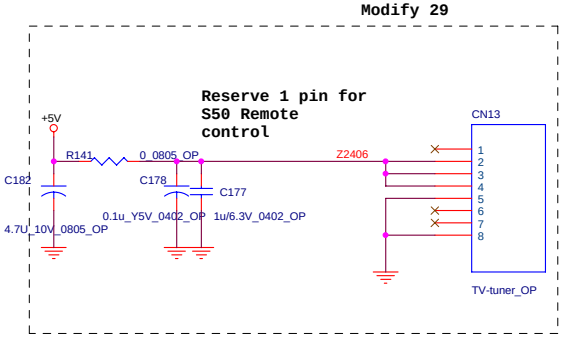


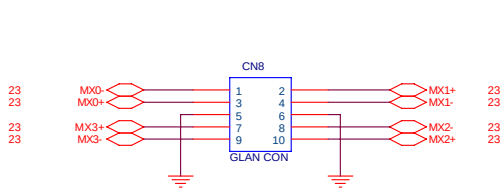


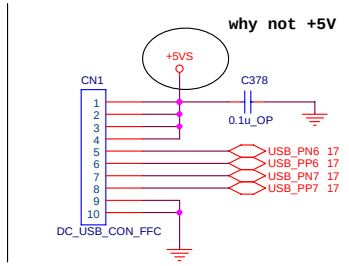


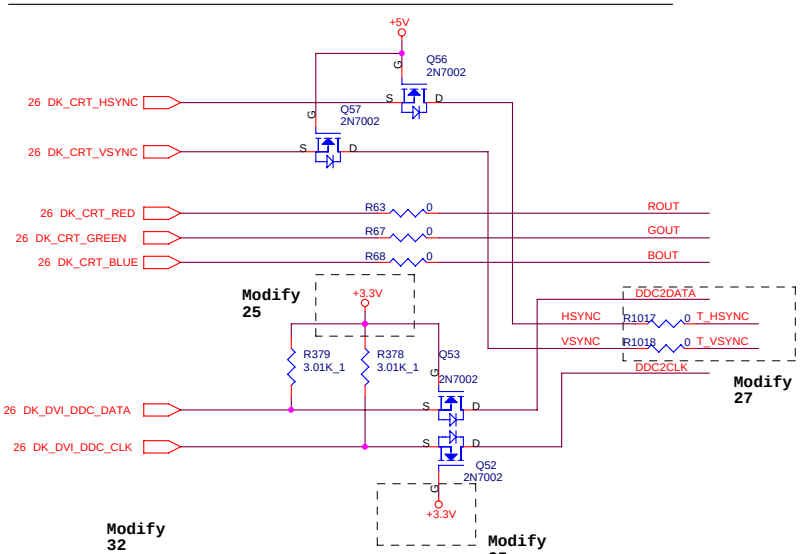


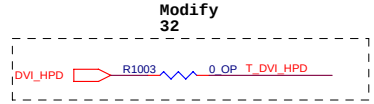
0 = enable
1 = disable

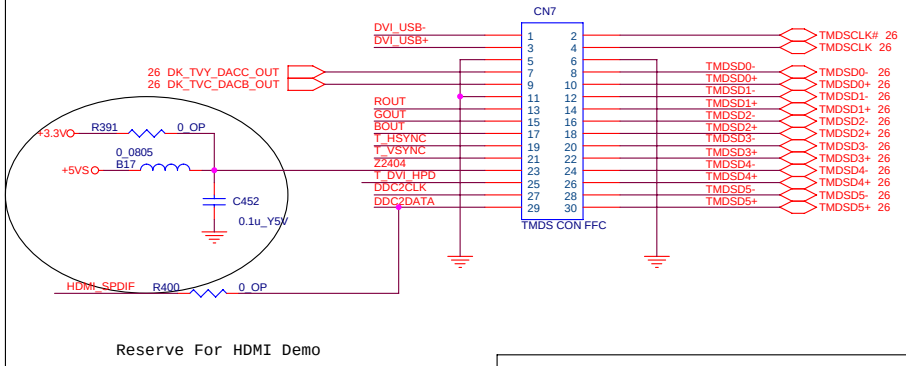












Reserve For HDMI Demo

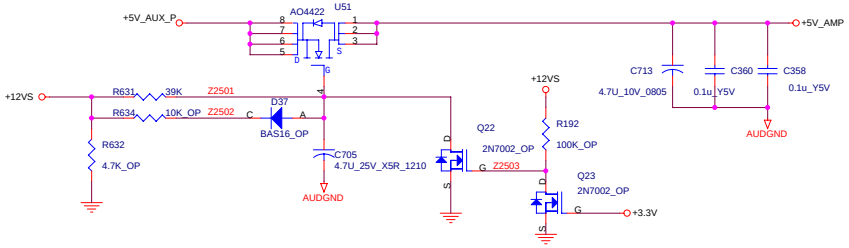
UNIWILL COMPUTER CORP.

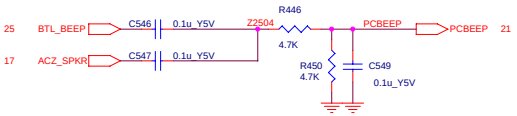
Title: P72IA0

Size | Document Number: 3220 I/O PORT CON | Rev: B

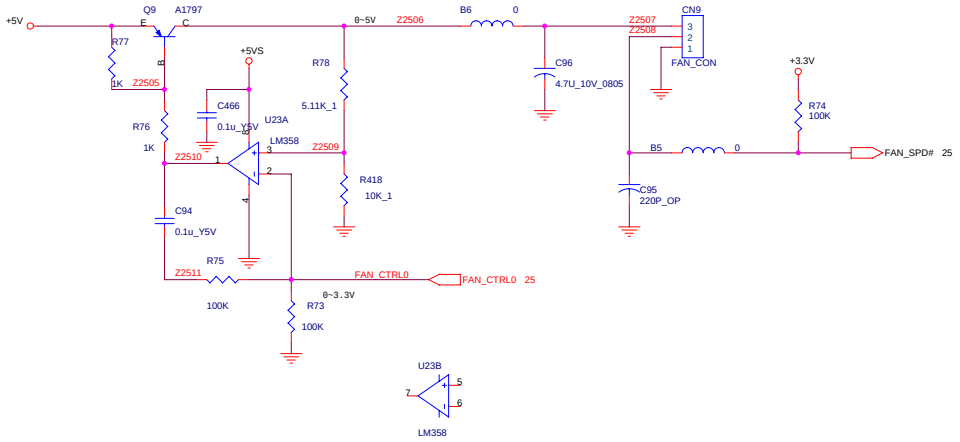
Date: Wednesday, October 19, 2005 | Sheet 21 of 33

AMP VDD

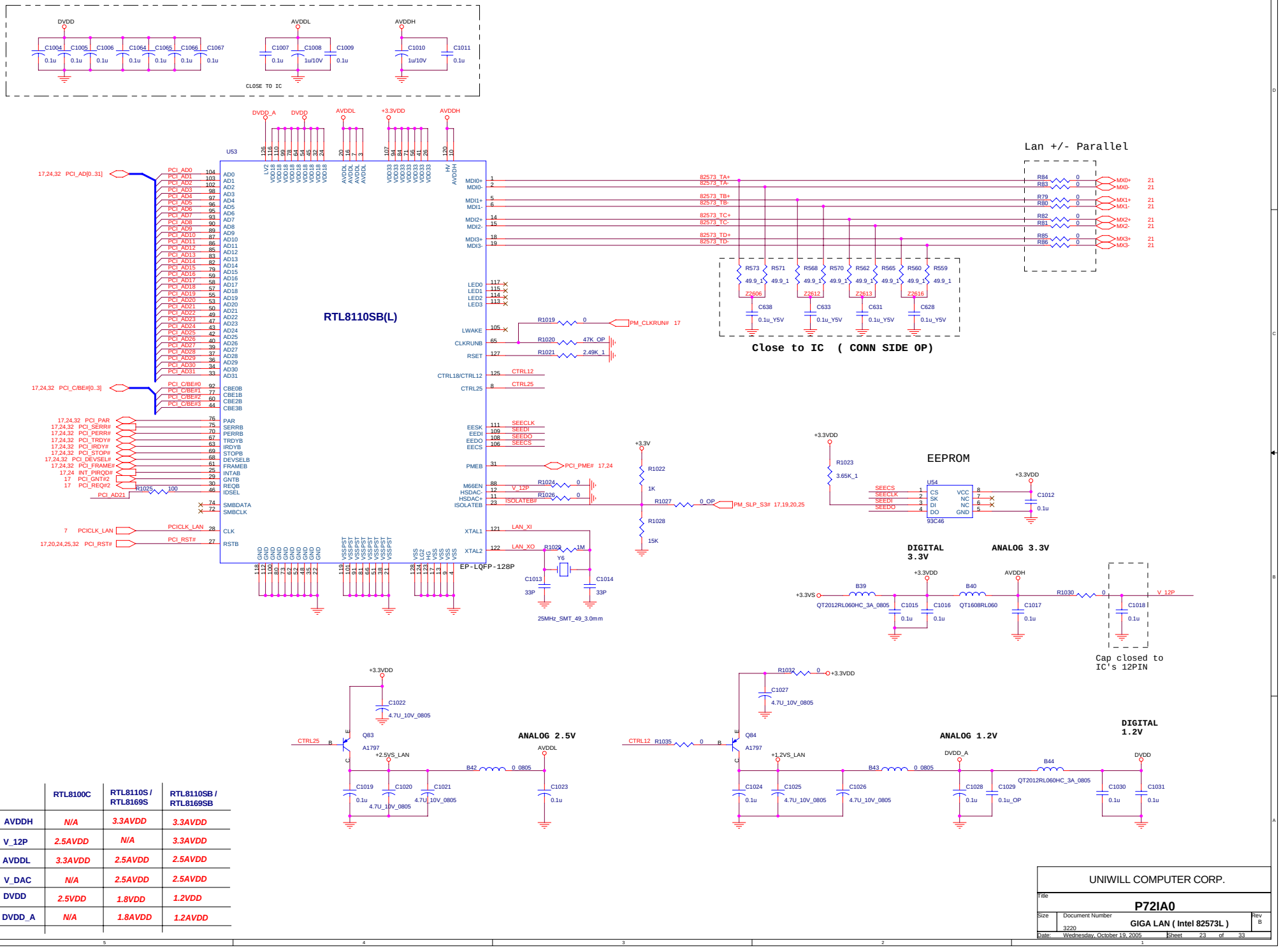




CPU FAN CONTROL



UNIWILL COMPUTER CORP.		
Title	P72IA0	
Size	Document Number: AUD PWR / FAN CTL (3220)	Rev: B
Date: Wednesday, October 19, 2005	Sheet 22 of 33	



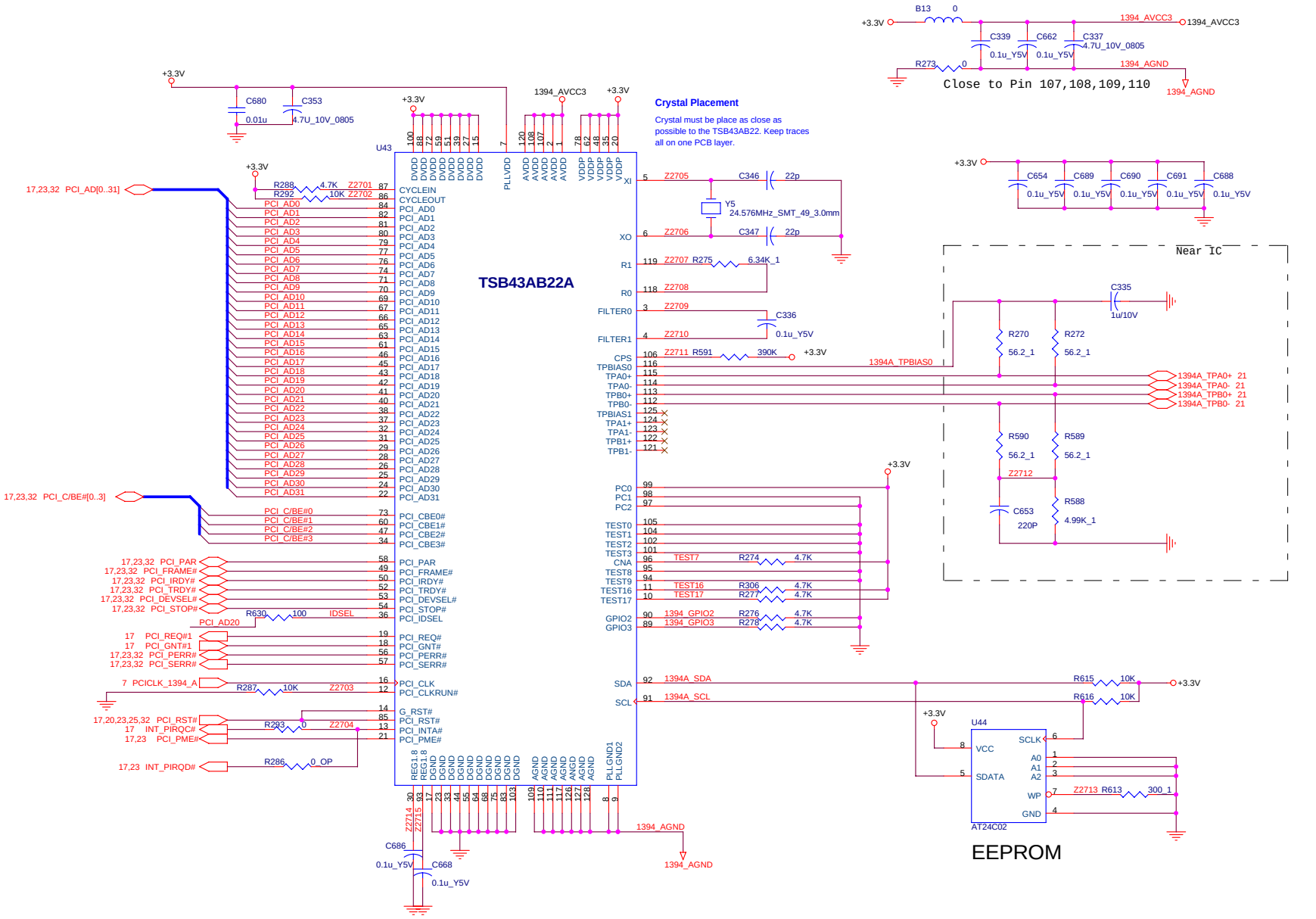
	RTL8100C	RTL8110S / RTL8169S	RTL8110SB / RTL8169SB
AVDDH	N/A	3.3AVDD	3.3AVDD
V_12P	2.5AVDD	N/A	3.3AVDD
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD
V_DAC	N/A	2.5AVDD	2.5AVDD
DVDD	2.5VDD	1.8VDD	1.2VDD
DVDD_A	N/A	1.8AVDD	1.2AVDD

UNIWILL COMPUTER CORP.

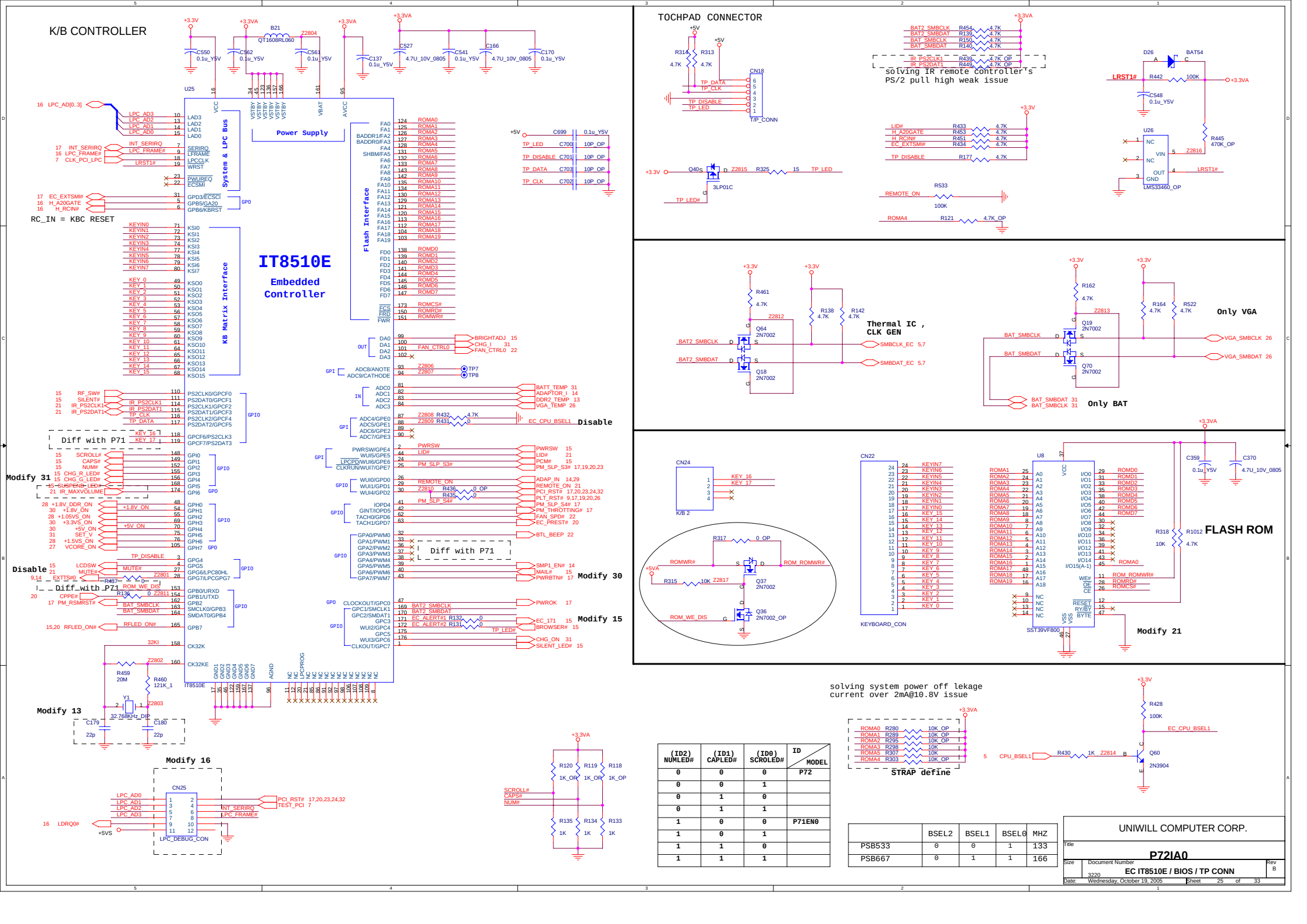
Title: P72IA0

Size: 3220 | Document Number: GIGA LAN (Intel 82573L) | Rev: B

Date: Wednesday, October 19, 2005 | Sheet 23 of 33

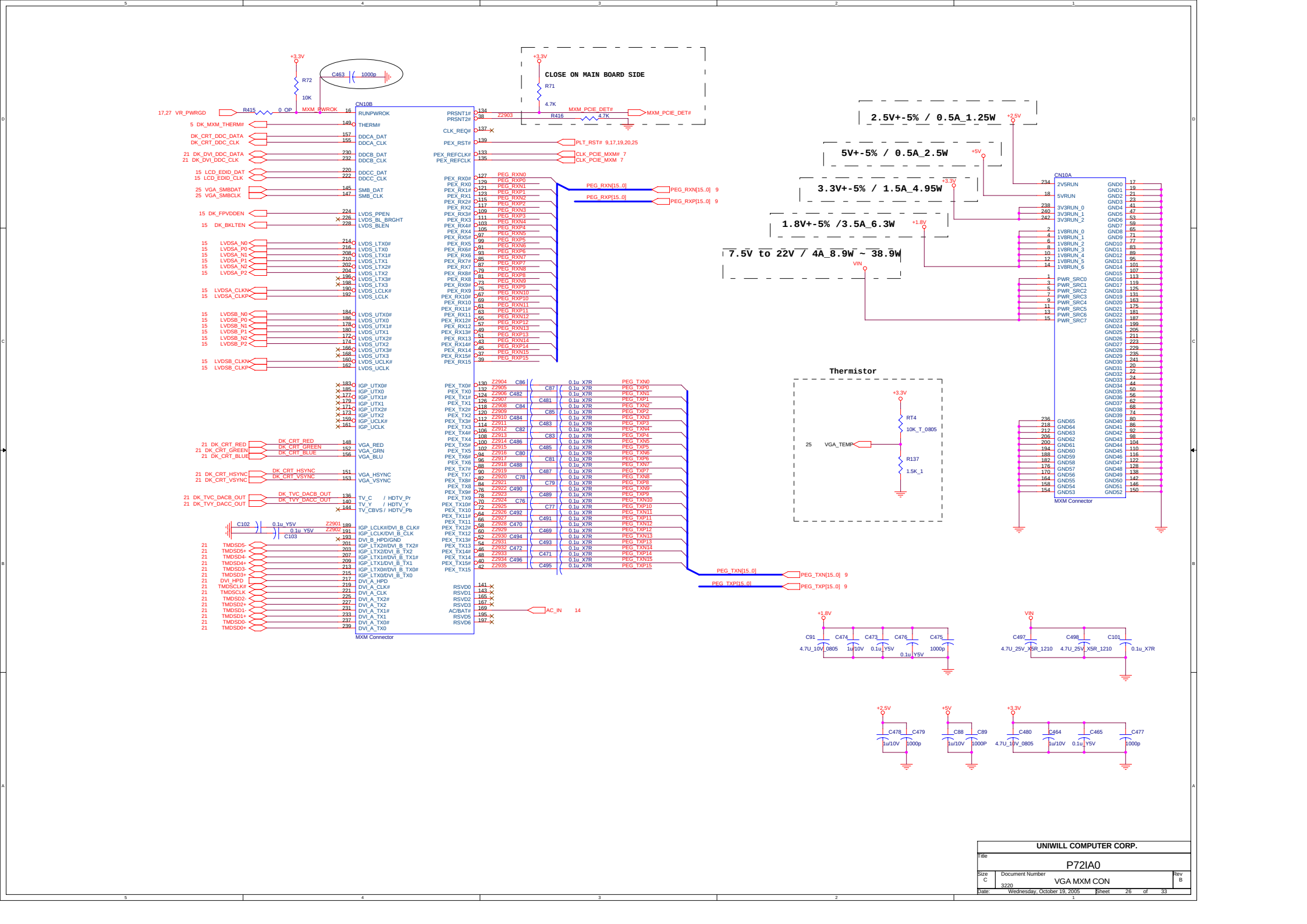


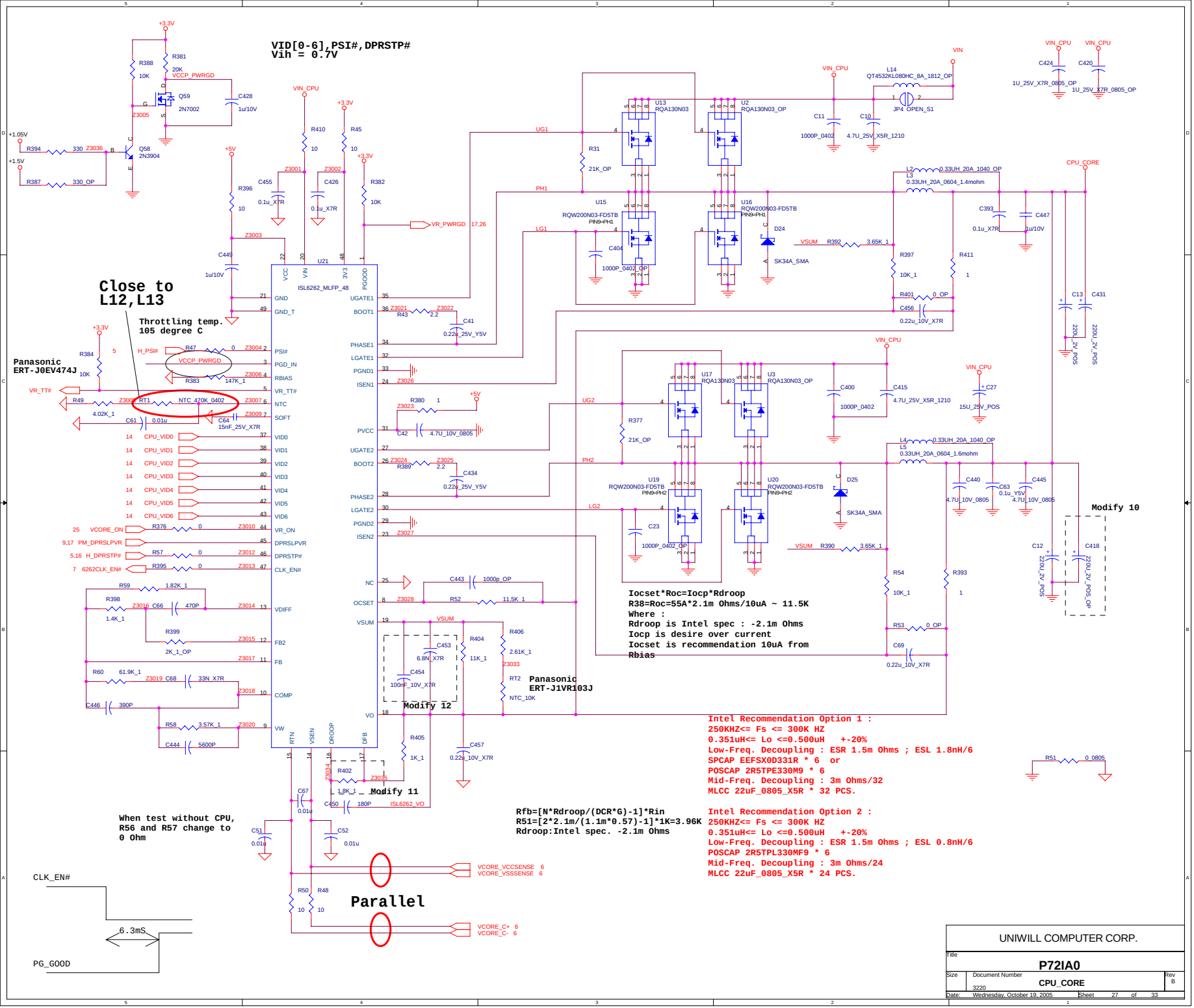
Unwill International Corp.		
Title: IEEE1394A TSB43AB22		
Size	Document Number: P72IA0	Rev: B
	3220	
Date: Wednesday, October 19, 2005	Sheet 24 of 33	

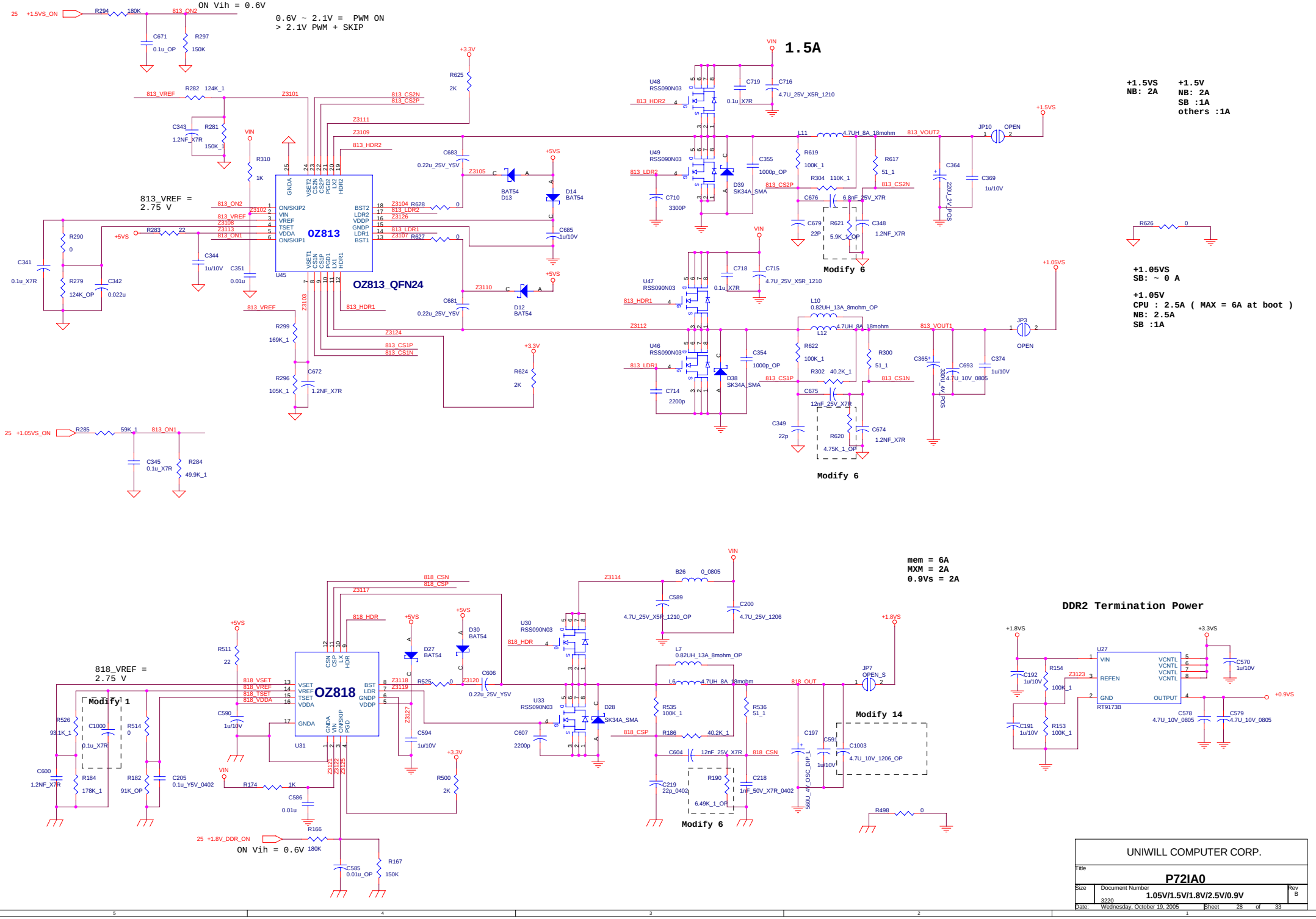


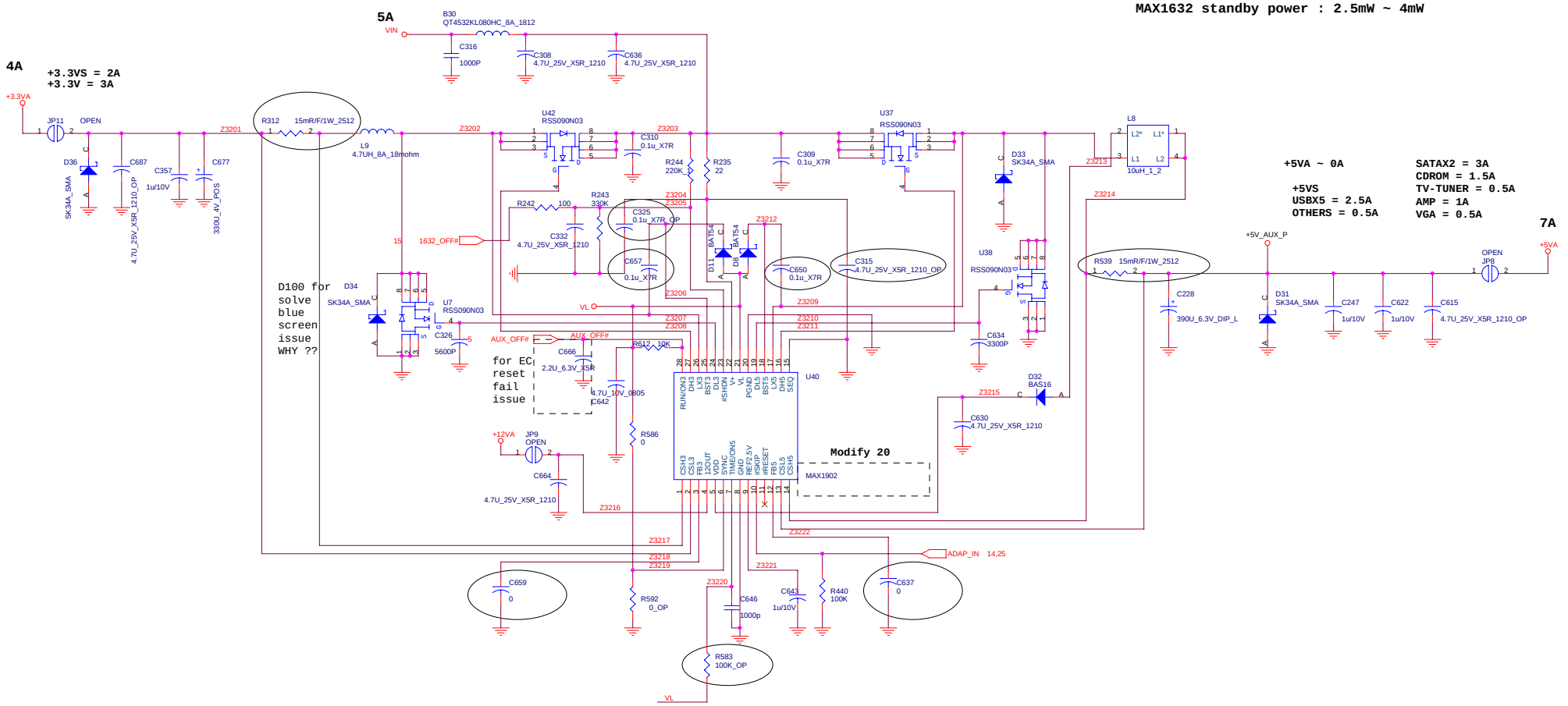
(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID / MODEL
0	0	0	P72
0	0	1	
0	1	0	
0	1	1	
1	0	0	P71EN0
1	0	1	
1	1	0	
1	1	1	

	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166


CLOSE ON MAIN BOARD SIDE
2.5V+-5% / 0.5A_1.25W
5V+-5% / 0.5A_2.5W
3.3V+-5% / 1.5A_4.95W
1.8V+-5% /3.5A_6.3W
7.5V to 22V / 4A_8.9W ~ 38.9W
Thermistor
CN10B
MXM Connector
CN10A
MXM Connector
UNIWILL COMPUTER CORP.
P72IA0
VGA MXM CON
Wednesday, October 19, 2005


VID[0-6],PSI#,DPRSTP#
Vih = 0.7V
Close to
L12,L13
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
ISL6262_MLFP_48
Iocset*Roc=Iocp*Rdroop
R38=Roc=55A*2.1m Ohms/10uA ~ 11.5K
Where :
Rdroop is Intel spec : -2.1m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from
Rbias
Panasonic
ERT-J1VR103J
Modify 10
Modify 12
Modify 11
When test without CPU,
R56 and R57 change to
0 Ohm
Rfb=[N*Rdroop/(DCR*G)-1]*Rin
R51=[2*2.1m/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms
Intel Recommendation Option 1 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
SPCAP EEFSX0D331R * 6 or
POSCAP 2R5TPE330M9 * 6
Mid-Freq. Decoupling : 3m Ohms/32
MLCC 22uF_0805_X5R * 32 PCS.
Intel Recommendation Option 2 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
POSCAP 2R5TPL330MF9 * 6
Mid-Freq. Decoupling : 3m Ohms/24
MLCC 22uF_0805_X5R * 24 PCS.
Parallel
CLK_EN#
6.3mS
PG_GOOD
UNIWILL COMPUTER CORP.
P72IA0
CPU_CORE
Wednesday, October 19, 2005


ON Vih = 0.6V
0.6V ~ 2.1V = PWM ON
> 2.1V PWM + SKIP
1.5A
OZ813
OZ813_QFN24
813_VREF = 2.75 V
Modify 6
+1.5VS NB: 2A
+1.5V NB: 2A SB :1A others :1A
+1.05VS SB: ~ 0 A
+1.05V CPU : 2.5A (MAX = 6A at boot) NB: 2.5A SB :1A
OZ818
818_VREF = 2.75 V
Modify 1
Modify 14
mem = 6A MXM = 2A 0.9Vs = 2A
DDR2 Termination Power
ON Vih = 0.6V
UNIWILL COMPUTER CORP.
P72IA0
1.05V/1.5V/1.8V/2.5V/0.9V
Wednesday, October 19, 2005



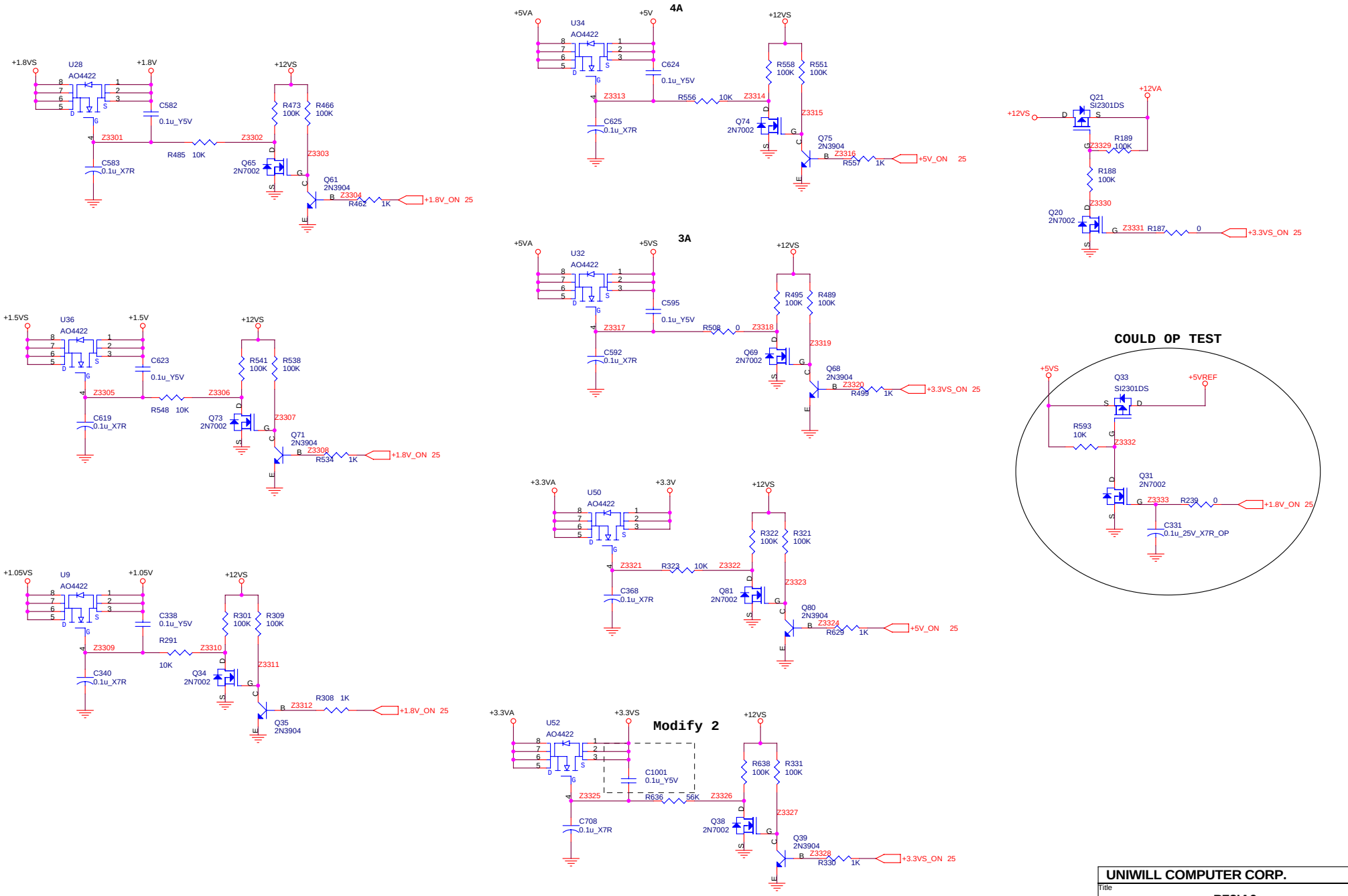
	MAX1632 MAX1902	SC1404
C637	0	100pF
C659	0	100pF
R583	100K_OP	100K
R312,R539	15mR,15mR	8mR,8mR
C315	OP	4.7U_25V
C325	OP	0.1U_25V
C650,C657	0.1U_X7R	0.22U_25V

UNIWILL COMPUTER CORP.

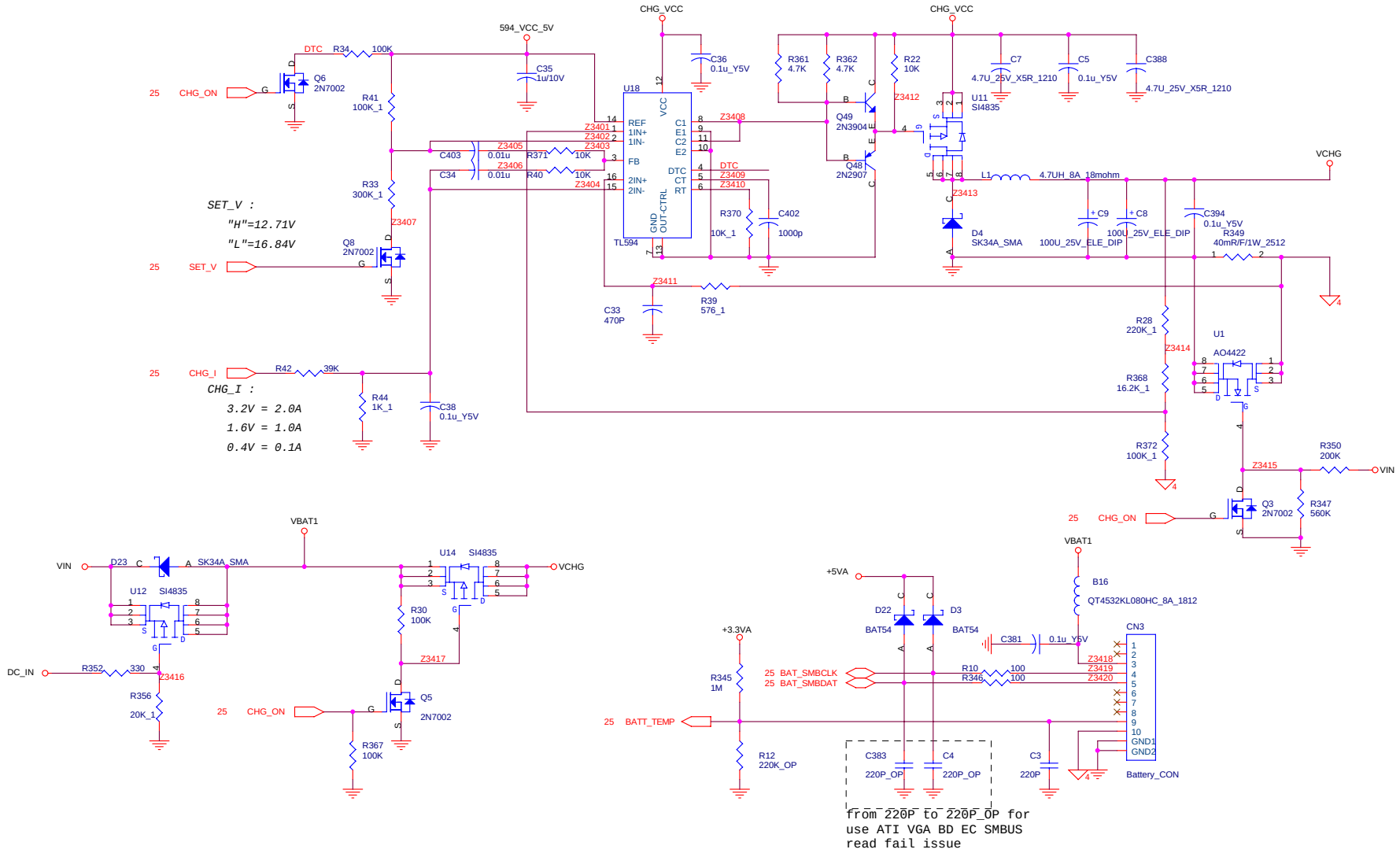
Title: **P72IA0**

Size: | Document Number: 3220 | **+3.3VA/+5VA/+12VA** | Rev: B

Date: Wednesday, October 19, 2005 | Sheet 29 of 33



UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size: Custom	Document Number: P72IA0 3220	Rev: B
	VCC SW/+1.05VS/+1.5VS	
Date: Wednesday, October 19, 2005	Sheet 30 of 33	



H8 C264D107 H5 C315D154 H10 C315D154 H6 C315D154 H4 C264D107 H9 C264D107 H14 C264D107 H20 C264D107 H19 C264D107 H13 C264D107 H12 C264D107 H3 C264D107

H11 C237D111 H22 C158D158 H2 C158D158 H21 C158D158 H1 C158D158 H7 C315B178D178 H23 C256B126D126 H18 C263D103 H17 C237D111

H1000 C197D91 H1001 C197D91

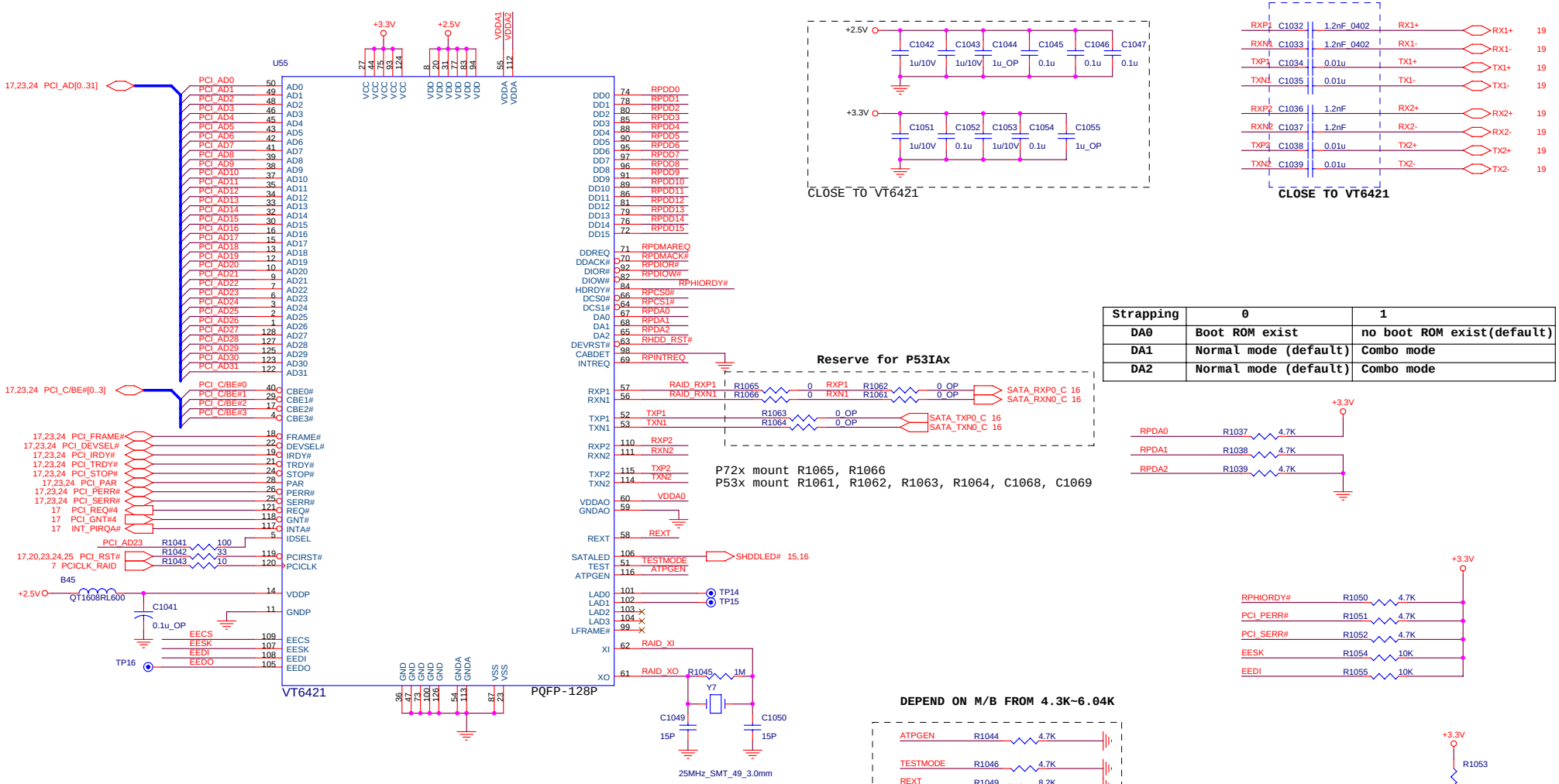
M12 M-MARK1 M15 M-MARK1 M14 M-MARK1 M16 M-MARK1 M13 M-MARK1 M19 M-MARK1 M17 M-MARK1 M20 M-MARK1 M21 M-MARK1 M18 M-MARK1 M5 M-MARK1 M4 M-MARK1 M23 M-MARK1 M6 M-MARK1 M22 M-MARK1 M7 M-MARK1 M3 M-MARK1 M24 M-MARK1 M9 M-MARK1 M25 M-MARK1 M2 M-MARK1 M10 M-MARK1 M8 M-MARK1 M11 M-MARK1 M1 M-MARK1

UNIWILL COMPUTER CORP.

Title: **P72IA0**

Size: | Document Number: 3220 **BATT IN / Charger** | Rev: B

Date: Wednesday, October 19, 2005 | Sheet 31 of 33



Strapping	0	1
DA0	Boot ROM exist	no boot ROM exist(default)
DA1	Normal mode (default)	Combo mode
DA2	Normal mode (default)	Combo mode

UNIWILL COMPUTER CORP.

Title: P71EN0

Size: Document Number: RAID IC VT6421 3220 | Rev: 01

Date: Wednesday, October 19, 2005 | Sheet 32 of 33

RA to RB change list -1011

Modify 1 : Add one 0.1u_X7R C1000 to OZ818 Vref .
Modify 2 : Add one 0.1u_Y5V C1001 to U52 gate and source .
Modify 3 : Add R530 => 0 hom , R509 => 10K make sure PCI CLK will work fine.
Modify 4 : Reserve R1006 (10k_OP) for SB PM_DPRSLPVR sometimes will floating bug.
Modify 5 : Swap the mini-card TX , RX pairs .
Modify 6 : Change R190 , R620 , R621 OP .
Modify 7 : Change R611 OP , add R1000 , to make Mini-card RST from PCI_RST# to PLT_RST# .
Modify 8 : Change R171 to 100 Ohm , make sure USB 48M work fine with CLKGEN Ver.A .
Modify 9 : Swap HDD RXP and RXN signals.
Modify 10 : C417 and C418 OP .
Modify 11 : R402 change to 1.8K_1 for fine tune Vcore load-line.
Modify 12 : C454 change to 100NF , C453 change to 6.8N for improve Vcore dynamic ripple.
Modify 12 : C454 change to 100NF , C453 change to 6.8N for improve Vcore dynamic ripple.