

EF5 BLOCK DIAGRAM

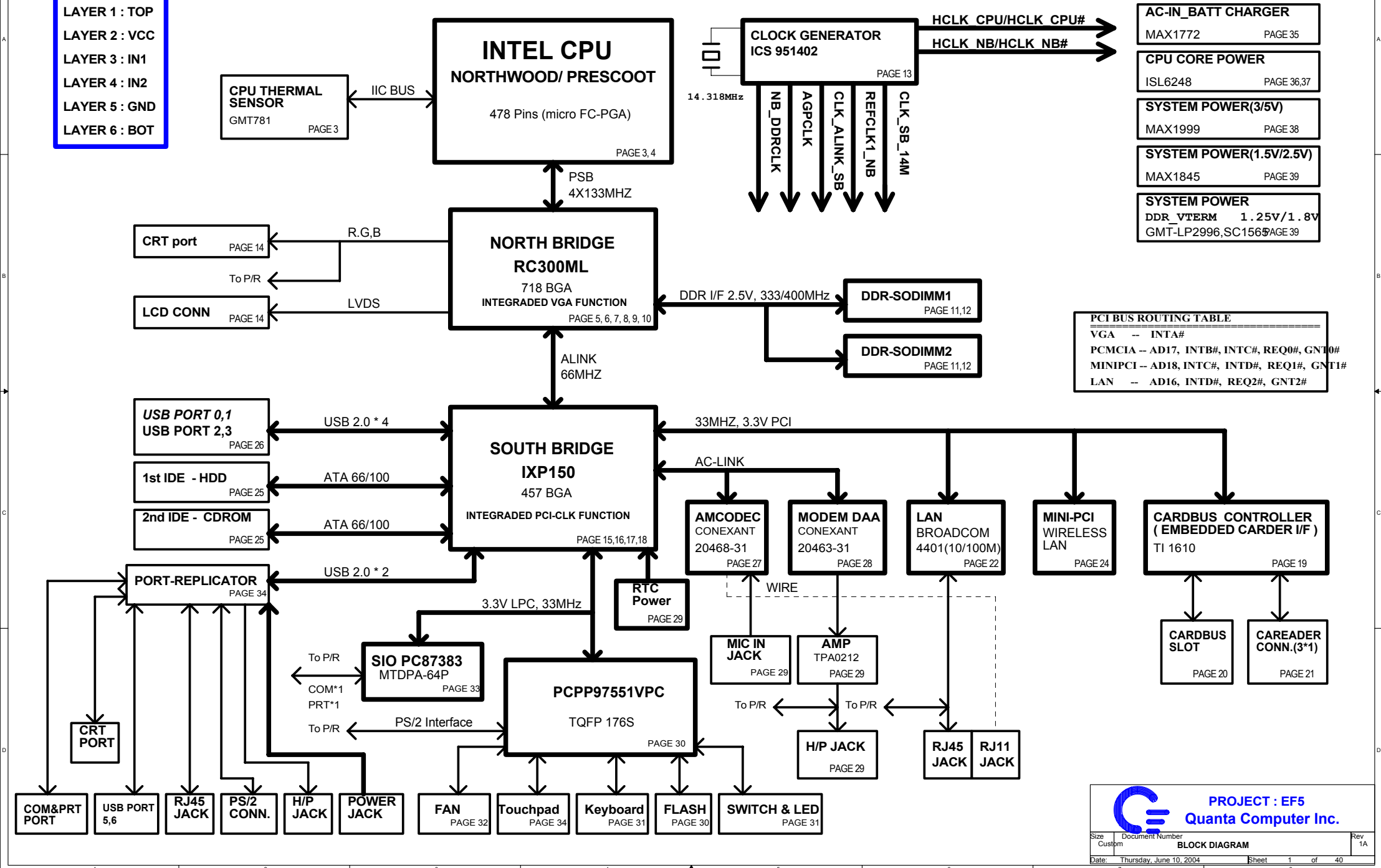
01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

NORTHWOOD-PRESCOOT/RC300ML/IXP150

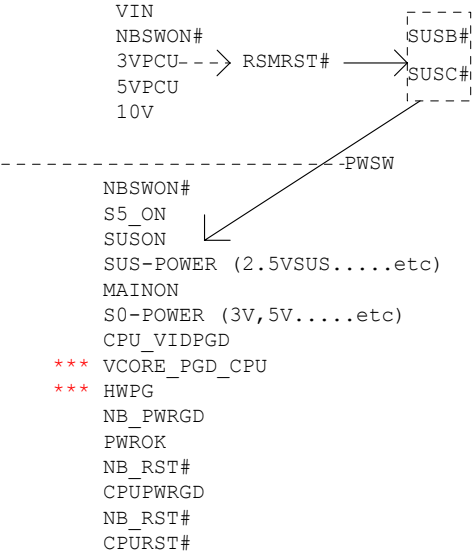
POWER-SOURCE CONTROL



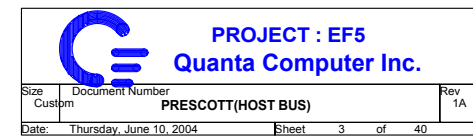
Voltage Rails	Core voltage for Processor	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON
SMDDR_VREF	1.25V for DDR Reference voltage	X	X			SUSON
SMDDR_VTERM	1.25V for DDR Termination voltage	X				MAINON
1.5V		X				MAINON
1.8V		X				MAINON
2.5VSUS		X	X			SUSON
2.5V		X				MAINON
2.5VPCU		X	X	X	X	VL
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
5V		X				MAINON

PCI DEVICE	IDSEL#	REQ/GNT#	Interrupts
LAN(10/100)	AD16	2/2	INTD#
CARDBUS	AD17	0/0	INTB#, INTC#
MINI-PCI	AD18	1/1	INTC#, INTD#

POWER SEQUENCE

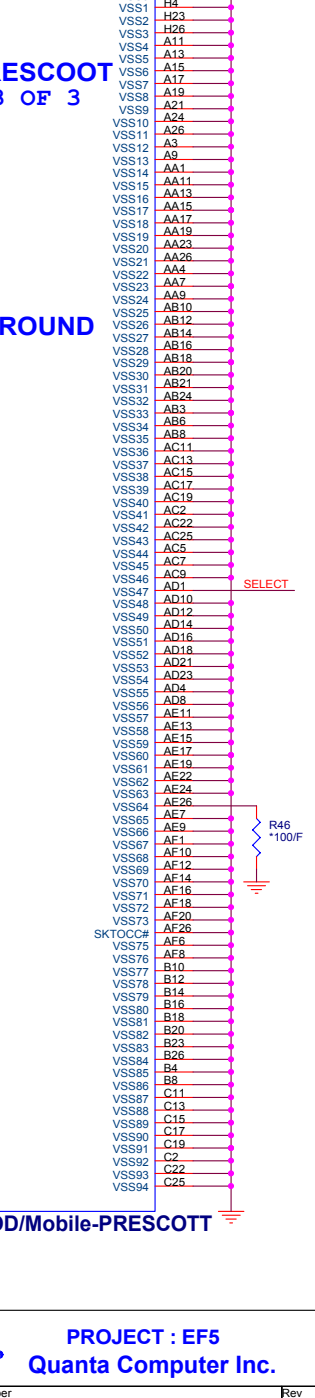
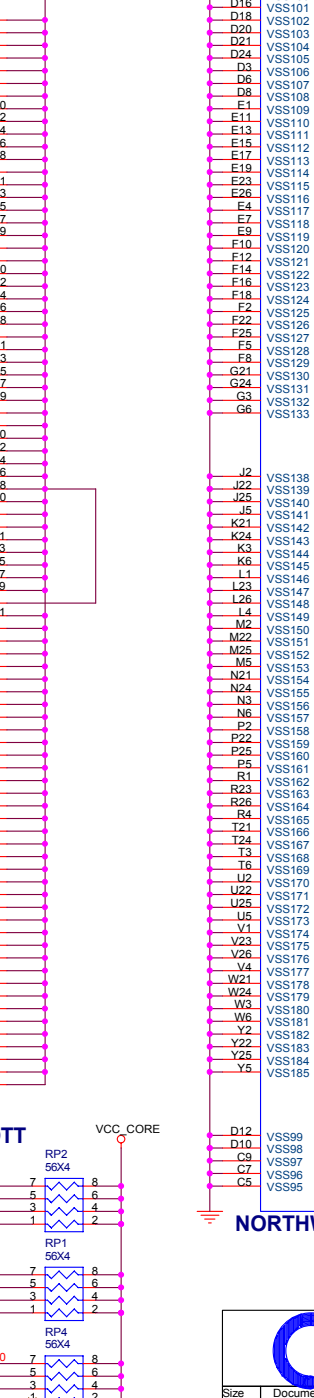
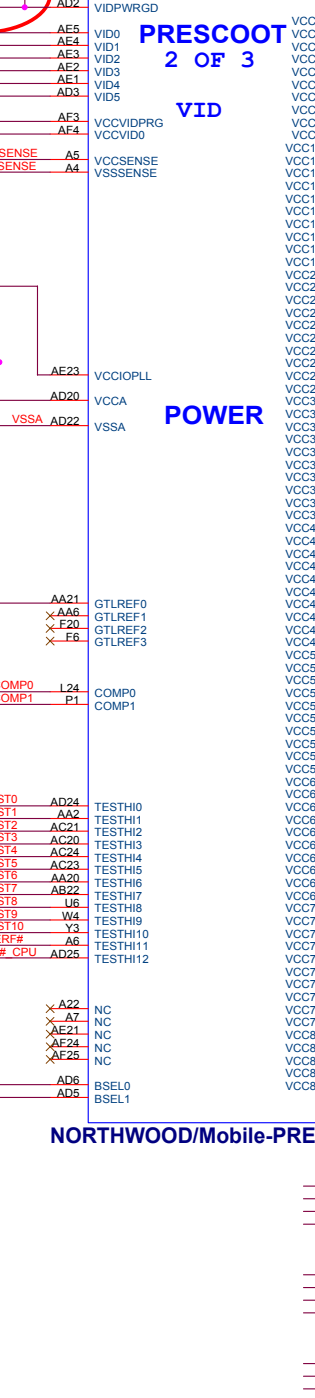
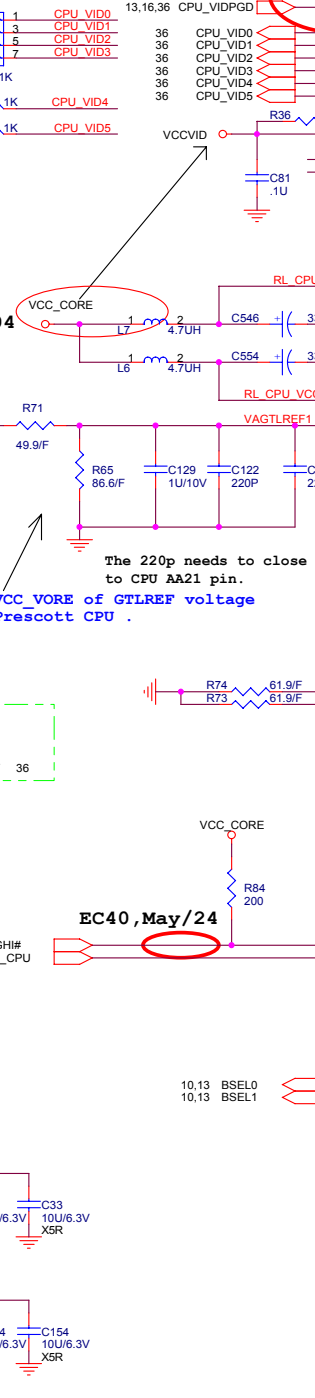
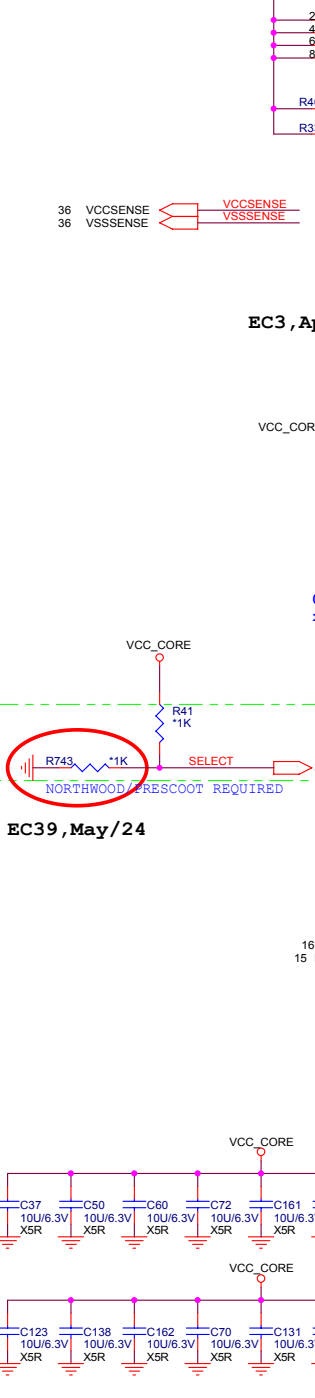
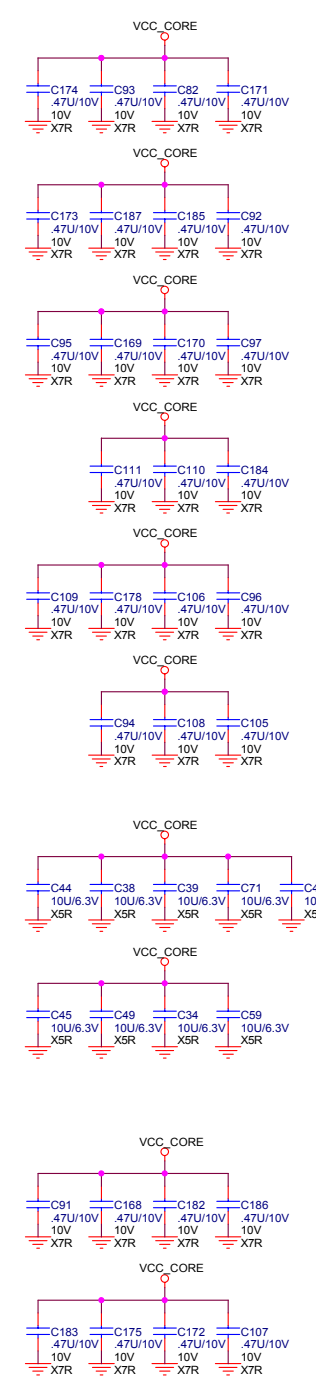


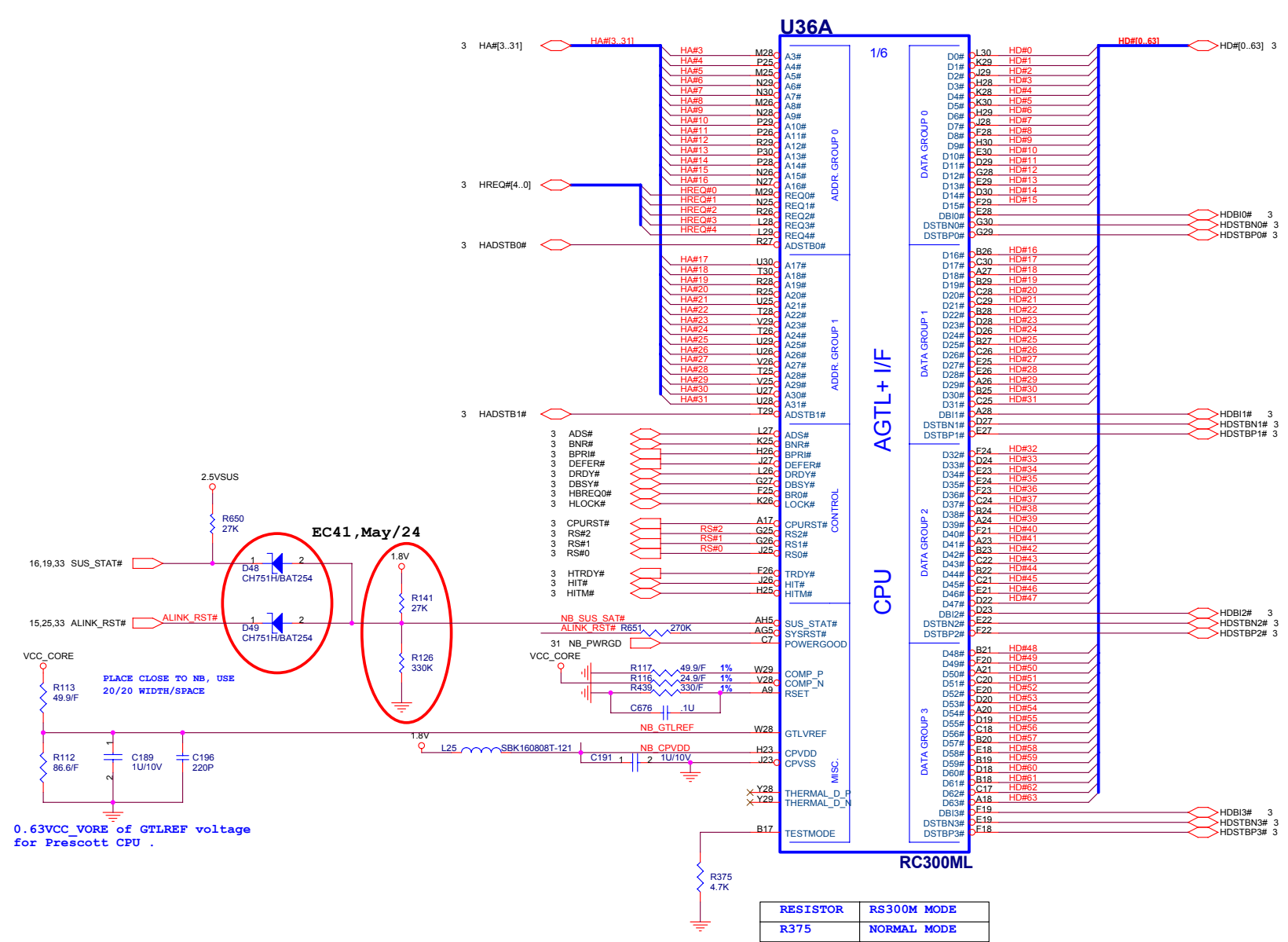
03

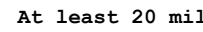


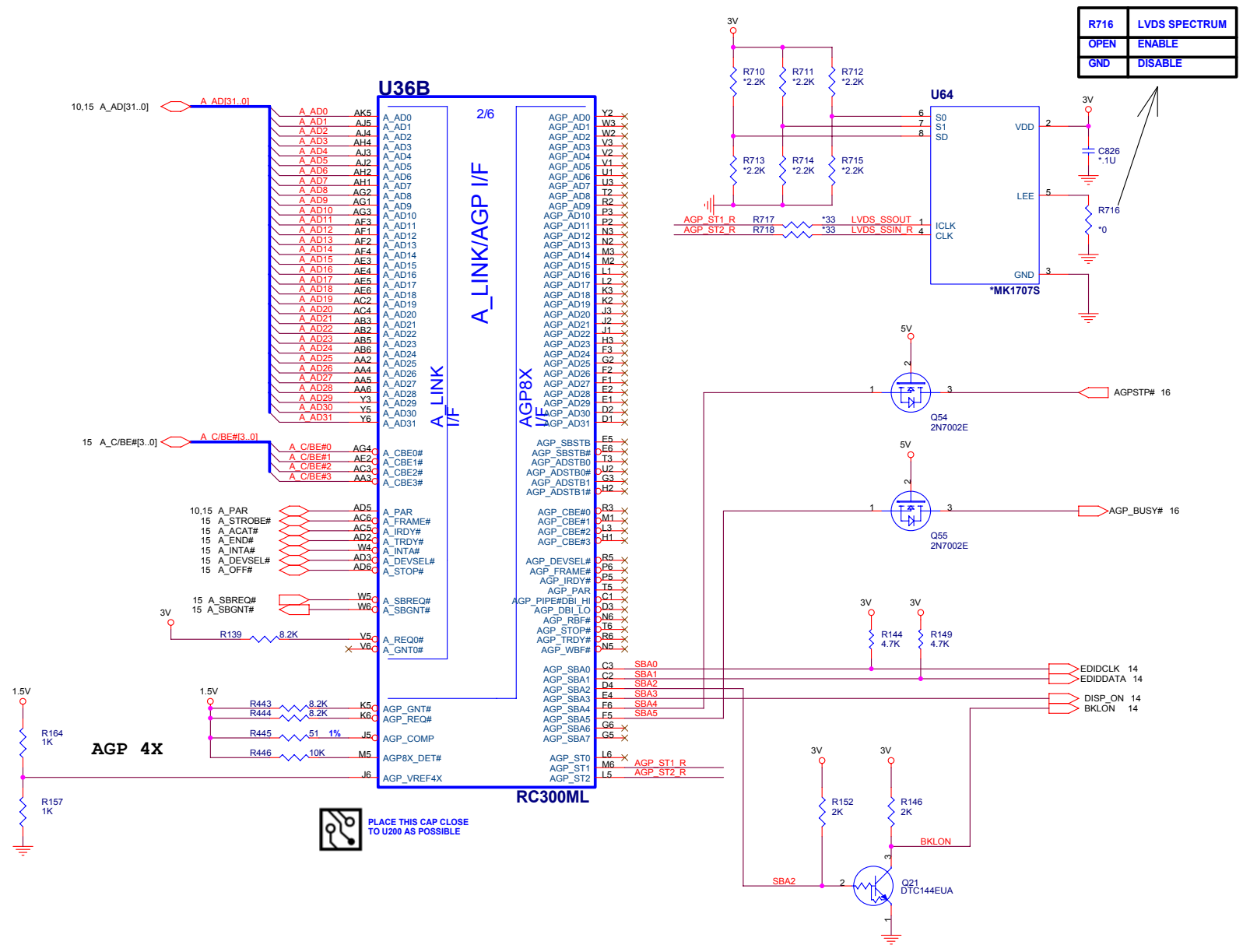
NORTHWOOD/Mobile-PRESCOTT CPU - PWR/GND

EC38, May/24



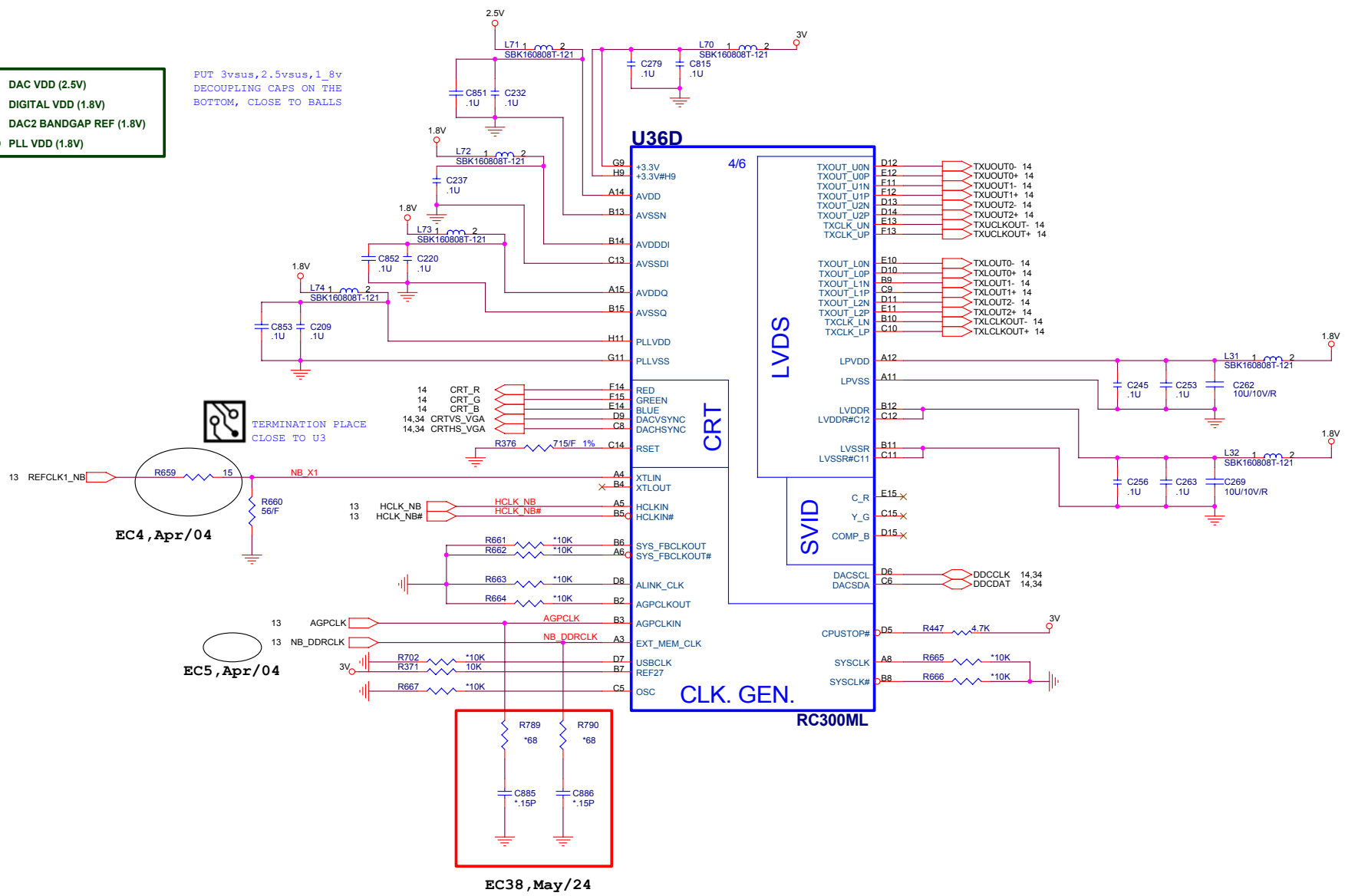




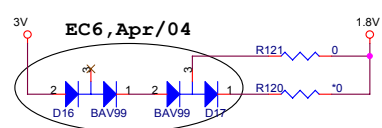


- AVDD DAC VDD (2.5V)
- AVDDDI DIGITAL VDD (1.8V)
- AVDDQ DAC2 BANDGAP REF (1.8V)
- PLLVD PLL VDD (1.8V)

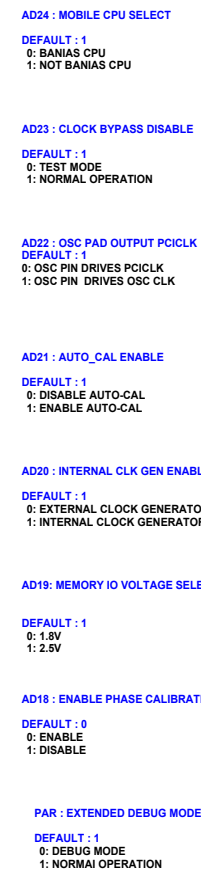
PUT 3vsus, 2.5vsus, 1.8v
DECOUPLING CAPS ON THE
BOTTOM, CLOSE TO BALLS

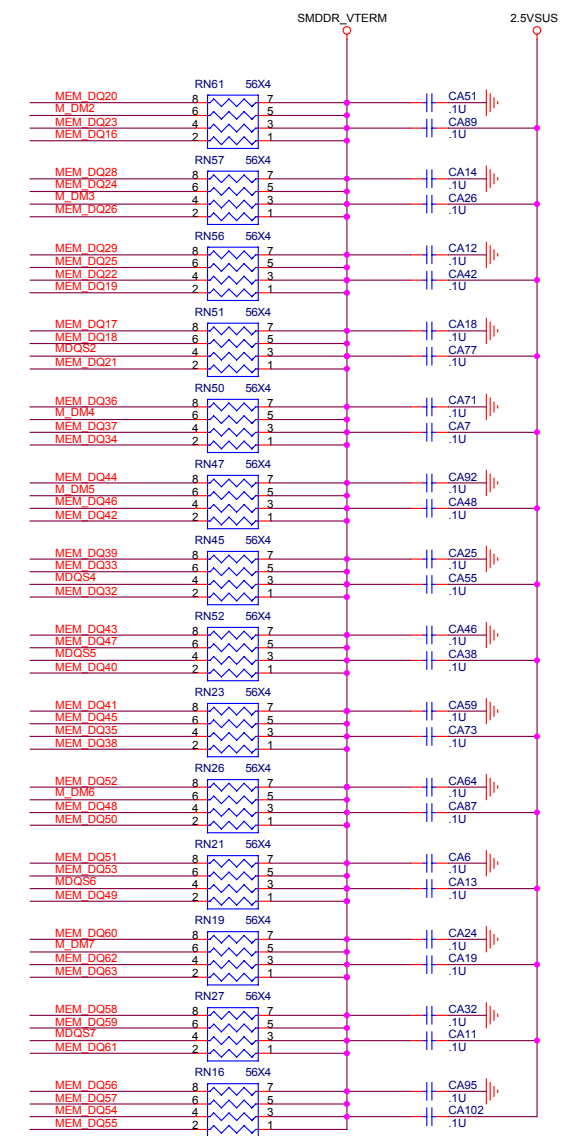
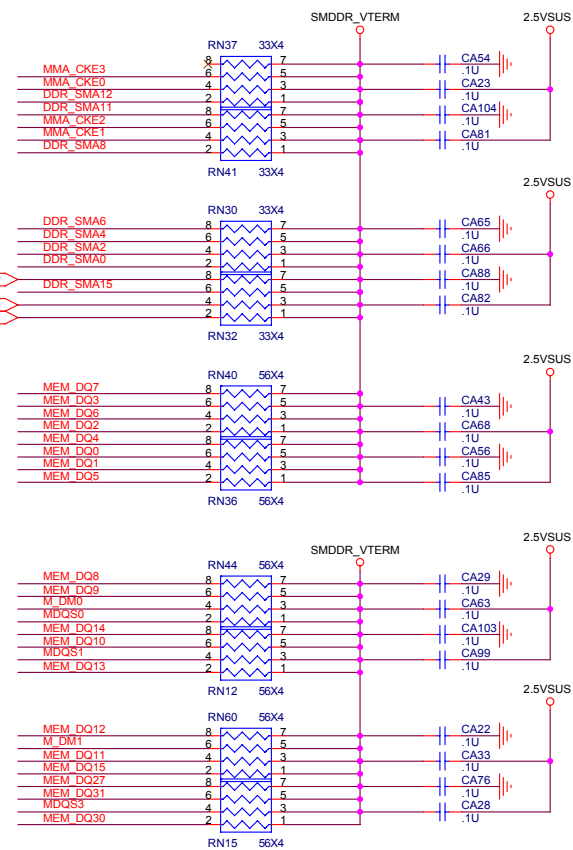
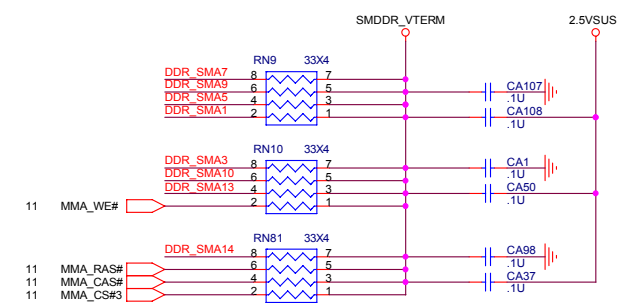
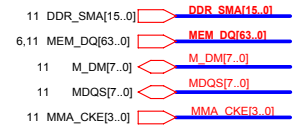


09

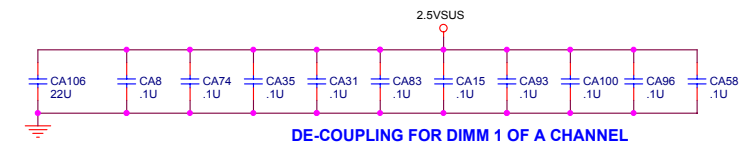
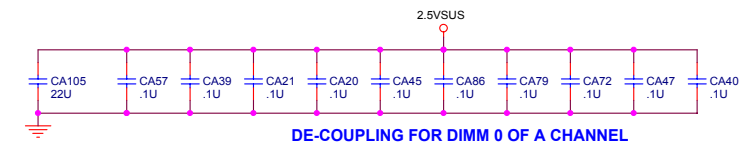


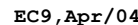
 PROJECT : EF5
Quanta Computer Inc.





- 1) 2 DE-COUPLING CAPS PER RPAK
- 2) PLACE RPAKS&RESISTORS AFTER THE LAST DIMM





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1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE AS U66 AS
POSSIBLE
2- ROUTE ALL CPUCLK/#, NBCLK/# AND
ITPClk/# AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U66
POWER PIN

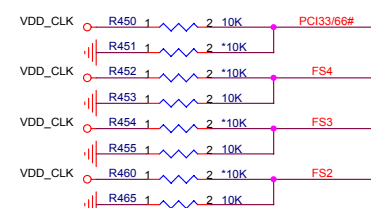
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EC42, May/24

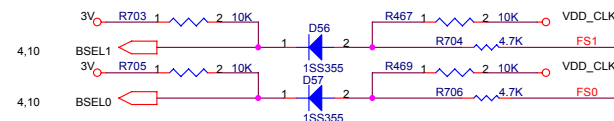
EC10, Apr/04

EC38, May/24

EXP. COST FREQUENCY OF CHECKS (PERCENT)																		
FS4 FS3 FS2 FS1 FS0					CPU	MEM	AGP	PCI	FS4 FS3 FS2 FS1 FS0					CPU	MEM	AGP	PCI	
0	0	0	0	0	0	100.01	100.01	66.66	66.66	1	0	0	0	0	99.51	99.51	66.66	66.66
0	0	0	0	0	1	133.33	133.33	66.66	66.66	1	0	0	0	1	132.69	132.69	66.66	66.66
0	0	0	0	1	0	200.01	200.01	66.66	66.66	1	0	0	1	0	199.02	199.02	66.66	66.66
0	0	0	0	1	1	166.64	166.64	66.66	66.66	1	0	0	1	1	165.85	165.85	66.66	66.66
0	0	0	1	0	0	100.01	133.34	66.66	66.66	1	0	1	0	0	99.51	99.51	66.66	66.66
0	0	0	1	0	1	133.34	100.01	66.66	66.66	1	0	1	0	1	132.68	132.68	66.66	66.66
0	0	0	1	1	0	133.16	166.45	66.66	66.66	1	0	1	1	0	132.59	132.59	66.66	66.66
0	0	0	1	1	1	166.45	133.16	66.66	66.66	1	0	1	1	1	165.73	165.73	66.66	66.66
0	1	0	0	0	0	105.00	105.00	66.66	66.66	1	1	0	0	0	99.38	99.38	66.66	66.66
0	1	0	0	0	1	140.00	140.00	66.66	66.66	1	1	0	0	1	132.52	132.52	66.66	66.66
0	1	0	0	1	0	66.67	66.67	66.66	66.66	1	1	0	1	0	198.77	198.77	66.66	66.66
0	1	0	0	1	1	175.00	175.00	66.66	66.66	1	1	0	1	1	165.64	165.64	66.66	66.66
0	1	1	0	0	0	109.99	109.99	66.66	66.66	1	1	1	0	0	99.38	132.51	66.66	66.66
0	1	1	0	0	1	146.66	146.66	66.66	66.66	1	1	1	0	1	132.51	99.38	66.66	66.66
0	1	1	1	0	0	210.00	210.00	66.66	66.66	1	1	1	1	0	132.36	165.45	66.66	66.66
0	1	1	1	1	1	183.27	183.27	66.66	66.66	1	1	1	1	1	165.45	132.36	66.66	66.66

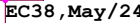


INTERNAL PULL DOWN



PROJECT : EF5
Quanta Computer Inc.

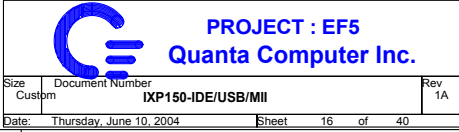
14



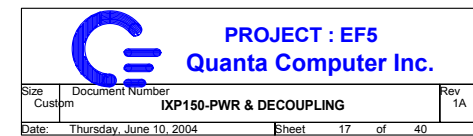
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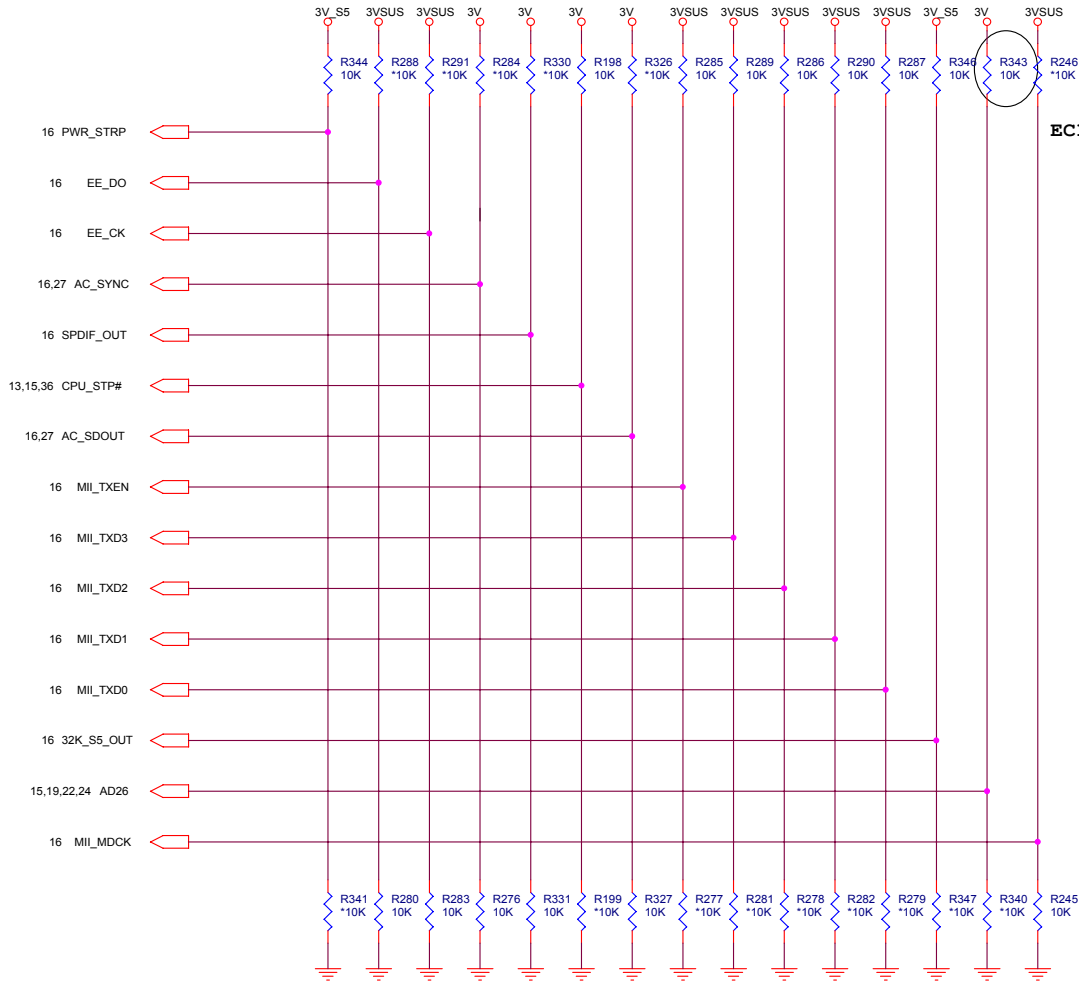
16



17

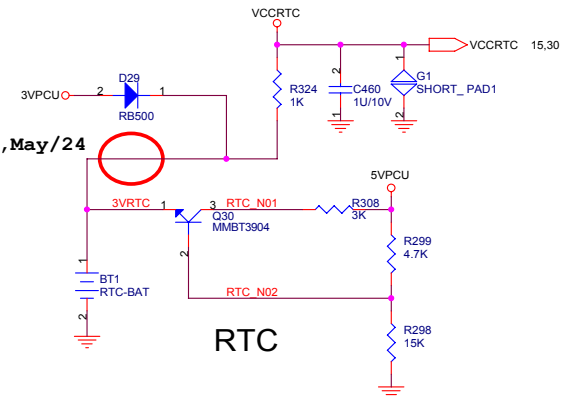


There is no such strap for A41 SB200

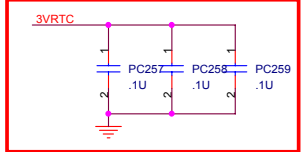


EC13, Apr/04

EC52, May/24



EC38, May/24

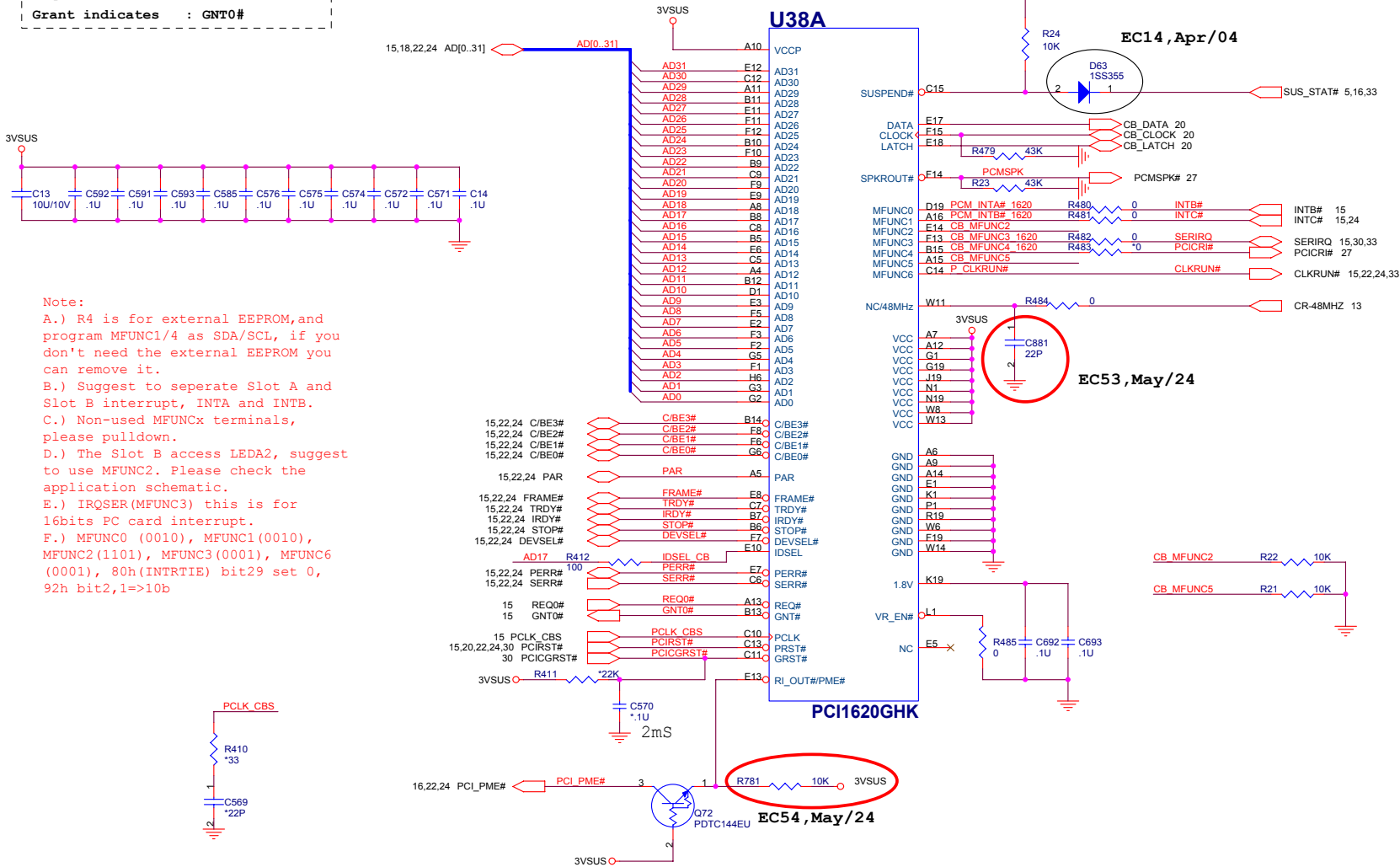


OVERLAP COMMON PADS
FOR DUAL-OP
RESISTORS

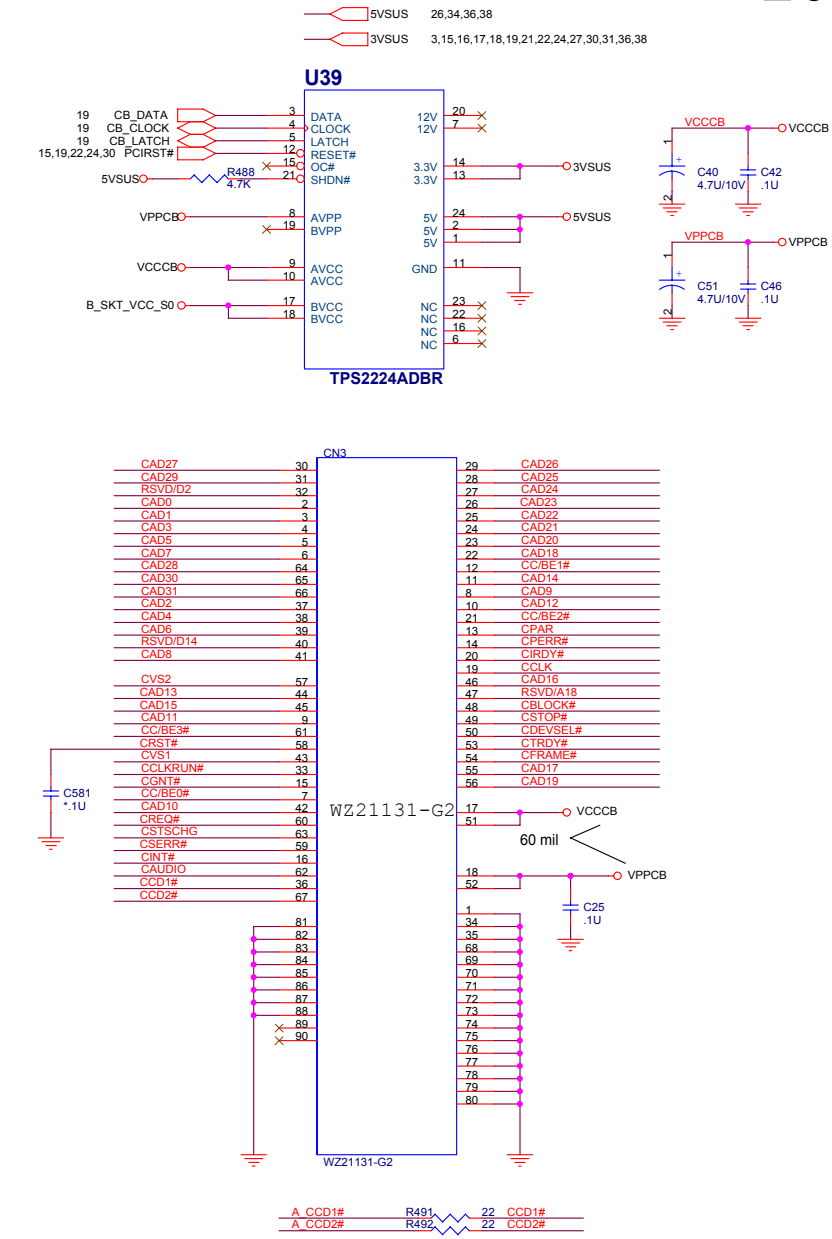
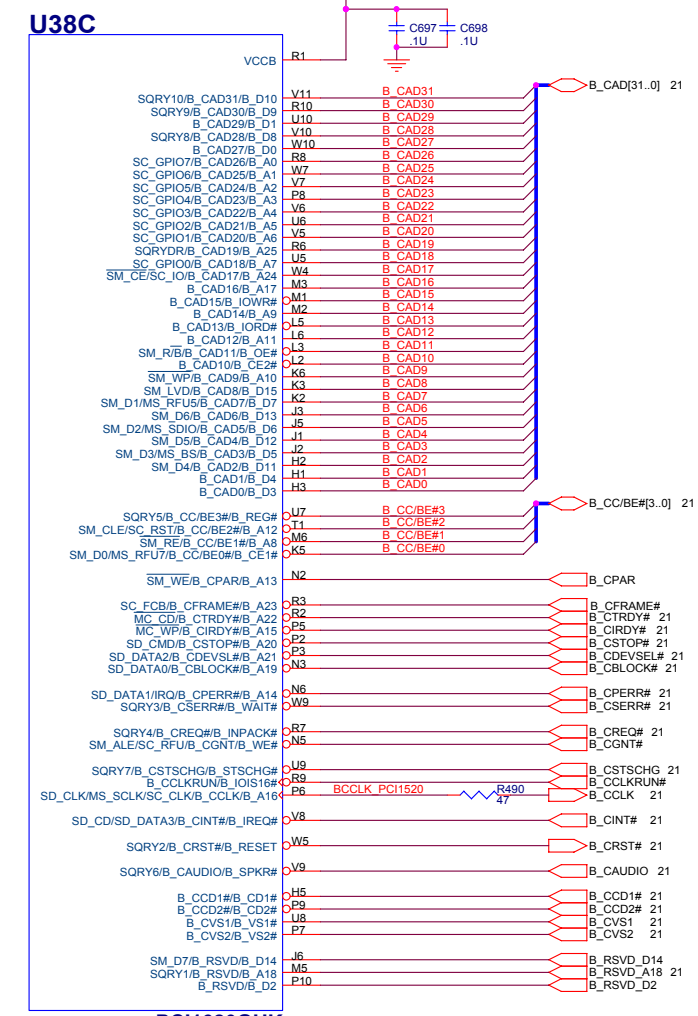
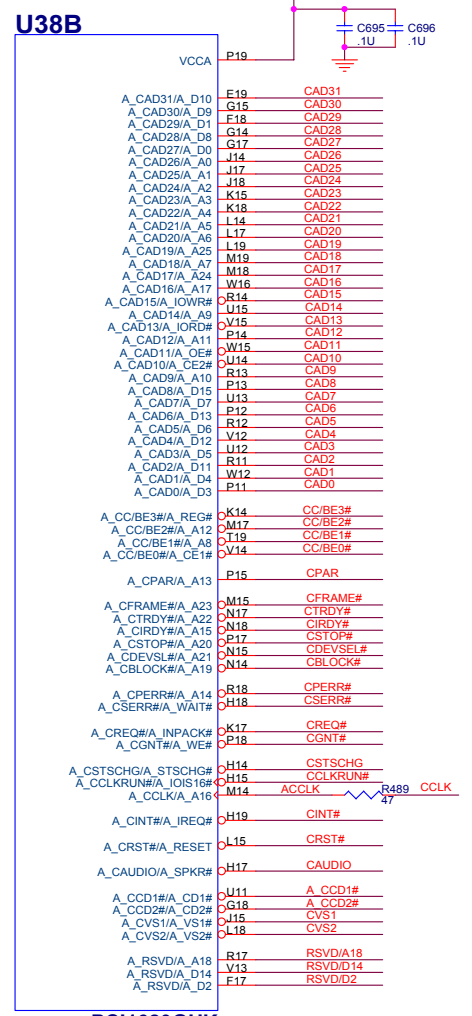
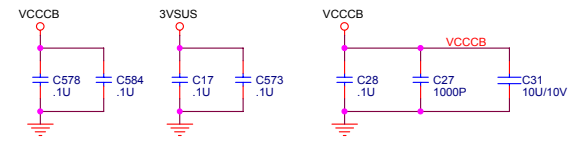
REQUIRED SYSTEM STRAPS

STRAP	PWR_STRP	EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	CPU_STP#	TX_EN	ETHERNET TXD[3:0]		32KHZ_S5	PCI_AD26
	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	ROM ON PCI BUS	INIT ACTIVE HIGH(AMD)	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP DEFAULT	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER		32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT	BIOS use LPC cycle DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (P4) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP	ENABLE CPU FREQSETTING			32KHZ INPUT TO SB200 (EXT RTC)	BIOS uSE FWH Cycle

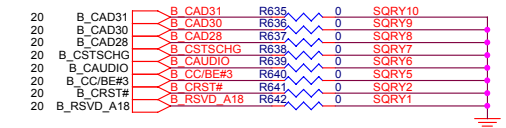
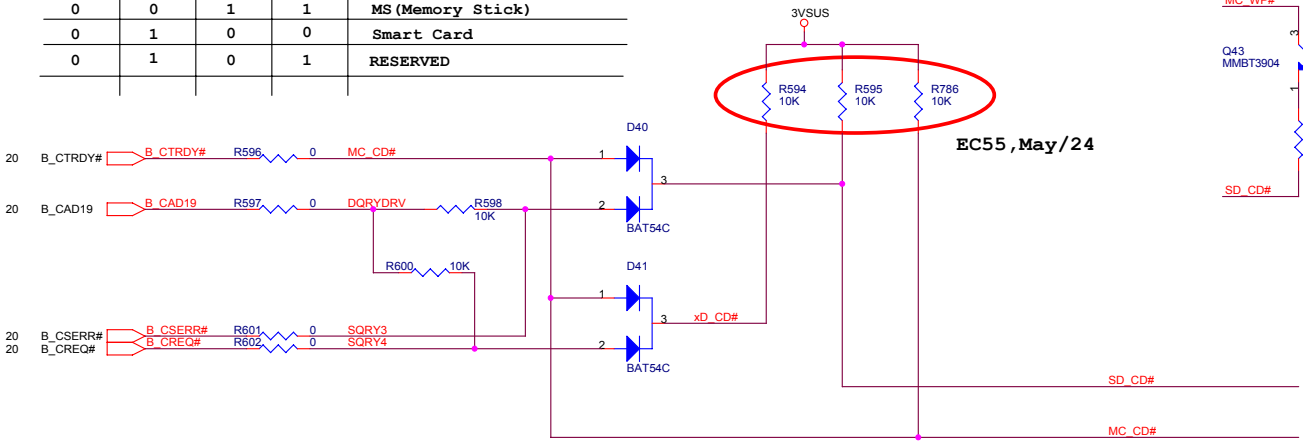
ID Select : AD17
Interrupt Pin : INTB#, INTC#
Request indicates : REQ0#
Grant indicates : GNT0#



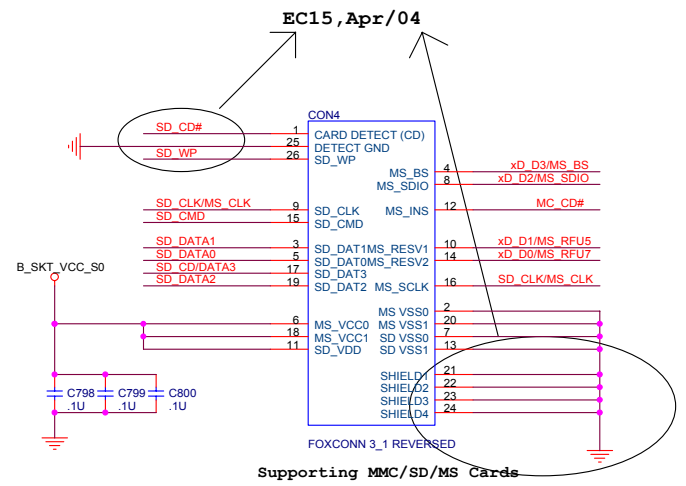
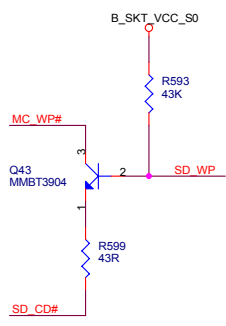
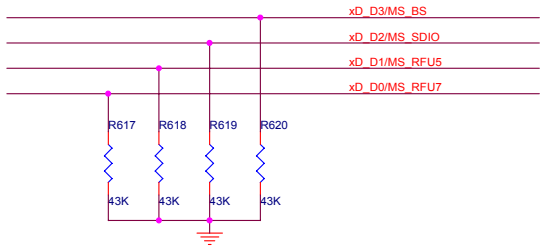
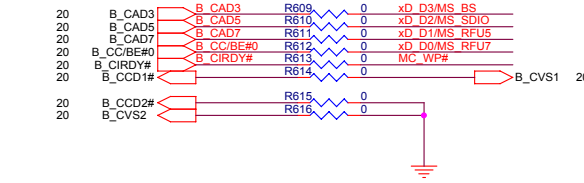
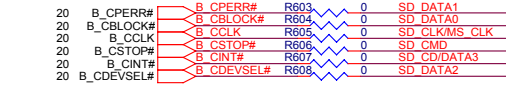
CARDREADER I/F & CARDBUS SLOT



SQRY6	SQRY5	SQRY4	SQRY3	Interface Implement
0	0	0	0	RESERVED
0	0	0	1	SM/XD
0	0	1	0	SD/MMC
0	0	1	1	MS (Memory Stick)
0	1	0	0	Smart Card
0	1	0	1	RESERVED

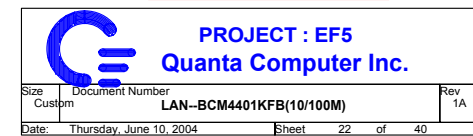


SQRY2	SQRY1	Card Voltage
0	0	Vcc=3.3V, Vpp/Vcore=1.8V
0	1	Vcc=5V, Vpp=3.3V
1	0	RESERVED

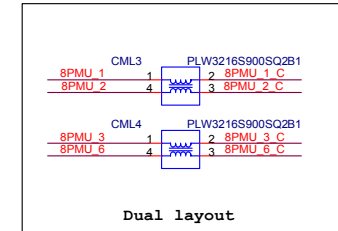
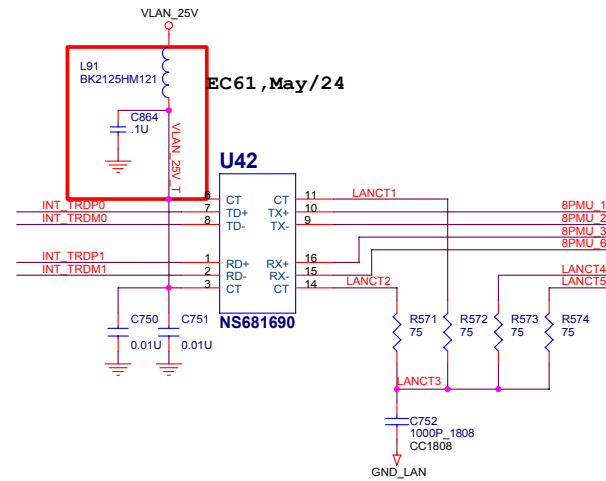
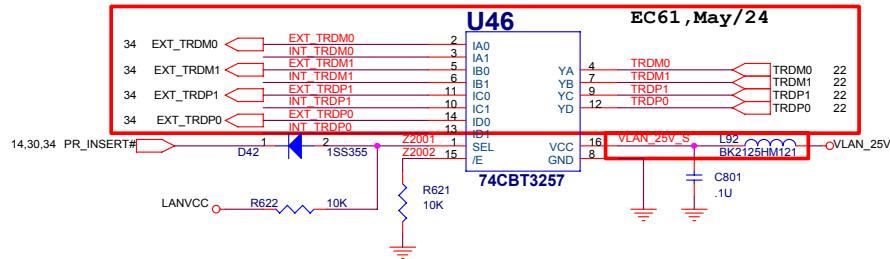


BCM4401--10/100
BCM5705--10/100/GIGA

EC56, May/24



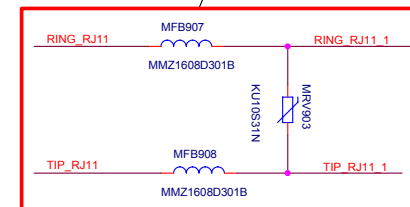
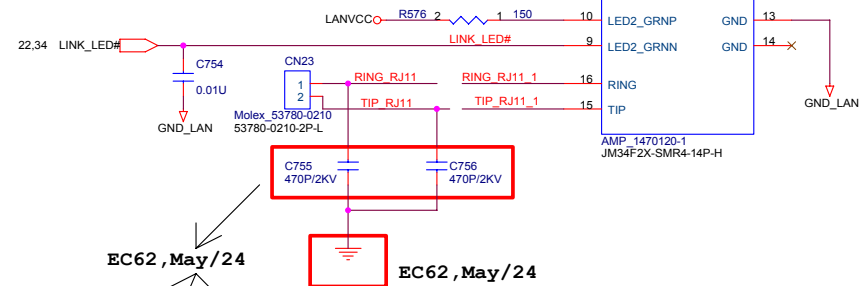
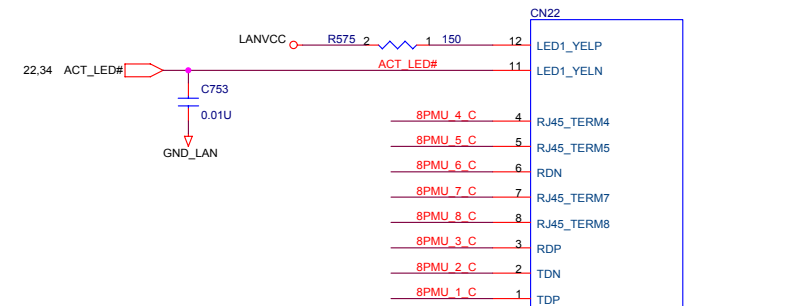
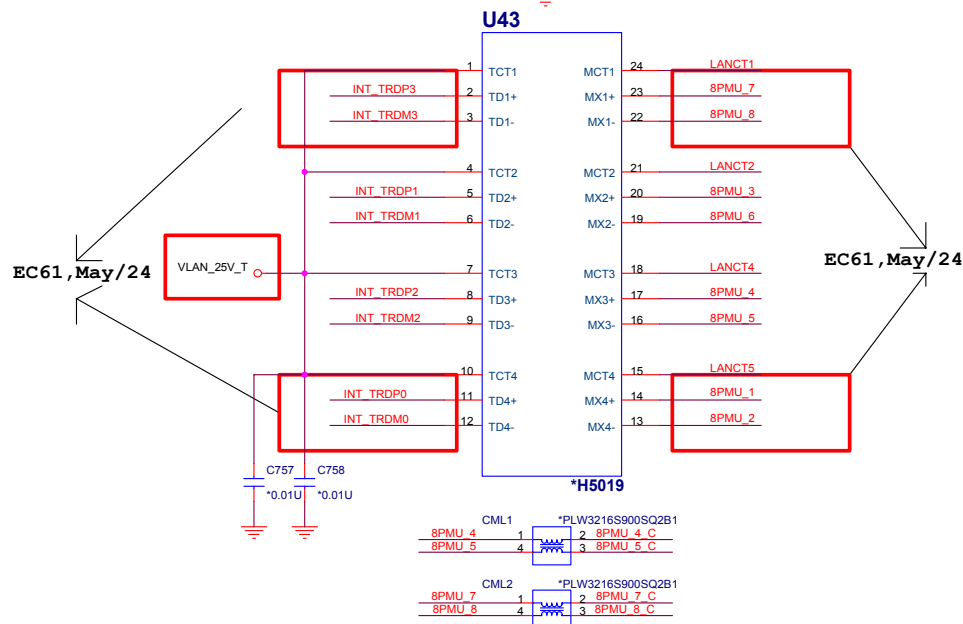
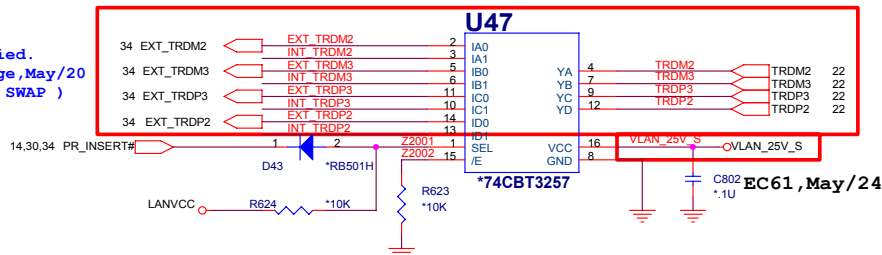
SWITCHING BETWEEN SYSTEM AND PORT REPLICATOR



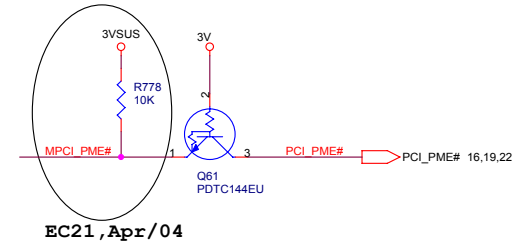
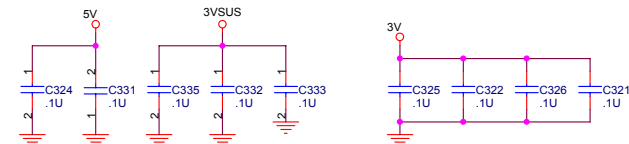
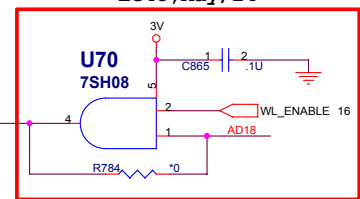
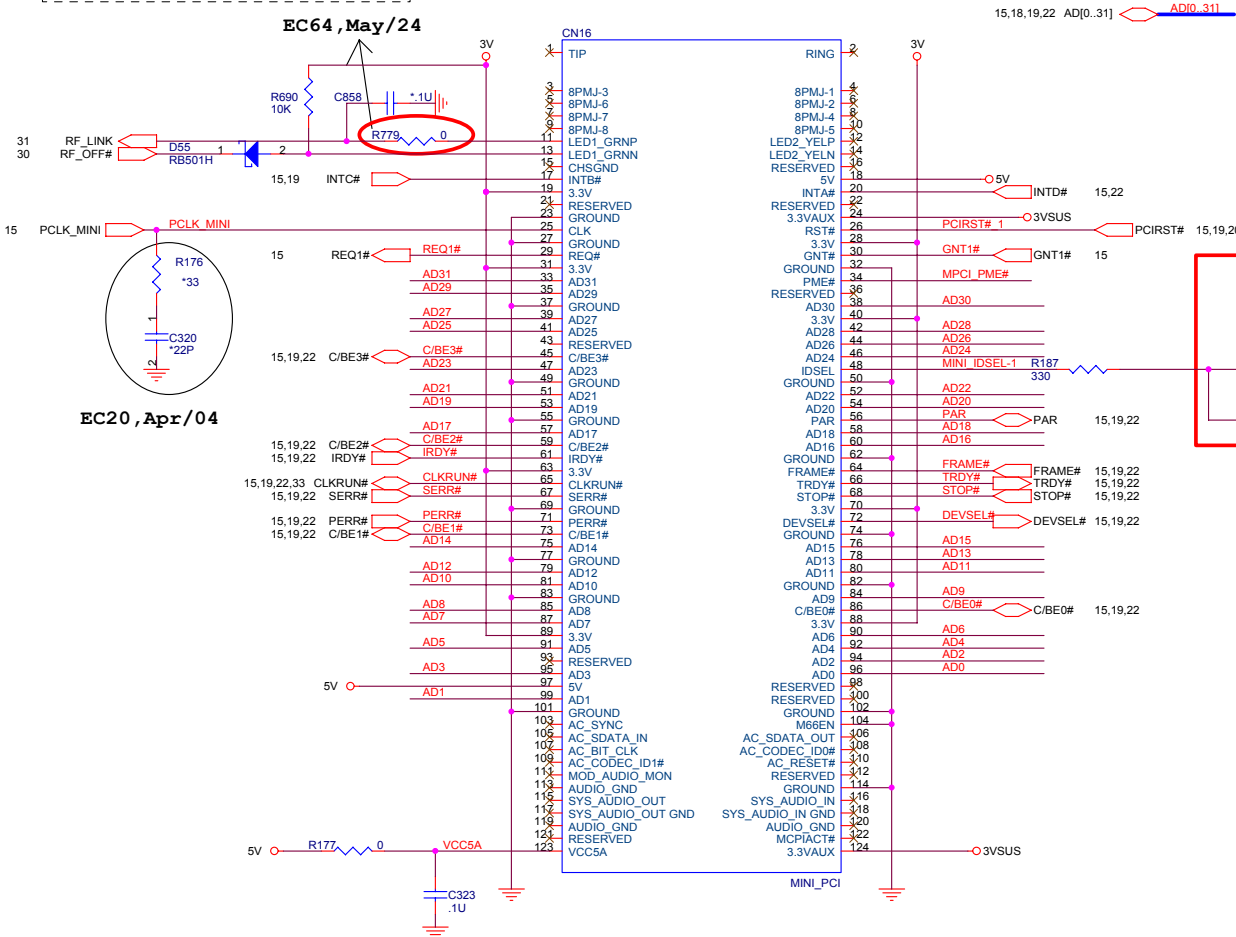
Reserved for Gigabit

Modified.
 C-Stage, May/20
 (PIN SWAP)

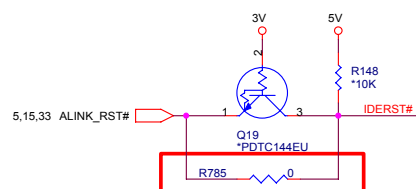
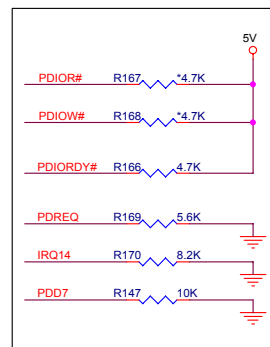
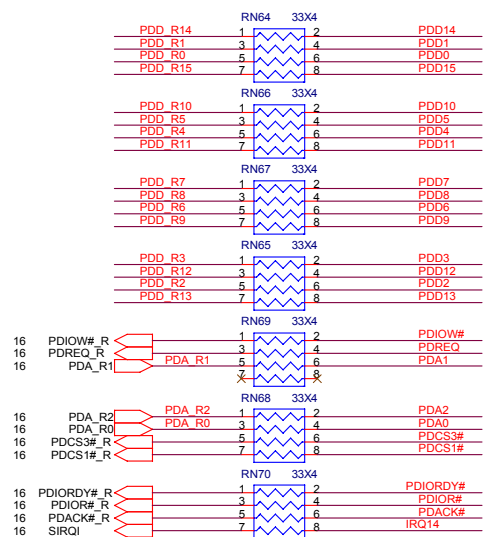
EC61, May/24



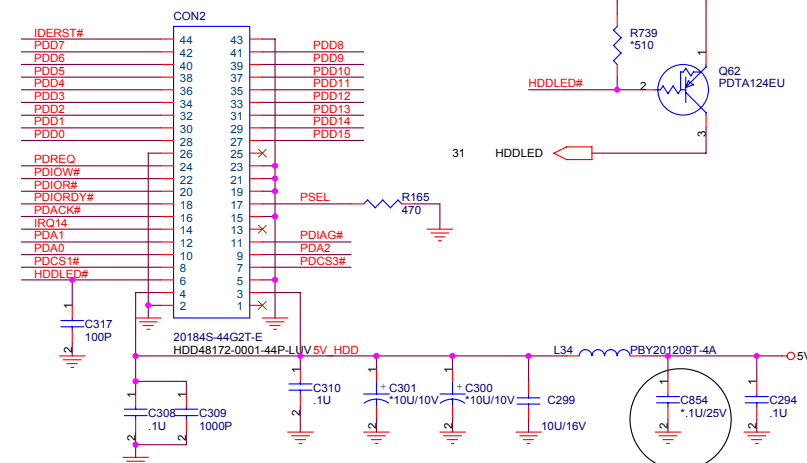
ID Select : AD18
Interrupt Pin : INTC# , INTD#
Request indicates : REQ1#
Grant indicates : GNT1#



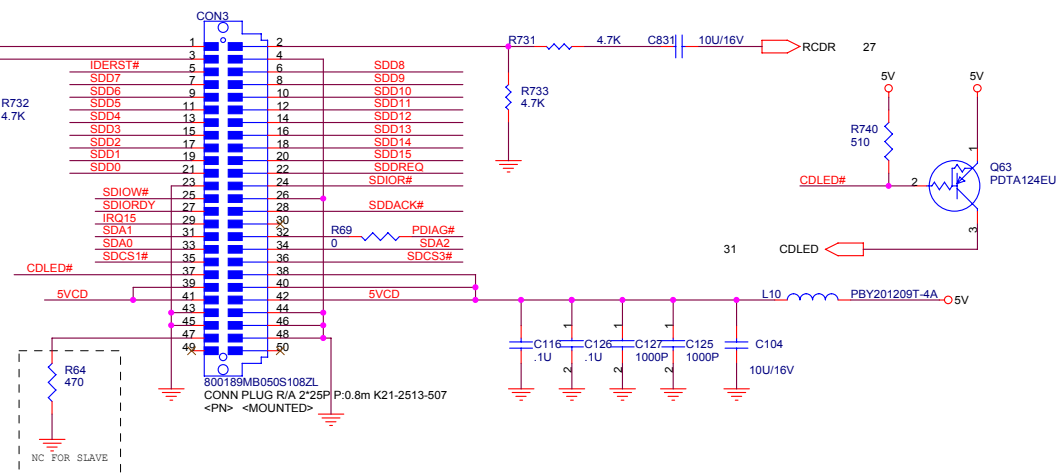
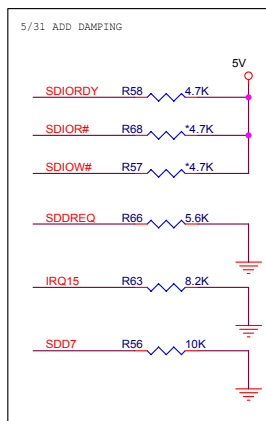
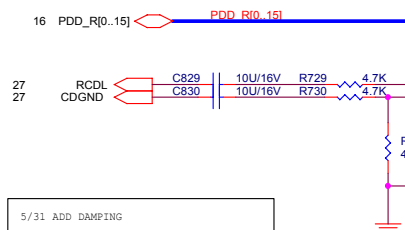
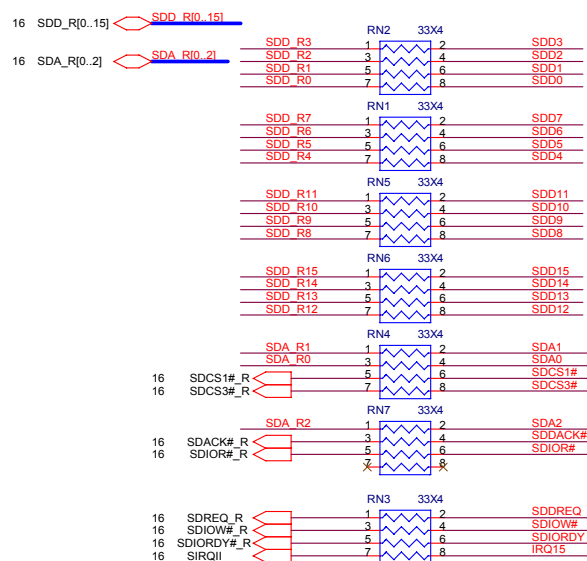
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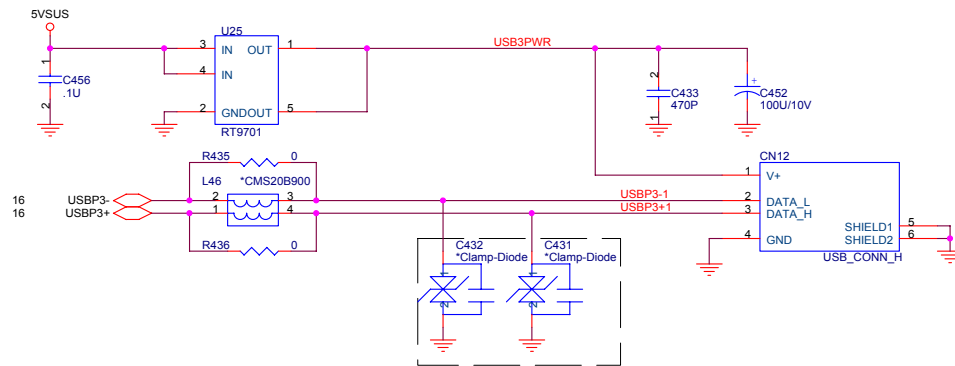
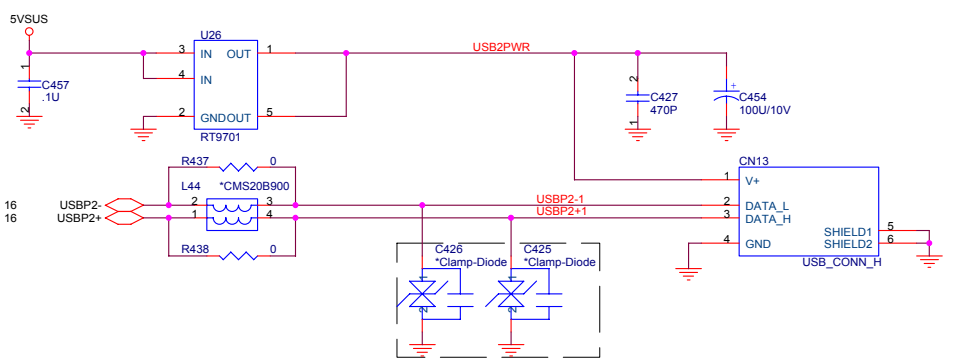
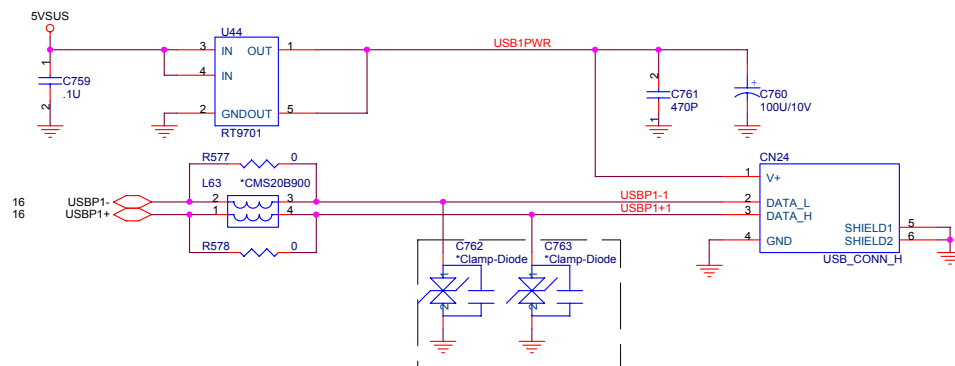
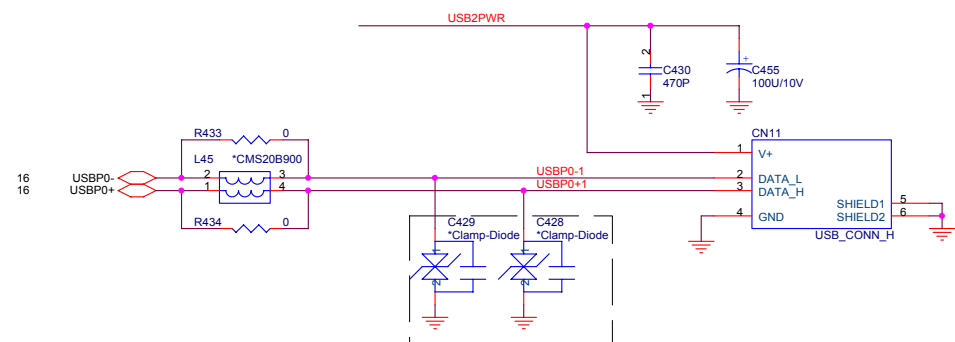
EC64 , May/24



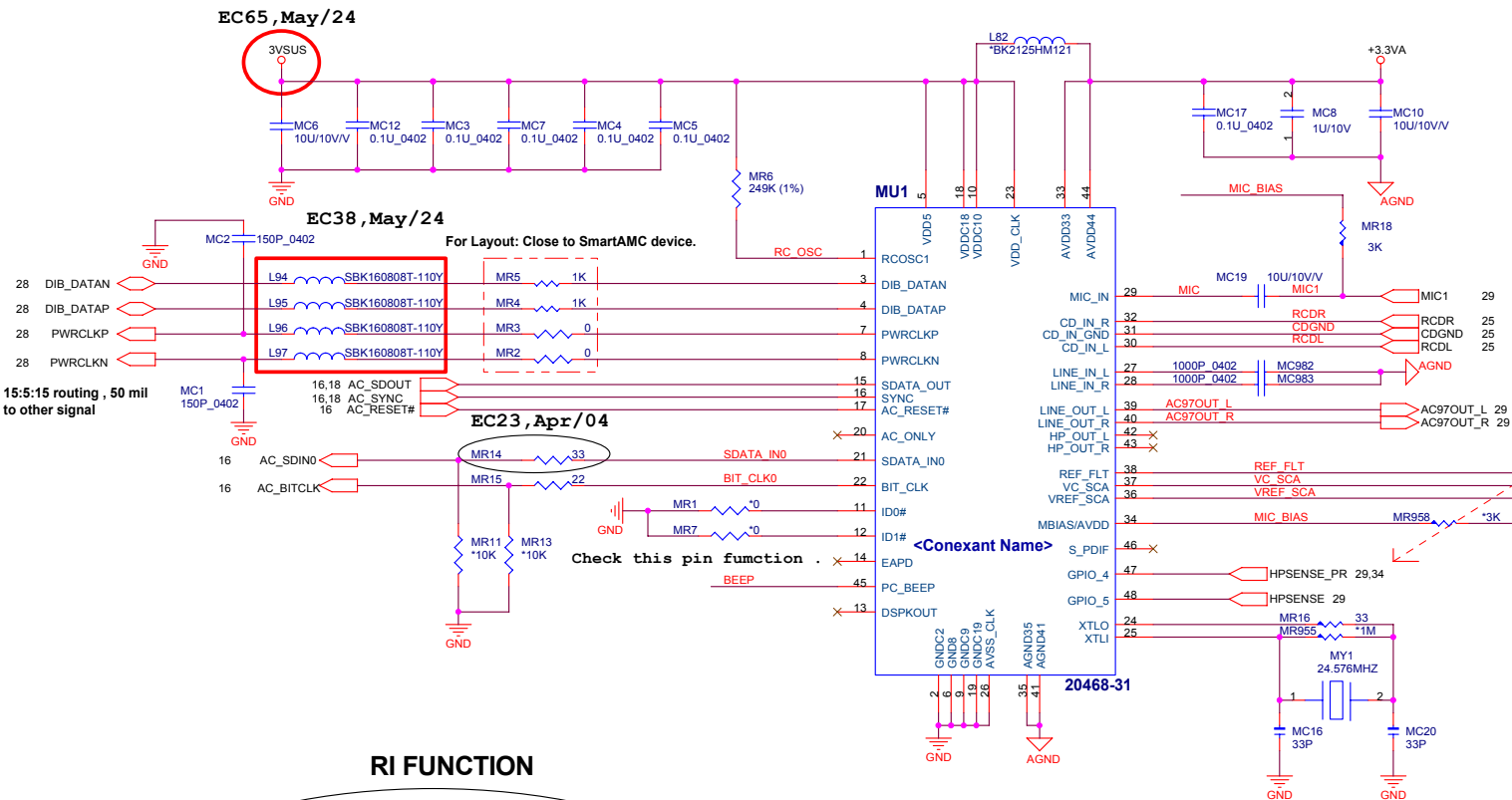
EC22, Apr/04



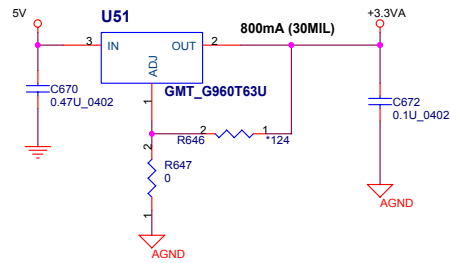
PROJECT : EF5
Quanta Computer Inc.



For Layout:
Place decoupling caps near the power pins of
SmartAMC device.



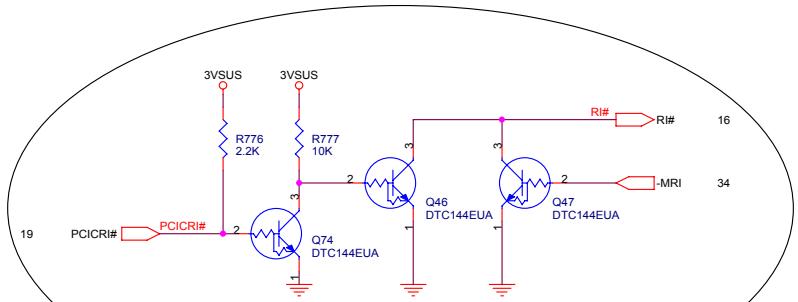
CODEC POWER



SOFTWARE EQ CONTROL TABLE

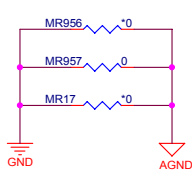
GPIO4	GOIO5	S/W EQ
LOW	LOW	ON
LOW	HIGH	OFF
HIGH	LOW	OFF
HIGH	HIGH	OFF

RI FUNCTION

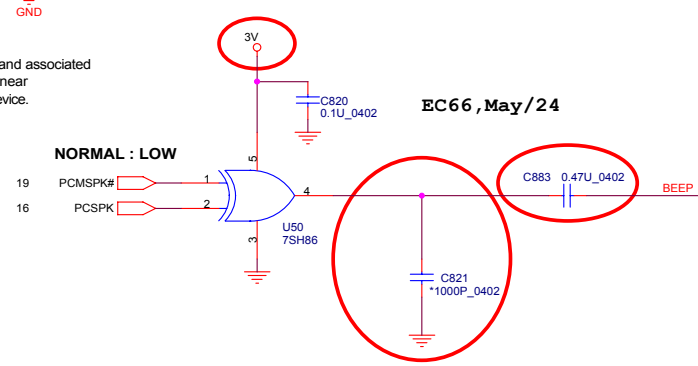


EC24, Apr/04

Ground Tie



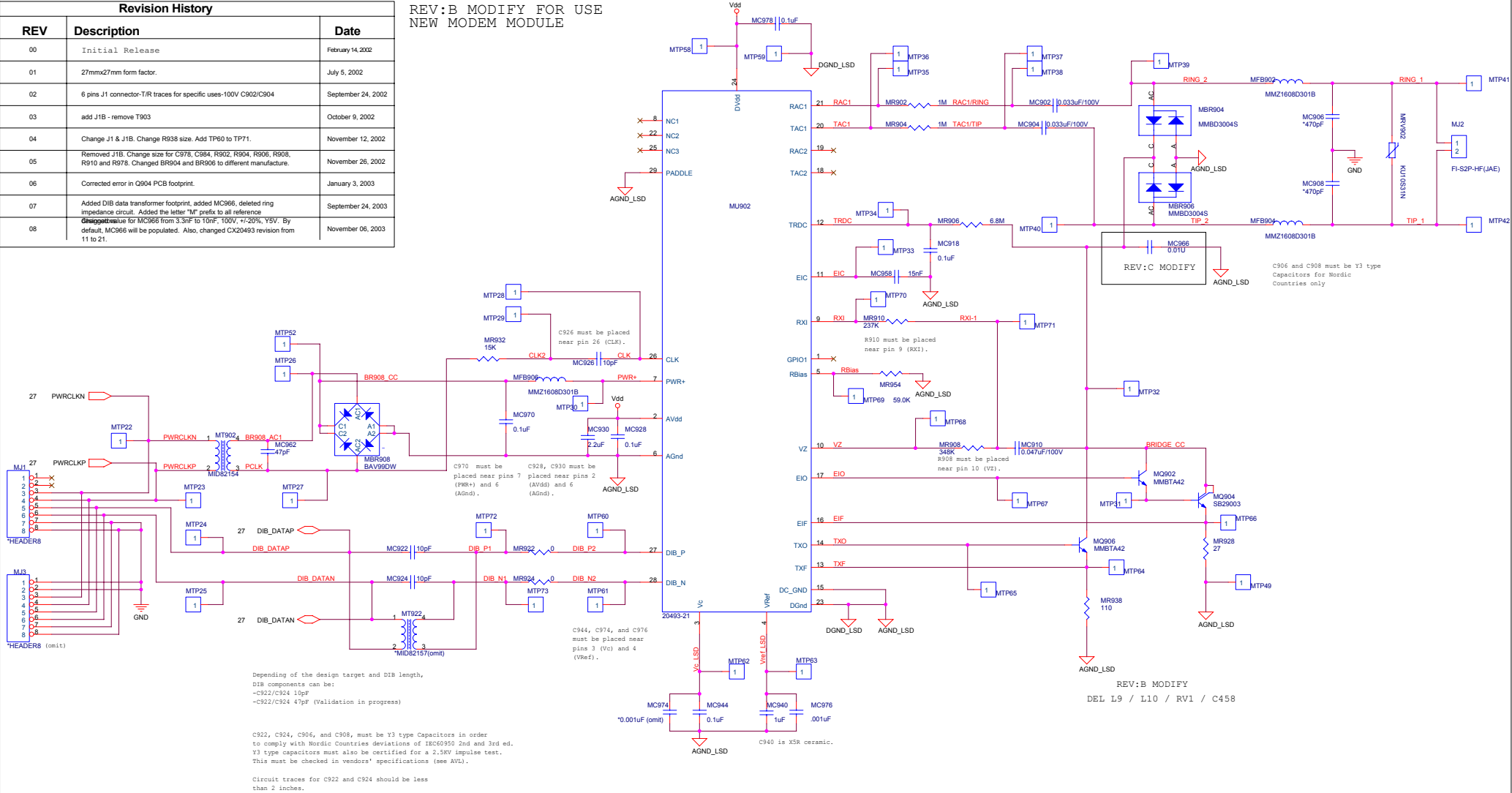
PC BEEP CONTROL

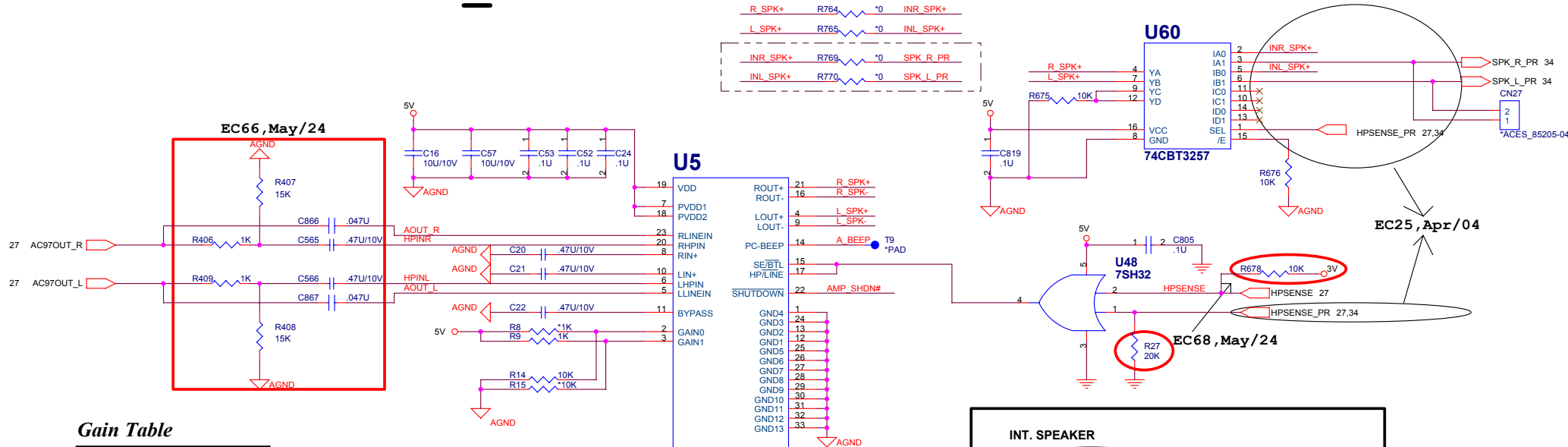


For Layout:
Place crystal and associated
circuitry very near
SmartAMC Device.

Revision History		
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

REV:B MODIFY FOR USE
NEW MODEM MODULE

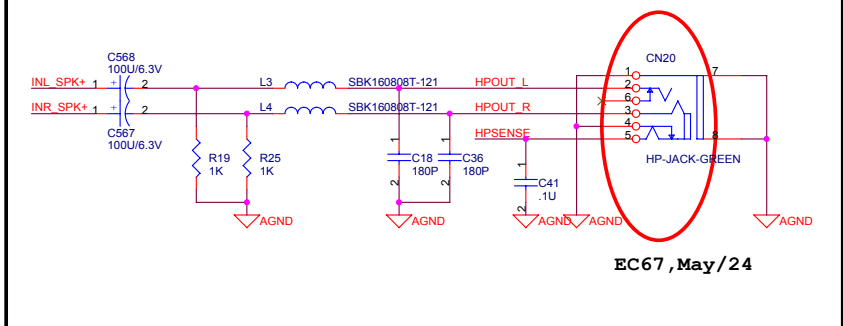




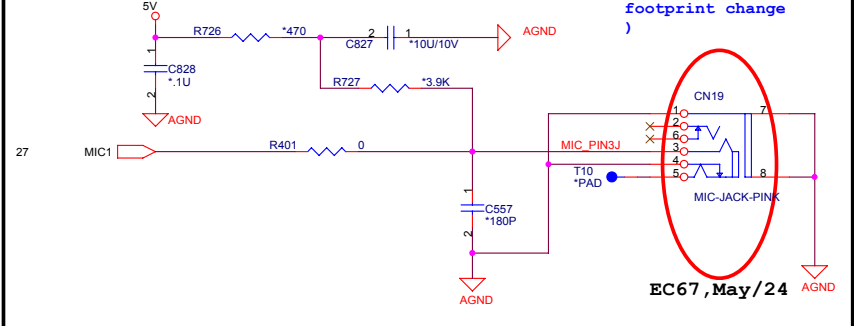
Gain Table

Gain0	Gain1	Av
0	0	2 times
0	1	6 times
1	0	12 times
1	1	24 times

Headphone out



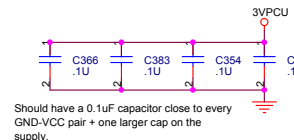
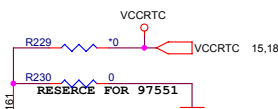
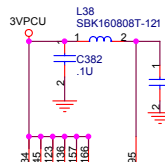
Mic in



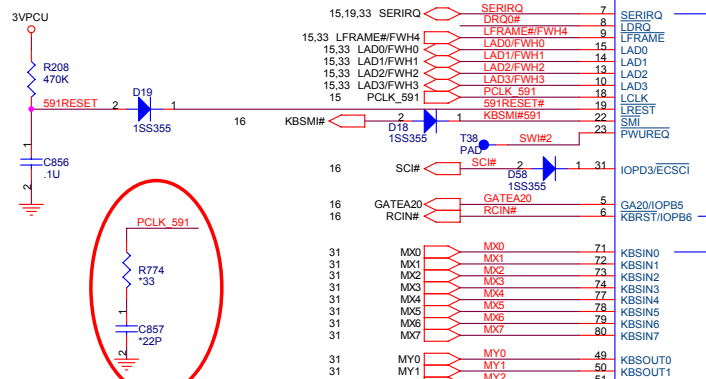
LDRQ#(pin 8) internal is no use

15.33 LPC_DRQ0# ← LPC_DRQ0# R212 *0 DRQ0#

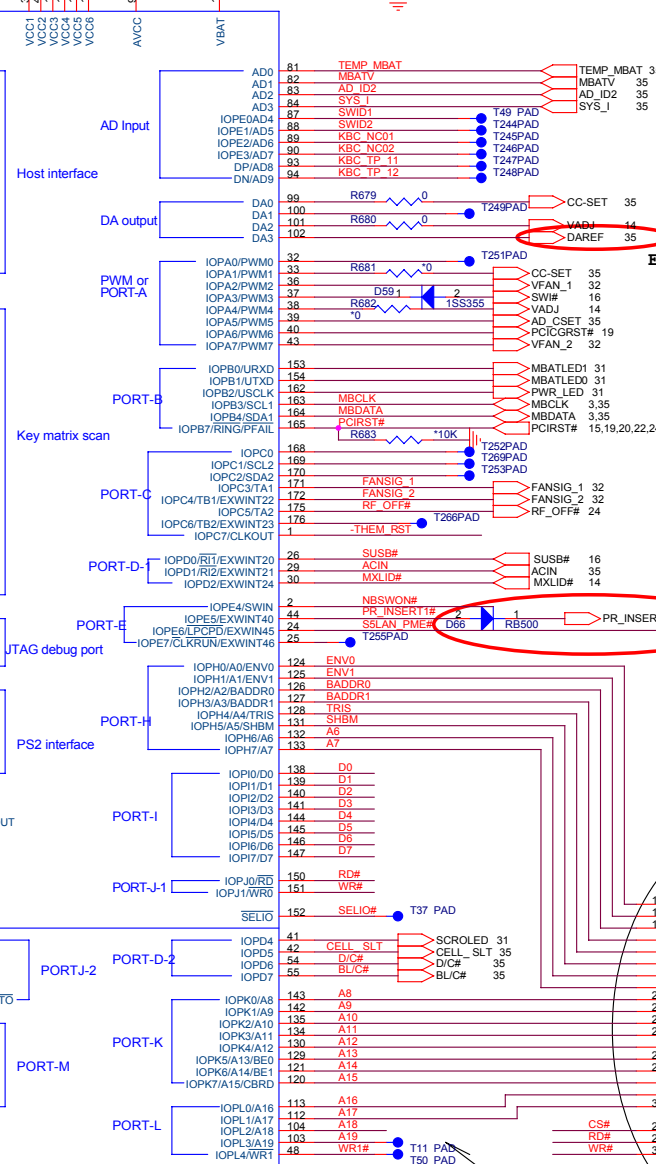
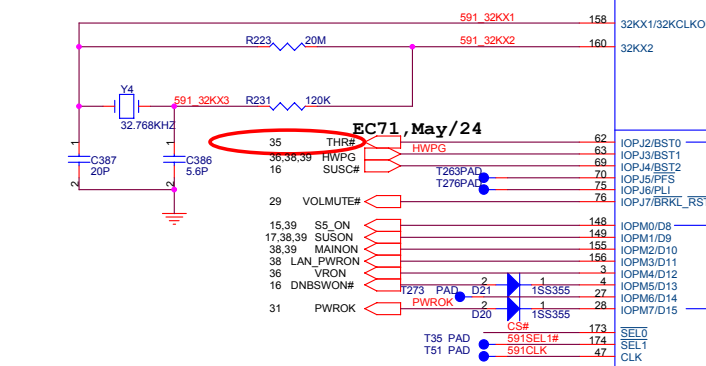
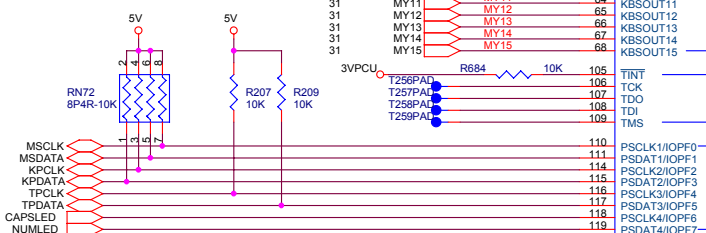
U1



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply



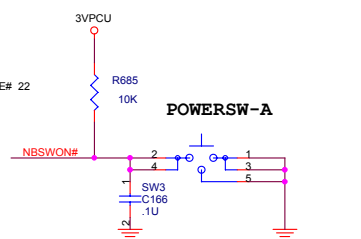
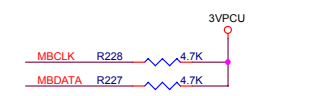
EC27, Apr/04



EC71, May/24

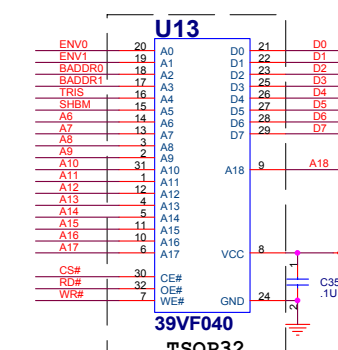
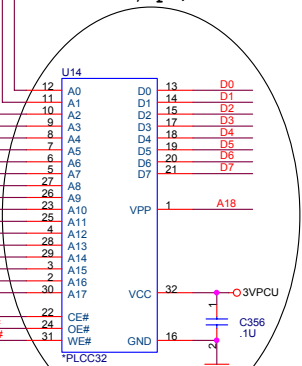
EC72, May/24

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+
1 1	Reserved	



POWERSW-A

EC28 , Apr / 04



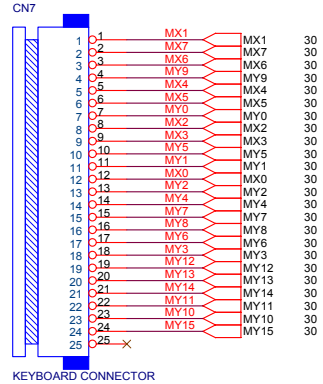
PC97551VPC

Pin 103 internal is "A19", Can't use to GPIO

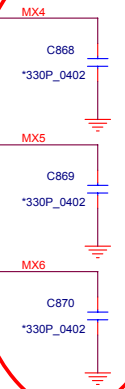
KEYBOARD CONN & INDICATOR

31

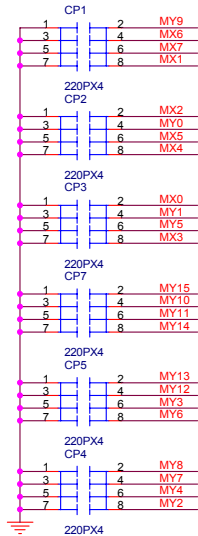
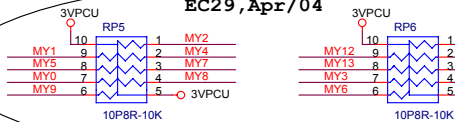
KEYBOARD CONNECTOR



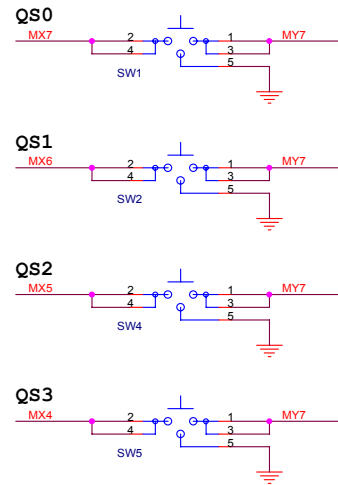
EC38, May/24



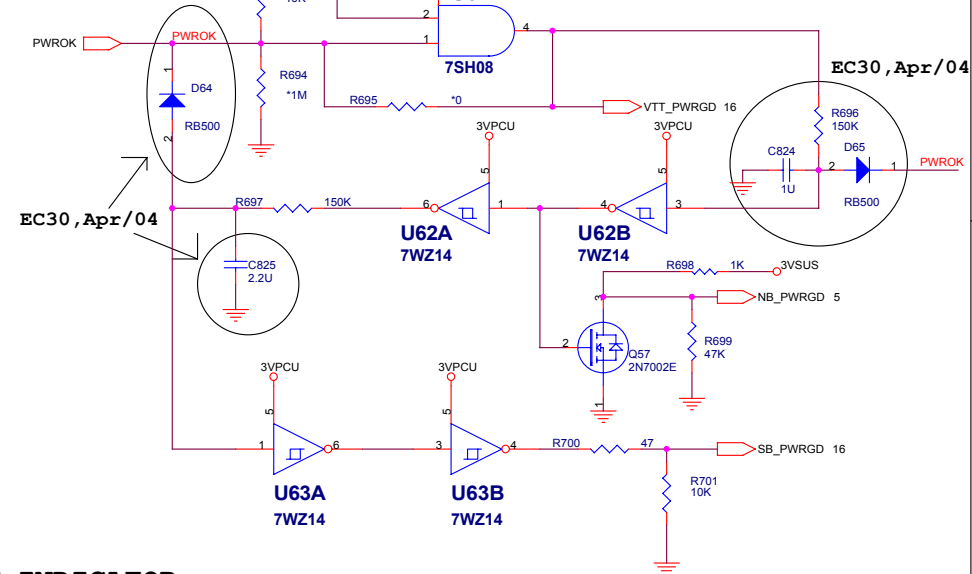
EC29, Apr/04



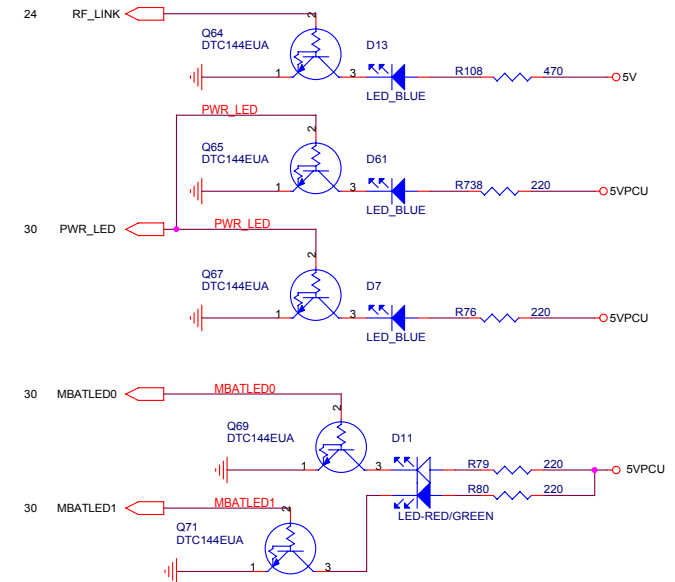
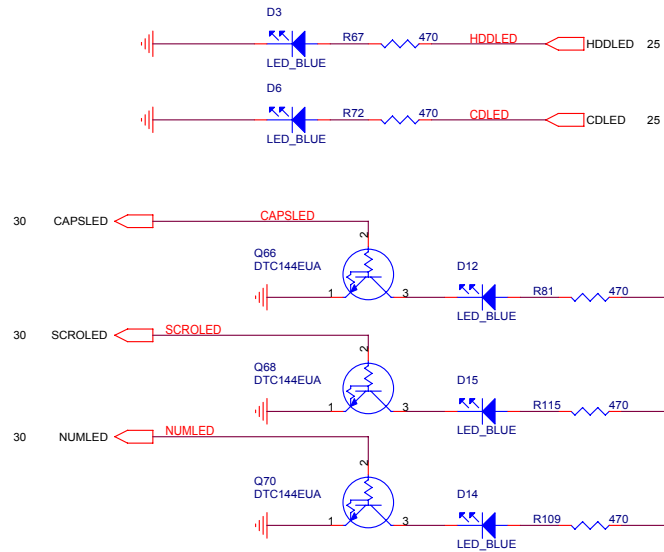
QUICK SWITCH



EC30, Apr/04

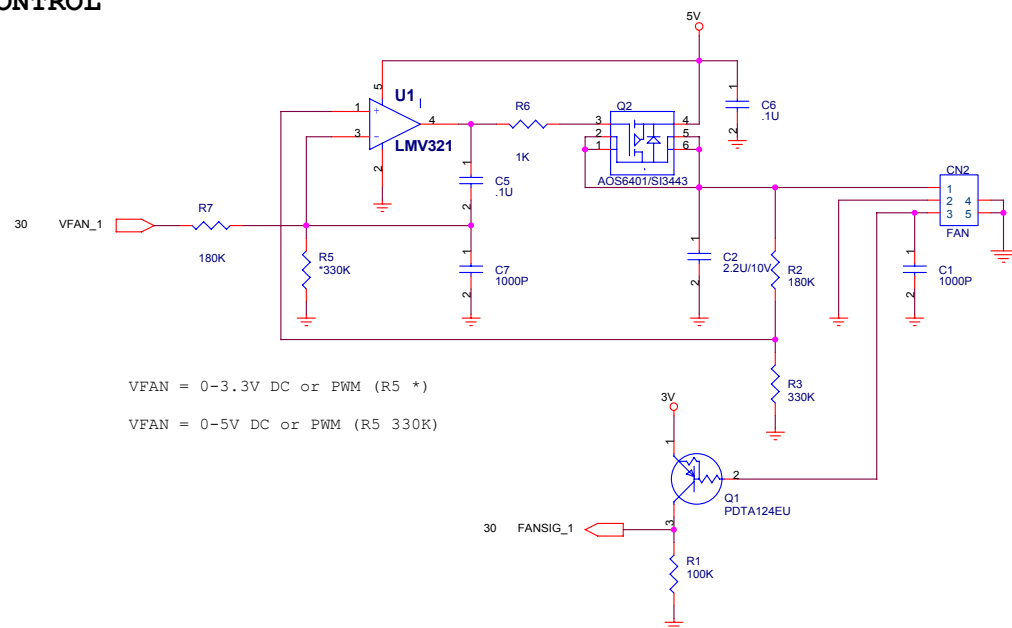


SYSTEM INDICATOR



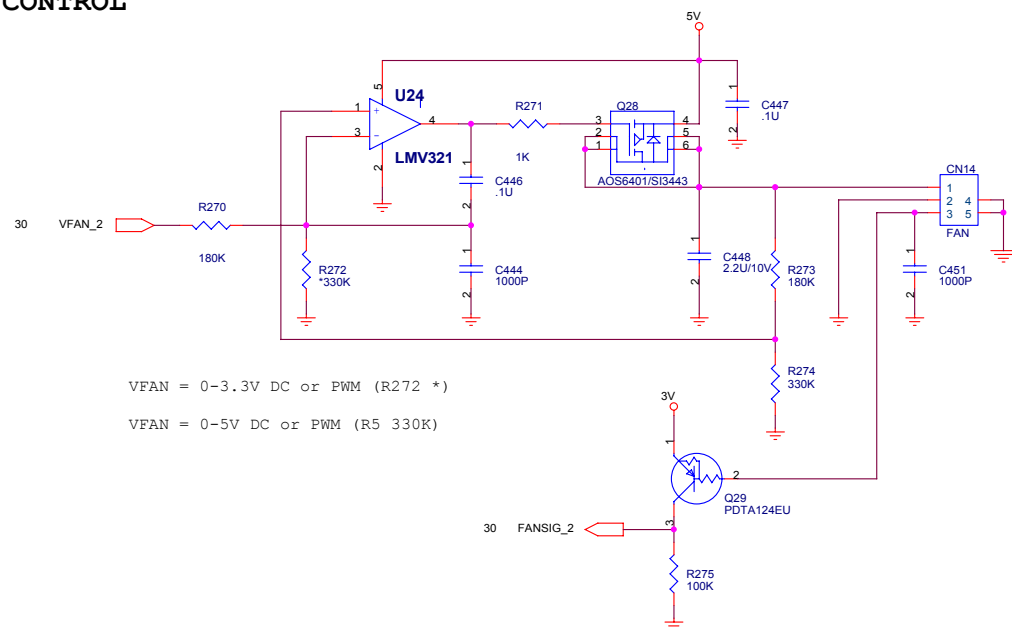
PROJECT : EF5
Quanta Computer Inc.

FAN1 CONTROL



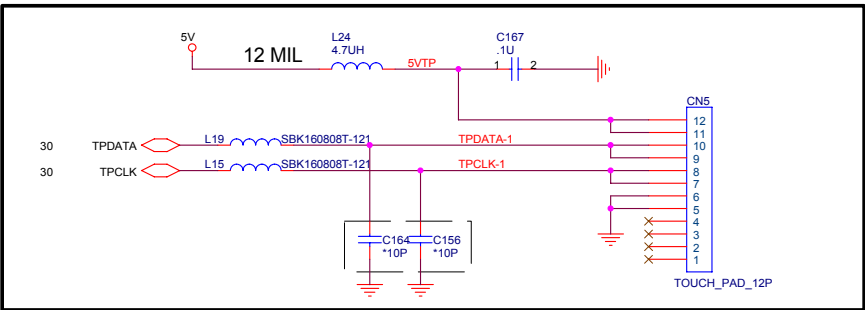
VFAN = 0-3.3V DC or PWM (R5 *)
VFAN = 0-5V DC or PWM (R5 330K)

FAN2 CONTROL

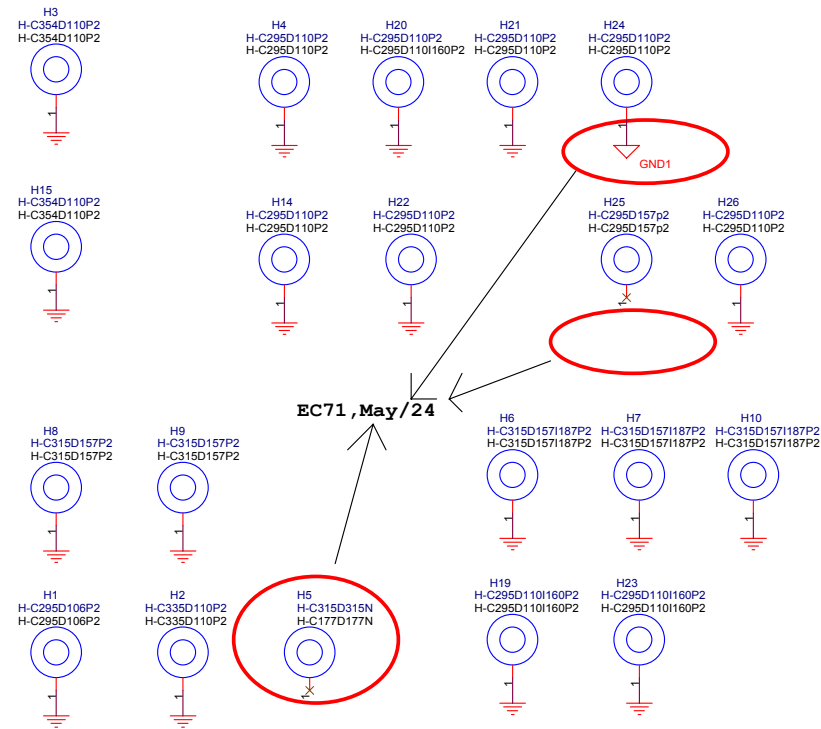


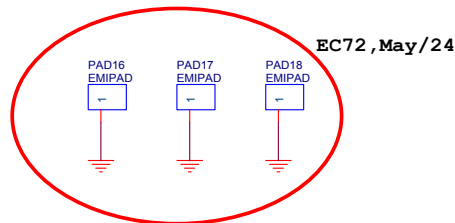
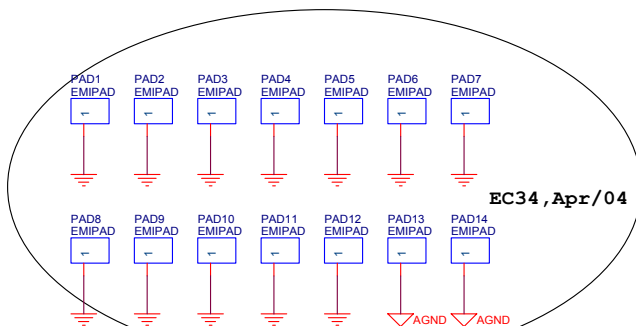
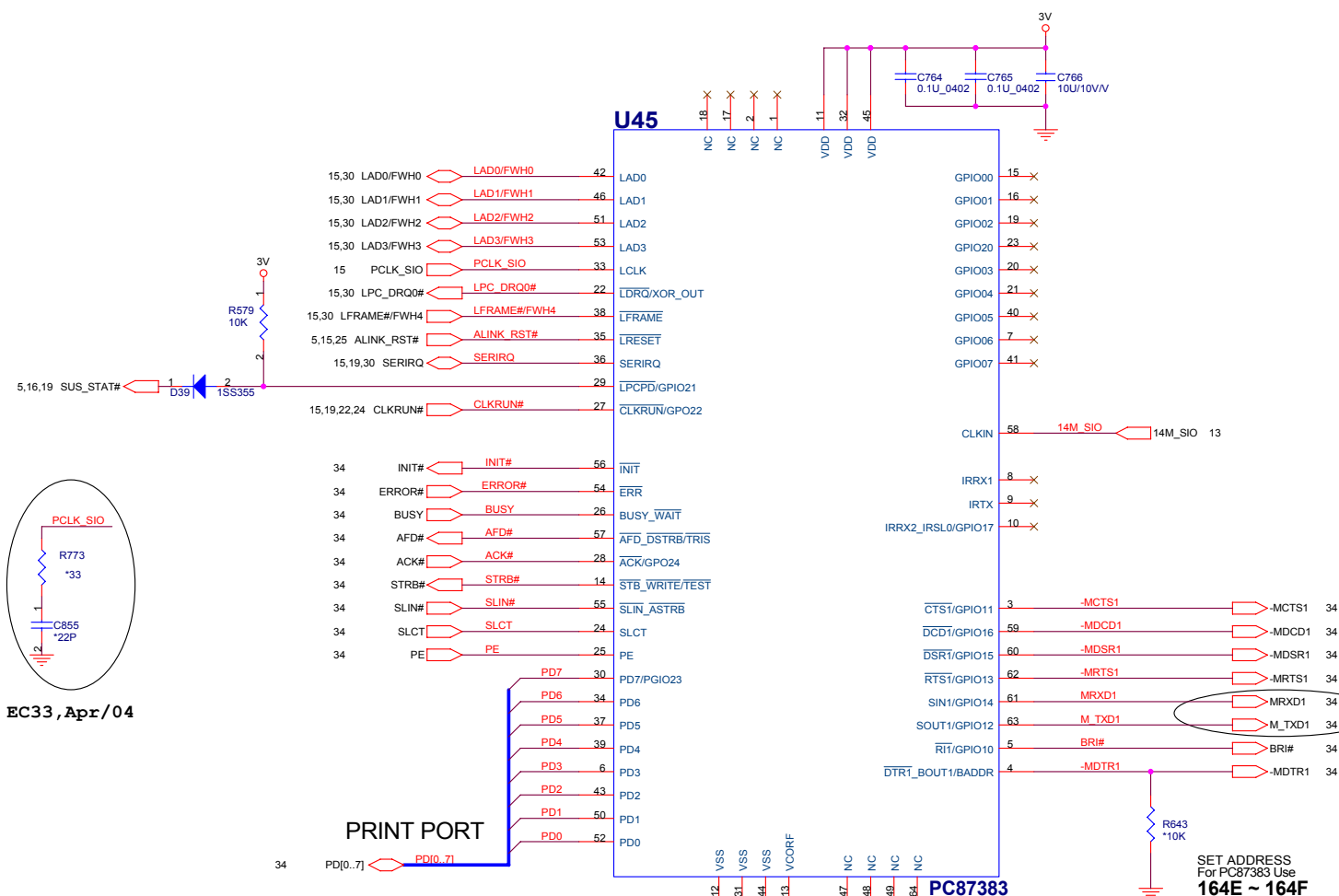
VFAN = 0-3.3V DC or PWM (R272 *)
VFAN = 0-5V DC or PWM (R5 330K)

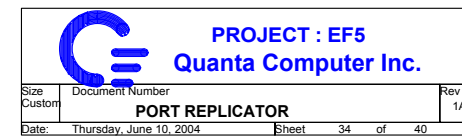
TOUCH PAD CONN.



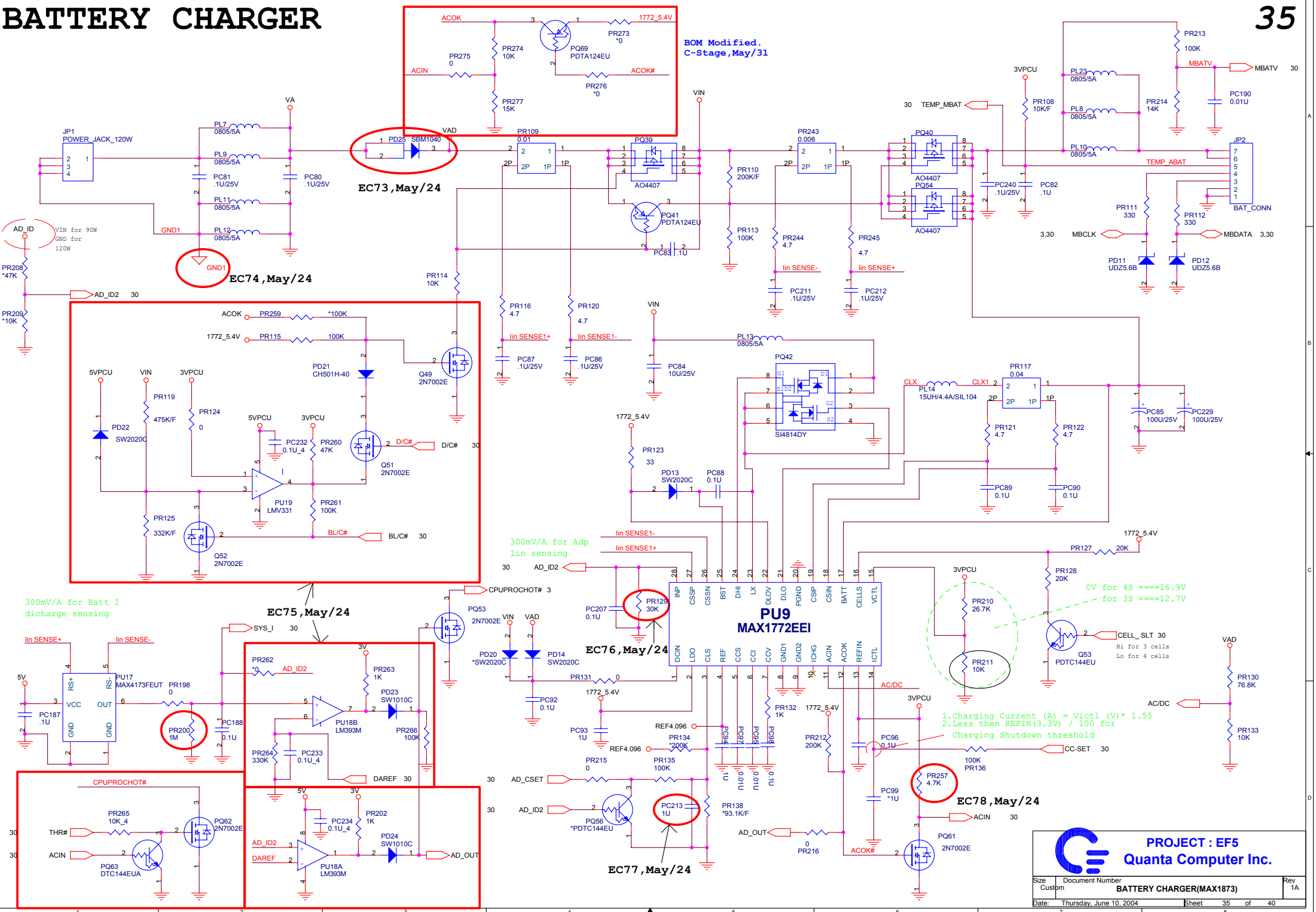
SCREW HOLE



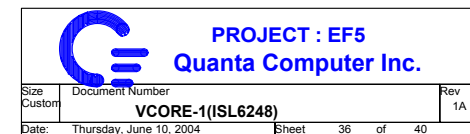
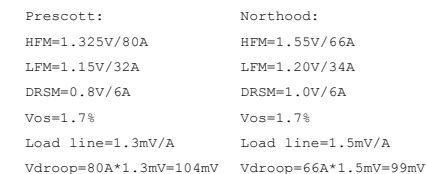


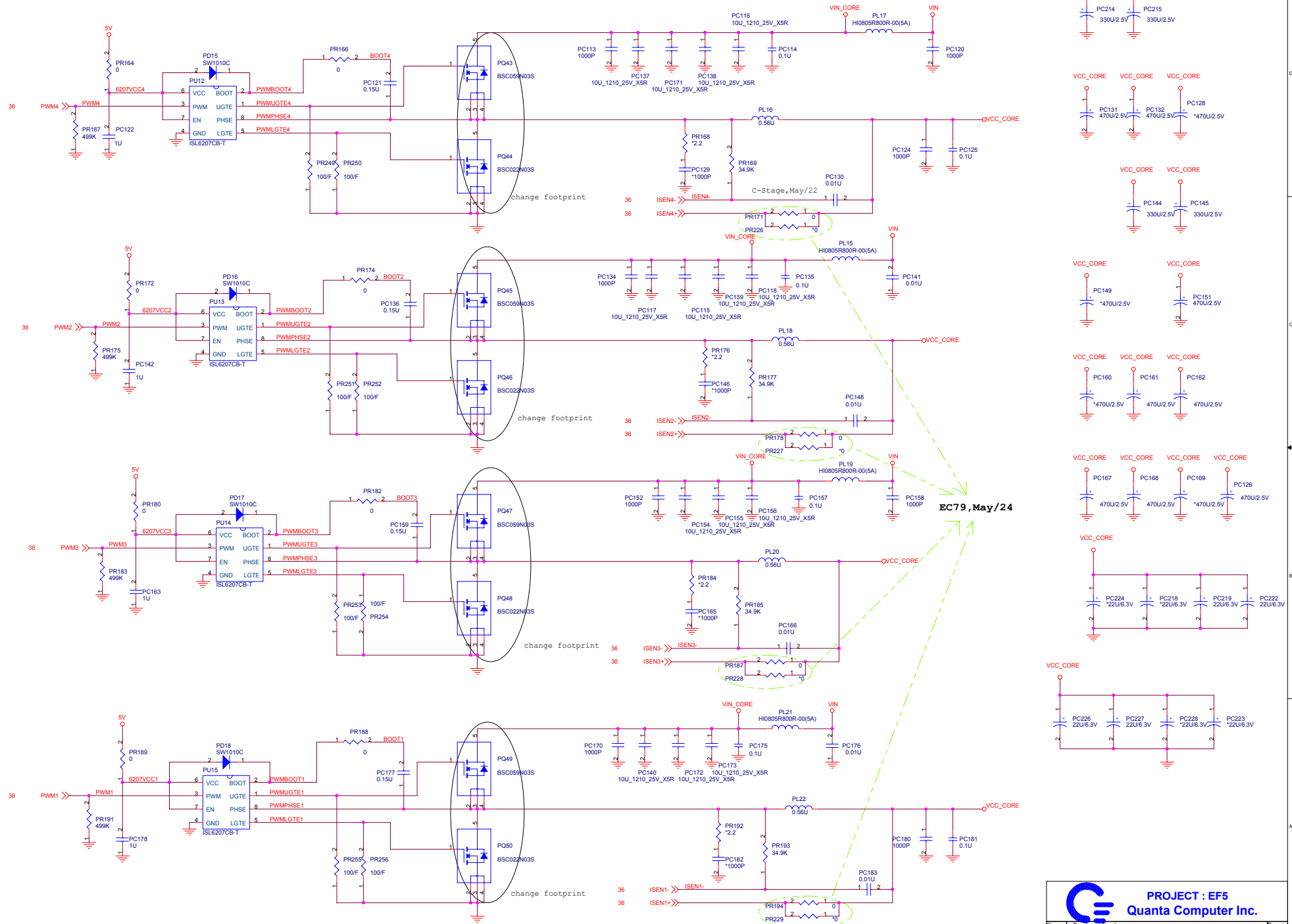


BATTERY CHARGER

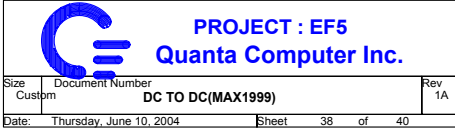


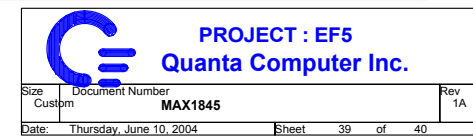
36





38





MODEL	REV	CHANGE LIST			MODEL		
					PAGE	EF5	
						FROM	TO
EF5 Main Board	1A	First Release			01	1A	
	2A	SHEET	EC.		02	1A	
					03	1A	
		P.3	1	EC recommend	04	1A	
			2	Intel recommend	05	1A	
		P.4	3	Intel recommend	06	1A	
			P.8	4	Waveform fine tune for ATi recommend	07	1A
		5		Layout modify for EMI concern.	08	1A	
		P.9	6	ATi recommend	09	1A	
			P.11	7	Layout modify for pin swap - easy routing	10	1A
		8		DDR-Module recognize modify	11	1A	
		P.13	9	ATi recommend	12	1A	
			10	Pin swap for CLK frequency select control	13	1A	
		P.16	11	USB port pull down resistor placement from Port Replicator to system	14	1A	
			12	ATi recommend	15	1A	
		P.18	13	Strapping-pin swap for PMC flash rom used	16	1A	
			14	Added diode to avoid leakage	17	1A	
		P.19	15	Pin define swap	18	1A	
			P.21	16	Delete resistor for double pull up	19	1A
		P.22		17	Separated power well with different analog power pin	20	1A
			18	Reserved for waveform fine tune	21	1A	
		P.24	19	No stuff for BCM4401	22	1A	
			20	Reserved for waveform fine tune	23	1A	
		P.25	21	Added pull up resistor for PME event	24	1A	
			22	Reserved for EMI fine tune	25	1A	
		P.27	23	BOM change for Conexant recommend	26	1A	
			24	Ring function modify	27	1A	
		P.29	25	Quick switch pin control for internal & external speaker out	28	1A	
			26	EMI recommend	29	1A	
		P.30	27	Reserved for waveform fine tune	30	1A	
			28	Package change for layout issue	31	1A	
		P.31	29	Change power well for Quick button wake up event	32	1A	
			30	Power sequence fine tune for ATi recommend	33	1A	
		P.33	31	Added pull up resistor for input pin	34	1A	
			32	Fixed serial port could not transfer data	35	1A	
		P.34	33	Reserved for waveform fine tune	36	1A	
	34		Added spring for EMI	37	1A		
	3A	P.3	35	EMI recommend	38	1A	
			36	CPU throttling support by Battery mode			
		P.4,8,11,13,14,15,19,31,34,36,38	37	Intel recommend			
			38	Reserved for EMI fine tune			
		P.4	39	Intel recommend			
			40	ATi recommend			
		P.5	41	ATi recommend			
			42	Value change for waveform fine tune			
		P.13	43	Added part for Lid switch protect			
			44	Waveform fine tune to meet VESA specification			
		P.14	45	Waveform fine tune to meet VESA specification			

Size Custom

Document Number

Date: Thursday, June 10, 2004

RELEASE NOTE

Rev 1A

PROJECT : EF5

Quanta Computer Inc.

Sheet 40 of 40

MODEL	REV	CHANGE LIST			MODEL		
					PAGE	EF5	
						FROM	TO
EF5 Main Board	3A	SHEET	EC.		01	1A	
		P.15	46	Value change for waveform fine tune	02	1A	
		P.16	47	ATi recommend	03	1A	
		P.16,24	48	Software specification implement	04	1A	
		P.16	49	ATi recommend	05	1A	
		P.17	50	ATi recommend	06	1A	
			51	ATi recommend	07	1A	
		P.18	52	ATi recommend	08	1A	
		P.19	53	Added capacitor for waveform fine tune	09	1A	
			54	Added resistor for PME function	10	1A	
		P.21	55	TI recommend	11	1A	
		P.22	56	Added one capacitor for Broadcom recommend	12	1A	
			57	Added capacitors for Broadcom recommend	13	1A	
			58	Circuit modify for PME function	14	1A	
			59	Added capacitors for Broadcom recommend	15	1A	
			60	Added capacitors for Broadcom recommend	16	1A	
		P.23	61	Pin swap for Broadcom recommend	17	1A	
			62	EMI suggestion	18	1A	
		P.24	63	Added resistor for Wireless Lan indicator	19	1A	
		P.25	64	Fine tune the IDE reset waveform	20	1A	
		P.27,29	65	Fixed Wake On Ring function	21	1A	
			66	Fine tune the Audio quality	22	1A	
		P.29	67	Layout package modify	23	1A	
			68	Fine tune the trigger level	24	1A	
		P.30	69	Power saving control for Battery only mode	25	1A	
		P.30,32	70	Power well modify and pin swap	26	1A	
		P.32	71	Modify for EMI & ESD issue	27	1A	
		P.33	72	Added spring for SMT issue	28	1A	
		P.34,35	73	Added diode to avoid spark while insert P.R.	29	1A	
			74	EMI suggestion	30	1A	
		P.35	75	Battery learning and power throttling	31	1A	
			76	Bom error	32	1A	
			77	Added capacitors for input current limit	33	1A	
			78	Value change for ACIN detect	34	1A	
		P.36	79	Modify feedback sense current	35	1A	
			80	Modify CPU OCP	36	1A	
			81	Modify compesation	37	1A	
			82	Fine tune Prescott CPU load line	38	1A	
			83	Fine tune Northwood CPU load line	39	1A	
	P.38	84	Modify 3V/5V OCP				
	P.39	85	Fine tune power sequence				
	86	Fine tune power sequence					
	87	Modify 2.5V OCP					
	88	Fine tune power sequence					



PROJECT : EF5
Quanta Computer Inc.

Size	Document Number	Rev
Custpm	RELEASE NOTE	1A
Date: Thursday, June 10, 2004	Sheet 41 of 41	