

First International Computer, Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : AMD S1 + Nvidia C51D + MCP51

Version : 0.6 (PTB51)

Initial Date : 05/13/2006

Confidential

Manager Sign by : Avery Lee

Drawing by : Jason Lee

Total confirm by : Adam Cho

		First International Computer, Inc. SFL NO.300, Yang Guang St., Neihu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751	
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Size: C	Document Number: TITLE		Rev: 0.6
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1. Schematic Page Description :

FIC Schematic Ver : 0.1

1. Title

2. Schematic Page Description

3. Block Diagram

4. ANNOTATIONS

5. Schematic History

6. AMD S1 HT(1/3)

7. AMD S1 DDR(2/3)

8. AMD S1 POWER(3/3)

9. CPU Thermal/Fan CNN

10. C51D_HT (1/3)

11. C51D_PCIE (2/3)

12. C51D_POWER(3/3)

13. DDRII SO-DIMM 0 RSV

14. DDRII SO-DIMM 1 STD

15. MCP51 HT(1/6)

16. MCP51 PCI(E)/LPC (2/6)

17. MCP51 SATA/PATA(3/6)

18. MCP51 AC97/USB(4/6)

19. MCP51 RGMII(5/6)

20. MCP51 POWER(6/6)
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22. G7X VIDEO_1

23. G7X VIDEO_2

24. G7X MEM CHANNEL

25. VGA DDR2_A CHANNEL

26. VGA DDR2_C CHANNEL

27. DVI Port

28. LCD CNN

29. TV Port

30. 1394 VIA VT6311S

31. Cardreader AU6366

32. New Card(express card)

33. PCIE Mini Card

34. GIGA PHY 88E1116

35. GIGA TRANSFORMER

36. FirmWare Hub

37. USB CNN

38. LED / SW

39. RTC/ BLUETOOTH CNN

40. SATA HD / CD-ROM CNN
41. Azalia ALC883GR- Codec

42. AMP (G1432&G1410)/AD CN

43. SPDIF HP/MIC JACK

44. MDC / Audio CNN

45. KBC / GP CNN

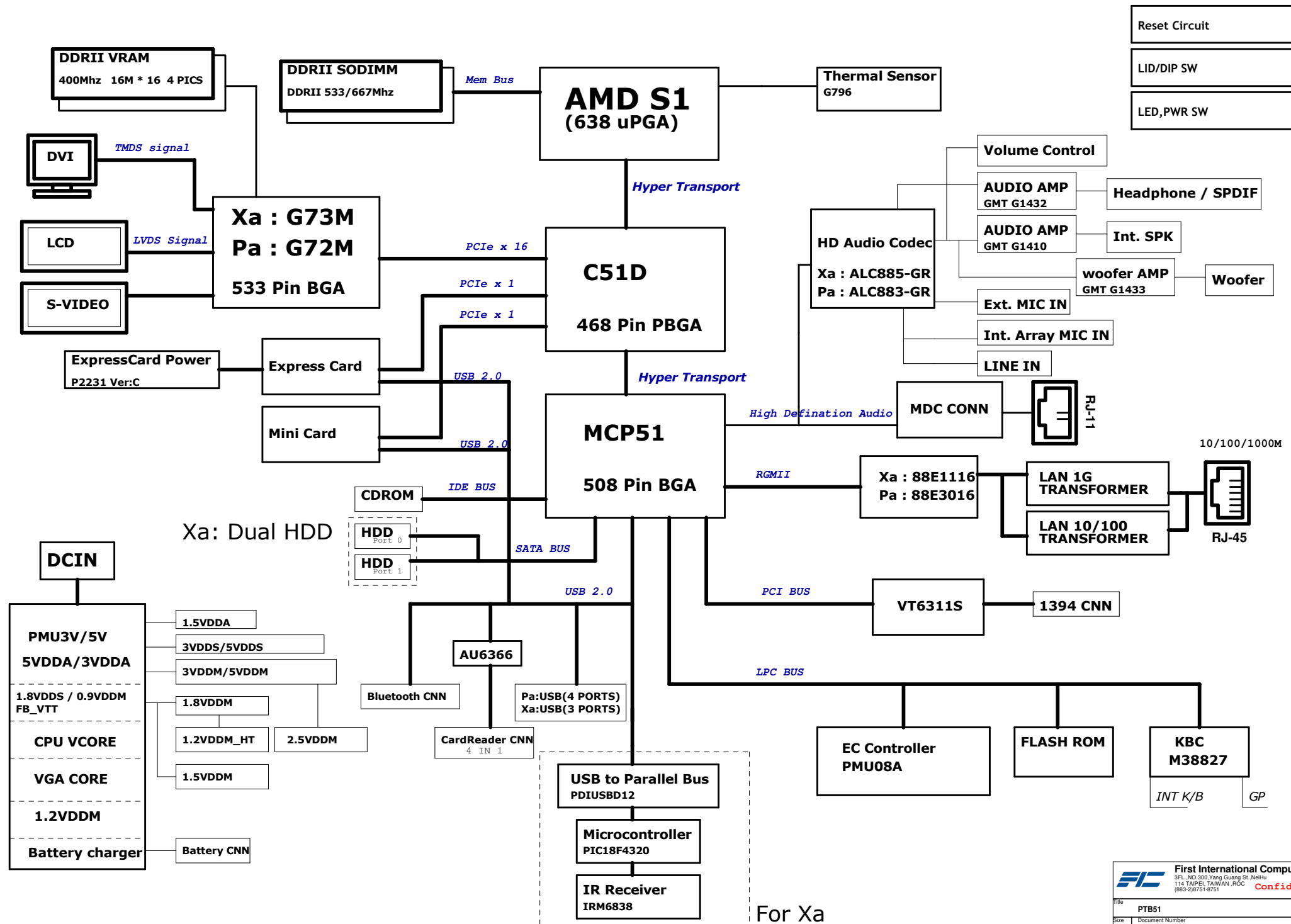
46. DIP/LID SW; SCREW

2. PCI BUS Description :

IDSEL	CHIP
AD22	1394 VIA VT6311S

PCIINT	CHIP
IRQA	1394 VIA VT6311S
IRQB	—
IRQC	—
IRQD	—

BUSMASTER	
REQ	CHIP
REQ0 / GNT0	—
REQ1 / GNT1	1394 VIA VT6311S
REQ2 / GNT2	—
REQ3 / GNT3	—
REQ4 / GNT4	—



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
1.5VDDA	1.5V always on power rail by DCON or PSUSC0
5VDDS	5.0V power rail
3VDDS	3.3V power rail
1.8VDDS	1.8V power rail
FB_VTT	0.9V power rail for VGA
0.9VDDM	0.9V DDR Termination Voltage
5VDDM	5.0V suspend power rail
3VDDM	3.3V suspend power rail
2.5VDDM	2.5V suspend power rail
1.5VDDM	1.5V suspend power rail
VDD_CORE	Core Voltage for VGA
VCPU_CORE	Core Voltage for CPU
1.2VDDM	VCC For CPU & NB
+1.2VHT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

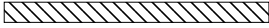
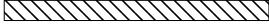
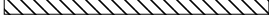
0	=	Active Low signal
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Signal Conditioning

D	=	Damped (by a resistor)
Q	=	Isolated (by a Q-switch)
L	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1/Mixer
Layer 4		GND
Layer 5		VCC
Layer 6		IN2/Mixer
Layer 7		GND
Layer 8		BOTTOM

6.Schematic modify Item and History :

V0.1 --> V0.2

- 1.Modify LED circuit for Pa and Xa co-layout.
- 2.Change Card Reader from AU6333 to AU6366.
- 3.R38,R41 change to 56k ohm,C670 change to2200pF,C658 change to 1500pF,Del R385,Add C47 0.1uF (tune power sequence)
- 4.CLK_PMU08 change connect point from R451 to R592
- 5.Add D51,R589 47k ohm (Solve HTMCP_RST# Glitch)
- 6.Revise CN21 Analog connection.
- 7.Change Q11 from 06-20726-01 to 06-23930-01
- 8.Add 0.1uF between U5 pin1,pin2 ,Remove D14.
- 9.Change Headphone AMP from M441 to G1410
- 10.R236 change to NU

V0.2 --> V0.3

- 1.Change JP1, JP2, JP3, JP9, JP15, JP19, JP23 to 0 ohm 11-14214-00
- 2.Change C16, C17 from 10-40729-02 to 10-60092-01
- 3.Add C883 10-52810-02 on Vcpu_core plane
- 4.L77, L79 changed from 12-01986-01 to 12-01955-01
- 5.C686 changed from NU to stuff.
- 6.CPU VDDIO_FB_L change to NC (FSC recommend)
- 7.Add PCIE CLK serial 0 hm resistor R603,R604,R605,R606,R607,R608 (FSC recommend)
- 8.C647,C652 change from 18pf to 27pf, C630,C633 change from 12pf to 18pf(tune crystal timing)
- 9.D13,R201,C379,R205 change to NU,R205 stuff, Add R600 10k ohm pull down (solve KBC issue)
- 10.For EMI solution
 - Add R272,R273,R274,R275,R276,R277,R278,R279 22 ohm
 - Add C870,C871,C872,C873,C874,C875,C876,C877,C6,C5,C518,C520 5pF
 - Add C551,C548,C546,C880,C881 10pF
 - Add C878,C568,C569 100pF,C571 150pF, C480 1000pF
 - Del L41,L42, Add R238,R239,R385,R521 10ohm

V0.3 --> V0.4

- 1.Del R571, Change R572 from 910 to 1K, change D17 to one lens LED for behavior issue.
- 2.Del Q65, Change Q70 to P-MOS (06-20593-01) for behavior issue.
- 3.Add C884, C885, C886, C887 location but no stuff to prevent noise issue.
- 4.Del JP7, JP18, JP25, JP13, JP24, JP11, JP10, JP8, JP12, JP14, JP29, JP4, JP22, JP6, JP21, JP5, JP17 to short.
- 5.C45(47pF), C55(33pF) change to 150pF, R31 change from 12k to 18k.
- 6.Add R613 between R531 to GND.
- 7.C1, C2, C535, C597 from NU to stuff .
- 8.Change L81, L82 to 0 ohm, add C891, C892, C893 for L1 enable function.
- 9.Add Card control power solution
- 10.R375 0 ohm change to NU, R595 10K ohm stuff
- 11.Add Lan PHY power control circuit.
- 12.Modify RF LED circuit.
- 13.Modify DVI circuit.
- 14.Modify Audio Mute circuit.
- 15.For EMI solution
 - Add C494 200pF
 - Add R189 0 ohm
 - Add C898,C899,C900,C901,C902,C903,C904,C905 5pF (NU)
 - Add one spring
 - Add R258,R329,R436 0 ohm (NU)
- 16.R337 2K ohm change to NU, R335 10K ohm stuff
- 17.U58 change to NU, R550 4.7K ohm stuff
- 18.L55, L56 change to 300 bead, C523,C526 change to NU(Modify for Microvision issue)
- 19.R264 change from220 ohm to 82 ohm, R573 change from220 ohm to 470 ohm.

V0.4 --> V0.5

- 1.Add R620, R621 0 ohm (NU)
- 2.Add R622 for EMI solution
- 3.Del R451, C707

PTB50V0.5 --> XTB70V0.1

- 1.Add internal MIC OP-AMP circuit
- 2.Del L39,L40,C778,C755
- 3.JP15 change to 0 ohm short
- 4.C15 stuff
- 5.For EMI solution
 - C5, C6 change to 33pF
 - R272,R273,R276,R277,R278,R279 change to 18nH
 - R274,R275 change to 15nH
 - R258,R329,R622 0 ohm stuff
 - C551 change to 220pF

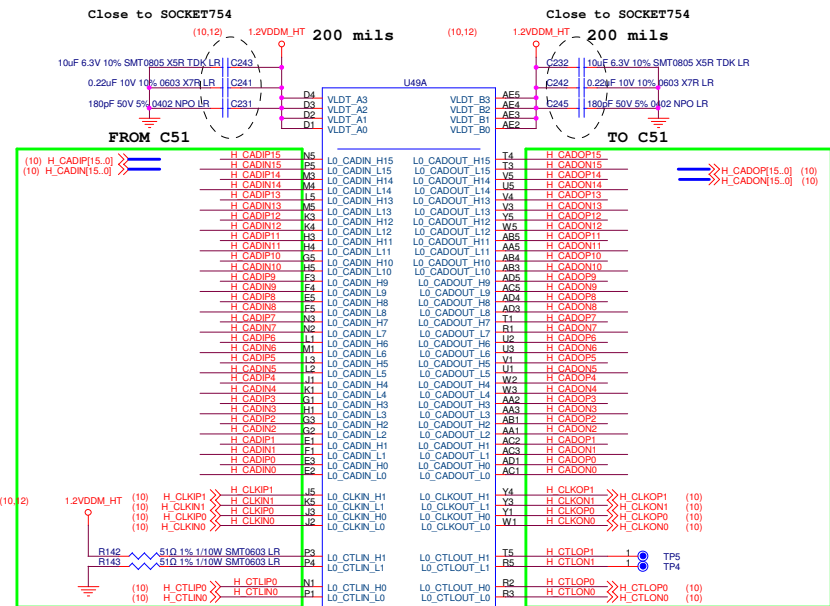
V0.1 --> V0.2

- 1.Modify USB port power from 5VDDM to 5VDDA

XTB70 V0.2 --> PTB50V0.6

- 1.Change USB power: 5VDDM to 5VDDA
- 2.Change KBC power: from M power plane to A power plane
- 3.Modift Bluetooth circuit.
 - R457 change to 1K ohm
 - U31.1 change 3VDDA

ClawHammer HT Interface



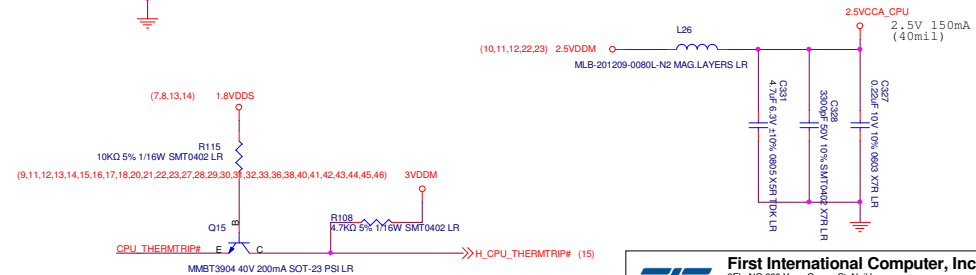
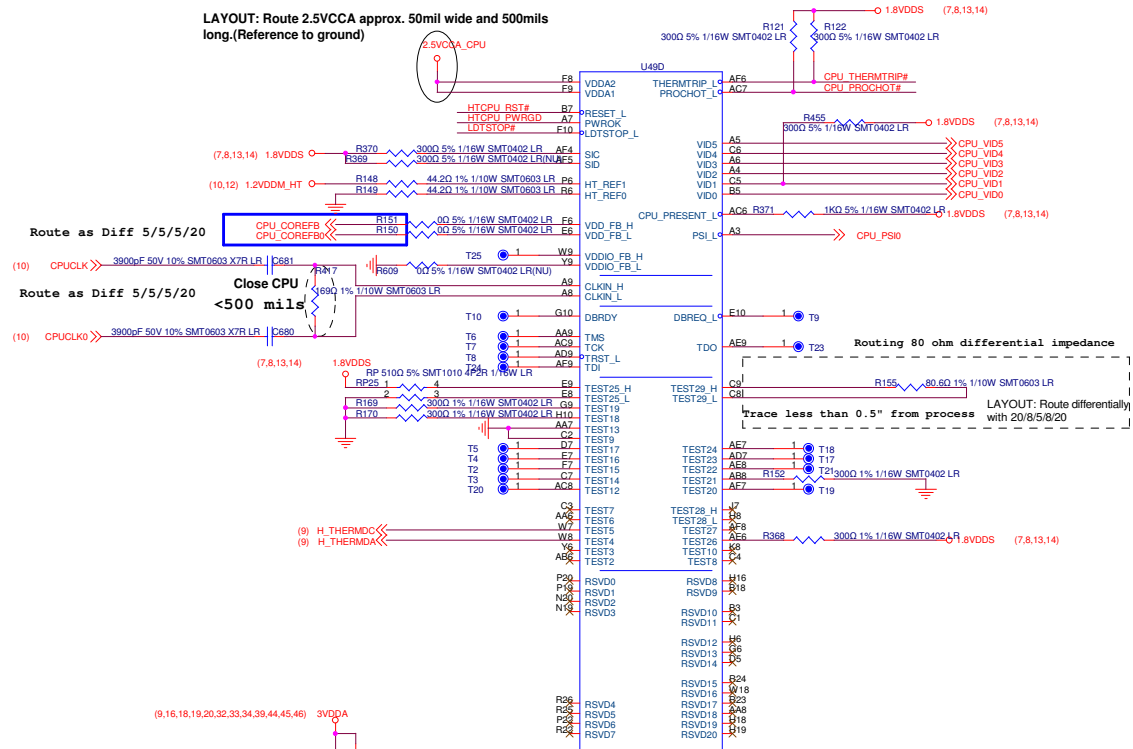
HT BUS General Routing Rules:

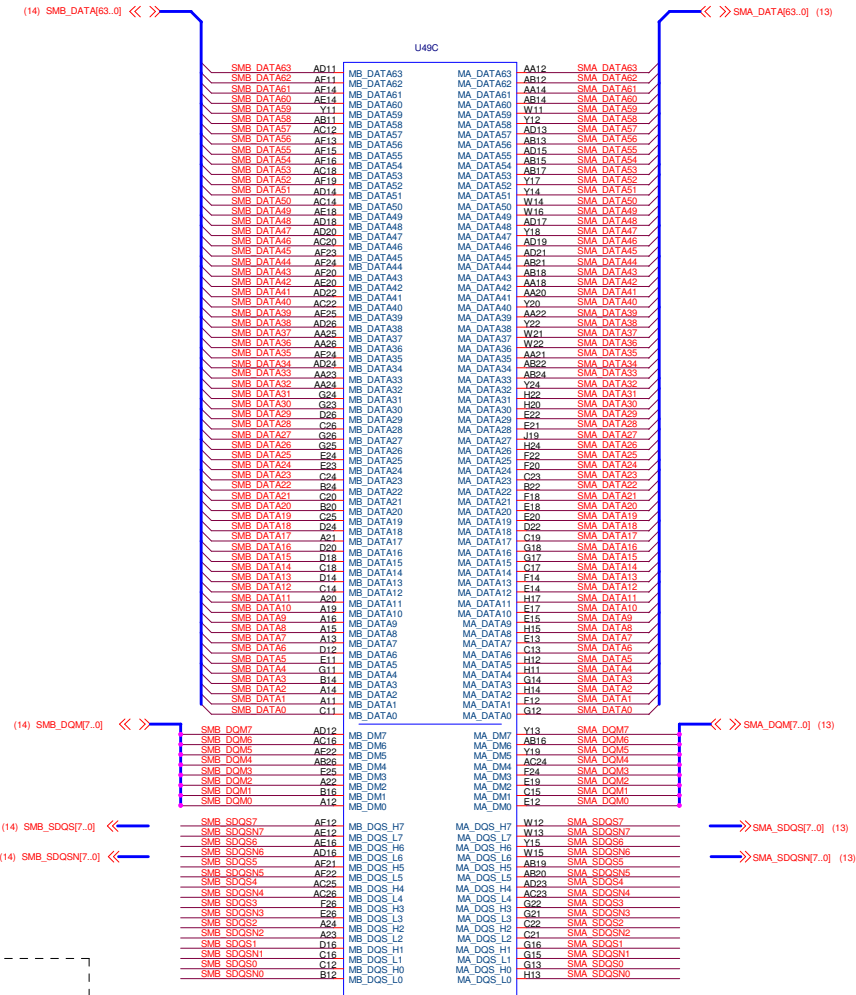
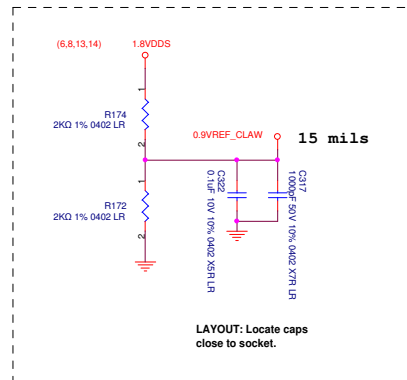
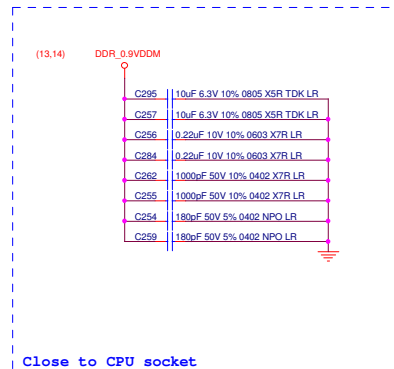
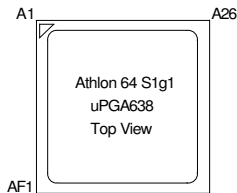
1. HT BUS is easy to route, and uses minimal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max) .
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.

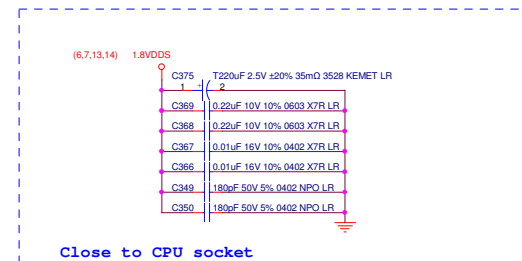
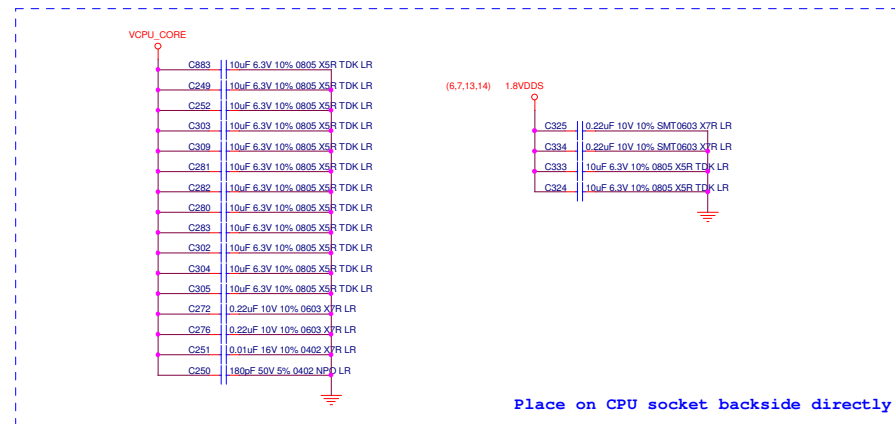
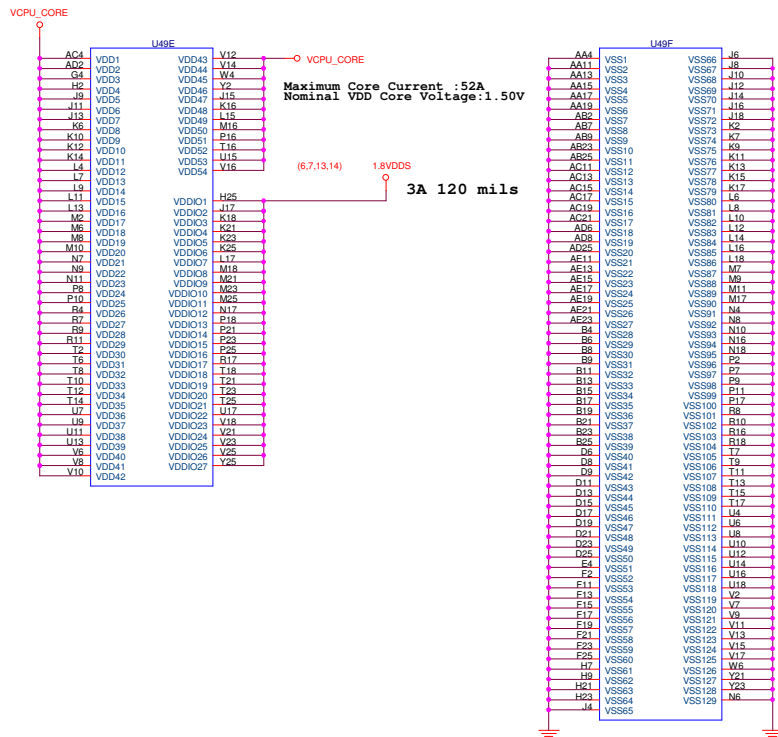
The figure illustrates four types of signal processing scenarios, each showing a signal path and its associated delays. The scenarios are labeled as follows:

- Top-left:** SIGNAL input, WSPAC=15mil, resulting in CADDIN_H (5mil) and CADDIN_L (5mil).
- Top-right:** SIGNAL input, WSPAC=15mil, resulting in CADDOUT_H (5mil) and CADDOUT_L (5mil).
- Bottom-left:** SIGNAL input, WSPAC=15mil, resulting in H_CLKIP/H_CTLIP (5mil) and H_CLKIN/H_CTLIN (5mil).
- Bottom-right:** SIGNAL input, WSPAC=15mil, resulting in H_CLKOP/H_CTLOP (5mil) and H_CLKON/H_CTLON (5mil).

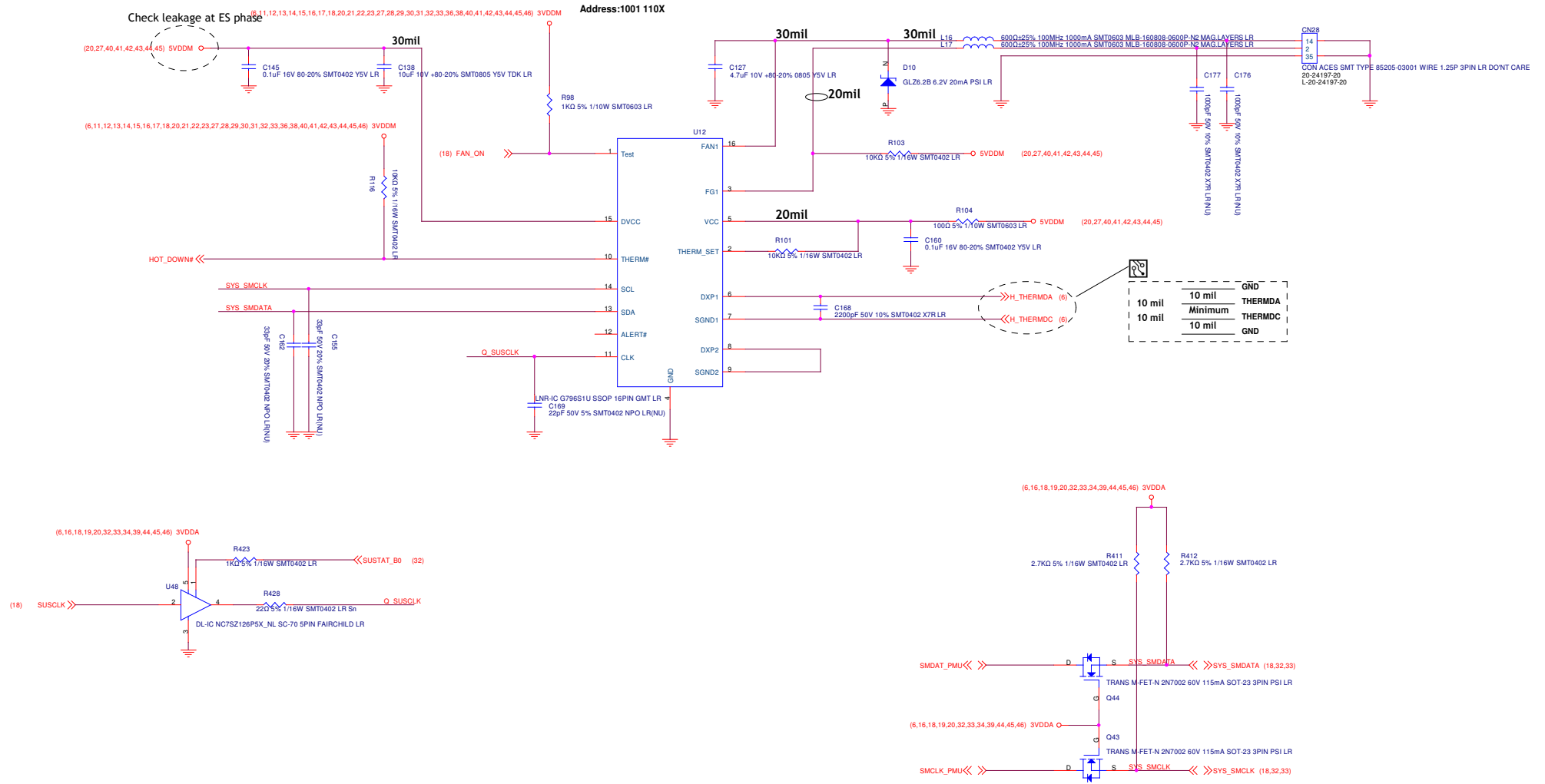
LAYOUT: Route 2.5VCCA approx. 50mil wide and 500mils long.(Reference to ground)

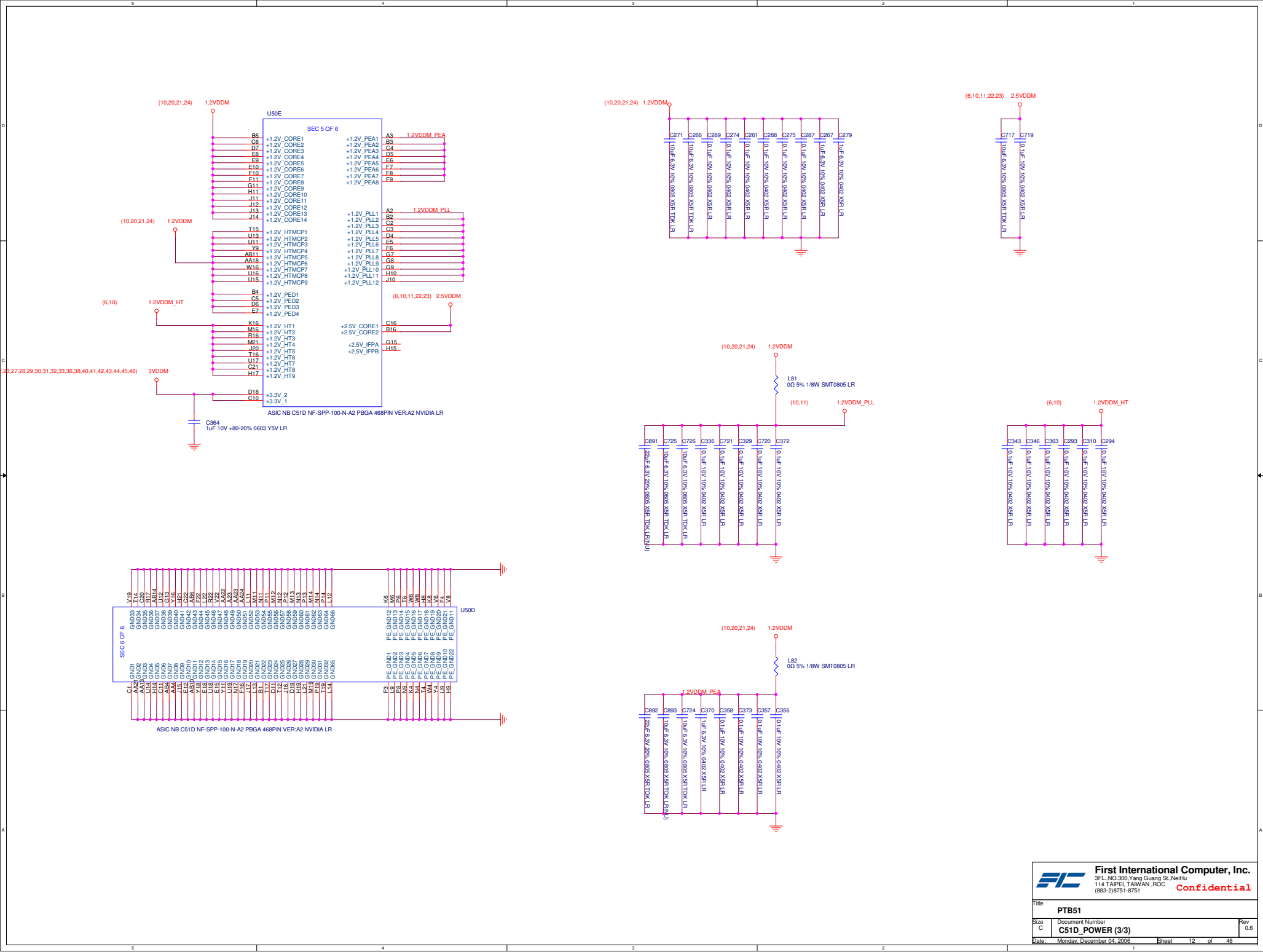


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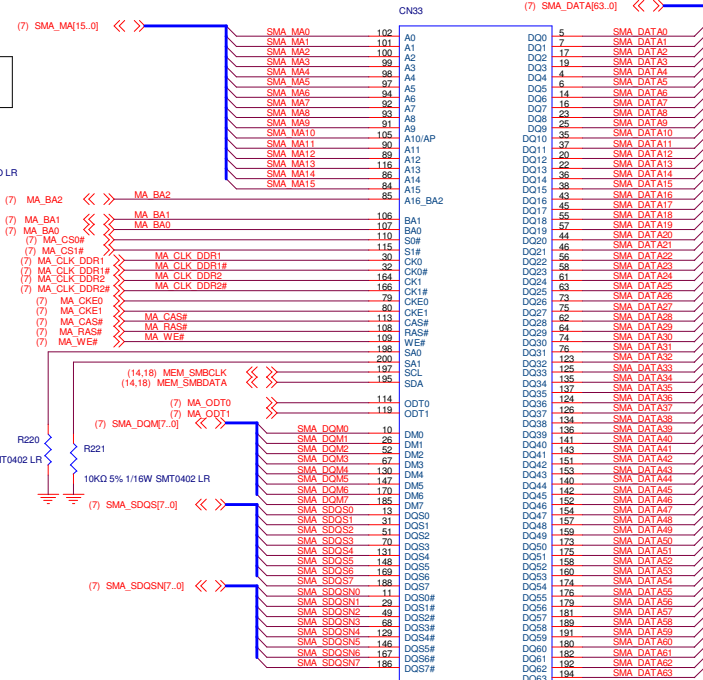
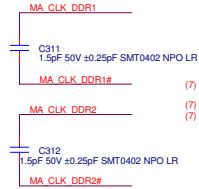


THERMAL SENSOR





PLACE CLOSE TO CPU
WITHIN 1.5 INCH



SO DIMM 0

REV TYPE

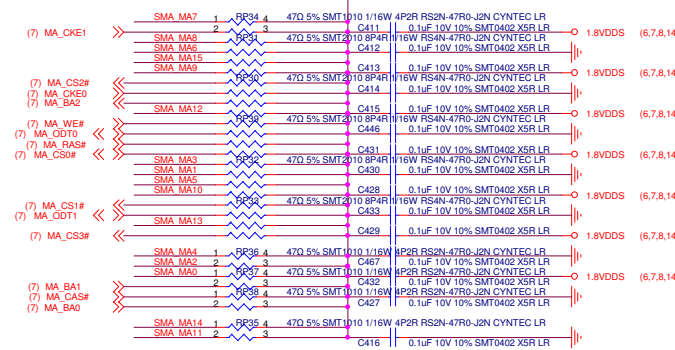
SOCKET FOXCONN SMT DDR2 SO-DIMM H-5.2 REV A50A421-N2RN-4F LR

LAYOUT GUIDE

Place one cap close to every 2 pullup resistors terminated to 0.9vddm

400 mils

DDR_0.9VDDM (7,14)



Place these resistors near So-Dimm1

(6,9,14) 1.8VDDM

120mil

Place these 2.2uF caps near So-Dimm1

Place these 0.1uF caps near So-Dimm1

Place these Hi-Freq decoupling caps near GMCH

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

Place these 0.01uF caps around VDDIO plane

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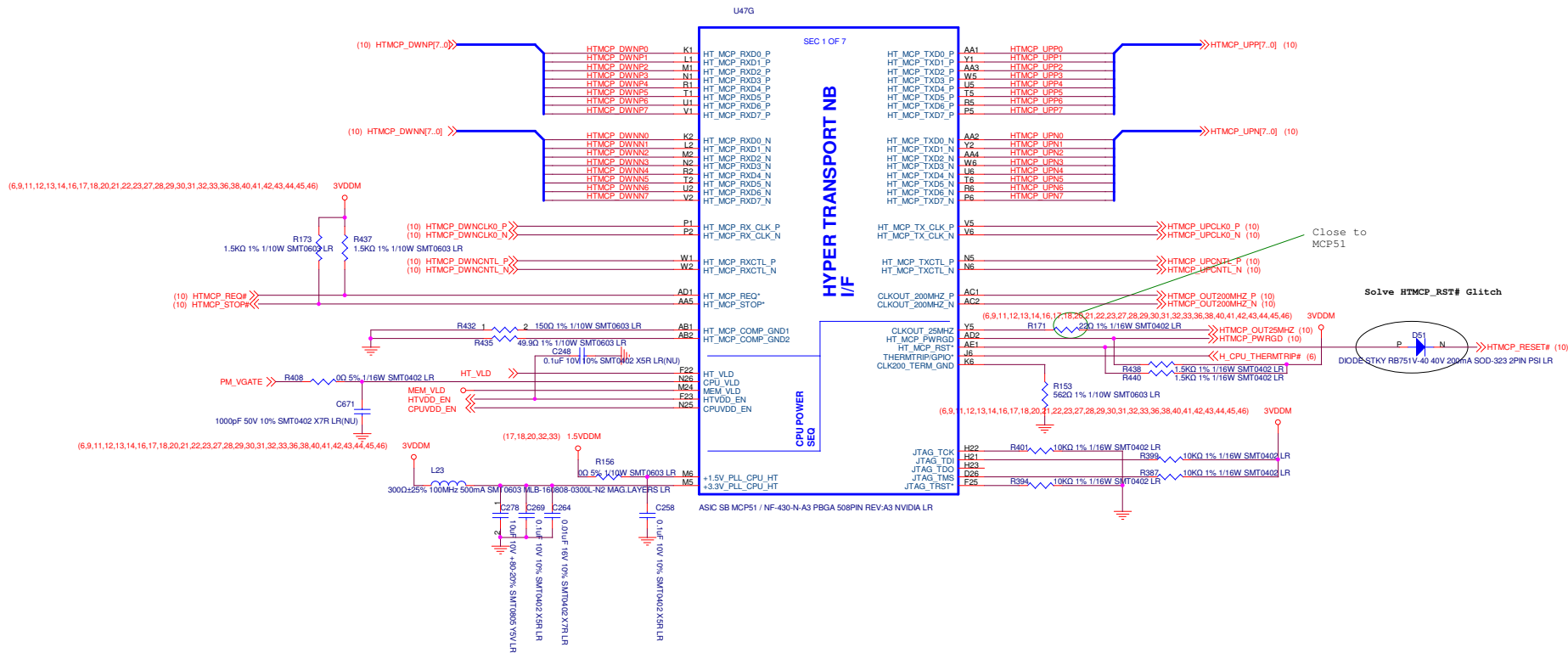
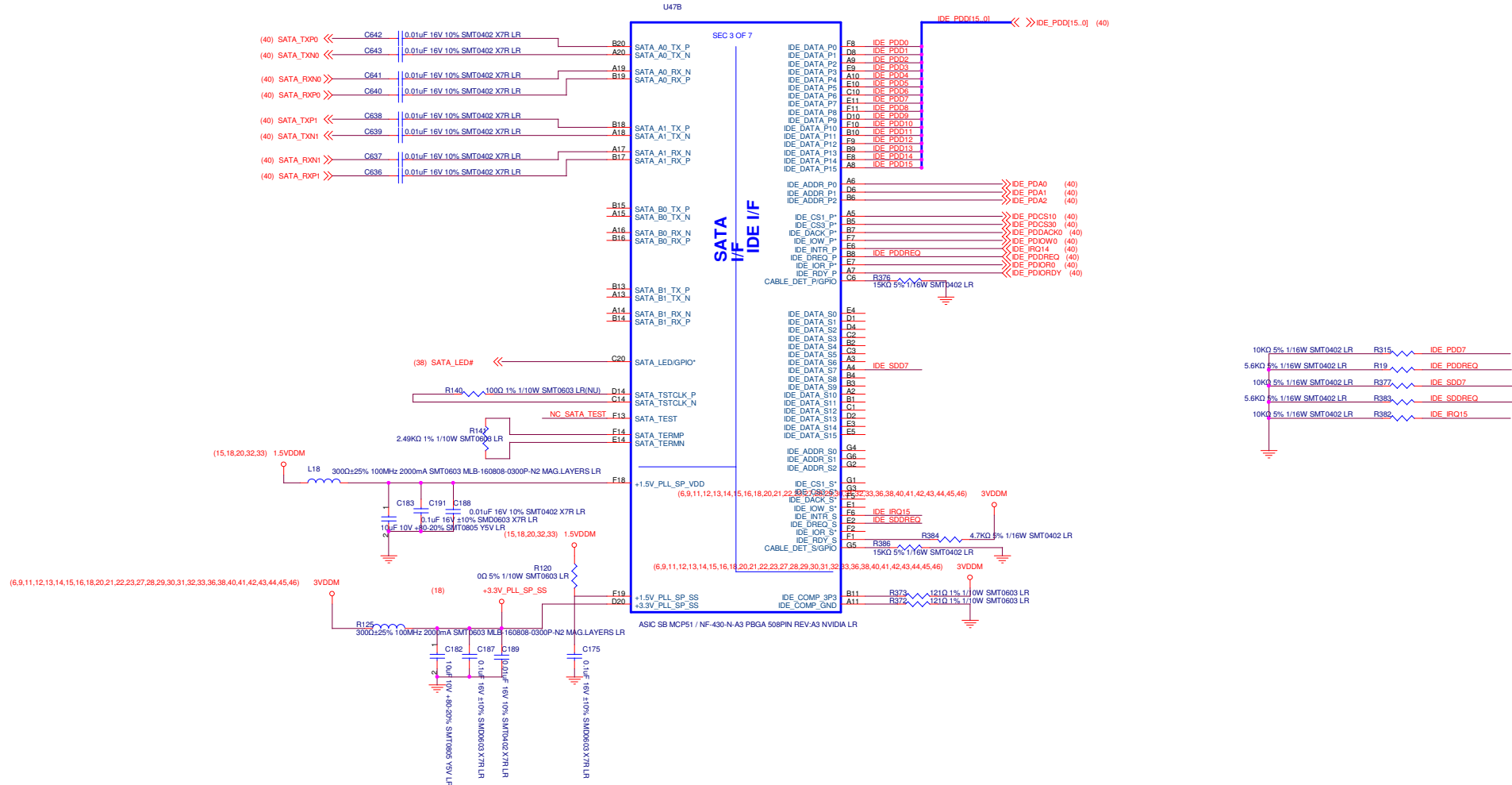
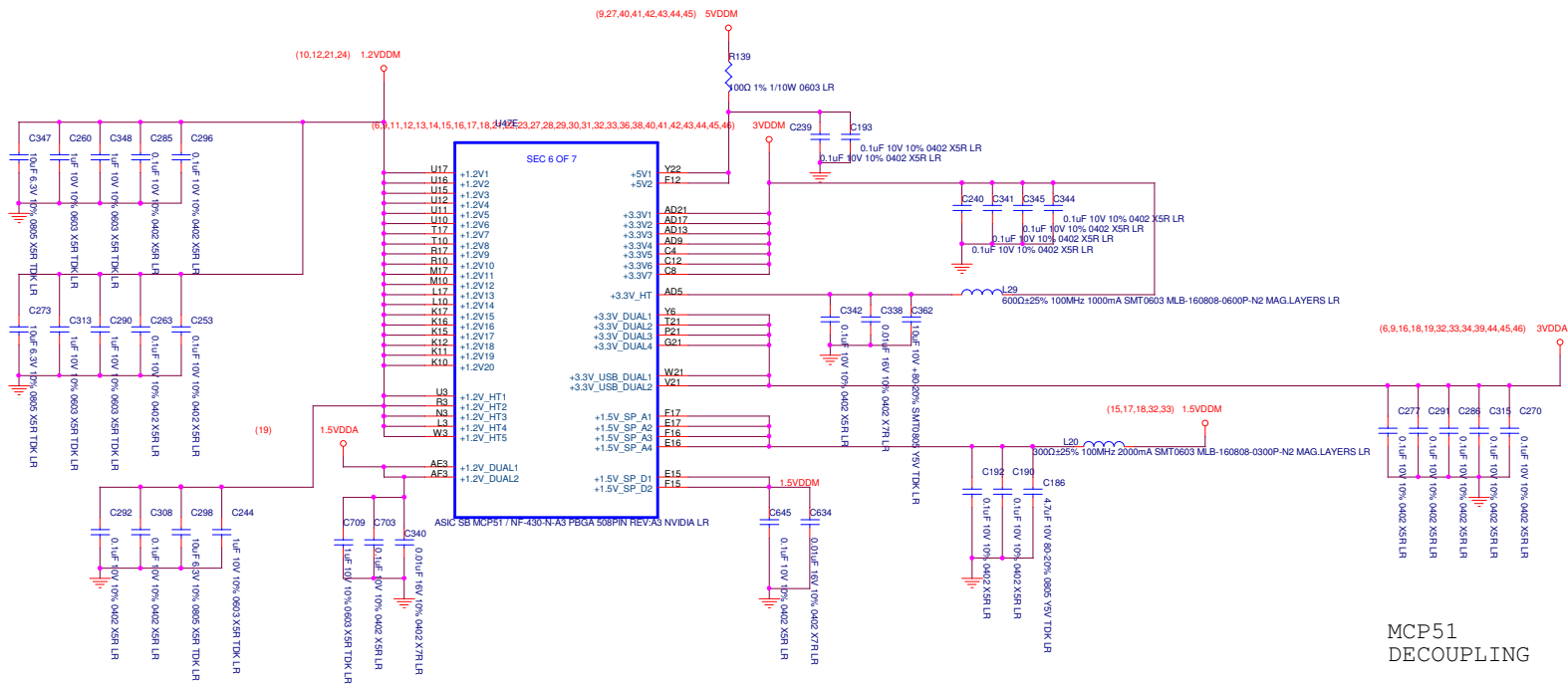
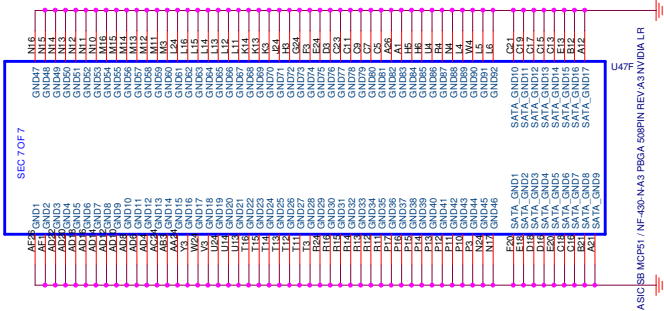


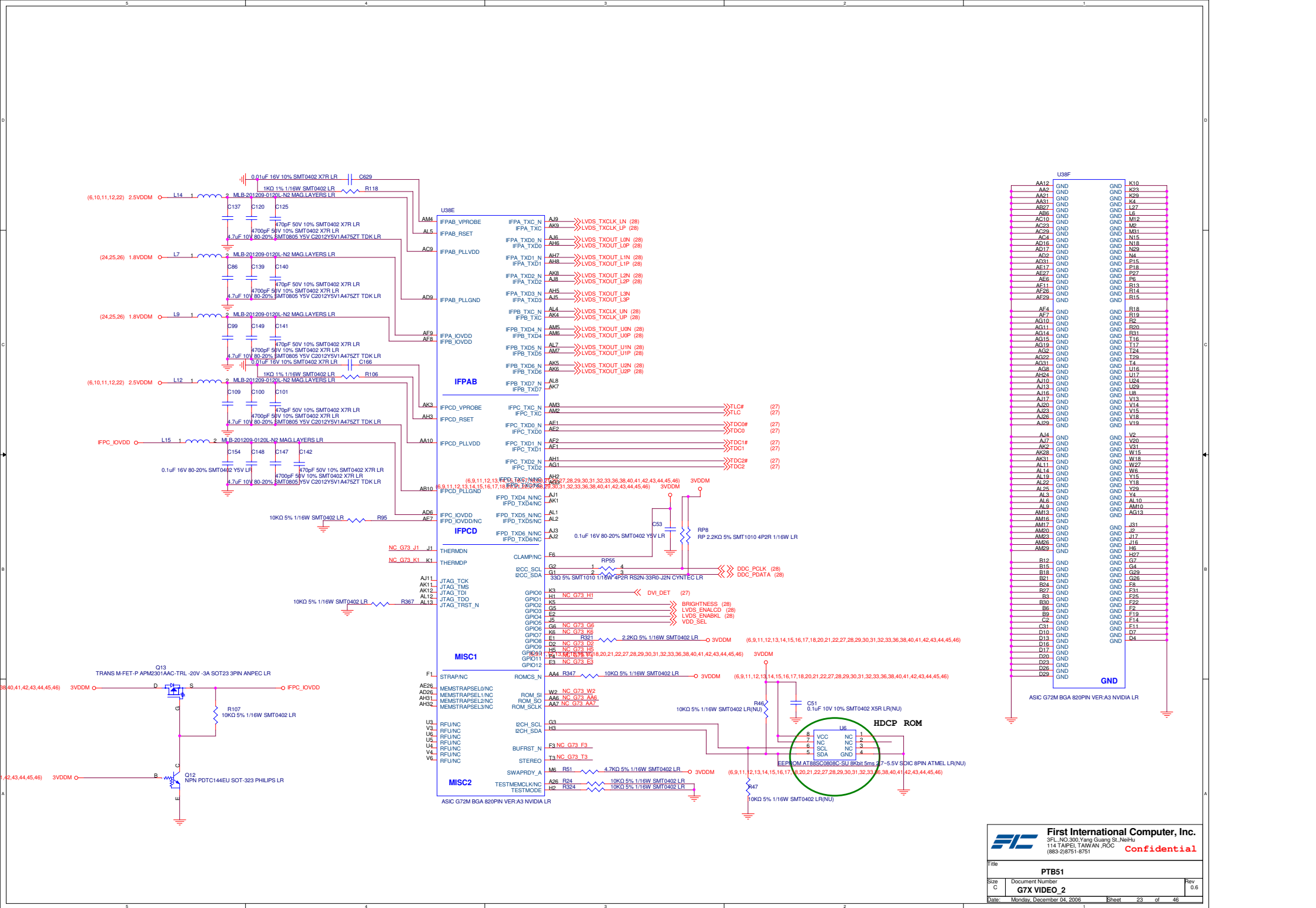


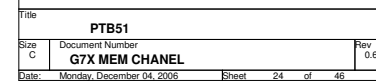
Diagram illustrating the connections for the PCI Express interface components:

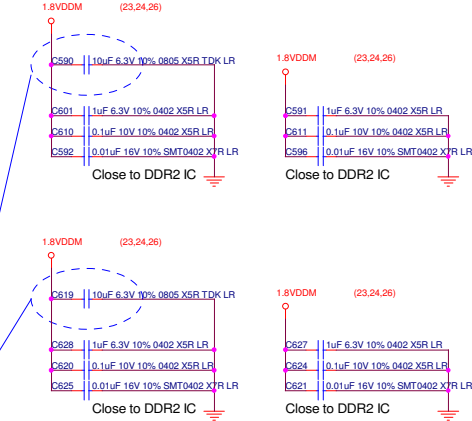
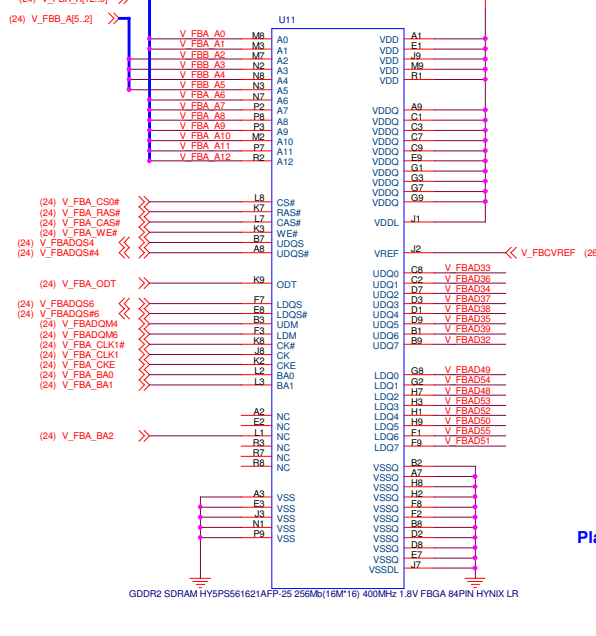
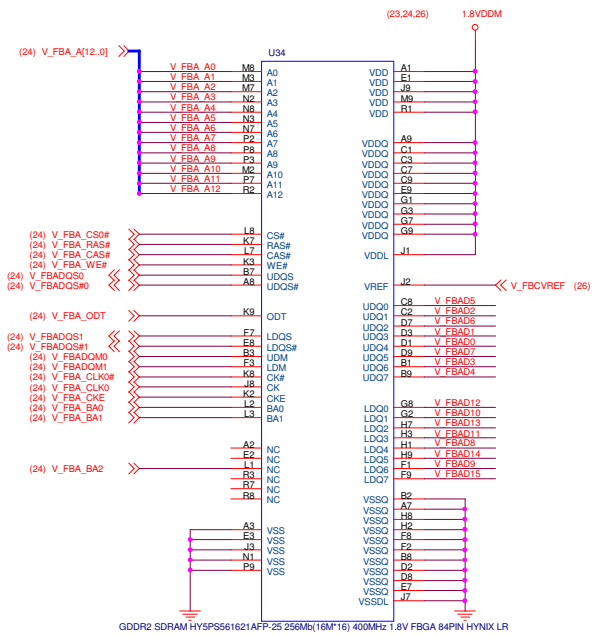
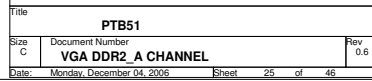
- RP75** (8.2K 5% SMT2010 1/16W 8P4R LR) is connected to:
 - 1 to PCI_REQ04
 - 2 to PCI_FRAME0 (30)
 - 3 to PCI_TRDVO (30)
 - 4 to PCI_TRDYO (30)
- RP76** (8.2K 5% SMT2010 1/16W 8P4R LR) is connected to:
 - 1 to PCI_SERR0 (30)
 - 2 to PCI_DEVSEL0 (30)
 - 3 to PCI_STOP0 (30)
 - 4 to PCI_PERR0 (30)
- R452** (8.2K 5% 1/16W SMT0402 LR) is connected to:
 - PCI_CLKRUN# (45)
- R58** (10K 1% 1/16W SMT0402 LR) is connected to:
 - PCI_SERRIQ (45)
- RP27** (8.2K 5% SMT2010 1/16W 8P4R LR) is connected to:
 - 1 to PCI_IRQA0 (30)
 - 2 to PCI_IRQB0 (30)
 - 3 to PCI_IRQC0 (30)
 - 4 to PCI_IRQD0 (30)
- RP69** (8.2K 5% SMT2010 1/16W 8P4R LR) is connected to:
 - 1 to PCI_REQ02 (30)
 - 2 to PCI_REQ01 (30)
 - 3 to PCI_REQ03 (30)
 - 4 to PCI_REQ00 (30)
- R471** (8.2K 1% 1/10W SMT0603 LR (NU)) is connected to:
 - PCI_GNT00





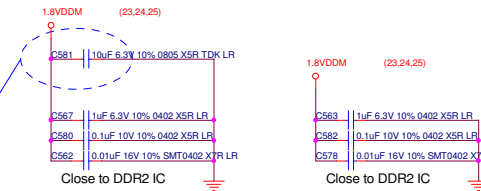
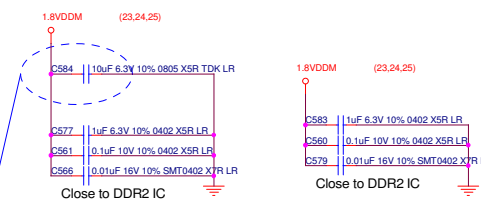
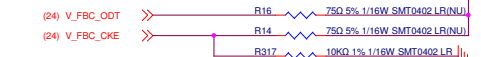
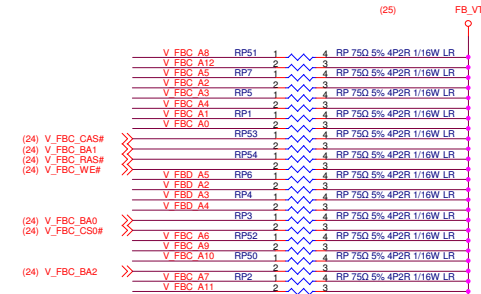
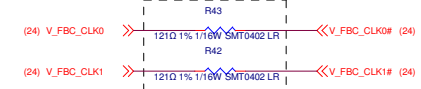






Pa: No Stuff
Xa: Stuff

G72M : 120 ohm
G73M : 470 ohm (11-13130-00)



Placed between two VRAM

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CRT CIRCUIT

USE 47 ohms@100MHZ
BLM18BB470SN1 (MURATA)

20 mil	Other Signal
20 mil	MXM_RED
20 mil	MXM_GREEN
20 mil	MXM_BLUE
20 mil	Other Signal

(22) RED
(22) GREEN
(22) BLUE

WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms

(10mil)

(10mil)

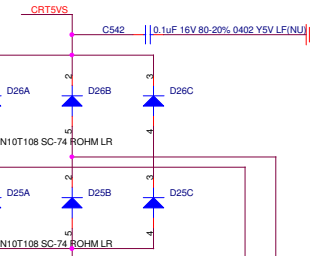
WIDTH=4 MILS Z0=55 ohms

WIDTH=4 MILS Z0=55 ohms

For EMI

(6,8,11,12,13,14,15,16,17,18,20,21,22,23,28,29,30,31,32,33,36,38,40,41,42,43,44,45,46)

For EMI



WIDTH= 8 MILS Z0=75 ohms
WIDTH= 8 MILS Z0=75 ohms
WIDTH= 8 MILS Z0=75 ohms

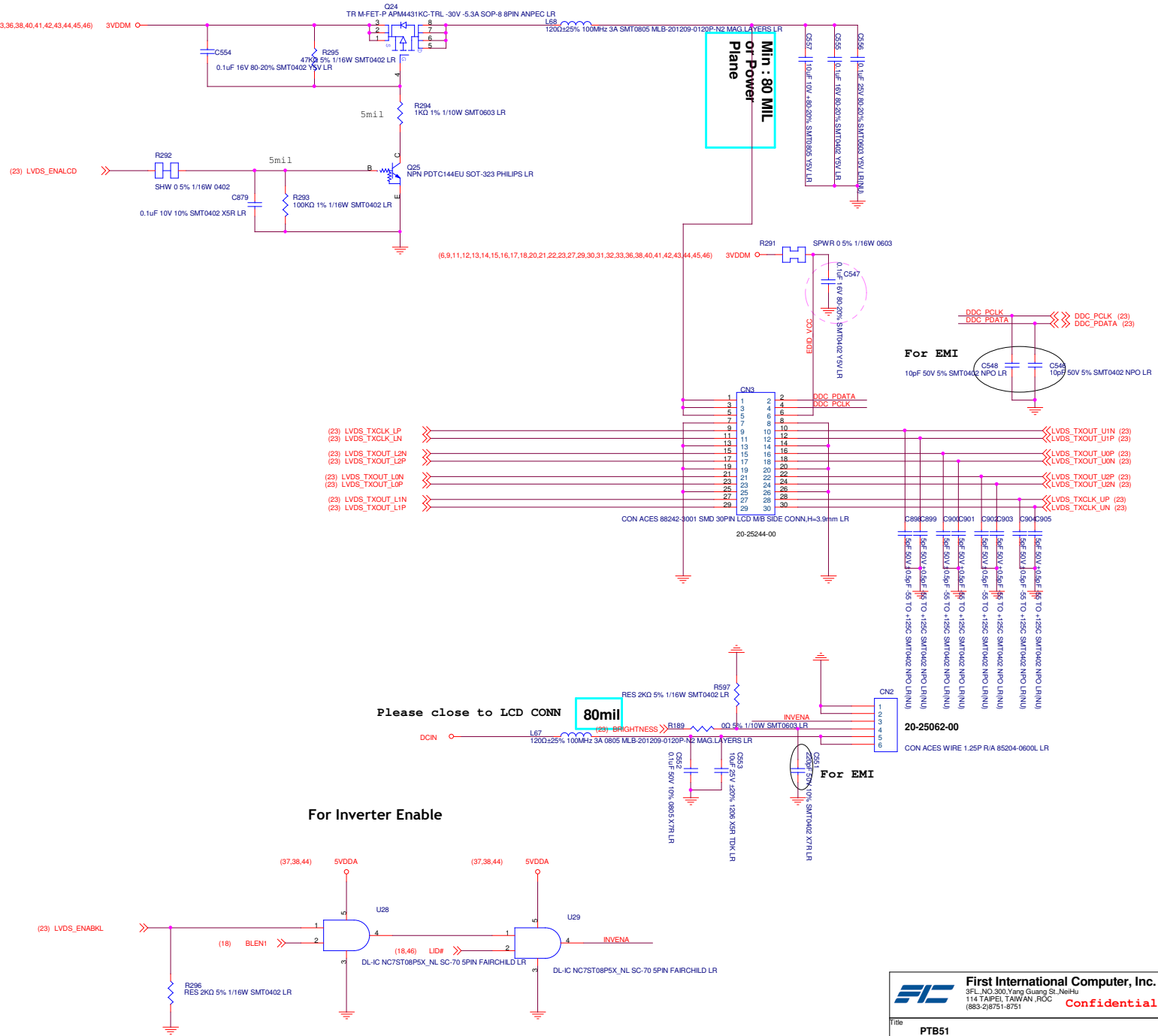
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26	CASE
1	CASE#M3
2	TMDS Data2-
3	TMDS Data2+
4	TMDS Data2# Shield
5	TMDS Data4-
6	TMDS Data4+
7	DDC Clock
8	DDC Data
9	Analog VSYNC
10	TMDS Data1-
11	TMDS Data1+
12	TMDS Data1# Shield
13	TMDS Data3-
14	TMDS Data3+
15	+5V Power
16	GND (for +5V)
17	Hot Plug Detect
18	TMDS Data0-
19	TMDS Data0+
20	TMDS Data0# Shield
21	TMDS Data5-
22	TMDS Data5+
23	TMDS Clock Shield
24	TMDS Clock-
25	TMDS Clock+
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HSYNC
C5	Analog GND
C6	Analog GND/C6
C7	CASE#M4
C8	CASE#M2

06/25
MODIFY

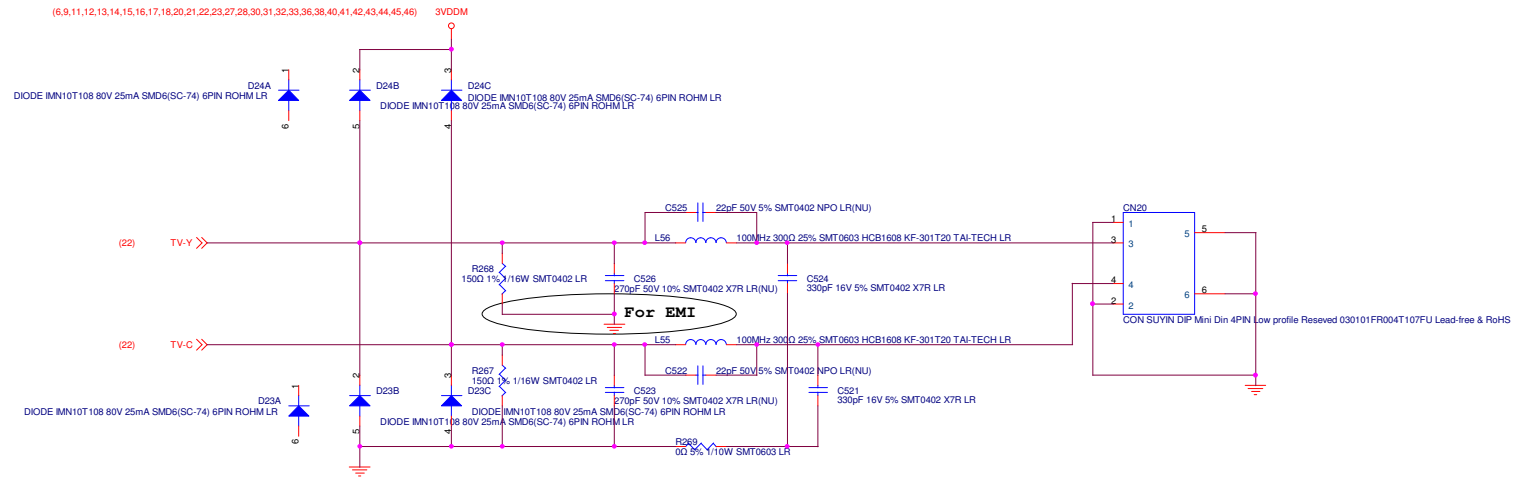
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C	DVI Port	0.6	
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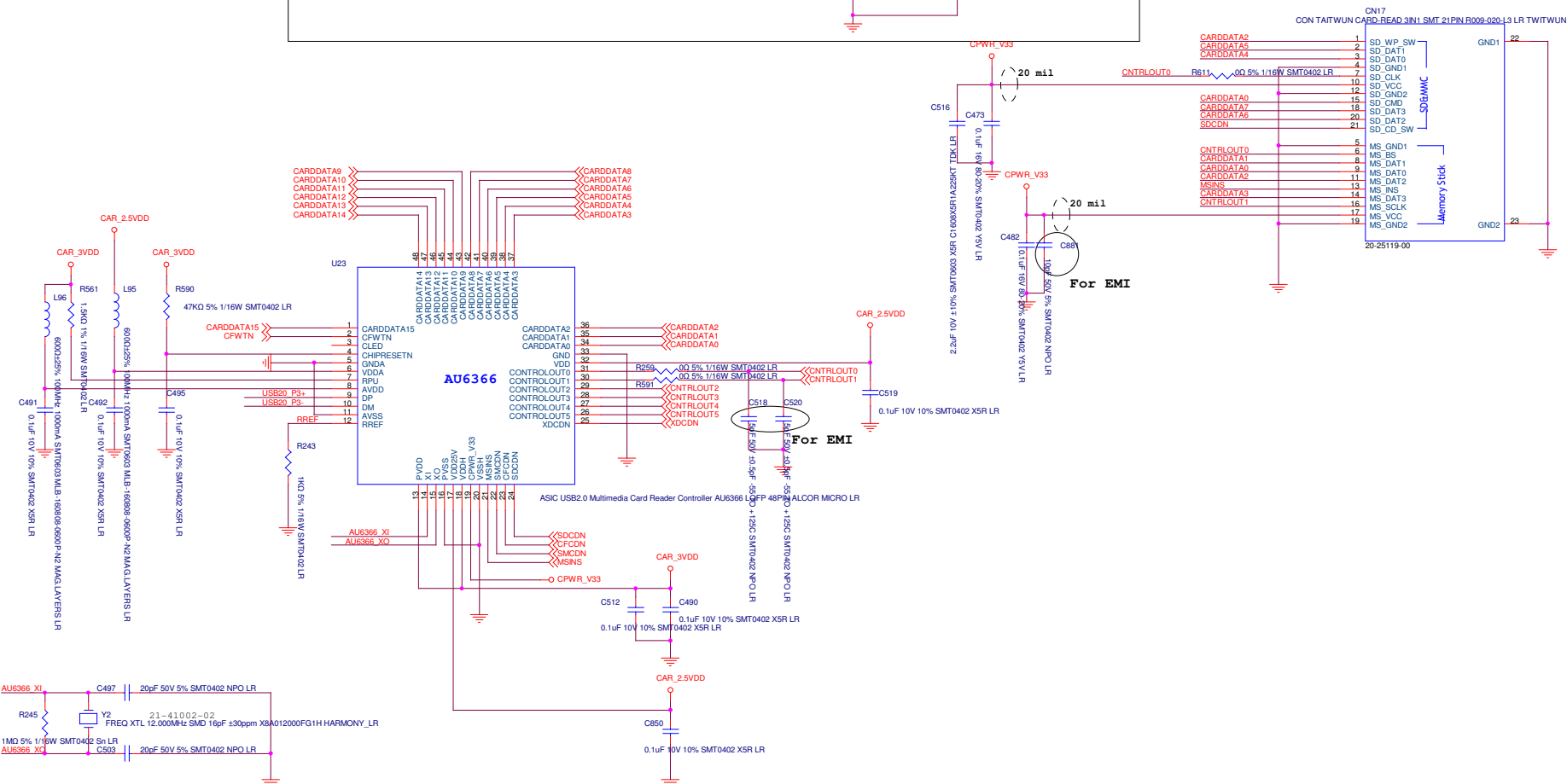
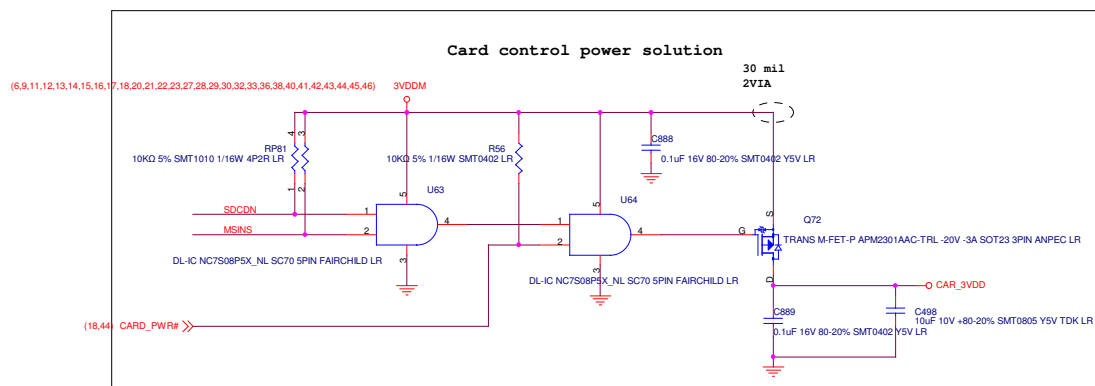
(6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,29,30,31,32,33,36,38,40,41,42,43,44,45,46)
 ICC_MAX=2A
 PATTERN
 WIDTH=MIN.
 2MM(80MIL)



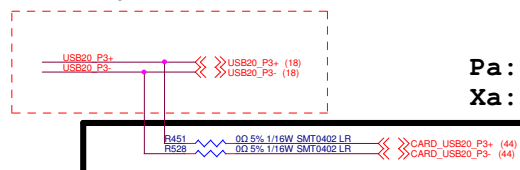
TV OUT CIRCUIT




```
Pa: Stuff
Xa: No Stuff
```

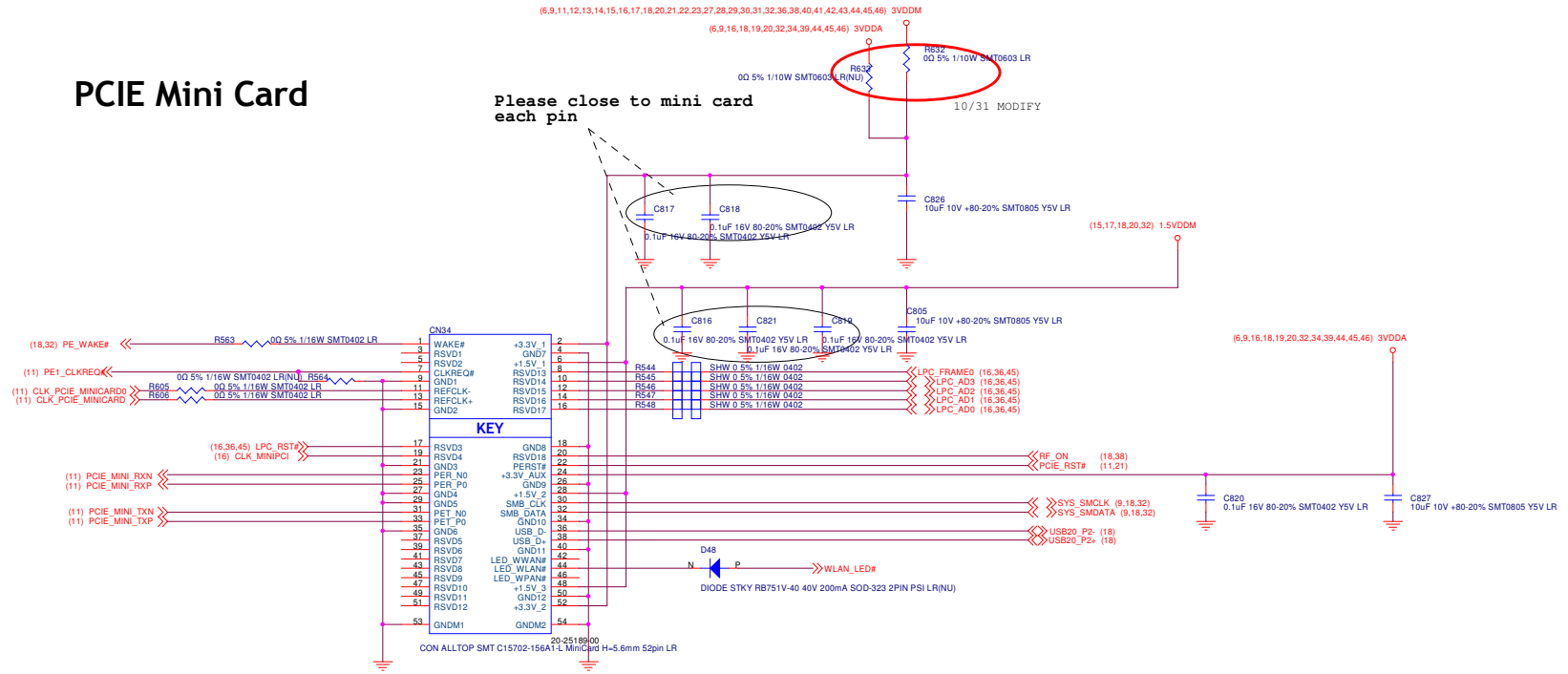


INTERFACE

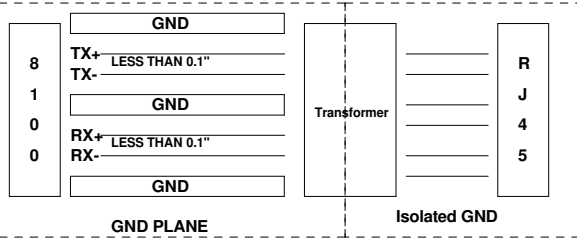


```
Pa: No Stuff
Xa: Stuff
```

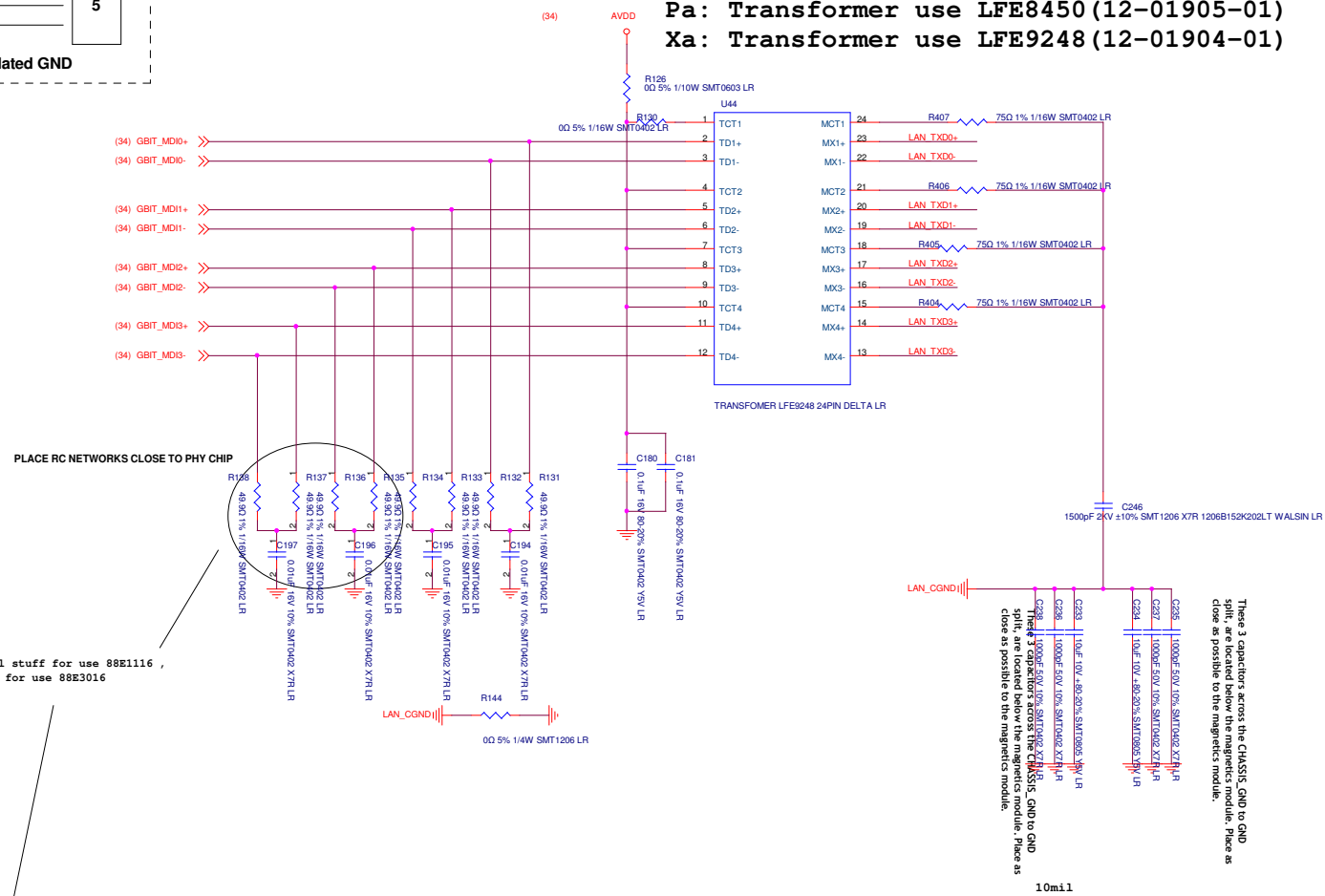

PCIE Mini Card



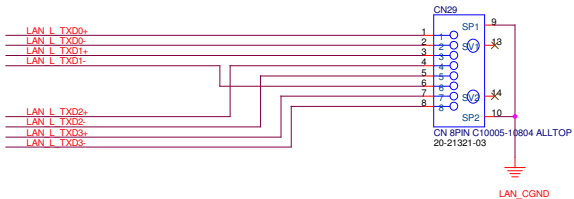
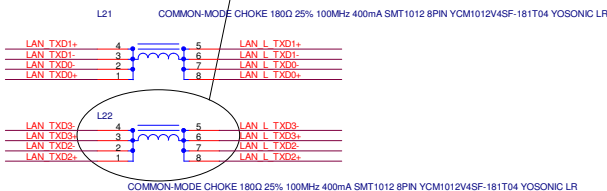
TX 100 ohm ----> trace 4 mil , space 10 mil
RX 50 mil space from other signals
Total Trace Length no more thans 4.8"
2 Differential pairs must have the same length



Pa: Transformer use LFE8450 (12-01905-01)
Xa: Transformer use LFE9248 (12-01904-01)



All stuff for use 88E1116 ,
NU for use 88E3016



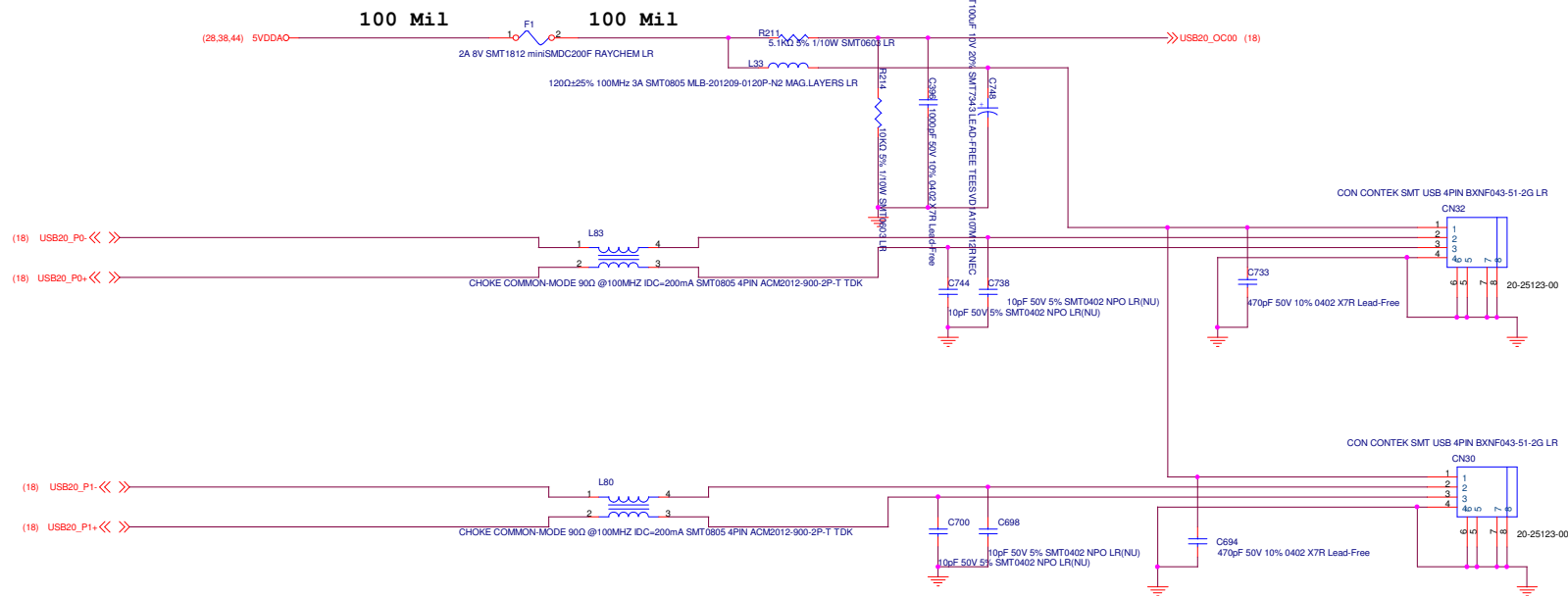
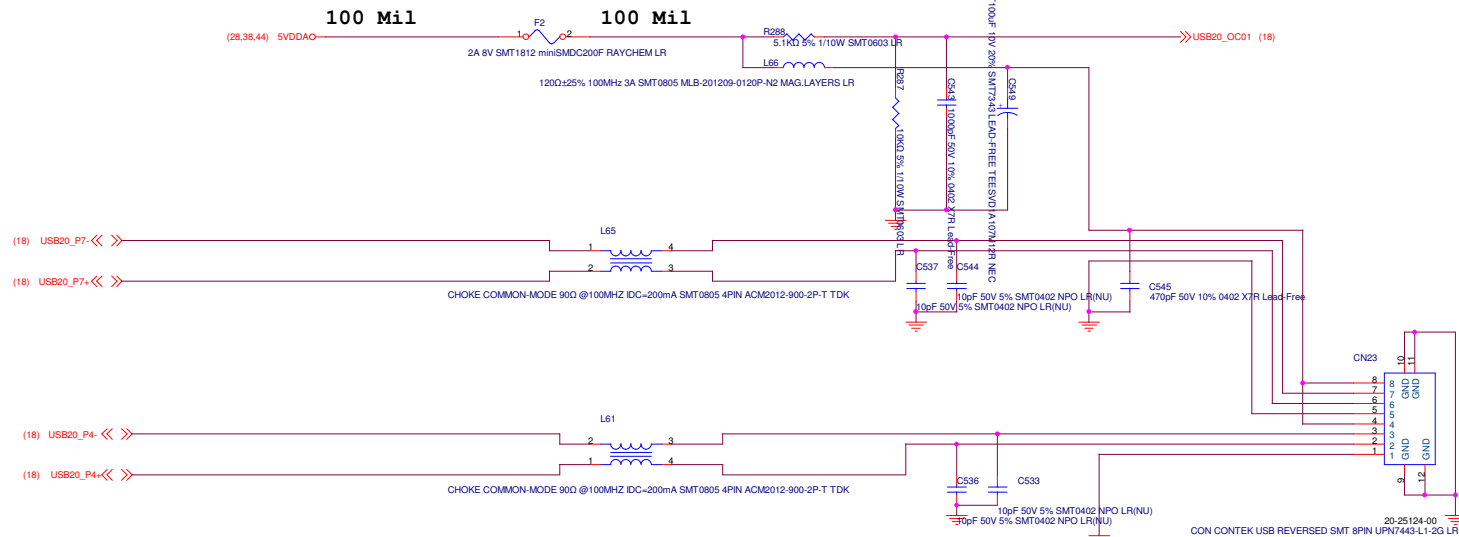
These 3 capacitors across the CHASSIS GND to GND
spike, are located below the magnetics module. Place as
close as possible to the magnetics module.

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	GIGA TRANSFORMER				
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5 mil _____ GND_POWER
5 mil _____ 10 mil USB20_P+
5 mil _____ 5 mil USB20_P-
5 mil _____ 10 mil GND_POWER

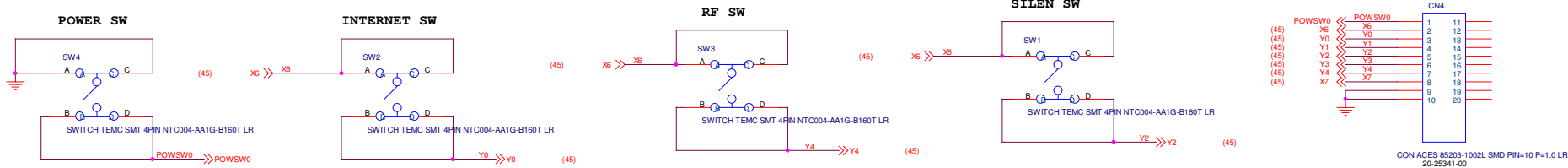
USBP+/- must same length



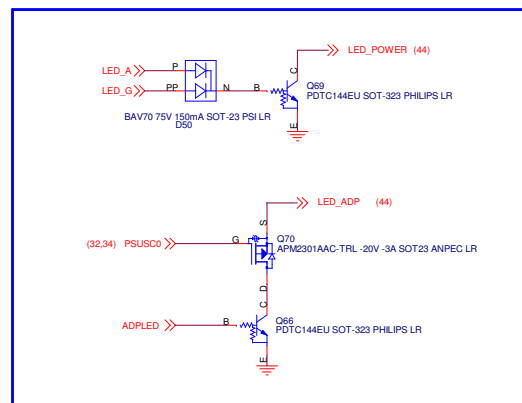
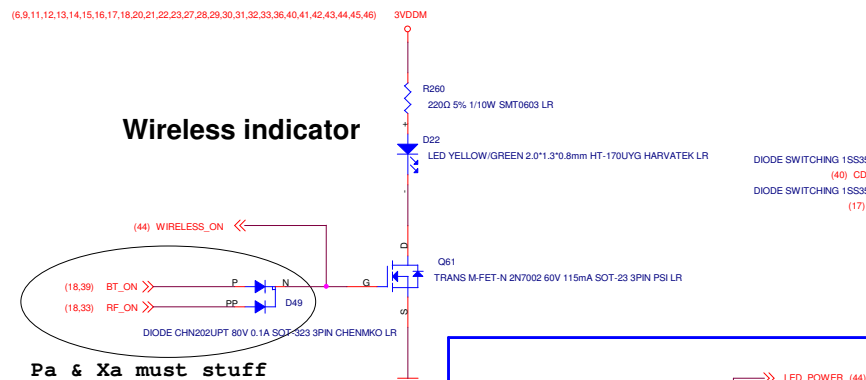
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Title			PTB51
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C	USB CNN	0.6	
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Pa: Switch Xa: No stuff



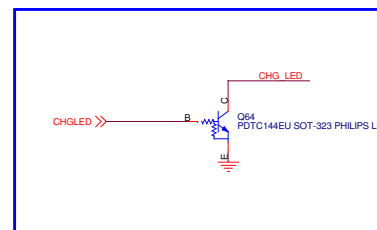
Pa: LED indicator control logic Xa: No stuff



NOTICE

PTB50 → NO STUFF

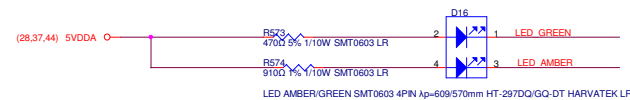
XTB70 → ALL STUFF



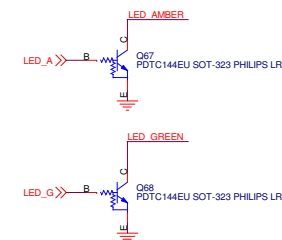
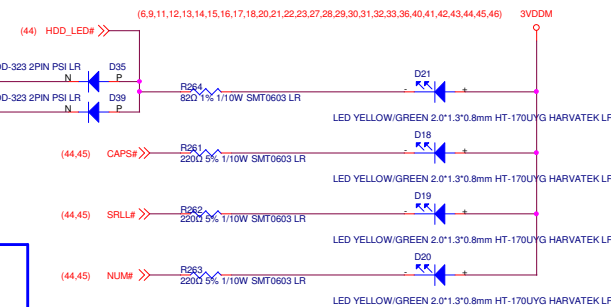
NOTICE

PTB50 / XTB70 → ALL STUFF

Power indicator



Charge indicator



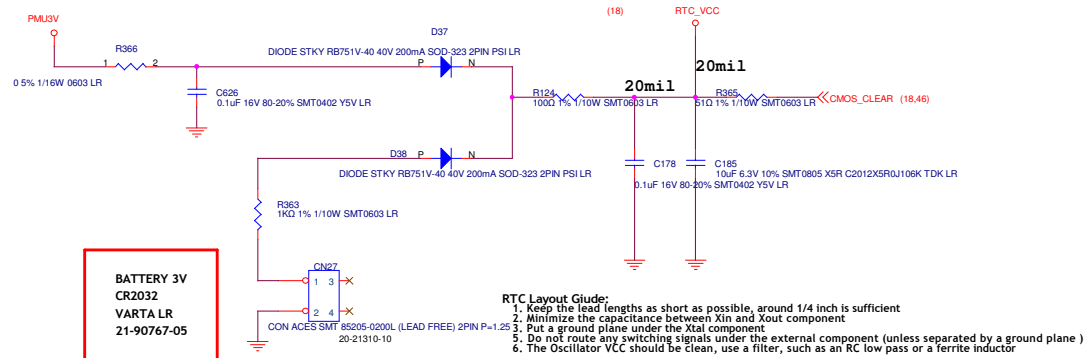
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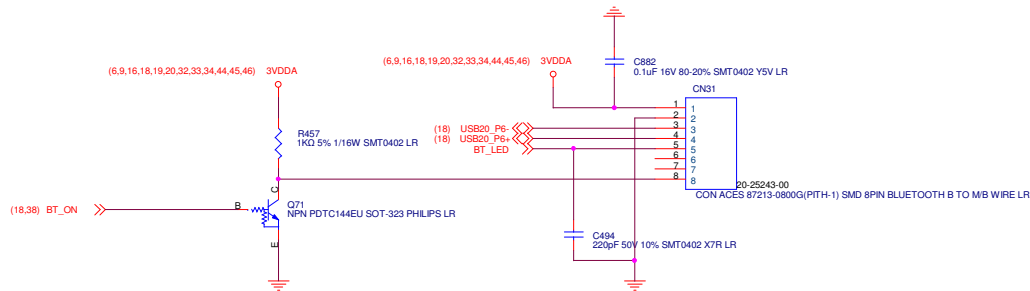
Confidential

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RTC Discharge Circuit

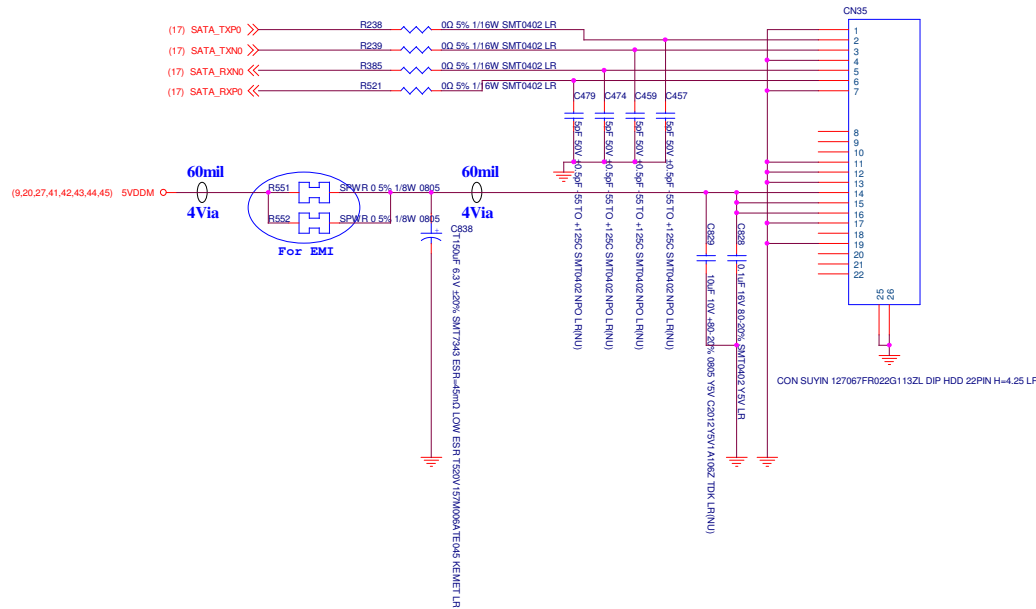


BLUETOOTH

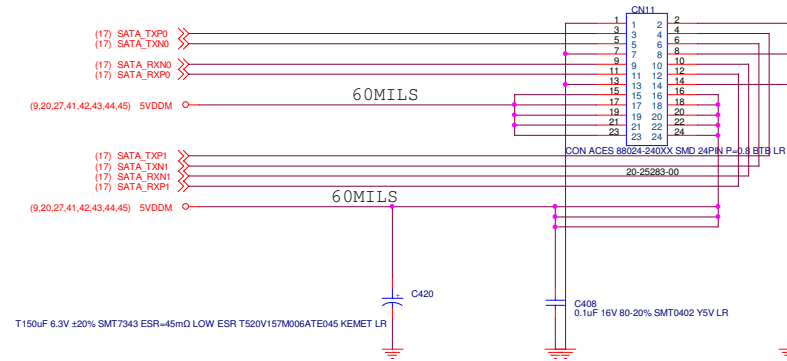


For Pa

HDD I/F



For Xa



SATA Layout Note:

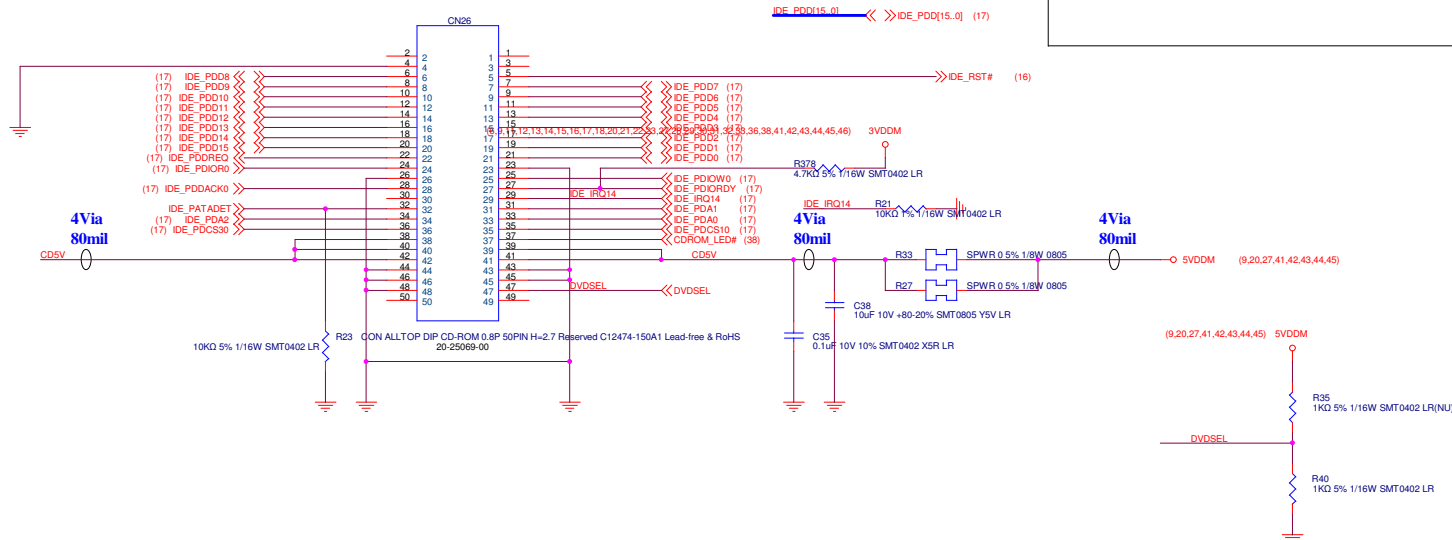
MS or SL:	5mils	5mils	5mils	5mils
	20mils	8mils	20mils	8mils

TX

RX

- * Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- * TX/RX trace length < 2 inchs.
- * TX+/- need matching trace ±10 mils length.
- * RX+/- need matching trace ±10 mils length.
- * SATA Pair to Pair Trace matching trace ±10 mils length.

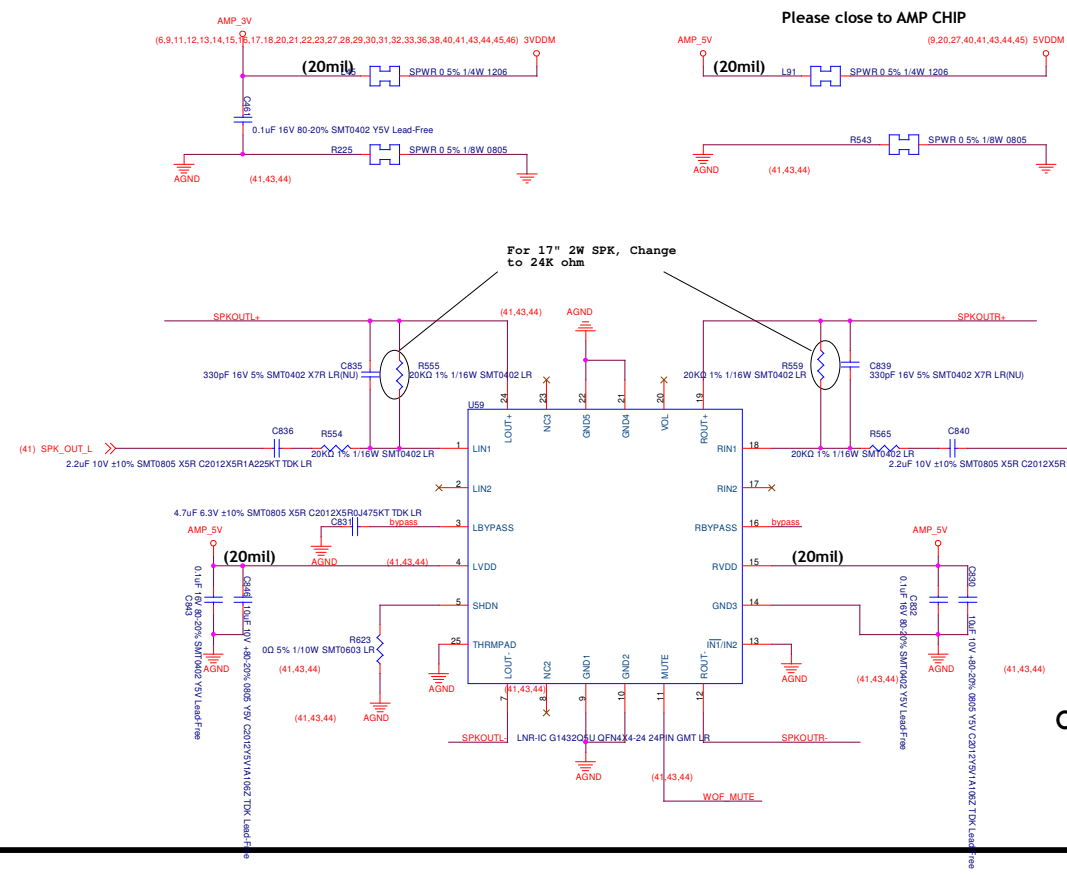
CD-ROM CNN



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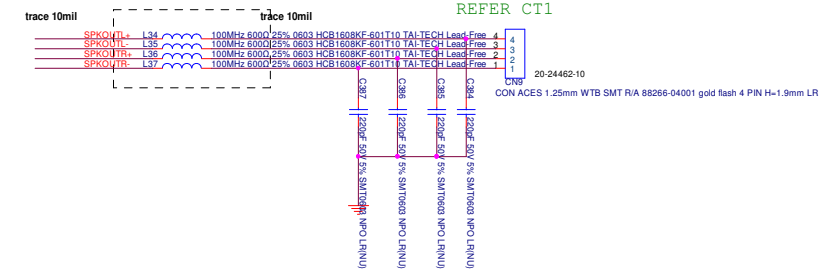
Title	PTB51	Rev	0.6
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C	SATA HD / CD-ROM CNN		
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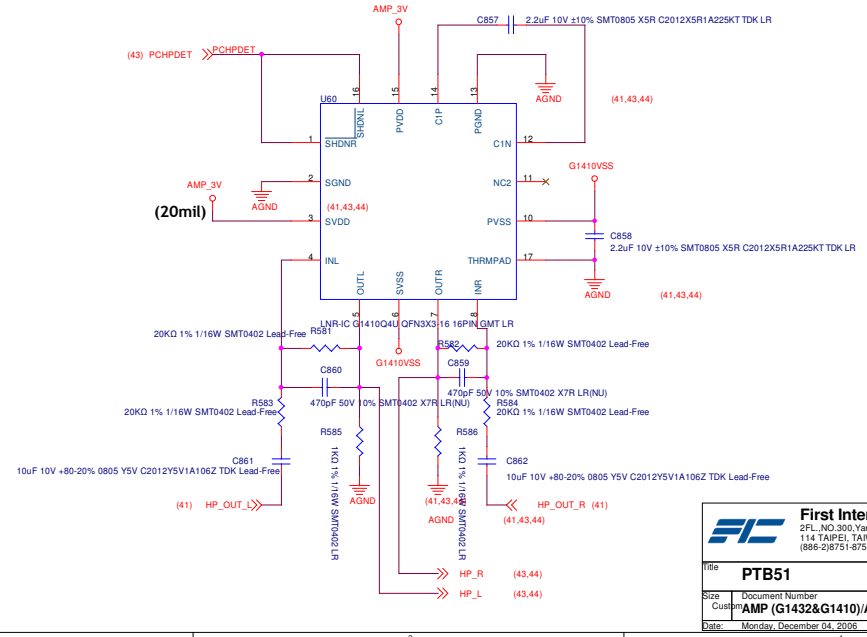
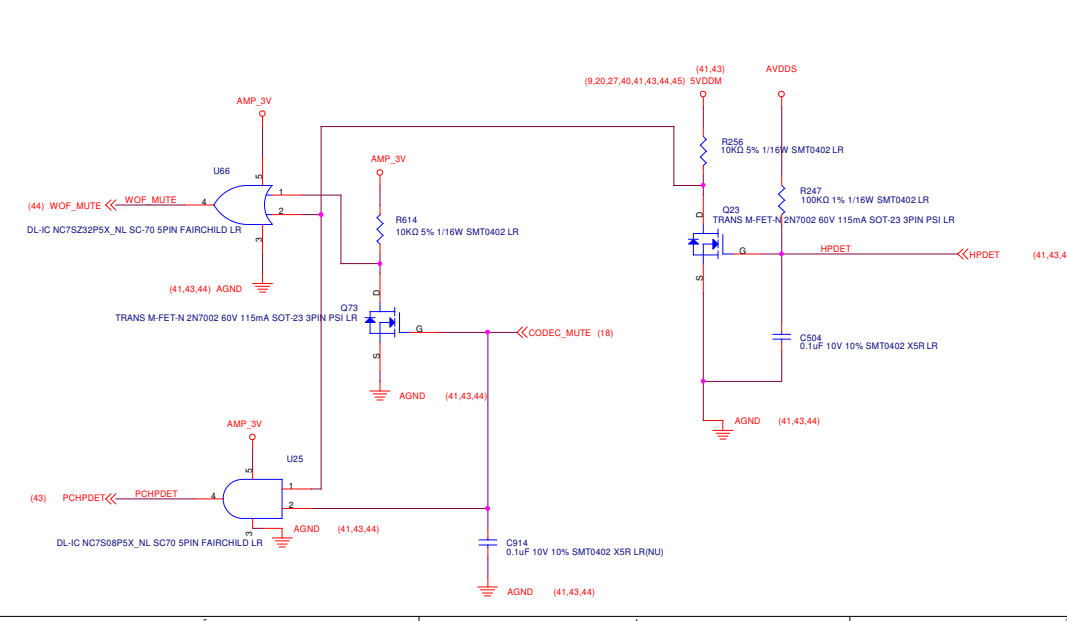
OP CIRCUIT FOR SPEKAER

AGND	10mil	10mil
SPKOUTL+	10mil	10mil
AGND	10mil	10mil
SPKOUTL-	10mil	10mil
AGND	10mil	10mil
SPKOUTR+	10mil	10mil
AGND	10mil	10mil
SPKOUTR-	10mil	10mil
AGND	10mil	10mil

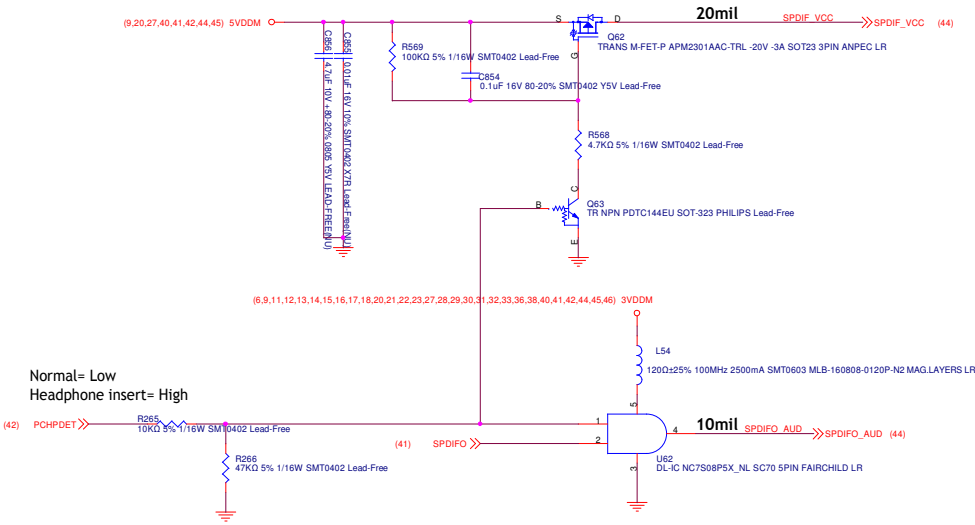
AGND	10mil	10mil
SPK_OUT_L / SPKL	10mil	10mil
AGND	10mil	10mil
SPK_OUT_R / SPKR	10mil	10mil
AGND	10mil	10mil



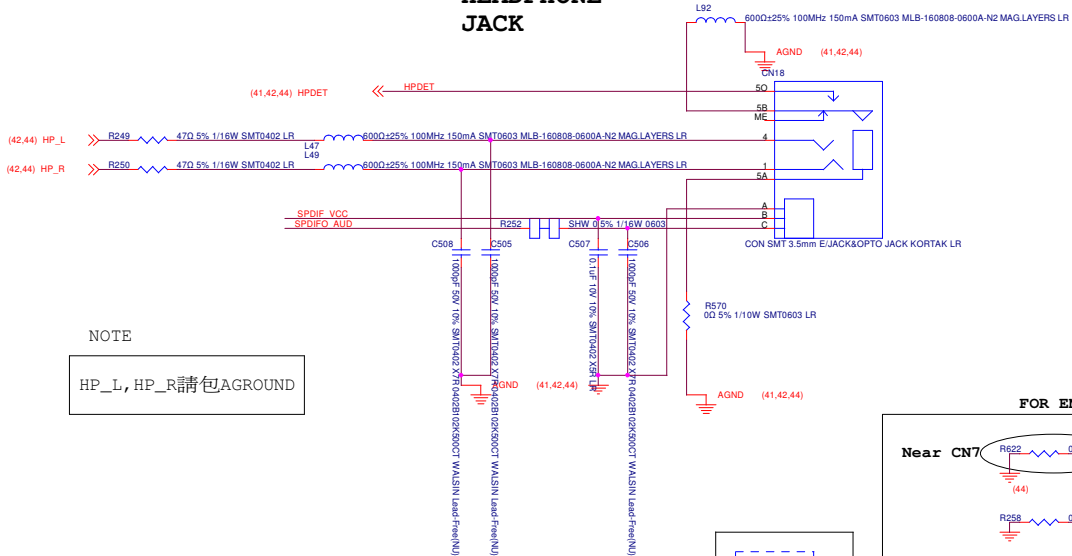
OP CIRCUIT FOR HeadPhone



S/PDIF Power



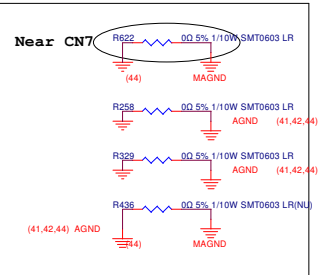
**SPDIF &
HEADPHONE
JACK**



NOTE

HP_L, HP_R請包AGROUND

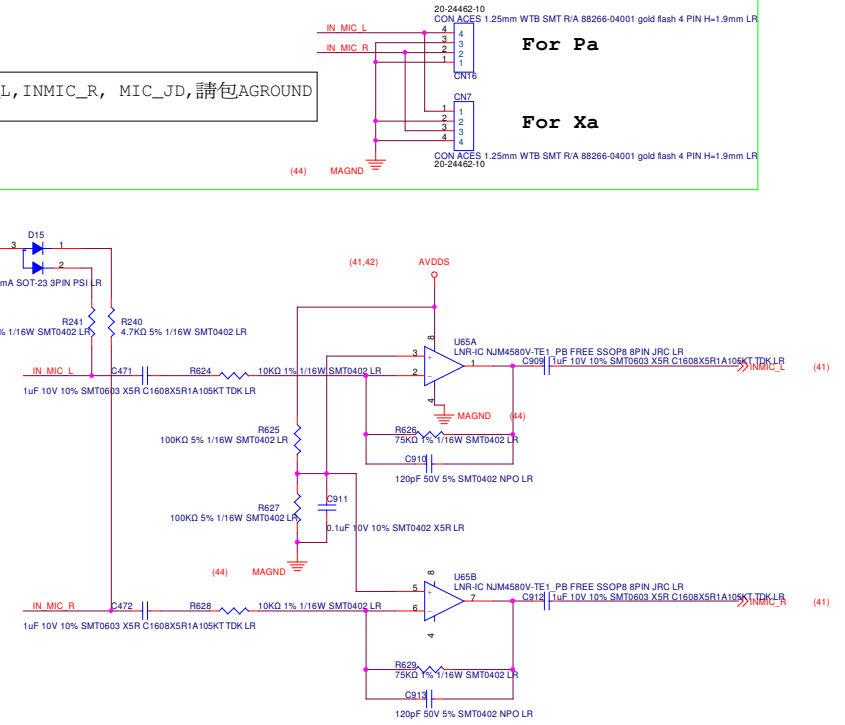
FOR EMI



Internal array MIC

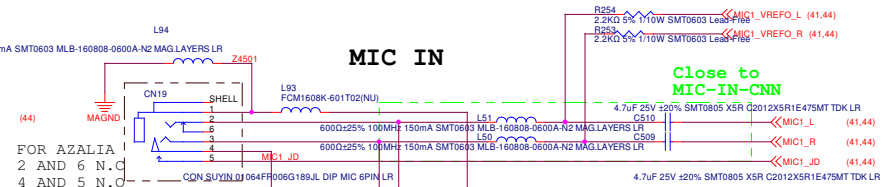
NOTE

INMIC_L, INMIC_R, MIC_JD, 請包AGROUND



MIC IN

Close to
MIC-IN-CNN



NOTE

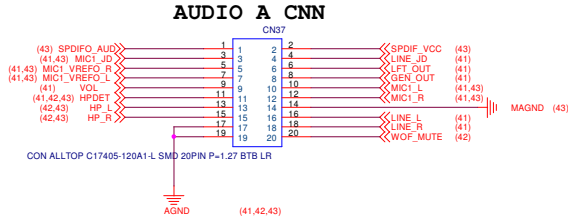
MIC1IN, MIC2IN, MIC_JD, 請包AGROUND



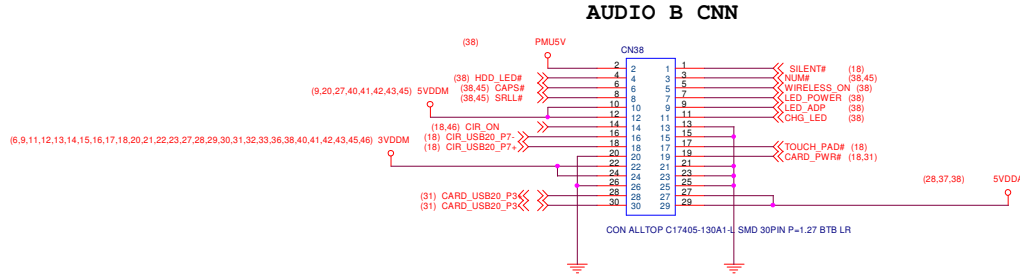
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C	SPDIF OUT				0.6
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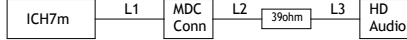
Pa: No Stuff
Xa: Stuff



Pa: No Stuff
Xa: Stuff



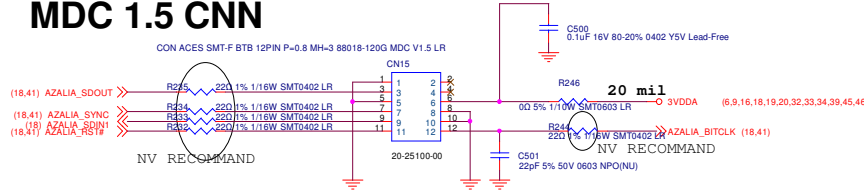
HD Audio-ACZ_SDIN (MDC Connector)



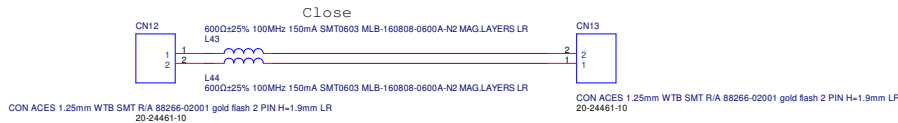
Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"-15" L2 = 0.5"-1.5" L3 = 0.5"

*** Breakout can be routed 4 on 4 up to 400 mils

MDC 1.5 CNN

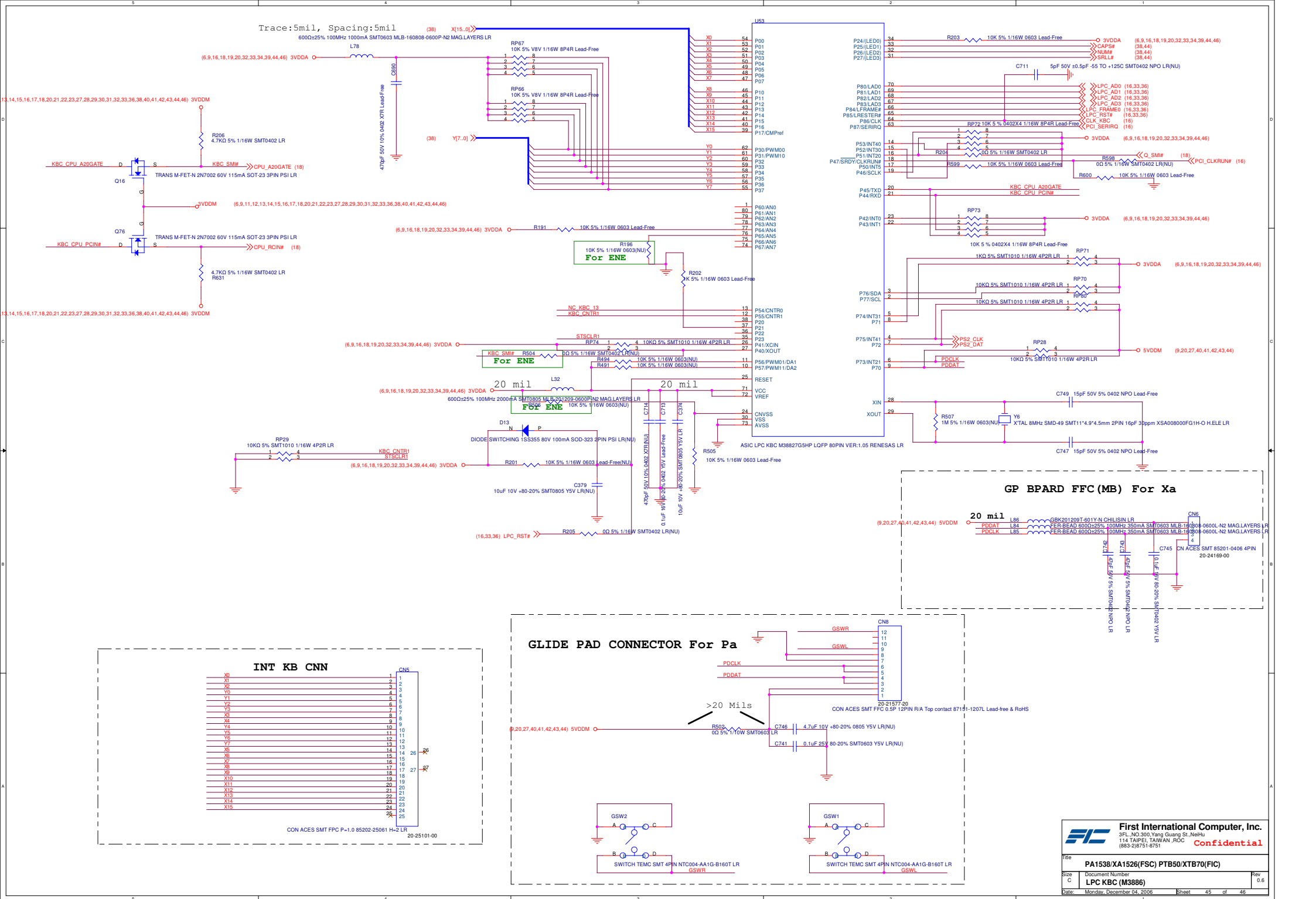


FOR EMI Solution

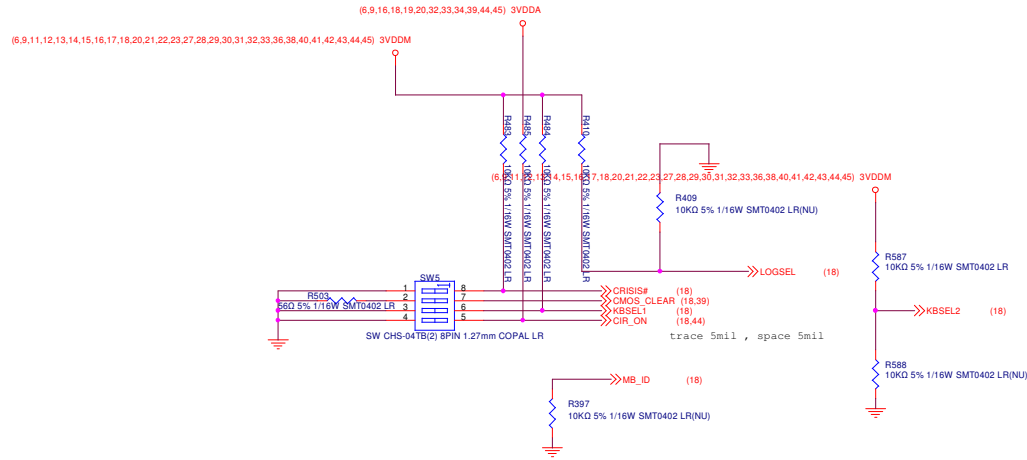


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PTB51
Size C Document Number
DIP SW/CIR/SCREW
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DIP SWITCH



LID Switch

