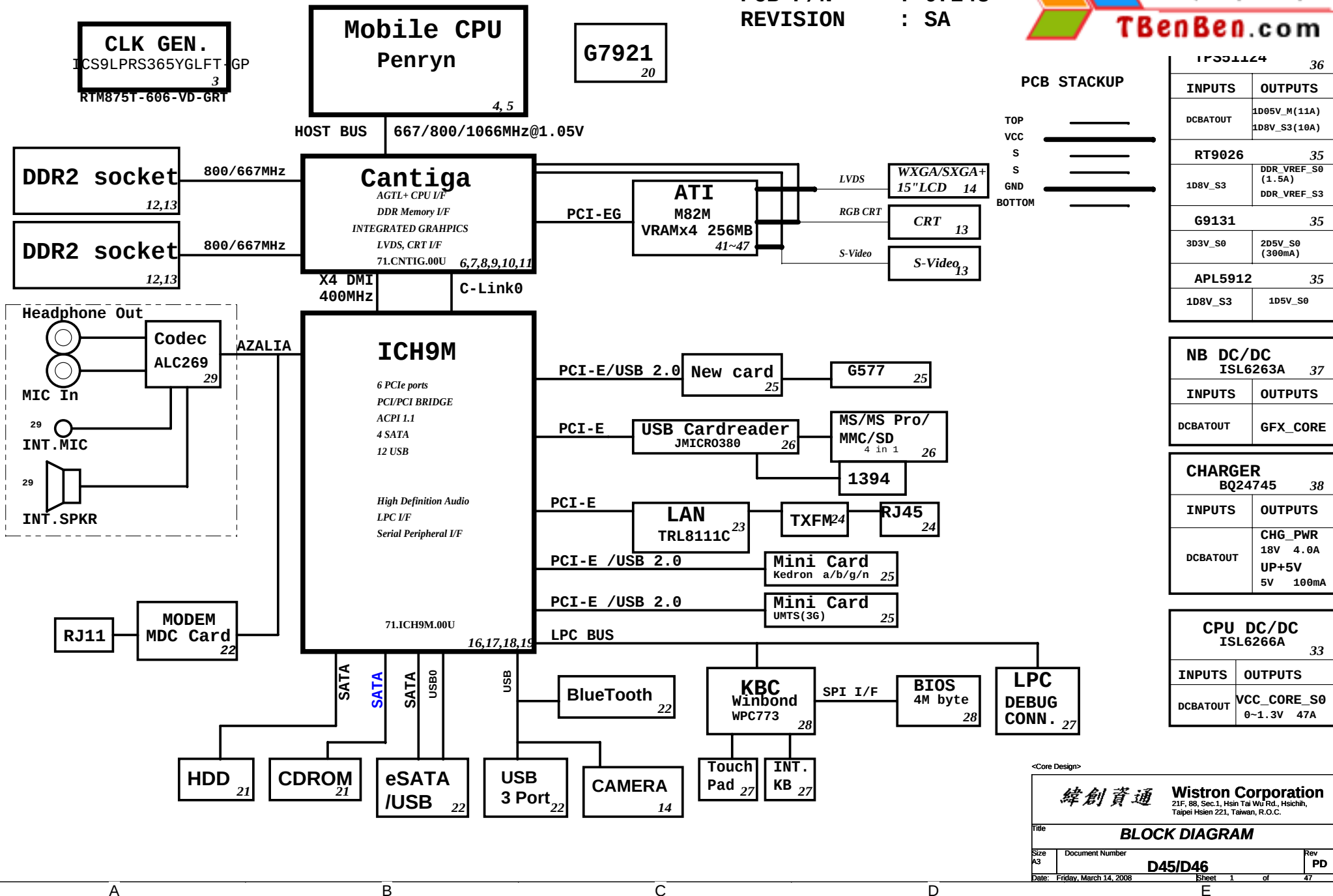


# D45/D46 Block Diagram

Project code: 91.4J00  
91.4K00  
PCB P/N : 07248  
REVISION : SA



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

| Signal                    | Usage/When Sampled                                                     | Comment                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HDA_SDOUT                 | XOR Chain Entrance/<br>PCIE Port Config1 bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down            |
| HDA_SYNC                  | PCIE config1 bit0,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)                                                                                                                     |
| GNT2#/GPIO53              | PCIE config2 bit2,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)                                                                                                                     |
| GPIO20                    | Reserved                                                               | This signal should not be pulled high.                                                                                                                                                                           |
| GNT1#/GPIO51              | ESi Strap (Server Only)<br>Rising Edge of PWROK                        | ESi compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.                                                                                                   |
| GNT3#/GPIO55              | Top-Block Swap Override.<br>Rising Edge of PWROK.                      | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space).<br>Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#:<br>SPI_CS1#/GPIO58 | Boot BIOS Destination Selection 0:1.<br>Rising Edge of PWROK.          | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10).<br>GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.                                                                                   |
| SPI_MOSI                  | Integrated TPM Enable,<br>Rising Edge of CLPWROK                       | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.                                       |
| GPIO49                    | DMI Termination Voltage,<br>Rising Edge of PWROK.                      | The signal is required to be low for desktop applications and required to be high for mobile applications.                                                                                                       |
| SATALED#                  | PCI Express Lane Reversal. Rising Edge of PWROK.                       | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)                                                                                                                          |
| SPKR                      | No Reboot.<br>Rising Edge of PWROK.                                    | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.                                            |
| TP3                       | XOR Chain Entrance.<br>Rising Edge of PWROK.                           | This signal should not be pull low unless using XOR Chain testing.                                                                                                                                               |
| GPIO33/<br>HDA_DOCK_EN#   | Flash Descriptor Security Override Strap<br>Rising Edge of PWROK       | Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.      |

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL                   | Resistor Type/Value                                                                                                 |
|--------------------------|---------------------------------------------------------------------------------------------------------------------|
| CL_CLK[1:0]              | PULL-UP 20K                                                                                                         |
| CL_DATA[1:0]             | PULL-UP 20K                                                                                                         |
| CL_RST0#                 | PULL-UP 20K                                                                                                         |
| DPRSLPVR/GPIO16          | PULL-DOWN 20K                                                                                                       |
| ENERGY_DETECT            | PULL-UP 20K                                                                                                         |
| HDA_BIT_CLK              | PULL-DOWN 20K                                                                                                       |
| HDA_DOCK_EN#/GPIO33      | PULL-UP 20K                                                                                                         |
| HDA_RST#                 | PULL-DOWN 20K                                                                                                       |
| HDA_SDIN[3:0]            | PULL-DOWN 20K                                                                                                       |
| HDA_SDOUT                | PULL-DOWN 20K                                                                                                       |
| HDA_SYNC                 | PULL-DOWN 20K                                                                                                       |
| GLAN_DOCK#               | The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K                                                                                                         |
| GPIO[20]                 | PULL-DOWN 20K                                                                                                       |
| GPIO[49]                 | PULL-UP 20K                                                                                                         |
| LDA[3:0]#/FWH[3:0]#      | PULL-UP 20K                                                                                                         |
| LAN_RXD[2:0]             | PULL-UP 20K                                                                                                         |
| LDRQ[0]                  | PULL-UP 20K                                                                                                         |
| LDRQ[1]/GPIO23           | PULL-UP 20K                                                                                                         |
| PME#                     | PULL-UP 20K                                                                                                         |
| PWRBTN#                  | PULL-UP 20K                                                                                                         |
| SATALED#                 | PULL-UP 15K                                                                                                         |
| SPI_CS1#/GPIO58/CLGPIO6  | PULL-UP 20K                                                                                                         |
| SPI_MOSI                 | PULL-DOWN 20K                                                                                                       |
| SPI_MISO                 | PULL-UP 20K                                                                                                         |
| SPKR                     | PULL-DOWN 20K                                                                                                       |
| TACH_[3:0]               | PULL-UP 20K                                                                                                         |
| TP[3]                    | PULL-UP 20K                                                                                                         |
| USB[11:0][P,N]           | PULL-DOWN 15K                                                                                                       |

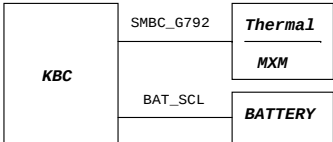
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

| Pin Name                                     | Strap Description                                            | Configuration                                                                                                                                                           |
|----------------------------------------------|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]                                     | FSB Frequency Select                                         | 000 = FSB1067<br>011 = FSB867<br>010 = FSB800<br>others = Reserved                                                                                                      |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved                                                     |                                                                                                                                                                         |
| CFG5                                         | DMI x2 Select                                                | 0 = DMI x2<br>1 = DMI x4 (Default)                                                                                                                                      |
| CFG6                                         | iTPM Host Interface                                          | 0= The iTPM Host Interface is enabled(Note2)<br>1=The iTPM Host Interface is disabled(default)                                                                          |
| CFG7                                         | Intel Management engine Crypto strap                         | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = TLS cipher suite with confidentiality (default)                                          |
| CFG9                                         | PCIE Graphics Lane                                           | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane Numbered in order                                                                              |
| CFG10                                        | PCIE Loopback enable                                         | 0 = Enable (Note 3)<br>1= Disabled (default)                                                                                                                            |
| CFG[13:12]                                   | XOR/ALL                                                      | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALLZ mode Enabled (Note 3)<br>11 = Disabled (default)                                                                     |
| CFG16                                        | FSB Dynamic ODT                                              | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)                                                                                                           |
| CFG19                                        | DMI Lane Reversal                                            | 0 = Normal operation(Default):<br>Lane Numbered in Order<br>1 = Reverse Lanes<br>DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20                                        | Digital Display Port (SDVO/DP/iHDMI)<br>Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default)<br>1 = Digital display Port and PCie are operting simulataneously via the PEG port                       |
| SDVO_CTRLDATA                                | SDVO Present                                                 | 0 =No SDVO Card Present (Default)<br>1 = SDVO Card Present                                                                                                              |
| L_DDC_DATA                                   | Local Flat Panel (LFP) Present                               | 0 = LFP Disabled (Default)<br>1= LFP Card Present; PCIE disabled                                                                                                        |

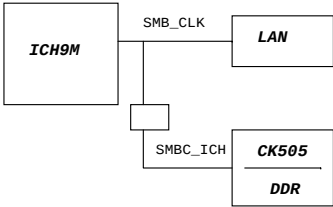
NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

| USB  |                   |
|------|-------------------|
| Pair | Device            |
| 0    | Combo (ESATA/USB) |
| 1    | NC                |
| 2    | USB2              |
| 3    | USB4              |
| 4    | USB3              |
| 5    | BLUETOOTH         |
| 6    | WEBCAM            |
| 7    | FT                |
| 8    | MINICARD          |
| 9    | NEW1              |



PCI Routing

page 17

|        | IDSEL | INT                                               | REQ | GNT |
|--------|-------|---------------------------------------------------|-----|-----|
| TI7412 | AD22  | G:CARDBUS<br>B:1394<br>F:Flash Media<br>G:SD Host | 0   | 0   |

PCIE Routing

|       |               |
|-------|---------------|
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN  |

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title

Reference

Size

Document Number

D45/D46

Rev

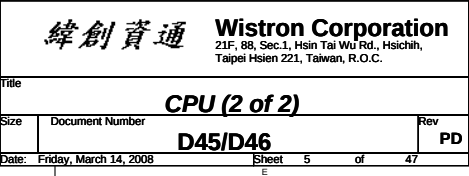
PD

Date: Friday, March 14, 2008

Sheet 2 of 47

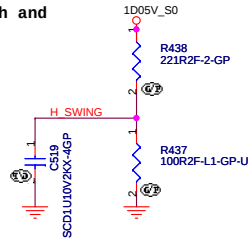




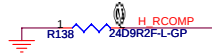


H\_SWING routing Trace width and Spacing use 10 / 20 mil

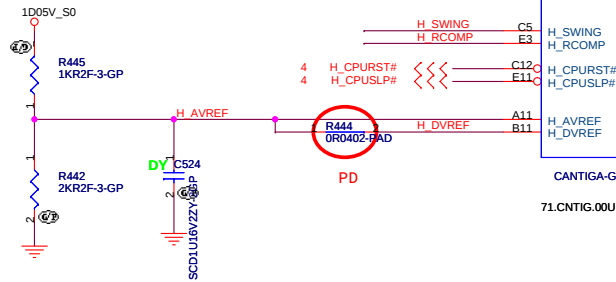
H\_SWING Resistors and Capacitors close MCH 500 mil ( MAX )



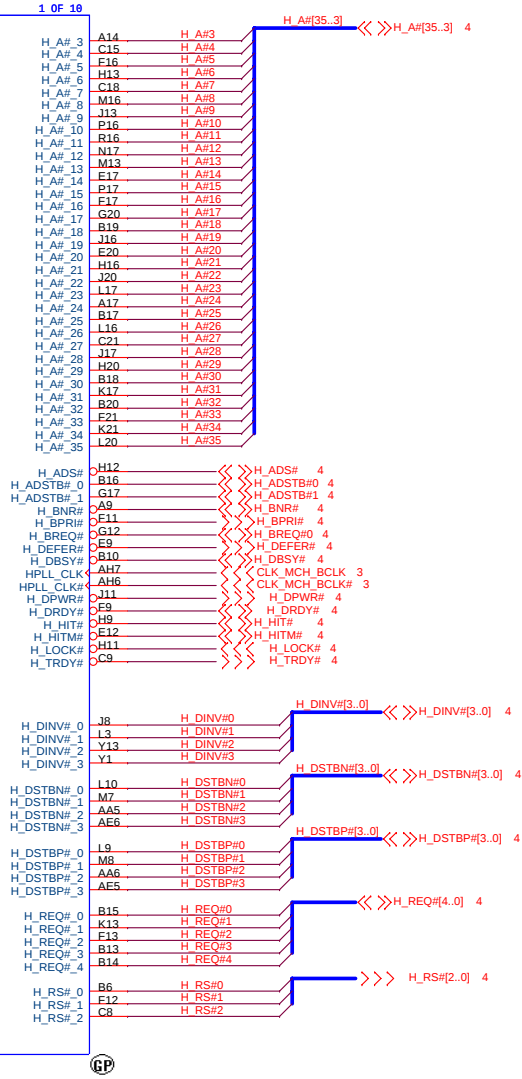
H\_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip ( < 0.5")



HOST



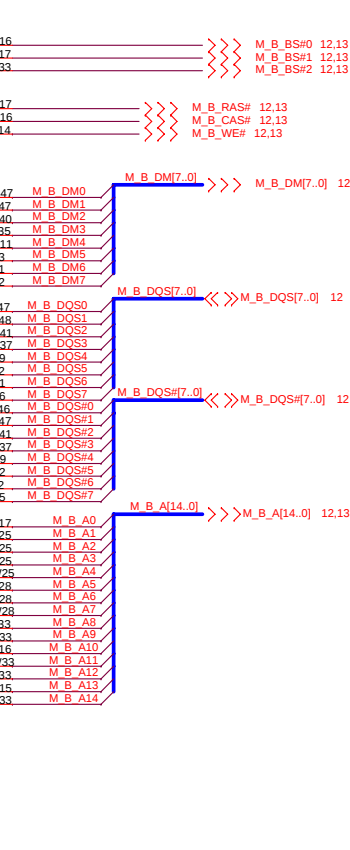
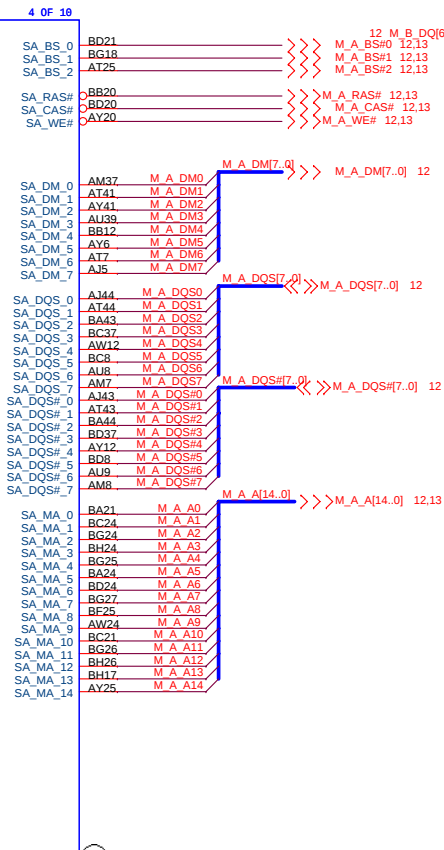
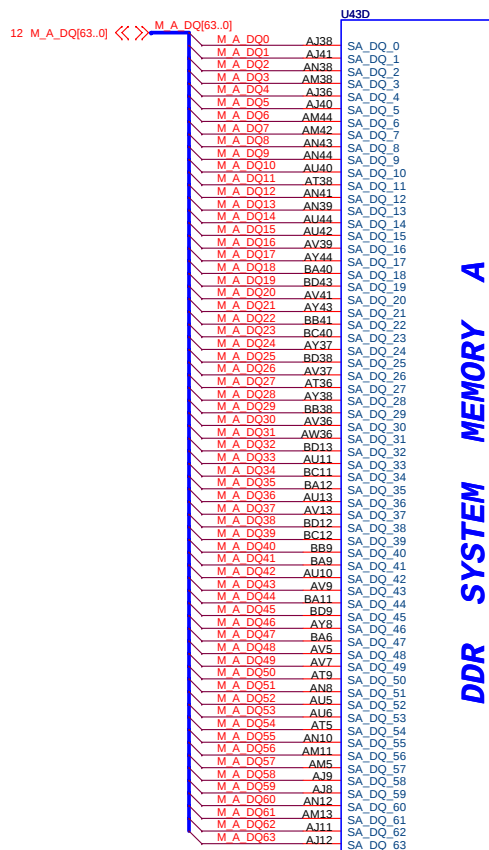
D45 SB use 71.CNTIG.H0U

D46 SB use 71.CNTIG.G0U

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|                              |                 |       |
|------------------------------|-----------------|-------|
| Title                        |                 |       |
| Cantiga (1 of 6)             |                 |       |
| Size                         | Document Number | Rev   |
|                              | D45/D46         | PD    |
| Date: Friday, March 14, 2008 | Sheet 6         | of 47 |





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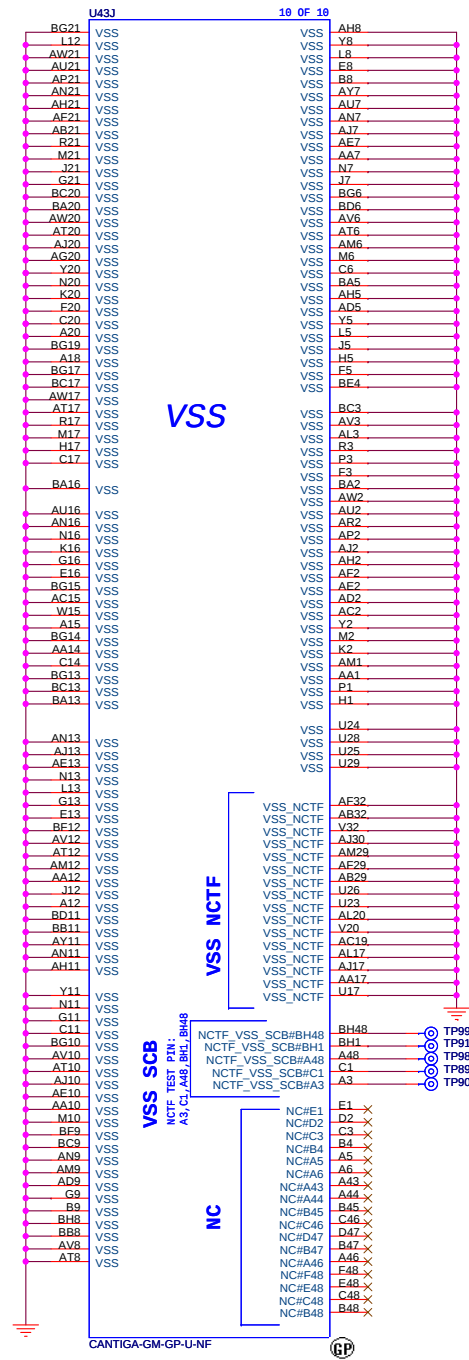
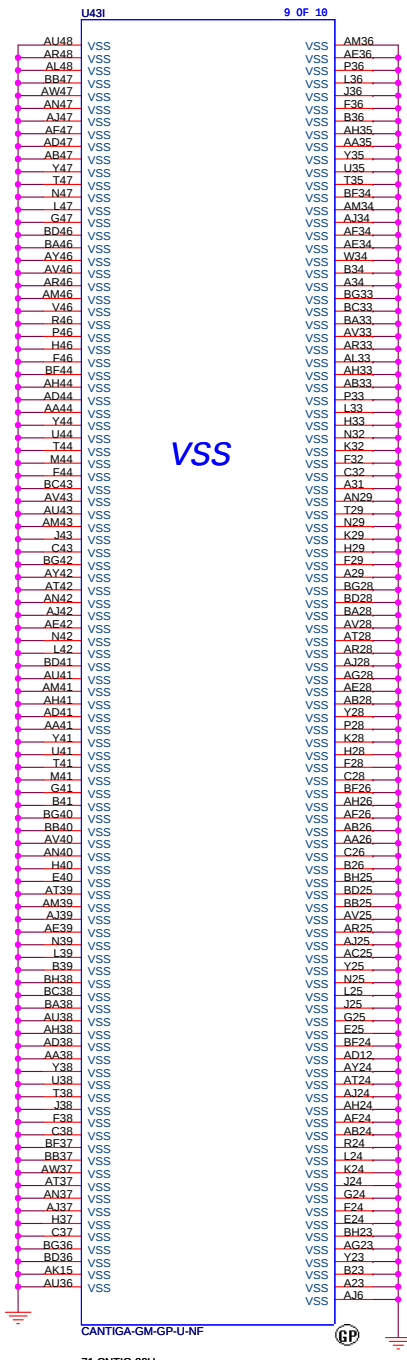
Title

Size Document Number Rev

Date: Friday, March 14, 2008 Sheet 8 of 47







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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**Cantiga (6 of 6)**

Size Document Number Rev  
**D45/D46** PD

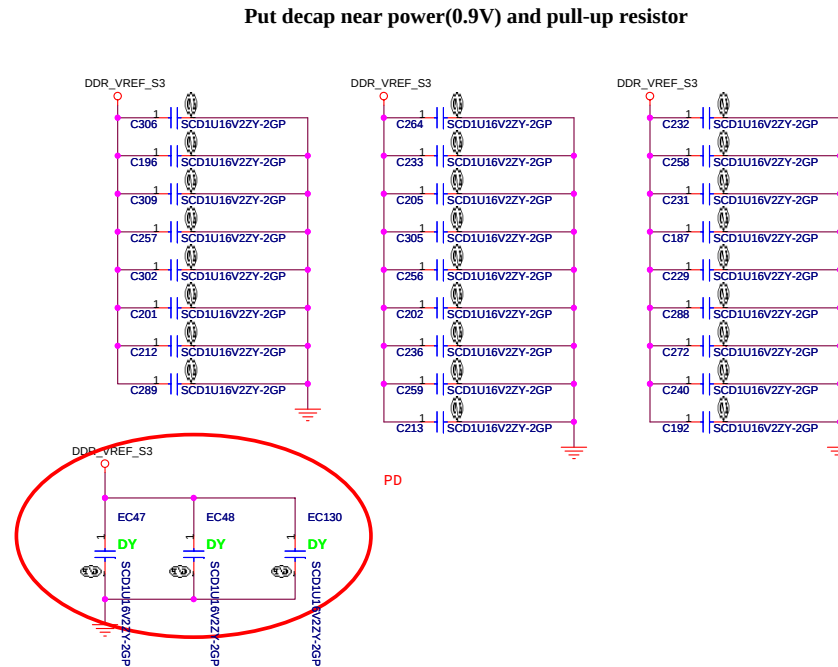
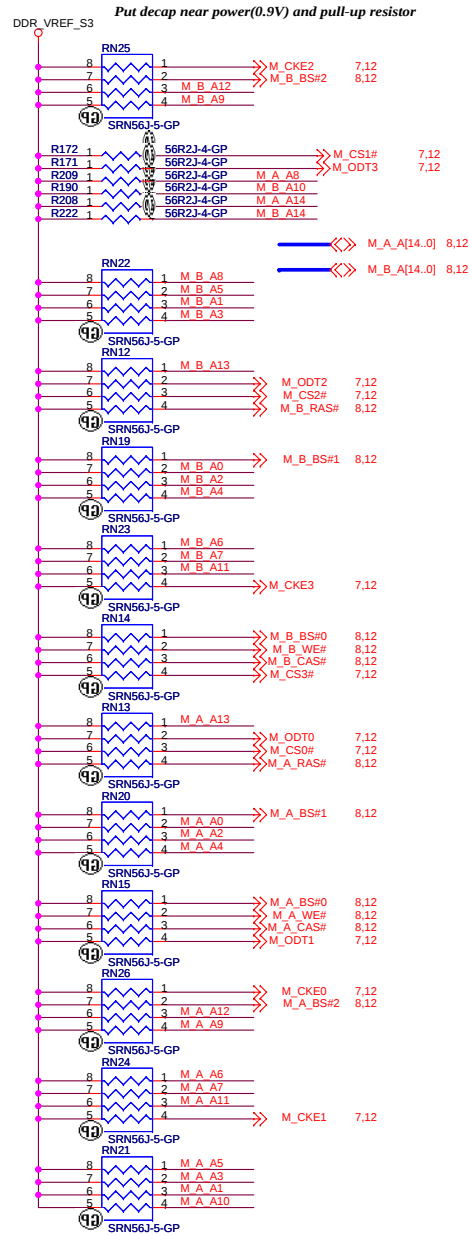
Date: Friday, March 14, 2008 Sheet 11 of 47

1



# PARALLEL TERMINATION

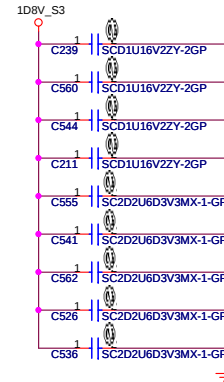
# Decoupling Capacitor



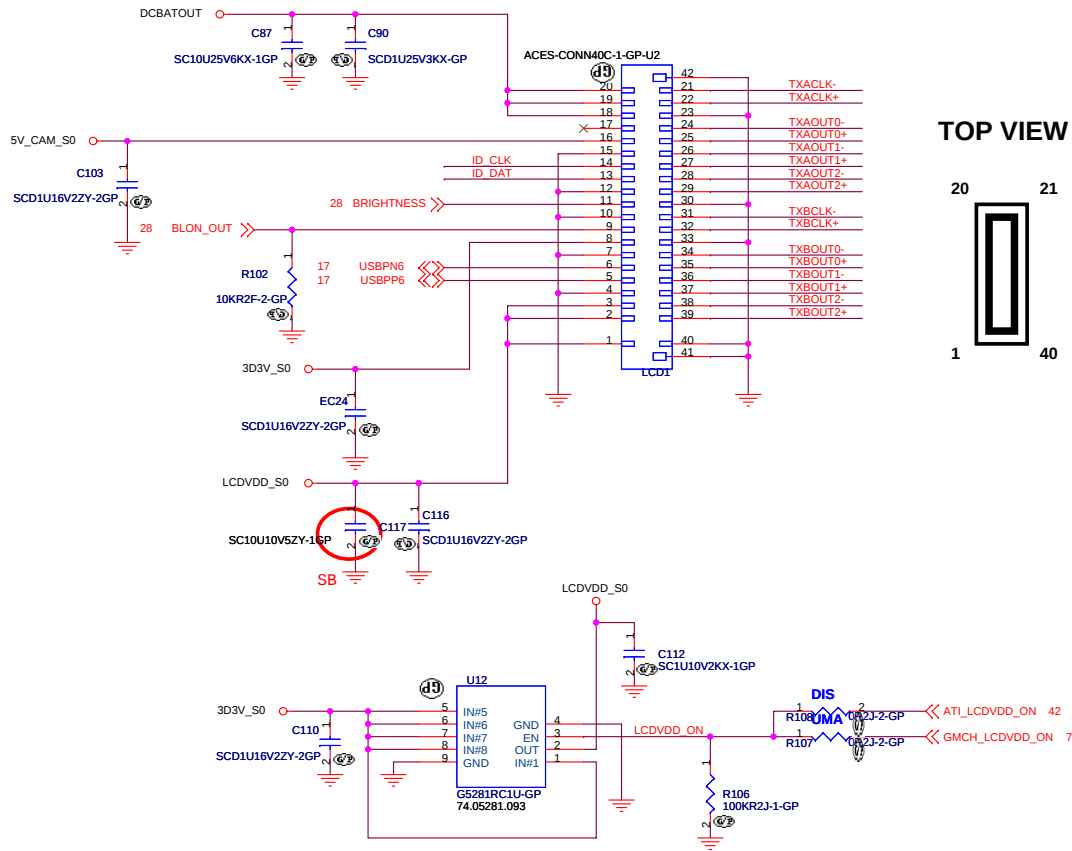
Place these Caps near DM1



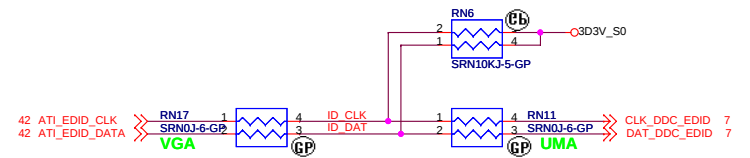
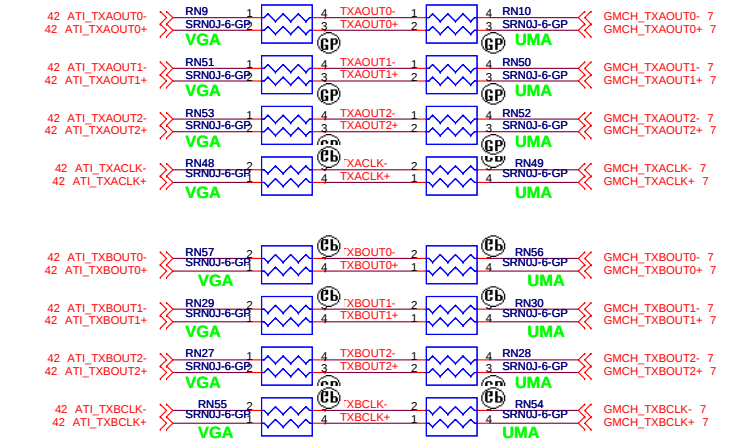
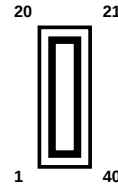
Place these Caps near DM2



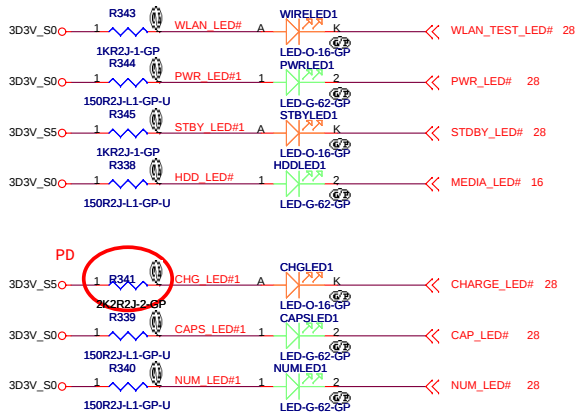
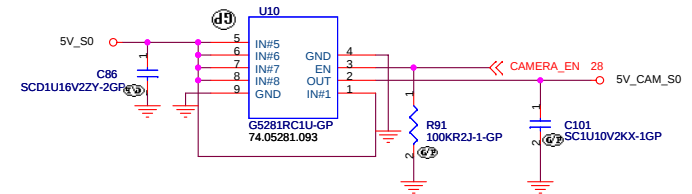
# LCD CONNECTOR



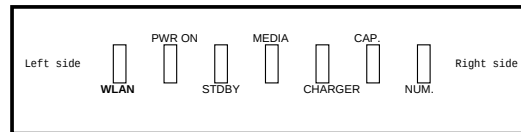
## TOP VIEW



## WEBCAM POWER



## LED Location and Sequence ( The edge of PCB,Top view )

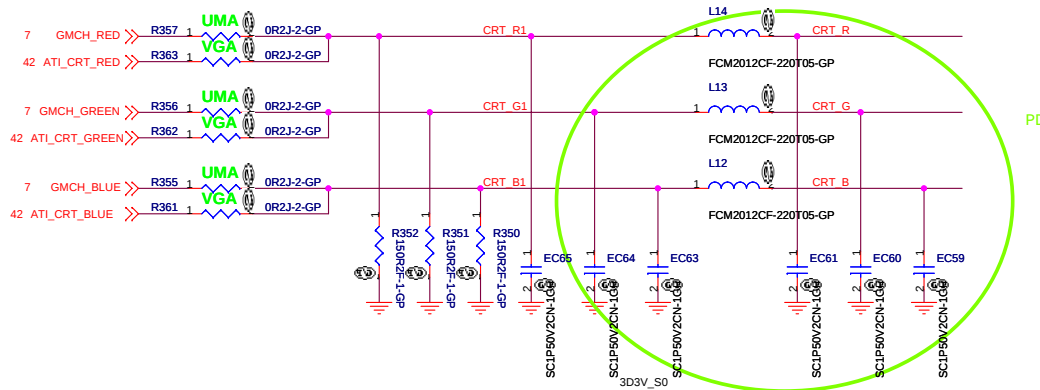


ZZZZ

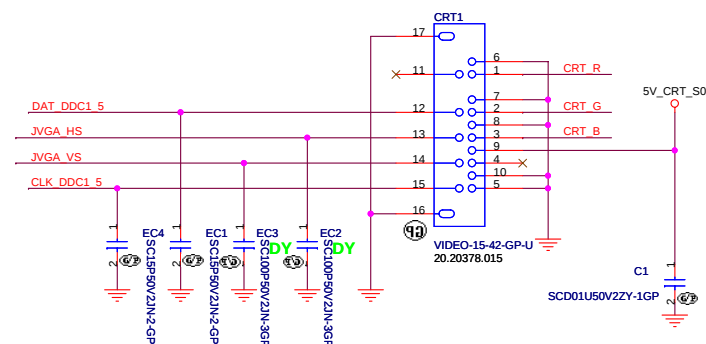
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|----------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>緯創資通</b><br><b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title                                                                                                                      |                 |
| <b>LCD CONN / LED / WEBCAM</b>                                                                                             |                 |
| Size                                                                                                                       | Document Number |
| A3                                                                                                                         | D45/D46         |
| Date:                                                                                                                      | Rev             |
| Friday, March 14, 2008                                                                                                     | PD              |
| Sheet                                                                                                                      | of              |
| 14                                                                                                                         | 47              |

**Layout Note:**  
Place these resistors close to the CRT-out connector

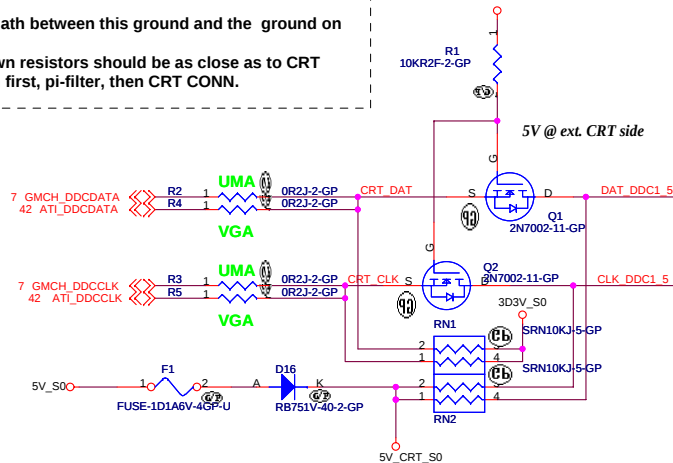
Ferrite bead impedance: 10 ohm@100MHz  
PD use 22 ohm 68.00215.211



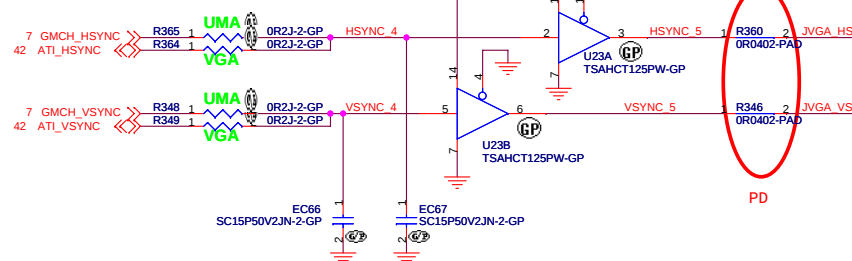
## CRT I/F & CONNECTOR



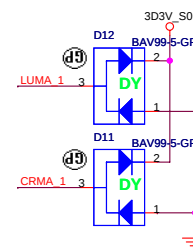
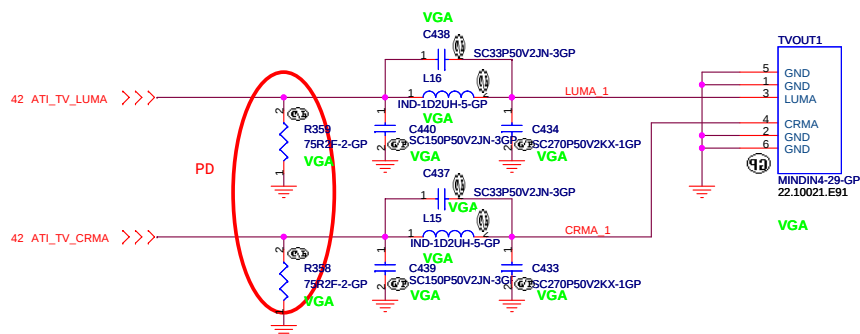
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



### Hsync & Vsync level shift



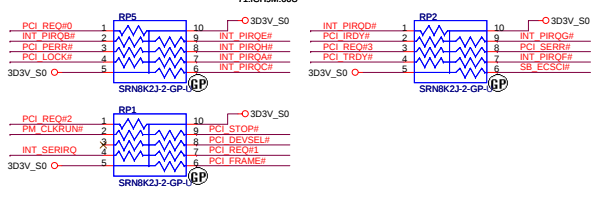
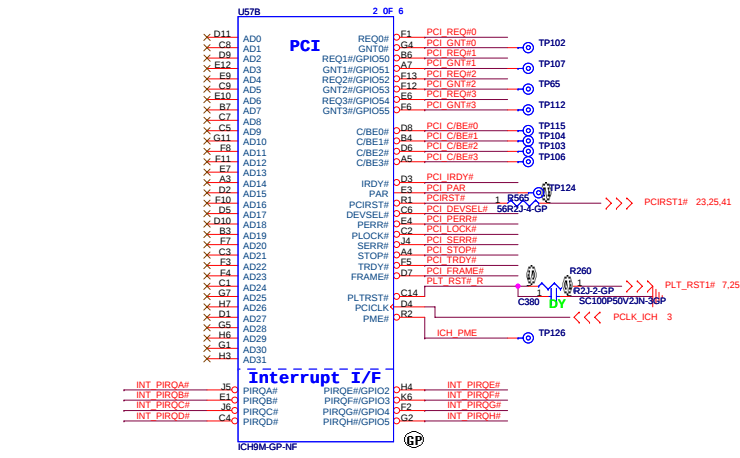
## TV CONN



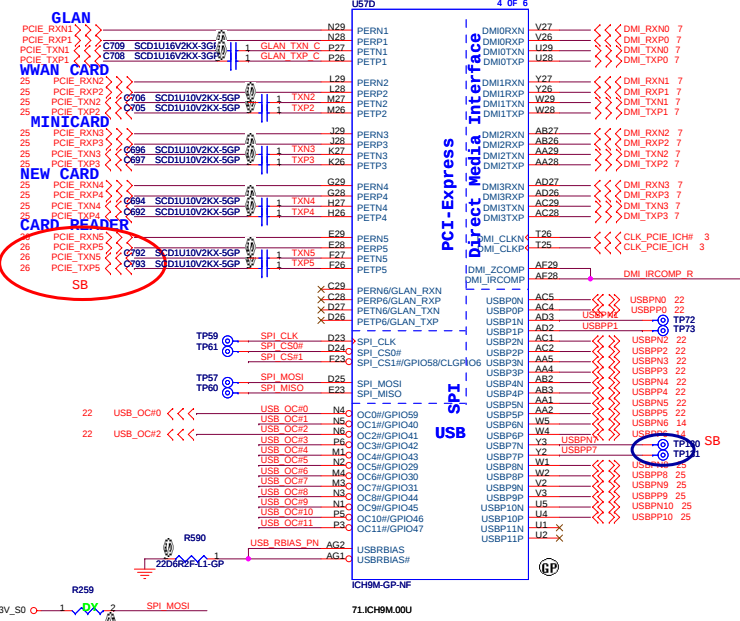
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|                         |                         |                |
|-------------------------|-------------------------|----------------|
| Title                   |                         |                |
| <b>CRT/TV Connector</b> |                         |                |
| Size                    | Document Number         | Rev            |
|                         | <b>D45/D46</b>          | <b>PD</b>      |
| Date:                   | Tuesday, March 18, 2008 | Sheet 15 of 47 |

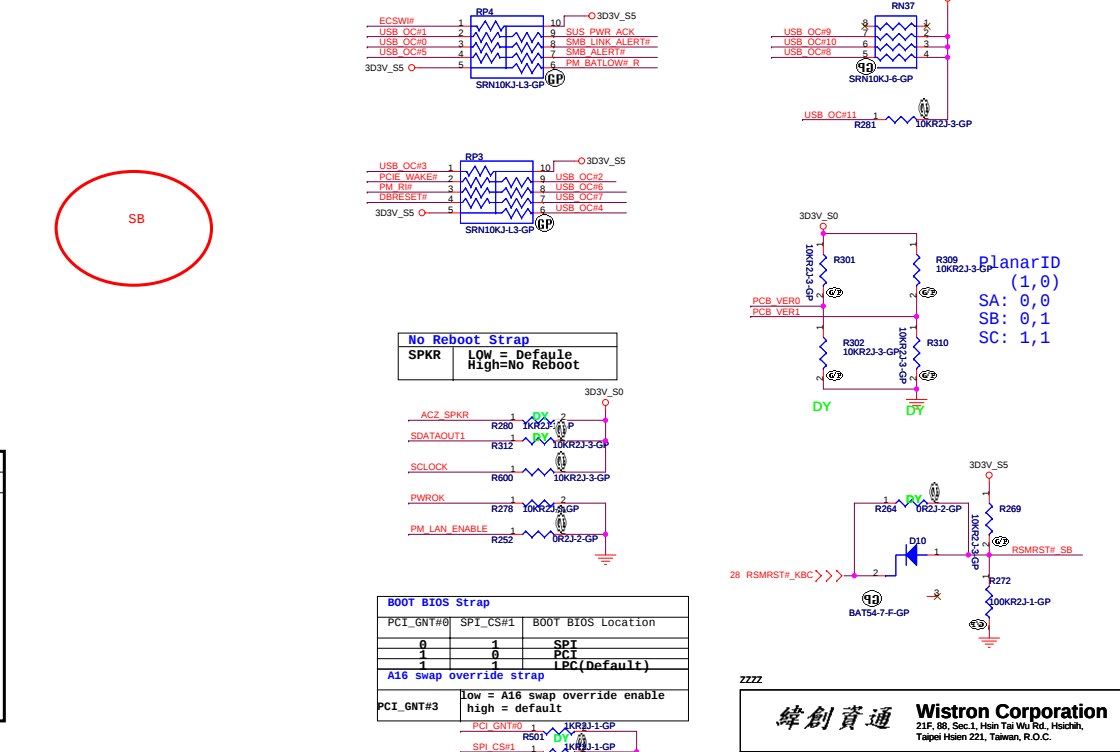
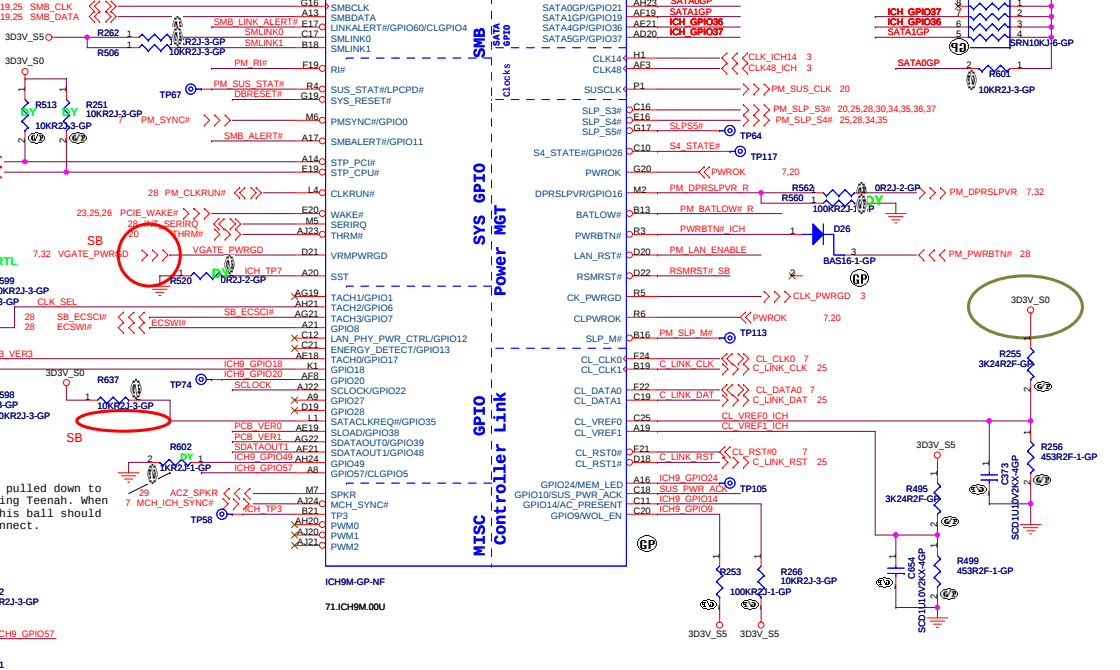


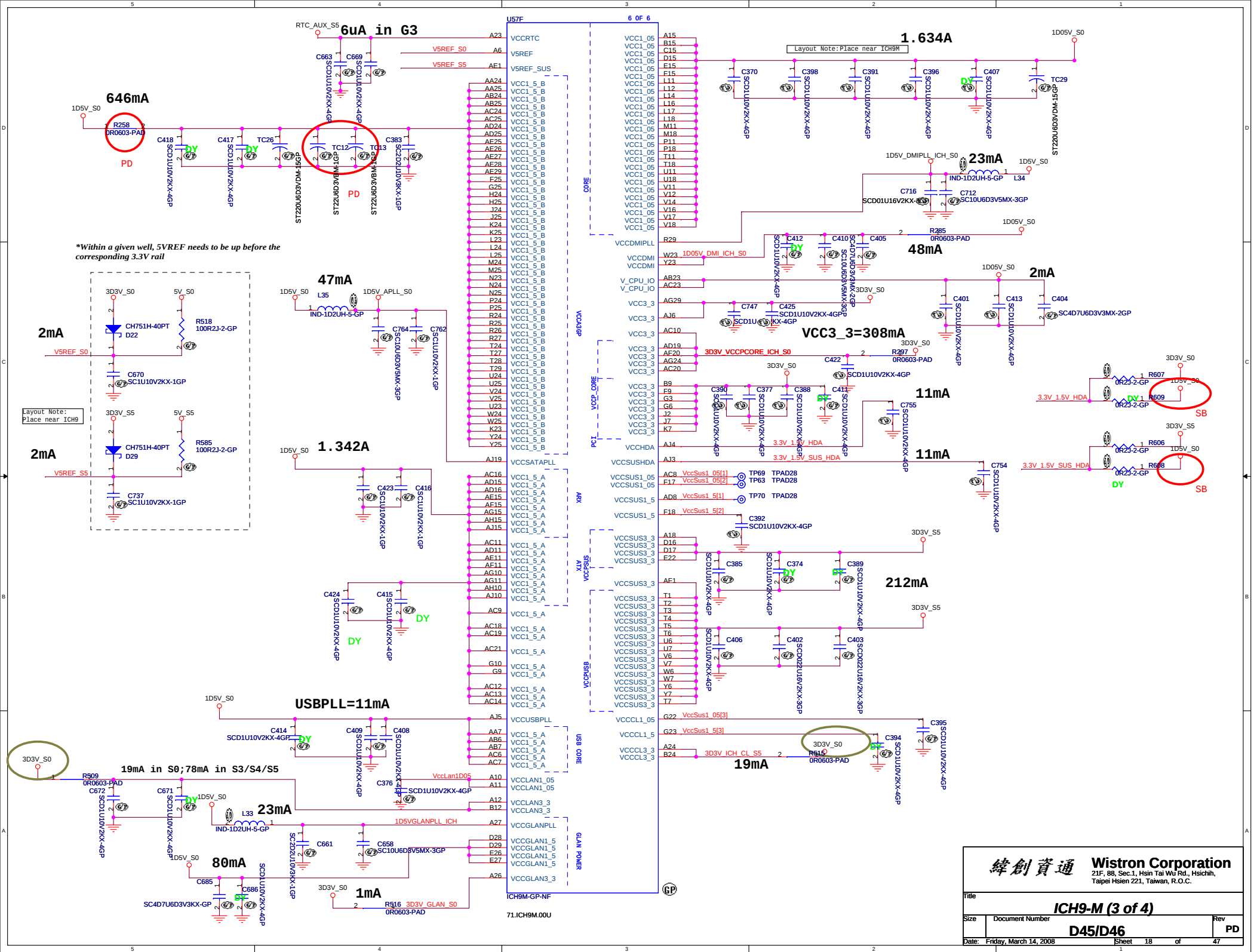


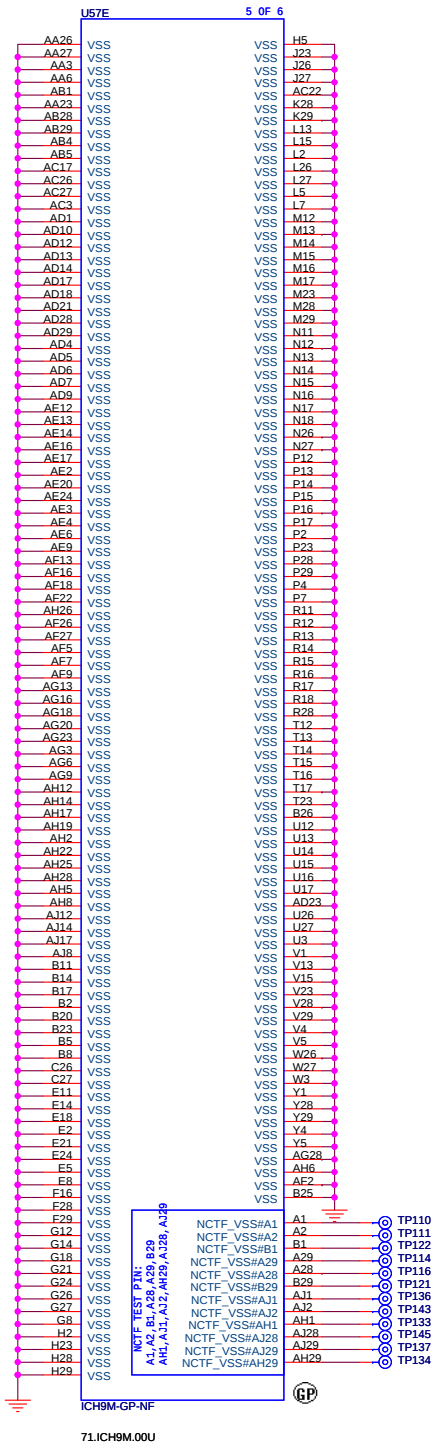
Layout Note:  
PCIe AC coupling caps  
need to be within 250 mils of the driver.



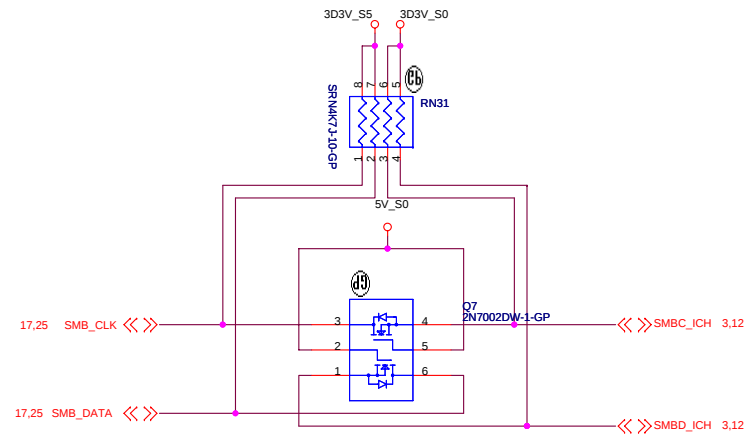
| Pair | Device    |
|------|-----------|
| 0    | USB1      |
| 1    | NC        |
| 2    | USB2      |
| 3    | USB3      |
| 4    | USB4      |
| 5    | BLUETOOTH |
| 6    | WEBCAM    |
| 7    | NC        |
| 8    | MINICARD  |
| 9    | UMTS      |
| 10   | NEW CARD  |







71.ICH9M.00U



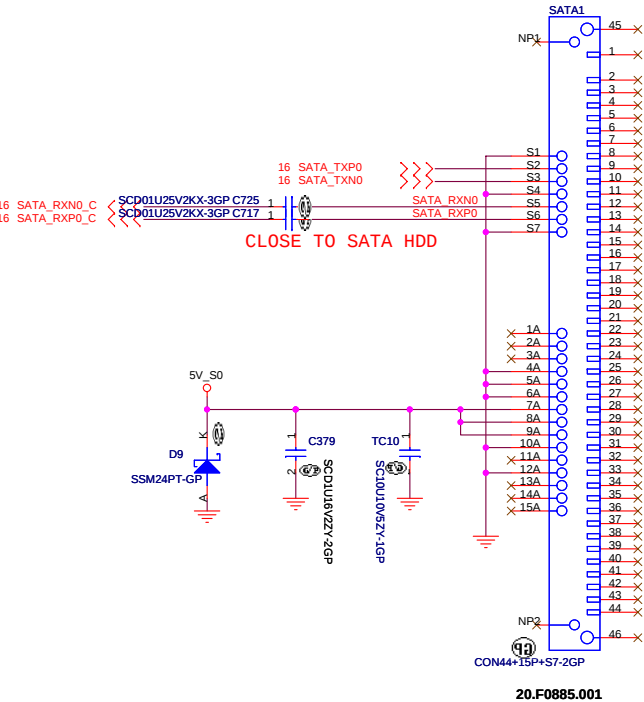
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

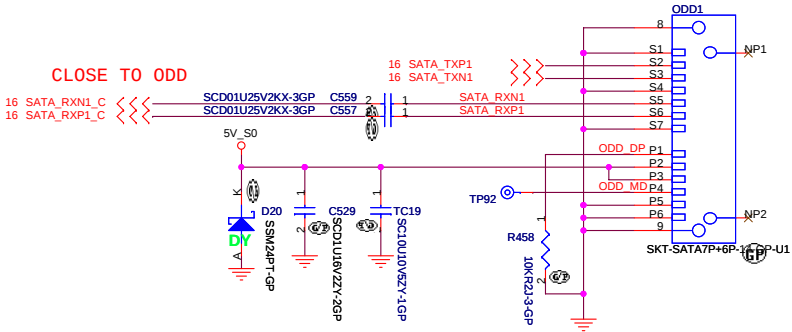
|                                                                            |                 |
|----------------------------------------------------------------------------|-----------------|
| 緯創資通 Wistron Corporation                                                   |                 |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title ICH9-M (4 of 4)                                                      |                 |
| Size                                                                       | Document Number |
| D45/D46                                                                    |                 |
| Date: Friday, March 14, 2008                                               | Sheet 19 of 47  |
| Rev PD                                                                     |                 |



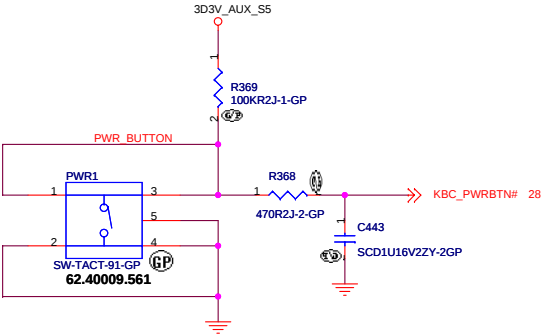
# SATA HD Connector



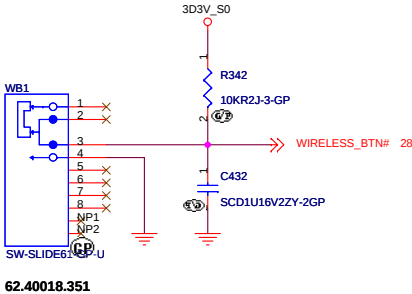
# ODD Connector



# LAUNCH BUTTON



# WIRELESS BUTTON



USBBCN1

21

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

22

5V\_S5

C450

SCD1U16V2ZY-2GP

USB PWR\_EN#

USBP2 17

USBPP2 17

USBP3 17

USBPP3 17

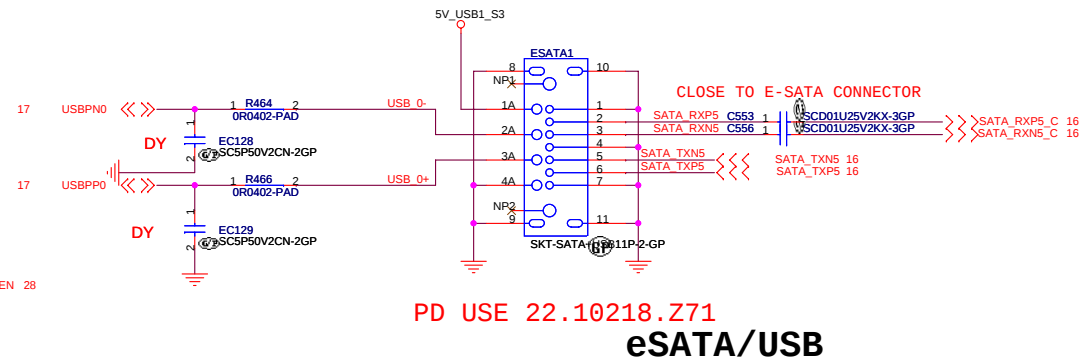
USBP4 17

USBPP4 17

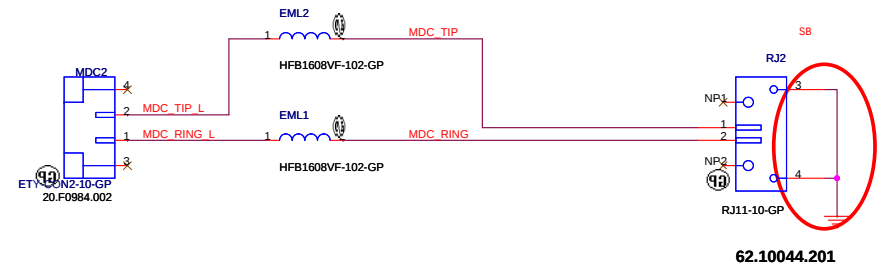
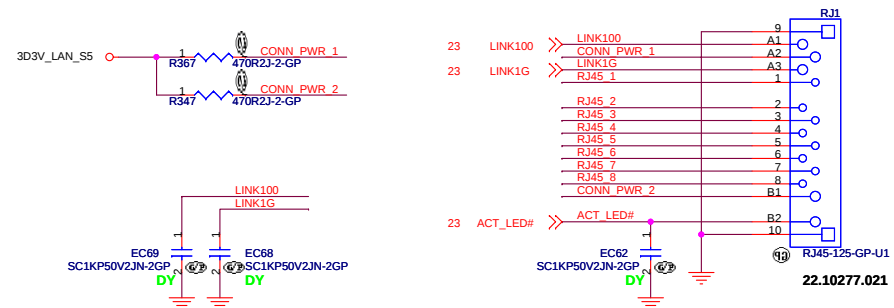
USB\_OC#2 17

ACES-CON20-2-GP

20.K0261.020







- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

### Newcard Frame



(ROBISON RESERVE)

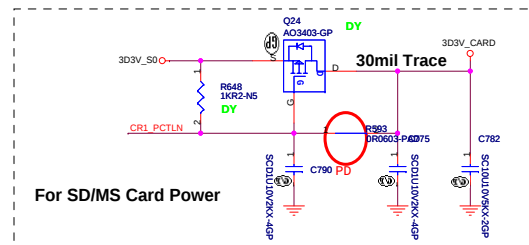
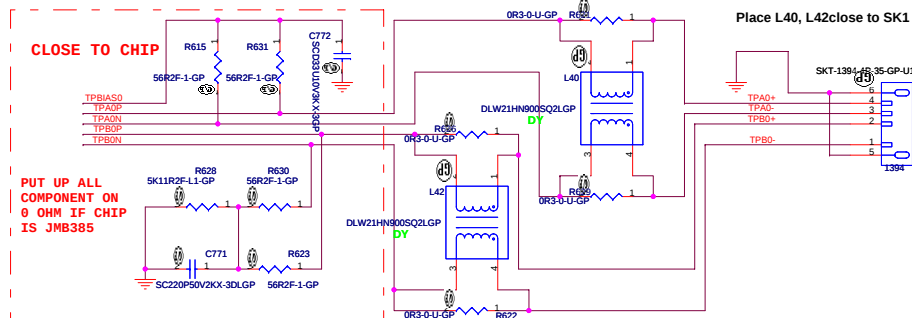
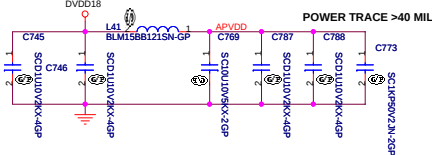
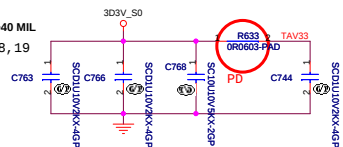
WWAN1



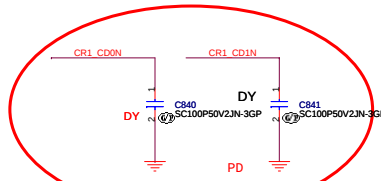
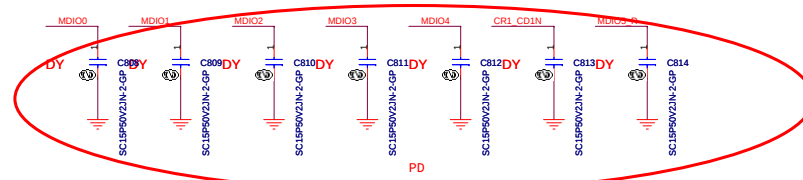
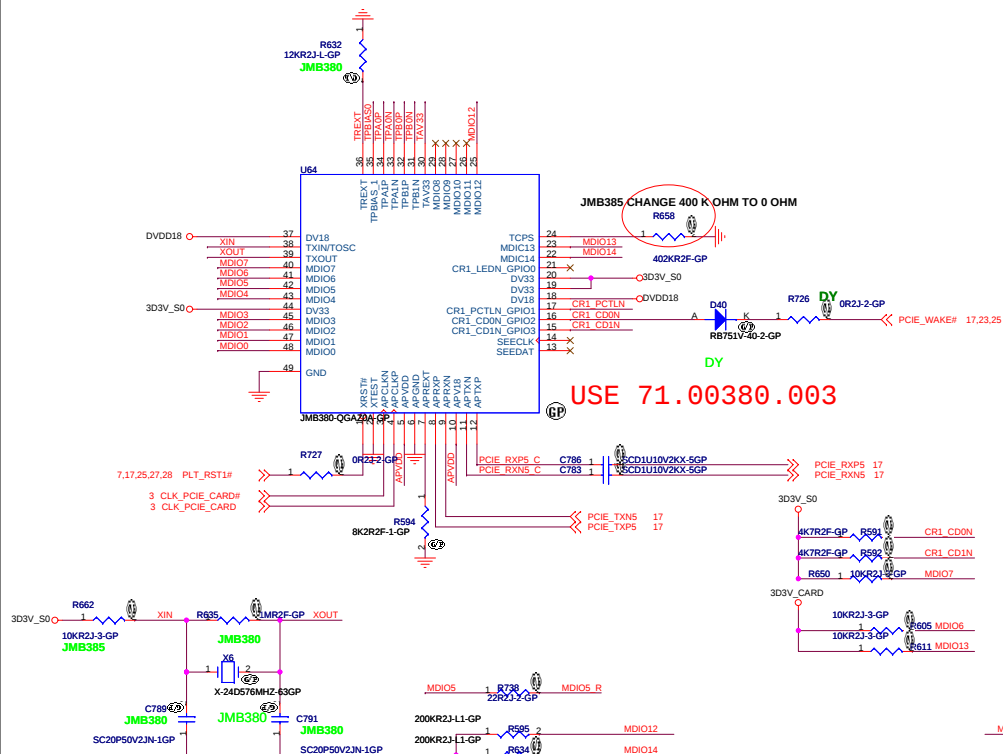
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|                           |                        |  |                |
|---------------------------|------------------------|--|----------------|
| Title                     |                        |  |                |
| <b>Mini Card/New Card</b> |                        |  |                |
| Size                      | Document Number        |  | Rev            |
|                           | <b>D45/D46</b>         |  | <b>PI</b>      |
| Date:                     | Monday, March 24, 2008 |  | Sheet 25 of 47 |

POWER TRACE >40 MIL  
Close to Pin 18,19



MS / MS PRO  
SD / MMC



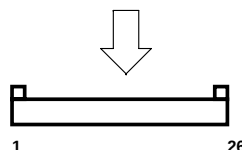
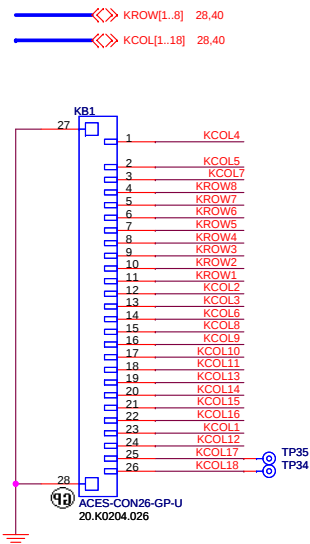
緯創資通 Wistron Corporation  
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh,  
Taipai Hsien 221, Taiwan, R.O.C.

Title USB Card Reader JM380

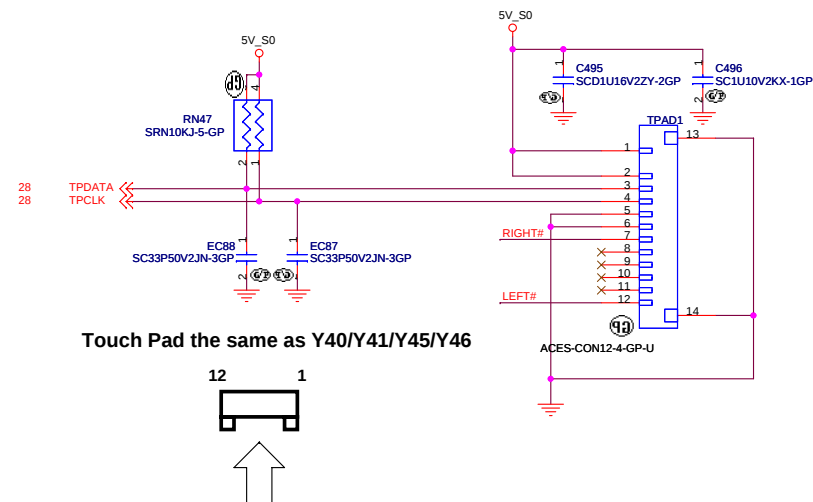
Size Custom Document Number Rev PD

Date: Monday, March 24, 2008 Sheet 26 of 47

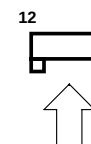
## Internal KeyBoard Connector



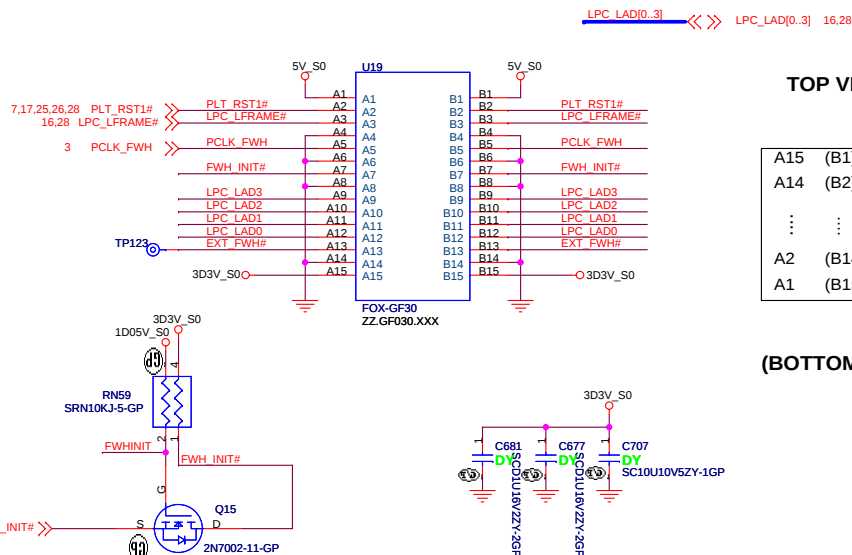
## TouchPad Connector



Touch Pad the same as Y40/Y41/Y45/Y46



## GOLDEN FINGER FOR DEBUG BOARD

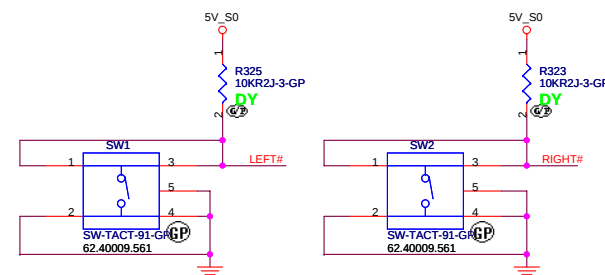


TOP VIEW

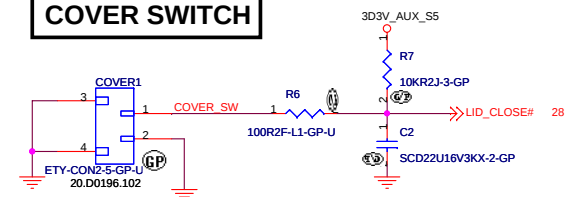
A15 (B1)  
A14 (B2)  
:  
:  
A2 (B14)  
A1 (B15)

(BOTTOM VIEW)

## 15" TOUCHPAD BUTTON SWITCH



## COVER SWITCH



ZZZZ

|                            |                         |                                                                               |          |
|----------------------------|-------------------------|-------------------------------------------------------------------------------|----------|
| <b>緯創資通</b>                |                         | <b>Wistron Corporation</b>                                                    |          |
|                            |                         | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title                      |                         |                                                                               |          |
| <b>KeyBoard/TPAD/Debug</b> |                         |                                                                               |          |
| Size                       | Document Number         | Rev                                                                           |          |
| Custom                     | <b>D45/D46</b>          | <b>PD</b>                                                                     |          |
| Date:                      | Tuesday, March 25, 2008 | Sheet                                                                         | 27 of 47 |

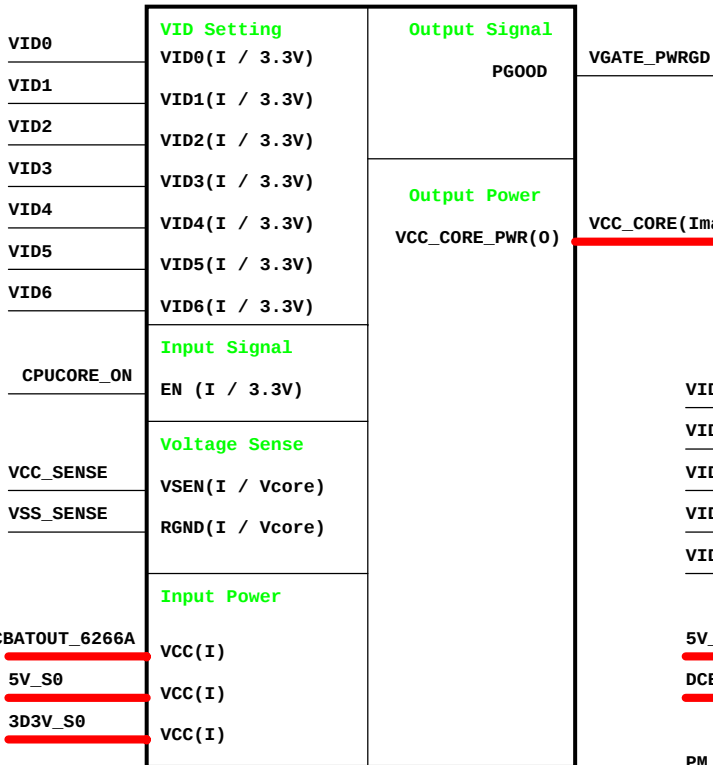




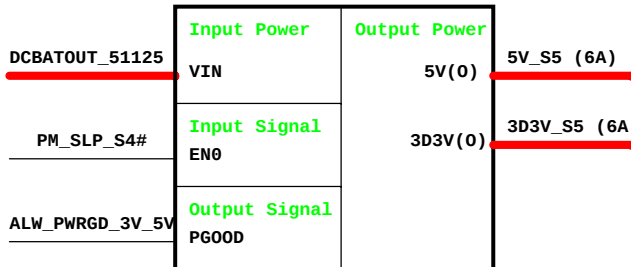
**緯創資通** **Wistron Corporation**  
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|       |                        |                |       |                                         |    |     |   |
|-------|------------------------|----------------|-------|-----------------------------------------|----|-----|---|
| Title |                        |                |       | <b><i>RUN POWER and 3D3V_AUX_S5</i></b> |    |     |   |
| Size  | Document Number        |                |       |                                         |    | Rev | P |
|       |                        | <b>D45/D46</b> |       |                                         |    |     |   |
| Date: | Friday, March 14, 2008 |                | Sheet | 30                                      | of | 47  |   |

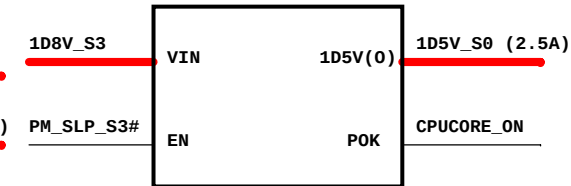
CPU\_CORE  
ISL6266A



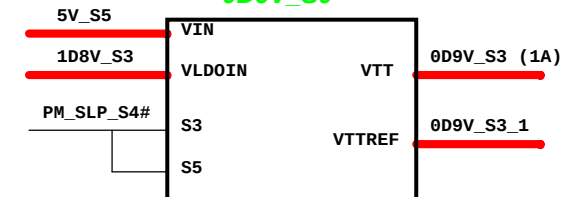
TPS51125  
5V/3D3V



APL5912  
1D5V\_S0



0D9V\_S0



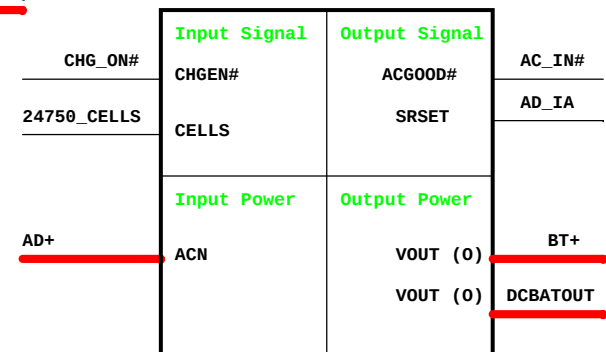
TPS51100

2D5V\_S0

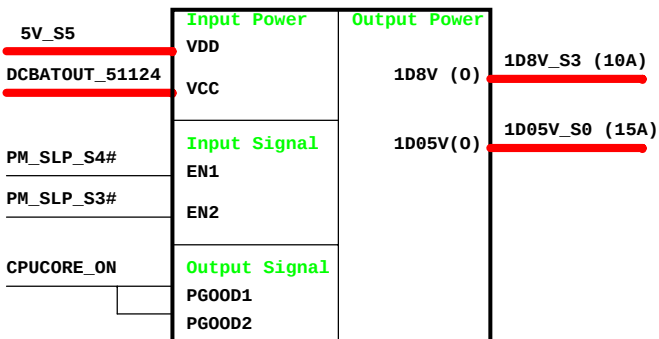


APL5913

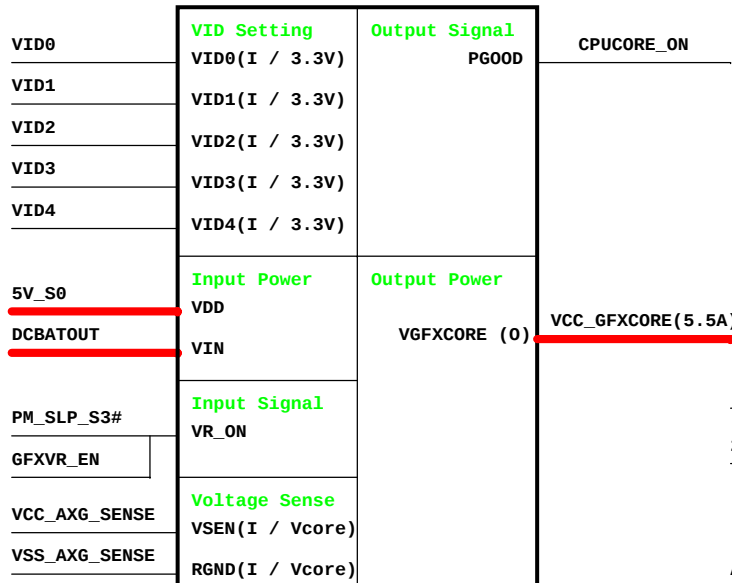
Charger BQ24750



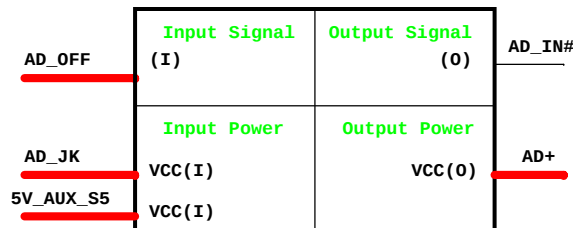
TPS51124  
1D8V/1D05V



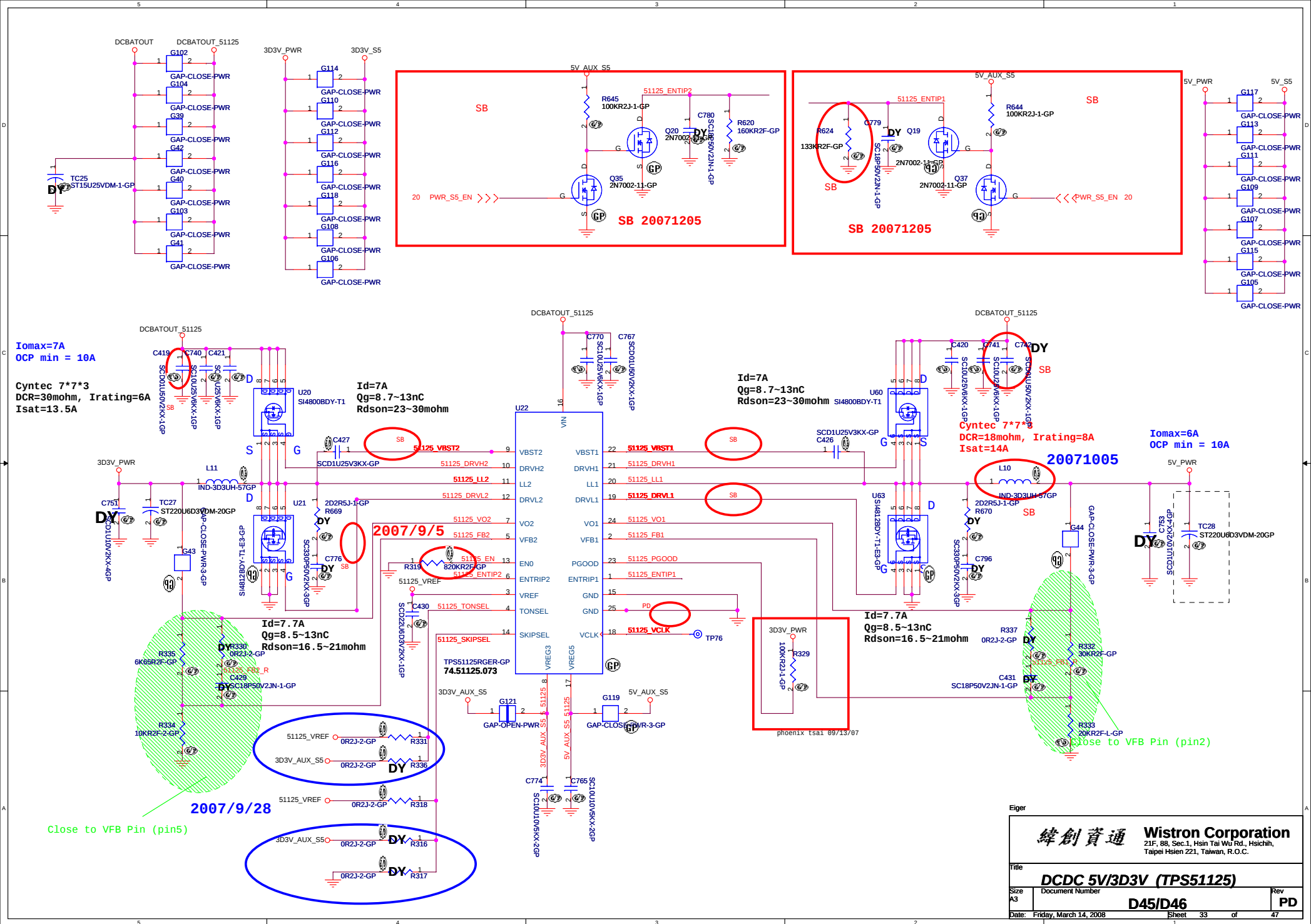
GFX\_CORE  
ISL6263A



Adapter

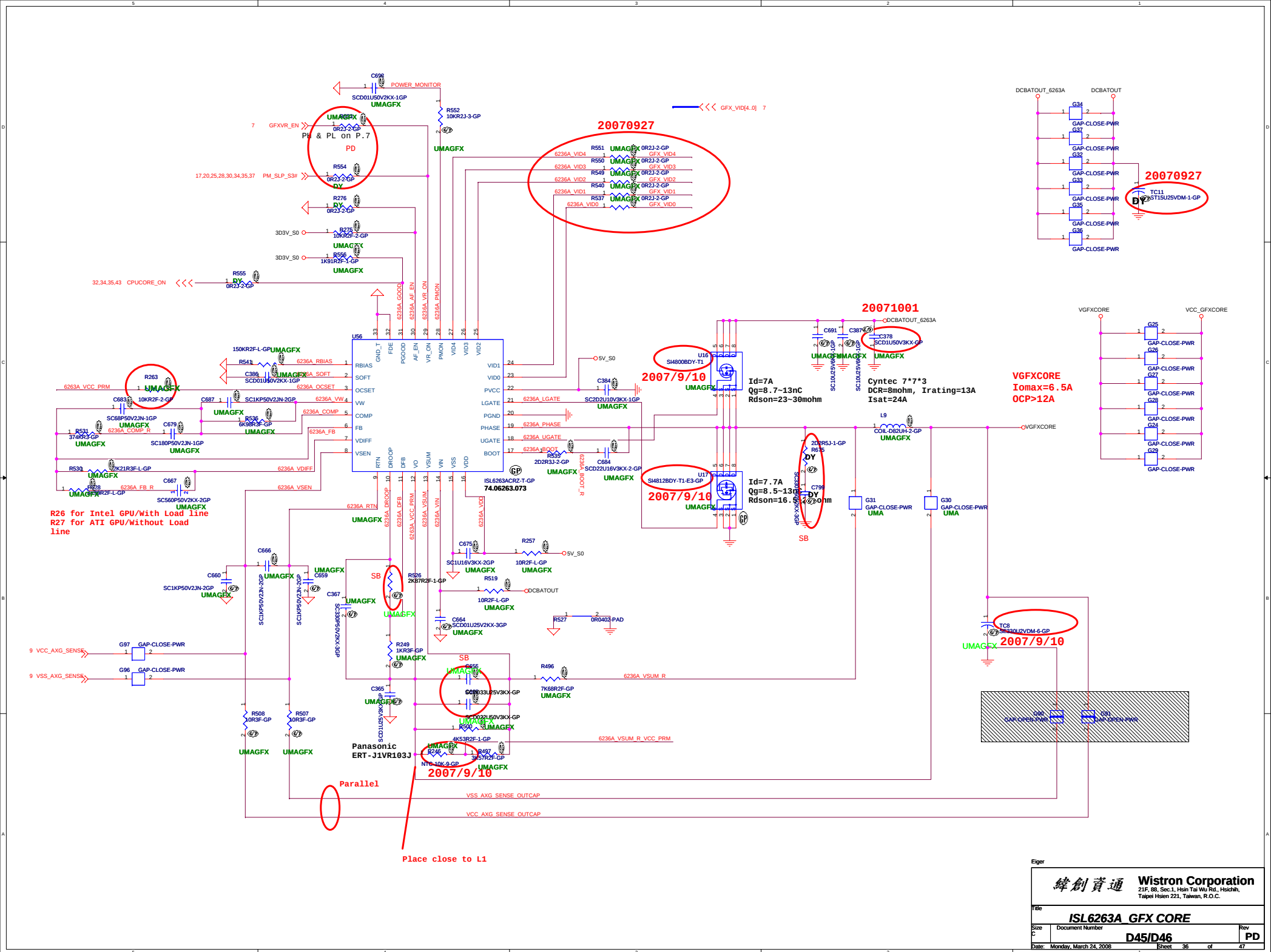


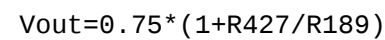
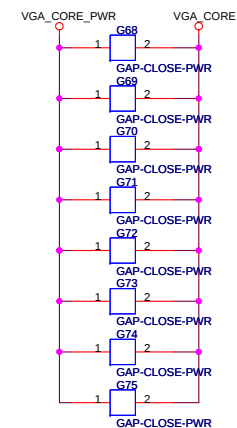


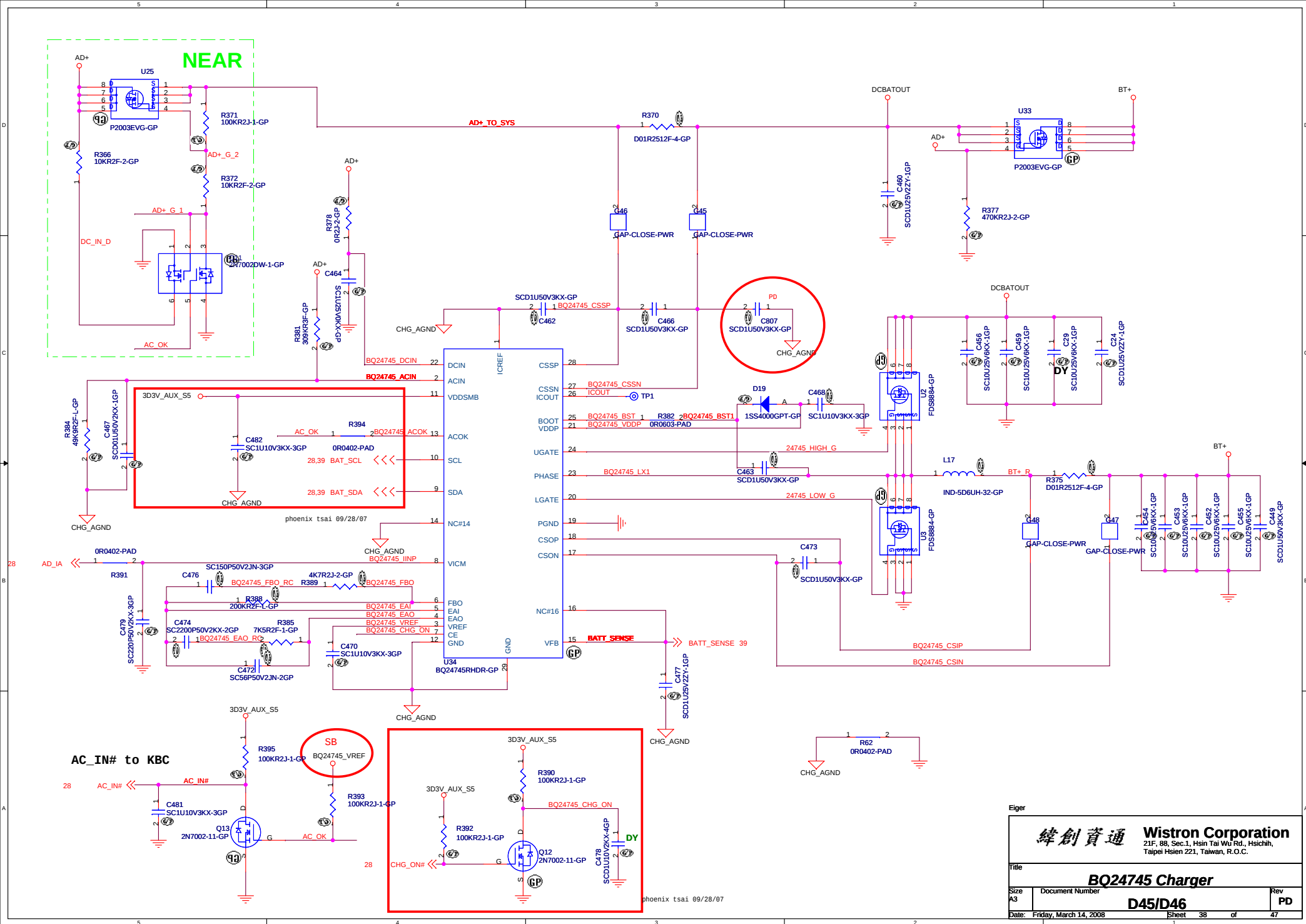




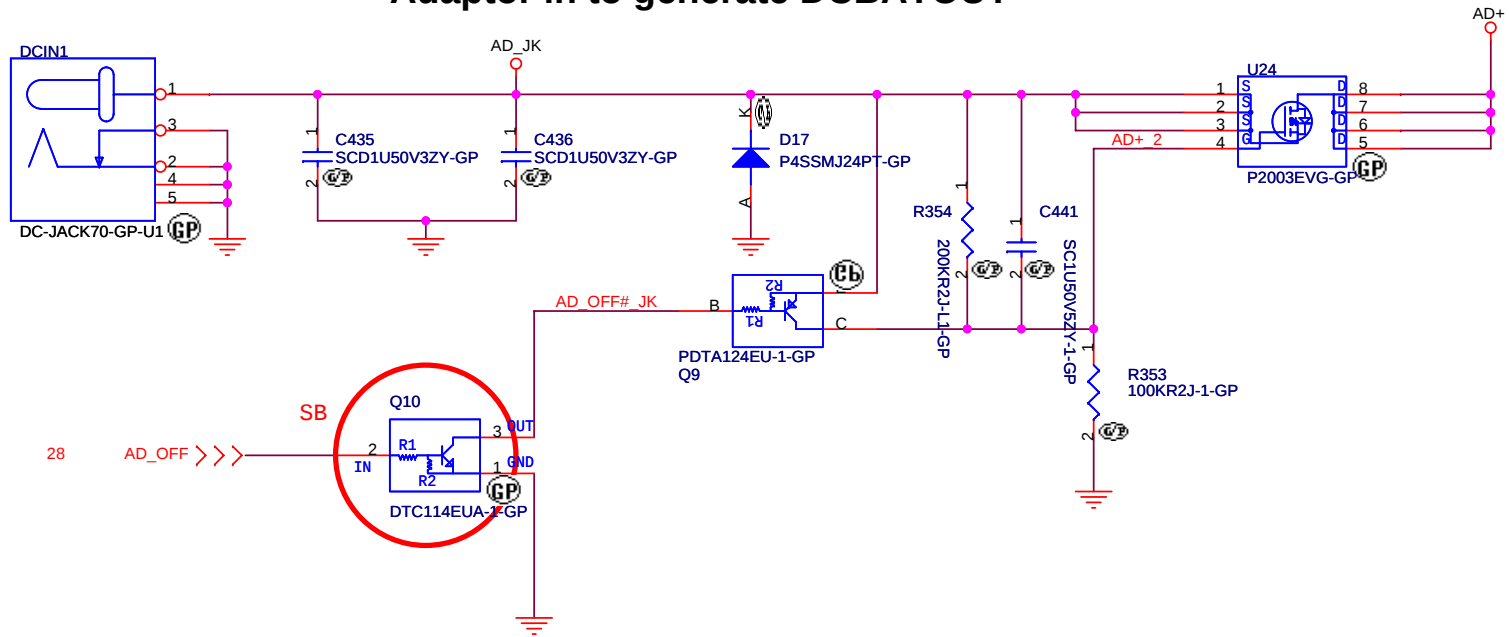




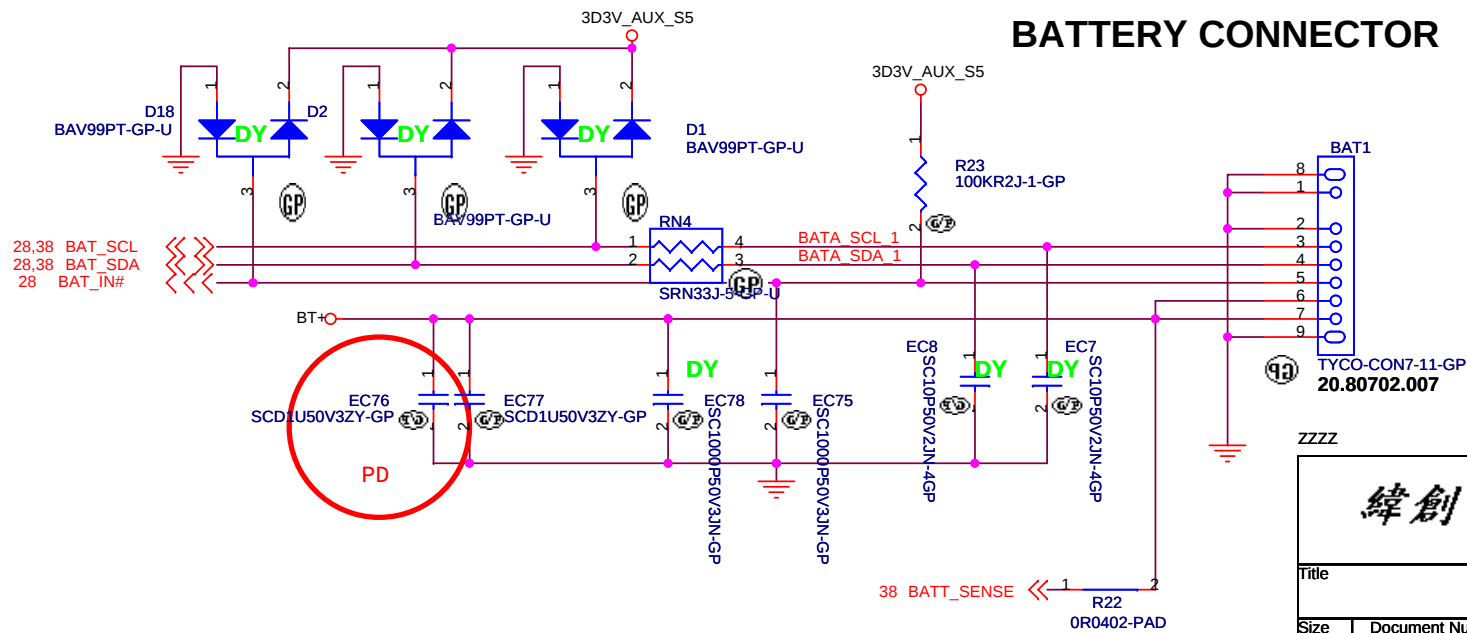




## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



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Title

**AD/BATT CONN**

Size

Document Number

**D45/D46**

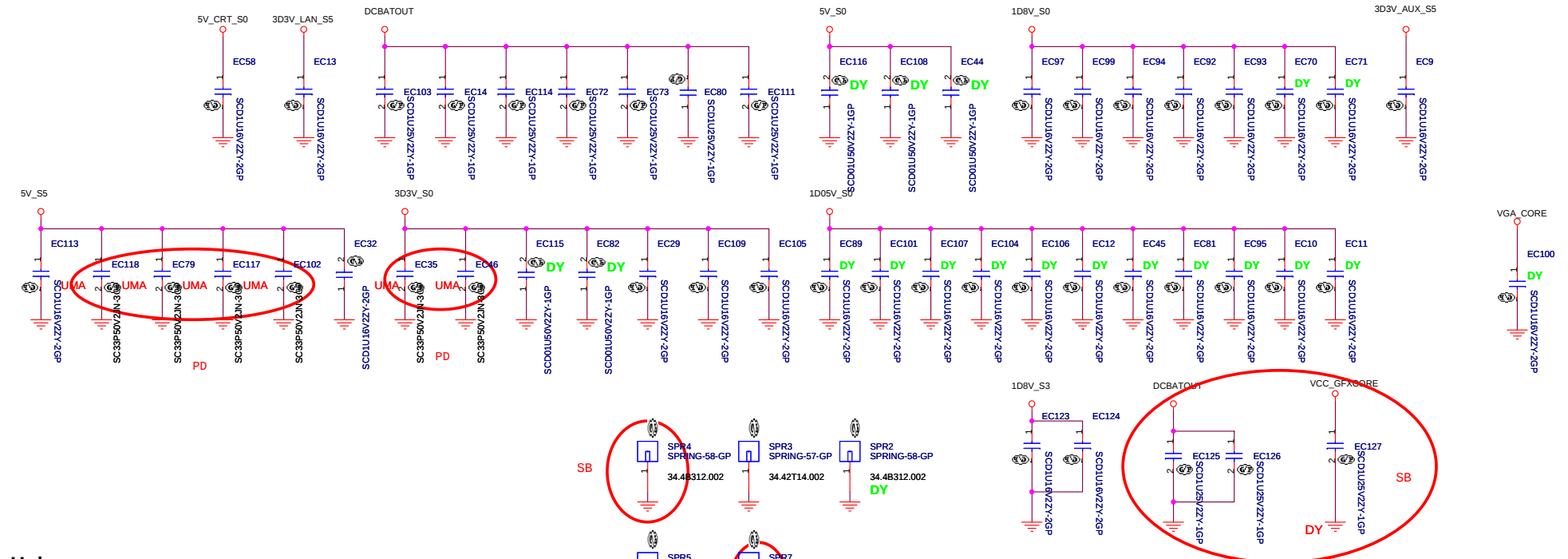
Rev

**PD**

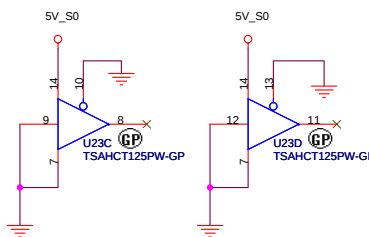
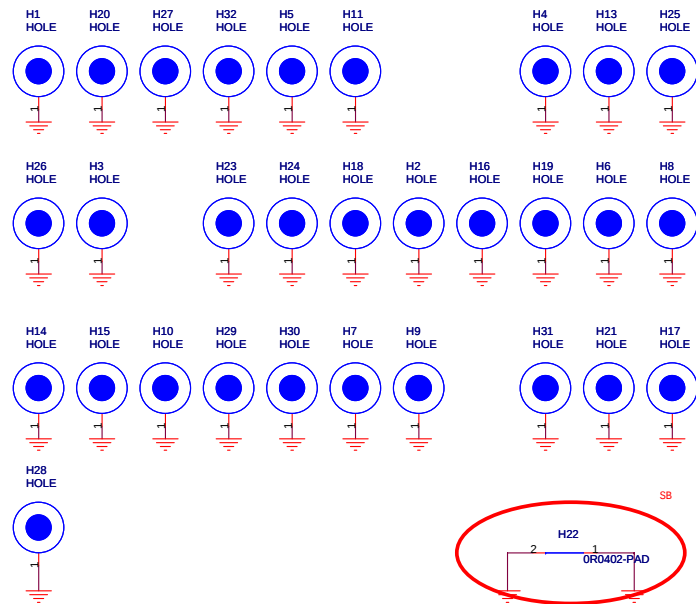
Date: Monday, March 24, 2008

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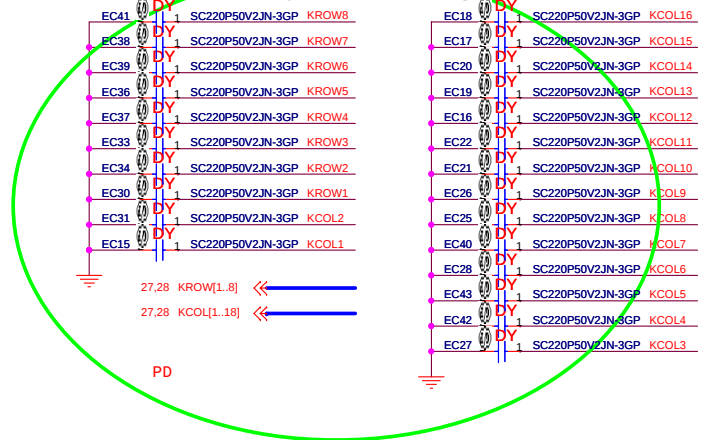
## EMI Caps



## Holes

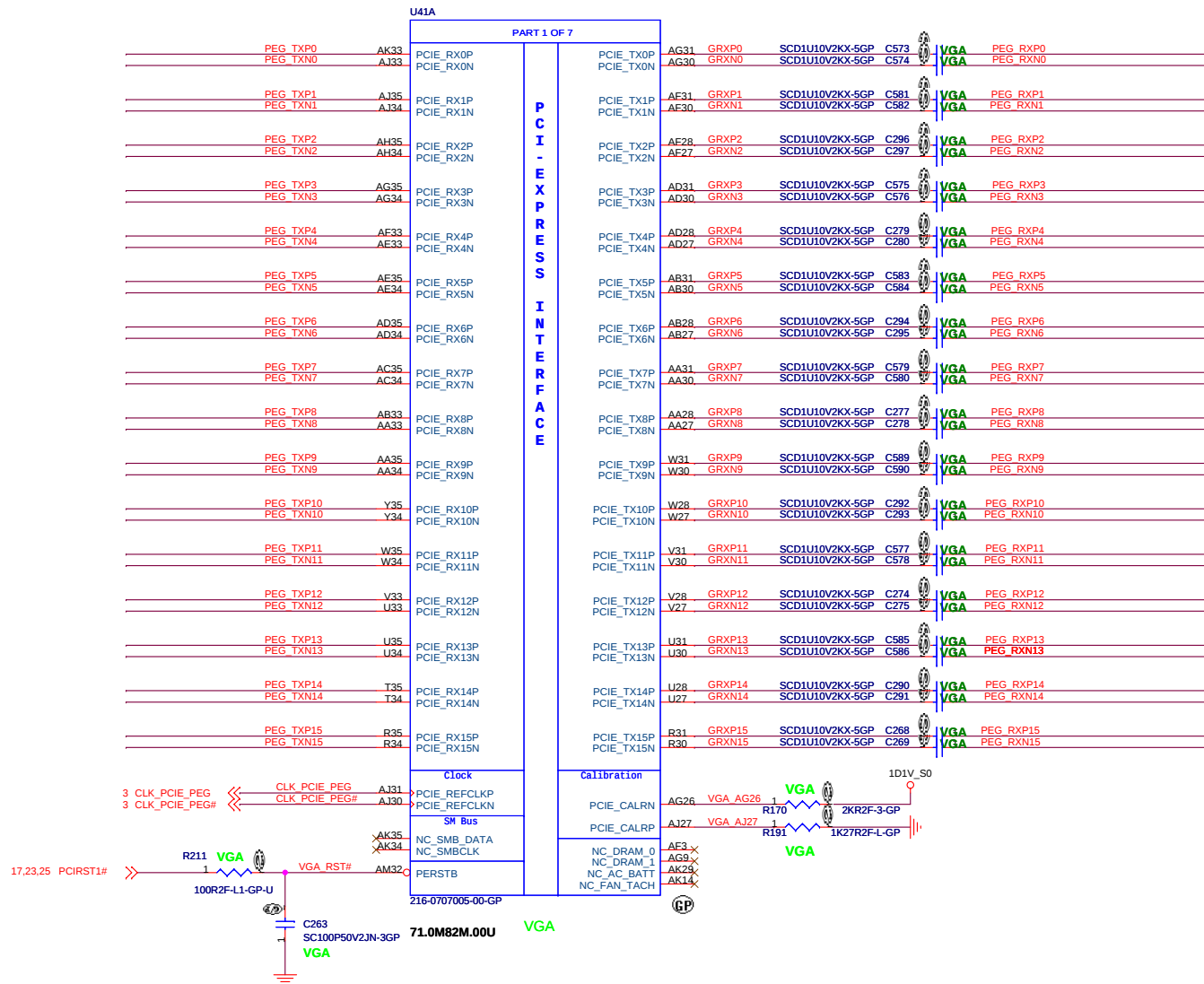


## Keyboard EMI Caps



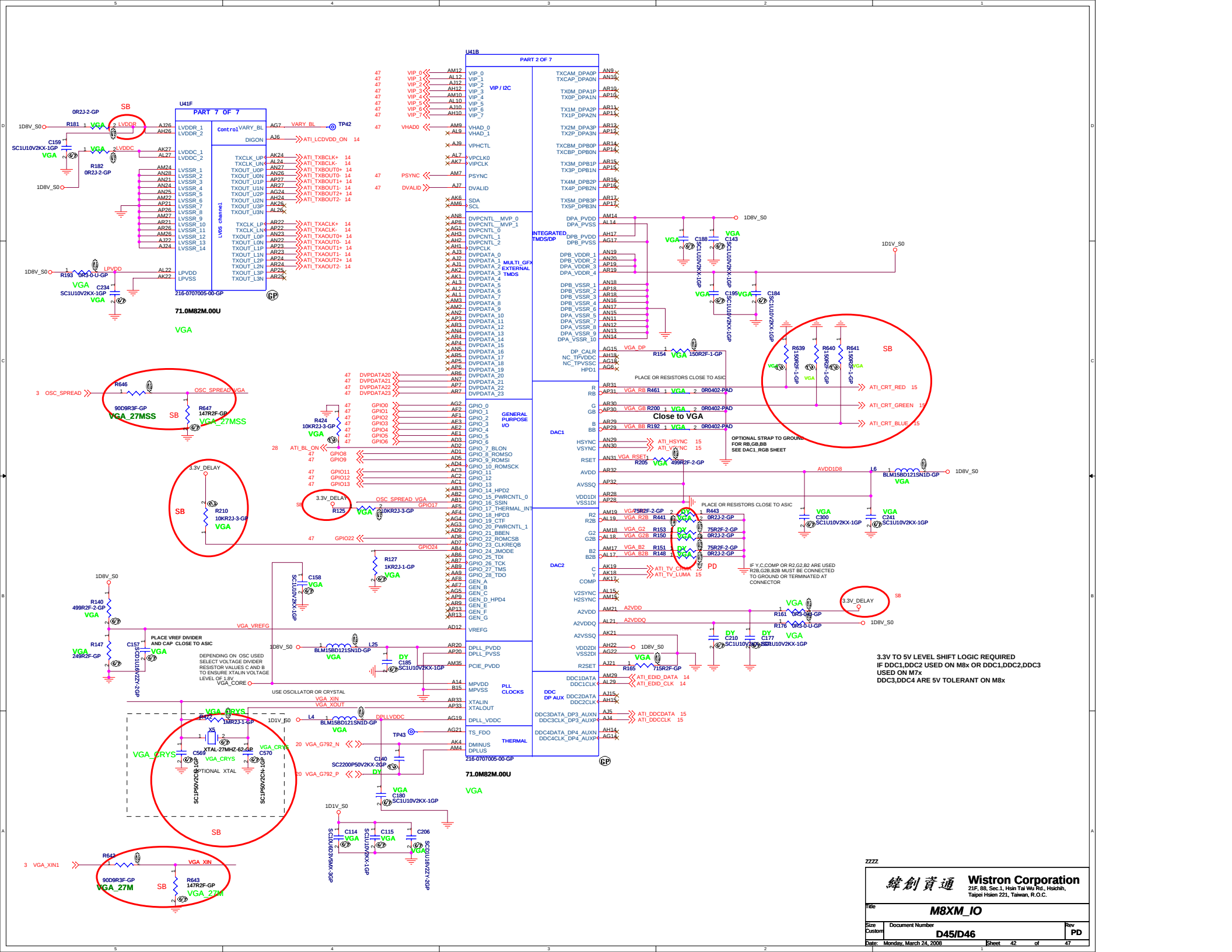
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|  <b>緯創資通</b><br>21F, No. 1, Hsien Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                        | <b>Wistron Corporation</b><br>21F, No. 1, Hsien Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title                                                                                                                                                                           |                        |                                                                                                          |          |
| <b>EMI/Spring/Boss</b>                                                                                                                                                          |                        |                                                                                                          |          |
| Size                                                                                                                                                                            | Document Number        | Rev                                                                                                      |          |
| <b>D45/D46</b>                                                                                                                                                                  |                        | <b>PD</b>                                                                                                |          |
| Date:                                                                                                                                                                           | Monday, March 17, 2008 | Sheet                                                                                                    | 40 of 47 |

7 PEG\_RXP[15..0] << PEG\_RXP[15..0]  
7 PEG\_RXN[15..0] << PEG\_RXN[15..0]  
7 PEG\_TXP[15..0] << PEG\_TXP[15..0]  
7 PEG\_TXN[15..0] << PEG\_TXN[15..0]



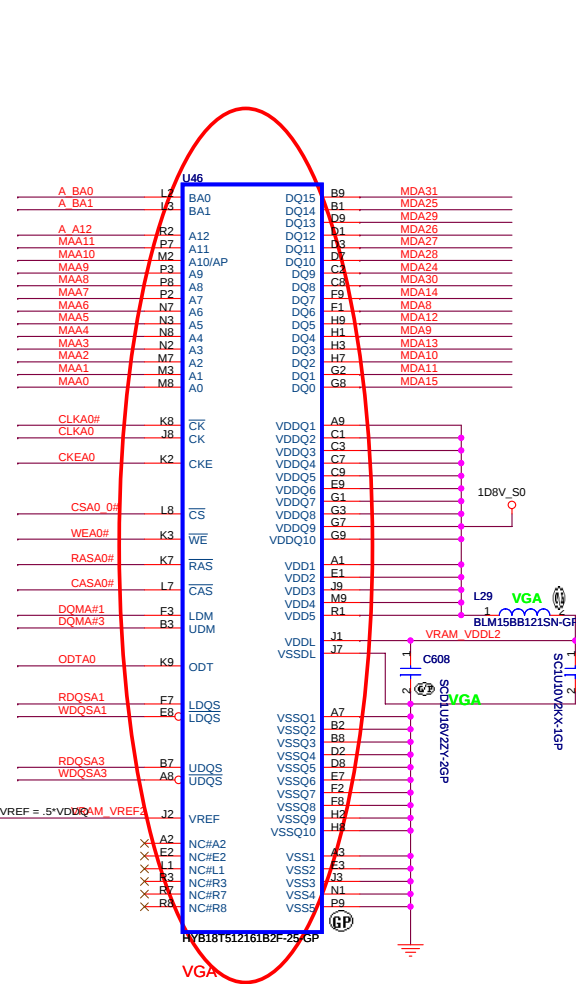
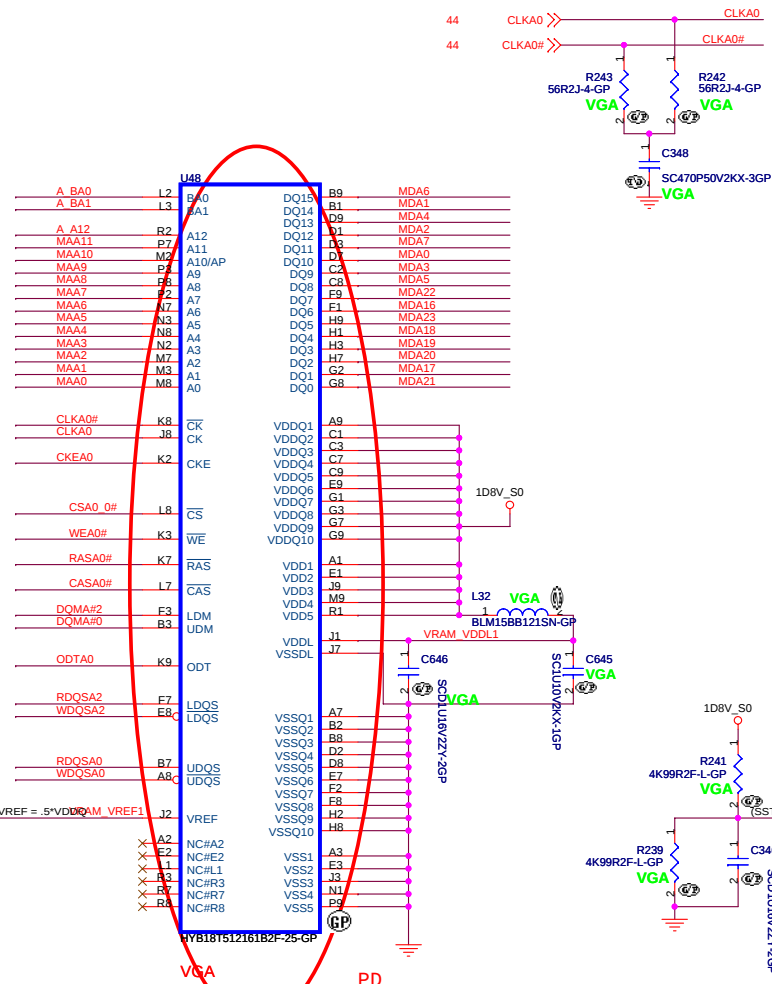
7777

|                                                                            |                        |                     |          |
|----------------------------------------------------------------------------|------------------------|---------------------|----------|
| 緯創資通                                                                       |                        | Wistron Corporation |          |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                        |                     |          |
| Title                                                                      |                        |                     |          |
| M8XM PCIE                                                                  |                        |                     |          |
| Size                                                                       | Document Number        | Rev                 | PD       |
| D45/D46                                                                    |                        |                     |          |
| Date:                                                                      | Friday, March 14, 2008 | Sheet               | 41 of 47 |

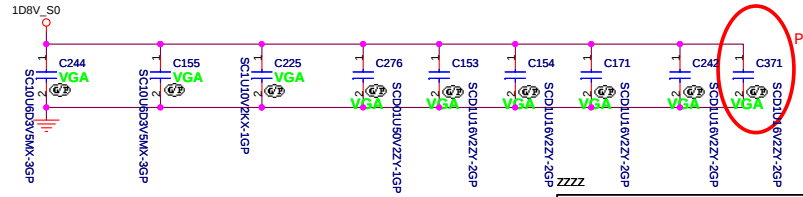
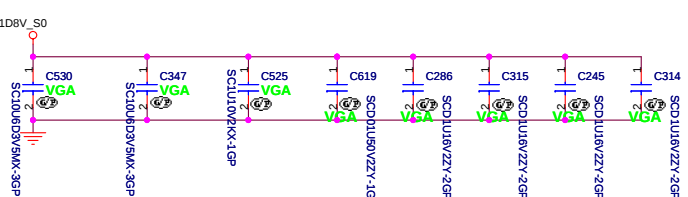


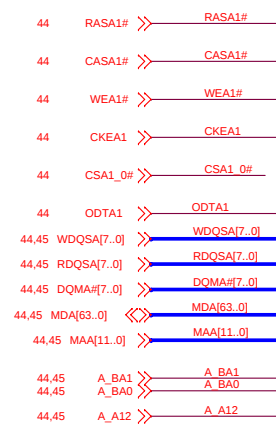
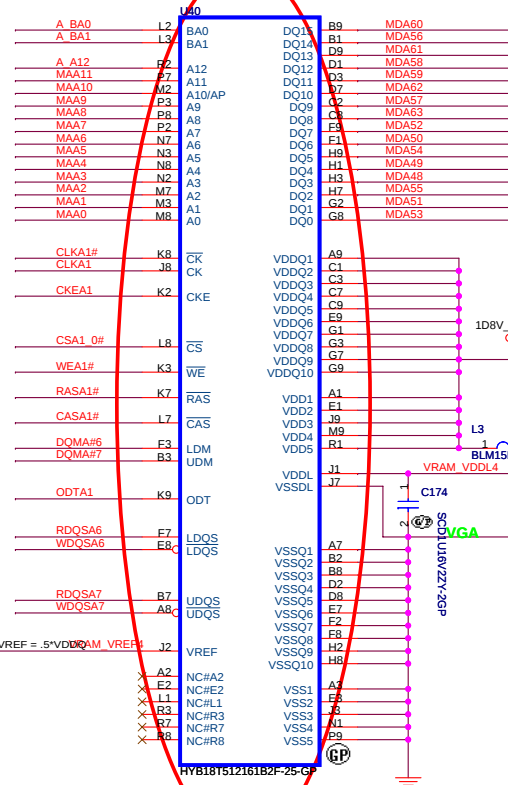
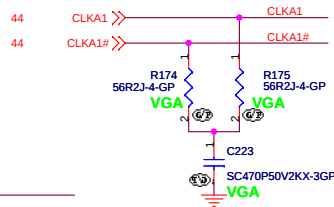
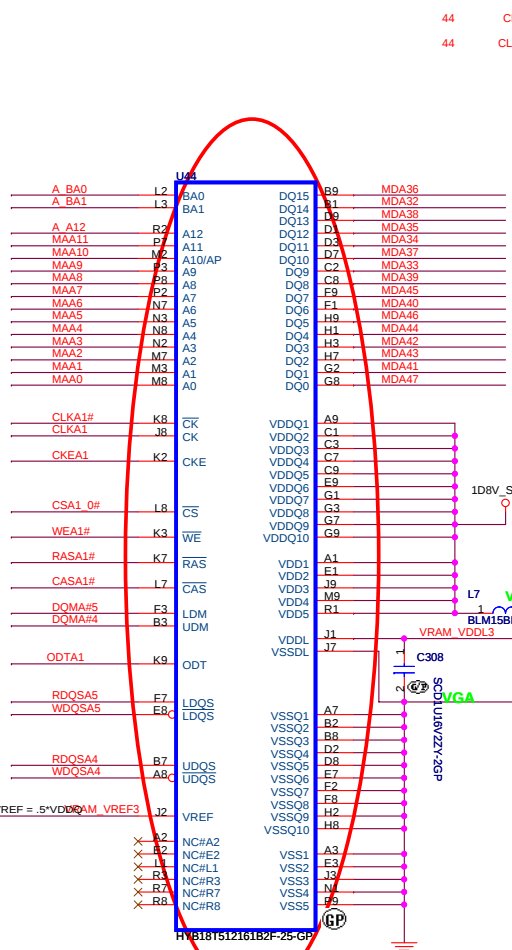




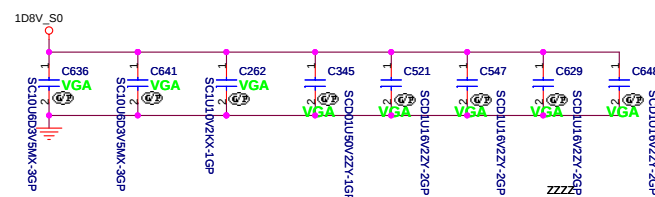
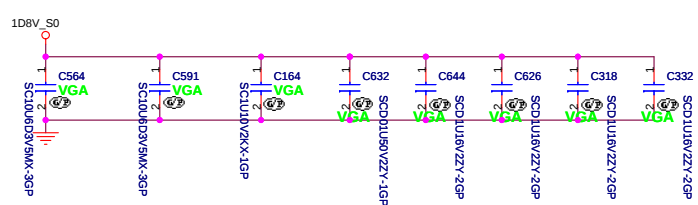


- 44 RAS0# >> RAS0#
- 44 CAS0# >> CAS0#
- 44 WEA0# >> WEA0#
- 44 CKEA0 >> CKEA0
- 44 CSA0\_0# >> CSA0\_0#
- 44 ODTA0 >> ODTA0
- 44.46 WDQSA[7..0] >> WDQSA[7..0]
- 44.46 RDQSA[7..0] >> RDQSA[7..0]
- 44.46 DQMA[7..0] >> DQMA[7..0]
- 44.46 MDA[63..0] >> MDA[63..0]
- 44.46 MAA[11..0] >> MAA[11..0]
- 44.46 A\_BA1 >> A\_BA1
- 44.46 A\_BA0 >> A\_BA0
- 44.46 A\_A12 >> A\_A12





2nd source 72.55162.00U



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Title

VRAM DDR2 B

Size

A3

Document Number

D45/D46

Rev

PD

Date

Monday, March 24, 2008

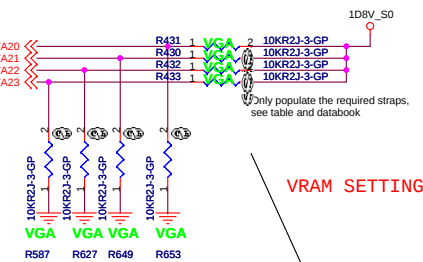
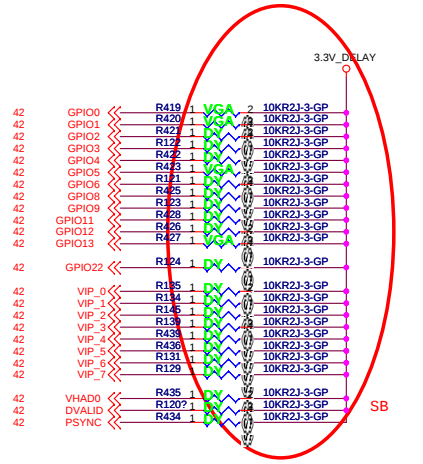
Sheet

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of

47

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M  
Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X



| CONFIGURATION STRAPS                                                                                    |                                                                                           |                                                 | RECOMMENDED SETTINGS                                                                                                                            |         |
|---------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET |                                                                                           |                                                 | 0= DO NOT INSTALL RESISTOR<br>1= INSTALL 10K RESISTOR<br>X = DESIGN DEPENDANT<br>NA = NOT APPLICABLE<br>RSVD = ATI RESERVED<br>(DO NOT INSTALL) |         |
| STRAPS                                                                                                  | PIN                                                                                       | DESCRIPTION OF DEFAULT SETTINGS                 | M8x                                                                                                                                             | M7x     |
| BIF_MSI_DIS                                                                                             | VIP1                                                                                      | MESSAGE SIGNAL INTERRUPT ENABLED                | NA                                                                                                                                              | 0       |
| BIF_AUDIO_EN                                                                                            | VIP3                                                                                      | ENABLE HD AUDIO (M7XM and M86M ONLY) Note:1     | X                                                                                                                                               | X       |
| BIF_64BAR_EN_A                                                                                          | VIP5                                                                                      | 64 BIT BARS DISABLED                            | NA                                                                                                                                              | 0       |
| TX_PWRS_ENB                                                                                             | GPIO0                                                                                     | PCIE FULL TX OUTPUT SWING                       | X                                                                                                                                               | X       |
| TX_DEEMPH_EN                                                                                            | GPIO1                                                                                     | PCIE TRANSMITTER DE-EMPHASIS ENABLED            | X                                                                                                                                               | X       |
| BIF_DEBUG_ACCESS                                                                                        | GPIO4                                                                                     | DEBUG SIGNALS MUXED OUT                         | 0                                                                                                                                               | 0       |
| BIF_AUDIO_EN                                                                                            | GPIO8                                                                                     | ENABLE HD AUDIO (M82M ONLY) Note:2              | X                                                                                                                                               | RSVD    |
| BIF_GEN2_EN_A                                                                                           | GPIO5                                                                                     | Allows either PCIe 2.5GT/s or 5.0GT/s operation | X                                                                                                                                               | 0       |
| BIOS_ROM_EN                                                                                             | GPIO_22_ROMCSB                                                                            | DISABLE EXTERNAL BIOS ROM                       | NA                                                                                                                                              | X       |
| ROMIDCFG(3:0)                                                                                           | GPIO[13:11,9]                                                                             | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT  | XX X X                                                                                                                                          | X X X X |
| VIP_DEVICE_STRAP_ENA                                                                                    | VSYN                                                                                      | IGNORE VIP DEVICE STRAPS                        | 0                                                                                                                                               | 0       |
| BIF_VGA_DIS                                                                                             | PSYN                                                                                      | VGA ENABLED                                     | 0                                                                                                                                               | 0       |
| BIF_HDMI_EN                                                                                             | HSYN                                                                                      | HDMI ENABLE (SEE NOTE 2)                        | X                                                                                                                                               | X       |
| DEBUG_I2C_ENABLE                                                                                        | GPIO6                                                                                     | Internal use only                               | 0                                                                                                                                               | 0       |
| MEM_TYPE                                                                                                | ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN | MEMORY TYPE,MAKE AND SIZE INFO                  | X X X X                                                                                                                                         | X X X X |

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

| ATI RESERVED CONFIGURATION STRAPS                                                                              |      |          |      |              |      |       |       |        |  |
|----------------------------------------------------------------------------------------------------------------|------|----------|------|--------------|------|-------|-------|--------|--|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET        |      |          |      |              |      |       |       |        |  |
| VHAD0                                                                                                          | VIP0 | VIP2     | VIP4 | VIP6         | VIP7 | GPIO2 | GPIO3 | H2SYNC |  |
| PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET |      |          |      |              |      |       |       |        |  |
| GPIO_28_TDO                                                                                                    |      | GENERICC |      | GPIO21_BB_EN |      |       |       |        |  |

For Hynix 上R431,R430,R432,R433 (63.10334.1DL)  
Delete R587,R627,R649,R653  
For Qimonda 上R431,R430,R432,R587 (63.10334.1DL)  
Delete R433,R627,R649,R653  
For Samsung 上R431,R430,R627,R433 (63.10334.1DL)  
Delete R587,R432,R649,R653

|           |   |                         |
|-----------|---|-------------------------|
| DVPDATA20 | 1 |                         |
| DVPDATA21 | 1 | HY5PS121621CFP-25 Hynix |
| DVPDATA22 | 1 | 72.51216.F0U            |
| DVPDATA23 | 1 |                         |

|           |   |                            |
|-----------|---|----------------------------|
| DVPDATA20 | 1 |                            |
| DVPDATA21 | 1 | HYB18T512161B2F-25 Qimonda |
| DVPDATA22 | 1 | 72.18512.M0U               |
| DVPDATA23 | 0 |                            |

|           |   |                         |
|-----------|---|-------------------------|
| DVPDATA20 | 1 |                         |
| DVPDATA21 | 1 | K4N51163QE-ZC25 SamSung |
| DVPDATA22 | 0 | 72.45116.A0U            |
| DVPDATA23 | 1 |                         |

|           |   |                       |
|-----------|---|-----------------------|
| DVPDATA20 | 1 |                       |
| DVPDATA21 | 1 | H5PS5162FFR-25C HYNIX |
| DVPDATA22 | 0 |                       |
| DVPDATA23 | 0 | 72.55162.00U          |

|                                                 |                                                                                                                                                                                                                                                                                                   |                                                |
|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|
| 手動改D45 BOM U43 71.CNTIG.H0U<br>U57 71.ICH9M.E0U | 手動改共同BOM<br>DM2 62.10017.G31<br>U49 84.04634.037<br>U15 84.08896.037<br>H29 34.4B417.001<br>H30 34.4B417.001<br>H27 34.4F403.001<br>H31 34.4F403.001<br>H7 34.4F403.001<br>H9 34.4F403.001<br>H10 34.4G501.001<br><br>U11 71.00773.00G<br>U64 71.00380.003<br>U35 62.10053.401<br>U7 71.08111.E03 | 手動改NET<br>DM2 62.10017.G31<br>U35 62.10053.401 |
| R186,187,188,198,201,202-> 63.R0034.1DL         |                                                                                                                                                                                                                                                                                                   |                                                |
| D45 VRAM SELECT                                 |                                                                                                                                                                                                                                                                                                   |                                                |
| 手動改D46 BOM U43 71.CNTIG.G0U<br>U57 71.ICH9M.E0U |                                                                                                                                                                                                                                                                                                   |                                                |