GIGABYTE GA-K8U-939 Schematics

REV:1.0

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19,20	PCI SLOT 1,2,3,4,5
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34	R_USB , RESET
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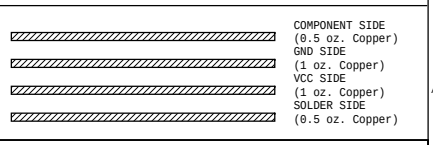
SHEET	TITLE



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Title: COVER SHEET

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Component value change history

Date	Change Item	Reason
94/02/05	R255 change to 47K/6 , R256 change to 49.9K/6/1 , C304 change to 2.2U/6/y/6.3v	com port loop back tool cause RI power on when power off
94/02/25	DR30 change to 15.4K/6/1 DR24,DR11 change to 2.4K/6/1	For the Vcore loadline finetune
94/03/25	Remove R299,Q33,RN84,R296,Q31,Q32,EC54 Add R297 0/6	For the CPU FAN alwass keep max speed,even boot fail
94/03/25	Remove EC42	SATA realibility can be fixed by BIOS , EC42 can be remove.
94/03/25	Add R455 0/6	To fix the ULI M1689 thermaltrip# function fail as boot fail .
94/03/25	Remove EC43 , add EC61	Remove EC43 , add EC61 to reduce 3VSTR ripple
94/03/25	RN95,RN96,RN97,RN98,RN99,RN100,RN101,RN102 RN103,RN104,RN105,RN106,RN107,RN108,RN109 RN110,RN111,RN112,RN113,RN114, RN115,RN116 RN117,RN118,RN119,RN120,RN121,RN122,RN123 RN124,RN125,RN126,RN127,RN128,RN129,RN130 RN131,RN132,RN133,RN134, RN135,RN136, RN137,RN138,RN139,RN140,RN141,RN142,RN143 RN144,RN145,RN146,RN147,RN148,RN149 RN150,RN151,RN152	change to 56 ohm from 47 ohm for the compability
94/04/25	DR11 , DR24 change to 4.99K/6/1 , DR30 change to 10k/6/1 , DR29 change to 3K/6/1, DC8 change to 100pf	For CPU PWM fine tune
94/04/25	Remove DR28	For CPU PWM fine tune
94/04/25	U1 change to FSB 1GHz from FSB 800MHz	Form 3800+ CG in high temperature burn in issue

ULi M1689 single chip FOR AMD K8_939

Circuit or PCB layout change for next version

Date	Change Item	Reason
94/03/25	Remove C271	
94/03/25	Remove U17,R374,R373,R414 ,R376,R375,C281,Q71,URN1	For realibility ,Saving space for DDRVTT to CPU by reduce the reverse power sequence circuit.
94/03/25	Add R455	Connect -RSMRST to -THRMTRIP_NB by R455 to fix the M1689 thermtrip issue
94/03/25	Add EC61 1000u/6.3V footprint , colay with EC43	Reverse for the 25VSTR & DDRVTT for higher CPU to reduce ripple.
	.	

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Title: BOM & PCB MODIFY HISTORY

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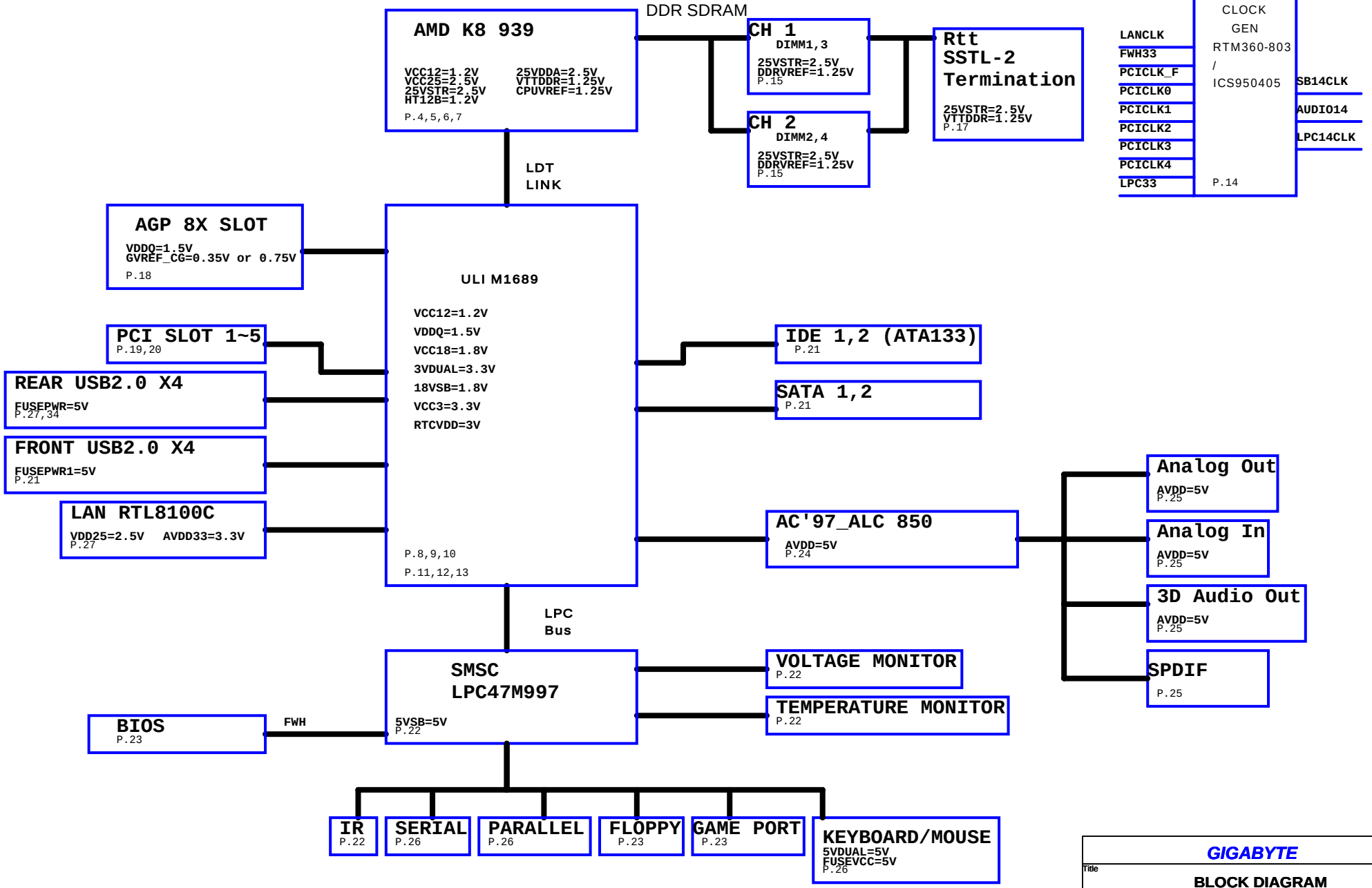
GA-K8U-939 BLOCK DIAGRAM

System Block Diagram



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Title	BLOCK DIAGRAM	
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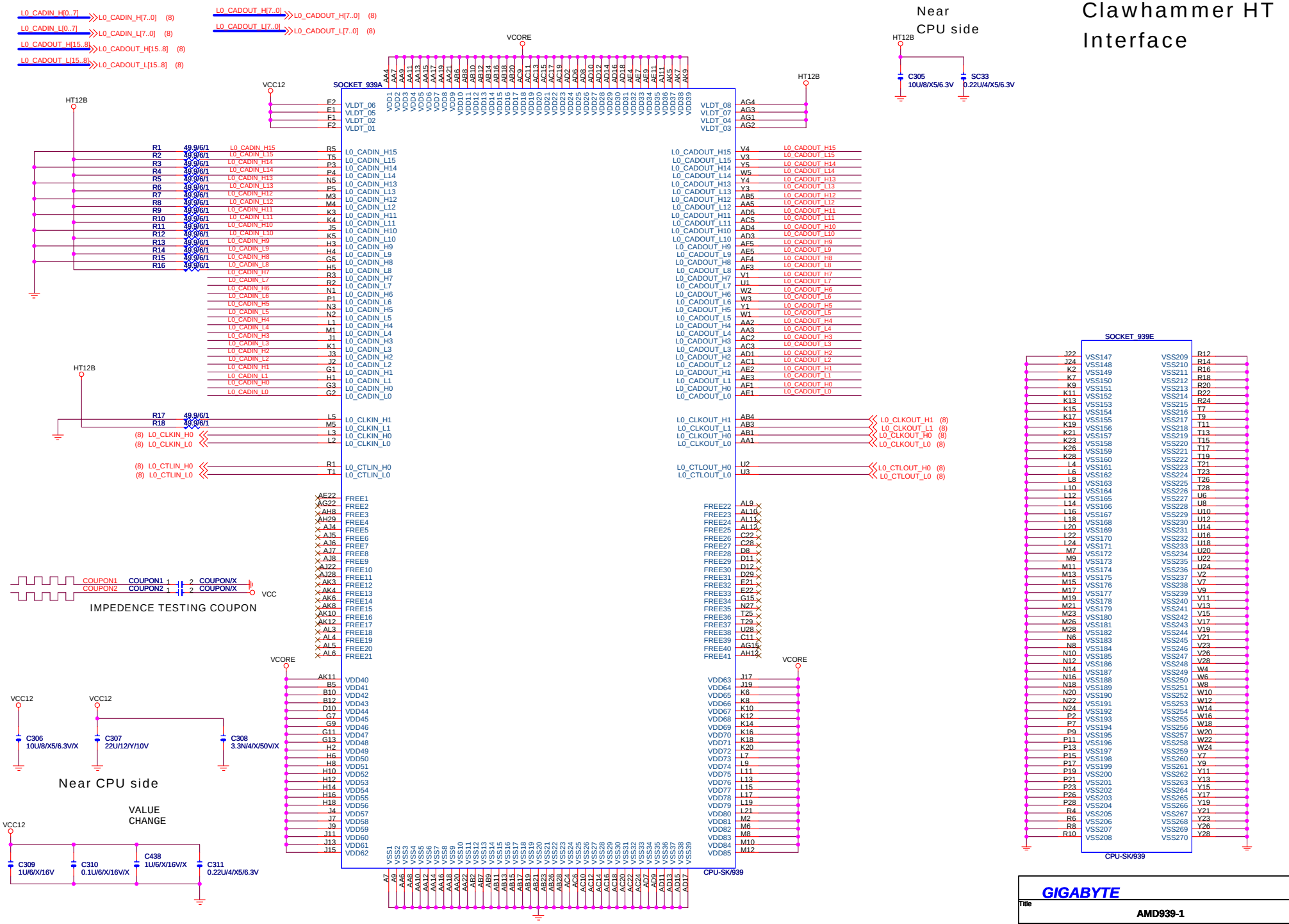
Clawhammer HT Interface



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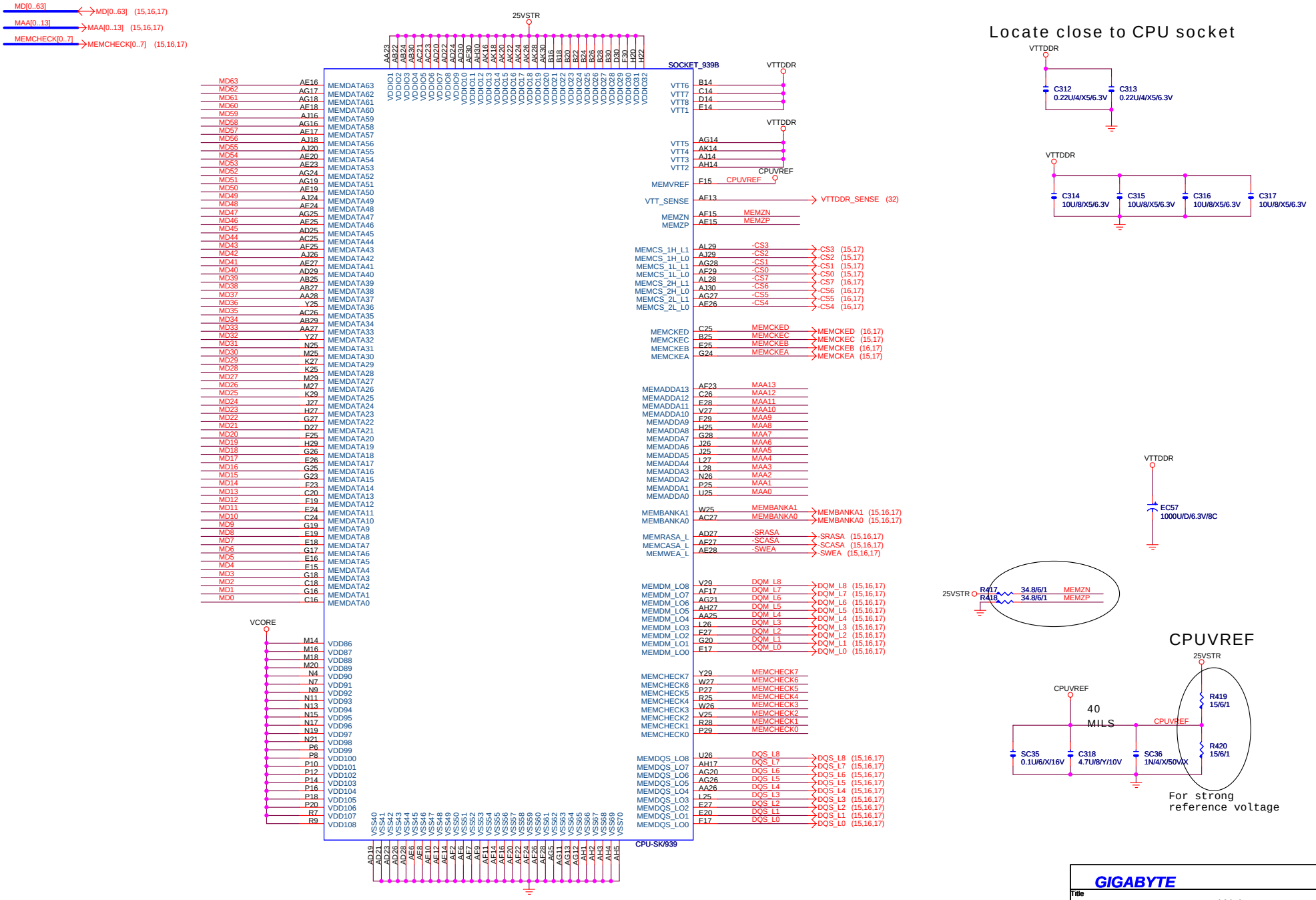
MD[0..63]
MD[0..63] (15,16,17)
MAA[0..13]
MAA[0..13] (15,16,17)
MEMCHECK[0..7]
MEMCHECK[0..7] (15,16,17)
25VSTR
SOCKET_939B
CPU-SK/939
VCORE
VTTDDR
CPUVREF
VTTDDR_SENSE (32)
Locate close to CPU socket
C312 0.22U/4/X5/6.3V
C313 0.22U/4/X5/6.3V
C314 10U/8/X5/6.3V
C315 10U/8/X5/6.3V
C316 10U/8/X5/6.3V
C317 10U/8/X5/6.3V
EC57 1000U/D/6.3V/8C
R417 34.8/6/1
R418 34.8/6/1
CPUVREF
40 MILS
R419 15/6/1
R420 15/6/1
SC35 0.1U/6/X/16V
C318 4.7U/8/Y/10V
SC36 1N/4/X/50V/X
For strong reference voltage
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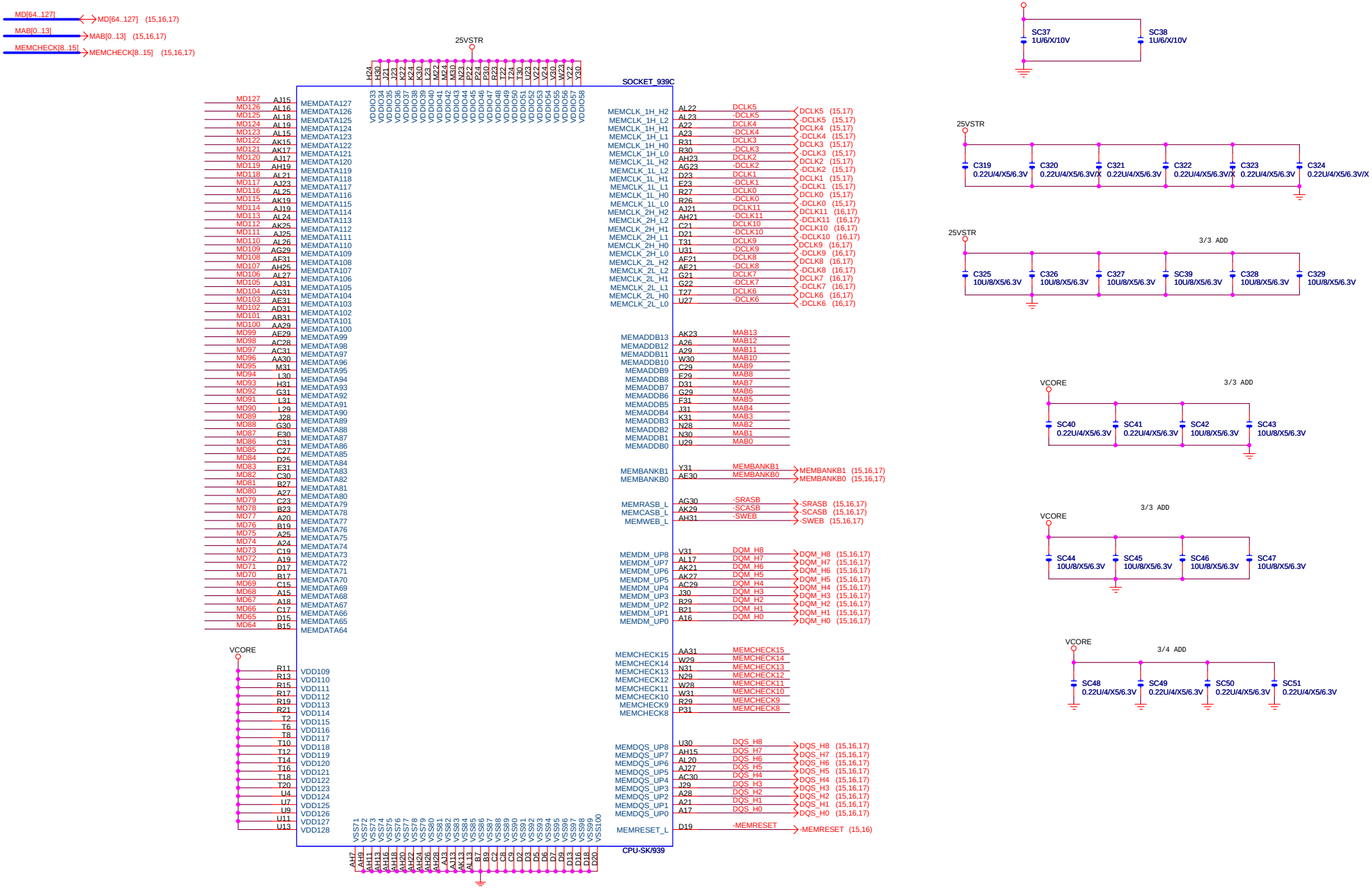

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Size: Custom	Document Number: GA-K8U-939
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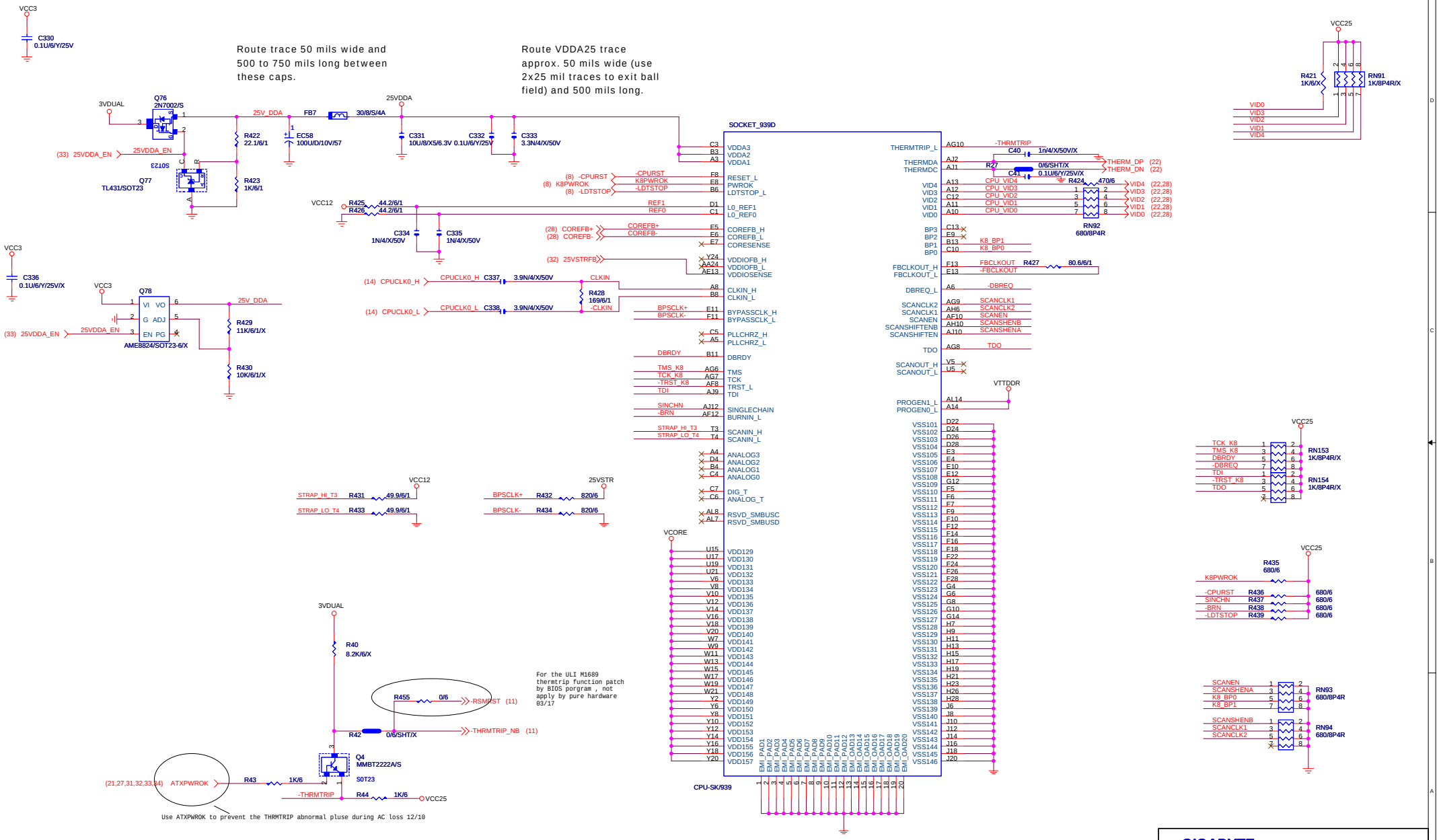
Route trace 50 mils wide and 500 to 750 mils long between these caps.
Route VDDA25 trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.
SOCKET_939D
CPU-SK/939
Q76 2N7002/S
Q77 TL431/SOT23
Q78 AME8824/SOT23-6/X
Q4 MMBT2222A/S
C330 0.1U/6/Y/25V
C331 10U/8/X5/6.3V
C332 0.1U/6/Y/25V
C333 3.3N/4/X/50V
C334 1N/4/X/50V
C335 1N/4/X/50V
C336 0.1U/6/Y/25V/X
EC58 100U/D/10V/57
FB7 30/8/S/4A
R422 22.1/6/1
R423 1K/6/1
R425 44.2/6/1
R426 44.2/6/1
R427 80.6/6/1
R428 169/6/1
R429 11K/6/1/X
R430 10K/6/1/X
R431 49.9/6/1
R432 820/6
R433 49.9/6/1
R434 820/6
R435 680/6
R436 680/6
R437 680/6
R438 680/6
R439 680/6
R40 8.2K/6/X
R42 0/6/SHT/X
R43 1K/6
R44 1K/6
R455 0/6
C40 1n4/X/50V/X
C41 0.1U/6/Y/25V/X
R27 0/6/SHT/X
R424 470/6
RN91 1K/8P4R/X
RN92 680/8P4R
RN93 680/8P4R
RN94 680/8P4R
RN153 1K/8P4R/X
RN154 1K/8P4R/X
For the ULI M1689 thermtrip function patch by BIOS porgram , not apply by pure hardware 03/17
Use ATXPWROK to prevent the THRMTRIP abnormal pluse during AC loss 12/10
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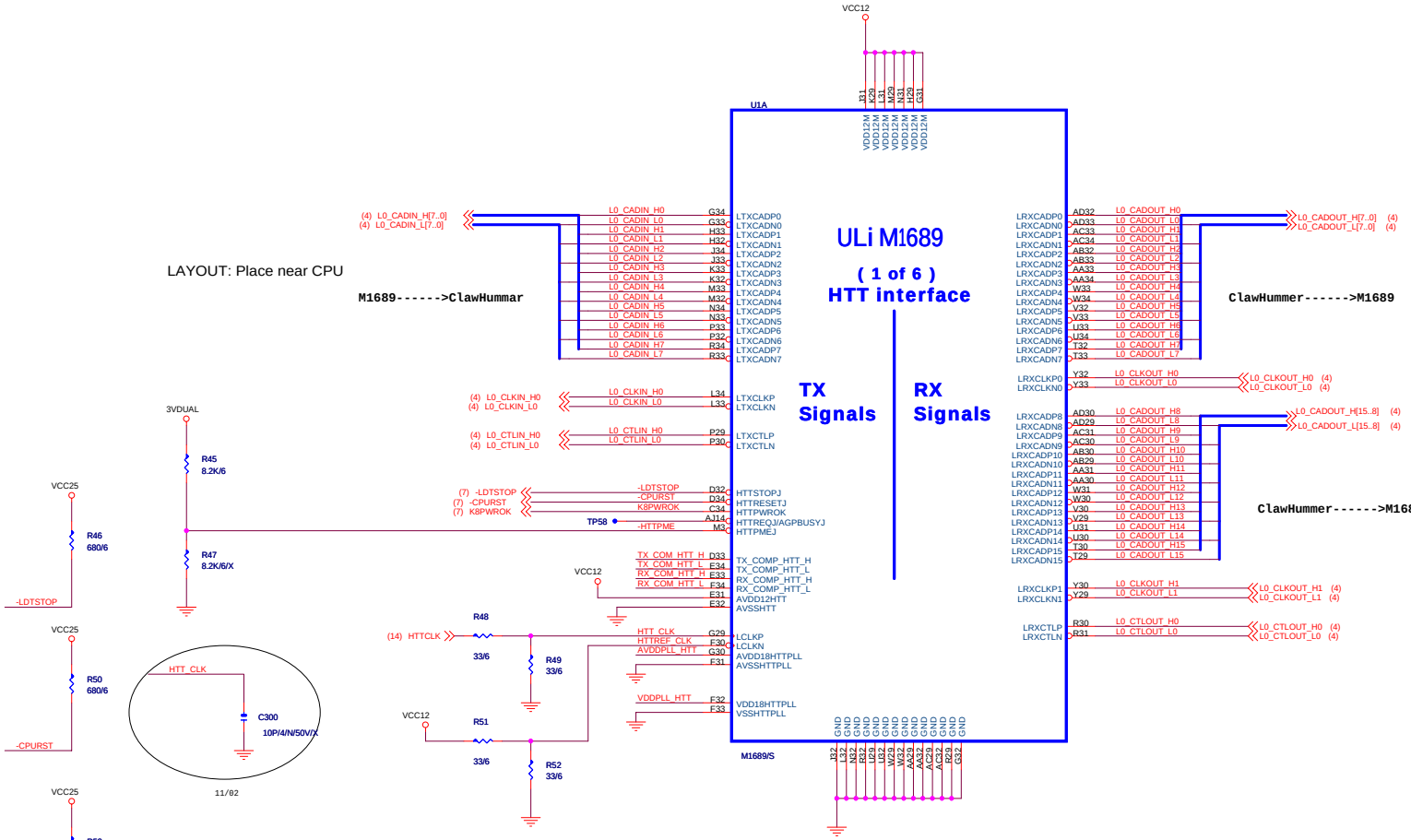
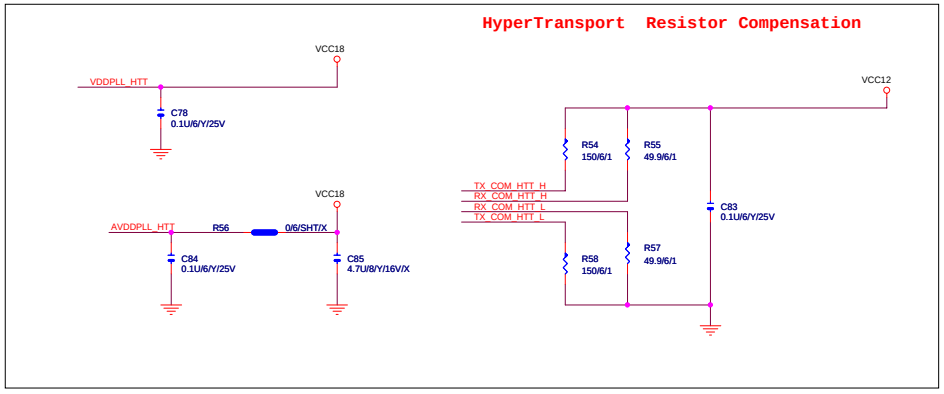
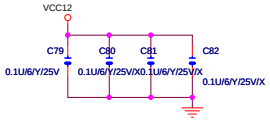


GND SINGLE USE TRACE
TO SYS GND PLACE



LAYOUT: Place HTT bypass caps on
topside near connected M1689 HTT link.



GIGABYTE		
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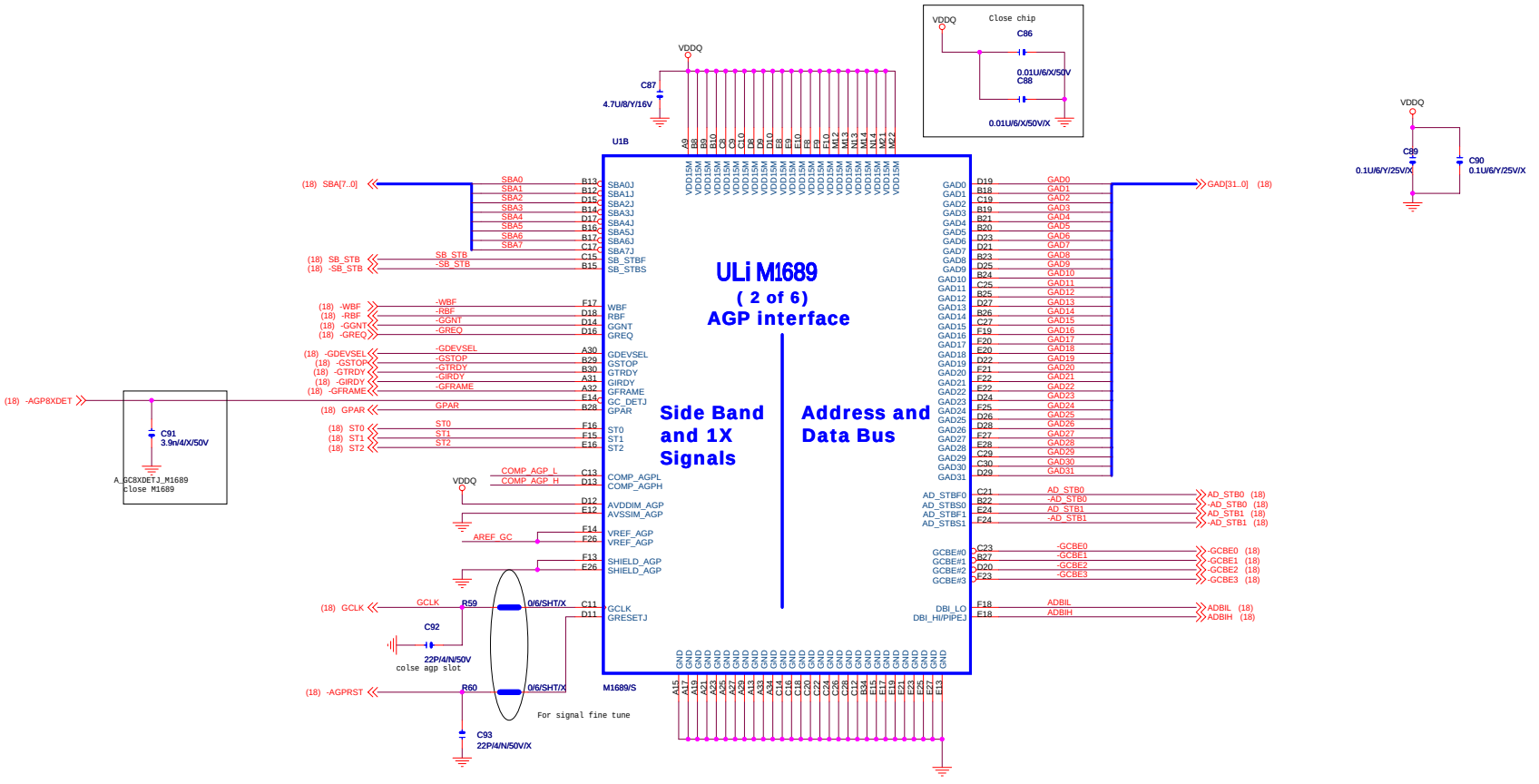

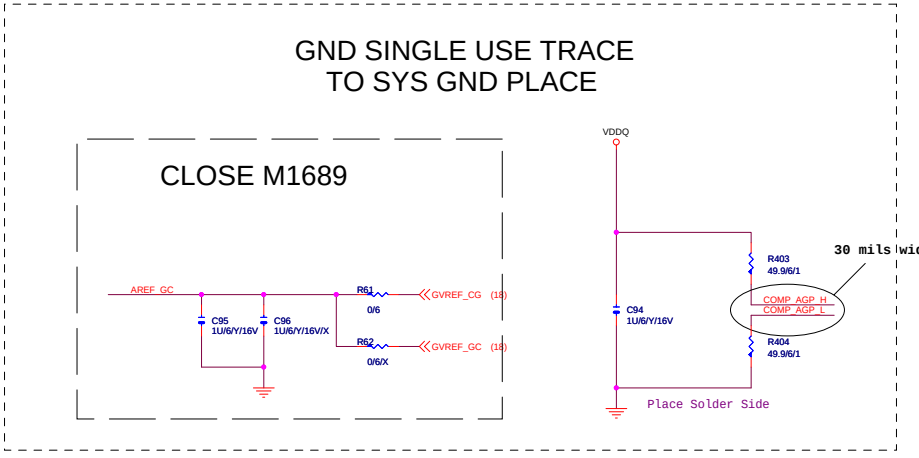

GIGABYTE			
Title: ULI AGP8X & CONTROL			
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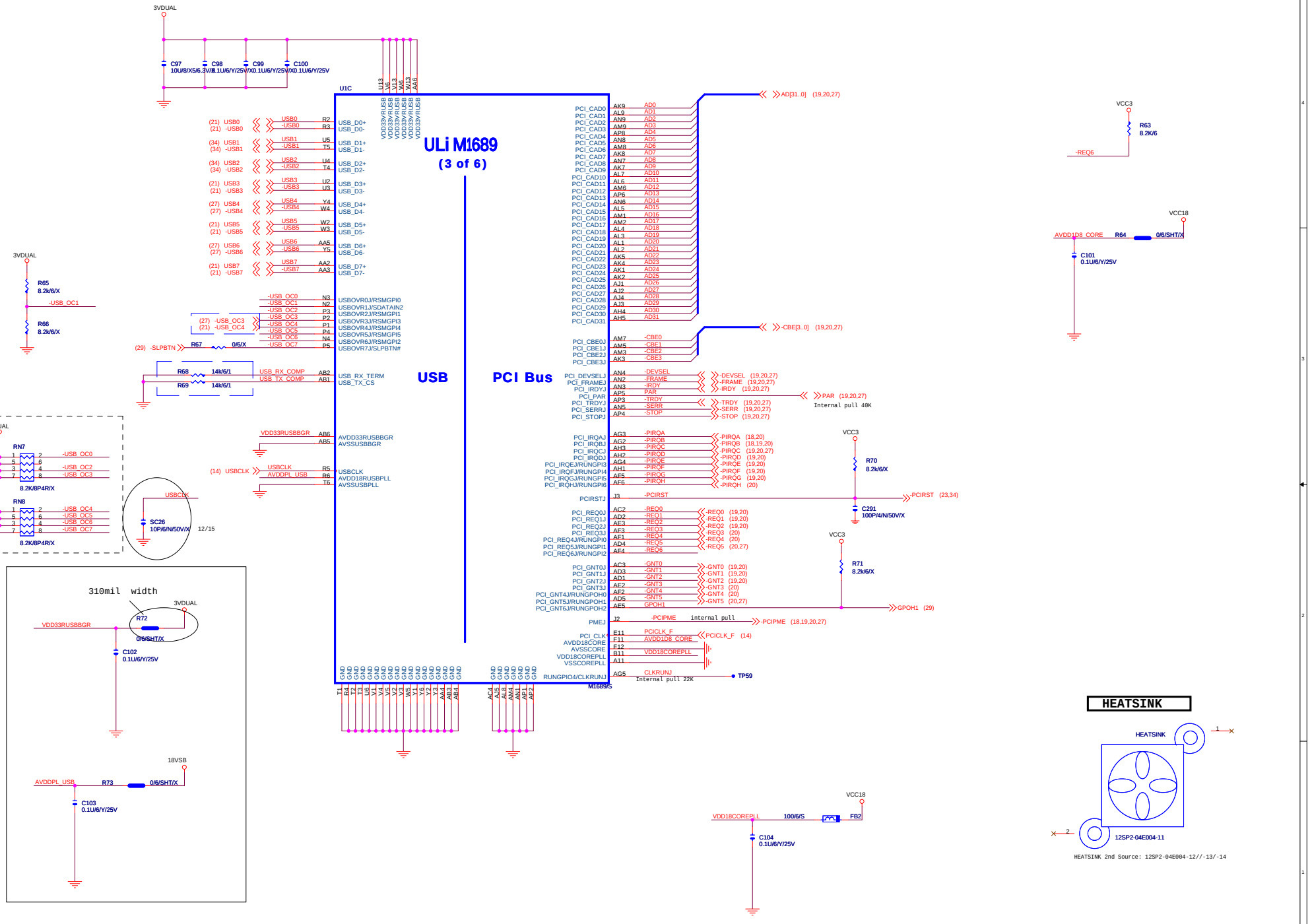
ULi M1689
(3 of 6)
U1C
USB
PCI Bus
M1689/S
3VDUAL
C97 10U/8/X5/6.3V/M
C98 0.1U/6/Y/25V/X
C99 0.1U/6/Y/25V/X
C100 0.1U/6/Y/25V/X
VDD33V/RUSB
USB_D0+
USB_D0-
USB_D1+
USB_D1-
USB_D2+
USB_D2-
USB_D3+
USB_D3-
USB_D4+
USB_D4-
USB_D5+
USB_D5-
USB_D6+
USB_D6-
USB_D7+
USB_D7-
USBOVR0J/RSMGPI0
USBOVR1J/SDATAIN2
USBOVR2J/RSMGPI1
USBOVR3J/RSMGPI3
USBOVR4J/RSMGPI4
USBOVR5J/RSMGPI5
USBOVR6J/RSMGPI2
USBOVR7J/SLPBTN#
USB_RX_TERM
USB_TX_CS
AVDD33RUSBBGR
AVSSUSBBGR
USBCLK
AVDDPL_USB
AVDD18RUSBPLL
AVSSUSBPLL
AD[31..0] (19,20,27)
PCI_CAD0
PCI_CAD1
PCI_CAD2
PCI_CAD3
PCI_CAD4
PCI_CAD5
PCI_CAD6
PCI_CAD7
PCI_CAD8
PCI_CAD9
PCI_CAD10
PCI_CAD11
PCI_CAD12
PCI_CAD13
PCI_CAD14
PCI_CAD15
PCI_CAD16
PCI_CAD17
PCI_CAD18
PCI_CAD19
PCI_CAD20
PCI_CAD21
PCI_CAD22
PCI_CAD23
PCI_CAD24
PCI_CAD25
PCI_CAD26
PCI_CAD27
PCI_CAD28
PCI_CAD29
PCI_CAD30
PCI_CAD31
-CBE[3..0] (19,20,27)
PCI_CBE0J
PCI_CBE1J
PCI_CBE2J
PCI_CBE3J
PCI_DEVSELJ
PCI_FRAMEJ
PCI_IRDYJ
PCI_PAR
PCI_TRDYJ
PCI_SERRJ
PCI_STOPJ
PAR (19,20,27)
Internal pull 40K
PCI_IRQAJ
PCI_IRQBJ
PCI_IRQCJ
PCI_IRQDJ
PCI_IRQEJ/RUNGPI3
PCI_IRQFJ/RUNGPI4
PCI_IRQGJ/RUNGPI5
PCI_IRQHJ/RUNGPI6
PCIRSTJ
PCIRST (23,34)
PCI_REQ0J
PCI_REQ1J
PCI_REQ2J
PCI_REQ3J
PCI_REQ4J/RUNGPI0
PCI_REQ5J/RUNGPI1
PCI_REQ6J/RUNGPI2
PCI_GNT0J
PCI_GNT1J
PCI_GNT2J
PCI_GNT3J
PCI_GNT4J/RUNGPOH0
PCI_GNT5J/RUNGPOH1
PCI_GNT6J/RUNGPOH2
GPOH1 (29)
PMEJ
-PCIPME internal pull
-PCIPME (18,19,20,27)
PCI_CLK
PCICLK_F (14)
AVDD18CORE
AVDD1D8_CORE
AVSSCORE
VDD18COREPLL
VSSCOREPLL
RUNGPIO4/CLKRUNJ
CLKRUNJ
Internal pull 22K
TP59
GND
R63 8.2K/6
R64 0/6/SHT/X
R65 8.2k/6/X
R66 8.2k/6/X
R67 0/6/X
R68 14k/6/1
R69 14k/6/1
R70 8.2k/6/X
R71 8.2k/6/X
R72 0/6/SHT/X
R73 0/6/SHT/X
100/6/S
FB2
RN7
RN8
8.2K/8P4R/X
SC26 10P/6/N/50V/X
12/15
C101 0.1U/6/Y/25V
C102 0.1U/6/Y/25V
C103 0.1U/6/Y/25V
C104 0.1U/6/Y/25V
C291 100P/4/N/50V/X
VCC3
VCC18
18VSB
AVDD1D8_CORE
-REQ6
-SLPBTN
-USB_OC0
-USB_OC1
-USB_OC2
-USB_OC3
-USB_OC4
-USB_OC5
-USB_OC6
-USB_OC7
-PIRQA (18,20)
-PIRQB (18,19,20)
-PIRQC (19,20,27)
-PIRQD (19,20)
-PIRQE (19,20)
-PIRQF (19,20)
-PIRQG (19,20)
-PIRQH (20)
-REQ0 (19,20)
-REQ1 (19,20)
-REQ2 (19,20)
-REQ3 (20)
-REQ4 (20)
-REQ5 (20,27)
-GNT0 (19,20)
-GNT1 (19,20)
-GNT2 (19,20)
-GNT3 (20)
-GNT4 (20)
-GNT5 (20,27)
-DEVSEL (19,20,27)
-FRAME (19,20,27)
-IRDY (19,20,27)
-TRDY (19,20,27)
-SERR (19,20,27)
-STOP (19,20,27)
310mil width
HEATSINK
12SP2-04E004-11
HEATSINK 2nd Source: 12SP2-04E004-12//-13/-14
GIGABYTE
Title
ULI USB & PCI
Size C
Document Number
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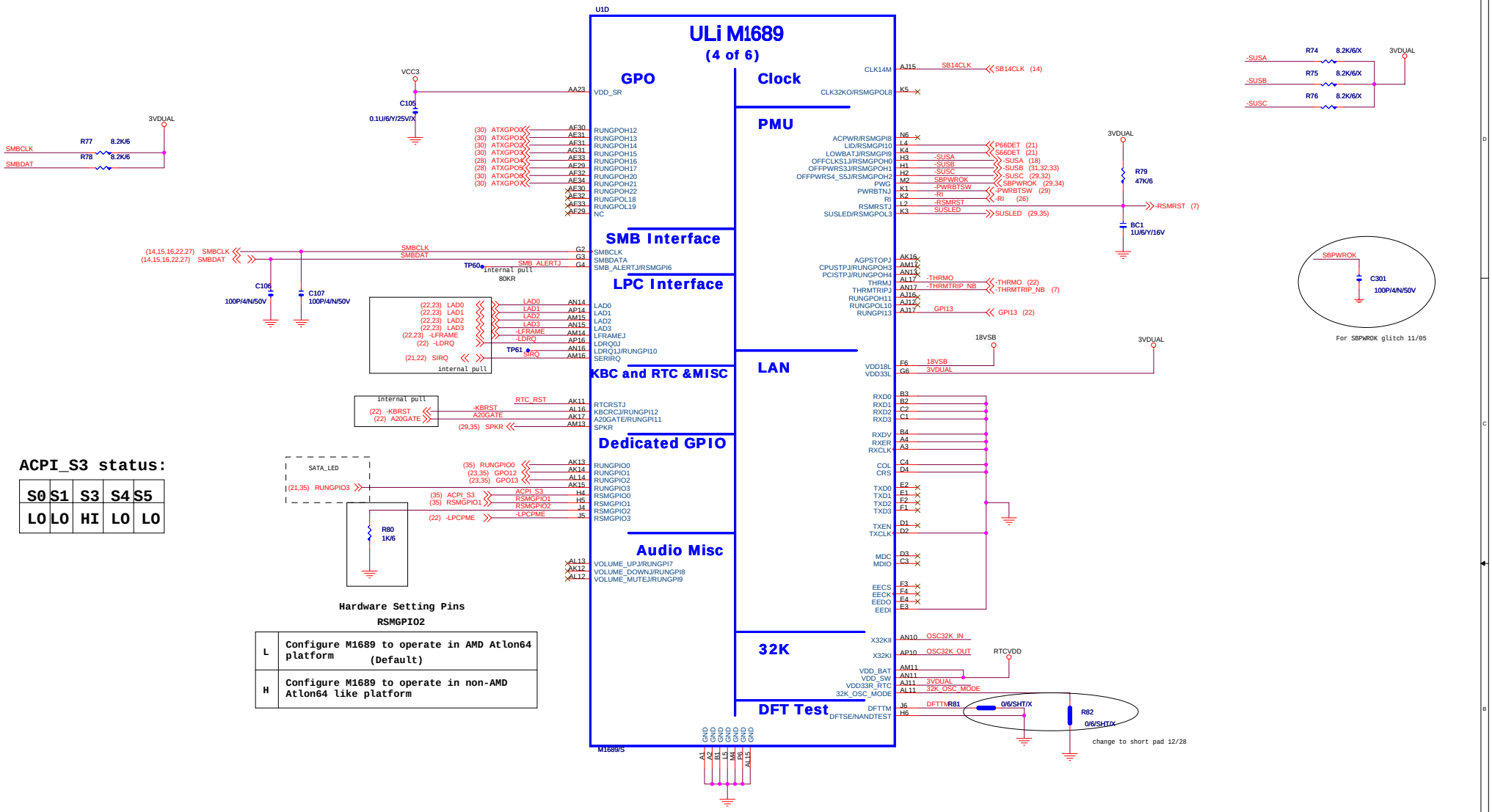
U1D
ULi M1689
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GPO
Clock
PMU
SMB Interface
LPC Interface
KBC and RTC &MISC
LAN
Dedicated GPIO
Audio Misc
32K
DFT Test
M1689/S
ACPI_S3 status:
S0 S1 S3 S4 S5
LO LO HI LO LO
Hardware Setting Pins
RSMGPIO2
L Configure M1689 to operate in AMD Atlon64 platform (Default)
H Configure M1689 to operate in non-AMD Atlon64 like platform
For SBPWROK glitch 11/05
change to short pad 12/28
Add short wire 11NH2-010005-00 11/30
R86 change to 1K , C112 turn to RTCVDD plane for ac plug off drop off issue 11/30
CLR_CMOS CLEAR COMS JUMPER
1-2 Enable
2-3 Disable (Default)
GIGABYTE
Title
ULI GBE & SMB
Size C
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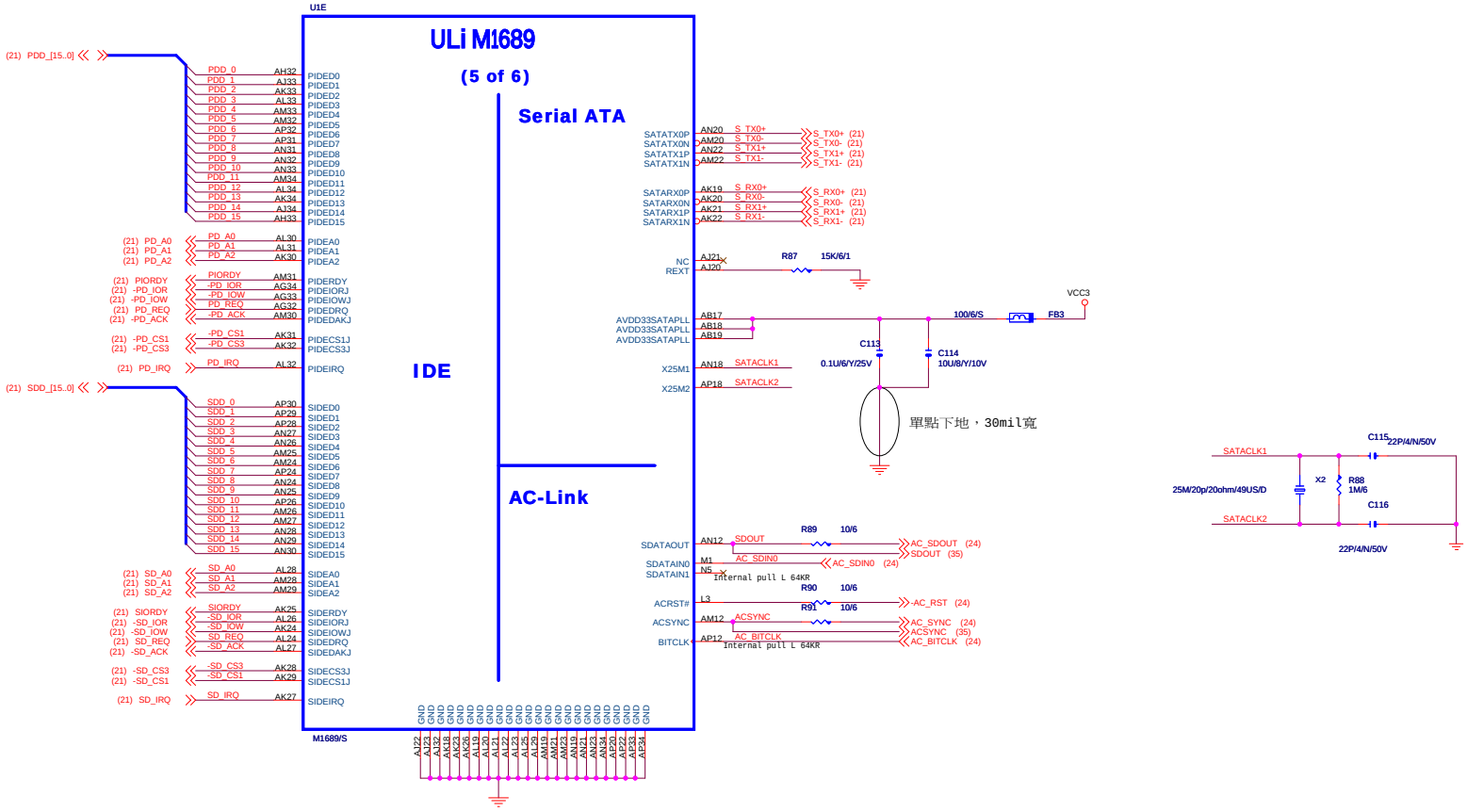

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Title	ULI IDE & SATA	
Size C	Document Number GA-K8U-939	Rev 1.0
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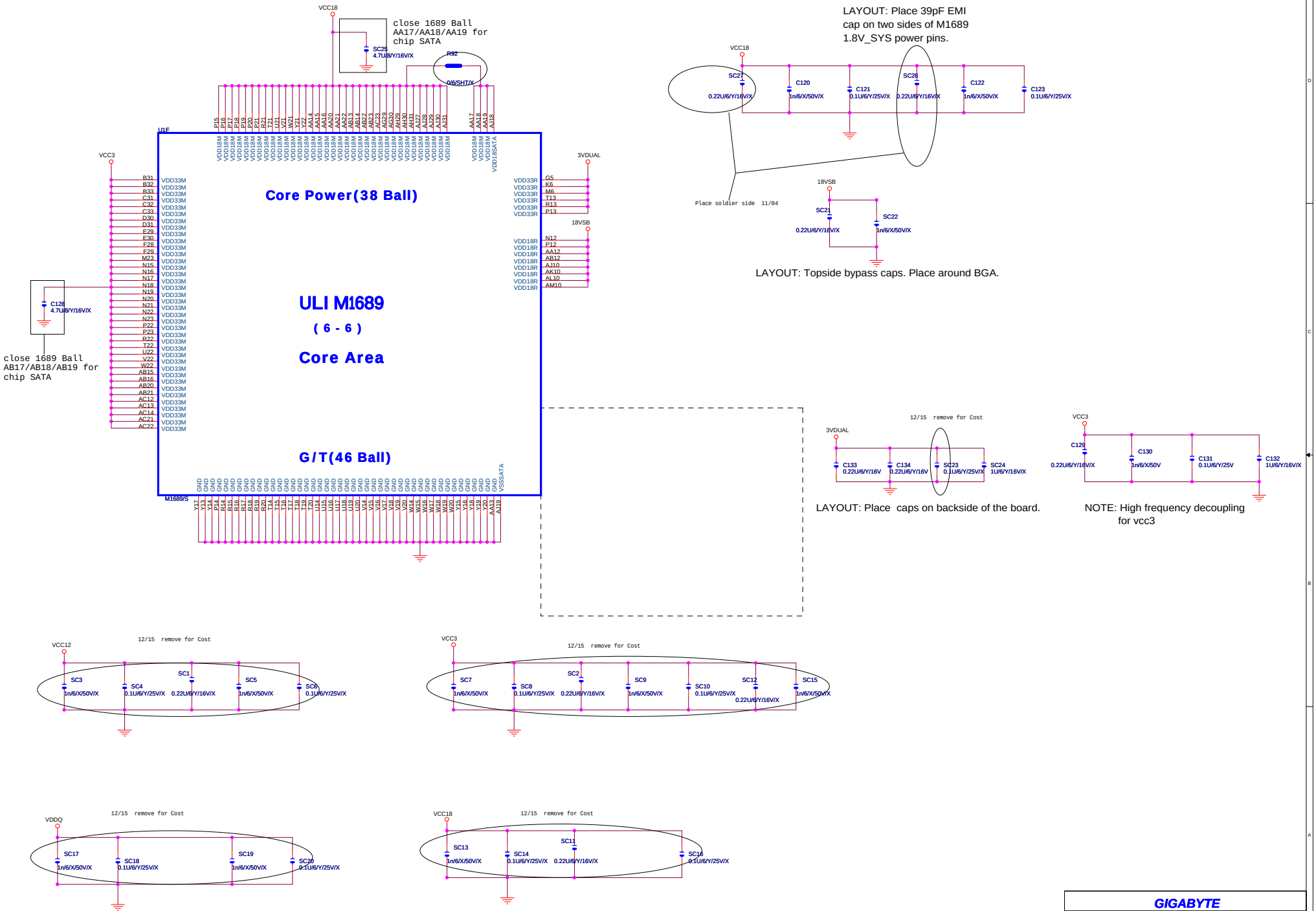

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Size	C
Document Number	GA-K8U-939
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Date:	Wednesday, June 22, 2005
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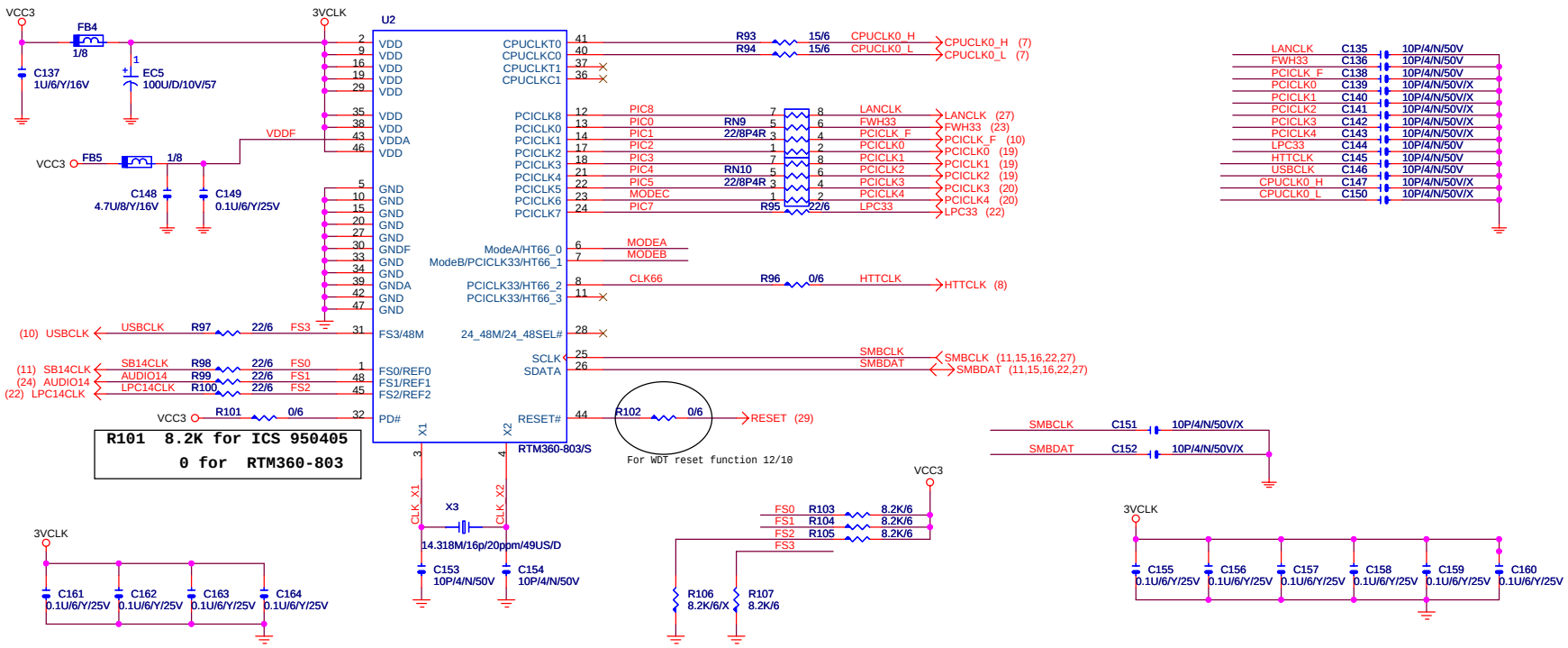

Internal PH *
Internal PL **

** FS3	* FS2	* FS1	* FS0	CPU MHz	HTT MHz	PCI MHz	
0	0	0	0	100.90	67.27	33.63	
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	66.68	33.34	
0	1	1	1	200.40	66.80	33.40	Default
1	0	0	0	150.00	60.00	30.00	
1	0	0	1	180.00	60.00	30.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	

Internal PH *

24_48_sel	Pin 28	
0	48MHz	
1 *	24MHz	(Default)

Internal PH *

MODE_A	MODE_B	Pin 6	Pin 7	Pin 8	Pin 11	
0	0	HTTCLK0	HTTCLK1	HTTCLK2	PCICLK10	(Default)
0	1	MODE_A (Input Only)	HTTCLK1	HTTCLK2	HTTCLK3	
1	0	PCICLK7	PCICLK8	PCICLK9	PCICLK10	
1 *	1 *	MODE_A (Input Only)	PCICLK8	PCICLK9	PCICLK10	

MODEC	Pin 23	Pin 24	
0	33MHz	33MHz	(Default)
1	33MHz	PCI_STOP#	

MODEC only for RTM360-803

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Title	CLOCK GEN		
Size Custom	Document Number GA-K8U-939		Rev 1.0
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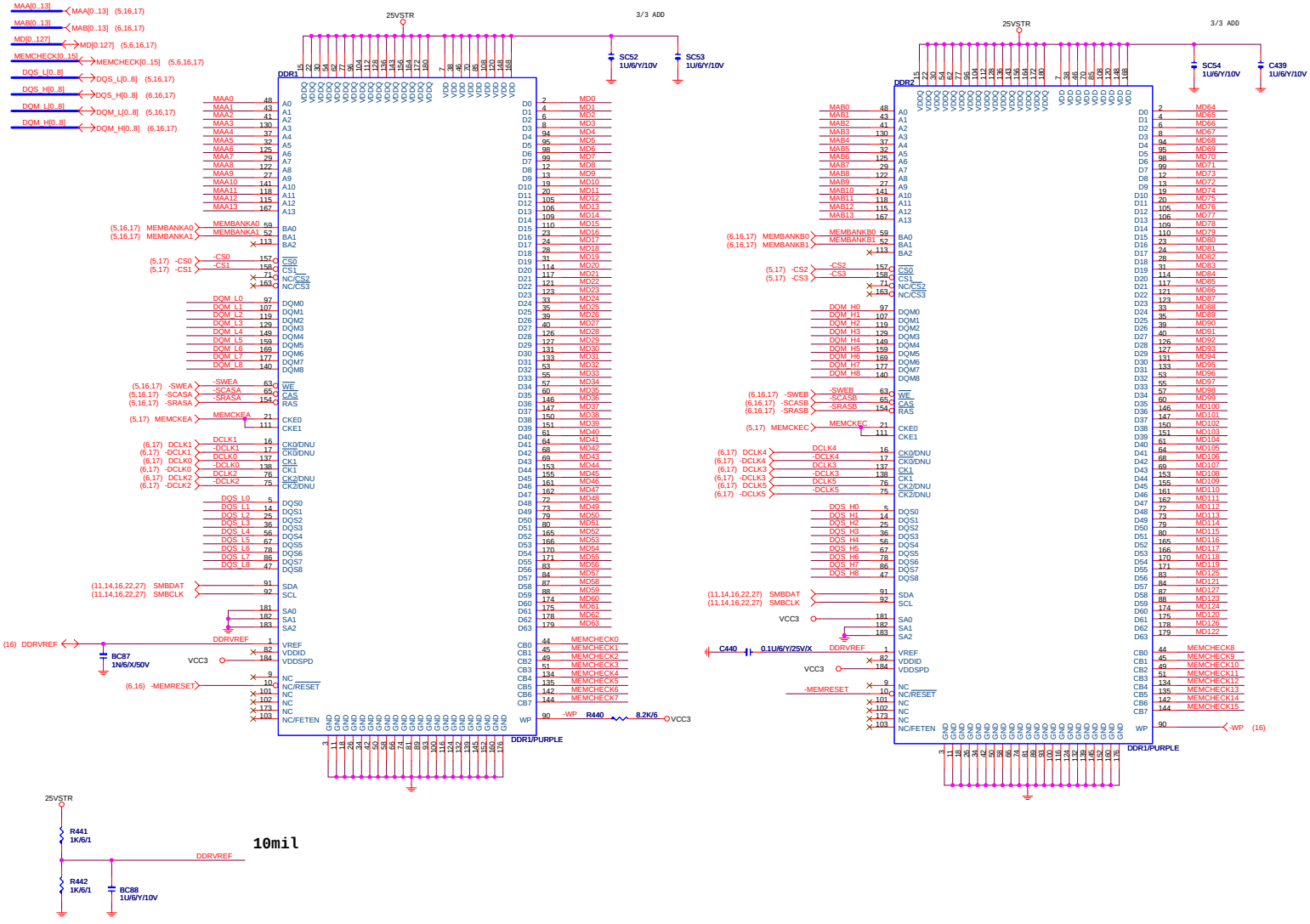

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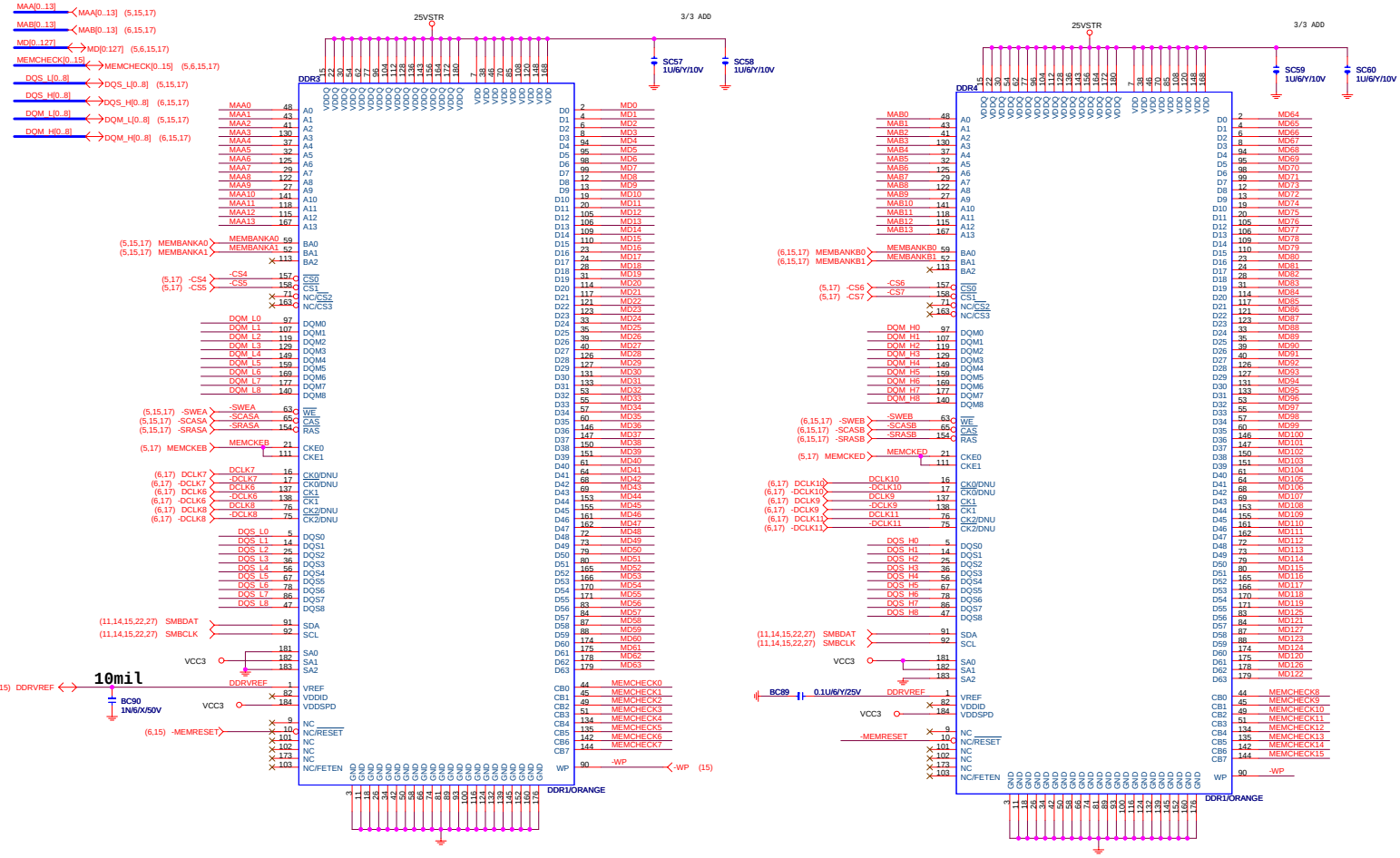
Size: Custom	Document Number: GA-K8U-939		Rev: 1.0
Date:		Sheet 15 of 35	



Title	DDR1_2		
Size	Document Number		Rev
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DDR termimator chagne to 56 ohm for compability 03/25

MAA[0..13] MAA[0..13] (5,15,16)
MAB[0..13] MAB[0..13] (6,15,16)
MD[0..127] MD[0:127] (5,6,15,16)
MEMCHECK[0..15] MEMCHECK[0..15] (5,6,15,16)
DQS_L[0..8] DQS_L[0..8] (5,15,16)
DQS_H[0..8] DQS_H[0..8] (6,15,16)
DQM_L[0..8] DQM_L[0..8] (5,15,16)
DQM_H[0..8] DQM_H[0..8] (6,15,16)
DCLK[0..11] DCLK[0..11] (6,15,16)
-DCLK[0..11] -DCLK[0..11] (6,15,16)

VTTDDR 25VSTR

C341 0.1U/4/Y/16V/X
C343 0.1U/4/Y/16V/X
C345 0.1U/4/Y/16V/X
C347 0.1U/4/Y/16V
C349 0.1U/4/Y/16V
C351 0.1U/4/Y/16V

C368 0.1U/4/Y/16V
C370 0.1U/4/Y/16V
C372 0.1U/4/Y/16V
C375 0.1U/4/Y/16V
C378 0.1U/4/Y/16V
C381 0.1U/4/Y/16V
C384 0.1U/4/Y/16V
C387 0.1U/4/Y/16V
C390 0.1U/4/Y/16V
C393 0.1U/4/Y/16V
C396 0.1U/4/Y/16V
C399 0.1U/4/Y/16V
C402 0.1U/4/Y/16V
C405 0.1U/4/Y/16V

C366 0.1U/4/Y/16V
C369 0.1U/4/Y/16V
C371 0.1U/4/Y/16V
C373 0.1U/4/Y/16V
C376 0.1U/4/Y/16V
C382 0.1U/4/Y/16V
C385 0.1U/4/Y/16V
C388 0.1U/4/Y/16V
C391 0.1U/4/Y/16V
C394 0.1U/4/Y/16V
C397 0.1U/4/Y/16V
C400 0.1U/4/Y/16V
C403 0.1U/4/Y/16V
C406 0.1U/4/Y/16V *

VTTDDR

SC61 10U/8/X5/6.3V SC62 10U/8/X5/6.3V

place under CPU socket

25VSTR

EC59 1000U/D/6.3V/8C
EC60 1000U/D/6.3V/8C
C427 0.1U/4/Y/16V
C429 0.1U/4/Y/16V/X

25VSTR

C441 10U/8/X5/6.3V
C442 10U/8/X5/6.3V
C443 10U/8/X5/6.3V
C444 10U/8/X5/6.3V

VTTDDR

MD71 MD67 MD76 MD73 MD64 MD68 MD69 MD65 MD72 MD77 DQM_H1 DQS_H1 MD78 MD79 MD74 MD75 MEMCKED MEMCKEC MAB12 MD84 MD80 MD81 MD85 DQS_H2 MD92 MD89 MD93 DQS_H3 DQM_H3 MAB4 MAB3 MD90 MAB0 MAB10 MEMCHECK10 MEMCHECK14 MEMCHECK6 MEMCHECK11 MEMBANKB1 MEMCHECK15 DQS_H4 DQM_H4 MD102 MD98 MD103 MEMBANKB0 MD99 MD108 MD112 MD113 MD117 MAB13 MD110 MD107 MD111 MD116 MD114 MD124 MD115 MD120 MD118 DQM_H6 DQS_H6 MD119 DQM_L5 -CS1 -CS5 -CS4

RN95 56/8P4R
RN98 56/8P4R
RN101 56/8P4R
RN104 56/8P4R
RN107 56/8P4R
RN110 56/8P4R
RN113 56/8P4R
RN116 56/8P4R
RN119 56/8P4R
RN122 56/8P4R
RN125 56/8P4R
RN128 56/8P4R
RN131 56/8P4R
RN134 56/8P4R
RN137 56/8P4R
RN139 56/8P4R
RN141 56/8P4R

(5,16) MEMCKED
(5,15) MEMCKEC
(6,15,16) MEMBANKB1
(6,15,16) MEMBANKB0
(5,15) -CS1
(5,16) -CS5
(5,16) -CS4

VTTDDR

MD46 MD43 MD42 DQS_L5 MD11 MD10 MD15 MD14 MD23 MAA8 MAA7 MD22 MEMCHECK0 MAA1 MEMCHECK5 MEMCHECK4 DQS_L2 MD21 MD17 MD16 MD24 MAA6 MAA5 MD19 -CS0 MD41 MD45 -SWEA MD34 DQM_L4 DQS_L4 MD33 MD104 -SRASB -SWEB MD109 MEMBANKA1 MEMCHECK3 MEMCHECK2 MAA10 DQS_L7 DQM_L7 MD57 MD56 MD105 -SCASA -CS2 -SCASB -SRASA MD40 MD44 MD35 DQS_L3 MD29 MD25 MD28

RN96 56/8P4R
RN99 56/8P4R
RN102 56/8P4R
RN105 56/8P4R
RN108 56/8P4R
RN111 56/8P4R
RN115 56/8P4R
RN118 56/8P4R
RN121 56/8P4R
RN124 56/8P4R
RN127 56/8P4R
RN130 56/8P4R
RN133 56/8P4R
RN136 56/8P4R

(5,15) -CS0
(5,15,16) -SWEA
(6,15,16) -SRASB
(6,15,16) -SWEB
(5,15,16) MEMBANKA1
(5,15,16) -SCASA
(5,15) -CS2
(6,15,16) -SCASB
(5,15,16) -SRASA

VTTDDR

MD126 MD127 MD122 MD123 MD59 MD63 MD58 MD62 MAA13 MD53 MD49 MD48 MD61 MD60 MD51 MD50 MD39 MEMBANKA0 MD38 MD88 MAB6 MAB5 MD83 MD52 MD47 -CS7 -CS6 MD37 MD36 MD32 MEMCHECK7 MD31 MAA2 MD27 MD30 MD94 MD91 MD95 MAB2 MD26 MAA3 MAA4 DQM_L3 MAA12 MD20 MEMCKEB MEMCKEA DQS_L1 DQM_L1 MD13 MD9 MD86 MAB7 MAB8 MD87 MD8 MD12 MD3 MD7 MD1 MD5 MD0 MD4

RN97 56/8P4R
RN100 56/8P4R
RN103 56/8P4R
RN106 56/8P4R
RN109 56/8P4R
RN112 56/8P4R
RN114 56/8P4R
RN117 56/8P4R
RN120 56/8P4R
RN123 56/8P4R
RN126 56/8P4R
RN129 56/8P4R
RN132 56/8P4R
RN135 56/8P4R
RN138 56/8P4R
RN140 56/8P4R

(5,15,16) MEMBANKA0
(5,16) -CS7
(5,16) -CS6
(5,16) MEMCKEB
(5,15) MEMCKEA

VTTDDR

C339 C340 C342 C344 C346 C348 C350 C352 C362 C364 C367 C374 C377 C380 C383 C386 C392 C395 C398 C401 C404 C407 C408 C409 C410 C411 C414 C415 C416 C418 C421 C422 C423 C424 C425 C426

0.1U/4/Y/16V
0.1U/4/Y/16V/X

VTTDDR

MEMCHECK9 DQS_H8 DQM_H8 MEMCHECK12 MEMCHECK13 MAB1 MEMCHECK8

RN142 56/8P4R
RN143 56/8P4R

MD2 MD6 DQS_L0 DQM_L0 MAA0 DQM_L8 DQS_L8 MEMCHECK1

RN146 56/8P4R
RN148 56/8P4R

DQM_H0 MD70 DQS_H0 MD66 -CS3 DQS_H5 DQM_H5 MD106

RN150 56/8P4R
RN152 56/8P4R

(5,15) -CS3

-DCLK0 R443 120/6 DCLK0
-DCLK1 R444 120/6 DCLK1
-DCLK2 R445 120/6 DCLK2
-DCLK3 R446 120/6 DCLK3
-DCLK4 R447 120/6 DCLK4
-DCLK5 R448 120/6 DCLK5
-DCLK6 R449 120/6 DCLK6
-DCLK7 R450 120/6 DCLK7
-DCLK8 R451 120/6 DCLK8
-DCLK9 R452 120/6 DCLK9
-DCLK10 R453 120/6 DCLK10
-DCLK11 R454 120/6 DCLK11

-CS5 -CS4 -SCASA

CN42 22P/8P4C
CN43 22P/8P4C
CN44 22P/8P4C
CN45 22P/8P4C
CN46 22P/8P4C
CN47 22P/8P4C
CN48 22P/8P4C
CN49 22P/8P4C
CN50 22P/8P4C
CN51 22P/8P4C

MEMBANKA0 C417 22P/4/N/50V
MEMBANKA1 C419 22P/4/N/50V
MEMBANKB1 C420 22P/4/N/50V

-CS3 -SCASB -CS2 -CS6
MEMBANKB0 -CS0 -SWEA -SRASA

MAA13 C428 22P/4/N/50V
MAB1 C430 22P/4/N/50V
MAB13 C431 22P/4/N/50V
-SWEB C432 22P/4/N/50V
-CS1 C433 22P/4/N/50V
-CS7 C434 22P/4/N/50V
MEMCKEC C435 22P/4/N/50V
MEMCKED C436 22P/4/N/50V
-SRASB C437 22P/4/N/50V

(5,15) MEMCKEC
(5,16) MEMCKED

MAB10 MAB0 MAA10 MAA0 MAA9 MAA11 MAB9 MAB11 MAB6 MAA6 MAA5 MAB5 MAA1 MAB2 MAA2 MAA12 MEMCKEB MEMCKEA MAB12 MAB8 MAB7 MAA8 MAA7 MAA3 MAA4 MAB3 MAB4

VTTDDR

MD18 MAA9 DQM_L2 MAA11 MD97 MD101 MD100 MD96 MD82 DQM_H2 MAB9 MAB11 MD55 MD54 DQS_L6 DQM_L6 MD125 MD121 DQM_H7 DQS_H7

RN144 56/8P4R
RN145 56/8P4R
RN147 56/8P4R
RN149 56/8P4R
RN151 56/8P4R

GIGABYTE

Title: DDR TERMINATOR

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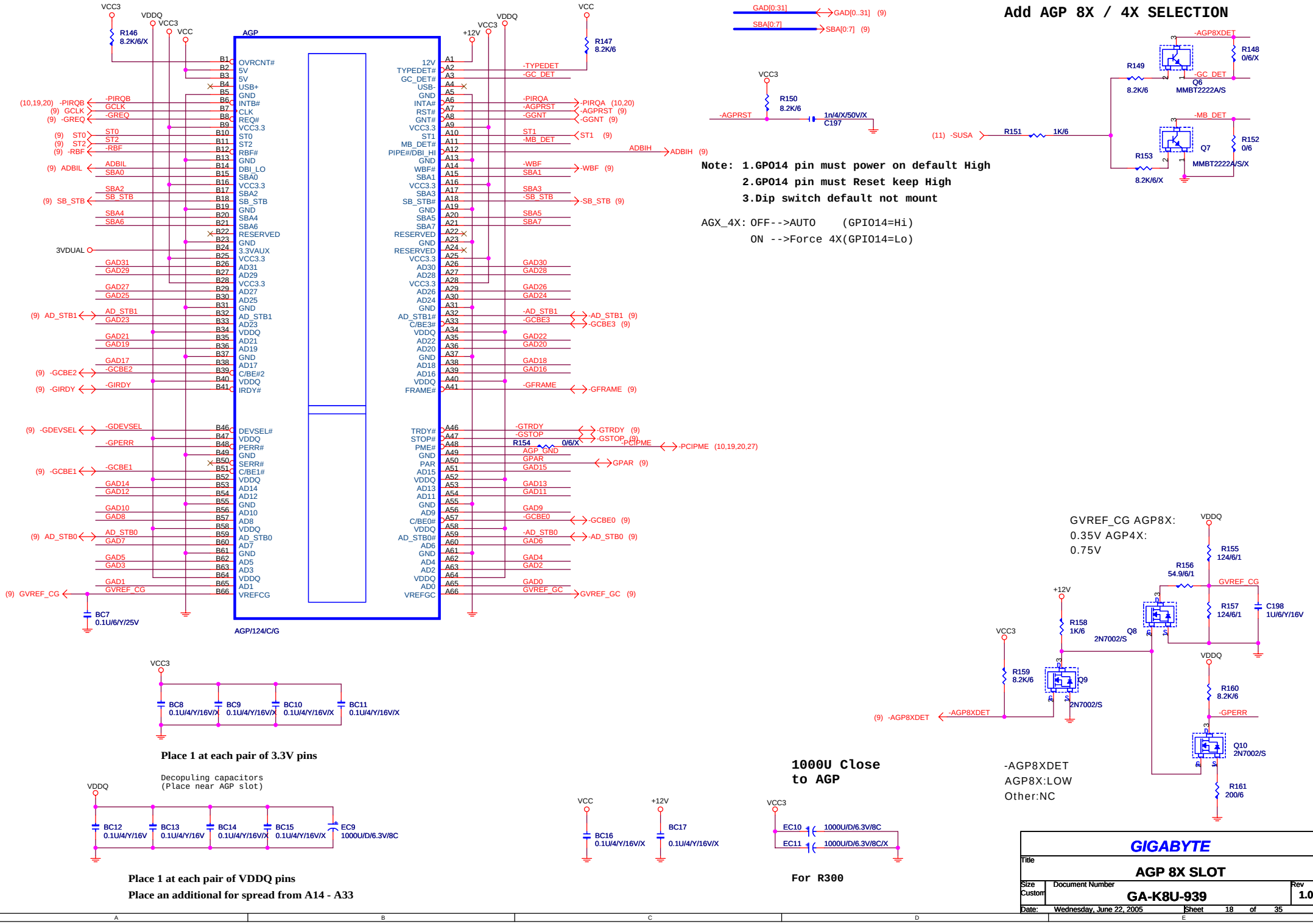
AGP
AGP/124/C/G
GAD[0:31]
SBA[0:7]
Add AGP 8X / 4X SELECTION
Note: 1.GPO14 pin must power on default High
2.GPO14 pin must Reset keep High
3.Dip switch default not mount
AGX_4X: OFF-->AUTO (GPIO14=Hi)
ON -->Force 4X(GPIO14=Lo)
GVREF_CG AGP8X:
0.35V AGP4X:
0.75V
-AGP8XDET
AGP8X:LOW
Other:NC
Place 1 at each pair of 3.3V pins
Decoupling capacitors
(Place near AGP slot)
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33
1000U Close
to AGP
For R300
GIGABYTE
AGP 8X SLOT
GA-K8U-939
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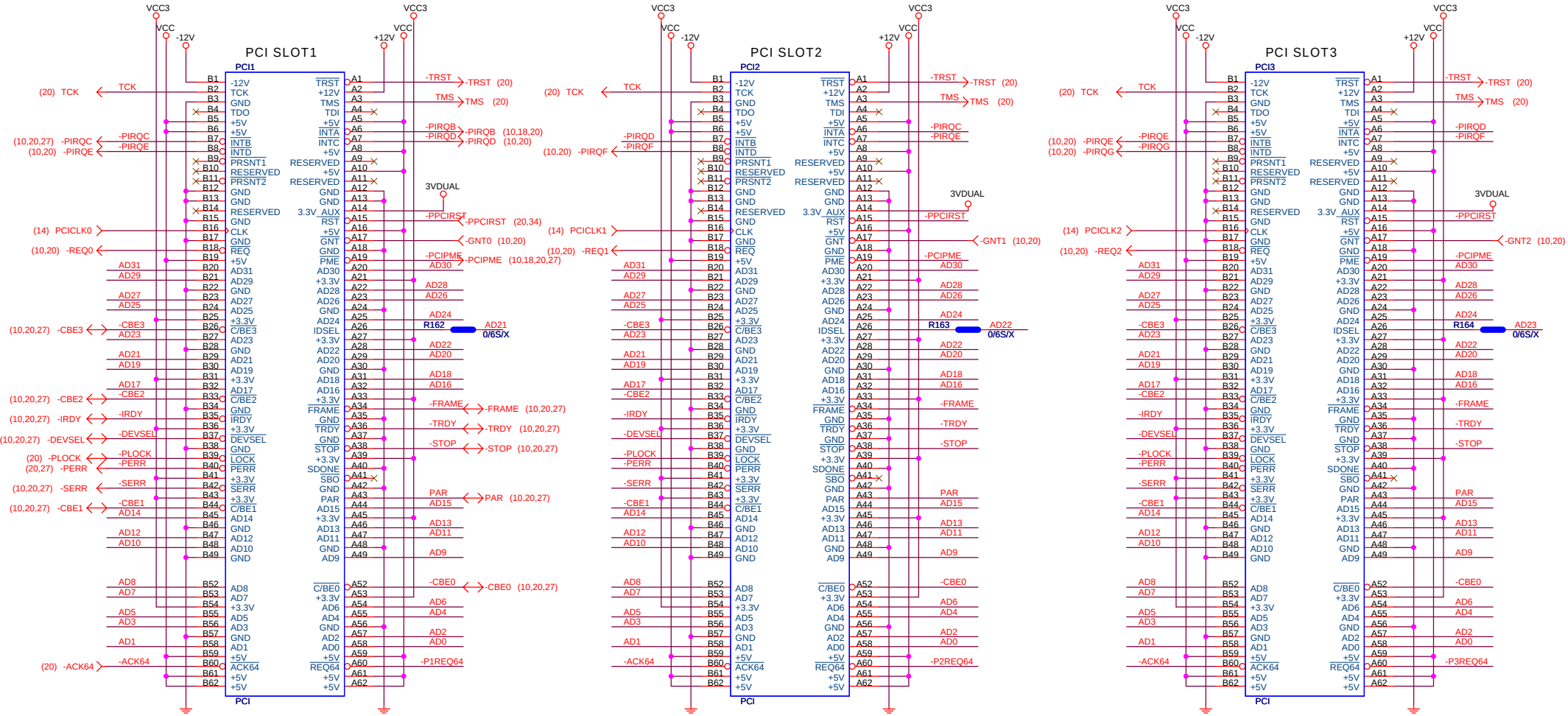
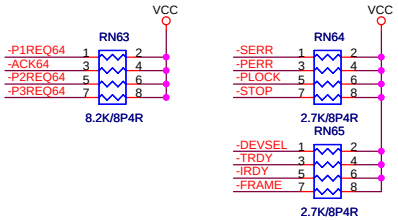
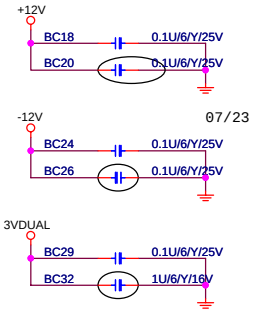
PCI SLOT 1,2,3

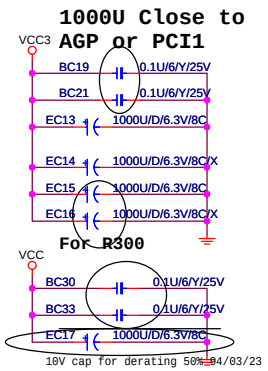
AD[0..31] <-> AD[0..31] (10,20,27)

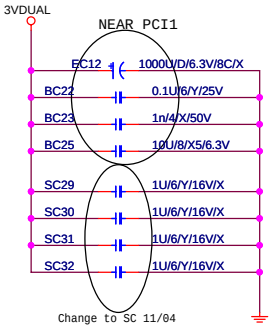


IDSEL(A21) IDSEL(A22) IDSEL(A23)









GIGABYTE		
Title: PCI SLOT 1,2,3		
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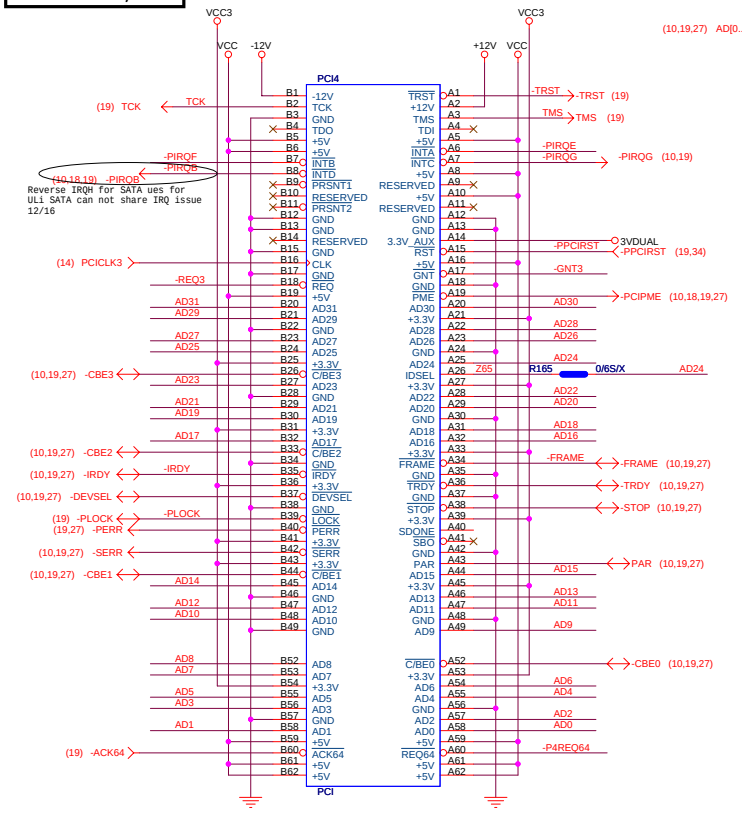
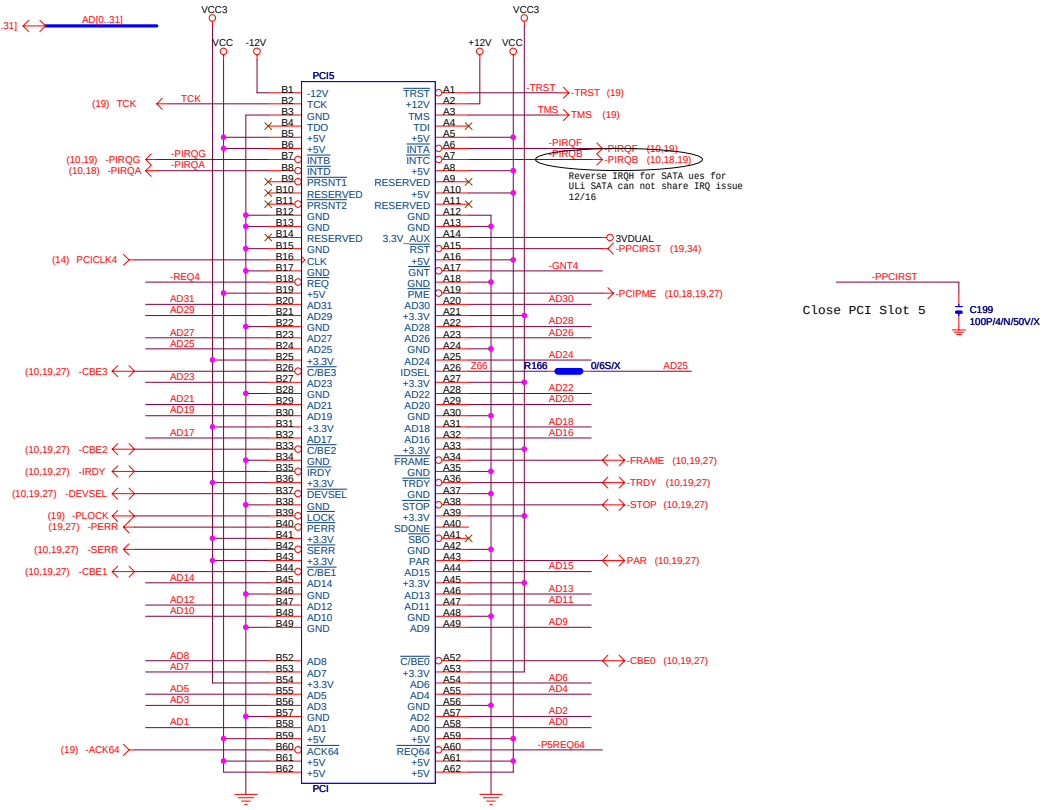
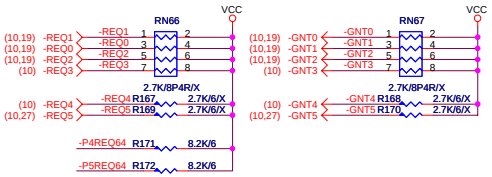
PCI SLOT 4,5

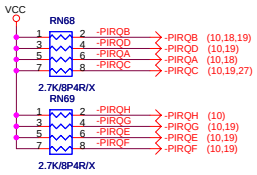


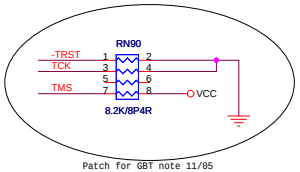
IDSEL(A24)
(A)



IDSEL(A25)
(B)







GIGABYTE		
Title: PCI SLOT 4, 5		
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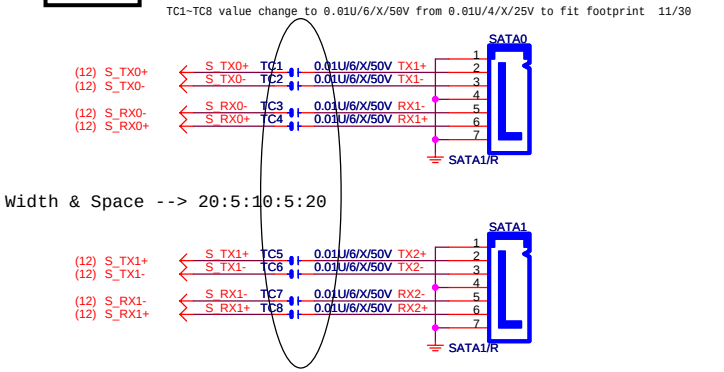
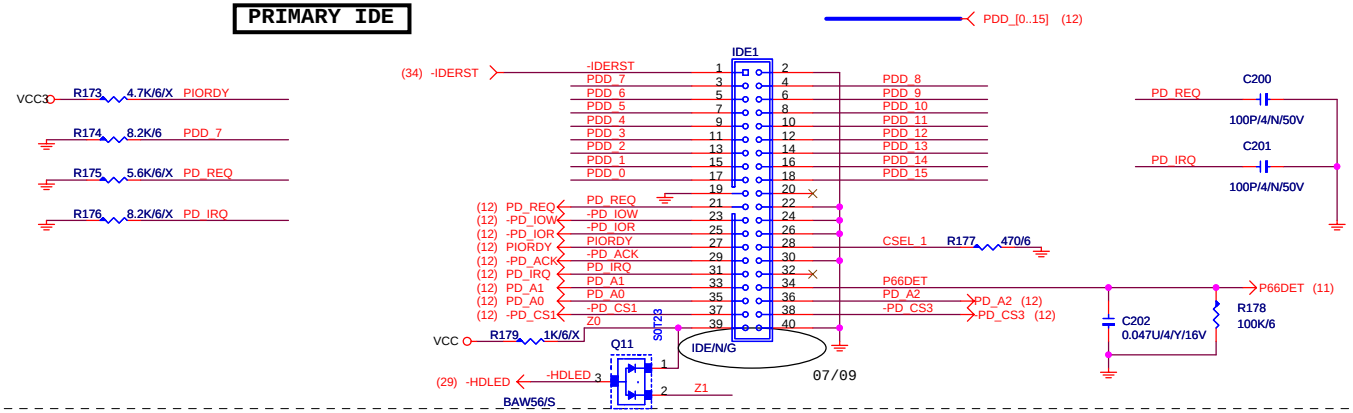
SATA

TC1~TC8 value change to 0.01U/6/X/50V from 0.01U/4/X/25V to fit footprint 11/30

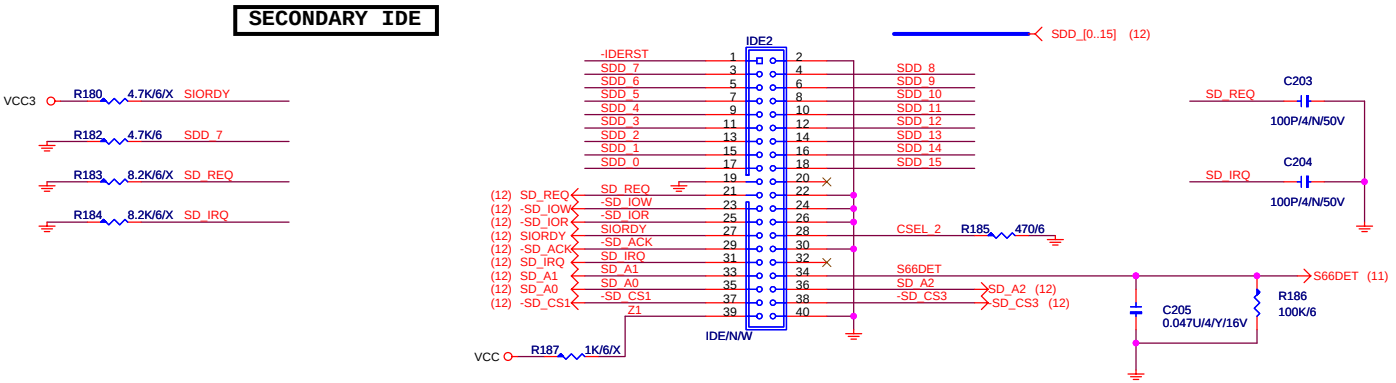
Width & Space --> 20:5:10:5:20



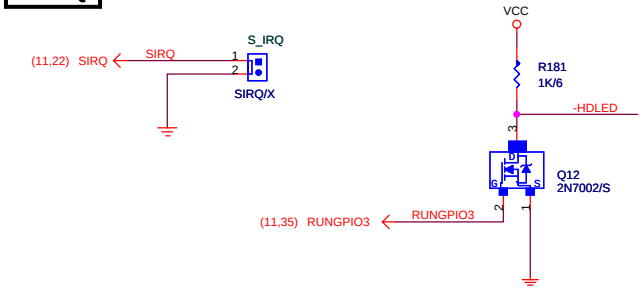
PRIMARY IDE



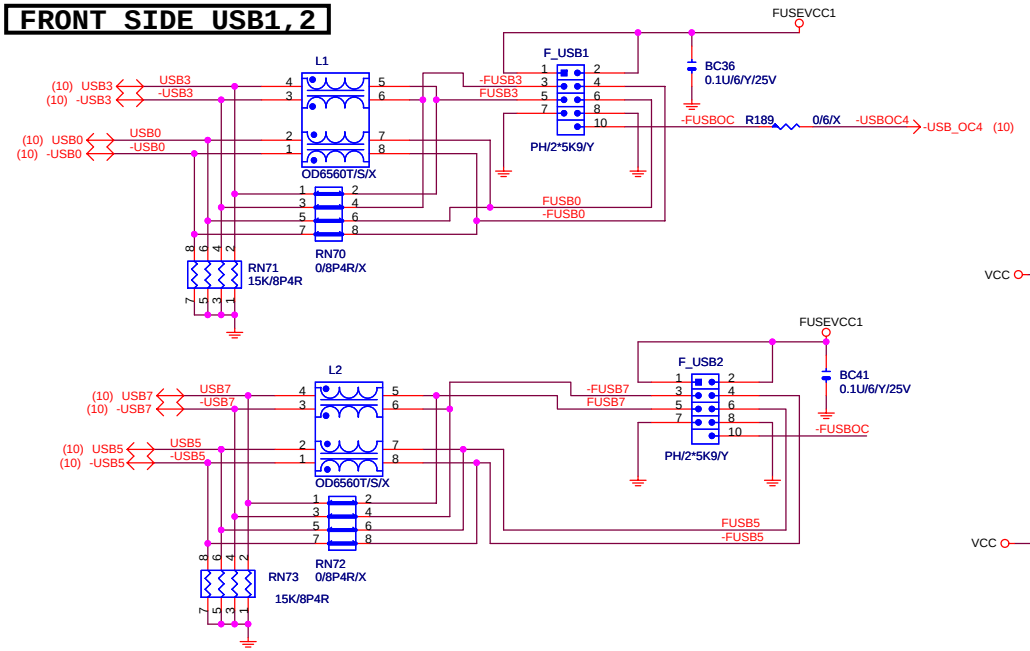
SECONDARY IDE



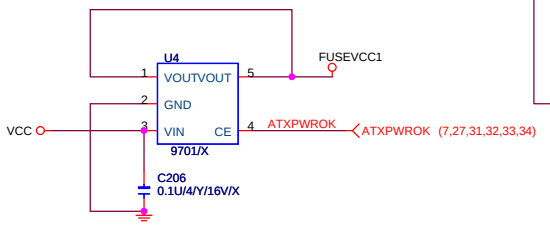
SIRQ



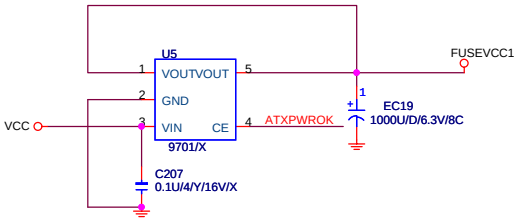
FRONT SIDE USB1,2



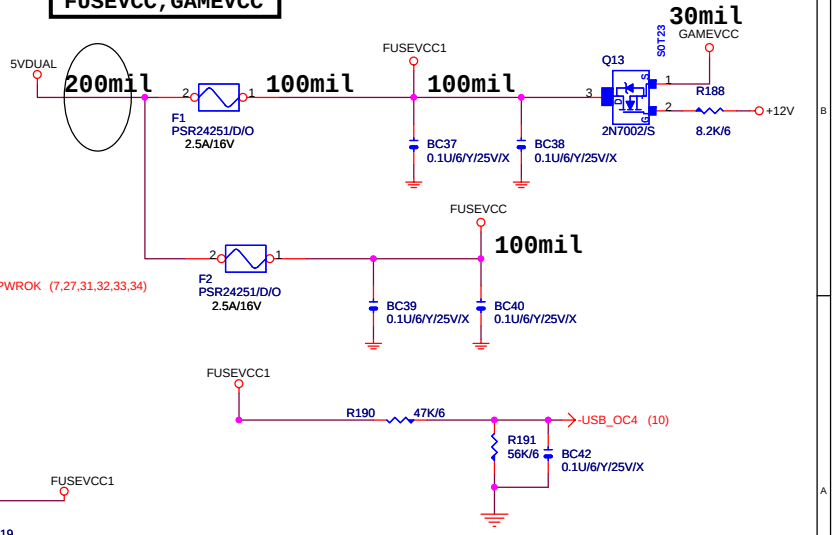
NEAR F_USB1 CONNECTOR



NEAR F_USB2 CONNECTOR



FUSEVCC,GAMEVCC



GIGABYTE

Title	IDE, F_USB , SATA	
Size: Custom	Document Number: GA-K8U-939	Rev: 1.0
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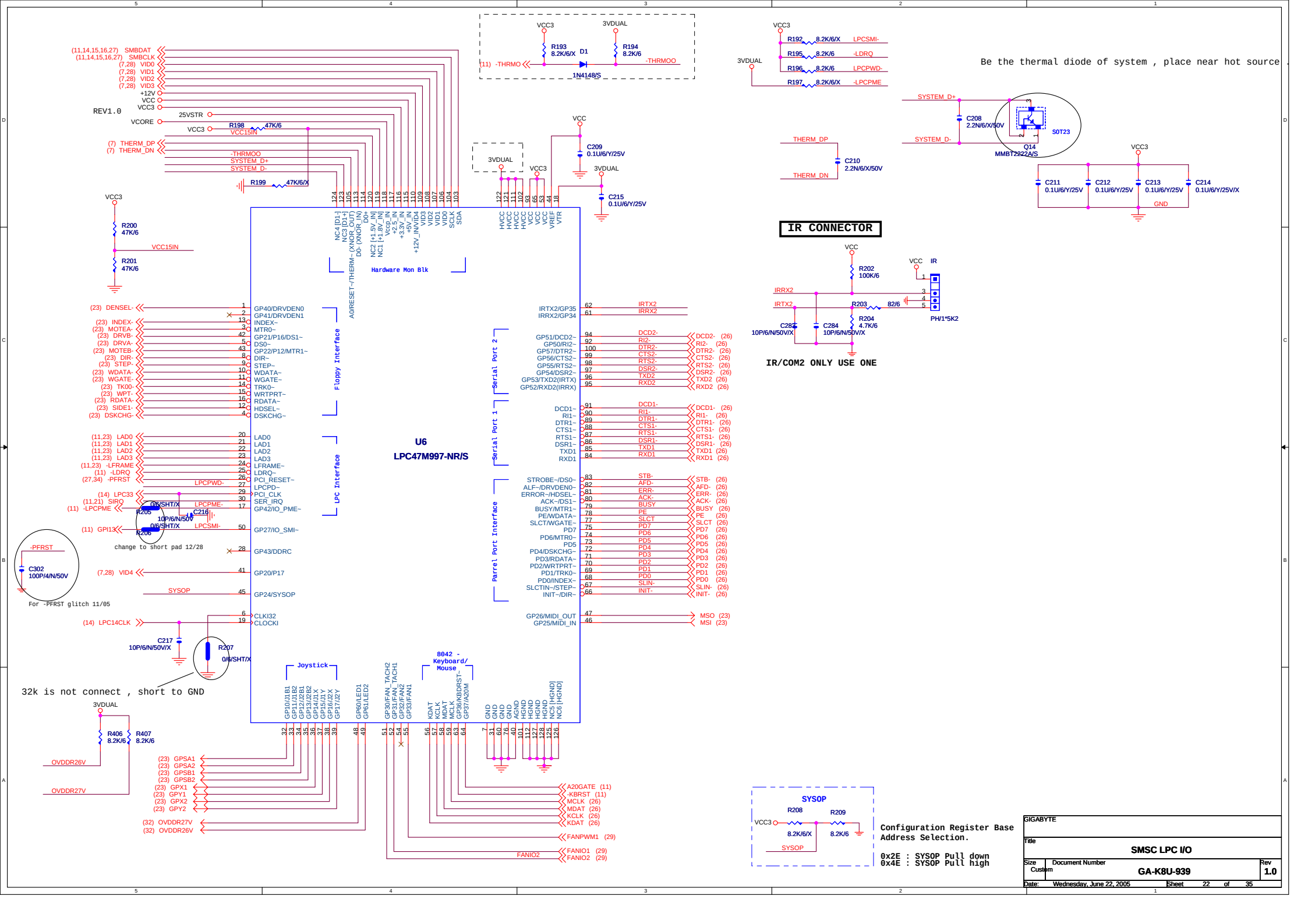
REV1.0
U6
LPC47M997-NR/S
Floppy Interface
LPC Interface
Serial Port 2
Serial Port 1
Parrel Port Interface
Hardware Mon Blk
Joystick
8042 - Keyboard/ Mouse
IR CONNECTOR
IR/COM2 ONLY USE ONE
Be the thermal diode of system , place near hot source .
change to short pad 12/28
For -PFRST glitch 11/05
32k is not connect , short to GND
SYSOP
Configuration Register Base Address Selection.
0x2E : SYSOP Pull down
0x4E : SYSOP Pull high
GIGABYTE
SMSC LPC I/O
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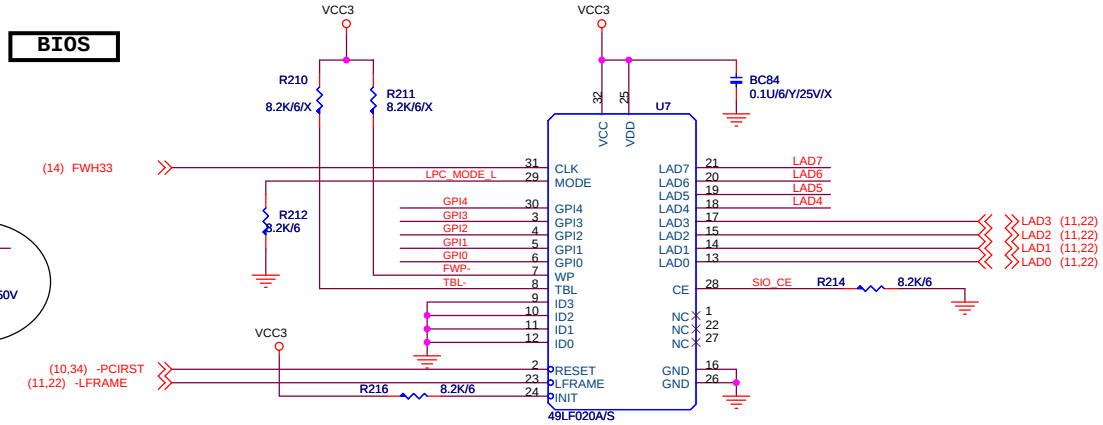
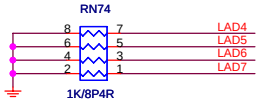
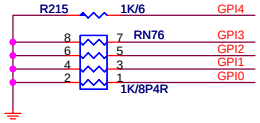
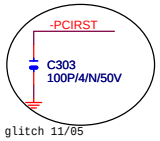
BIOS





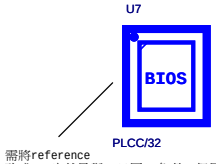




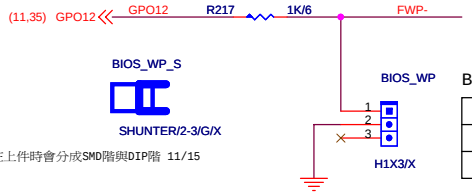
For -PCIRST glitch 11/05

REV 1.0

NOTE: INIT and RESET have the same function internally.



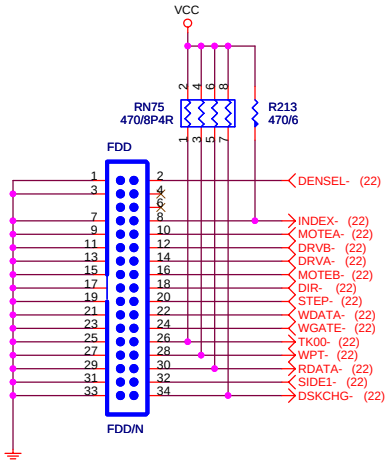
需將reference
改成U7,也就是與BIOS同一參考，但是因爲valu不同，在上件時會分成SMD階與DIP階 11/15



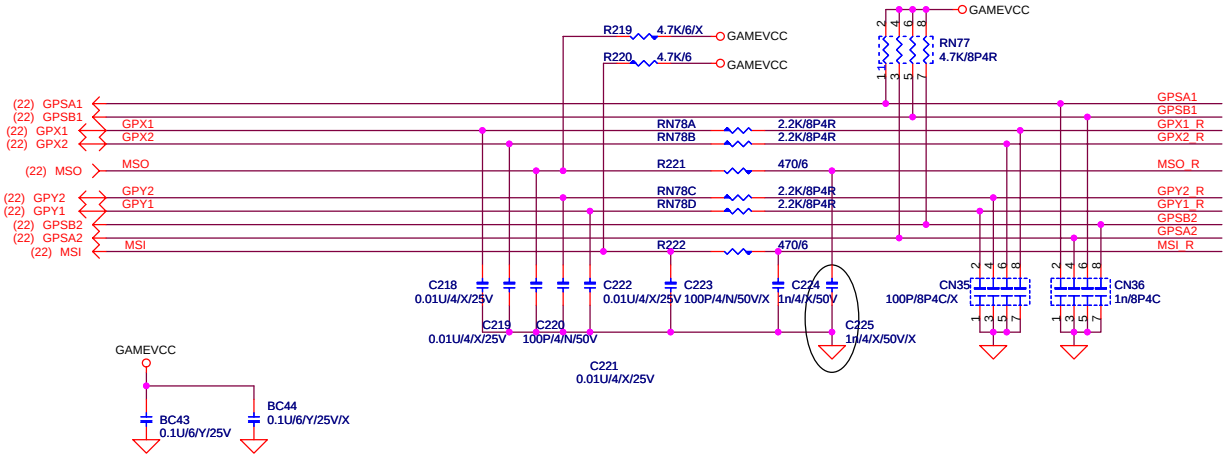
BIOS_WP: BIOS WRITE PROTECT

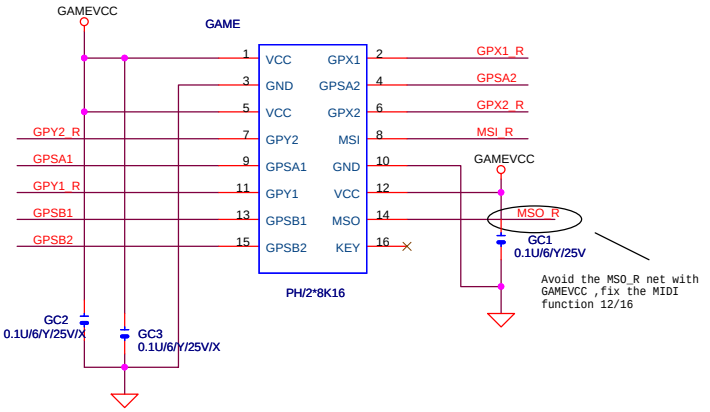
PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)

FDD



GAME PORT





Avoid the MSO_R net with GAMEVCC ,fix the MIDI function 12/16

GIGABYTE

Title	BIOS , FDD , GAME PORT	
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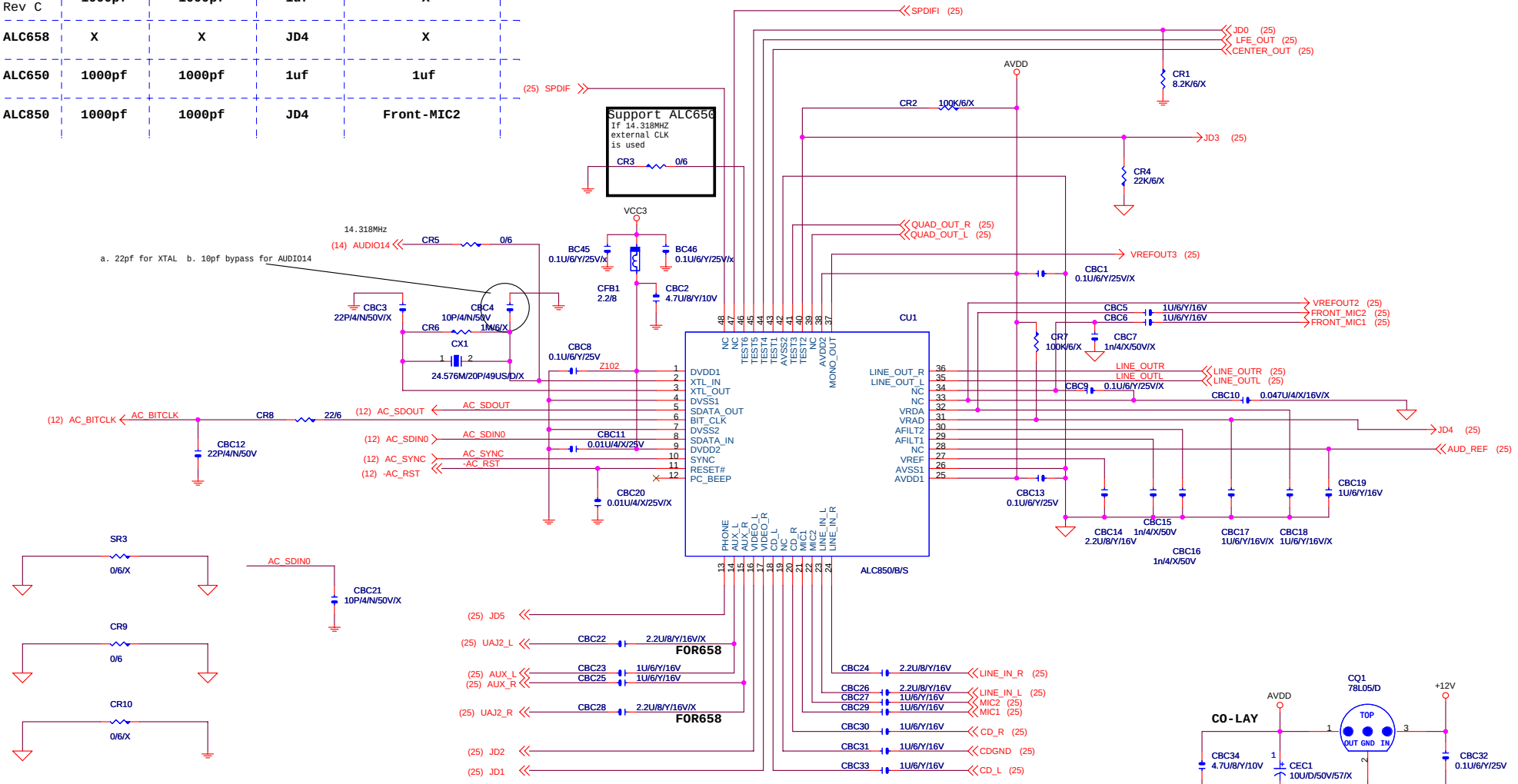
Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT Exernal pull high is needed	for LINE-IN Exernal pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

GIGABYTE	
Title	AUDIO AC97
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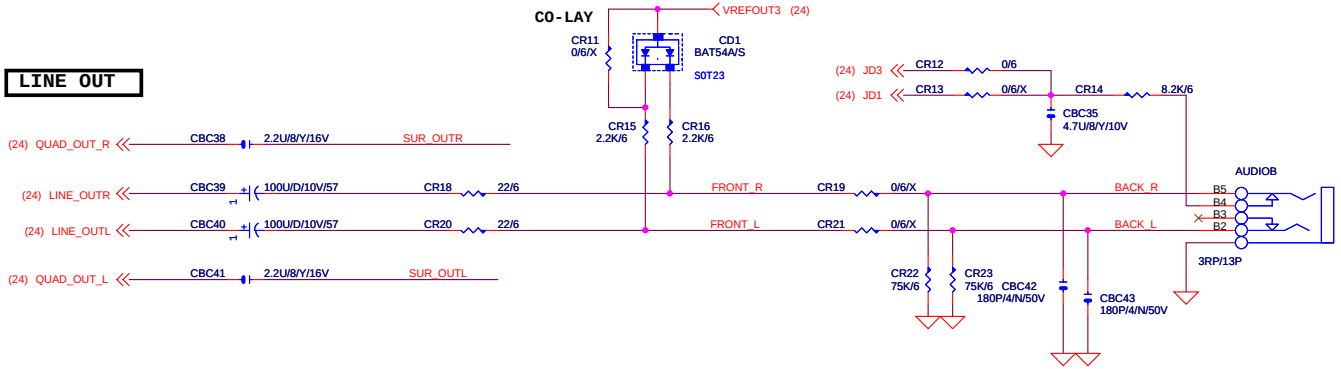
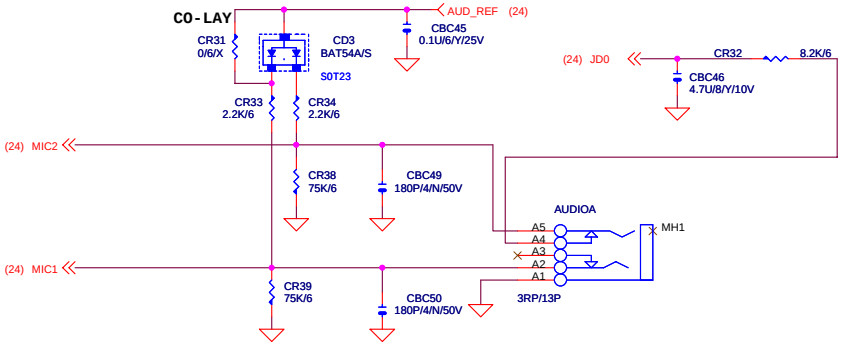
LINE OUT

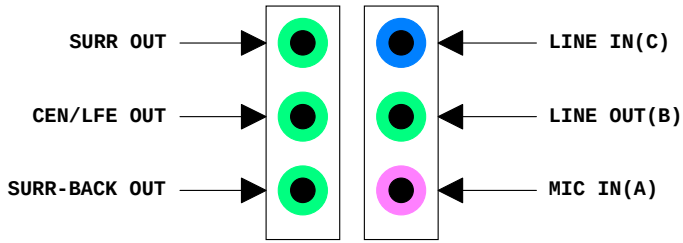


MIC



MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓與CR43,CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm===>microphone in
R<2.3k ohm or R>7.1k ohm===>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

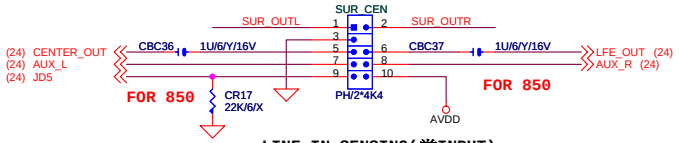


SURR KIT for 850 AUDIO PANEL

2x5 header for 850
For 850 if JD5 = low AUX-In is configued as input
For 850 if JD5 = high AUX-In is configued as output, Surr-Back out

FOR SUPPORT 6 CHANNEL, SURROUND OUT

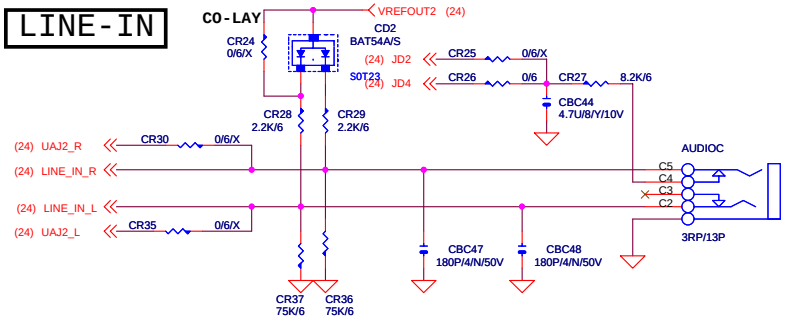
CENTER OUT,LOW FREQUENCY EFFECT OUT



LINE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

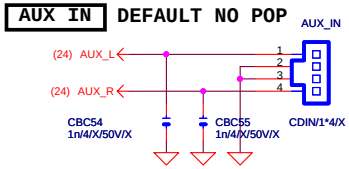
LINE IN SENSING(當INPUT)
swing of input signal>-40dbv(10mv)===>line in device active
swing of input signal<-40dbv(10mv)===>unknown line in device

LINE-IN

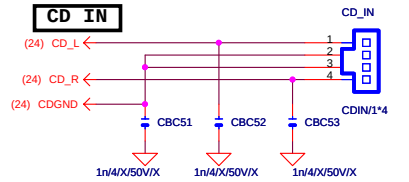


AUX IN

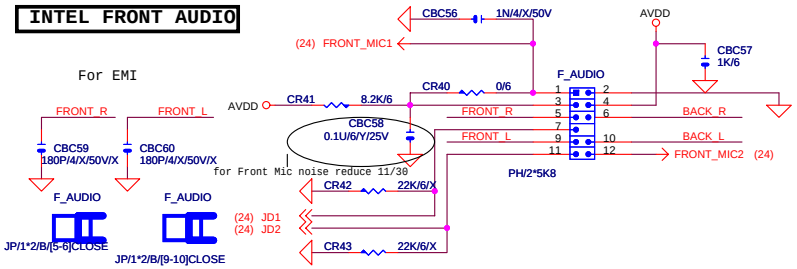
DEFAULT NO POP



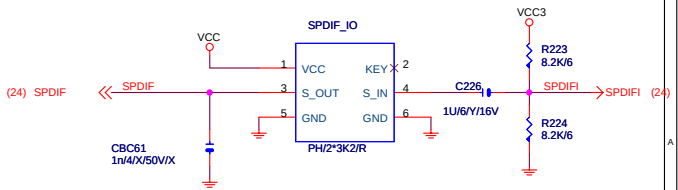
CD IN



INTEL FRONT AUDIO



SPDIF



GIGABYTE

Title: **AUDIO OUTPUT,GAME PORT**

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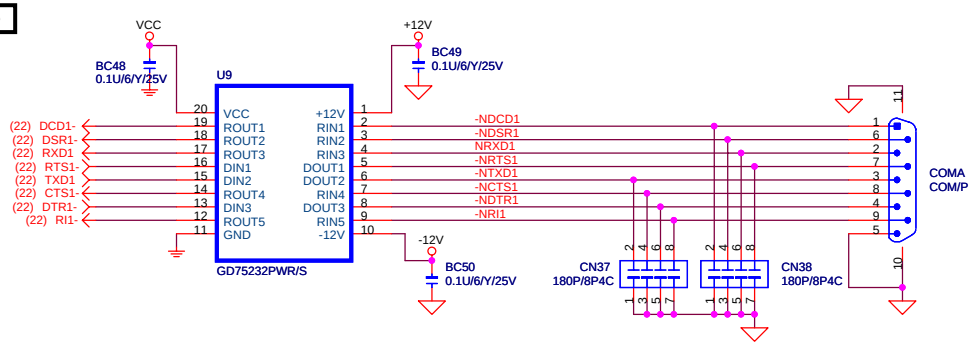
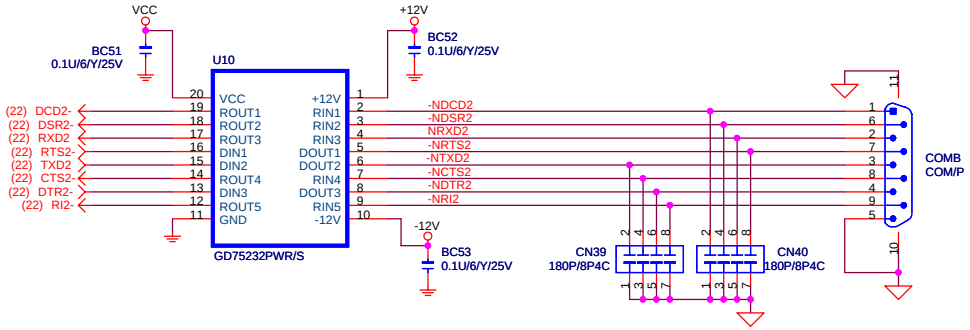
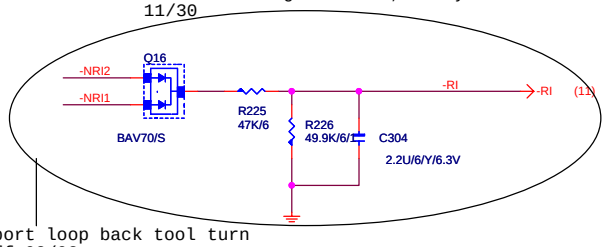
COM A,B





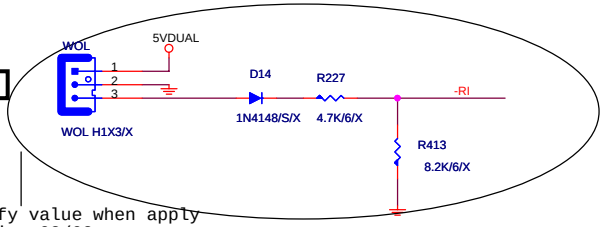
WAKE UP

-RI set to HIgh active ,modify circuit .
11/30



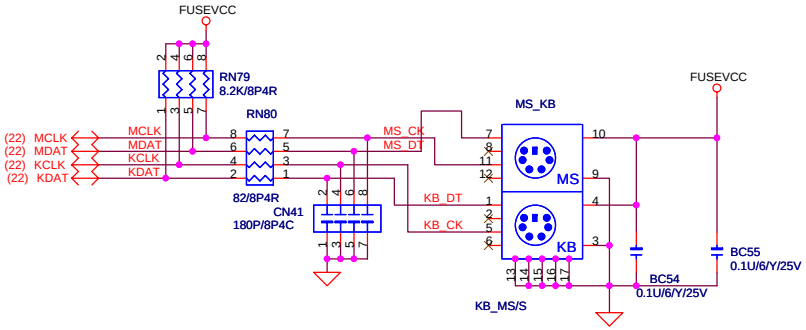
Modify value for com port loop back tool turn
on by RI when power off 02/02

WAKE ON LAN

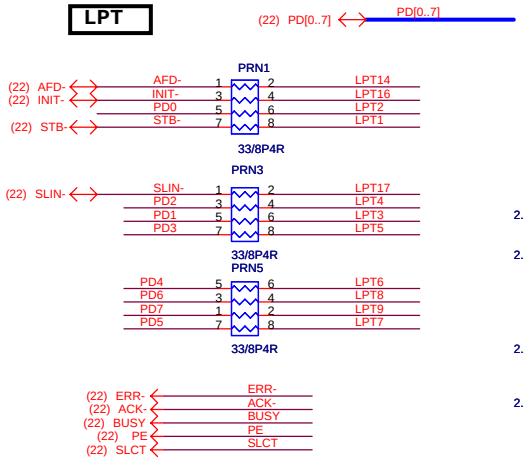


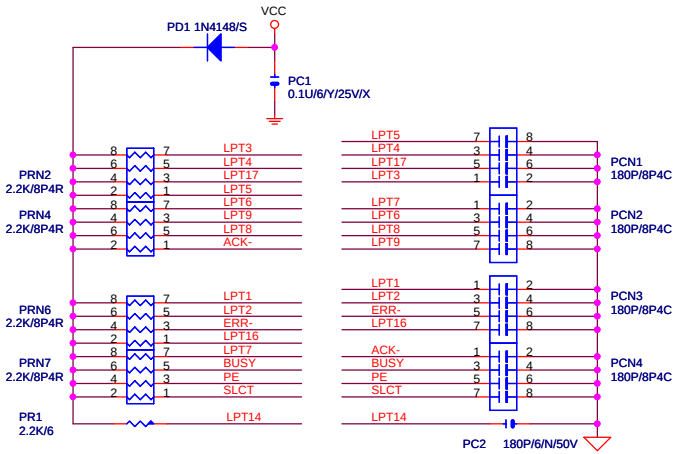
Need verify value when apply
the function 02/02

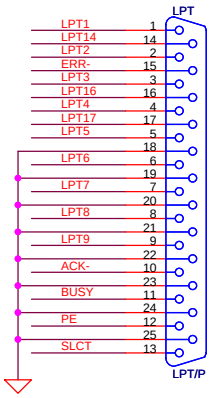
KBC/PS2



LPT







GIGABYTE

Title	COM,PRT,KB/MS,IR
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	10/100 8100C	Giga 8110S	Giga 8110SB
AVDDH	N/A	3.3V	3.3V
V_12P	2.5V	N/A	3.3V
AVDDL	3.3V	2.5V	2.5V
V_DAC	N/A	2.5V	2.5V
DVDD	2.5V	1.8V	1.3V
DVDD_A	2.5V	1.8V	1.3V

		Dual Color LED	
	Yellow	Green	Orange
10Mb	---	OFF	OFF
100Mb	---	ON	OFF
1Gb	---	OFF	ON
Link	ON	---	---
Active	Blink	---	---

POWER DECOUPLING CAP

3VDUAL — LEC1 100U/D/10V/57; LBC1–LBC7 1U/6Y/16V

07/23

LFB1: 100M:N/A 1G:0/8 — LFB1 0/8X; LR3 0/8X; LBC8–LBC14 0.1U/6Y/25V

LR16: 100M:N/A 8110SB:0/8 — V_12P

LFB2: 100M:0/8 1G:N/A — LFB2 0/8

LFB3: 100M:0/8 1G:N/A — LFB3 0/8; LBC15–LBC18 0.1U/6Y/25V; LEC2 100U/D/10V/57

LQ1: 100M:N/A 2SB1132 — LQ1 2SB1132/SOT89/X; CTRL25; AVDDL

For : Gigabyte LAN

LQ3: 100M:2N2907A 1G:N/A — LR6 0/6 CTRL25; CTRL_DVDD; LQ3 2907/SOT23

DVDD: 100M:2.5V 1G:1.8V — LR8 0/6 DVDD_A; LEC3 100U/D/10V/57; LBC20–LBC24 0.1U/6Y/25V

LQ2 AMS1117/SOT223/X — LR7 100/6/1/X; LR9 44.2/6/1/X; CTRL18; LBC19 0.1U/6Y/25V/X

LR1 5.6K/6 3VDUAL

LR2 8.2K/6/X 3VDUAL

LR2: 93C46:N/A 93C56:8.2K/6

LX1 25M/20p/20ohm/49US/D; LC1 27P/4/N/50V; LC2 27P/4/N/50V

LC3 0.1U/4/Y/16V; LR4 5.9K/6/1

LR4: 100M:5.9K/6/1 1G:2.49K/6/1

LU1: 100M:RTL8100C 1G:RTL8110S

RTL8100C/S

LR5: 100M:N/A 8110SB:0/6 — LR5 0/6/X; -PFRST; LC4 100P/6/N/50V

LR10 1K/6; LR11 15K/6; ISOLATE; DVDD

-PIRQC; -PFRST; LANCLK; -GNT5; -REQ5; -PCIPME

LAN EEPROM

LU2 AT93C46/S — L_EECS; L_EESK; L_EEDI; L_EEDO; LBC25 0.1U/4/Y/16V

LR24~LR27: 100M:N/A 1G:49.9/6/1

LBC32, LBC33: 100M:N/A 1G:0.01U/6

IDESEL 26

-REQ5/-GNT(5)

-PIRQC

-IRDY; -FRAME; -CBE2; -CBE3; -CBE1; -CBE0; PAR; -SERR; -SMBDAT; -SMBCLK; -PERR; -STOP; -DEVSEL; -TRDY

LR12 22/6/X; LR13 22/6/X; LR14 8.2K/6/X

R230 0/6/X; R231 0/6/X; SR4 9/6/SHT/X; R232 0/6/X; R233 0/6/X

07/28

FOR EMI

REAR USBX2

Close to USB port

FUSEVCC — EC21 100U/D/10V/57; R228 47K/6; R229 56K/6; -USB_OC3 (10)

RN81 0/8P4R/SHT/X; L3 OD6560T/X; RN82 15K/8P4R

(10) USB6; (10) -USB6; (10) USB4; (10) -USB4; RUSB6; -RUSB6; RUSB4; -RUSB4

In sloder side 11/04

SLU1 SLVU2.8-4/S/X; SLU2 SLVU2.8-4/S/X

Spacing : at least 50 mils between each differential pair

MDI0+; MDI0-; MDI1+; MDI1-; MDI2+; MDI2-; MDI3+; MDI3-

LR20–LR27 49.9/6/1 / 49.9/6/1X

LBC30 0.01U/6/X/50V; LBC31 0.01U/6/X/50V; LBC32 0.01U/6/X/50V/X; LBC33 0.01U/6/X/50V/X

LR22, LR23, LBC26 Close to Lan Chip
Realtek suggestion (TX+, TX-).

LR24, LR25, LBC27 Close to Lan Chip
Realtek Suggestion (RX+, RX-).

LBC26: 100M:N/A 1G:N/A — AVDDL; LR15 0/6/X; LBC26 0.1U/6/Y/25V/X

LR15: 100M:N/A 1G:0/6

LBC25: 100M:0.1U/6 1G:0.01U/6

USB_LAN — UP; DOWN

USB/LAN/100

FOR 1G:P35-152-19W9 11NR6-702009-01

FOR 100M:P35-152-11Z9 11NR6-702010-01

L_YEL-; YELLOW; GREEN-; ORANGE-; LR16 150/6; LR17 150/6; -RUSB4; RUSB4; -RUSB6; RUSB6

LFB4 0/8 For EMI; LBC27 0.1U/6Y/25V; LBC29 0.1U/6/Y/25V/X

For 8100C

FUSEVCC

YELLOW- LR19 0/6 L_YEL-

For 8110S

YELLOW- LR28 0/6/X YELLOW; L_10M- D2 1N4148/S/X L_YEL-; GREEN-; ORANGE-; D3 SOT23 BAW56/S/X

NEAR USB_LAN CONNECTOR

U11 9701/X — VOUTVOUT; GND; VIN; CE; FUSEVCC; ATXPWROK; ATXPWROK (7,21,31,32,33,34)

VCC; C227 0.1U/4/Y/16V/X

Title	GIGABYTE		
	LAN RTL8100C		
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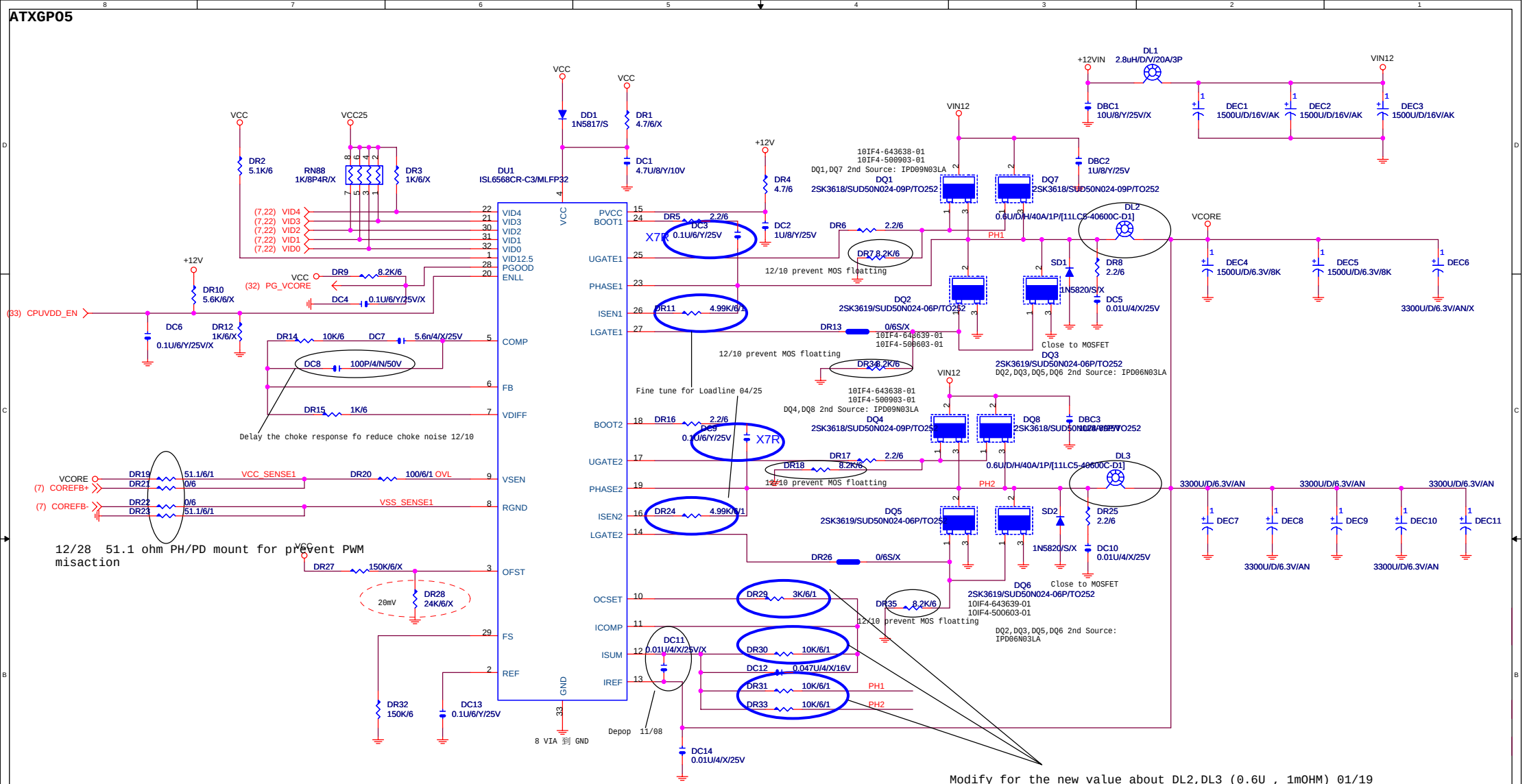
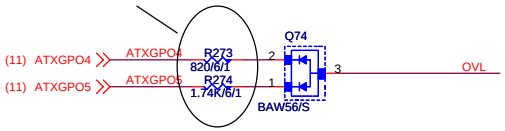
ATXGP05



12/28 51.1 ohm PH/PD mount for prevent PWM misaction

Modify for the new value about DL2,DL3 (0.6U , 1mOHM) 01/19

Fine tune the vaule for over voltage 12/09



	ATXGP04	ATXGP05
5%	HI	LO
7.5%	LO	HI
10%	LO	LO
Default	HI	HI

GIGABYTE

Title: VCORE (PWM ISL6568CR)

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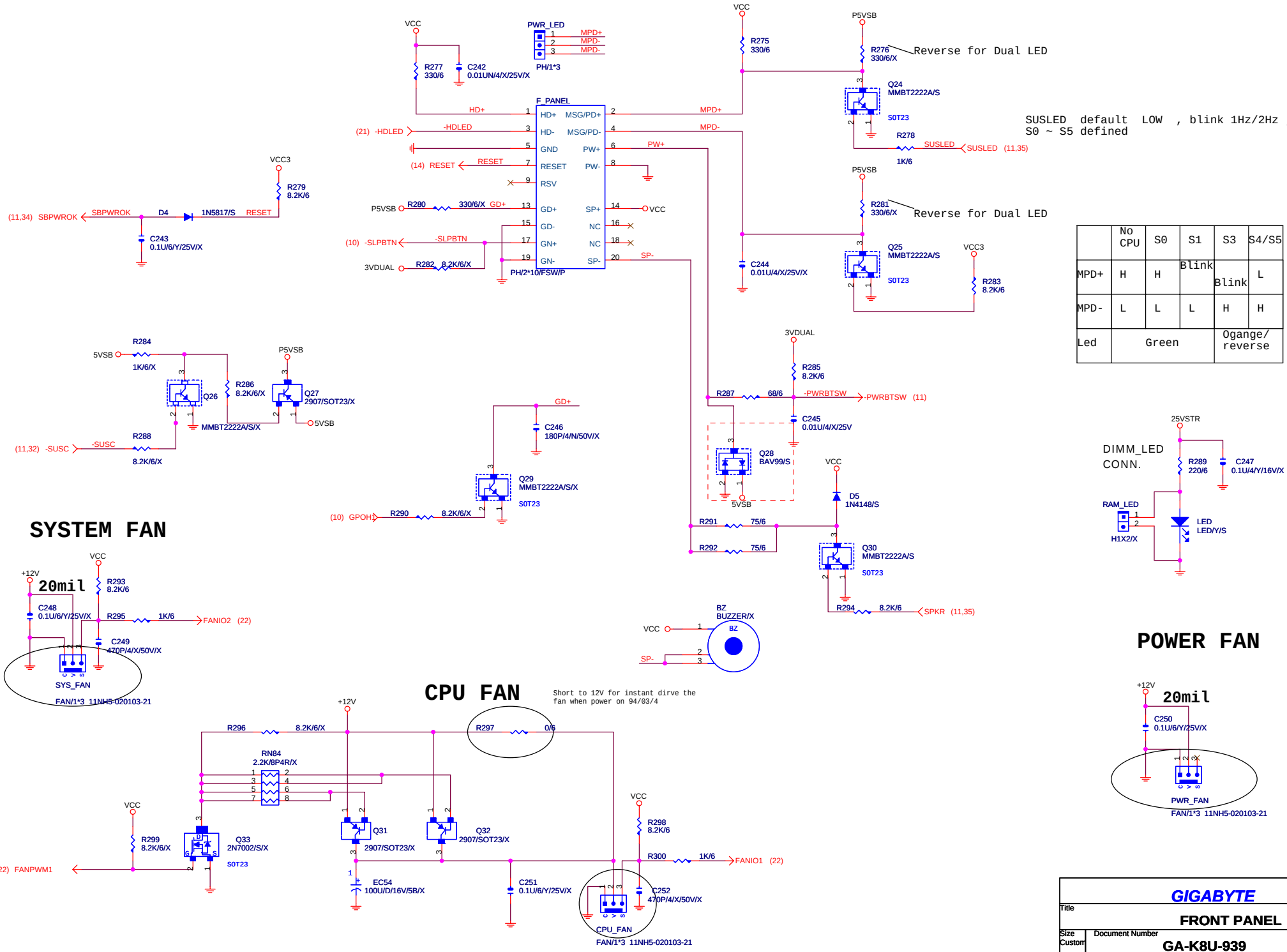

	No CPU	S0	S1	S3	S4/S5
MPD+	H	H	Blink	Blink	L
MPD-	L	L	L	H	H
Led	Green			Ogange/ reverse	

GIGABYTE			
Title	FRONT PANEL		
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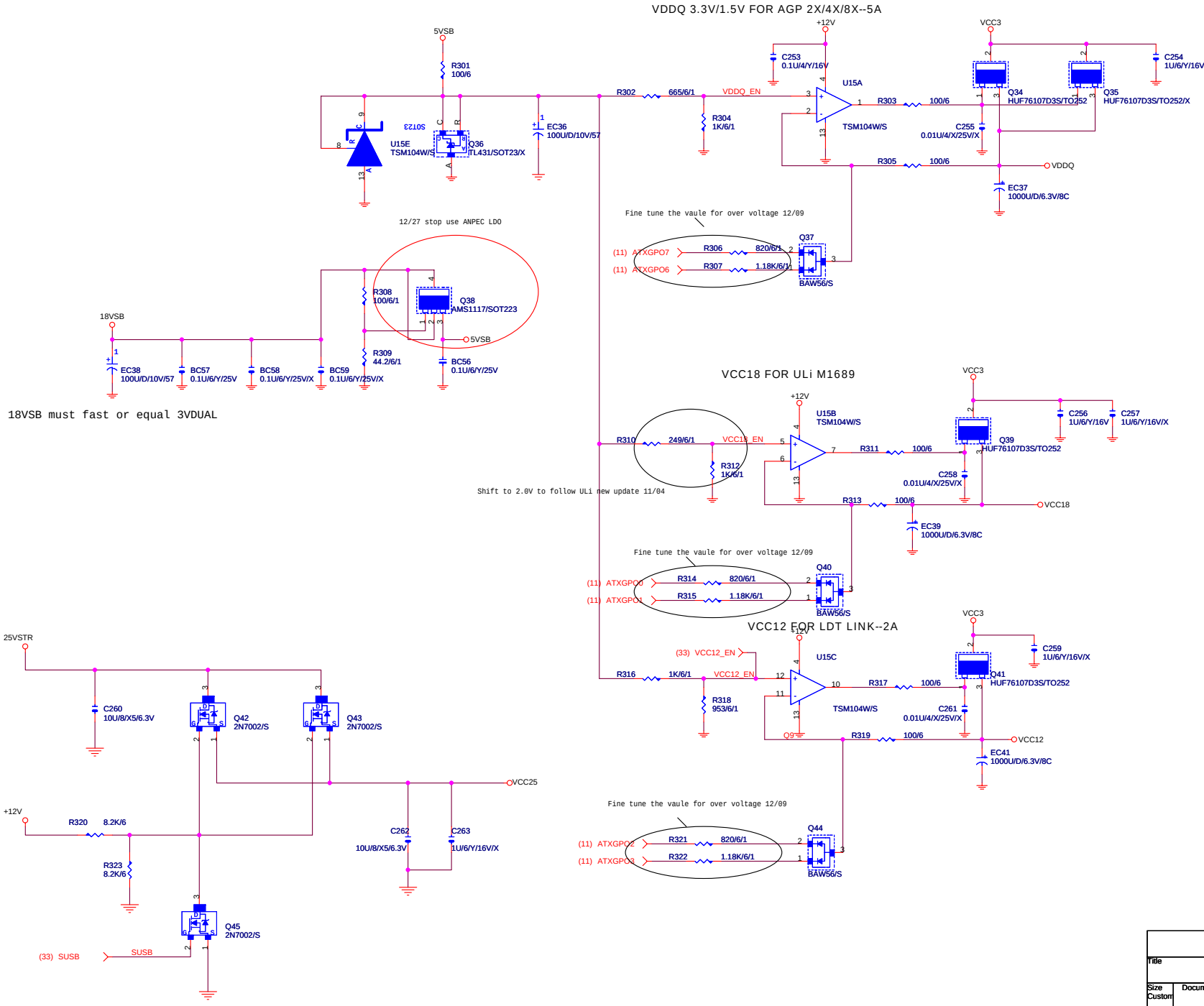

GIGABYTE

Title: VCC12,VCC18,VCC25,VDDQ		
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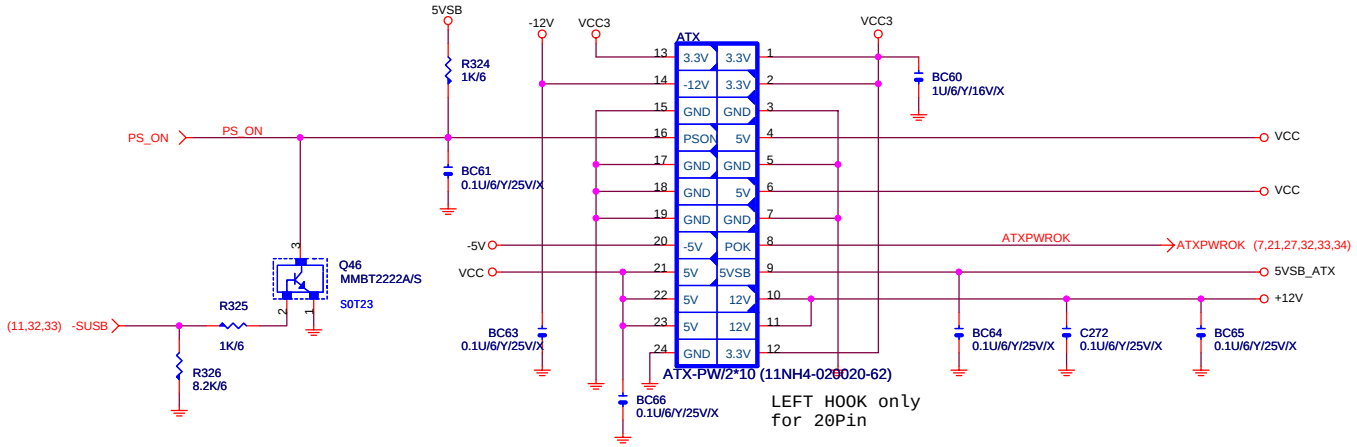
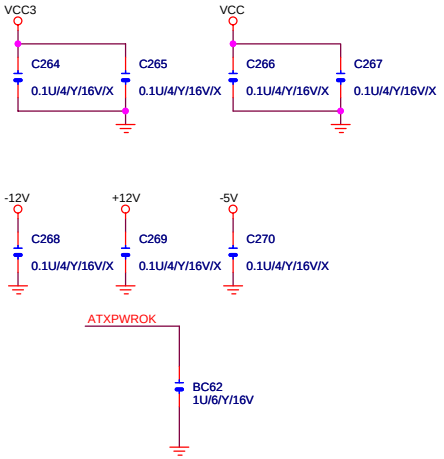
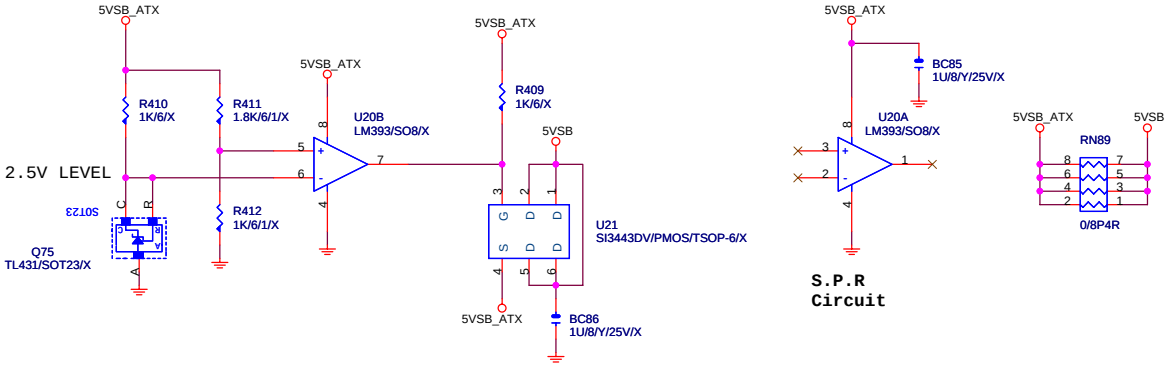
ATX CONN, DC POWER

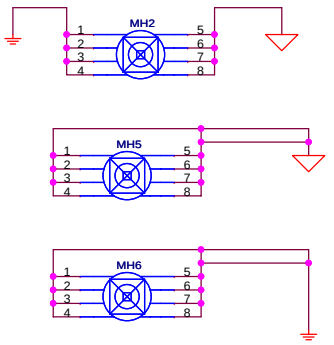
ATX POWER CONNECTOR



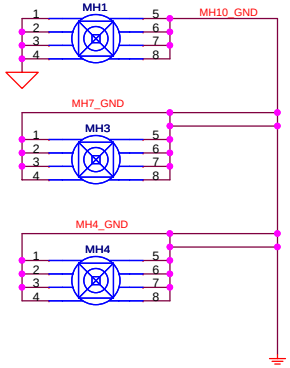


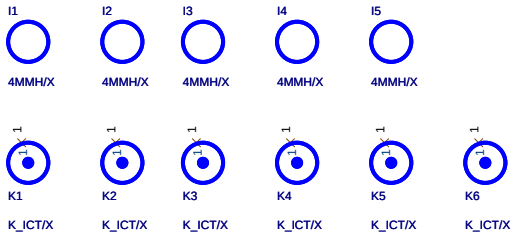


NOTE: MH2 is placed near audio.



ATX-12V CONNECTOR





LAYOUT: Located near PS/2 ports
and connects all I/O port CGND's

GIGABYTE		
Title: ATX, DC POWER		
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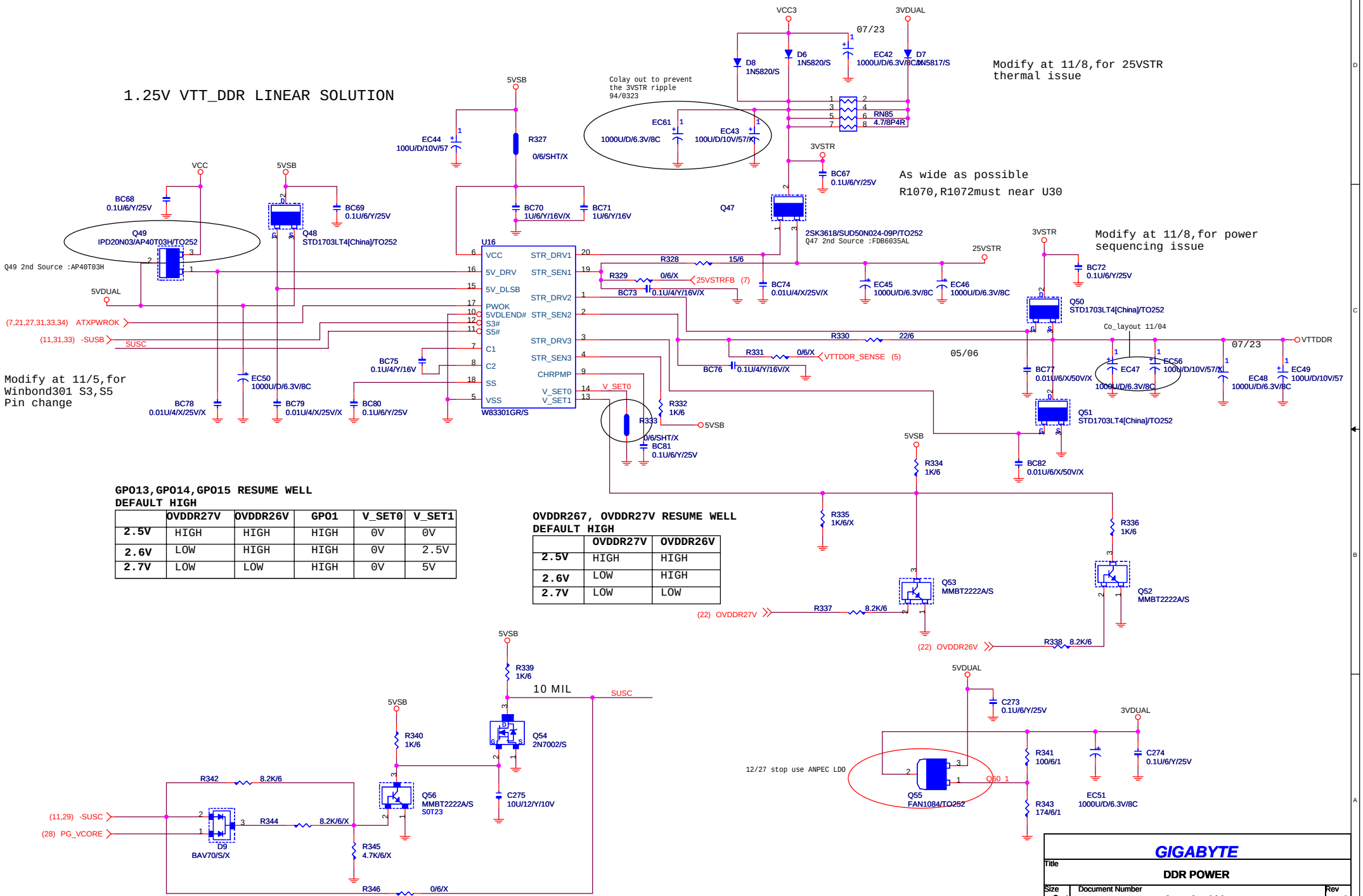
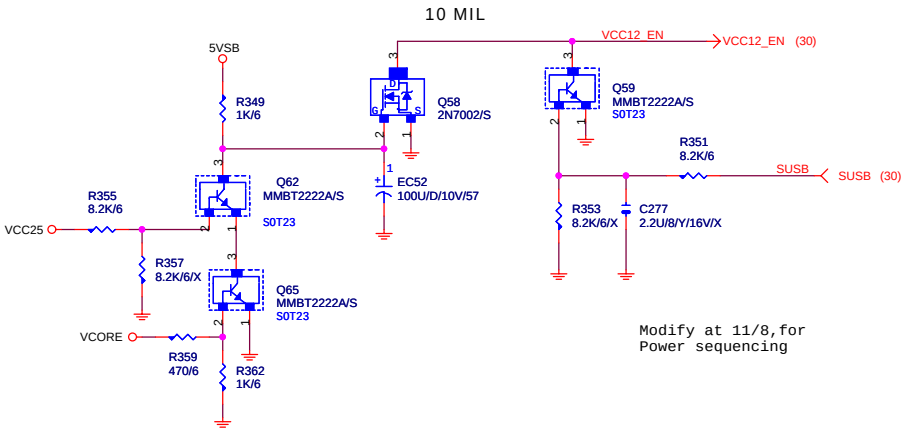
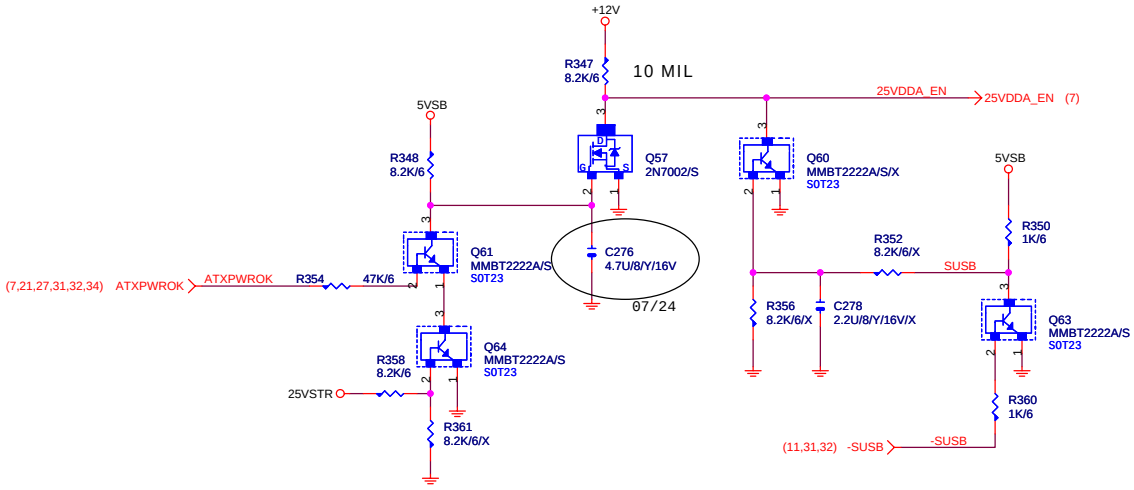


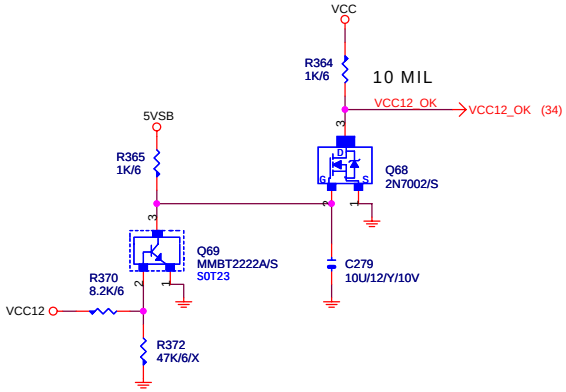
	OVDDR27V	OVDDR26V	GPO1	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V

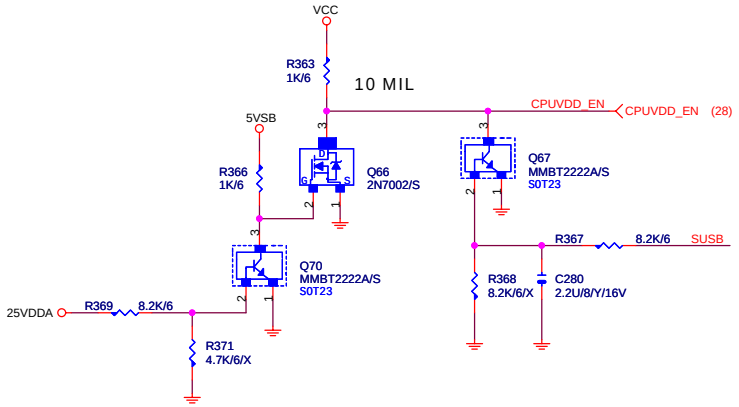
	OVDDR27V	OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW



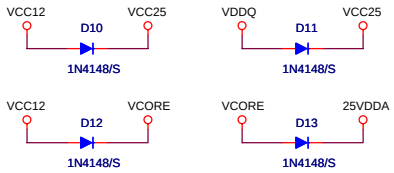
Modify at 11/8,for
Power sequencing







Remove IT8282 power sequence controller IC 94/03/23



GIGABYTE

Title	POWER SEQUENCE	
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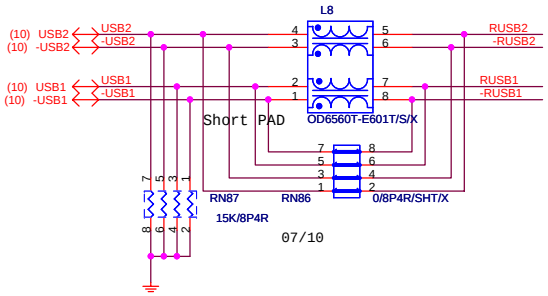
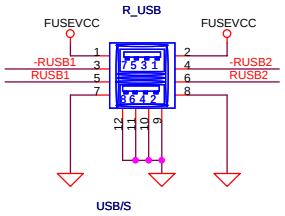
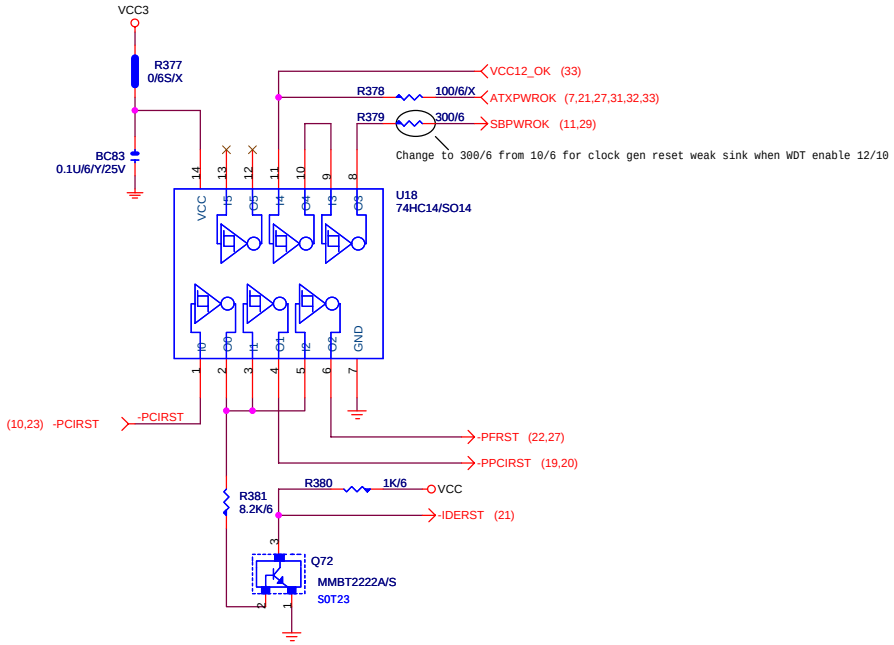
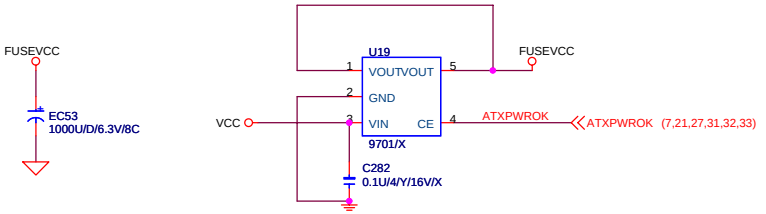
REAR USBX2







NEAR R_USB CONNECTOR



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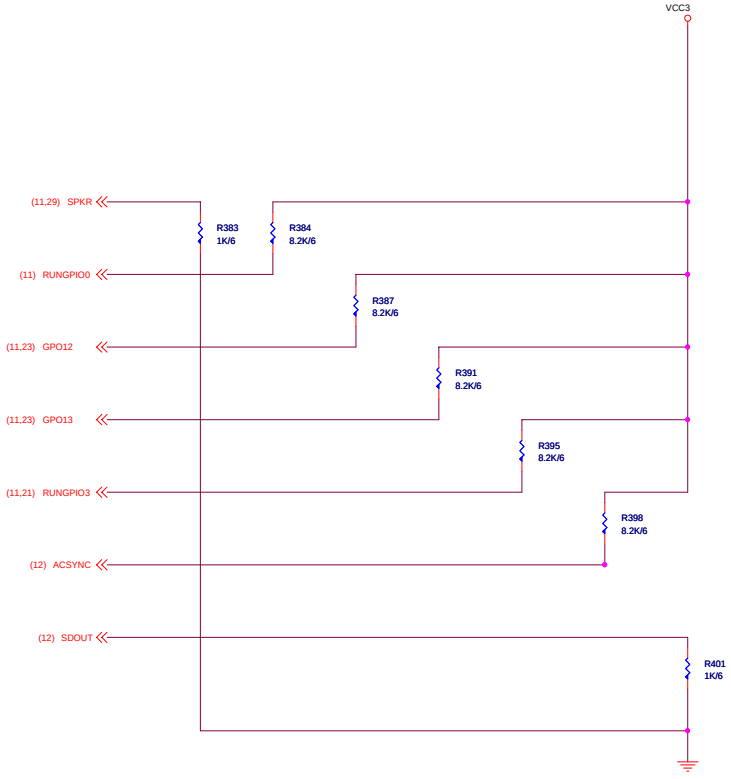
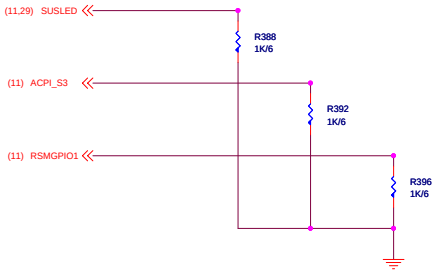
HW SETTING

The HW setting fixed for MP , remove the unuse resistor footprint





H:8.2K L:1K			
R388 SUSLED	(Default)	L	Normal Operation Mode
		H	Enable 32K Test Mode to select external 32K clock source from 32K Clock Test input pin ACPWR
R383 SPKR	(Default)	L	Normal Operation Mode
		H	Enable Debug Mode to route requests of internal high-speed PCI devices externally and replace requests form PCI slots
R384 RUNGPIO0		L	33MHz reference input for HTT PHY PLL
	(Default)	H	66MHz reference input for HTT PHY PLL
R387 GPO12		L	Enable Simulatio Mode to reduce reset active duration for pattern simulation
	(Default)	H	Normal Operation Mode
R391 GPO13		L	Enable Tester Mode to bypass PLL clock and select the external clock source form input pad PCICLK
	(Default)	H	Normal Operation Mode
R395 RUNGPIO3		L	External PCI bus type select to BUS0
	(Default)	H	External PCI bus type select to BUSN

H:8.2K L:1K				
R398 ACSYNC	R401 SDOUT	L	L	On chip core PLL output clock setting 33MHZ
		L	H	66MHZ
		H	L	133MHZ (Default)
		H	H	33MHZ
R396 RSMGPIO1	R392 ACPI_S3	L	L	HTT Unit ID of on-chip host bridge is assigned as 0 (Default)
		L	H	HTT Unit ID of on-chip host bridge is assigned as 2
		H	L	HTT Unit ID of on-chip host bridge is assigned as 3
		H	H	HTT Unit ID of on-chip host bridge is assigned as 4
RSMGPIO2	Look page 11			

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H/W SETTING		
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