# CK804A07

## nVIDIA CK804 Chipset forAM2 CPU

## 10/25/2006)


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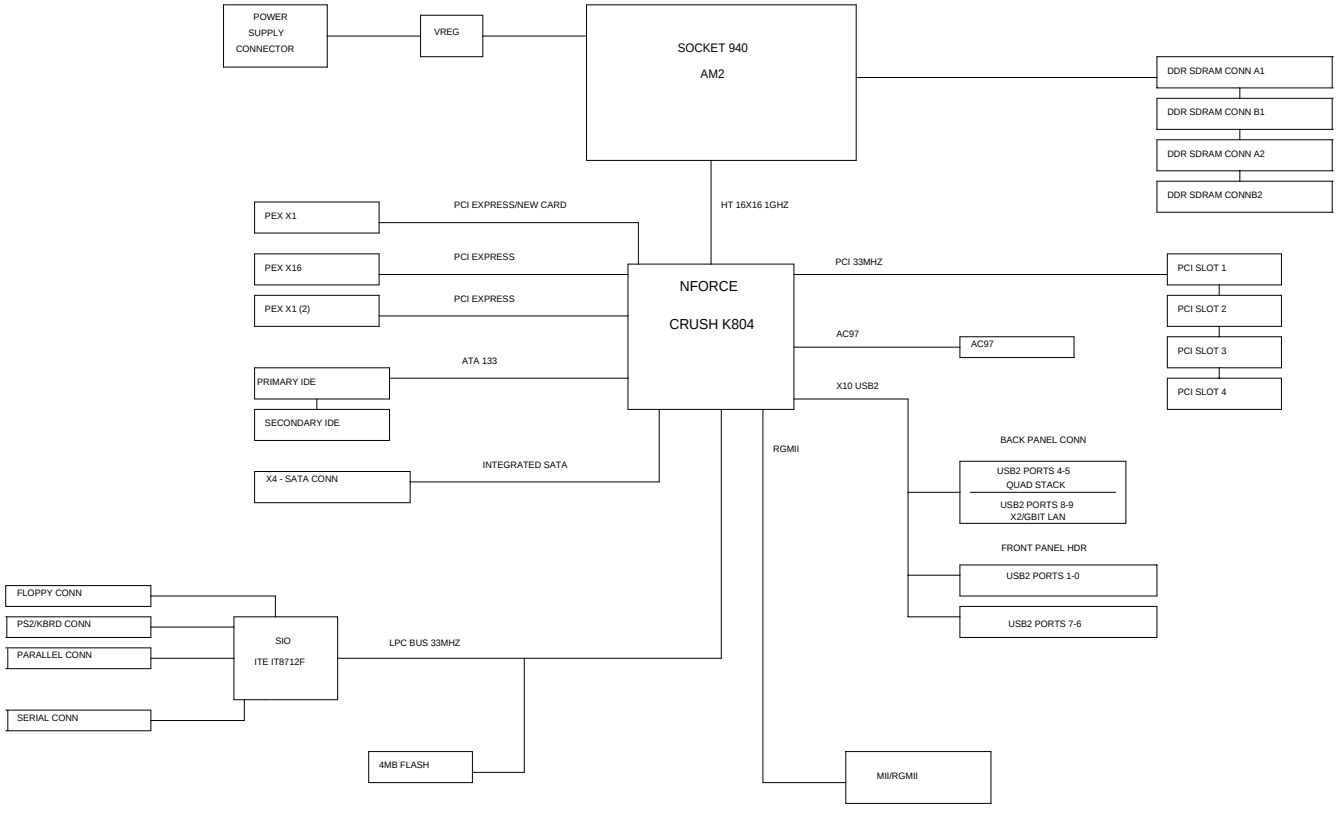
# BLOCK DIAGRAM

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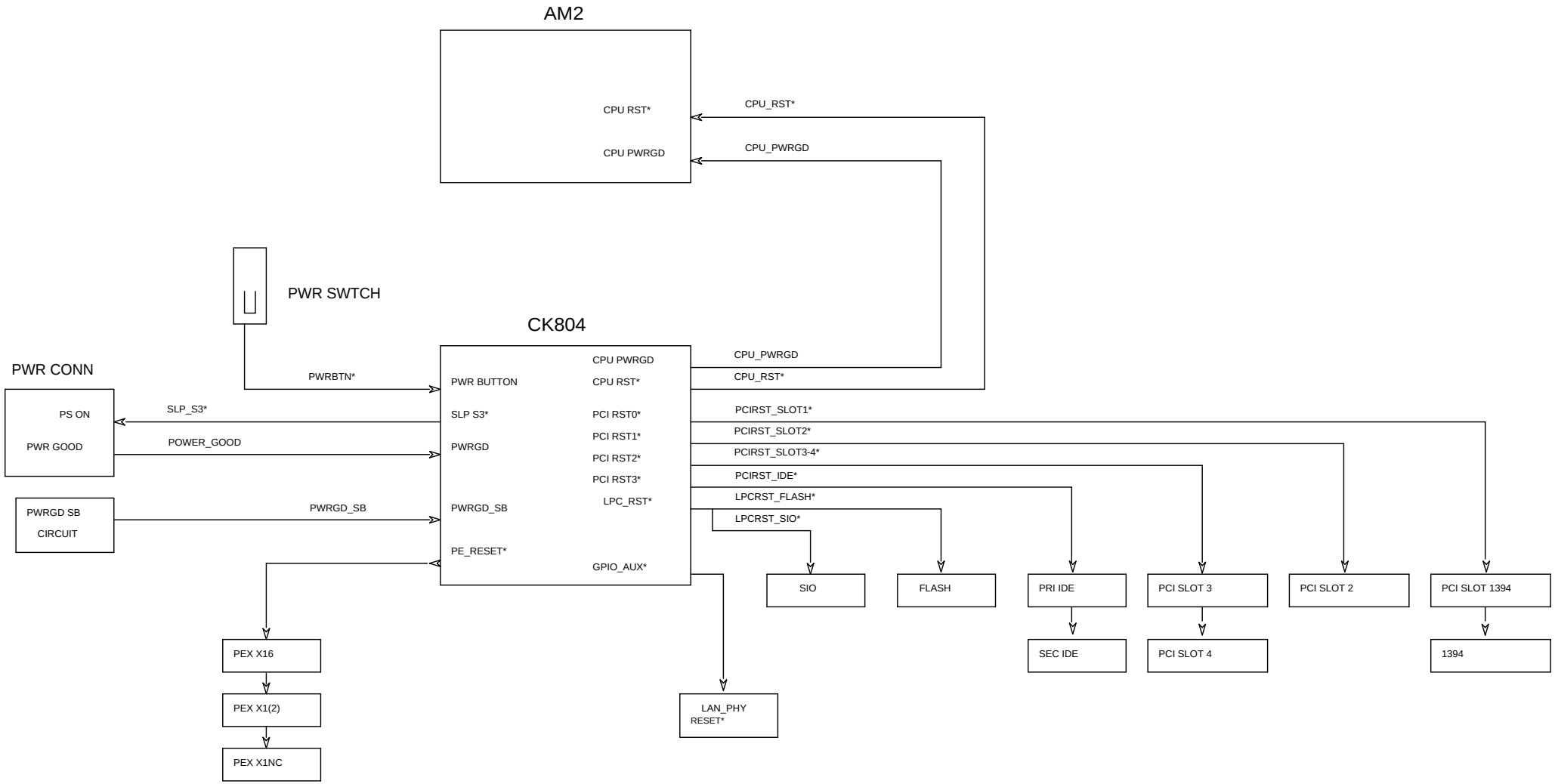
# RESET MAP

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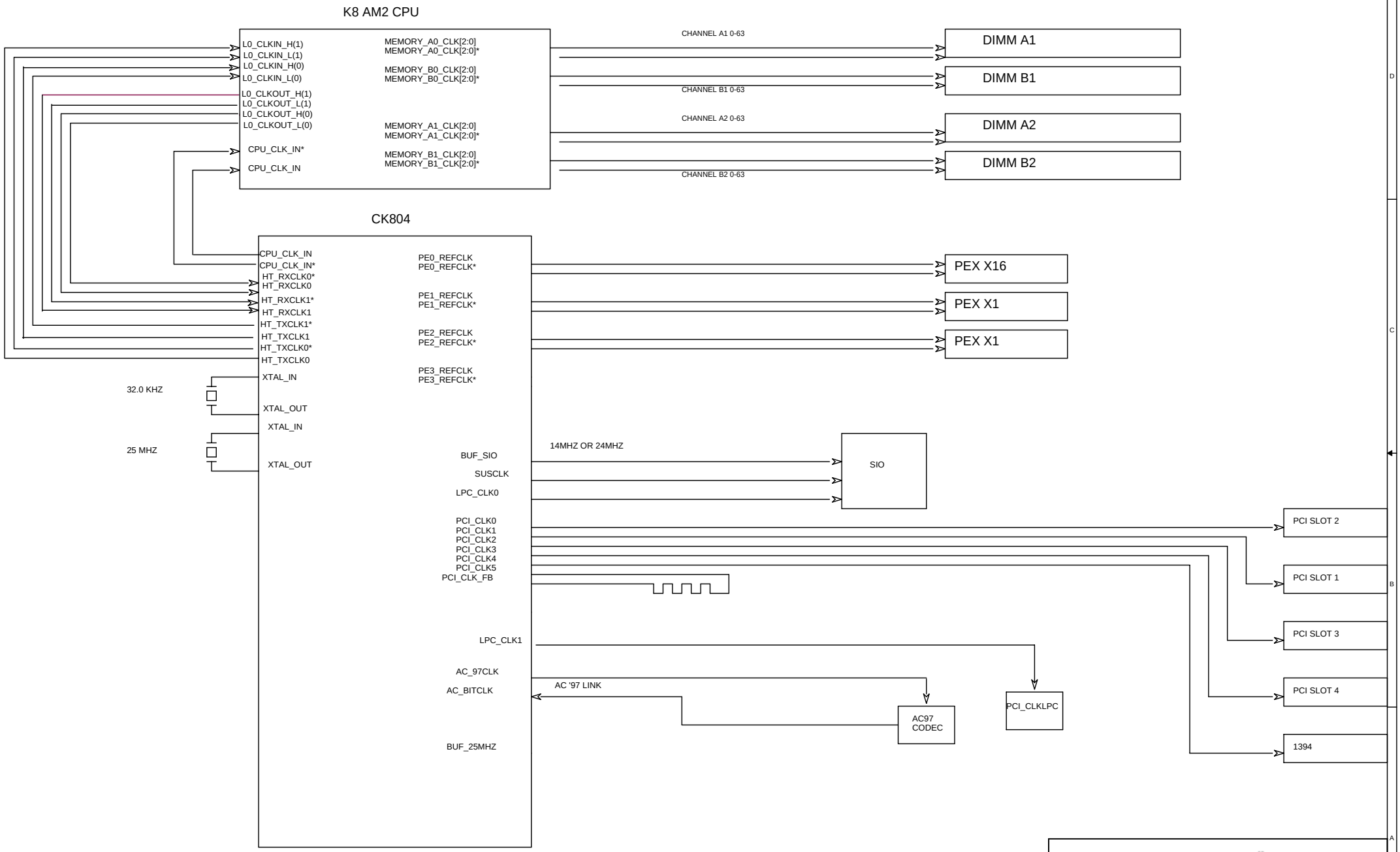


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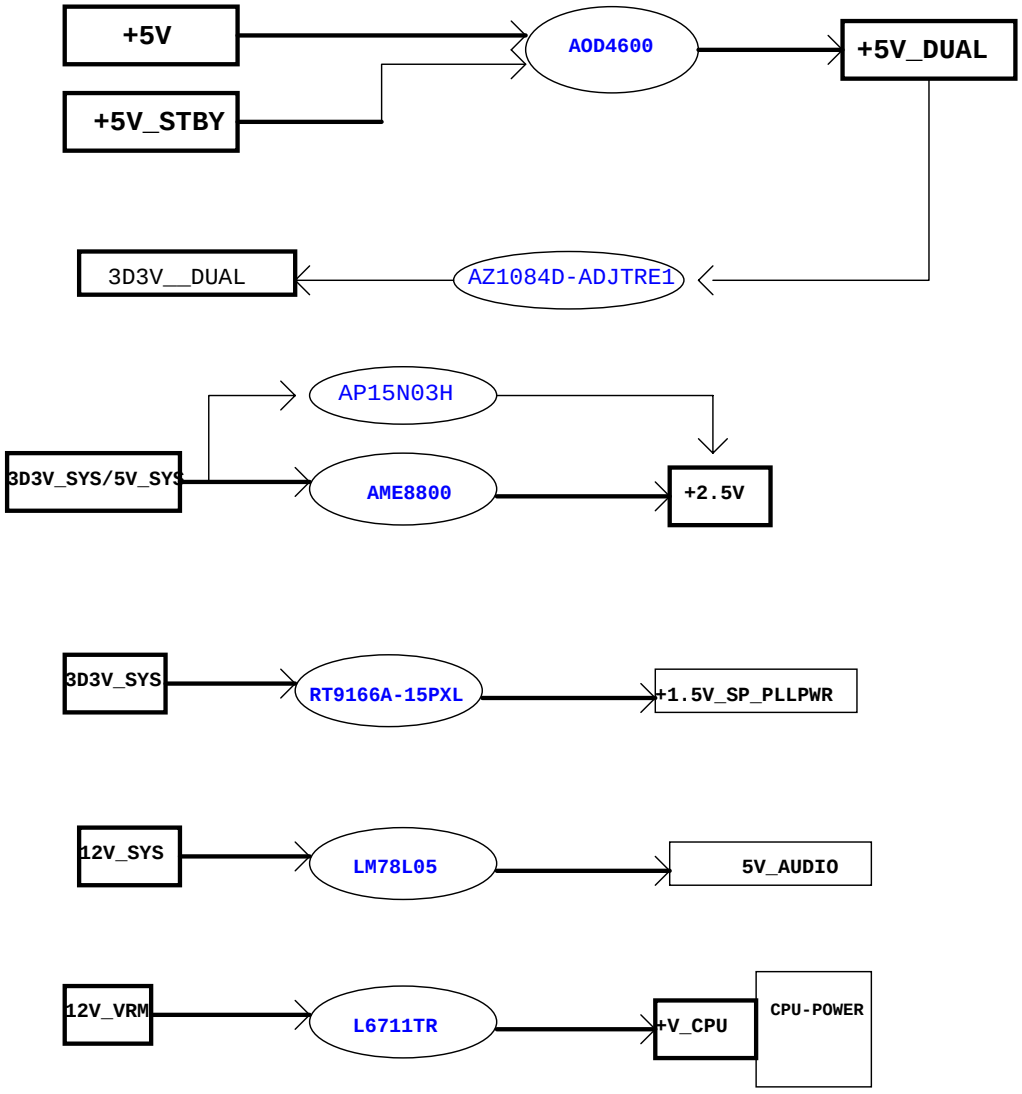


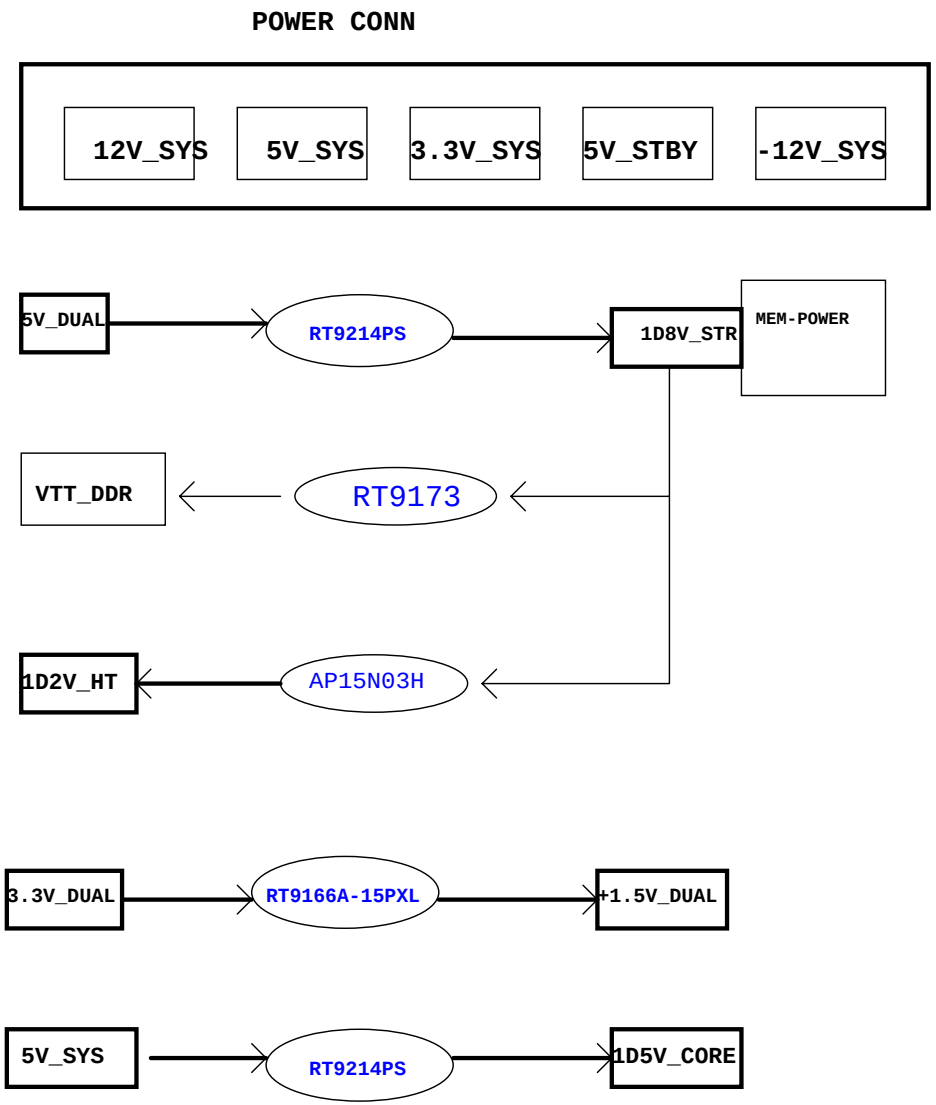


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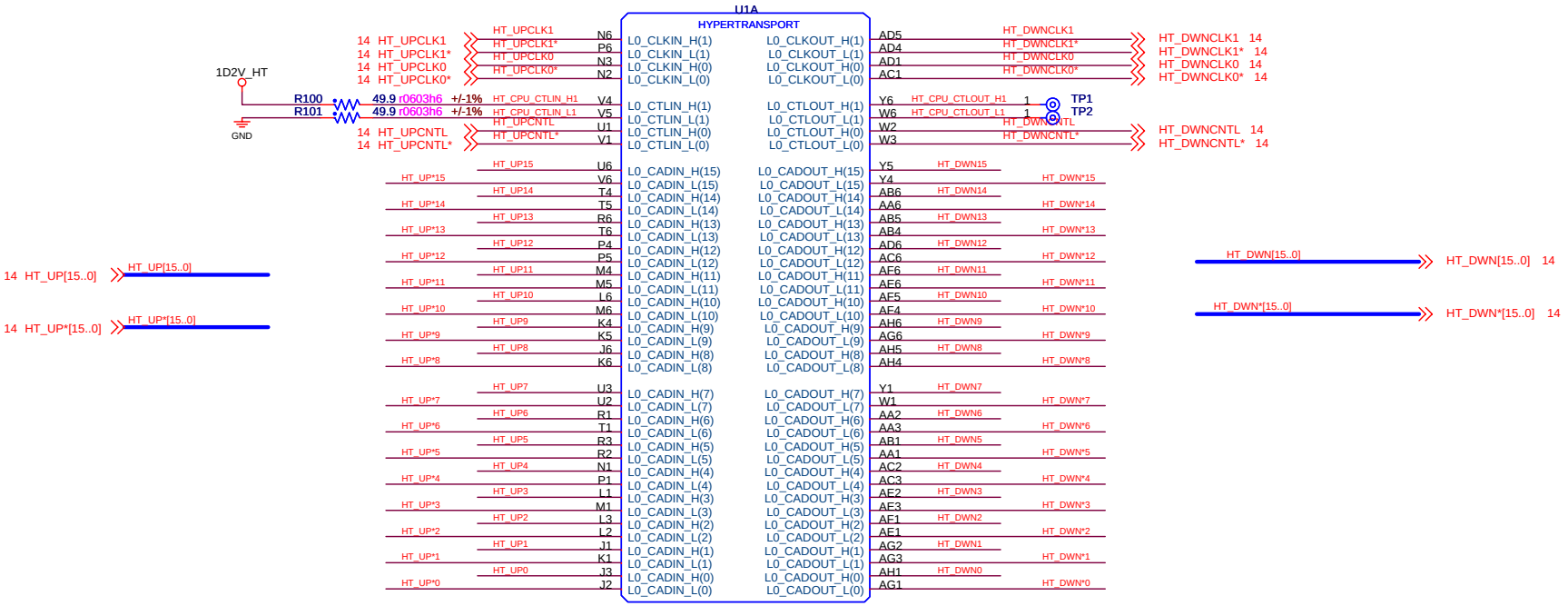


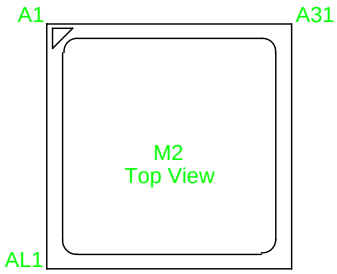


Layout: Add stitching caps if crossing plane split

HyperTransport Net Naming Convention

HT_"link driver"_"link receiver"_"function"_"polarity"_"number"

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| | | |
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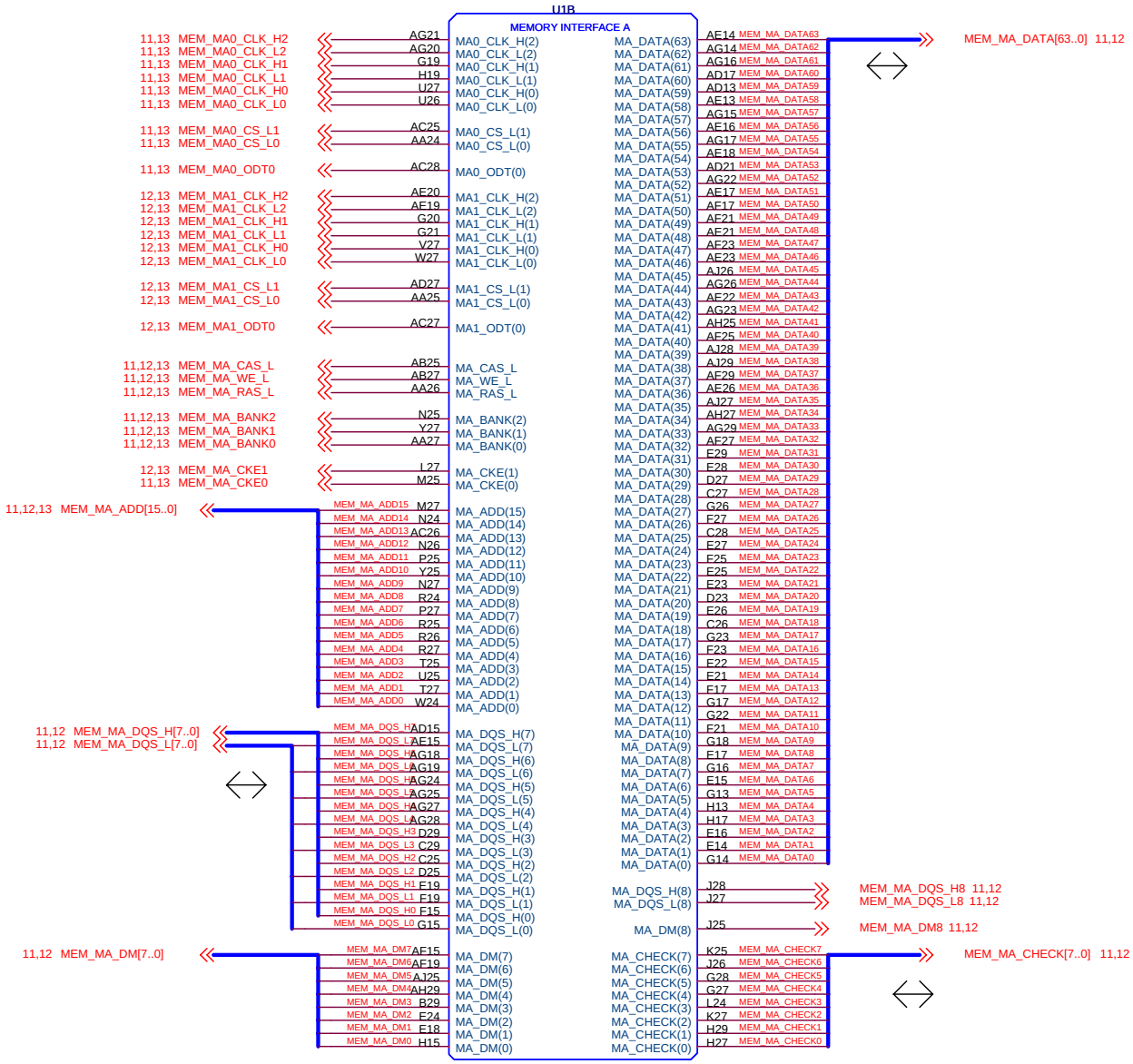


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|---|---|---|
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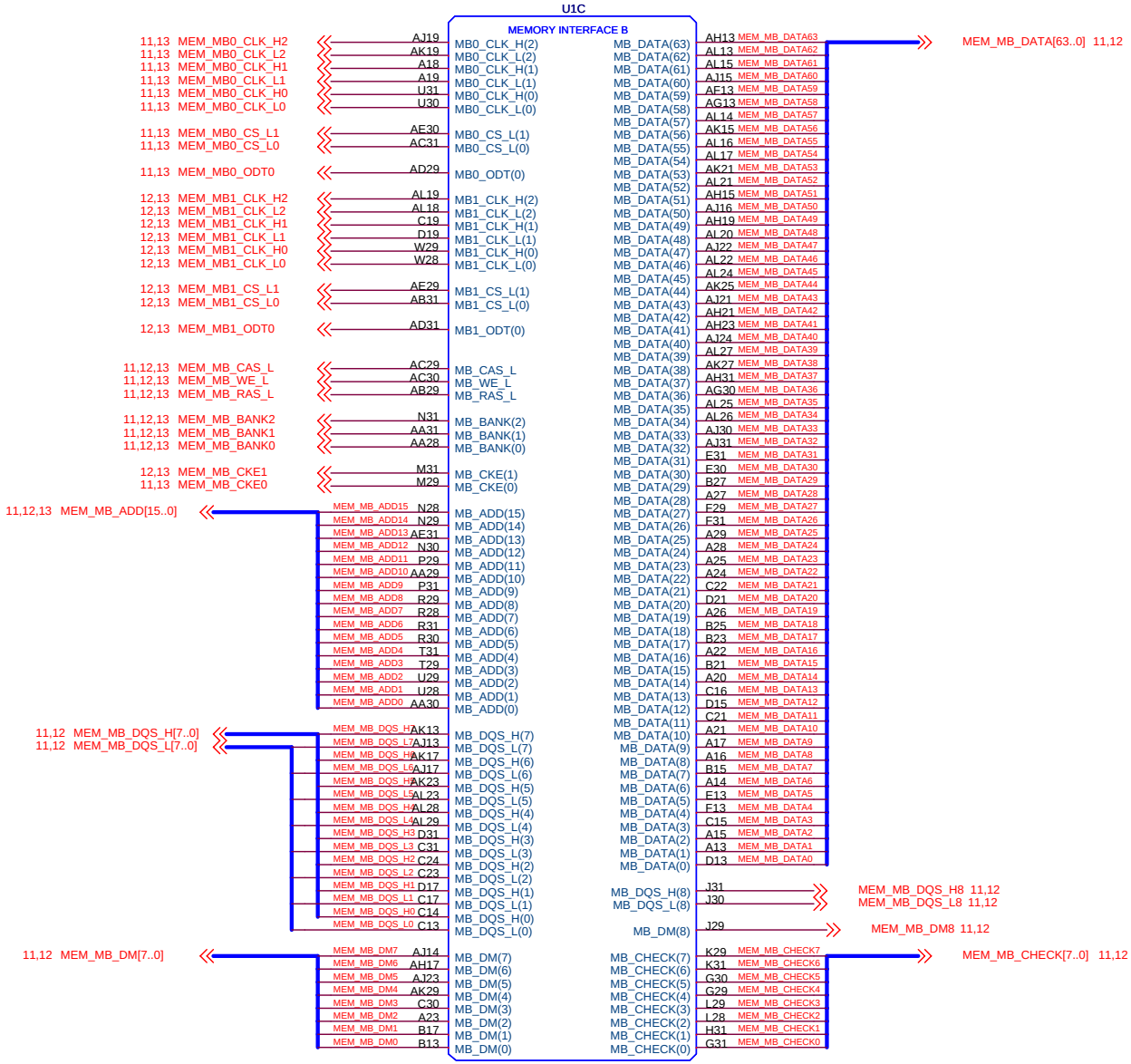


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# CPU Control & Debug Interfaces

VREG_VID4----RN1.6VREG_VID2---RN1.4VREG_VID3---RN1.2

Level translation buffers
Assuming system devices
Do not provide VDDIO
compatible voltage levels

These signals must be
driven low during S3
and S5 states, including
state transitions, to meet
HT I/O Link Specification

Keep trace to resistor
less than 600mils from CPU pin and
trace to AC caps less than 1250mils

Required for compatibility
with future processors

See Note 1

Keep trace to resistors
less than 1.5" from CPU pin

Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin

## Note 1

5-bit VID Implementation:
VID4:0 connects to VID4:0 of regulator*
VID5 should be left unconnected.
VID1 should be pulled up to VDDIO for compatibility with future processors *
Translation may be needed to meet the input requirements of the regulator inputs (See datasheet for processor Voh specs & regulator datasheet for Vih min requirements)

6-bit VID Implementation:
VID5:0 directly connects to VID5:0 of regulator.
VID1 should be pulled up to VDDIO for compatibility with future processors
NOTE: There is an incompatibility between the 5-bit VID code & 6-bit VID code x11111b. VID code 11111b is 悠FF for 5-bit VID controllers & a valid VID code for 6-bit VID controllers (011111b is 775mv & 111111b is 375mv). These are not planned to be operating VID扭 for non-mobile processors so no adverse system implications will occur using a 5-bit VID or 6-bit controller in non-mobile implementations. Please see AMD Socket M2 Motherboard Design Guide, PID #33165 for more details.

Erratum 133, Revision Guide for
AMD NPT 0Fh Processors

Erratum 133, Revision Guide for
AMD NPT 0Fh Processors

# CPU_M_VREF_SUS

Layout: Place near CPU socket

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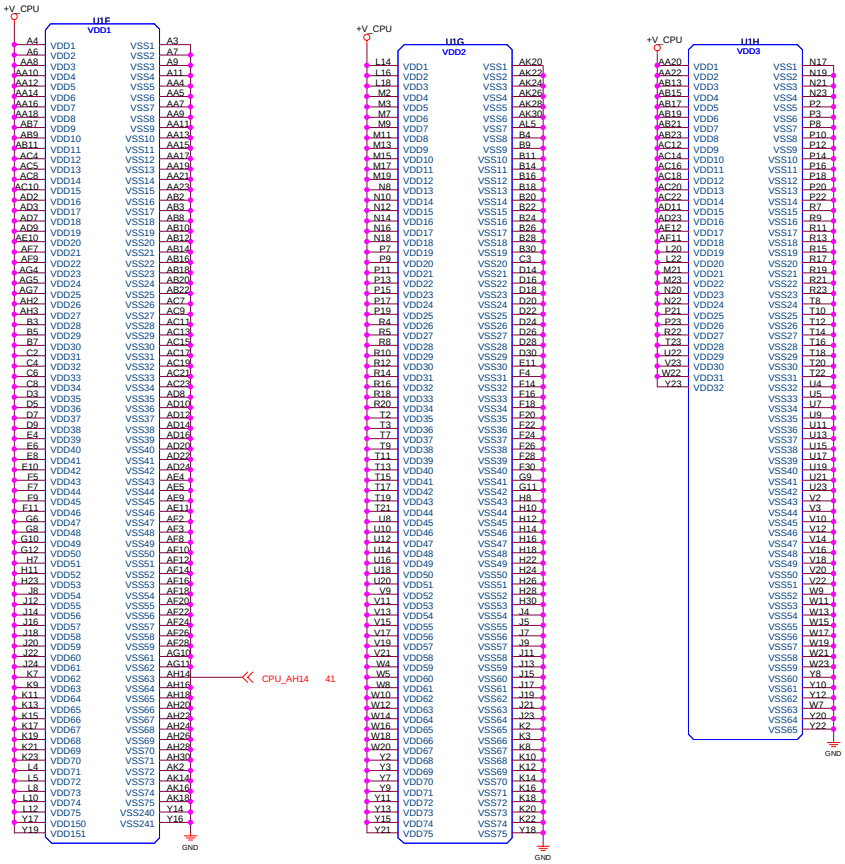
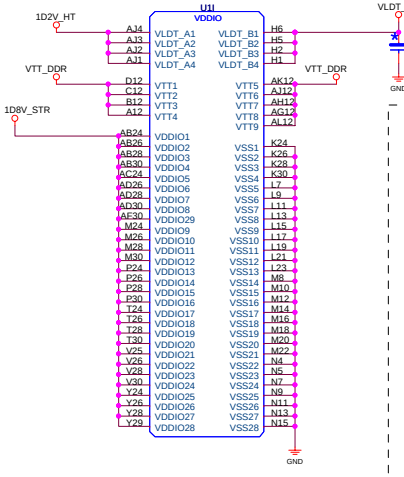
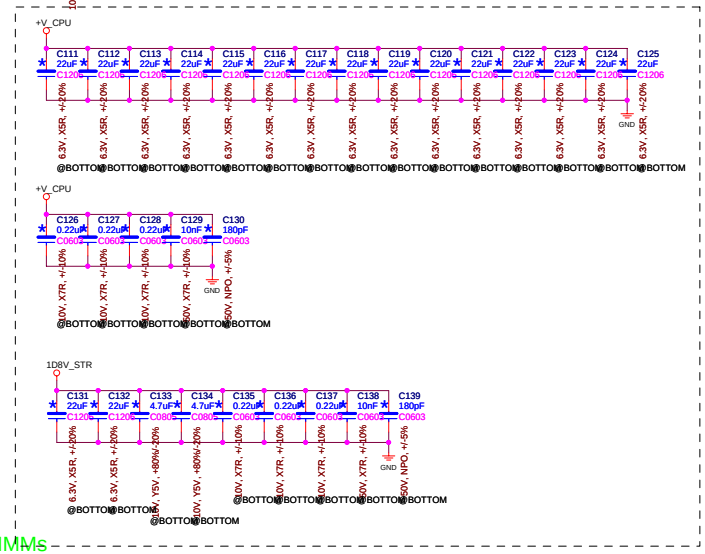
# Processor Power & Ground



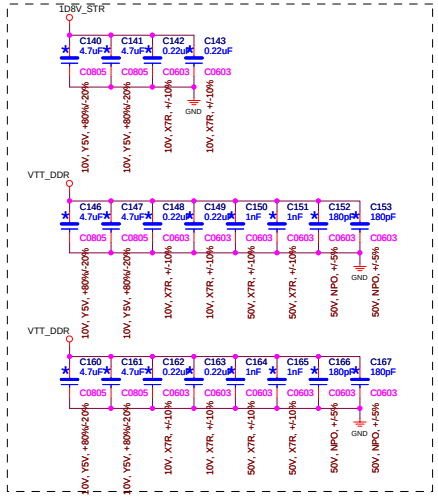

VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



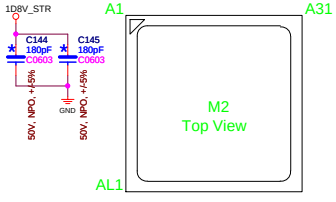

## Bottomside Decoupling



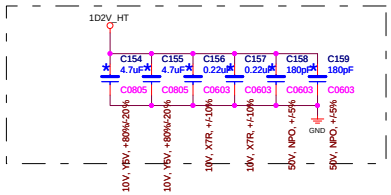

Decoupling Between Processor and DIMMs
Place as close to processor as possible.




Decoupling Between Processor and DIMMs




Place near processor on VLDT pour.

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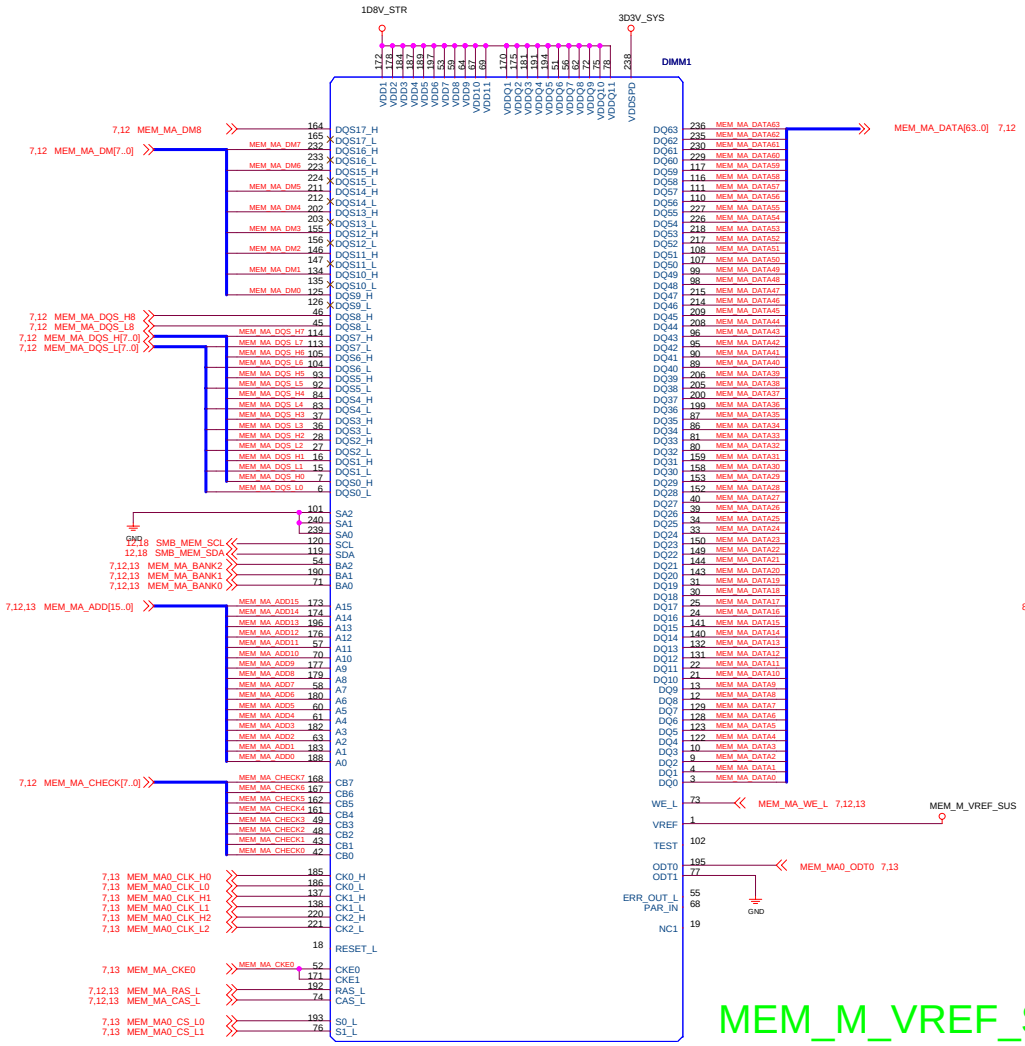
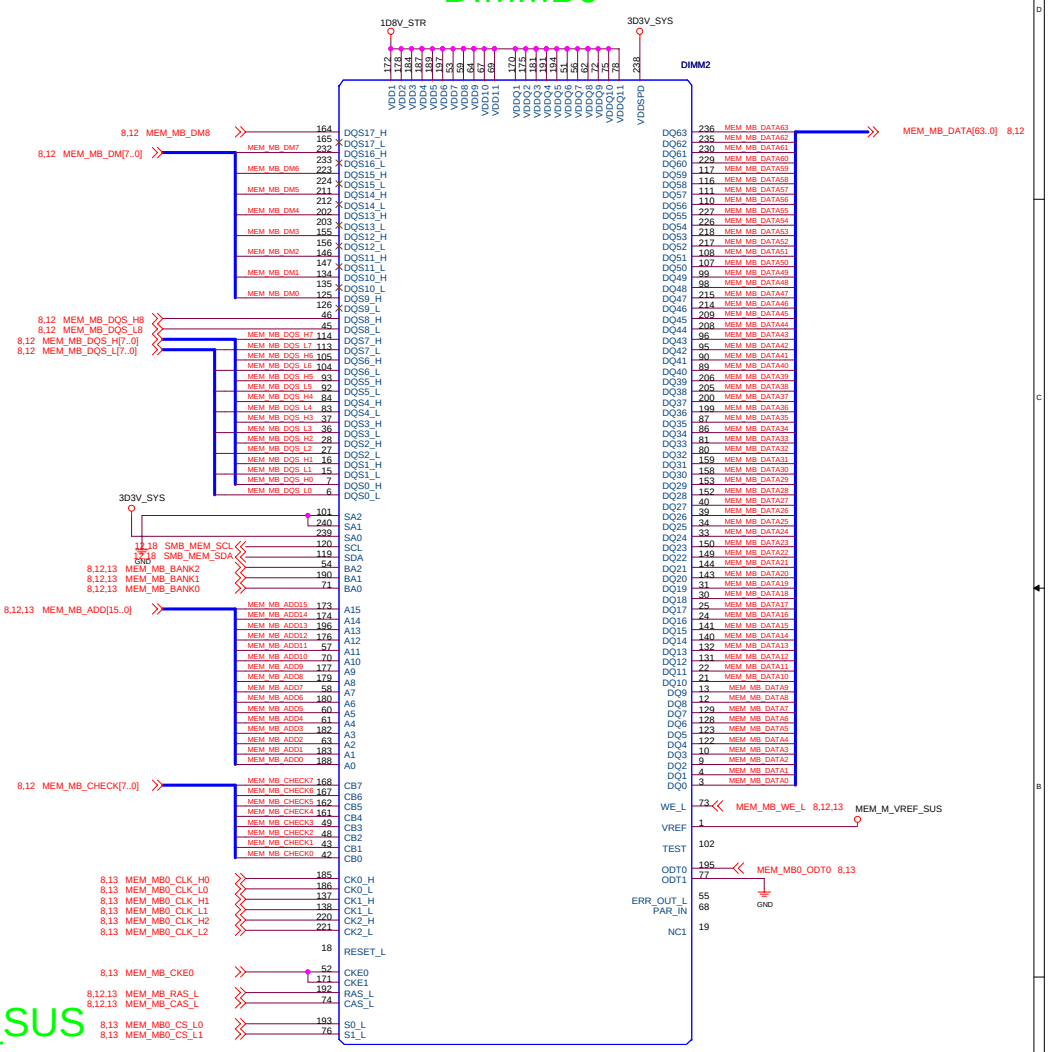
| SMB_MEM BUS ADDRESS | |
|---|---|
| DIMM 0 | 1010 000 |
| DIMM 1 | 1010 001 |
| DIMM 2 | 1010 010 |
| DIMM 3 | 1010 011 |

# First Logical DDR2 DIMM

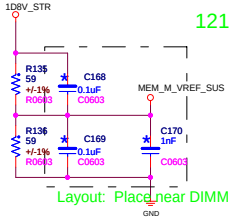
## DIMMA0



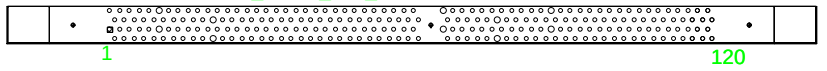

## DIMMB0




## MEM_M_VREF_SUS




Layout: Place near DIMM sockets

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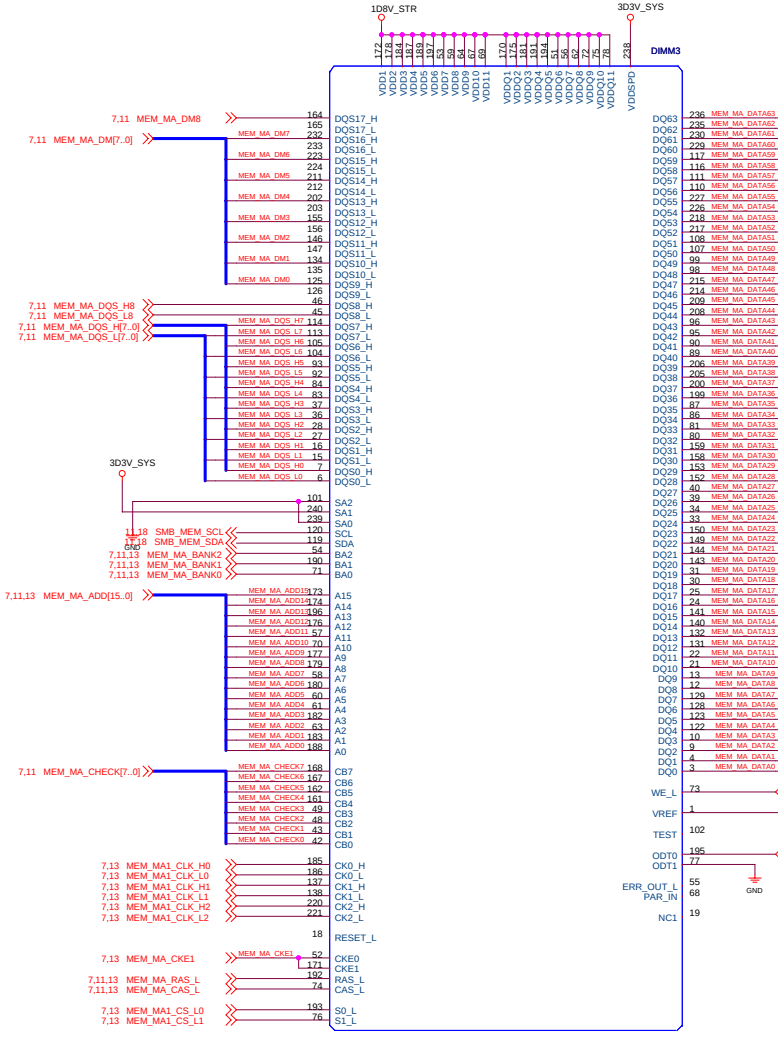
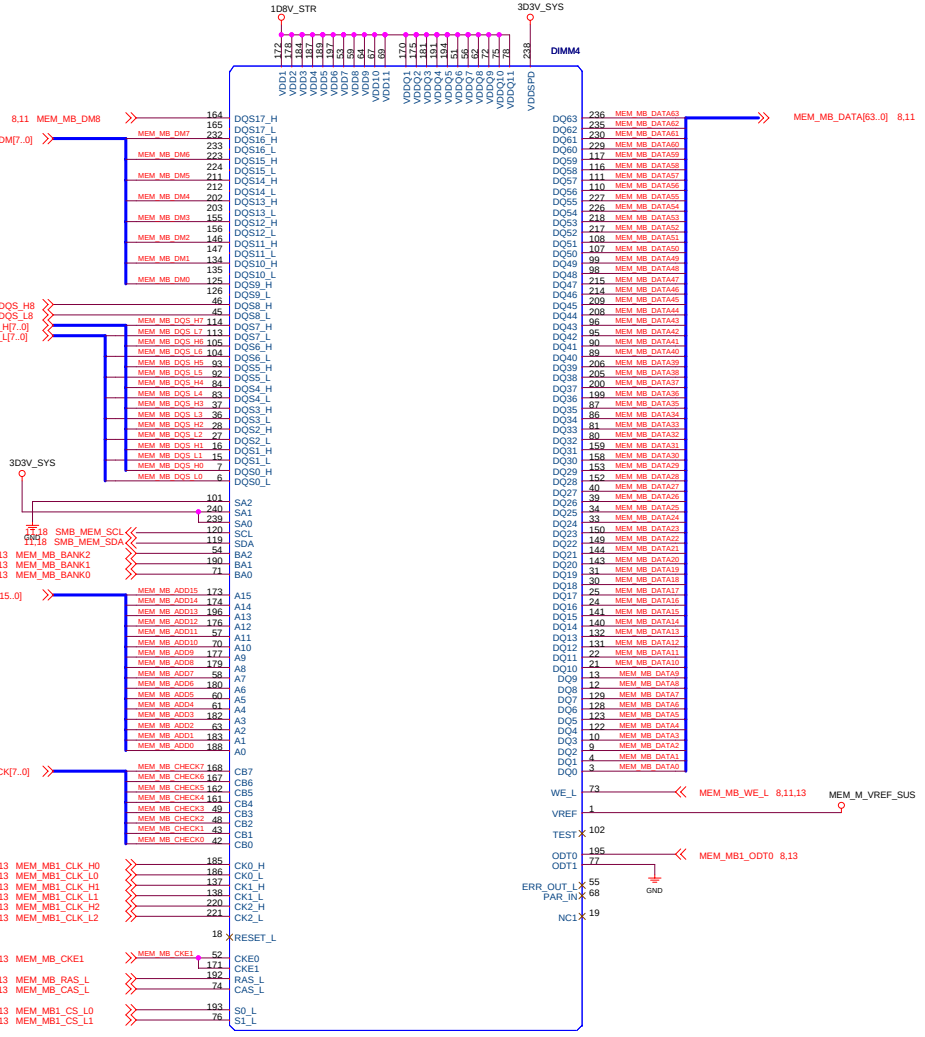
# Second Logical DDR2 DIMM

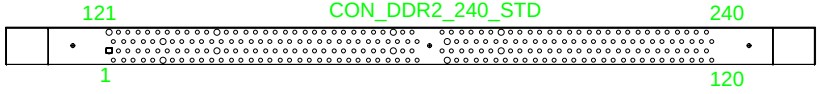
| SMB_MEM BUS ADDRESS | |
|---|---|
| DIMM 0 | 1010 000 |
| DIMM 1 | 1010 001 |
| DIMM 2 | 1010 010 |
| DIMM 3 | 1010 011 |

## DIMMA1




## DIMMB1

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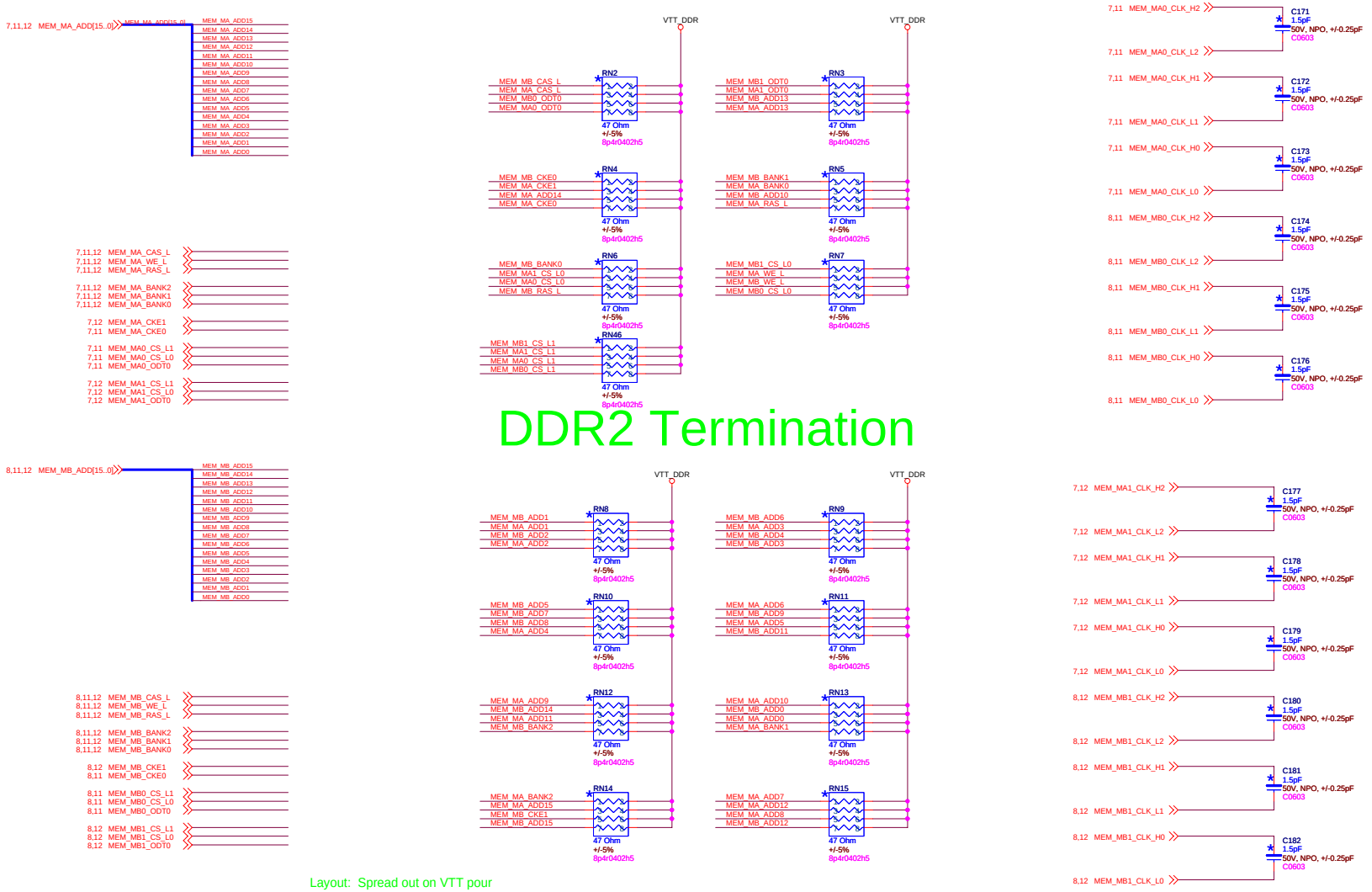
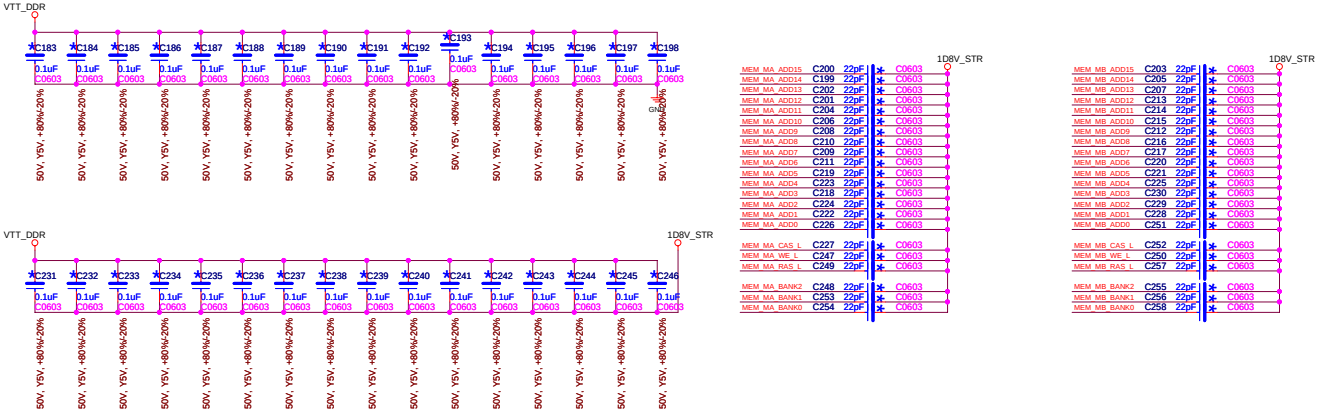
# DDR2 Termination




Layout: Spread out on VTT pour

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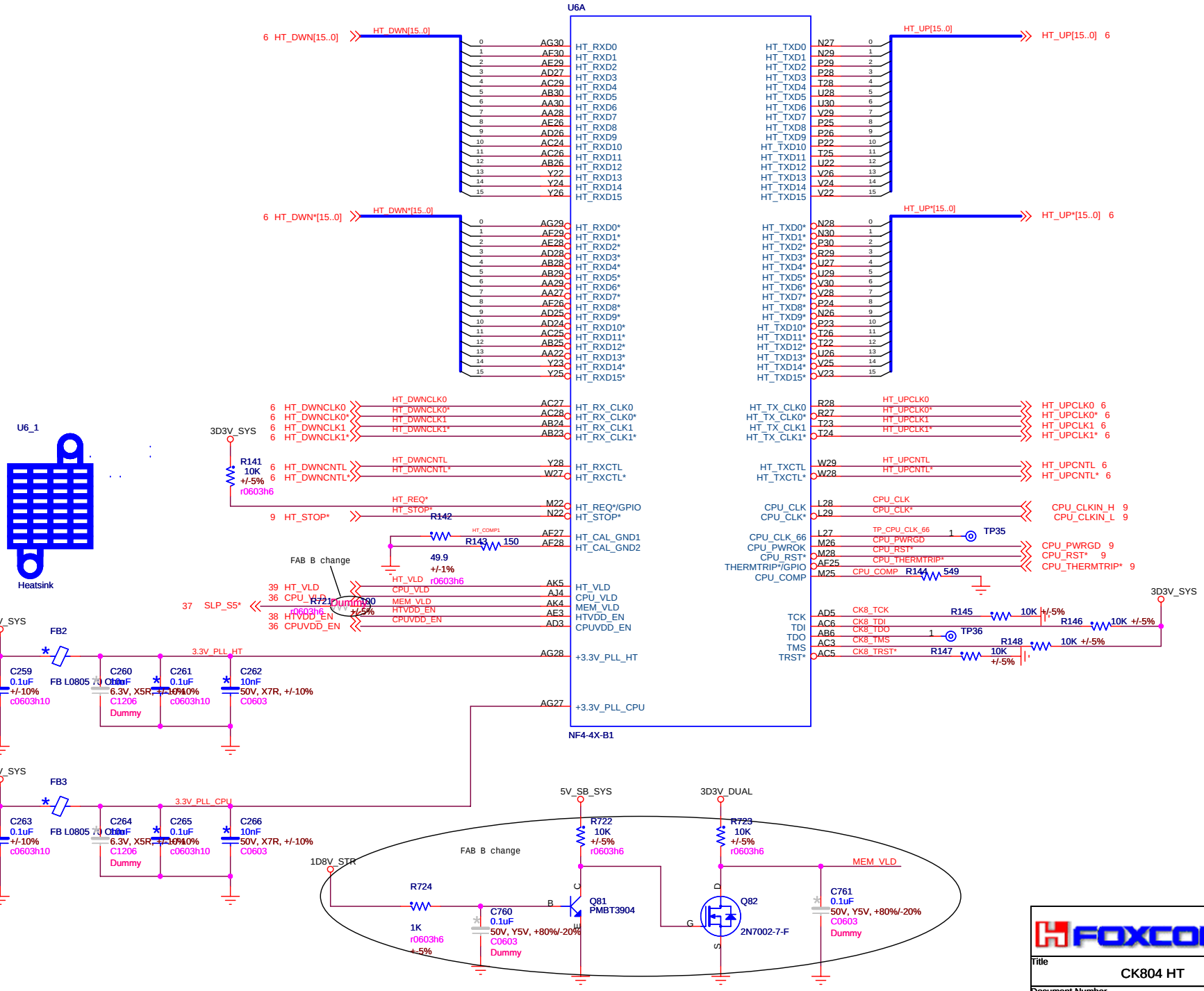


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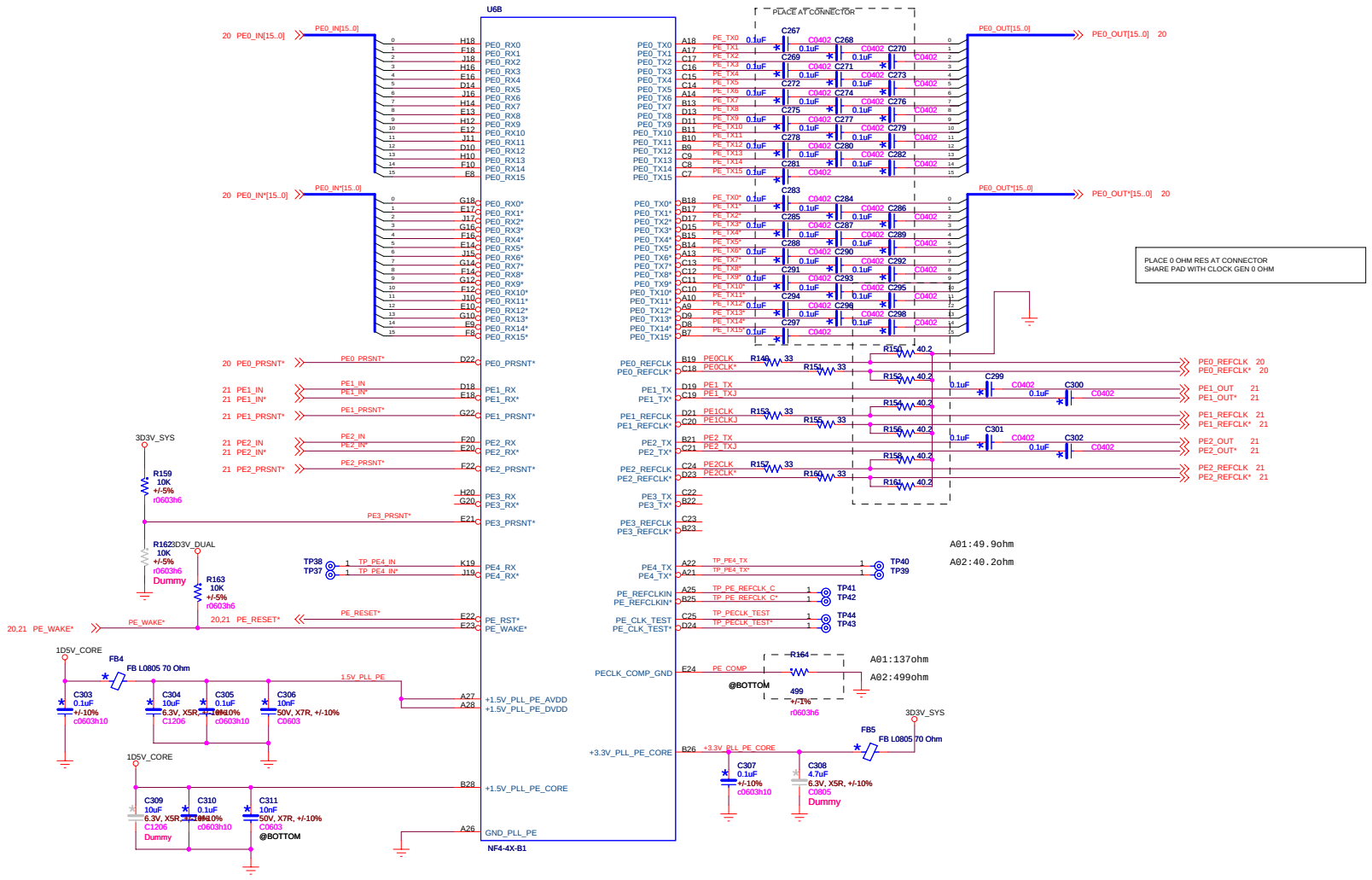
U6B
NF4-4X-B1
PLACE AT CONNECTOR
PE0_IN[15..0]
PE0_IN*[15..0]
PE0_OUT[15..0]
PE0_OUT*[15..0]
PE0_PRSNT*
PE1_IN
PE1_IN*
PE1_PRSNT*
PE2_IN
PE2_IN*
PE2_PRSNT*
PE3_PRSNT*
PE_WAKE*
PE_RESET*
PE0_REFCLK
PE0_REFCLK*
PE1_REFCLK
PE1_REFCLK*
PE2_REFCLK
PE2_REFCLK*
PE1_TX
PE1_TX*
PE2_TX
PE2_TX*
PE3_TX*
PE3_REFCLK*
PE4_TX
PE4_TX*
PE_REFCLKIN
PE_REFCLKIN*
PE_CLK_TEST
PE_CLK_TEST*
PECLK_COMP_GND
+3.3V_PLL_PE_CORE
+1.5V_PLL_PE_AVDD
+1.5V_PLL_PE_DVDD
+1.5V_PLL_PE_CORE
GND_PLL_PE
PLACE 0 OHM RES AT CONNECTOR
SHARE PAD WITH CLOCK GEN 0 OHM
A01:49.9ohm
A02:40.2ohm
A01:137ohm
A02:499ohm
3D3V_SYS
3D3V_DUAL
1D5V_CORE
1.5V_PLL_PE
FB4
FB5
FB L0805 70 Ohm
R159 10K +/-5% r0603h6
R162 10K +/-5% r0603h6 Dummy
R163 10K +/-5% r0603h6
R164 499 +/-1% r0603h6 @BOTTOM
C303 0.1uF +/-10% c0603h10
C304 10uF 6.3V, X5R, +/-10% C1206
C305 0.1uF +/-10% c0603h10
C306 10nF 50V, X7R, +/-10% C0603
C307 0.1uF +/-10% c0603h10
C308 4.7uF 6.3V, X5R, +/-10% C0805 Dummy
C309 10uF 6.3V, X5R, +/-10% C1206 Dummy
C310 0.1uF +/-10% c0603h10
C311 10nF 50V, X7R, +/-10% C0603 @BOTTOM
TP38 TP37 TP40 TP39 TP41 TP42 TP44 TP43
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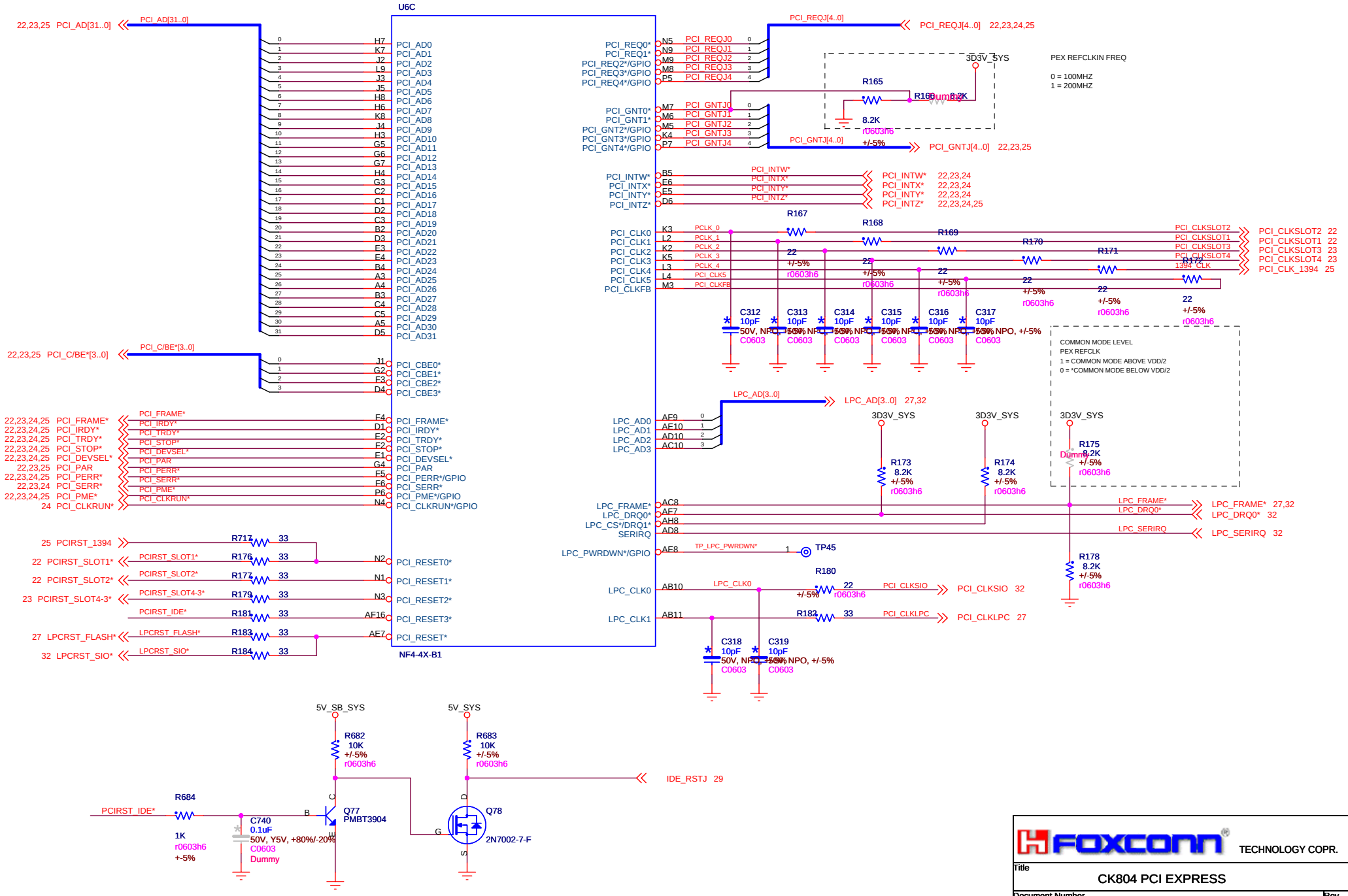
U6C
NF4-4X-B1
PCI_AD[31..0]
PCI_C/BE*[3..0]
PCI_REQJ[4..0]
PCI_GNTJ[4..0]
LPC_AD[3..0]
PEX REFCLKIN FREQ
0 = 100MHZ
1 = 200MHZ
COMMON MODE LEVEL
PEX REFCLK
1 = COMMON MODE ABOVE VDD/2
0 = *COMMON MODE BELOW VDD/2
3D3V_SYS
5V_SB_SYS
5V_SYS
R165
R166 Dummy 8.2K
R167
R168
R169
R170
R171
R172
R173 8.2K +/-5% r0603h6
R174 8.2K +/-5% r0603h6
R175 Dummy 8.2K +/-5% r0603h6
R176 33
R177 33
R178 8.2K +/-5% r0603h6
R179 33
R180 22 +/-5% r0603h6
R181 33
R182 33
R183 33
R184 33
R682 10K +/-5% r0603h6
R683 10K +/-5% r0603h6
R684 1K r0603h6 +-5%
C312 10pF 50V, NPO, +/-5% C0603
C313 10pF 50V, NPO, +/-5% C0603
C314 10pF 50V, NPO, +/-5% C0603
C315 10pF 50V, NPO, +/-5% C0603
C316 10pF 50V, NPO, +/-5% C0603
C317 10pF 50V, NPO, +/-5% C0603
C318 10pF 50V, NPO, +/-5% C0603
C319 10pF 50V, NPO, +/-5% C0603
C740 0.1uF 50V, Y5V, +80%/-20% C0603 Dummy
Q77 PMBT3904
Q78 2N7002-7-F
TP45
IDE_RSTJ 29
PCI_CLKSIO 32
PCI_CLKLPC 27
PCI_CLK_1394 25
LPC_FRAME* 27,32
LPC_DRQ0* 32
LPC_SERIRQ 32
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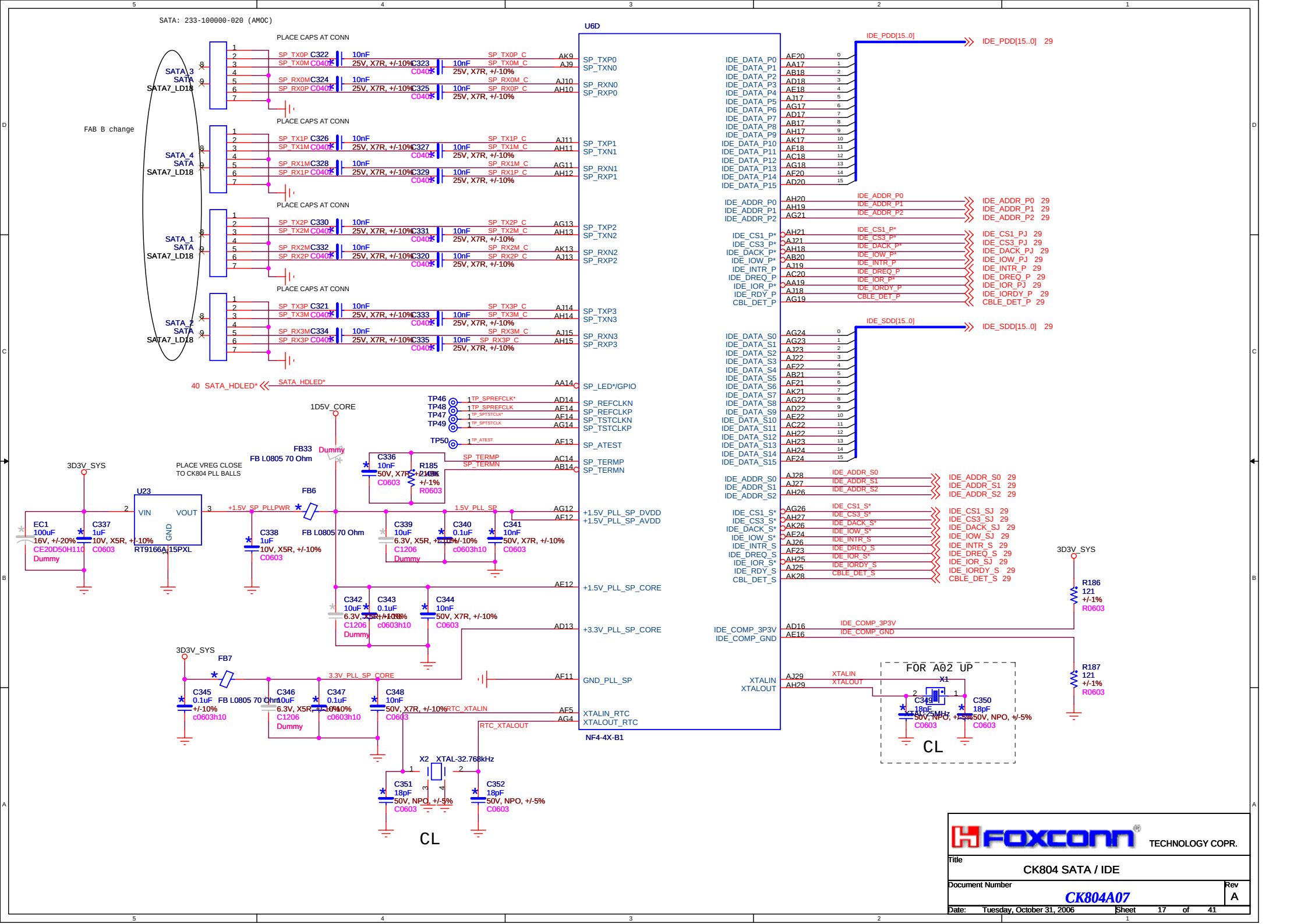


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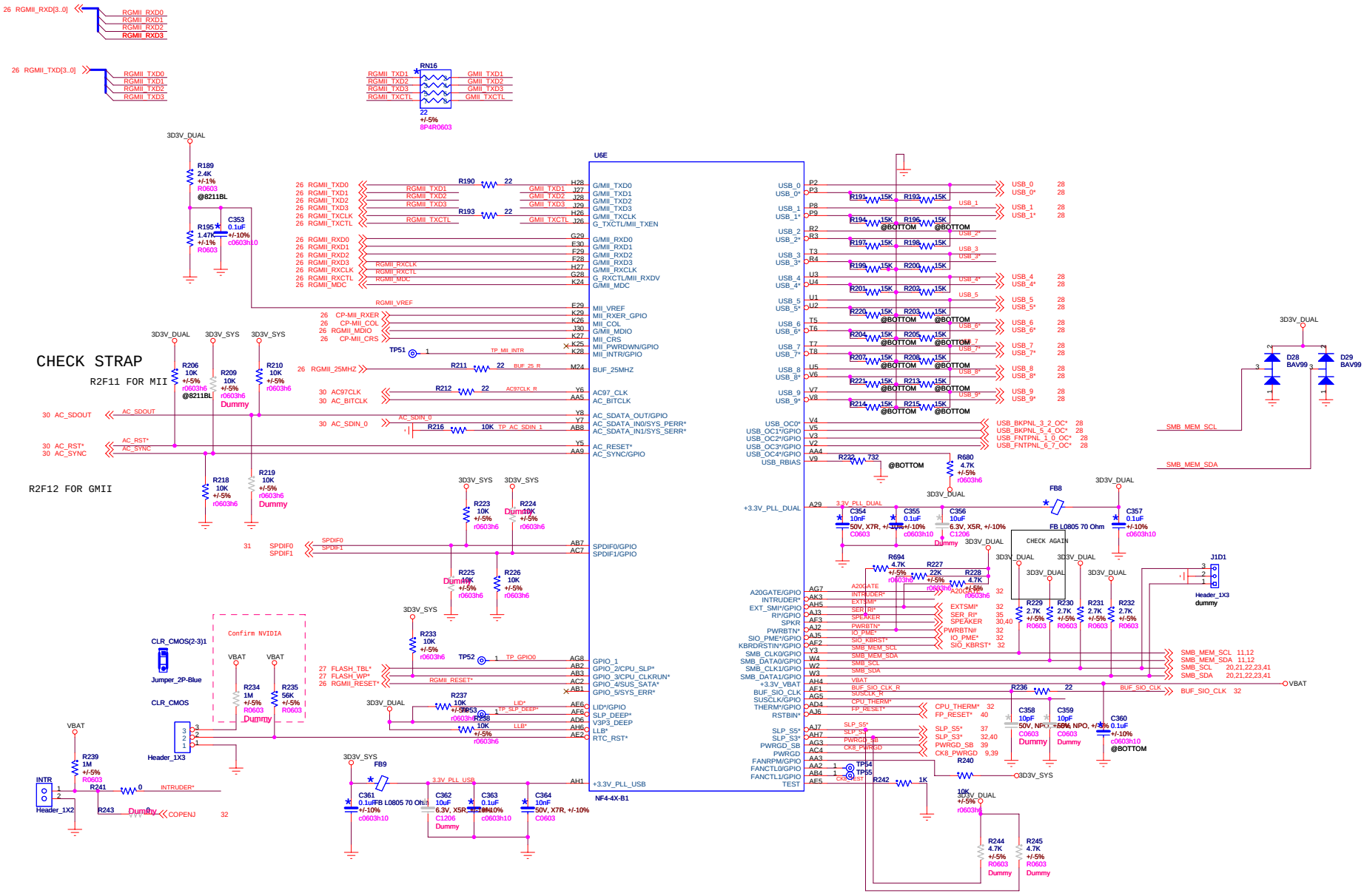


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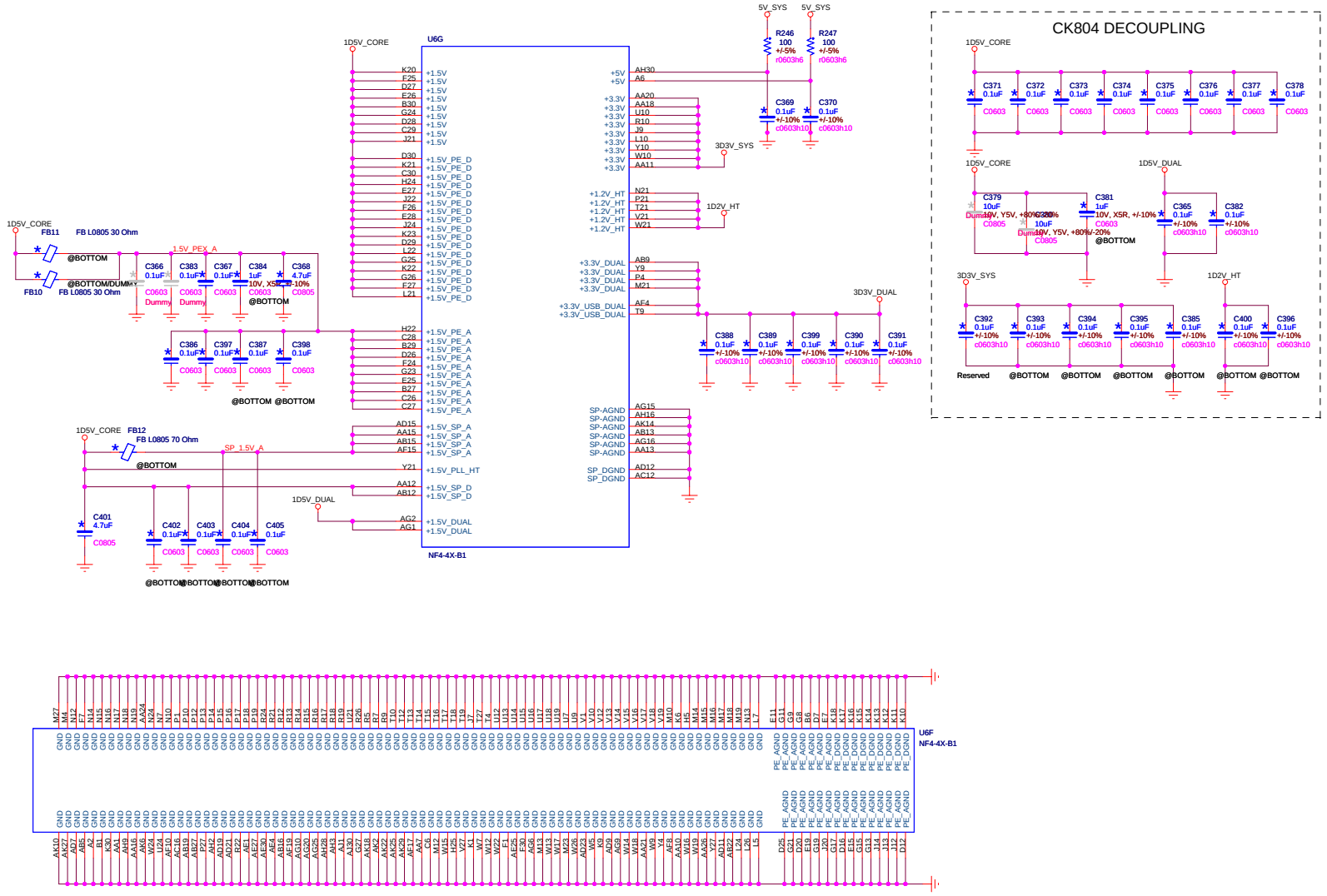


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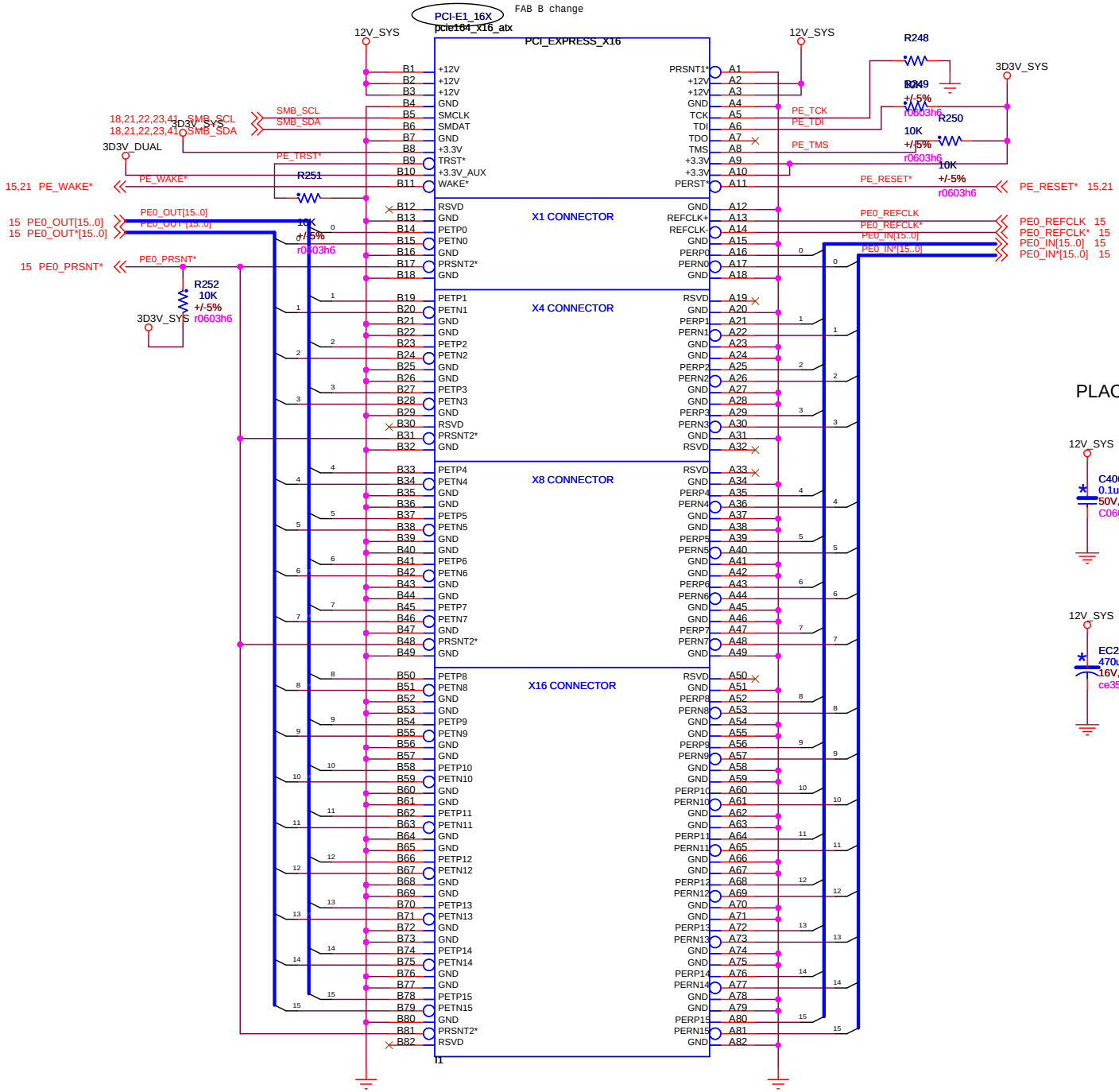
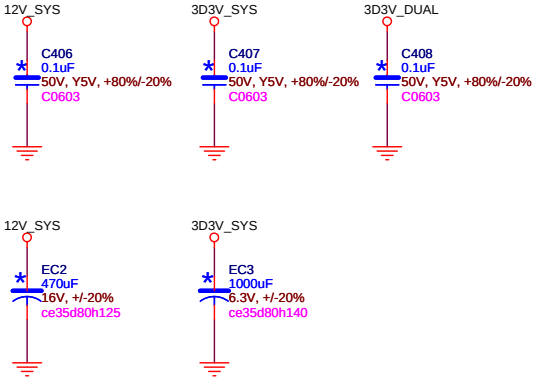



## PLACE CAPS NEAR PEX CONNECTORS

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| Title | PCI EXPRESS X16 CONNECTOR | |
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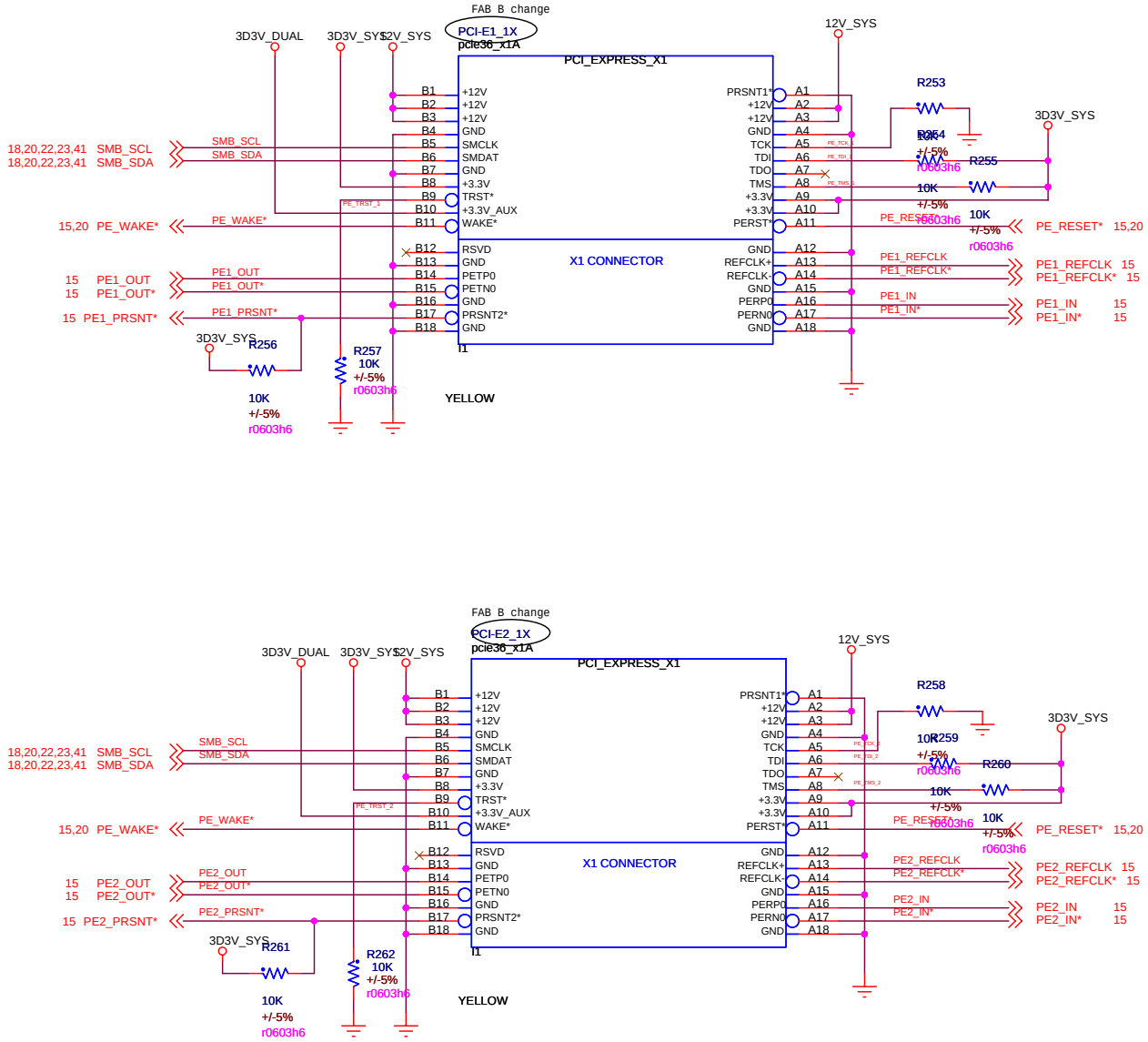
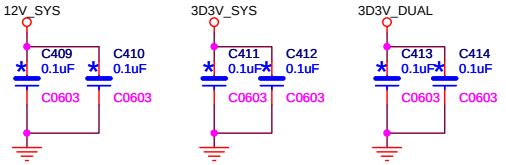
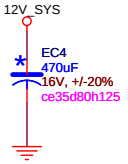
| Date: Tuesday, October 31, 2006 | Sheet 20 of 41 | |










FOXCONN TECHNOLOGY COPR.

Title: PCI EXPRESS X1 CONNECTOR

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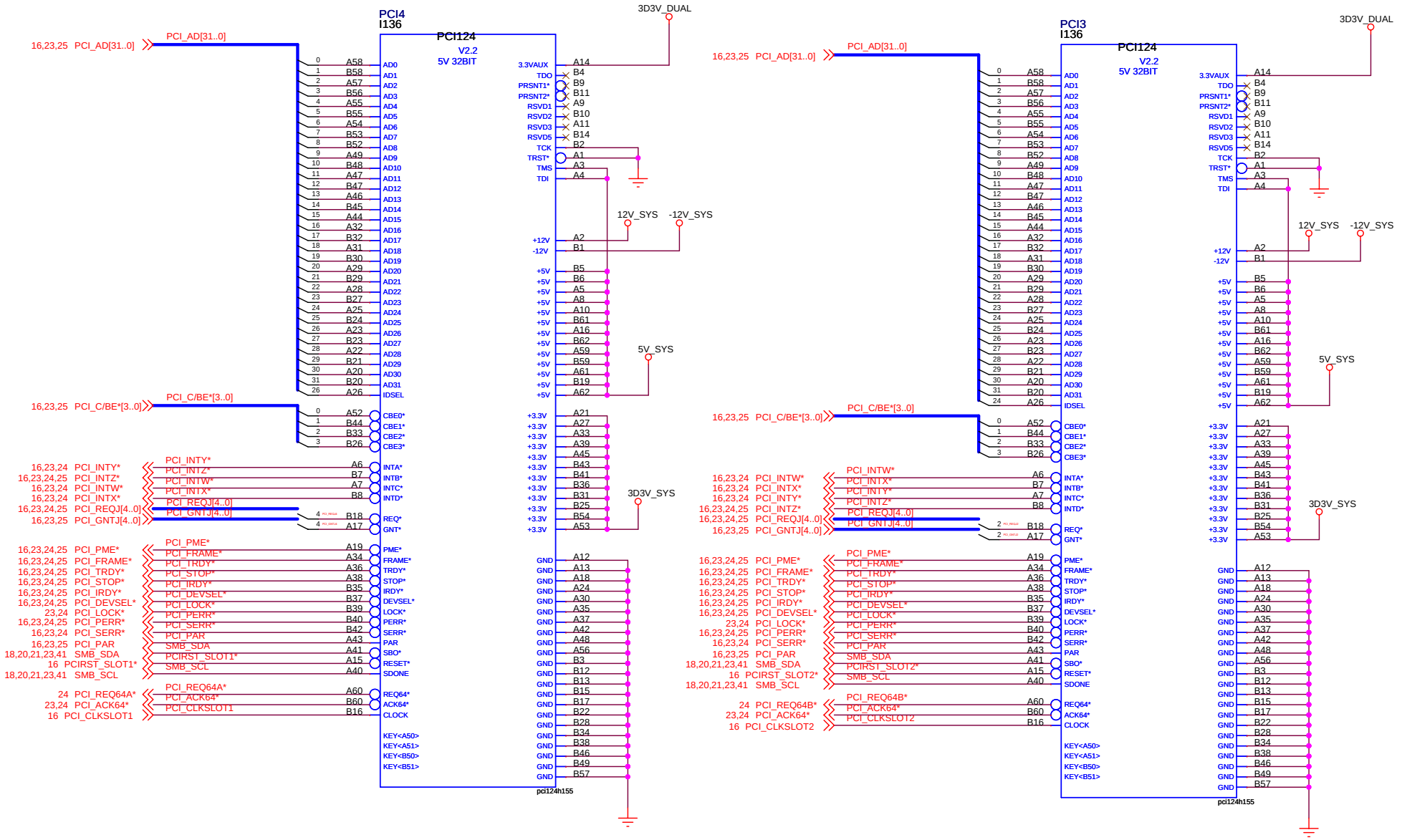
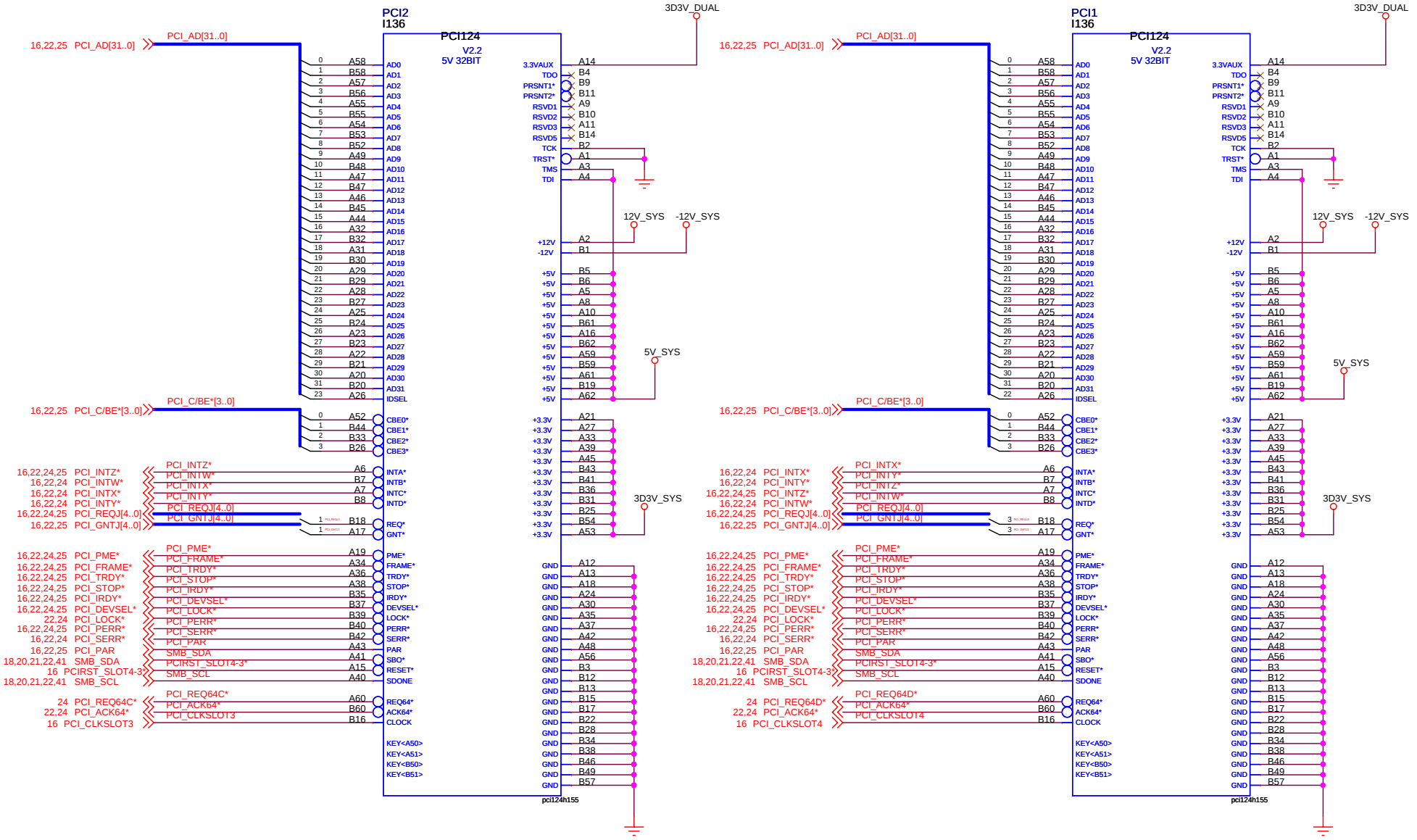
SLOT 1 (FURTHEST FROM CPU)

SLOT 2

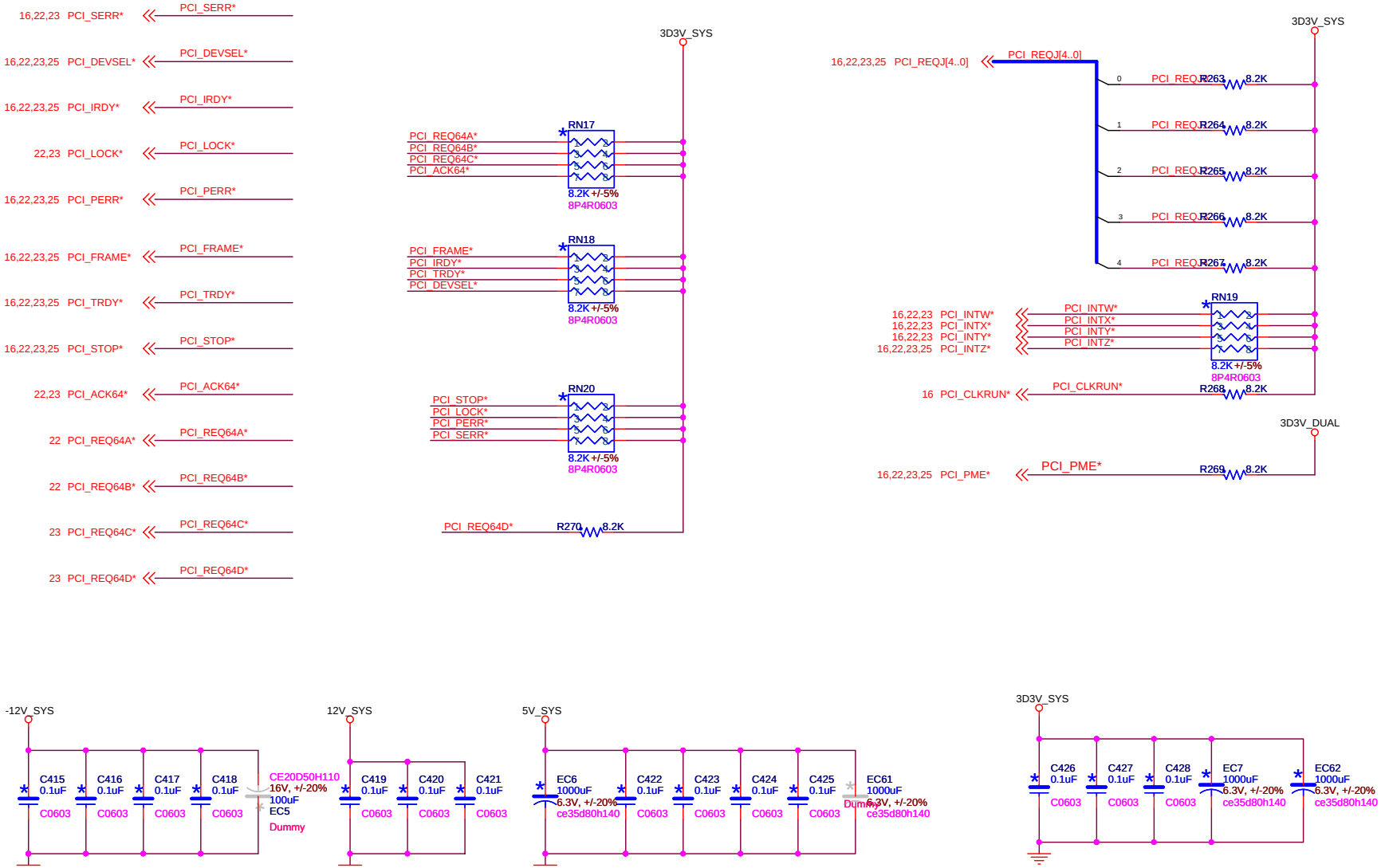



| | |
|---|---|
| FOXCONN TECHNOLOGY COPR. | |
| Title | PCI CONNECTOR 1-2 |
| Document Number | CK804A07 |
| Rev | A |
| Date: Tuesday, October 31, 2006 | Sheet 22 of 41 |




FOXCONN TECHNOLOGY COPR.

| | |
|---|---|
| Title | PCI CONNECTOR 3-4 |
| Document Number | CK804A07 |
| Rev | A |
| Date: Tuesday, October 31, 2006 | Sheet 23 of 41 |




FOXCONN TECHNOLOGY COPR.

Title: PCI TERMINATION

Document Number: CK804A07

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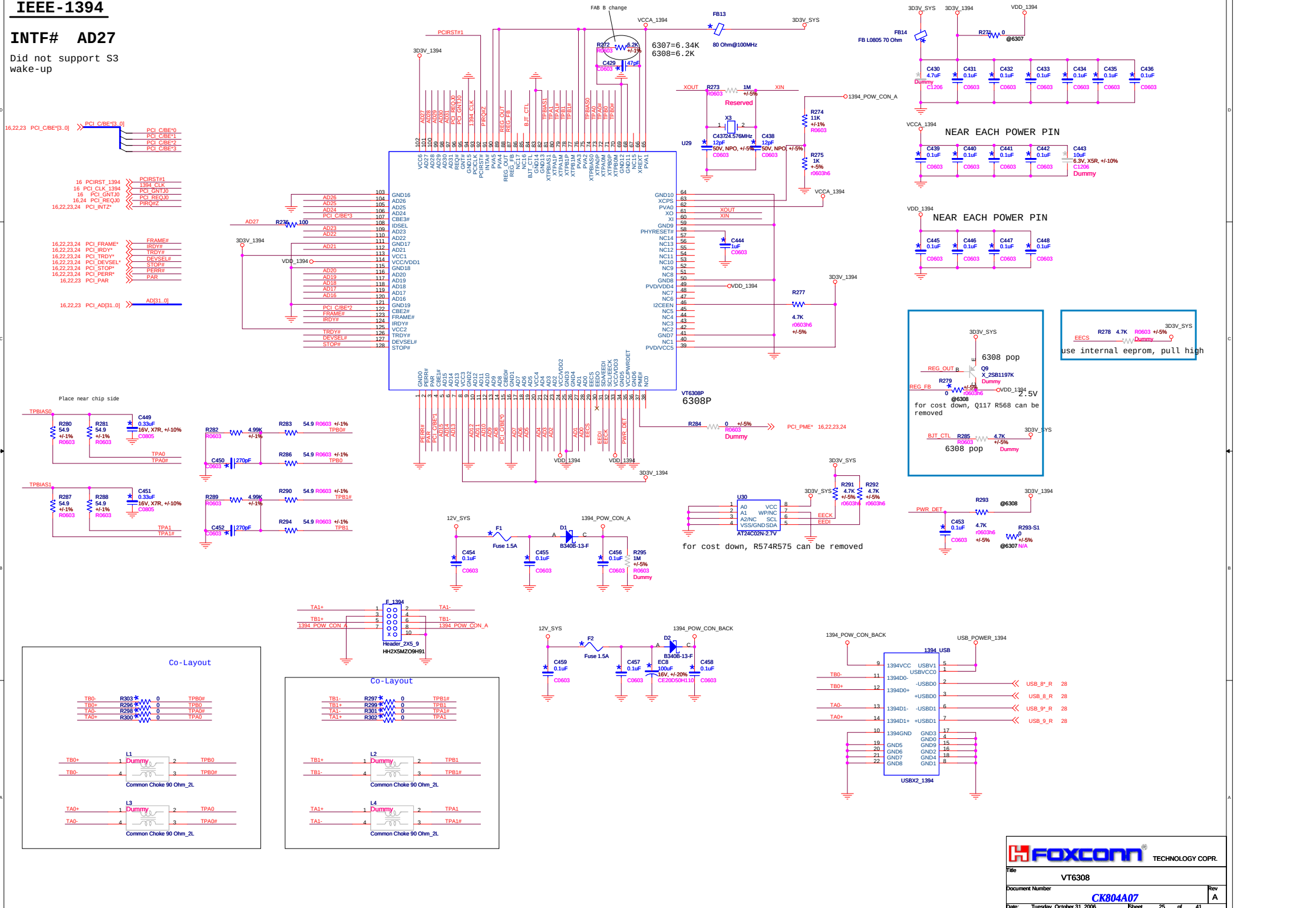
# IEEE-1394

## INTF# AD27

Did not support S3 wake-up




| | |
|---|---|
| Title | VT6308 |
| Document Number | CK804A07 |
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| Date: | Tuesday, October 31, 2006 |
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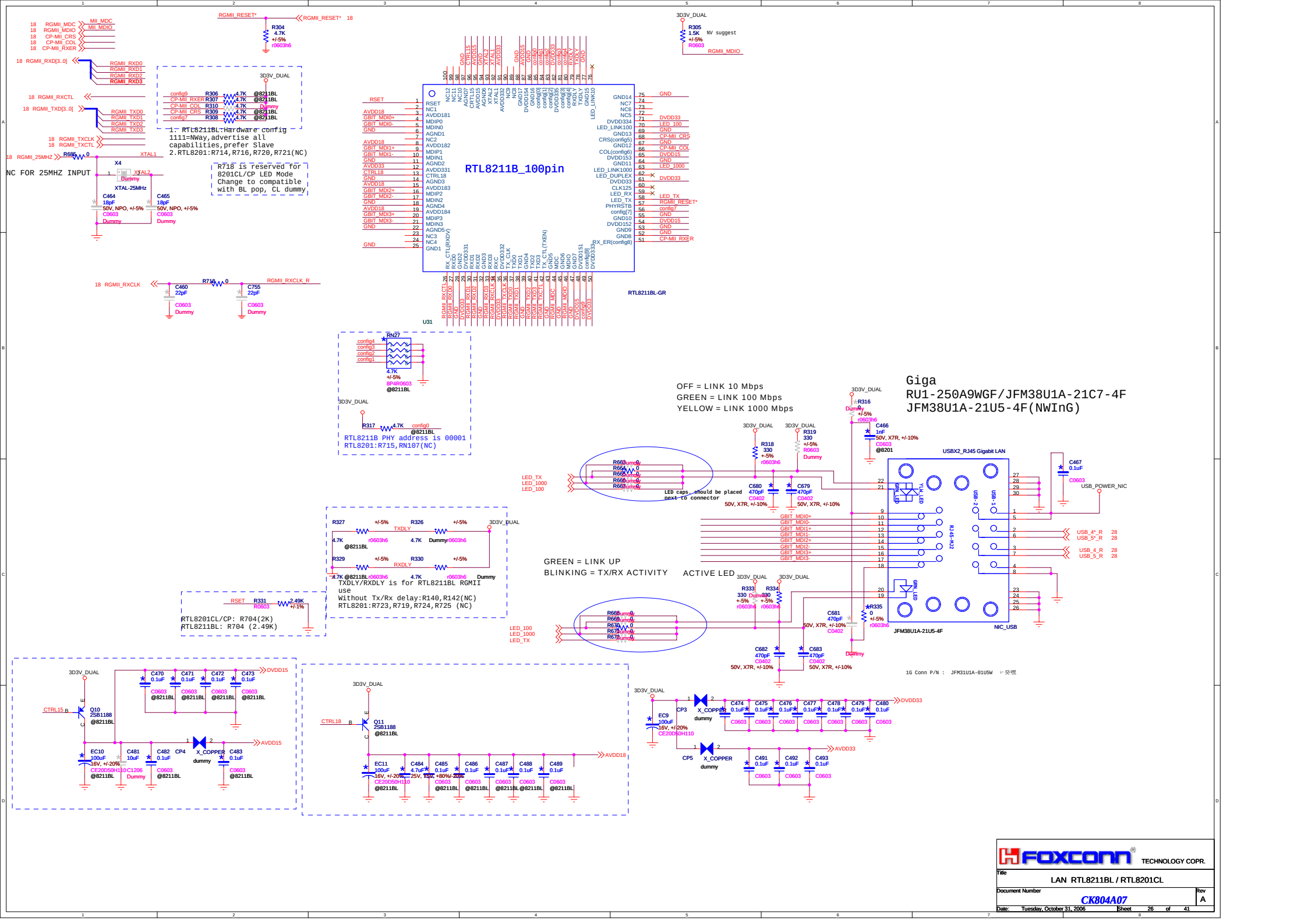
RTL8211B_100pin
RTL8211BL-GR
U31
1. RTL8211BL Hardware config
1111=NWay,advertise all
capabilities,prefer Slave
2.RTL8201:R714,R716,R720,R721(NC)
R718 is reserved for
8201CL/CP LED Mode
Change to compatible
with BL pop, CL dummy
NC FOR 25MHZ INPUT
XTAL-25MHz
RTL8211B PHY address is 00001
RTL8201:R715,RN107(NC)
TXDLY/RXDLY is for RTL8211BL RGMII
use
Without Tx/Rx delay:R140,R142(NC)
RTL8201:R723,R719,R724,R725 (NC)
RTL8201CL/CP: R704(2K)
RTL8211BL: R704 (2.49K)
OFF = LINK 10 Mbps
GREEN = LINK 100 Mbps
YELLOW = LINK 1000 Mbps
GREEN = LINK UP
BLINKING = TX/RX ACTIVITY
ACTIVE LED
LED caps should be placed
next to connector
USBX2_RJ45 Gigabit LAN
JFM38U1A-21U5-4F
NIC_USB
1G Conn P/N : JFM31U1A-01U5W
Giga
RU1-250A9WGF/JFM38U1A-21C7-4F
JFM38U1A-21U5-4F(NWInG)
FOXCONN TECHNOLOGY COPR.
LAN RTL8211BL / RTL8201CL
CK804A07
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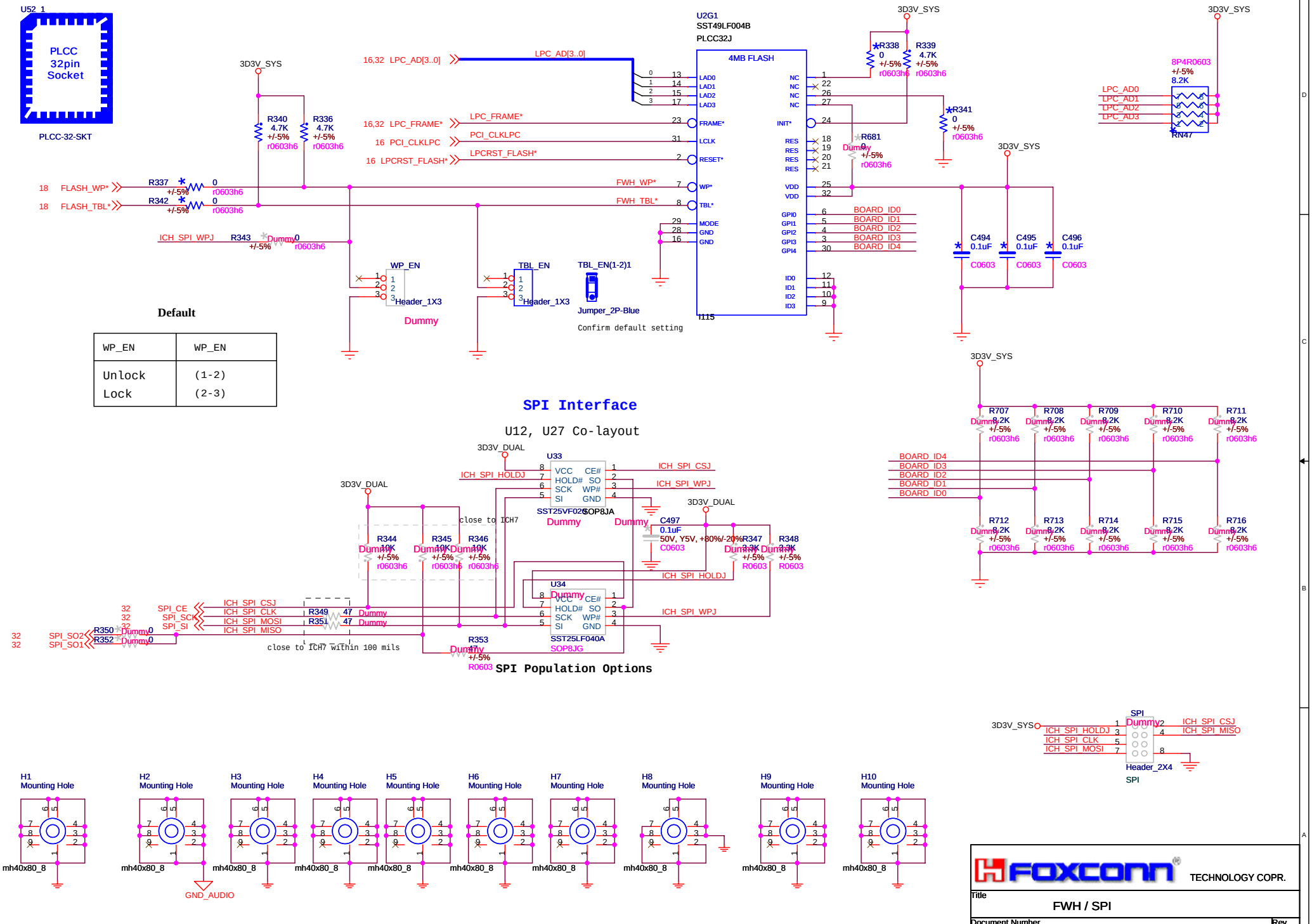
U52_1
PLCC 32pin Socket
PLCC-32-SKT
U2G1
SST49LF004B
PLCC32J
4MB FLASH
3D3V_SYS
16,32 LPC_AD[3..0]
LPC_AD[3..0]
16,32 LPC_FRAME*
LPC_FRAME*
16 PCI_CLKLPC
PCI_CLKLPC
16 LPCRST_FLASH*
LPCRST_FLASH*
LAD0
LAD1
LAD2
LAD3
FRAME*
LCLK
RESET*
WP*
TBL*
MODE
GND
INIT*
RES
VDD
GPI0
GPI1
GPI2
GPI3
GPI4
ID0
ID1
ID2
ID3
NC
R338 0 +/-5% r0603h6
R339 4.7K +/-5% r0603h6
R340 4.7K +/-5% r0603h6
R336 4.7K +/-5% r0603h6
R341 0 +/-5% r0603h6
R681 Dummy 0 +/-5% r0603h6
8P4R0603 +/-5% 8.2K
RN47
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
18 FLASH_WP*
18 FLASH_TBL*
R337 0 +/-5% r0603h6
R342 0 +/-5% r0603h6
FWH_WP*
FWH_TBL*
ICH_SPI_WPJ
R343 Dummy 0 +/-5% r0603h6
WP_EN
TBL_EN
Header_1X3
Dummy
TBL_EN(1-2)1
Jumper_2P-Blue
Confirm default setting
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
C494 0.1uF C0603
C495 0.1uF C0603
C496 0.1uF C0603
Default
WP_EN | WP_EN
Unlock | (1-2)
Lock | (2-3)
SPI Interface
U12, U27 Co-layout
3D3V_DUAL
U33
SST25VF020 SOP8JA
ICH_SPI_HOLDJ
ICH_SPI_CSJ
ICH_SPI_WPJ
ICH_SPI_HOLDJ
ICH_SPI_CLK
ICH_SPI_MOSI
ICH_SPI_MISO
SPI_CE
SPI_SCK
SPI_SI
SPI_SO2
SPI_SO1
R344 10K Dummy +/-5% r0603h6
R345 10K Dummy +/-5% r0603h6
R346 10K Dummy +/-5% r0603h6
C497 0.1uF 50V, Y5V, +80%/-20% C0603
R347 3.3K +/-5% R0603
R348 3.3K +/-5% R0603
R349 47 Dummy
R350 Dummy 0
R352 Dummy 0
R353 47 Dummy +/-5% R0603
close to ICH7
close to ICH7 within 100 mils
U34
SST25LF040A SOP8JG
SPI Population Options
R707 8.2K Dummy +/-5% r0603h6
R708 8.2K Dummy +/-5% r0603h6
R709 8.2K Dummy +/-5% r0603h6
R710 8.2K Dummy +/-5% r0603h6
R711 8.2K Dummy +/-5% r0603h6
R712 8.2K Dummy +/-5% r0603h6
R713 8.2K Dummy +/-5% r0603h6
R714 8.2K Dummy +/-5% r0603h6
R715 8.2K Dummy +/-5% r0603h6
R716 8.2K Dummy +/-5% r0603h6
SPI
Header_2X4
H1 Mounting Hole
H2 Mounting Hole
H3 Mounting Hole
H4 Mounting Hole
H5 Mounting Hole
H6 Mounting Hole
H7 Mounting Hole
H8 Mounting Hole
H9 Mounting Hole
H10 Mounting Hole
mh40x80_8
GND_AUDIO
FOXCONN TECHNOLOGY COPR.
Title
FWH / SPI
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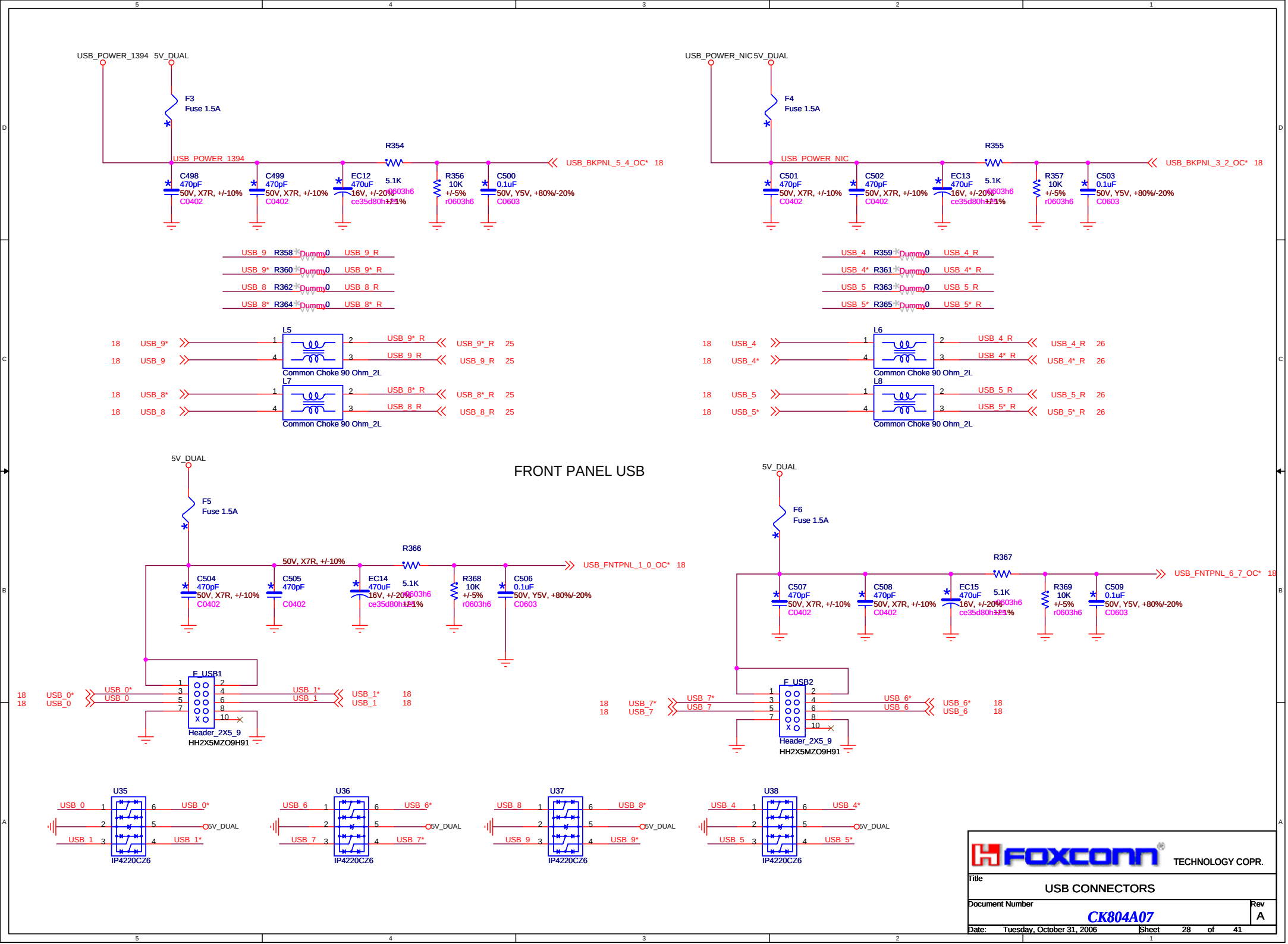
USB_POWER_1394
5V_DUAL
F3
Fuse 1.5A
R354
USB_POWER_1394
C498
470pF
50V, X7R, +/-10%
C0402
C499
470pF
50V, X7R, +/-10%
C0402
EC12
470uF
16V, +/-20%
ce35d80h+1
5.1K
0603h6
R356
10K
+/-5%
r0603h6
C500
0.1uF
50V, Y5V, +80%/-20%
C0603
USB_BKPNL_5_4_OC* 18
USB_POWER_NIC
5V_DUAL
F4
Fuse 1.5A
R355
USB_POWER_NIC
C501
470pF
50V, X7R, +/-10%
C0402
C502
470pF
50V, X7R, +/-10%
C0402
EC13
470uF
16V, +/-20%
ce35d80h+1
5.1K
0603h6
R357
10K
+/-5%
r0603h6
C503
0.1uF
50V, Y5V, +80%/-20%
C0603
USB_BKPNL_3_2_OC* 18
USB_9 R358 Dummy 0 USB_9_R
USB_9* R360 Dummy 0 USB_9*_R
USB_8 R362 Dummy 0 USB_8_R
USB_8* R364 Dummy 0 USB_8*_R
USB_4 R359 Dummy 0 USB_4_R
USB_4* R361 Dummy 0 USB_4*_R
USB_5 R363 Dummy 0 USB_5_R
USB_5* R365 Dummy 0 USB_5*_R
L5
18 USB_9* 1 2 USB_9*_R USB_9*_R 25
18 USB_9 4 3 USB_9_R USB_9_R 25
Common Choke 90 Ohm_2L
L7
18 USB_8* 1 2 USB_8*_R USB_8*_R 25
18 USB_8 4 3 USB_8_R USB_8_R 25
Common Choke 90 Ohm_2L
L6
18 USB_4 1 2 USB_4_R USB_4_R 26
18 USB_4* 4 3 USB_4*_R USB_4*_R 26
Common Choke 90 Ohm_2L
L8
18 USB_5 1 2 USB_5_R USB_5_R 26
18 USB_5* 4 3 USB_5*_R USB_5*_R 26
Common Choke 90 Ohm_2L
FRONT PANEL USB
5V_DUAL
F5
Fuse 1.5A
R366
50V, X7R, +/-10%
C504
470pF
50V, X7R, +/-10%
C0402
C505
470pF
C0402
EC14
470uF
16V, +/-20%
ce35d80h+1
5.1K
0603h6
R368
10K
+/-5%
r0603h6
C506
0.1uF
50V, Y5V, +80%/-20%
C0603
USB_FNTPNL_1_0_OC* 18
F_USB1
18 USB_0* USB_0* USB_0
USB_1* USB_1 USB_1* 18
USB_1 18
Header_2X5_9
HH2X5MZO9H91
5V_DUAL
F6
Fuse 1.5A
R367
C507
470pF
50V, X7R, +/-10%
C0402
C508
470pF
50V, X7R, +/-10%
C0402
EC15
470uF
16V, +/-20%
ce35d80h+1
5.1K
0603h6
R369
10K
+/-5%
r0603h6
C509
0.1uF
50V, Y5V, +80%/-20%
C0603
USB_FNTPNL_6_7_OC* 18
F_USB2
18 USB_7* USB_7* USB_7
USB_6* USB_6 USB_6* 18
USB_6 18
Header_2X5_9
HH2X5MZO9H91
U35
USB_0 1 6 USB_0*
2 5 5V_DUAL
USB_1 3 4 USB_1*
IP4220CZ6
U36
USB_6 1 6 USB_6*
2 5 5V_DUAL
USB_7 3 4 USB_7*
IP4220CZ6
U37
USB_8 1 6 USB_8*
2 5 5V_DUAL
USB_9 3 4 USB_9*
IP4220CZ6
U38
USB_4 1 6 USB_4*
2 5 5V_DUAL
USB_5 3 4 USB_5*
IP4220CZ6
FOXCONN TECHNOLOGY COPR.
Title
USB CONNECTORS
Document Number
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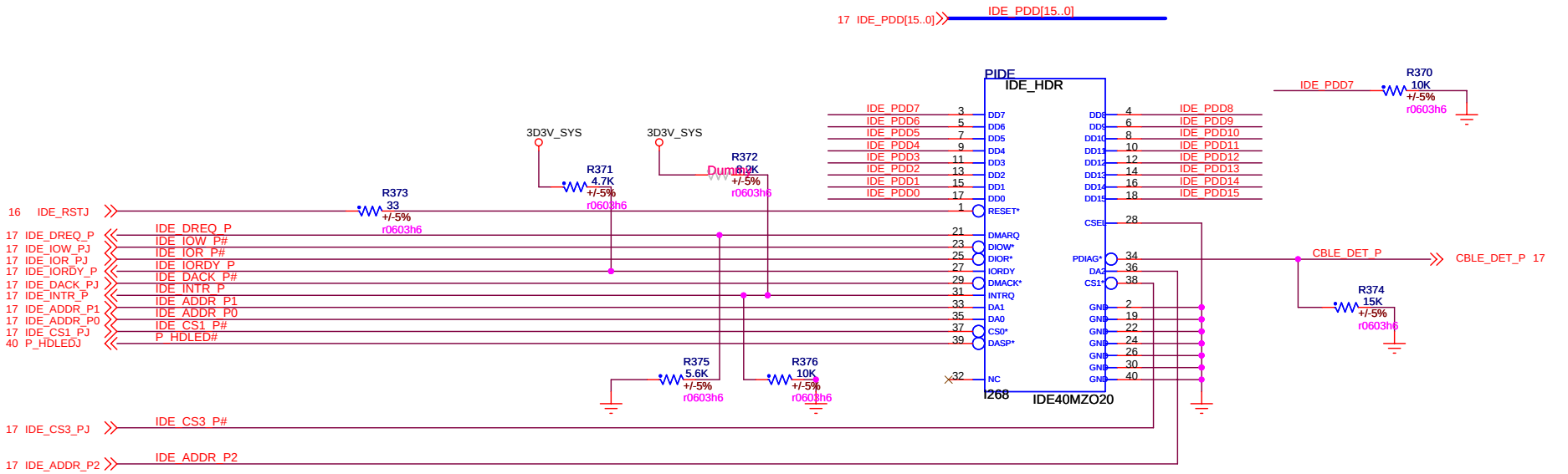


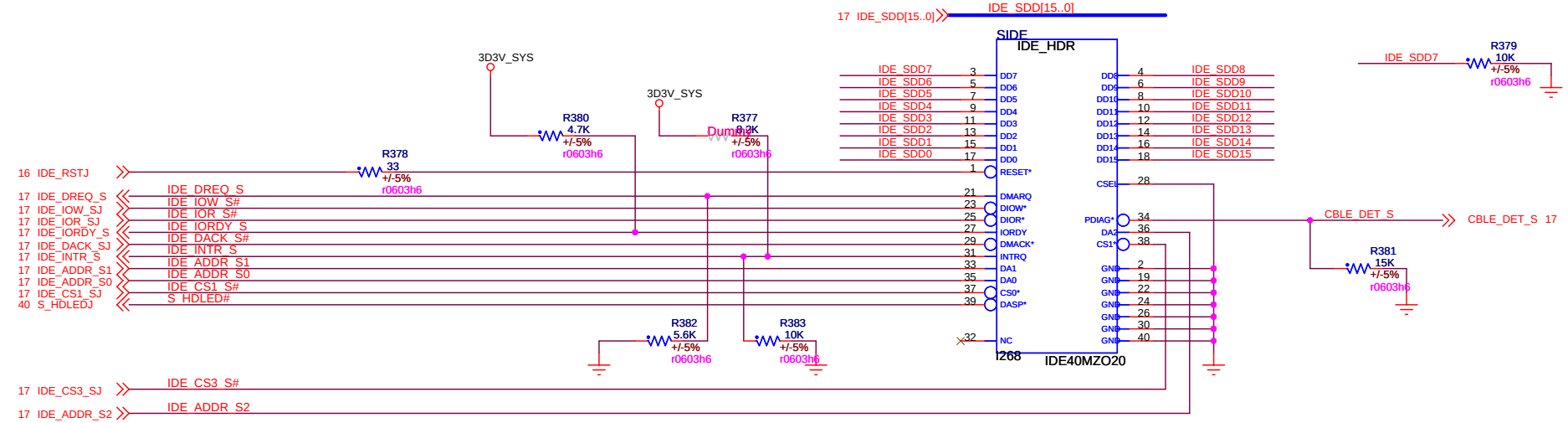


FOXCONN TECHNOLOGY COPR.

Title: IDE CONNECTORS

Document Number: CK804A07

Rev: A

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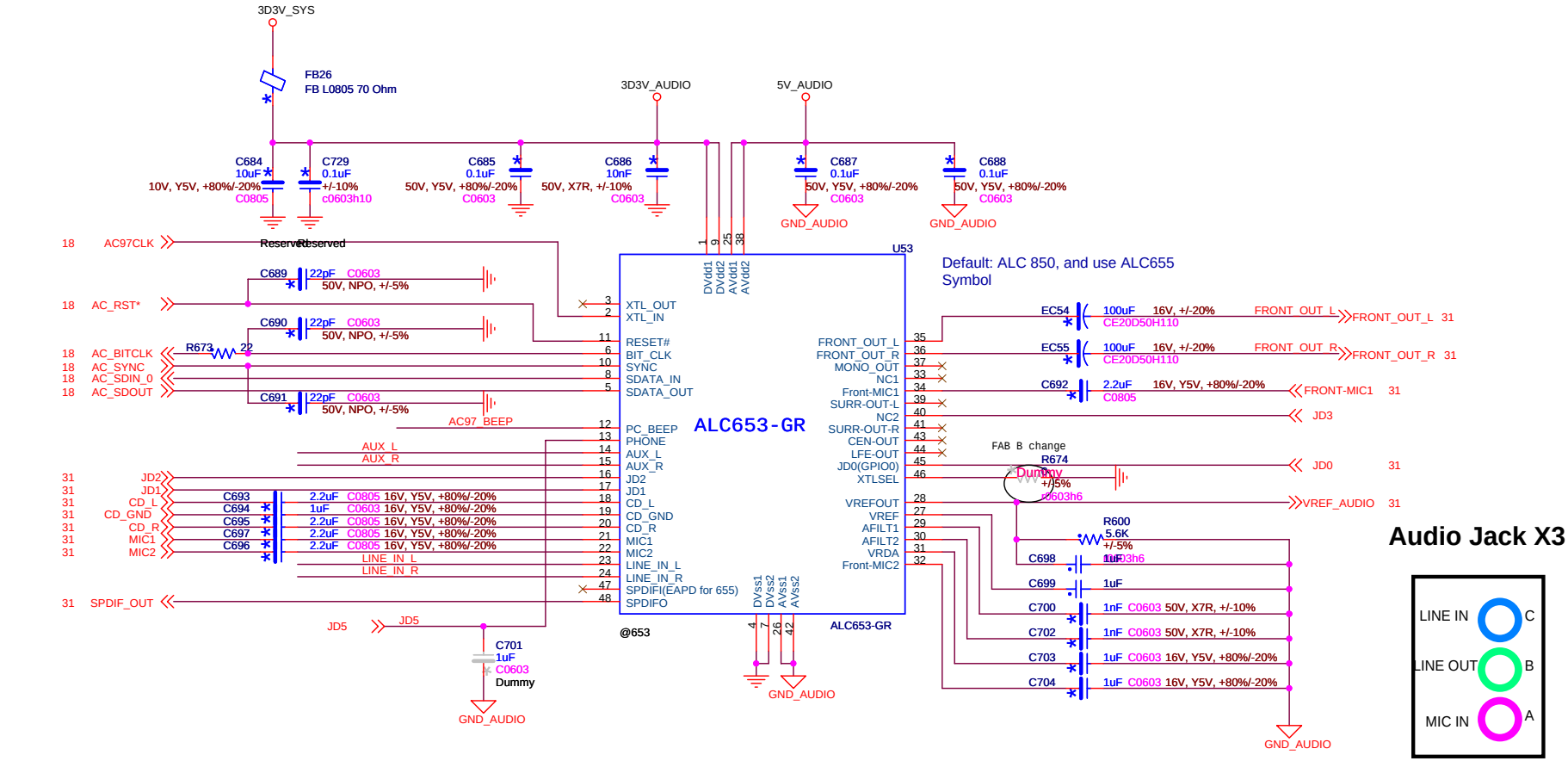


FOXCONN TECHNOLOGY COPR.

Title: AUDIO ALC653/850

Document Number: CK804A07

Rev: A

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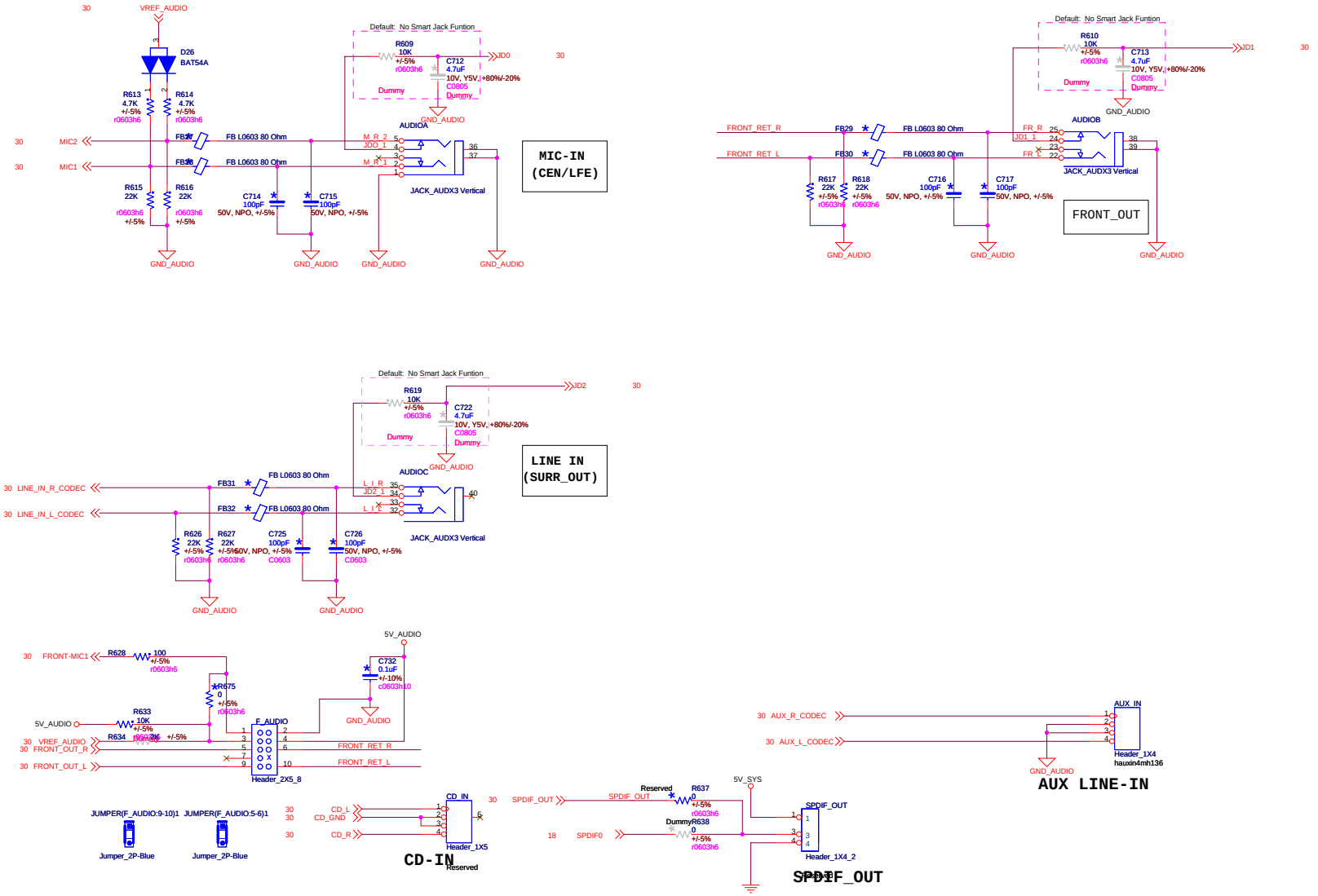


| | |
|---|---|
| FOXCONN TECHNOLOGY COPR. | |
| Title | AUDIO CONNECTORS 653/850 |
| Document Number | CK804A07 |
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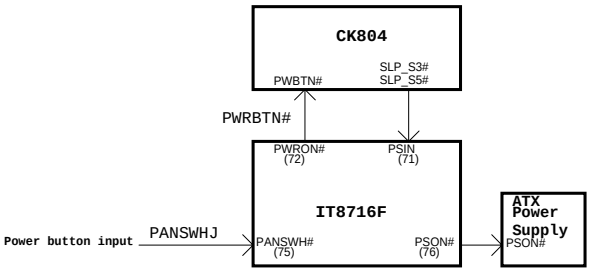
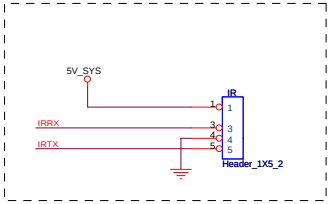
**Power On Strapping Options**

| | Symbol | value | Description |
|---|---|---|---|
| JP1 | Flashseg1_EN | 1 | Disabled. |
| | | 0 | Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled |
| JP2 | SerFlh_SO_SEL | 1 | FLH_SO1 is selected as the Serial Flash I/F SO pin. |
| | | 0 | FLH_SO2 is selected as the Serial Flash I/F SO pin. |
| JP3 | CHIP_SEL | -- | Chip selection in configuration. |
| JP4 | BUF_SEL | 1 | The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are open-drain. |
| | | 0 | The output buffers are push-pull. |
| JP5 | FAN_CTL_SEL | 1 | The default value of EC Index 15h / 16h / 17h is 00h |
| | | 0 | The default value of EC Index 15h / 16h / 17h is 40h |
| JP6 | VID_ISEL | 1 | The threshold voltage of VID is 2.0 / 0.8V |
| | | 0 | The threshold voltage of VID is 0.8 / 0.4V |

POWER ON SCHEME




IR Connector




Note:

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)




| | |
|---|---|
| FOXCONN TECHNOLOGY COPR. | |
| Title | SIO ITE8716 |
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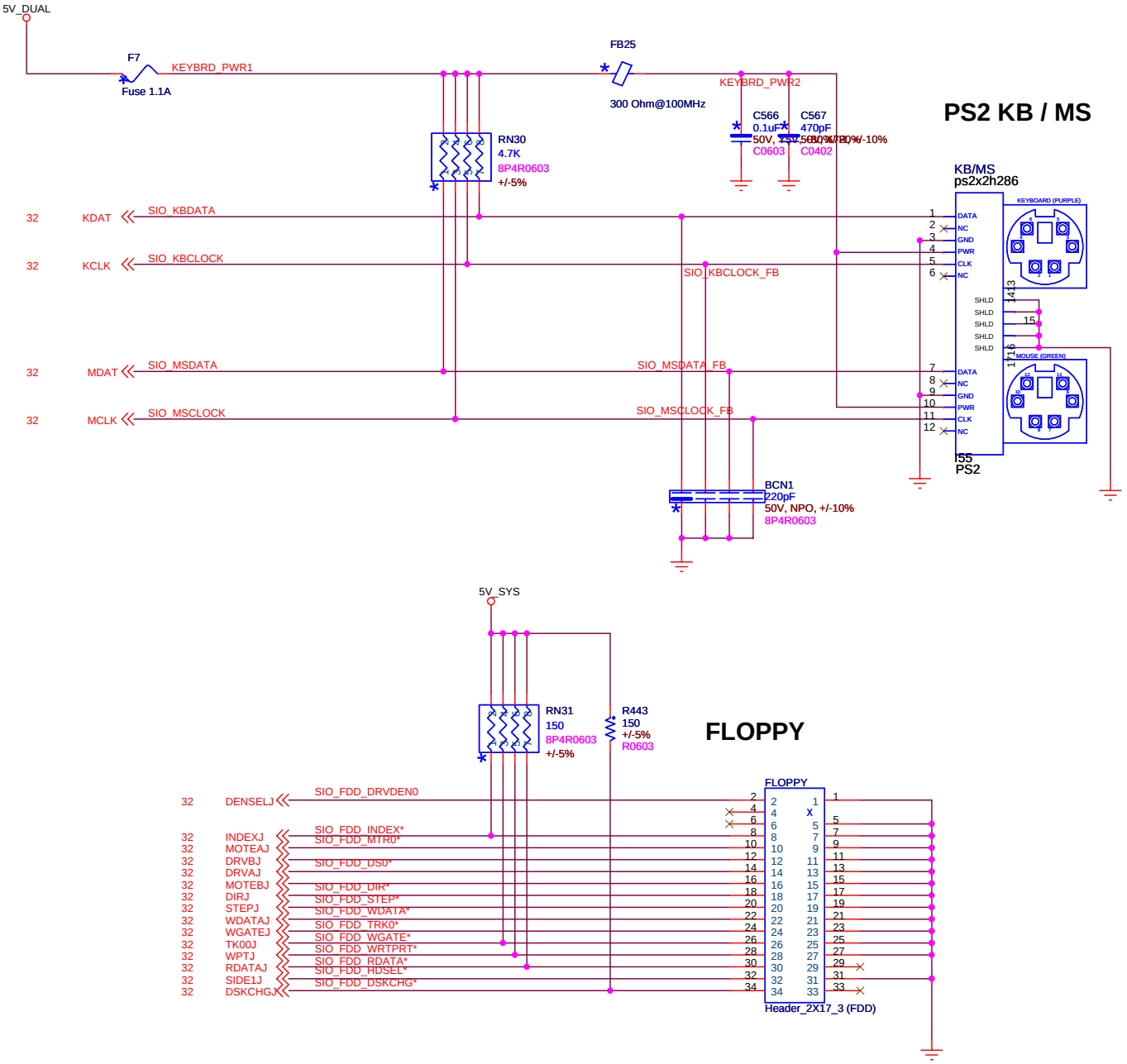


FOXCONN TECHNOLOGY COPR.

| | |
|---|---|
| Title | FDD / PS2 |
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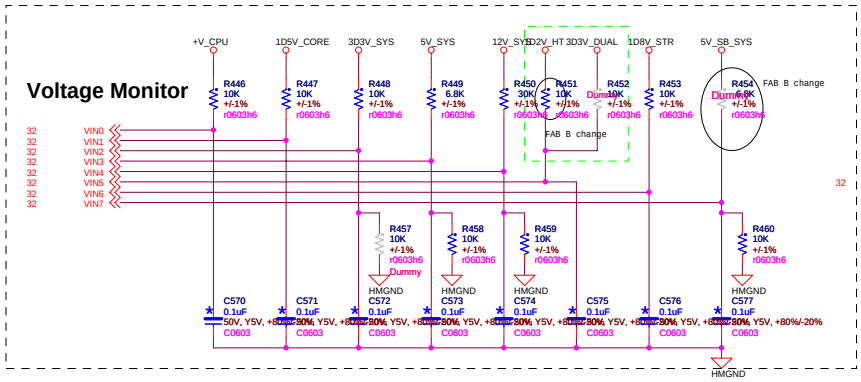
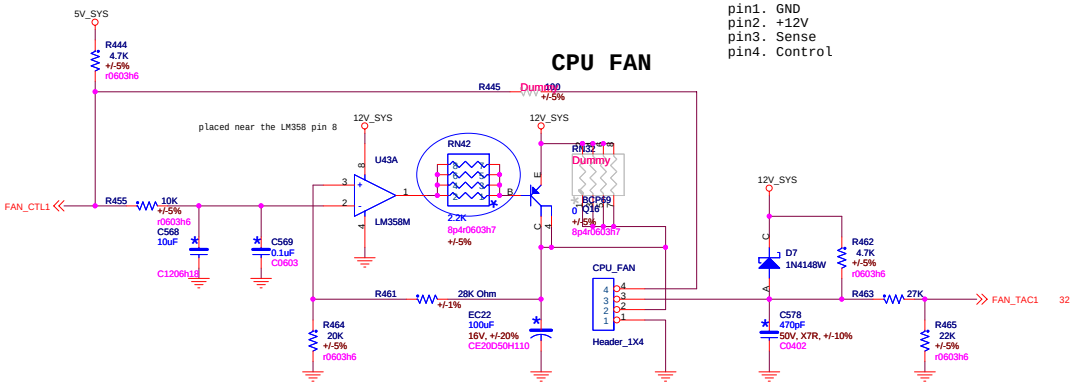
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

## Voltage Monitor

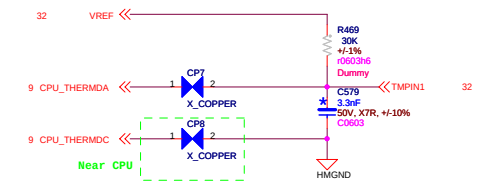


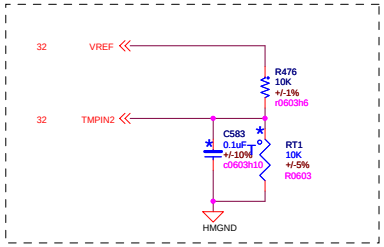

## CPU FAN



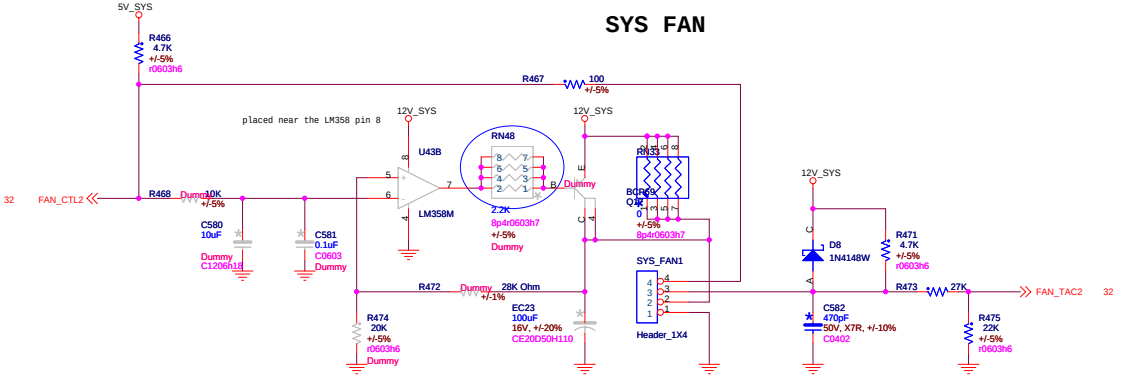

## Thermal Controller

Thermal Diode layout notice:
a. Place T.D. close to IT8712F/H.
c. Recommanded trace widths & spacings is 10 miles.
b. Keep the trace away from; +12V, Fast data bus, CRTs.
d. Isolate GNDA, GND.

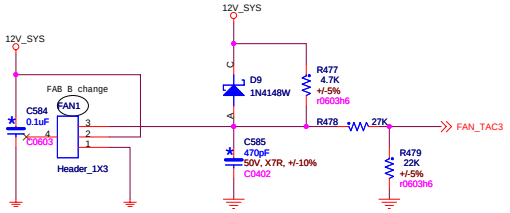



## SYS FAN




## CHIP FAN




FOXCONN TECHNOLOGY COPR.

| | |
|---|---|
| Title | FAN / HARDWARE MONITOR |
| Document Number | CK804A07 |
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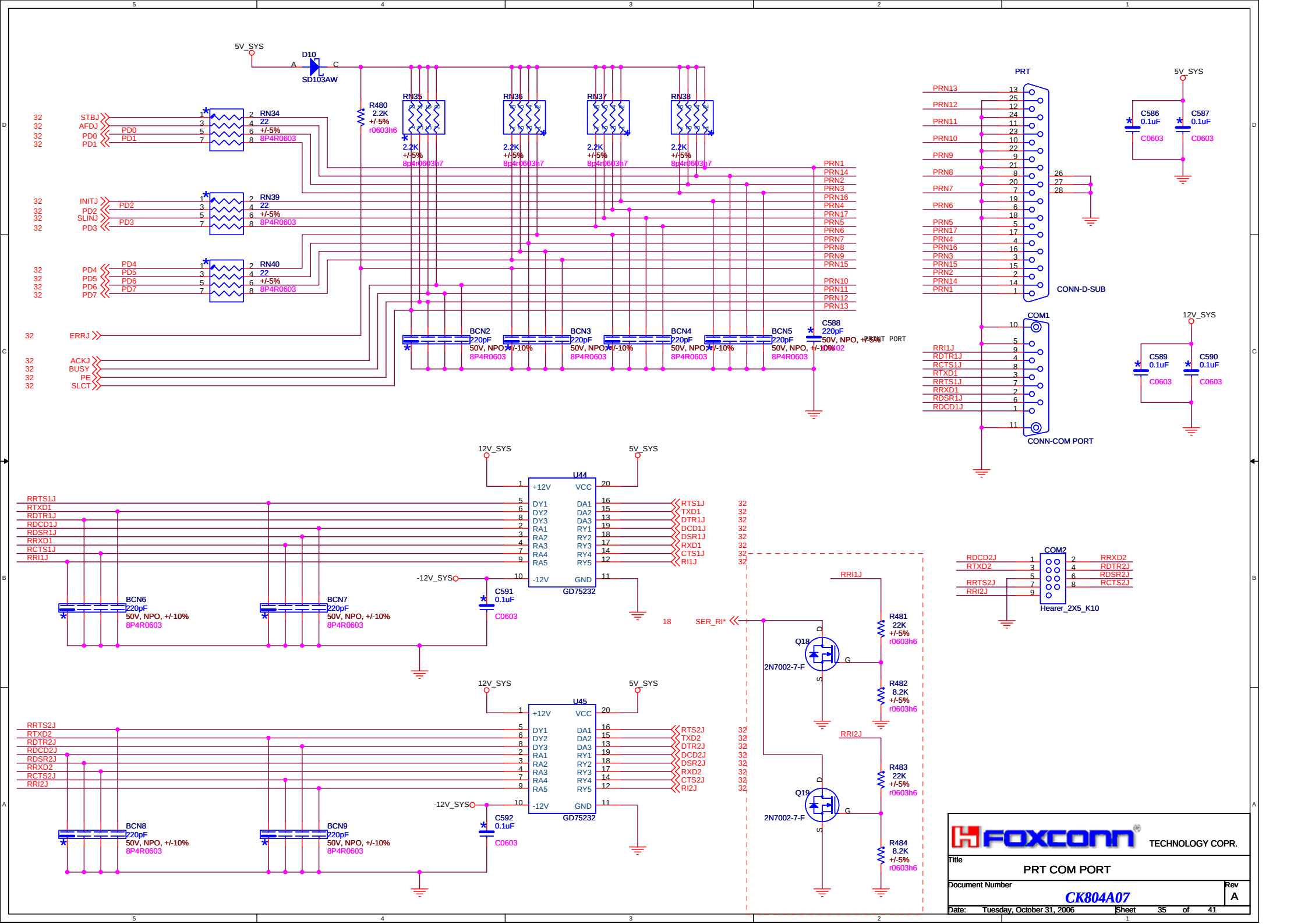
5V_SYS
D10
SD103AW
R480
2.2K
+/-5%
r0603h6
RN34
RN35
RN36
RN37
RN38
RN39
RN40
22
+/-5%
8P4R0603
2.2K
8p4r0603h7
STBJ
AFDJ
INITJ
SLINJ
ERRJ
ACKJ
BUSY
PE
SLCT
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
BCN2
BCN3
BCN4
BCN5
220pF
50V, NPO, +/-10%
8P4R0603
C588
50V, NPO, +/-10%
C0603
PRN1
PRN14
PRN2
PRN3
PRN16
PRN4
PRN17
PRN5
PRN6
PRN7
PRN8
PRN9
PRN15
PRN10
PRN11
PRN12
PRN13
PRT
CONN-D-SUB
C586
C587
0.1uF
C0603
12V_SYS
COM1
CONN-COM PORT
C589
C590
U44
U45
GD75232
+12V
VCC
-12V
GND
DY1
DY2
DY3
RA1
RA2
RA3
RA4
RA5
DA1
DA2
DA3
RY1
RY2
RY3
RY4
RY5
RRTS1J
RTXD1
RDTR1J
RDCD1J
RDSR1J
RRXD1
RCTS1J
RRI1J
RTS1J
TXD1
DTR1J
DCD1J
DSR1J
RXD1
CTS1J
RI1J
-12V_SYS
C591
C592
BCN6
BCN7
BCN8
BCN9
RRTS2J
RTXD2
RDTR2J
RDCD2J
RDSR2J
RRXD2
RCTS2J
RRI2J
RTS2J
TXD2
DTR2J
DCD2J
DSR2J
RXD2
CTS2J
RI2J
SER_RI*
Q18
Q19
2N7002-7-F
R481
R482
R483
R484
22K
8.2K
COM2
Hearer_2X5_K10
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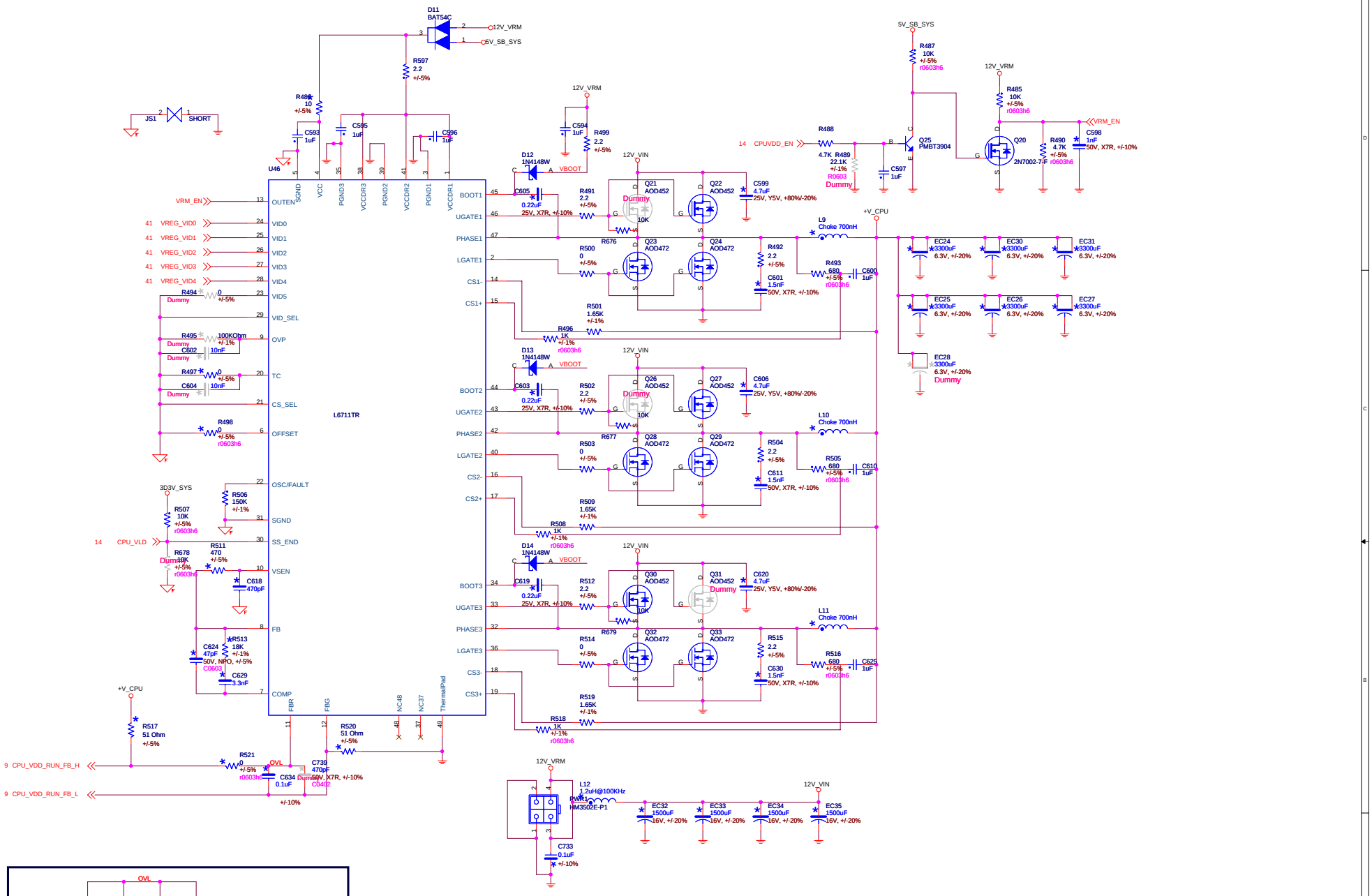
L6711TR
VCORE over VID CKT
PWM ST L6711 for AM2
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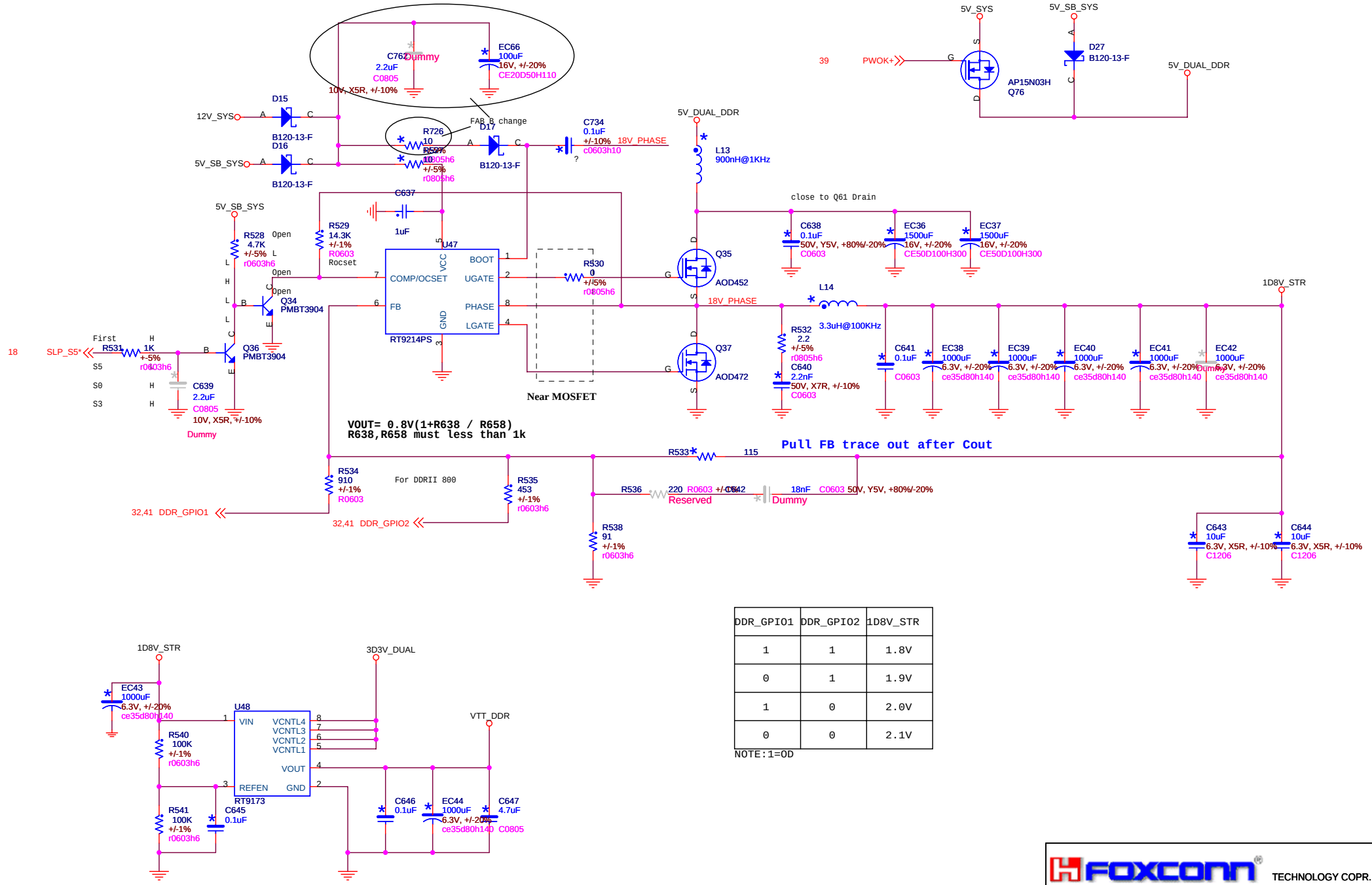


| DDR_GPIO1 | DDR_GPIO2 | 1D8V_STR |
|---|---|---|
| 1 | 1 | 1.8V |
| 0 | 1 | 1.9V |
| 1 | 0 | 2.0V |
| 0 | 0 | 2.1V |

NOTE:1=OD

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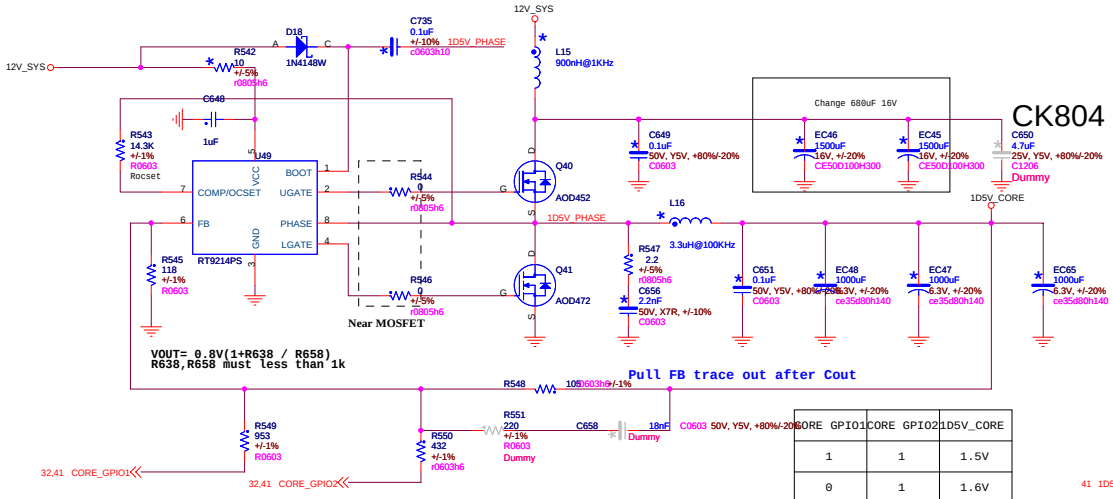
# 1D5V FOR CHIP

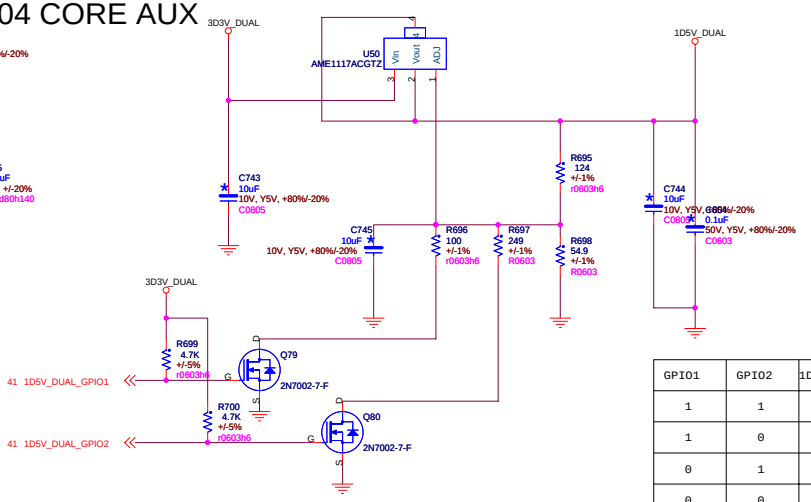



| CORE_GPIO1 | CORE_GPIO2 | 1D5V_CORE |
|---|---|---|
| 1 | 1 | 1.5V |
| 0 | 1 | 1.6V |
| 1 | 0 | 1.7V |
| 0 | 0 | 1.8V |

NOTE:1=OPEN DRAIN

1.5V_DUAL @ 275MA MAX

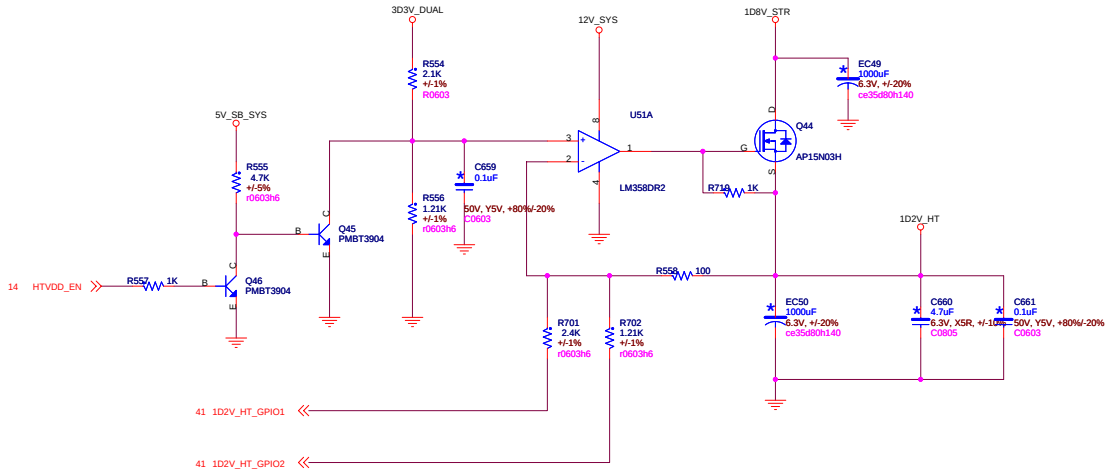
## CK804 CORE AUX

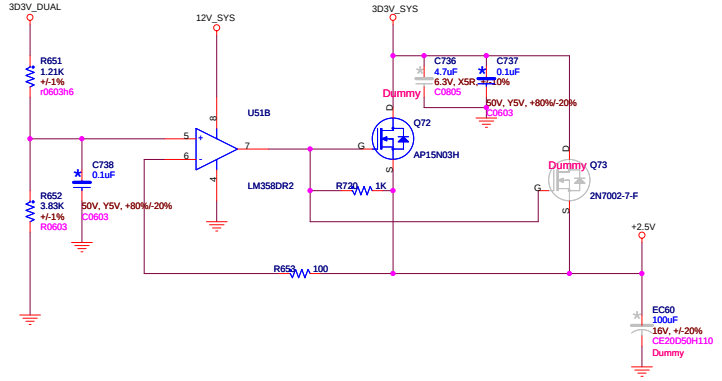



| GPIO1 | GPIO2 | 1D5V_DUAL |
|---|---|---|
| 1 | 1 | 1.5V |
| 1 | 0 | 1.6V |
| 0 | 1 | 1.7V |
| 0 | 0 | 1.8V |

NOTE:1=OPEN DRAIN

HT
1.2V @ 850MA AMPS MAX




| 1D2V_HT_GPIO1 | 1D2V_HT_GPIO2 | 1D2V_HT |
|---|---|---|
| 1 | 1 | 1.2V |
| 0 | 1 | 1.25V |
| 1 | 0 | 1.3V |
| 0 | 0 | 1.35V |

NOTE:1=OPEN DRAIN

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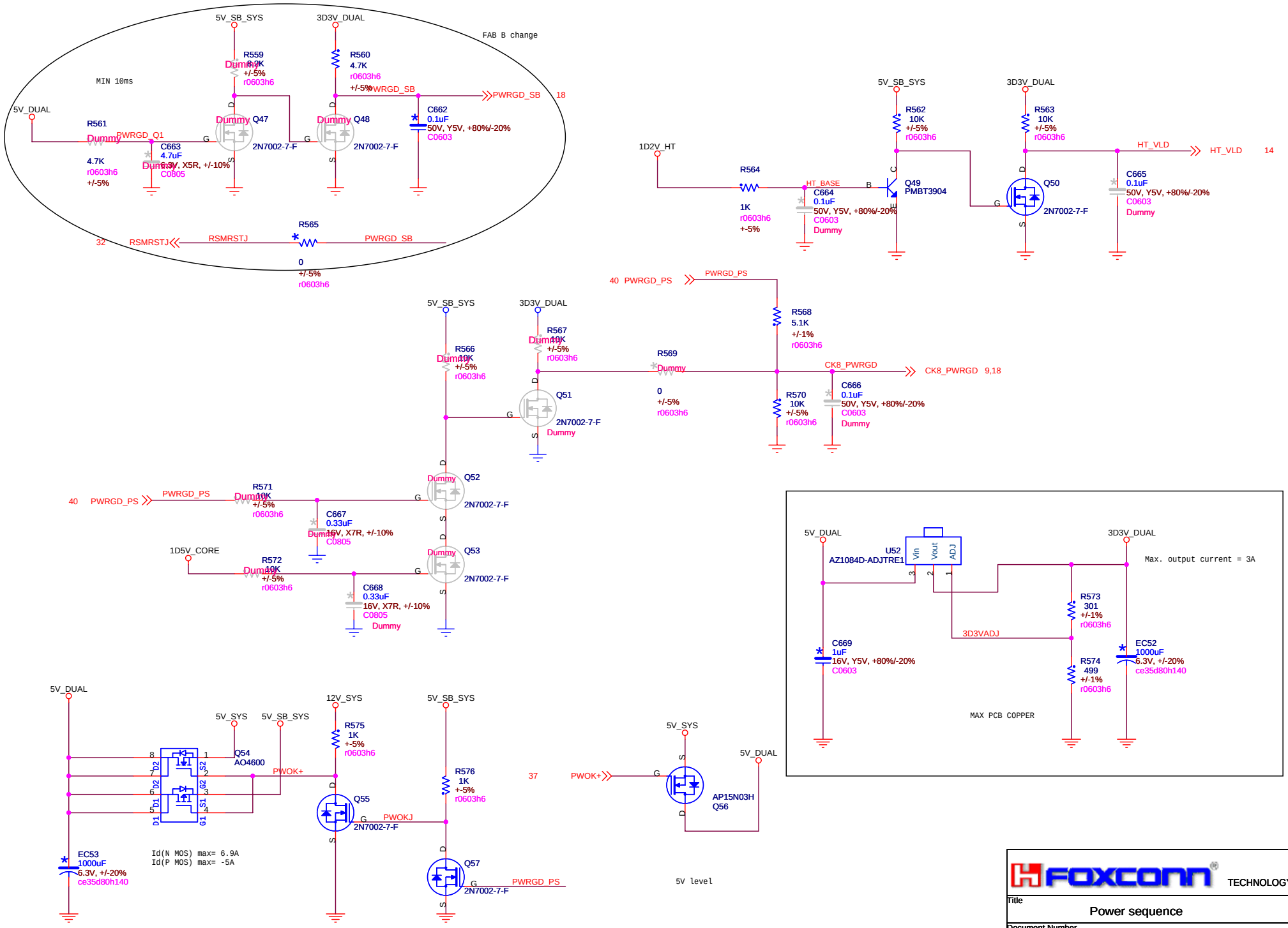
5V_SB_SYS
3D3V_DUAL
FAB B change
MIN 10ms
5V_DUAL
R559
Dummy 8.2K
+/-5%
r0603h6
R560
4.7K
r0603h6
+/-5%
PWRGD_SB
PWRGD_SB 18
R561
Dummy
PWRGD_Q1
Dummy Q47
Dummy Q48
2N7002-7-F
C662
0.1uF
50V, Y5V, +80%/-20%
C0603
C663
4.7uF
6.3V, X5R, +/-10%
C0805
4.7K
r0603h6
+/-5%
R565
0
+/-5%
r0603h6
32
RSMRSTJ
1D2V_HT
R564
1K
r0603h6
+-5%
HT_BASE
C664
0.1uF
50V, Y5V, +80%/-20%
C0603
Dummy
Q49
PMBT3904
R562
10K
+/-5%
r0603h6
R563
10K
+/-5%
r0603h6
HT_VLD
HT_VLD 14
Q50
2N7002-7-F
C665
0.1uF
50V, Y5V, +80%/-20%
C0603
Dummy
40 PWRGD_PS
R568
5.1K
+/-1%
r0603h6
R566
Dummy 10K
+/-5%
r0603h6
R567
Dummy 10K
+/-5%
r0603h6
R569
Dummy
0
+/-5%
r0603h6
CK8_PWRGD
CK8_PWRGD 9,18
R570
10K
+/-5%
r0603h6
C666
0.1uF
50V, Y5V, +80%/-20%
C0603
Dummy
Q51
2N7002-7-F
Dummy
Q52
Q53
R571
Dummy 10K
+/-5%
r0603h6
C667
Dummy 0.33uF
16V, X7R, +/-10%
C0805
1D5V_CORE
R572
Dummy 10K
+/-5%
r0603h6
C668
0.33uF
16V, X7R, +/-10%
C0805
Dummy
U52
AZ1084D-ADJTRE1
Vin
Vout
ADJ
Max. output current = 3A
R573
301
+/-1%
r0603h6
3D3VADJ
C669
1uF
16V, Y5V, +80%/-20%
C0603
R574
499
+/-1%
r0603h6
EC52
1000uF
6.3V, +/-20%
ce35d80h140
MAX PCB COPPER
12V_SYS
Q54
AO4600
R575
1K
+-5%
r0603h6
PWOK+
Q55
PWOKJ
R576
1K
+-5%
r0603h6
37
Q56
AP15N03H
Id(N MOS) max= 6.9A
Id(P MOS) max= -5A
EC53
1000uF
6.3V, +/-20%
ce35d80h140
Q57
PWRGD_PS
5V level
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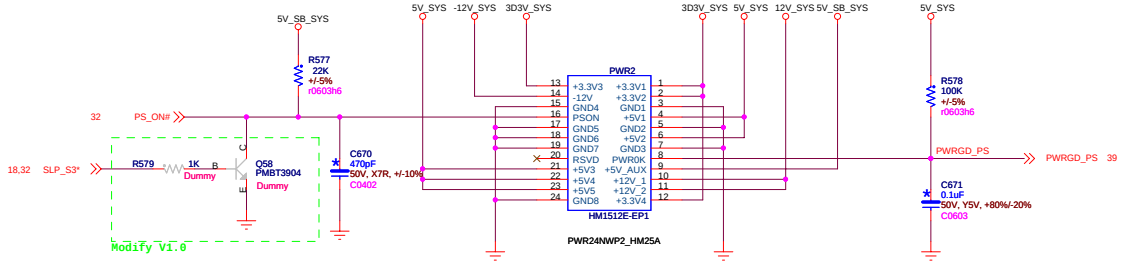
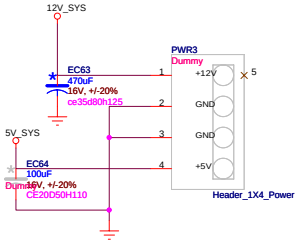
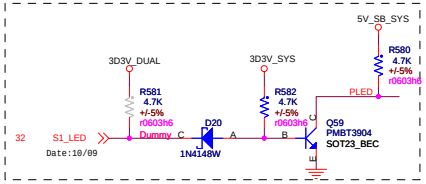
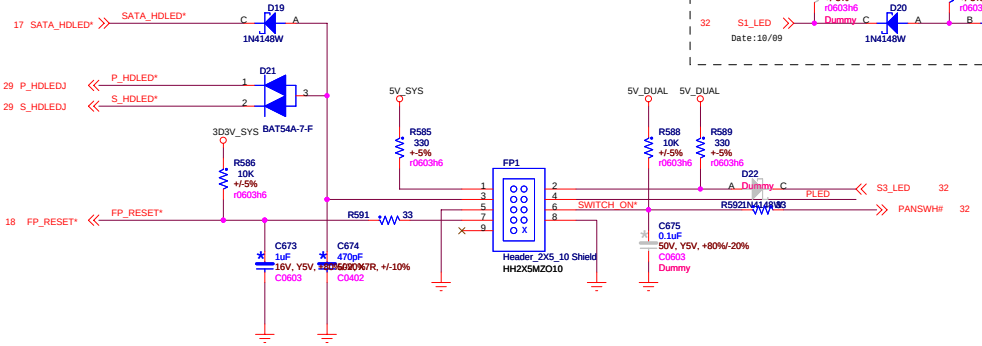
# AUX PEX PWR



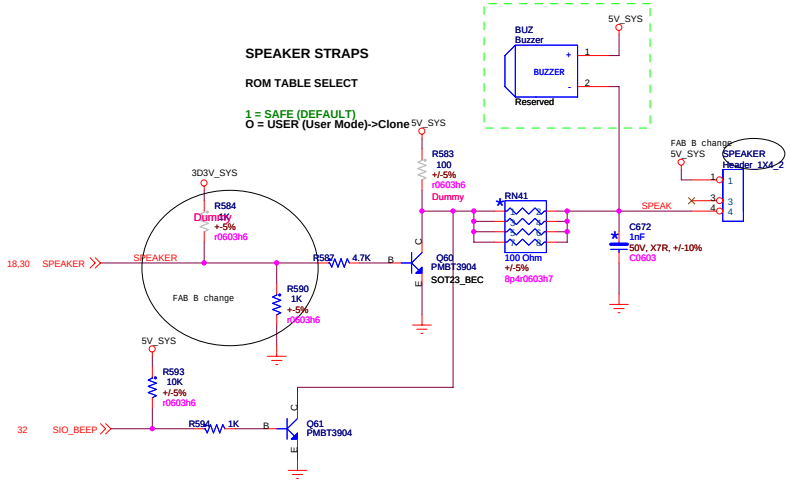



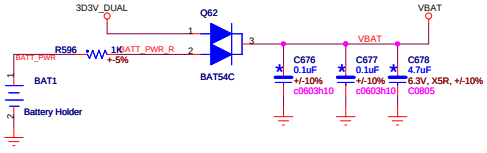



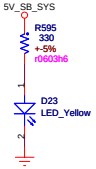

**SPEAKER STRAPS**

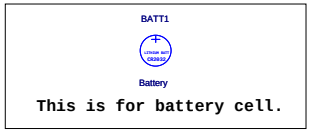
**ROM TABLE SELECT**

**1 = SAFE (DEFAULT)**
**O = USER (User Mode)->Clone**

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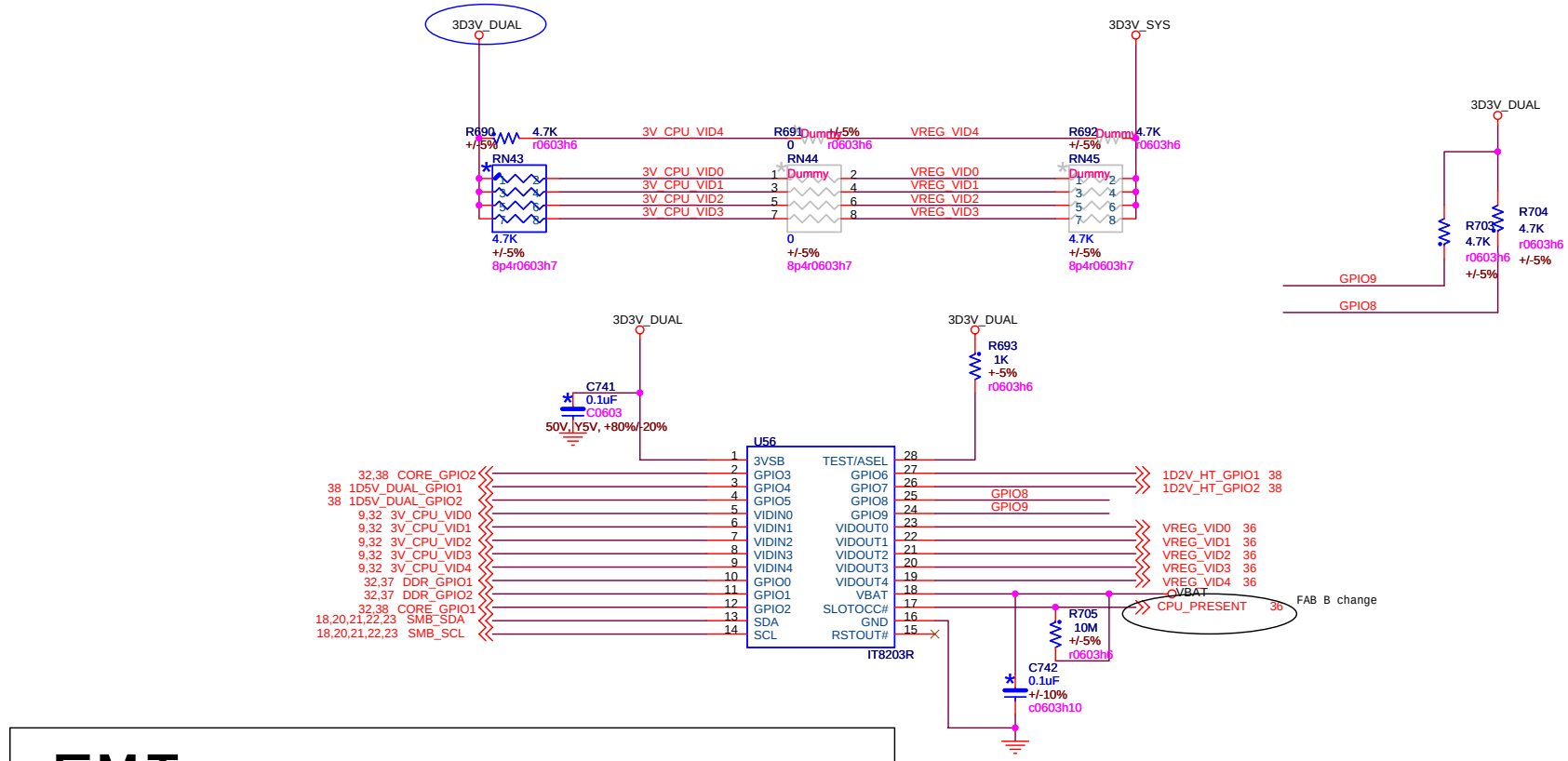


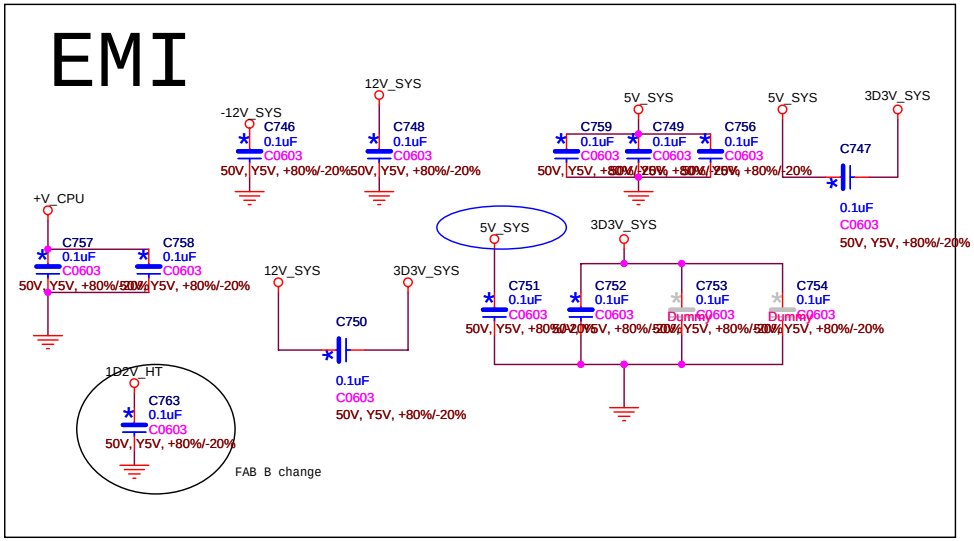


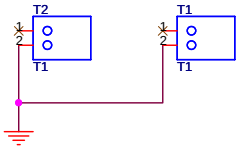


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# Fab. A to Fab.B change list

SCH change list
1,  Add VID level shift.
2,  Remove LDSTOP, PWROK, LRESET co-layout.
3,  Change R272 from 6.34K to 6.2k
4,  Add C464 10pF for EMI
5,  Change FAN circuit.
6,  Add R726, C762, EC66.
7,  Add memvld level shift.
8,  Add R725 pull high cpu_therm*

Layout change list
1,  Add VID level shift.
2,  Remove LDSTOP, PWROK, LRESET co-layout.
3,  Change FAN circuit.
4,  Add R726, C762, EC66.
5,  Add memvld level shift.
6,  Add R725 pull high cpu_therm*
7,  Add 5v_sys Power Plane for USB droop.
8,  Change silkscreen.

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| | |
|---|---|
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