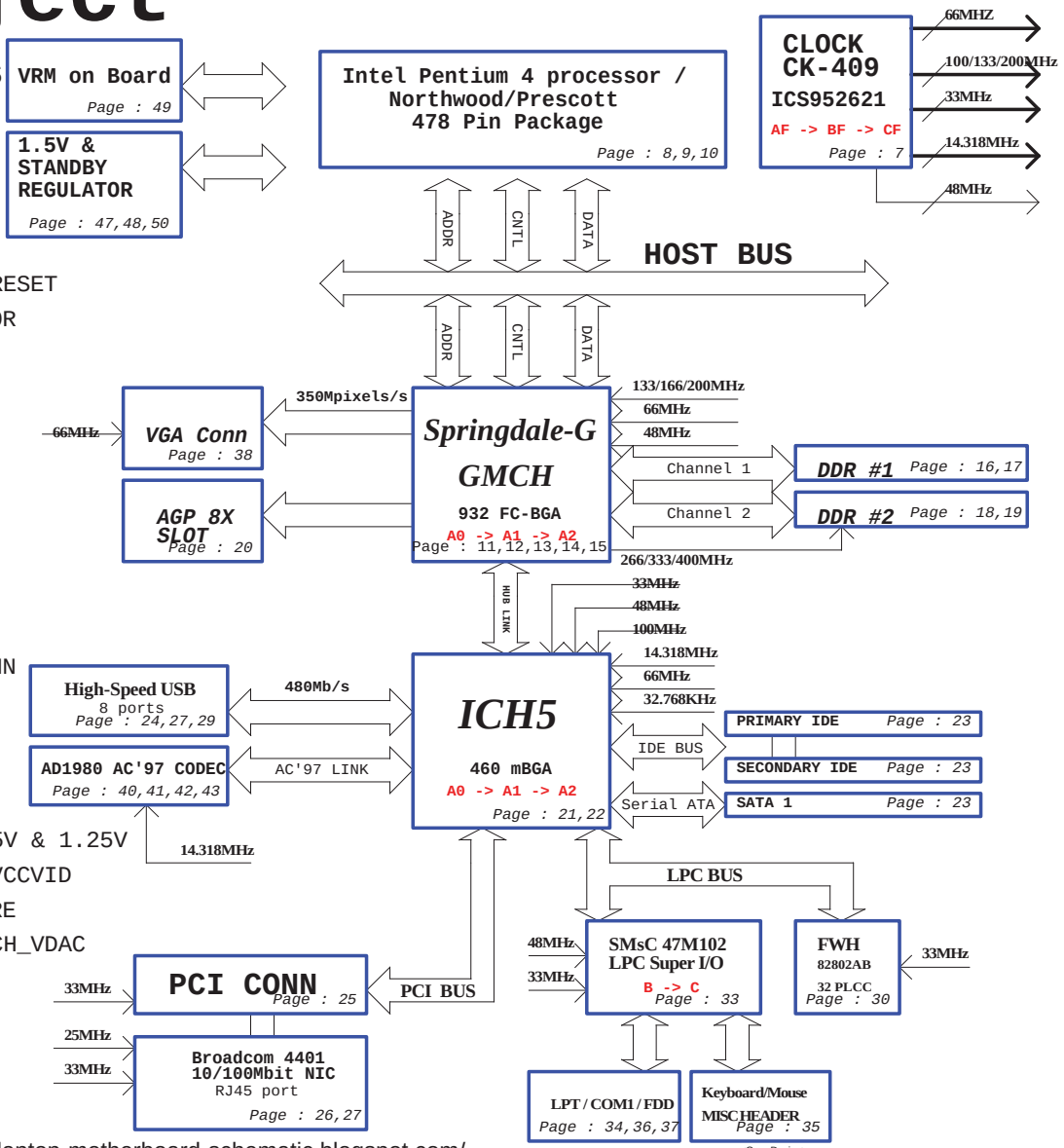
Phoenix 2 Project

Rev.X02-00(3/18/2003)-In progress



http://laptop-motherboard-schematic.blogspot.com/

<Core Design>

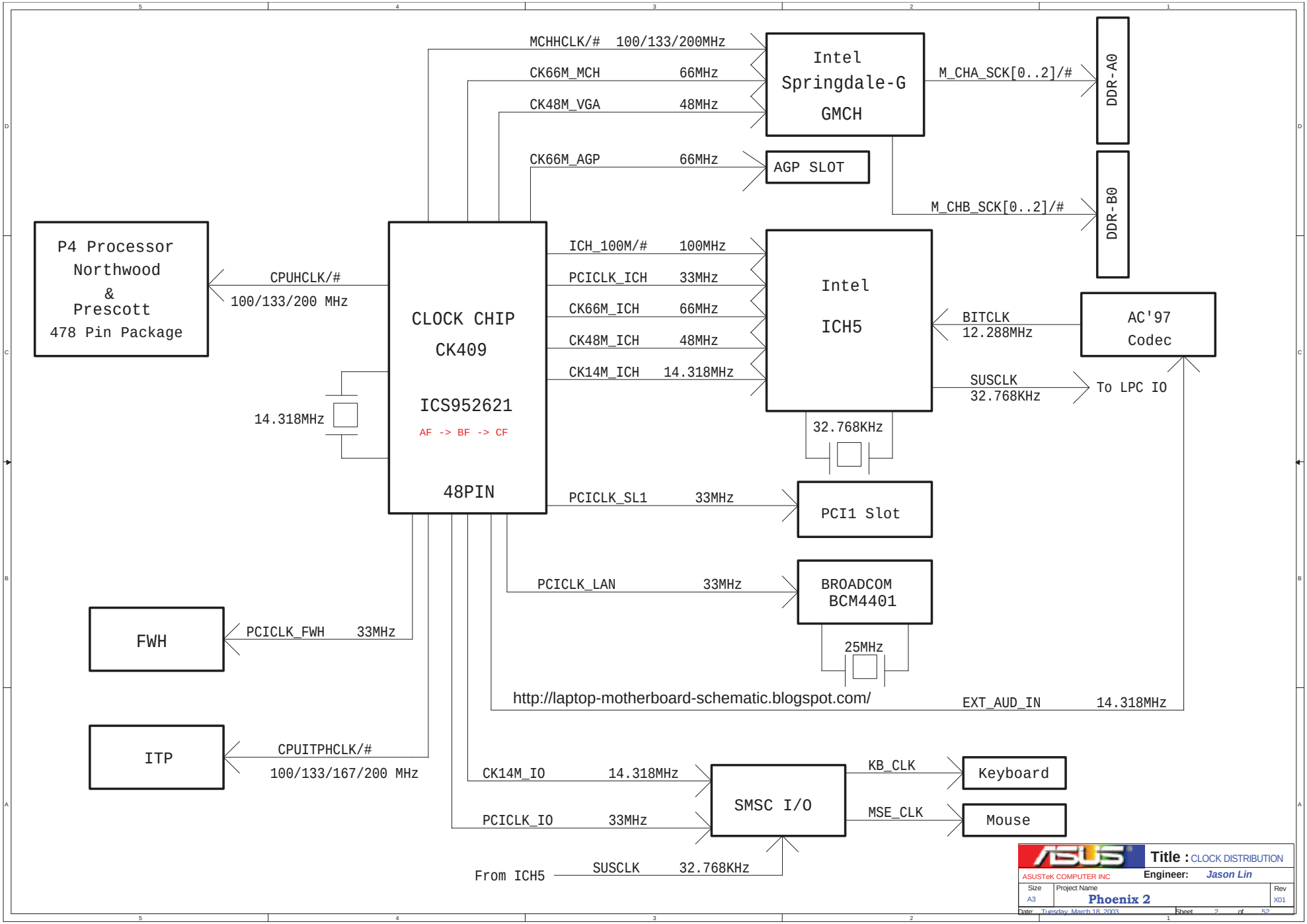
ASUStek Computer Inc.

Title : BLOCK DIAGRAM

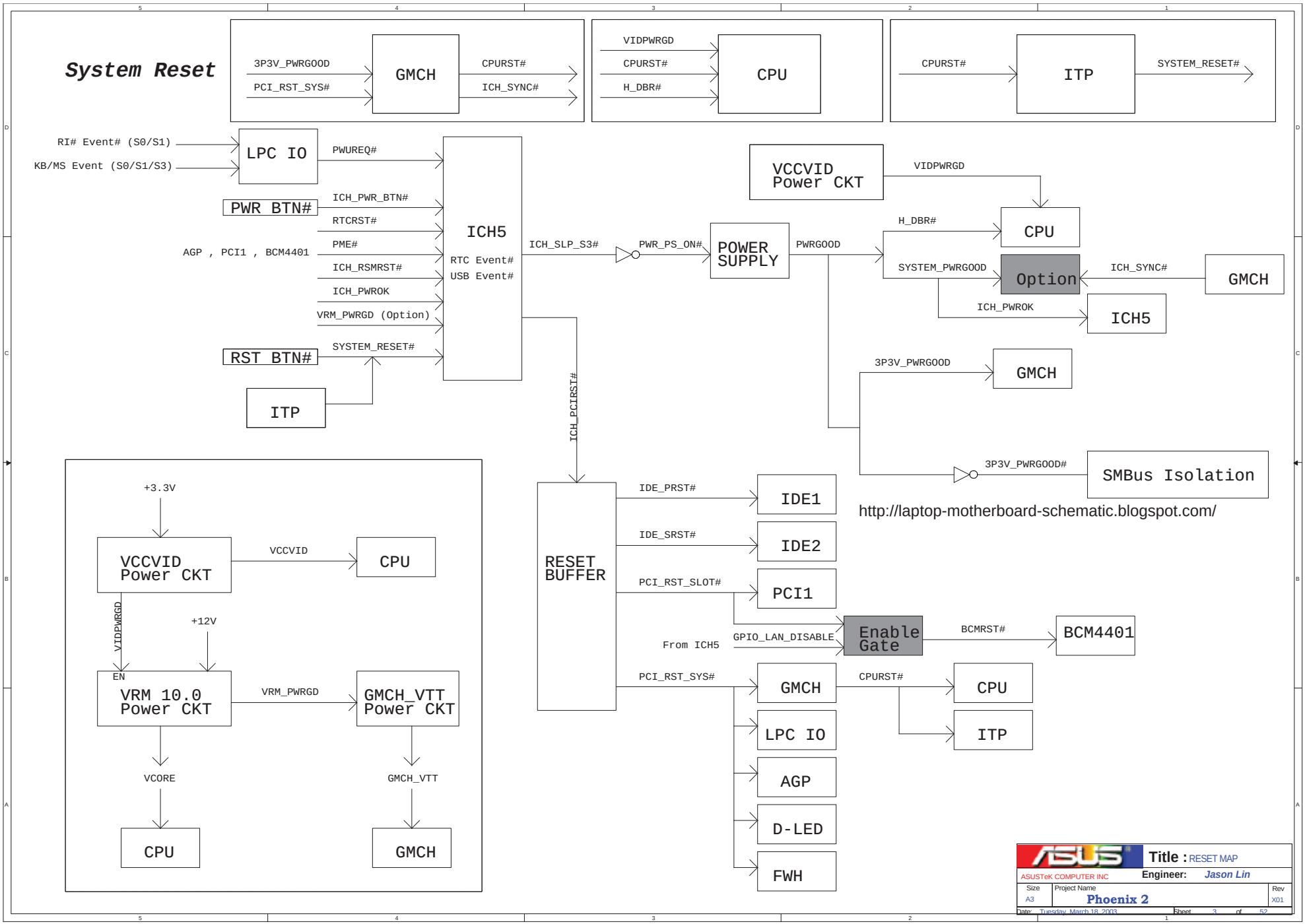
Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 1 of 52

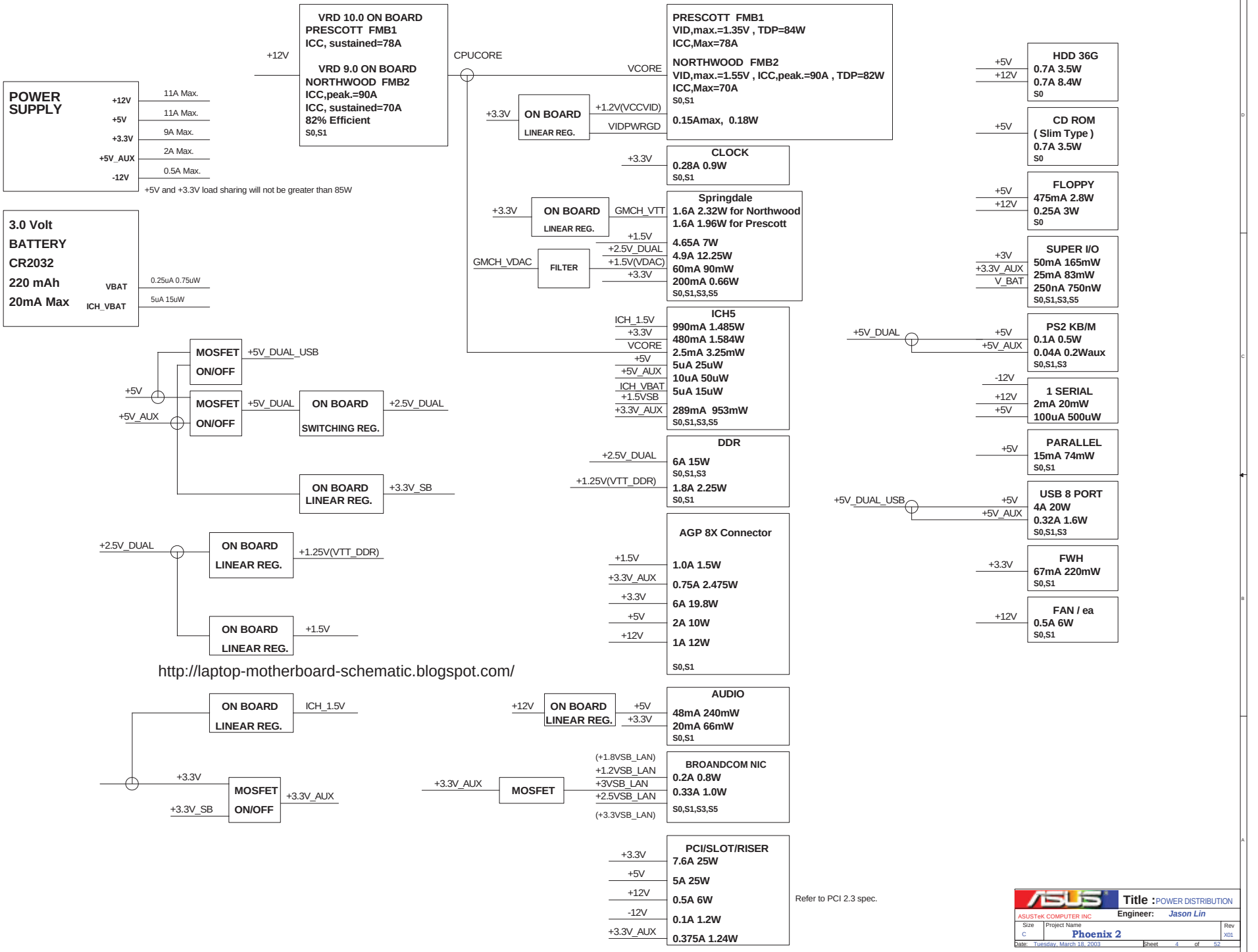

MCHHCLK/# 100/133/200MHz
CK66M_MCH 66MHz
CK48M_VGA 48MHz
CK66M_AGP 66MHz
Intel
Springdale-G
GMCH
M_CHA_SCK[0..2]/#
DDR-A0
AGP SLOT
M_CHB_SCK[0..2]/#
DDR-B0
P4 Processor
Northwood
&
Prescott
478 Pin Package
CPUHCLK/#
100/133/200 MHz
CLOCK CHIP
CK409
ICS952621
AF -> BF -> CF
48PIN
14.318MHz
ICH_100M/# 100MHz
PCICLK_ICH 33MHz
CK66M_ICH 66MHz
CK48M_ICH 48MHz
CK14M_ICH 14.318MHz
Intel
ICH5
BITCLK
12.288MHz
AC'97
Codec
SUSCLK
32.768KHz
To LPC IO
32.768KHz
PCICLK_SL1 33MHz
PCI1 Slot
PCICLK_LAN 33MHz
BROADCOM
BCM4401
25MHz
FWH
PCICLK_FWH 33MHz
http://laptop-motherboard-schematic.blogspot.com/
EXT_AUD_IN 14.318MHz
ITP
CPUITPHCLK/#
100/133/167/200 MHz
CK14M_IO 14.318MHz
PCICLK_IO 33MHz
SMSC I/O
KB_CLK
Keyboard
MSE_CLK
Mouse
From ICH5
SUSCLK 32.768KHz
Title : CLOCK DISTRIBUTION
ASUSTeK COMPUTER INC
Engineer: Jason Lin
Size A3
Project Name Phoenix 2
Rev X01
Date: Tuesday, March 18, 2003
Sheet 2 of 52

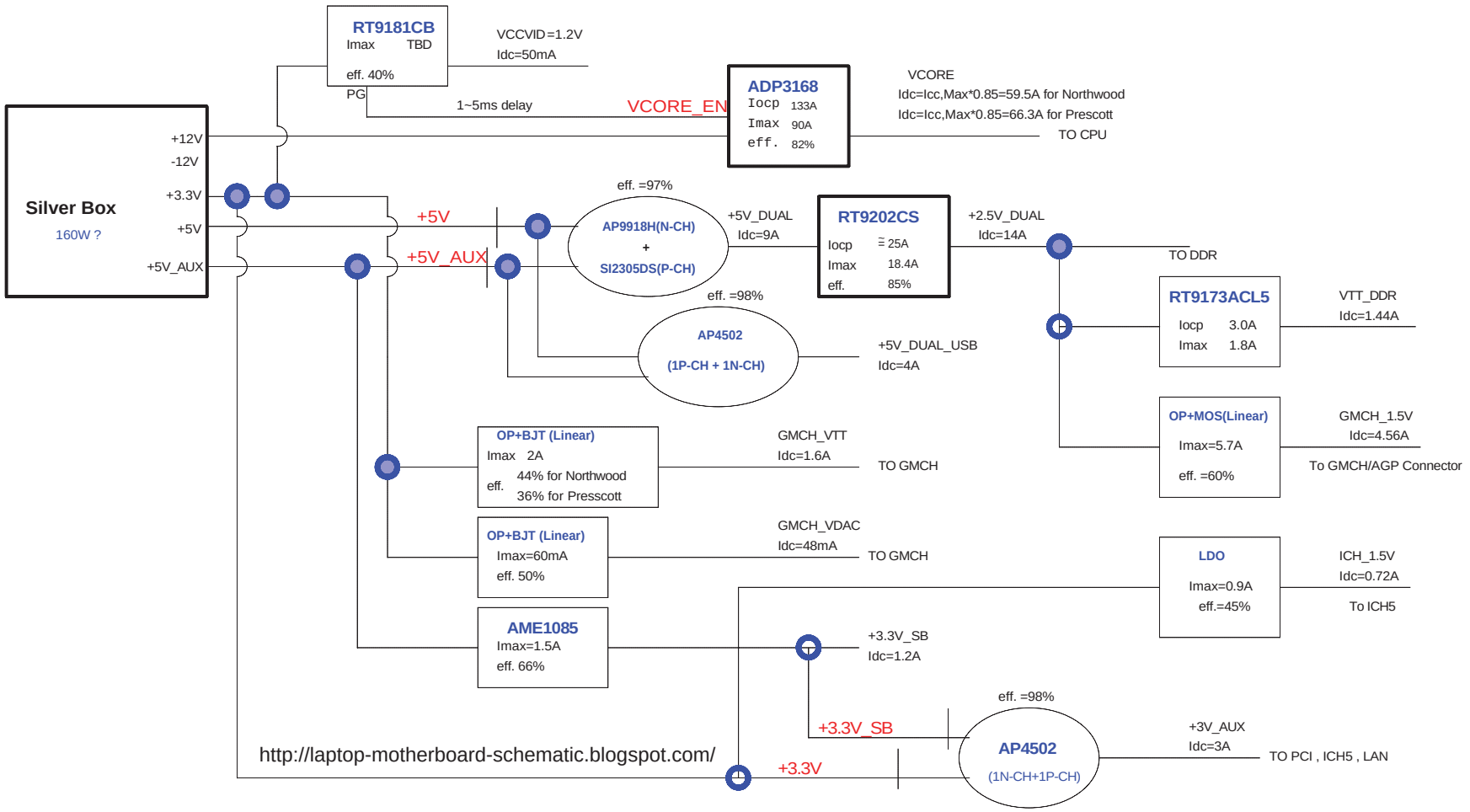
System Reset



http://laptop-motherboard-schematic.blogspot.com/

ASUSTeK COMPUTER INC	Title : RESET MAP	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 3 of 52	


POWER SUPPLY
+12V
+5V
+3.3V
+5V_AUX
-12V
11A Max.
11A Max.
9A Max.
2A Max.
0.5A Max.
+5V and +3.3V load sharing will not be greater than 85W
3.0 Volt BATTERY
CR2032
220 mAh
20mA Max
VBAT
ICH_VBAT
0.25uA 0.75uW
5uA 15uW
+12V
VRD 10.0 ON BOARD
PRESCOTT FMB1
ICC, sustained=78A
VRD 9.0 ON BOARD
NORTHWOOD FMB2
ICC,peak.=90A
ICC, sustained=70A
82% Efficient
S0,S1
CPUCORE
VCORE
PRESCOTT FMB1
VID,max.=1.35V , TDP=84W
ICC,Max=78A
NORTHWOOD FMB2
VID,max.=1.55V , ICC,peak.=90A , TDP=82W
ICC,Max=70A
S0,S1
+3.3V
ON BOARD
LINEAR REG.
+1.2V(VCCVID)
VIDPWRGD
0.15Amax, 0.18W
+3.3V
CLOCK
0.28A 0.9W
S0,S1
+3.3V
ON BOARD
LINEAR REG.
GMCH_VTT
Springdale
1.6A 2.32W for Northwood
1.6A 1.96W for Prescott
GMCH_VDAC
FILTER
+1.5V
+2.5V_DUAL
+1.5V(VDAC)
+3.3V
4.65A 7W
4.9A 12.25W
60mA 90mW
200mA 0.66W
S0,S1,S3,S5
ICH_1.5V
+3.3V
VCORE
+5V
+5V_AUX
ICH_VBAT
+1.5VSB
+3.3V_AUX
ICH5
990mA 1.485W
480mA 1.584W
2.5mA 3.25mW
5uA 25uW
10uA 50uW
5uA 15uW
289mA 953mW
S0,S1,S3,S5
+2.5V_DUAL
+1.25V(VTT_DDR)
DDR
6A 15W
S0,S1,S3
1.8A 2.25W
S0,S1
AGP 8X Connector
+1.5V
+3.3V_AUX
+3.3V
+5V
+12V
1.0A 1.5W
0.75A 2.475W
6A 19.8W
2A 10W
1A 12W
S0,S1
+12V
ON BOARD
LINEAR REG.
+5V
+3.3V
AUDIO
48mA 240mW
20mA 66mW
S0,S1
(+1.8VSB_LAN)
+1.2VSB_LAN
+3VSB_LAN
+2.5VSB_LAN
(+3.3VSB_LAN)
+3.3V_AUX
MOSFET
BROANDCOM NIC
0.2A 0.8W
0.33A 1.0W
S0,S1,S3,S5
+3.3V
+5V
+12V
-12V
+3.3V_AUX
PCI/SLOT/RISER
7.6A 25W
5A 25W
0.5A 6W
0.1A 1.2W
0.375A 1.24W
Refer to PCI 2.3 spec.
+5V
MOSFET
ON/OFF
+5V_DUAL_USB
+5V_AUX
MOSFET
ON/OFF
+5V_DUAL
ON BOARD
SWITCHING REG.
+2.5V_DUAL
ON BOARD
LINEAR REG.
+3.3V_SB
+2.5V_DUAL
ON BOARD
LINEAR REG.
+1.25V(VTT_DDR)
ON BOARD
LINEAR REG.
+1.5V
http://laptop-motherboard-schematic.blogspot.com/
ON BOARD
LINEAR REG.
ICH_1.5V
+3.3V
+3.3V_SB
MOSFET
ON/OFF
+3.3V_AUX
+5V
+12V
HDD 36G
0.7A 3.5W
0.7A 8.4W
S0
+5V
CD ROM
(Slim Type)
0.7A 3.5W
S0
+5V
+12V
FLOPPY
475mA 2.8W
0.25A 3W
S0
+3V
+3.3V_AUX
V_BAT
SUPER I/O
50mA 165mW
25mA 83mW
250nA 750nW
S0,S1,S3,S5
+5V_DUAL
+5V
+5V_AUX
PS2 KB/M
0.1A 0.5W
0.04A 0.2Waux
S0,S1,S3
-12V
+12V
+5V
1 SERIAL
2mA 20mW
100uA 500uW
+5V
PARALLEL
15mA 74mW
S0,S1
+5V_DUAL_USB
+5V
+5V_AUX
USB 8 PORT
4A 20W
0.32A 1.6W
S0,S1,S3
+3.3V
FWH
67mA 220mW
S0,S1
+12V
FAN / ea
0.5A 6W
S0,S1
ASUSTeK COMPUTER INC
Title : POWER DISTRIBUTION
Engineer: Jason Lin
Size C
Project Name Phoenix 2
Rev X01
Date: Tuesday, March 18, 2003
Sheet 4 of 52



Note:
1. **Imax is mean to peak current refered to power distribution on page 4.**
2. **Idc is mean to the sustain current , and is 80% of Imax current except Vcore is 85%.**
3. **Iocp is 1.5~2.0 times of Imax.**

Power Rail

Control Signal

Switch ON/OFF

Linear

Switching

ASUSTeK COMPUTER INC

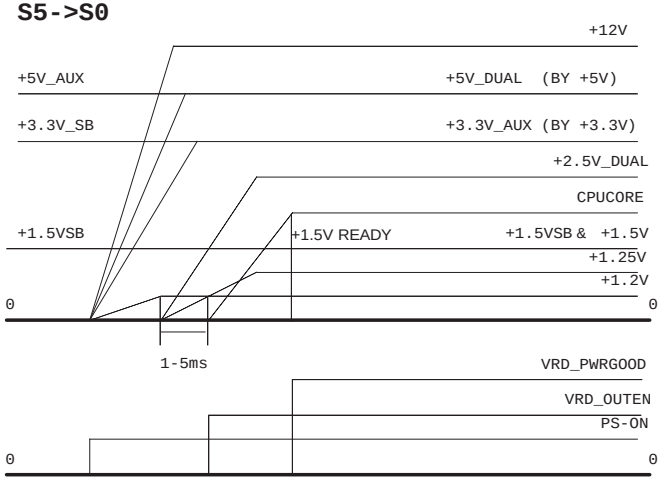
Title : POWER FLOW

Engineer: *Jason Lin*

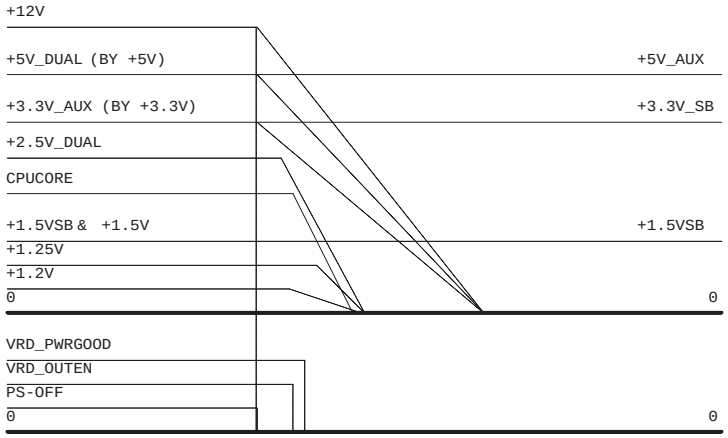
Size	Project Name	Rev
A3	**Phoenix 2**	X01

Date: Tuesday, March 18, 2003 Sheet 5 of 52

S5->S0

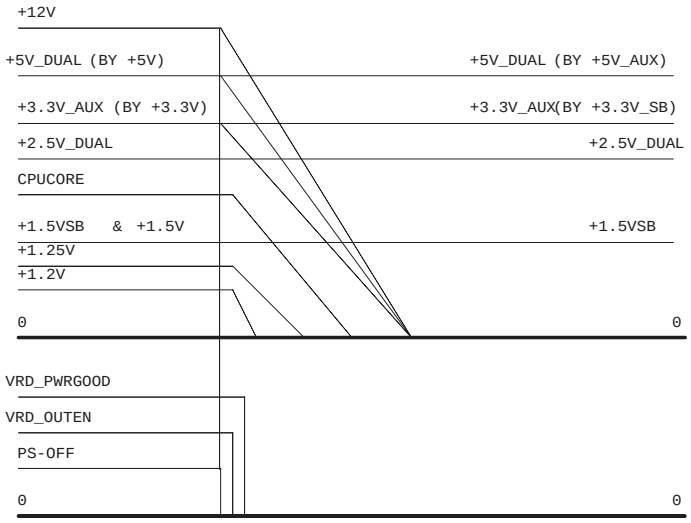


S0->S5

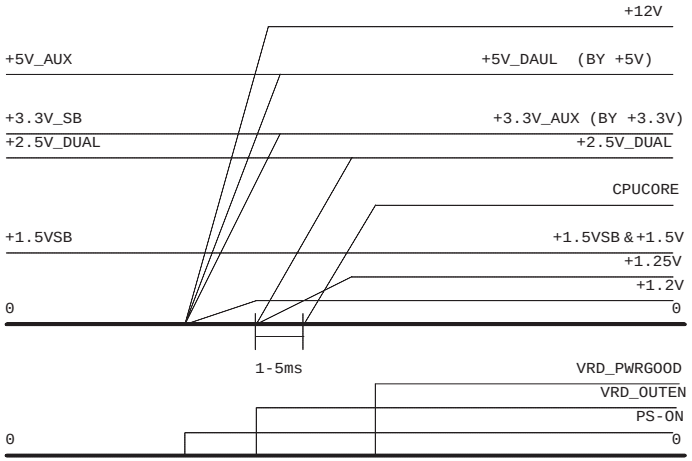


1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRD_OUTEN rises after the voltage across 90% of its specified value

S0->S3



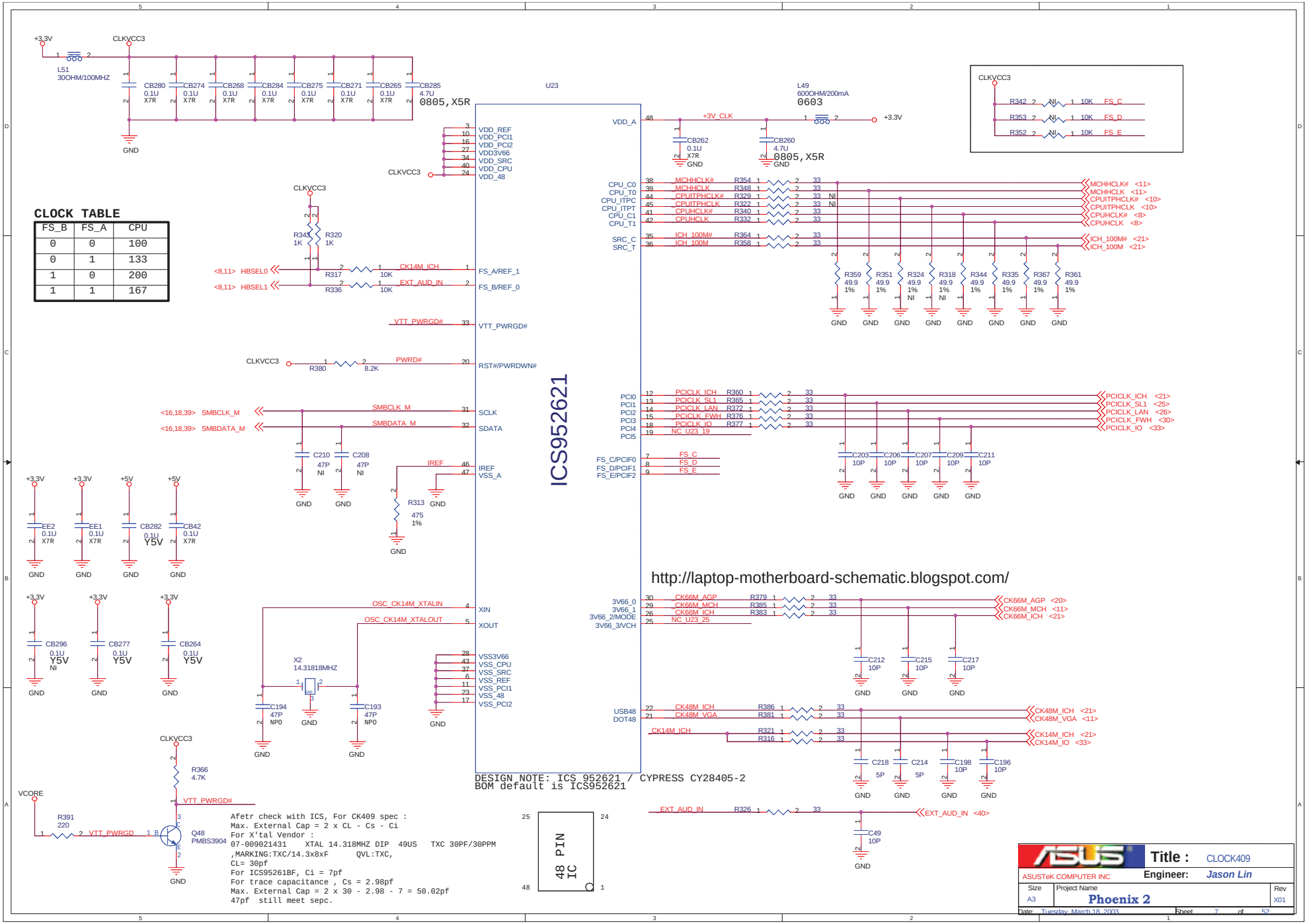
S3->S0

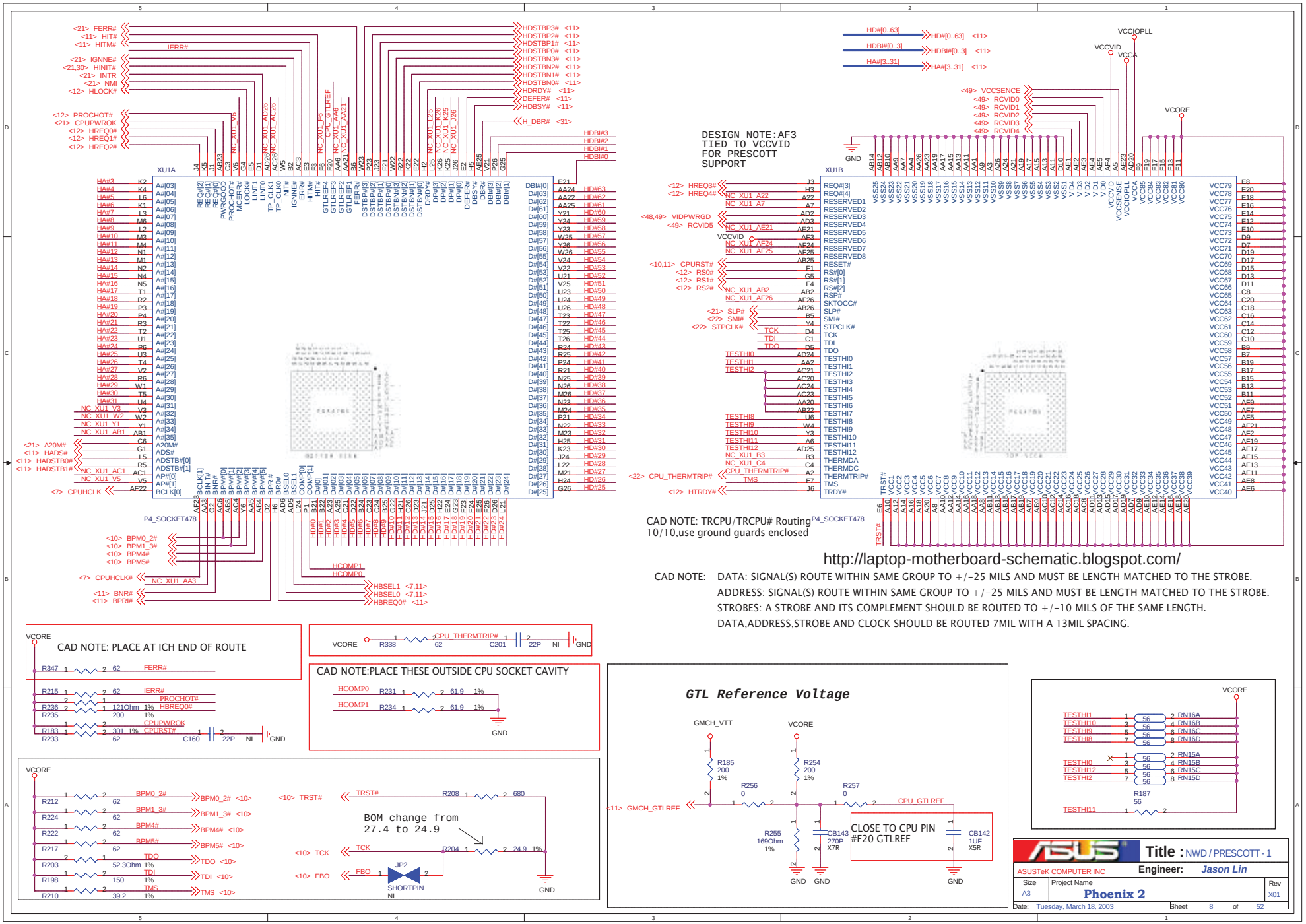


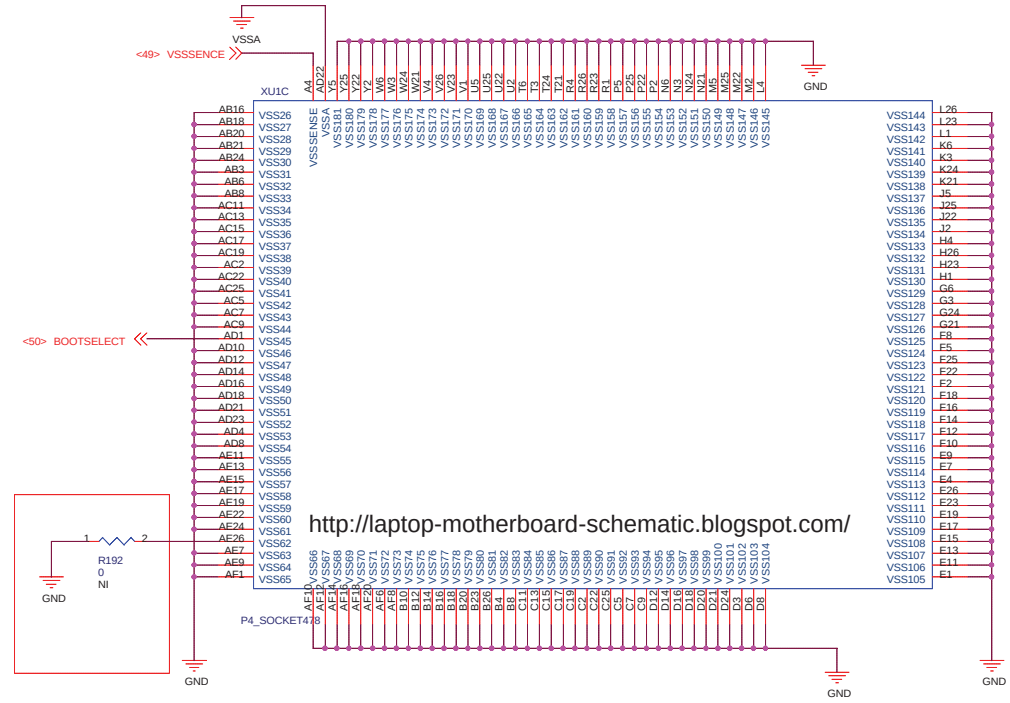
1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRD_OUTEN rises after the voltage across 90% of its specified value

S0: Windows Running +12V,+5V_DUAL,+5V_AUX,+3.3V_SB+3.3V,+3.3V_AUX,+2.5V_DUAL,CPUCORE,+1.5V,+1.5VSB,+1.25V,+1.2V existed
S3: Windows Standby+5V_DUAL,+5V_AUX,+3.3V_SB,+3.3V_AUX,+1.5VSB,+2.5V_DUAL existed
S5: AC Power On Only+5V_AUX,+3.3V_SB,+1.5VSB existed

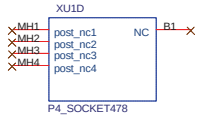
ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 6 of 52	


ICS952621
U23
CLOCK TABLE
FS_B FS_A CPU
0 0 100
0 1 133
1 0 200
1 1 167
L51
30OHM/100MHZ
L49
600OHM/200mA
0603
0805,X5R
4.7U
0.1U
X7R
10K
FS_C
FS_D
FS_E
VDD_REF
VDD_PCI1
VDD_PCI2
VDD3V66
VDD_SRC
VDD_CPU
VDD_48
VDD_A
+3V_CLK
CLKVCC3
HBSEL0
HBSEL1
CK14M_ICH
EXT_AUD_IN
FS_A/REF_1
FS_B/REF_0
VTT_PWRGD#
PWRD#
RST#/PWRDWN#
SMBCLK_M
SMBDATA_M
SCLK
SDATA
IREF
VSS_A
CPU_C0
CPU_T0
CPU_ITPC
CPU_ITPT
CPU_C1
CPU_T1
SRC_C
SRC_T
MCHHCLK#
MCHHCLK
CPUITPHCLK#
CPUITPHCLK
CPUHCLK#
CPUHCLK
ICH_100M#
ICH_100M
PCI0
PCI1
PCI2
PCI3
PCI4
PCI5
PCICLK_ICH
PCICLK_SL1
PCICLK_LAN
PCICLK_FWH
PCICLK_IO
NC_U23_19
FS_C/PCIF0
FS_D/PCIF1
FS_E/PCIF2
3V66_0
3V66_1
3V66_2/MODE
3V66_3/VCH
CK66M_AGP
CK66M_MCH
CK66M_ICH
NC_U23_25
USB48
DOT48
CK48M_ICH
CK48M_VGA
CK14M_ICH
CK14M_IO
OSC_CK14M_XTALIN
OSC_CK14M_XTALOUT
XIN
XOUT
X2
14.31818MHZ
VSS3V66
VSS_CPU
VSS_SRC
VSS_REF
VSS_PCI1
VSS_48
VSS_PCI2
EXT_AUD_IN
VCORE
Q48
PMBS3904
48 PIN IC
DESIGN_NOTE: ICS 952621 / CYPRESS CY28405-2
BOM default is ICS952621
Afetr check with ICS, For CK409 spec :
Max. External Cap = 2 x CL - Cs - Ci
For X'tal Vendor :
07-009021431 XTAL 14.318MHZ DIP 49US TXC 30PF/30PPM
,MARKING:TXC/14.3x8xF QVL:TXC,
CL= 30pf
For ICS95261BF, Ci = 7pf
For trace capacitance , Cs = 2.98pf
Max. External Cap = 2 x 30 - 2.98 - 7 = 50.02pf
47pf still meet sepc.
http://laptop-motherboard-schematic.blogspot.com/
Title : CLOCK409
ASUSTeK COMPUTER INC
Engineer: Jason Lin
Size A3
Project Name Phoenix 2
Rev X01
Date: Tuesday, March 18, 2003
Sheet 7 of 52

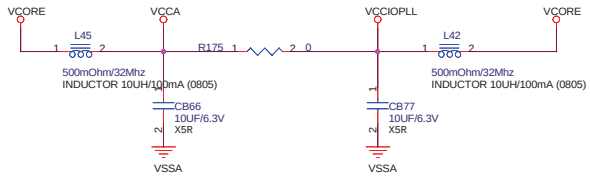

XU1A
XU1B
P4_SOCKET478
DESIGN NOTE:AF3 TIED TO VCCVID FOR PRESCOTT SUPPORT
CAD NOTE: TRCPU/TRCPU# Routing 10/10,use ground guards enclosed
http://laptop-motherboard-schematic.blogspot.com/
CAD NOTE: DATA: SIGNAL(S) ROUTE WITHIN SAME GROUP TO +/-25 MILS AND MUST BE LENGTH MATCHED TO THE STROBE.
ADDRESS: SIGNAL(S) ROUTE WITHIN SAME GROUP TO +/-25 MILS AND MUST BE LENGTH MATCHED TO THE STROBE.
STROBES: A STROBE AND ITS COMPLEMENT SHOULD BE ROUTED TO +/-10 MILS OF THE SAME LENGTH.
DATA,ADDRESS,STROBE AND CLOCK SHOULD BE ROUTED 7MIL WITH A 13MIL SPACING.
CAD NOTE: PLACE AT ICH END OF ROUTE
CAD NOTE:PLACE THESE OUTSIDE CPU SOCKET CAVITY
GTL Reference Voltage
BOM change from 27.4 to 24.9
CLOSE TO CPU PIN #F20 GTLREF
Title : NWD / PRESCOTT - 1
ASUSTeK COMPUTER INC
Engineer: Jason Lin
Project Name
Phoenix 2
Rev
X01
Date: Tuesday, March 18, 2003
Sheet 8 of 52



DESIGN NOTE:AE26 (OPTIMIZED/COMPAT) IS GND ON NORTHWOOD BUT WILL BE DETECT ON POESCOTT

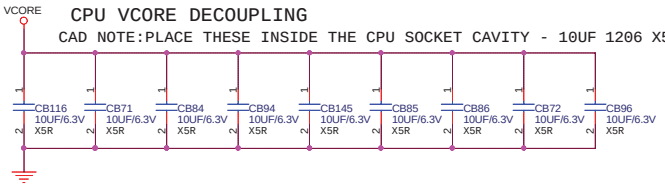


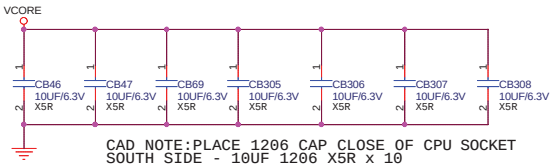
CAD NOTE:PLEASE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET,TRACE ROUTE TO CAP MUST BE NO SMALLER THAN 12MIL



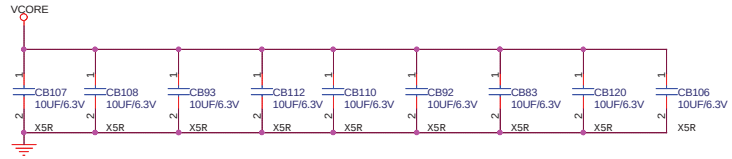
CPU VCORE DECOUPLING

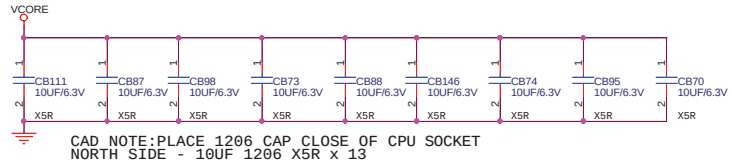
CAD NOTE:PLACE THESE INSIDE THE CPU SOCKET CAVITY - 10UF 1206 X5R x 18





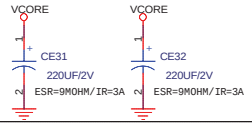
CAD NOTE:PLACE 1206 CAP CLOSE OF CPU SOCKET SOUTH SIDE - 10UF 1206 X5R x 10





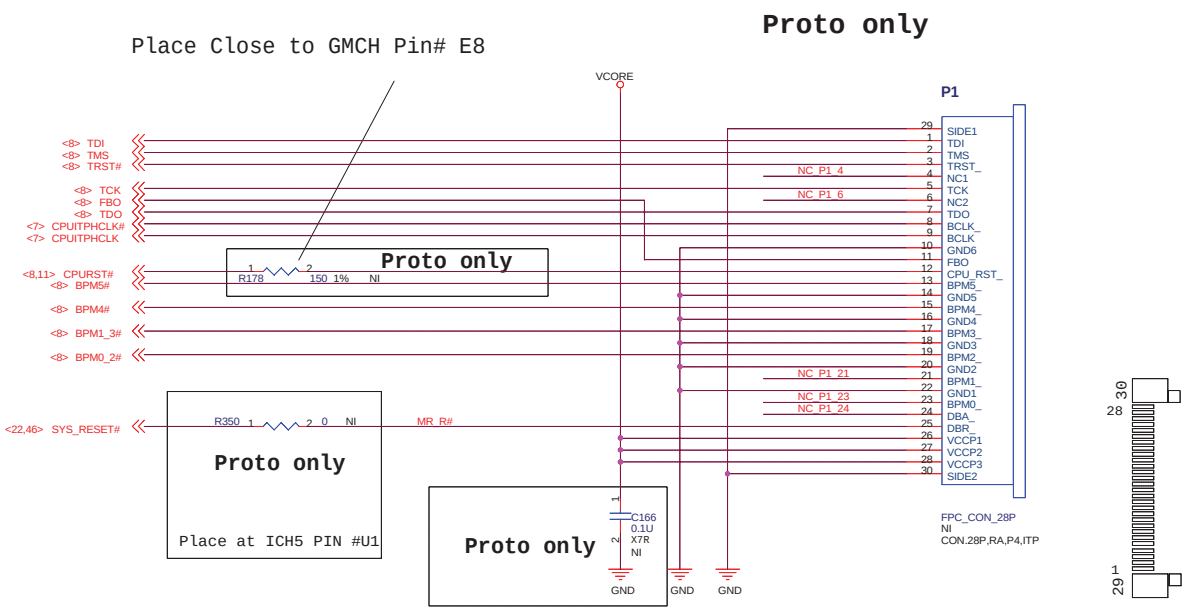
CAD NOTE:PLACE 1206 CAP CLOSE OF CPU SOCKET NORTH SIDE - 10UF 1206 X5R x 13

CHIP CAP



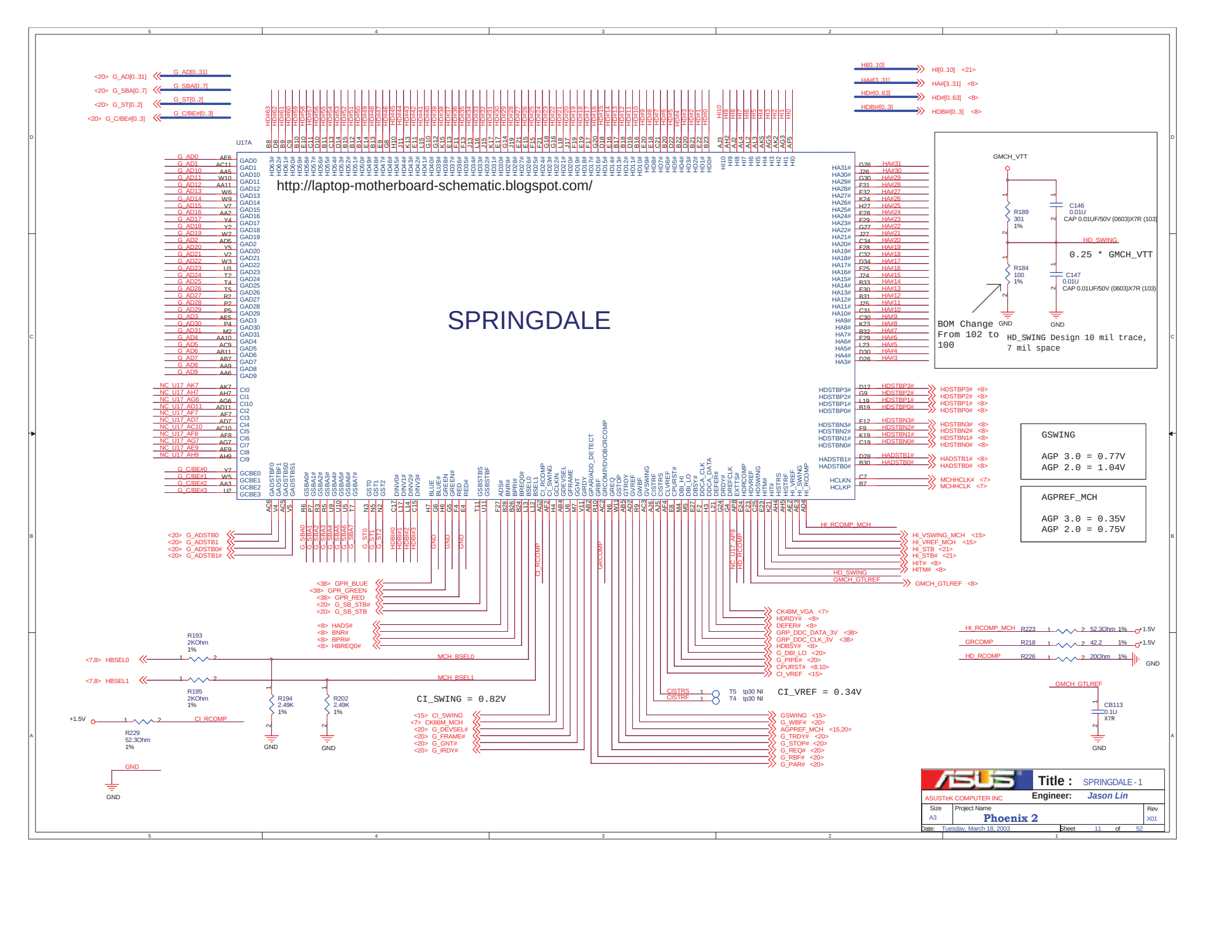
ASUSTeK COMPUTER INC	Title : NWD / PRESCOTT - 2	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoneix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 9 of 52	

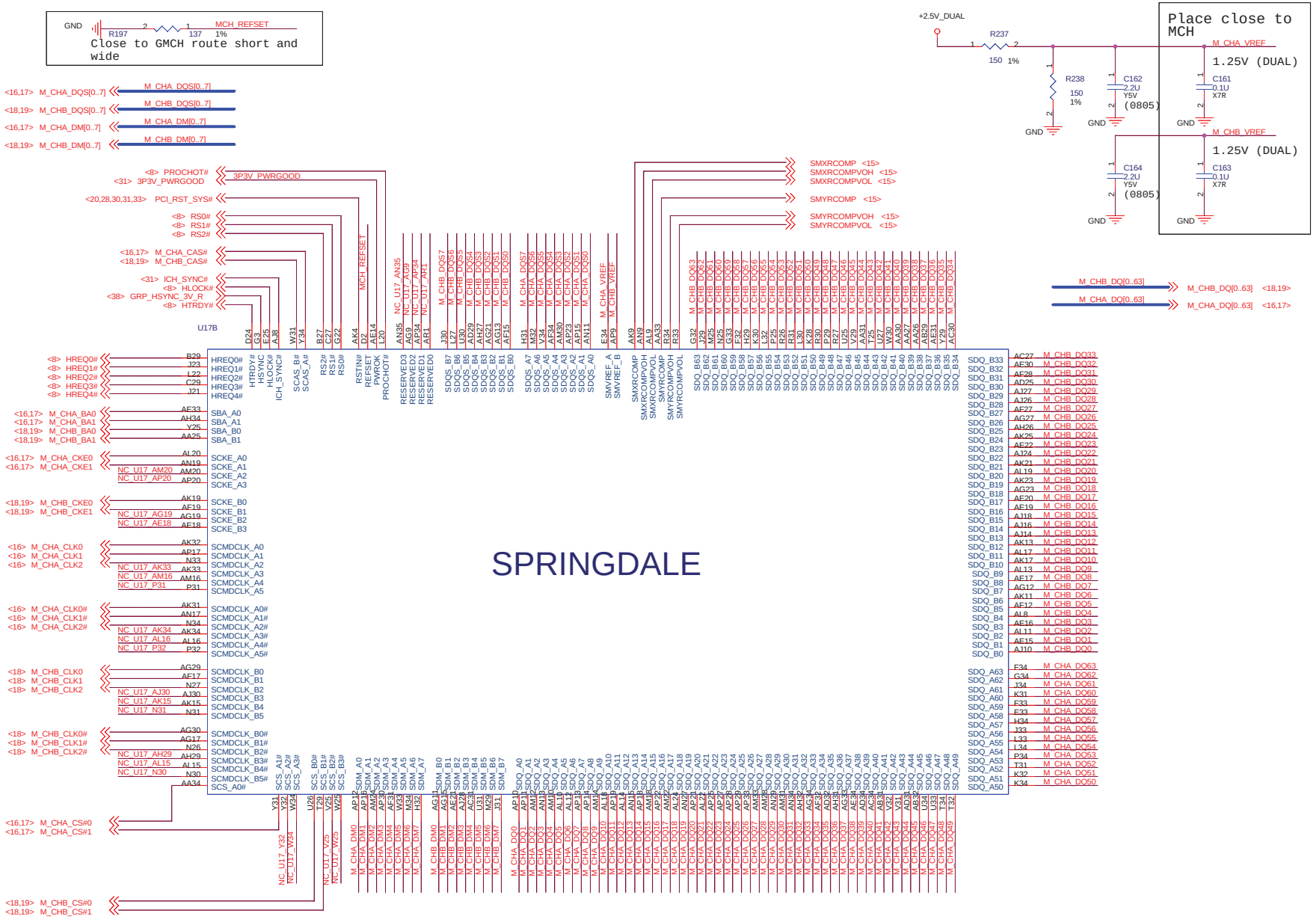
PROCESSOR ITP RIGHT-ANGLE,SURFACE MOUNT ITP CONNECTOR



http://laptop-motherboard-schematic.blogspot.com/

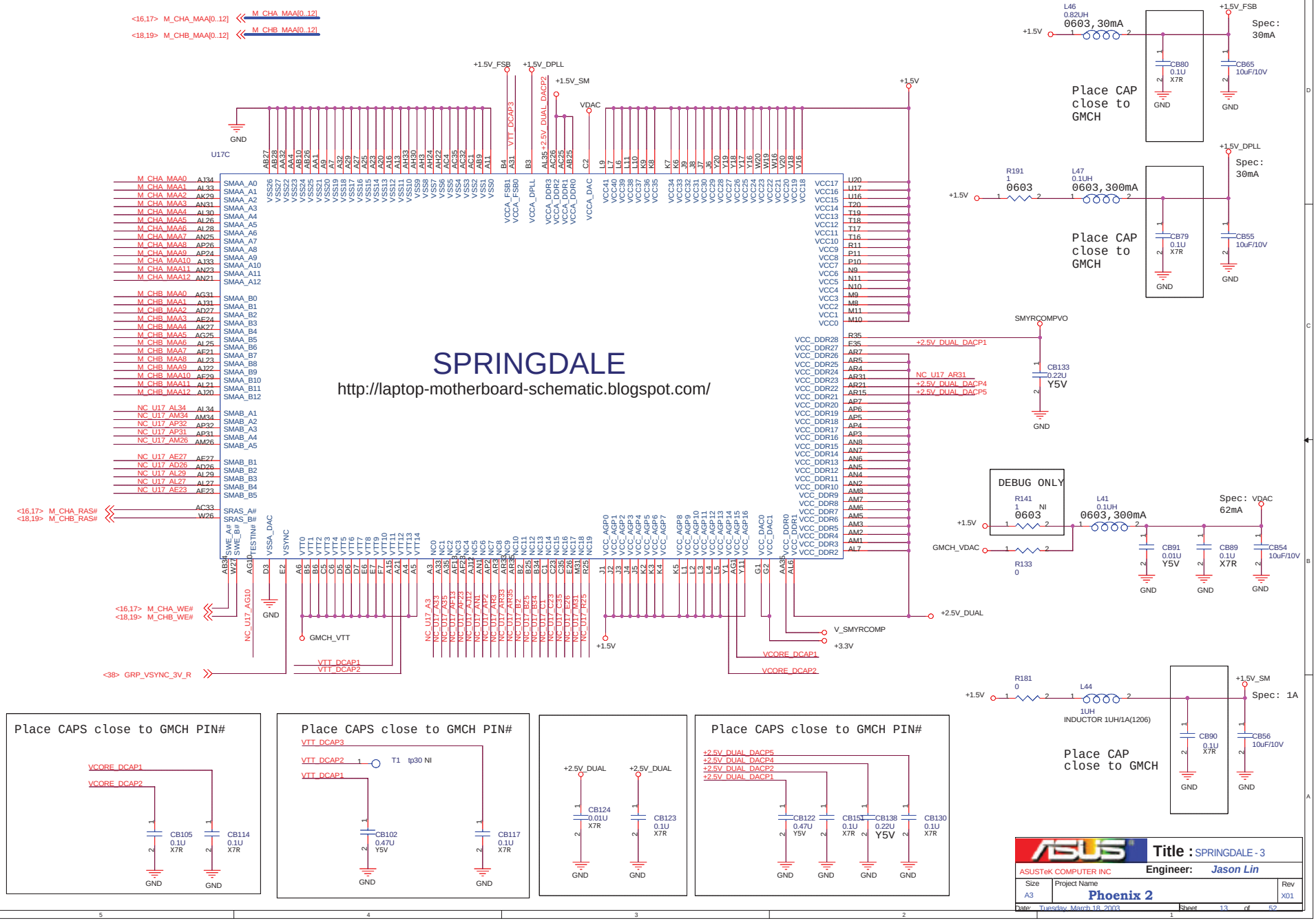
ASUSTeK COMPUTER INC	Title : ITP Port	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 10 of 52	

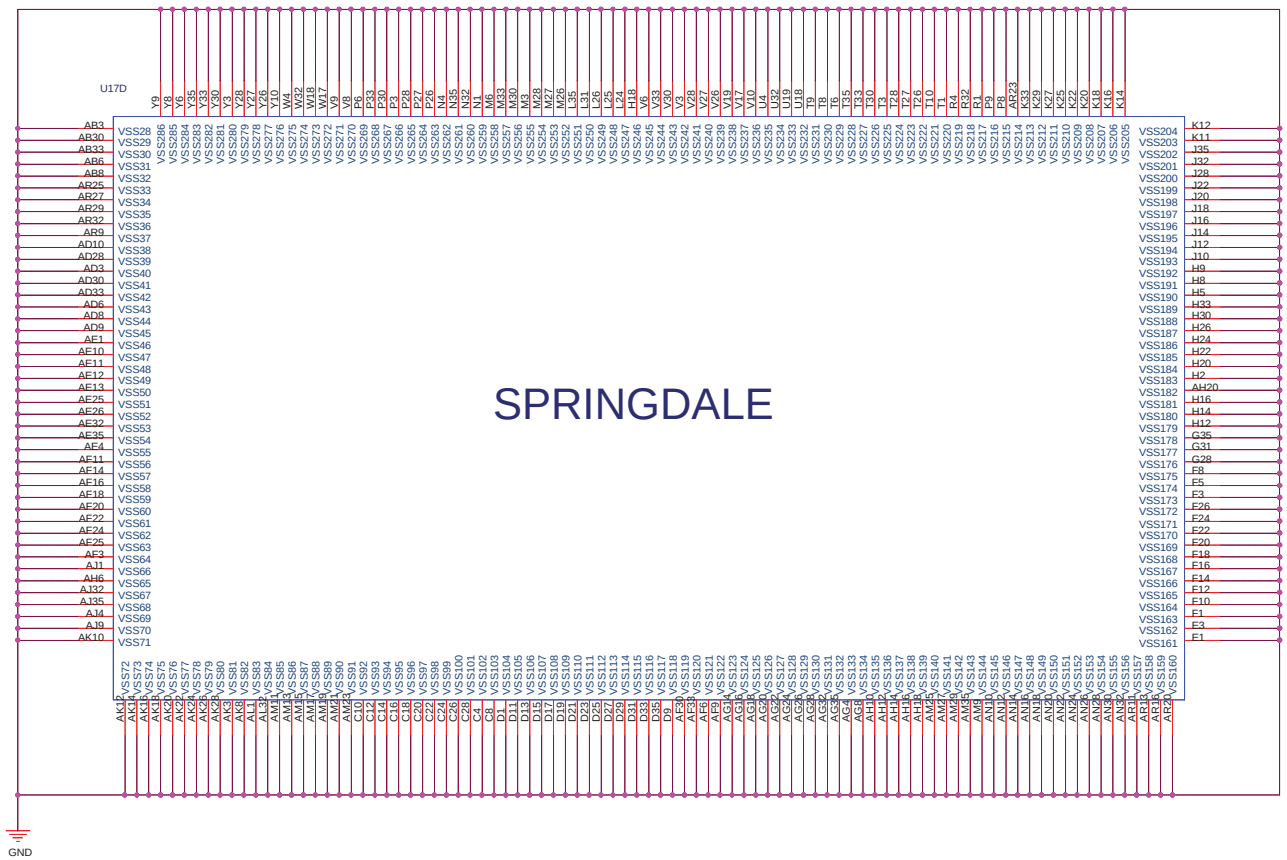

SPRINGDALE
http://laptop-motherboard-schematic.blogspot.com/
U17A
GMCH_VTT
R189 301 1%
R184 100 1%
C146 0.01U CAP 0.01UF/50V (0603)X7R (103)
C147 0.01U CAP 0.01UF/50V (0603)X7R (103)
HD_SWING
0.25 * GMCH_VTT
GND
BOM Change From 102 to 100
HD_SWING Design 10 mil trace, 7 mil space
GSWING
AGP 3.0 = 0.77V
AGP 2.0 = 1.04V
AGPREF_MCH
AGP 3.0 = 0.35V
AGP 2.0 = 0.75V
R193 2KOhm 1%
R195 2KOhm 1%
R194 2.49K 1%
R202 2.49K 1%
R229 52.3Ohm 1%
MCH_BSEL0
MCH_BSEL1
CI_SWING = 0.82V
CI_VREF = 0.34V
R223 52.3Ohm 1%
R218 42.2 1%
R226 20Ohm 1%
CB113 0.1U X7R
ASUSTeK COMPUTER INC
Title : SPRINGDALE - 1
Engineer: Jason Lin
Size A3
Project Name Phoenix 2
Rev X01
Date: Tuesday, March 18, 2003
Sheet 11 of 52

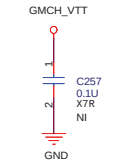


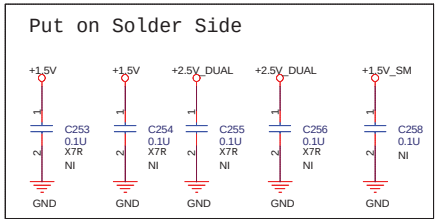
SPRINGDALE

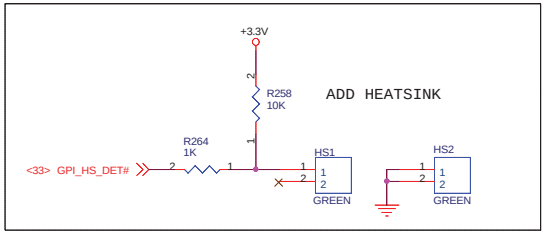
http://laptop-motherboard-schematic.blogspot.com/

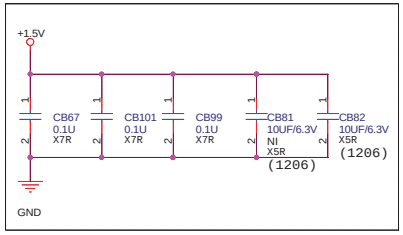


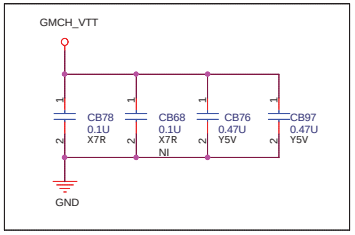


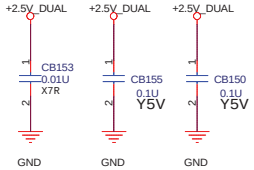












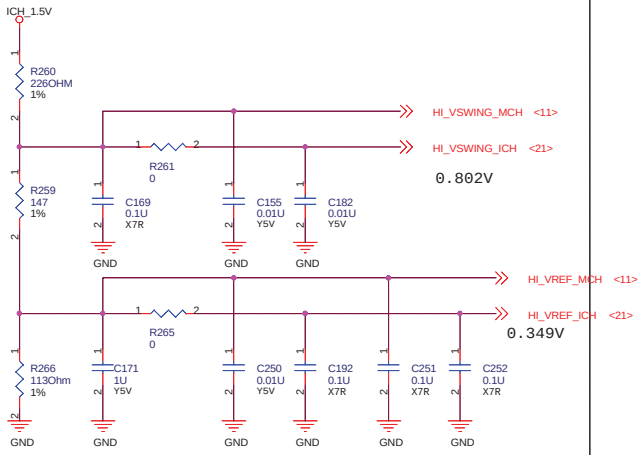
ASUSTeK COMPUTER INC

Title : SPRINGDALE - 4

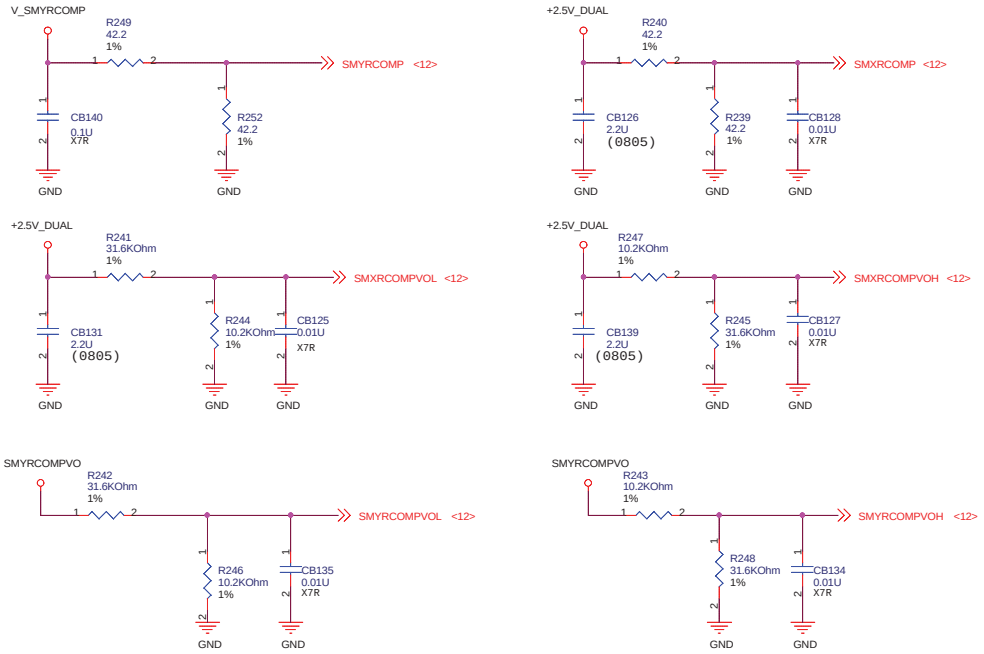
Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoneix 2	X01

Date: Tuesday, March 18, 2003 Sheet 14 of 52

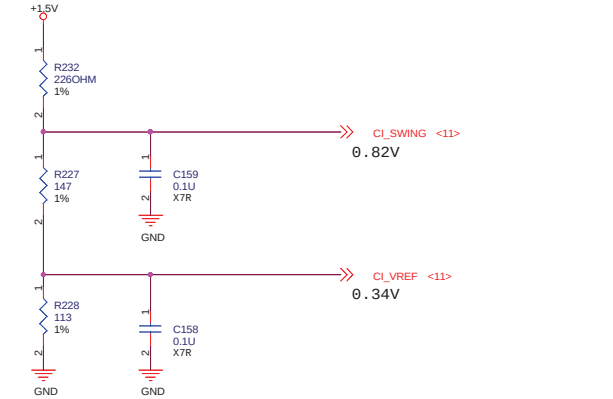


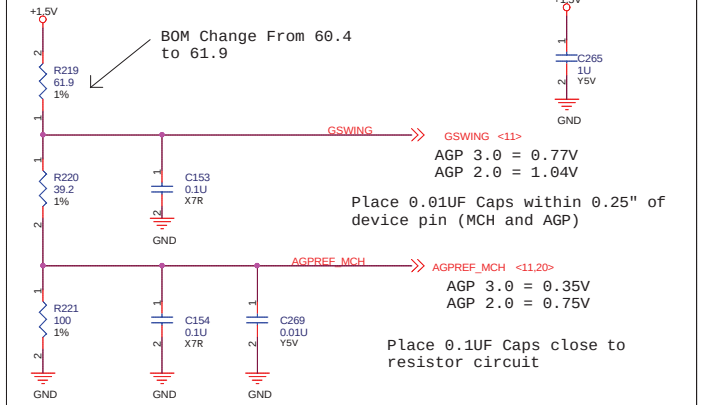
Resistor divider plus 1 Cap placed at midpoint of bus.
Two other Caps plaecd at MCH and ICH.
Use 10 mil trace, 7 mil space



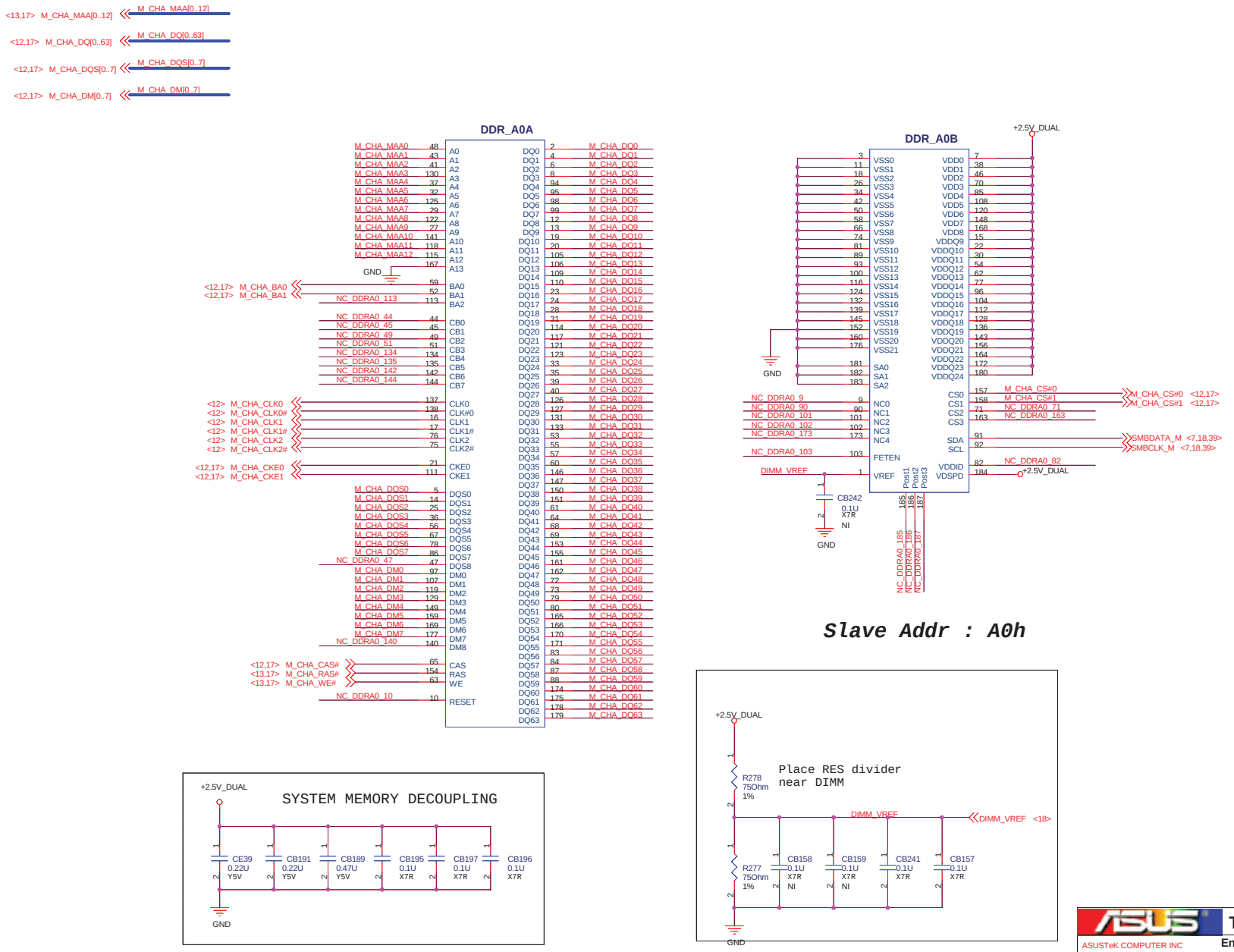
Bas on formula from v1.3 Spec is DDR RCOMP VOL = VCC_DDR*(1/4.112) +/-2% = 0.6323V
DDR RCOMP VOH = VCC_DDR*(3.112/4.112) +/-2% = 1.9677V

The 10K/30.1K will get 0.6484V and 1.9516V, but 10.2K/31.6K will get better value 0.6344V and 1.9655V.





ASUSTeK COMPUTER INC	Title : SPRINGDALE - 5	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 15 of 52	



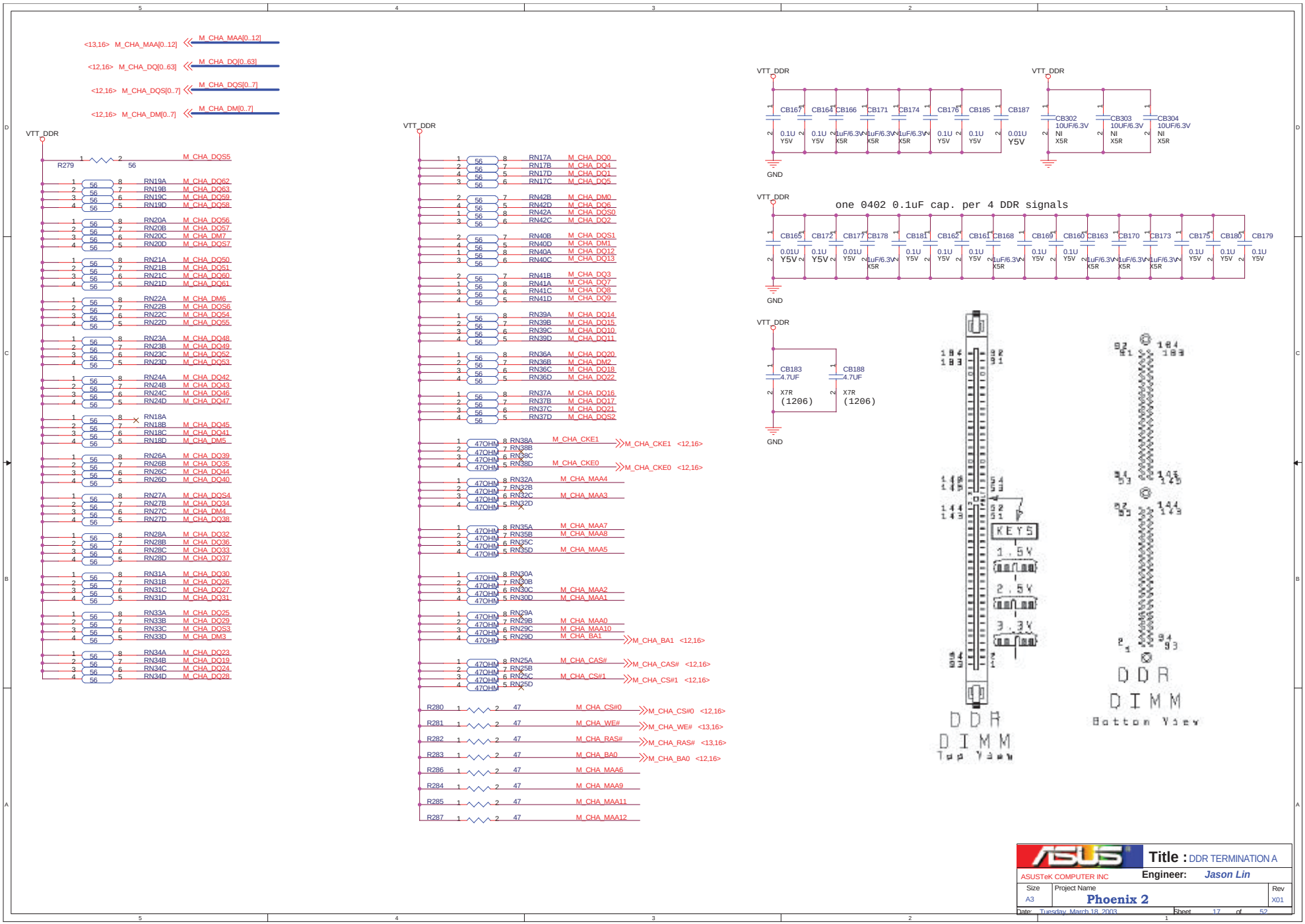
Title : DDR CHANNEL A

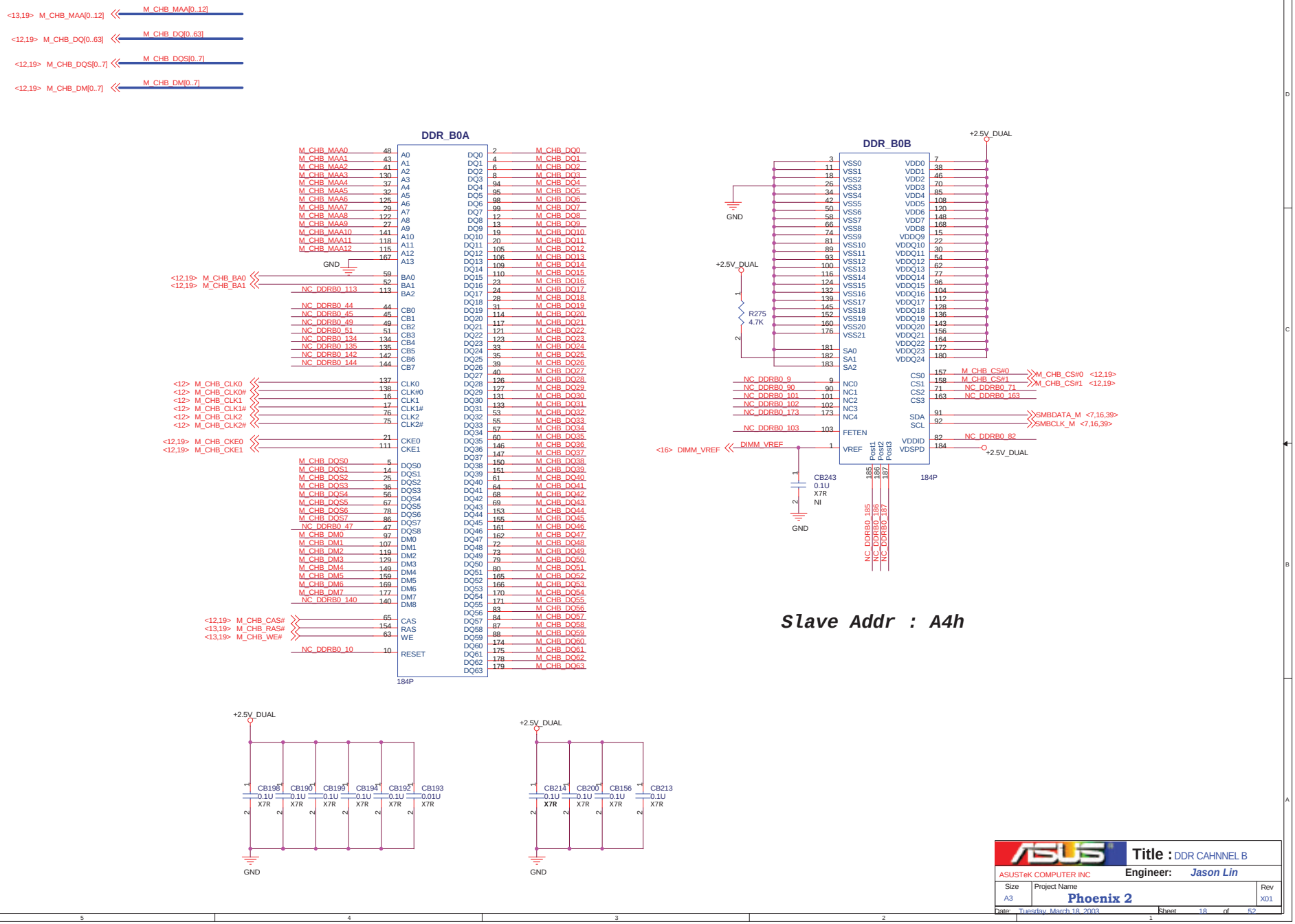
ASUSTeK COMPUTER INC

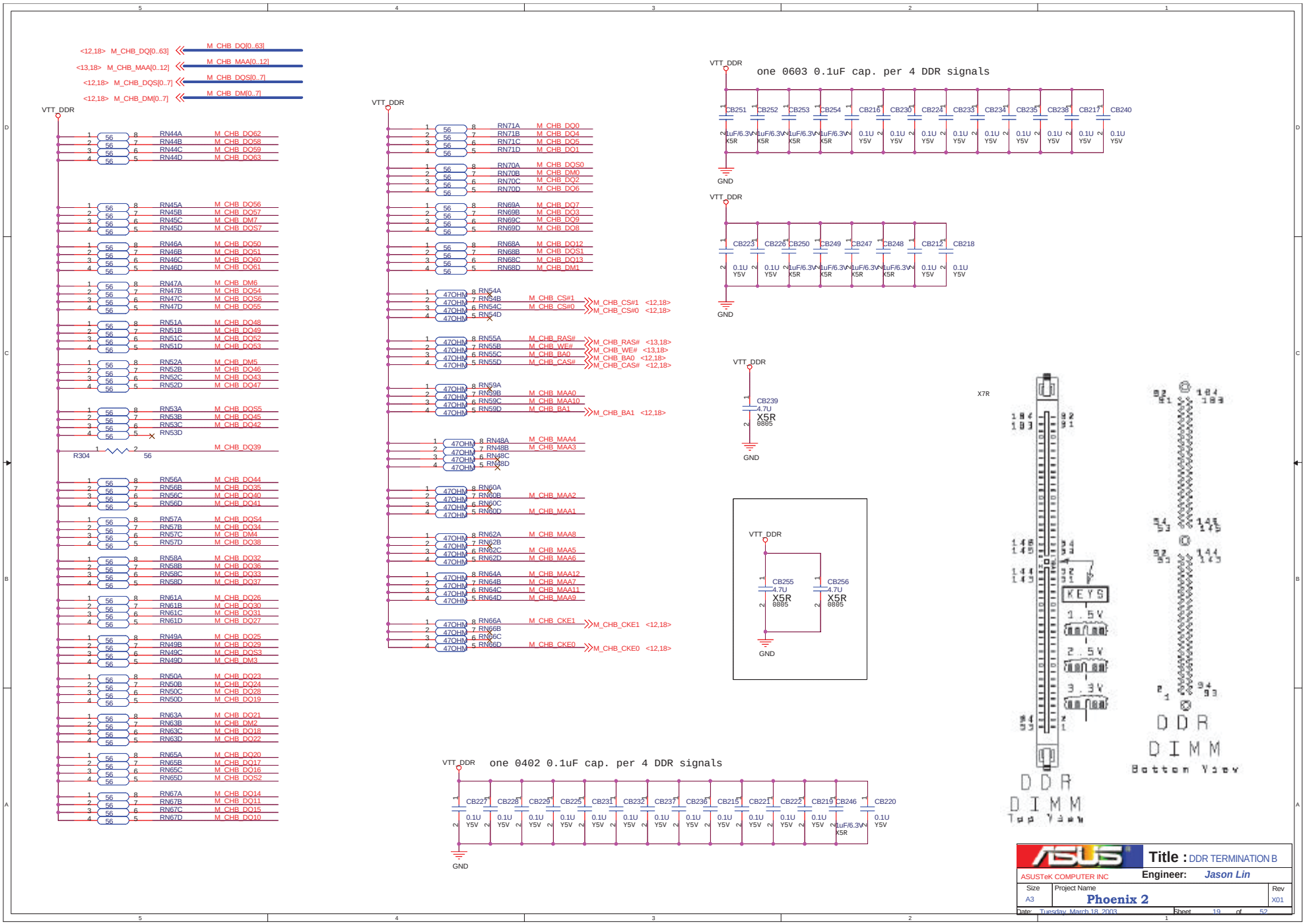
Engineer: Jason Lin

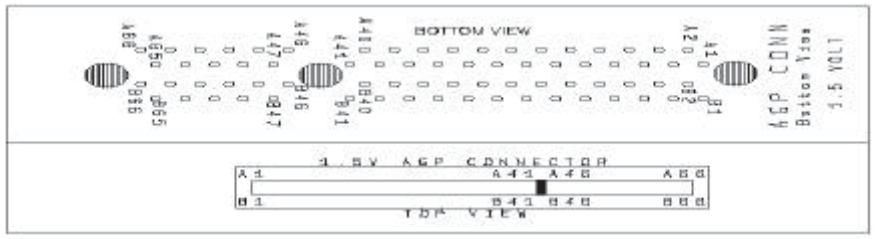
Size	Project Name	Rev
A3	Phoenix	X01

Date: Tuesday, March 18, 2003 Sheet 16 of 52







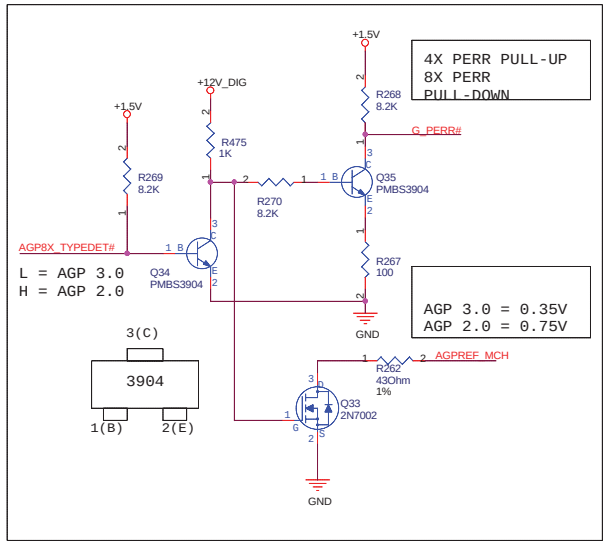


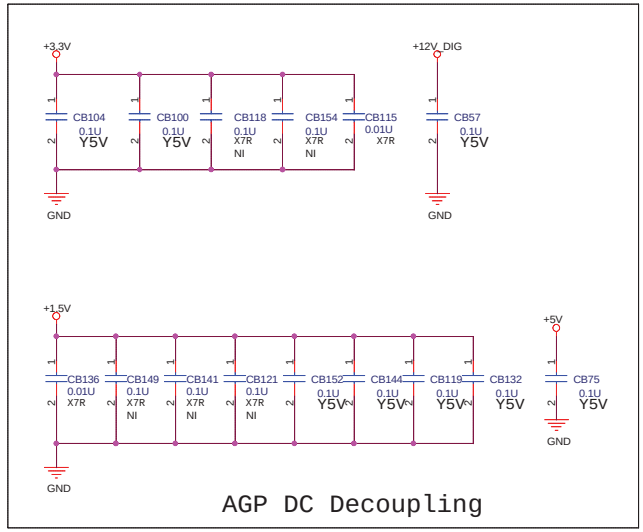
AGP8X_TYPEDET#

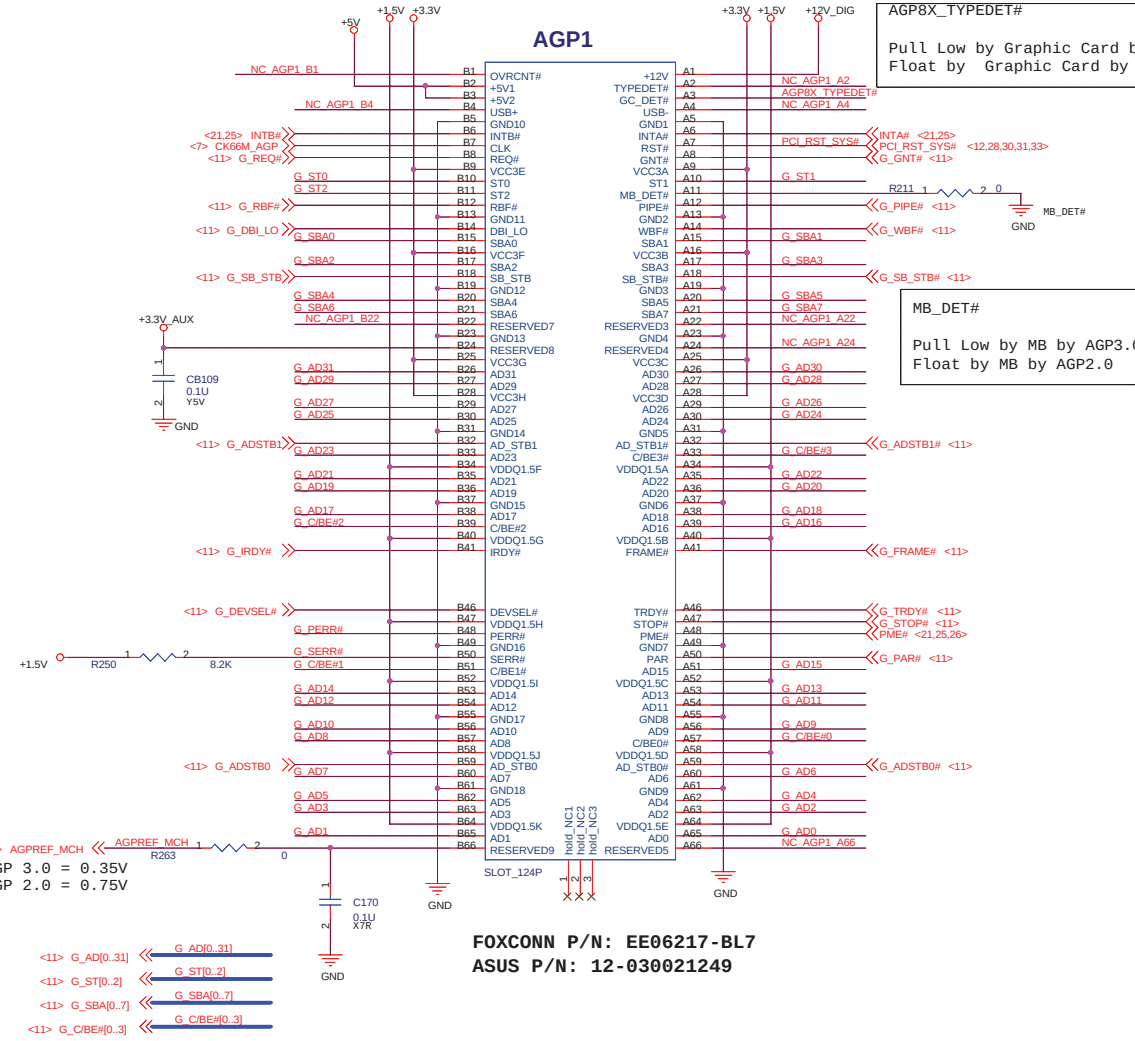
Pull Low by Graphic Card by AGP3.0
Float by Graphic Card by AGP2.0

MB_DET#

Pull Low by MB by AGP3.0
Float by MB by AGP2.0

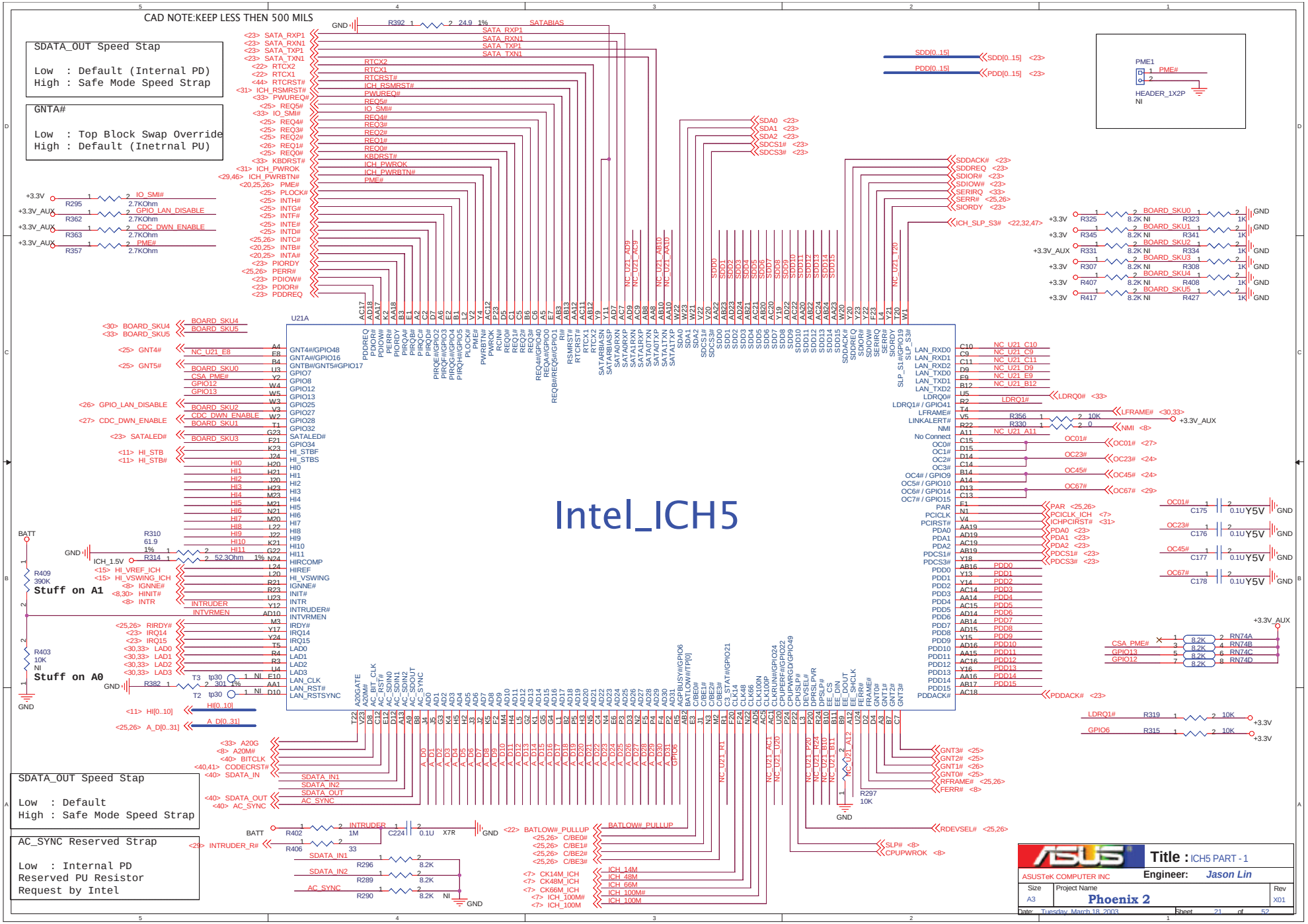


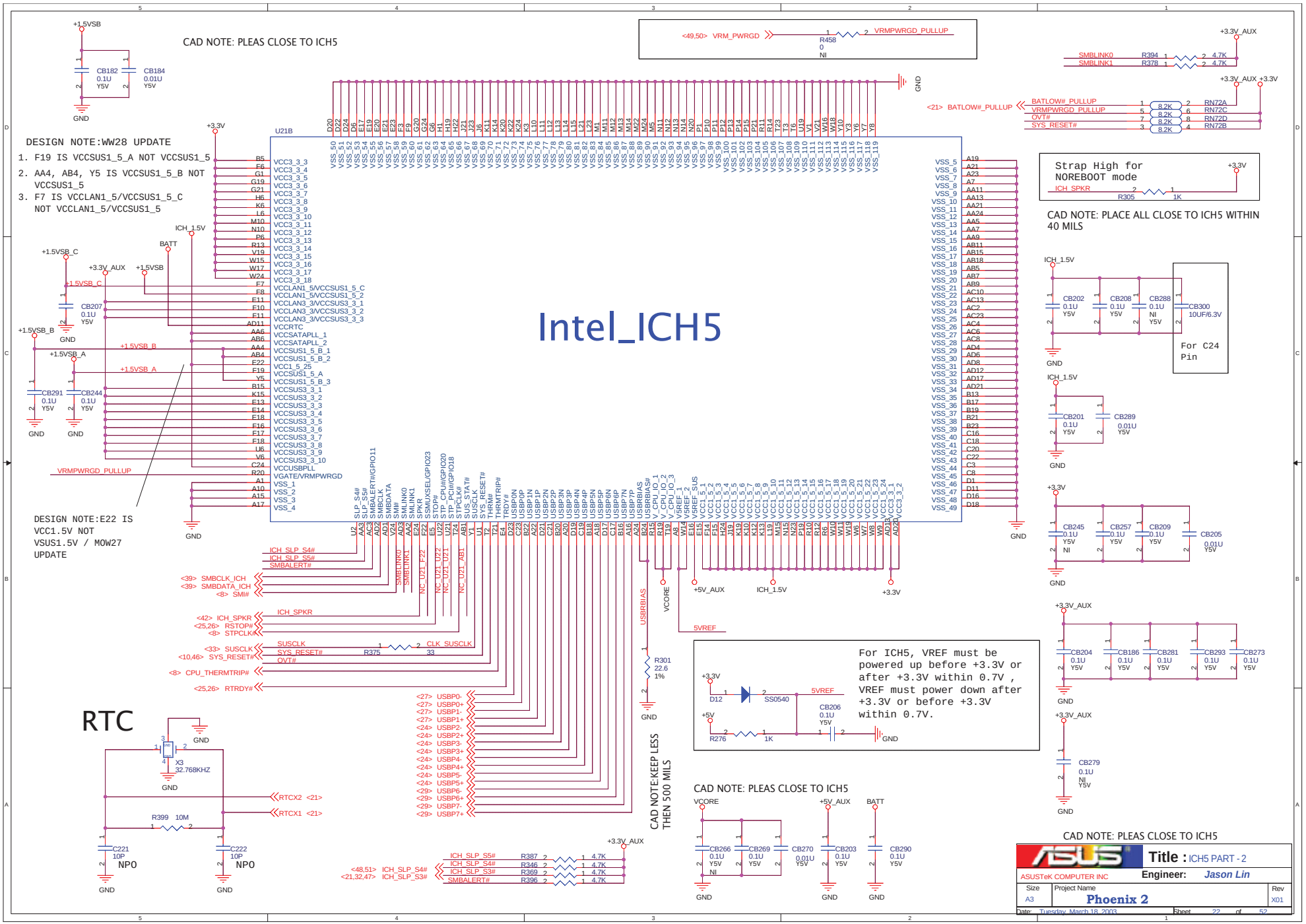




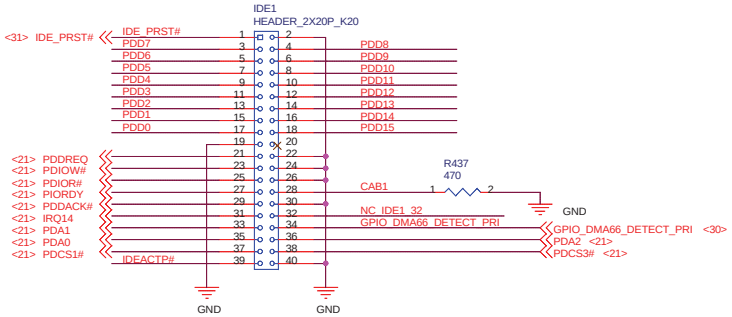
FOXCONN P/N: EE06217-BL7
ASUS P/N: 12-030021249

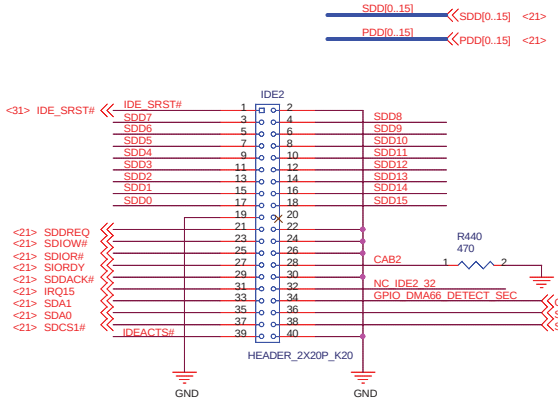
ASUSTeK COMPUTER INC	Title : AGP 8X CONNECTOR	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 20 of 52	

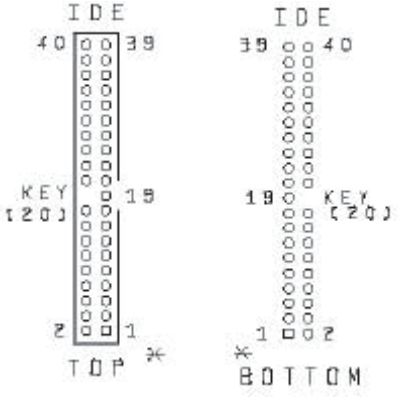


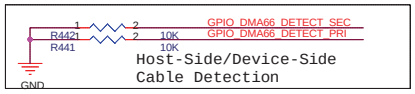


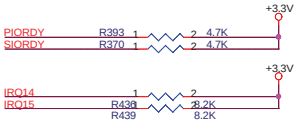
Parallel ATA



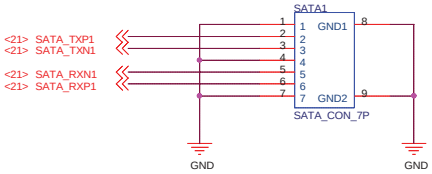


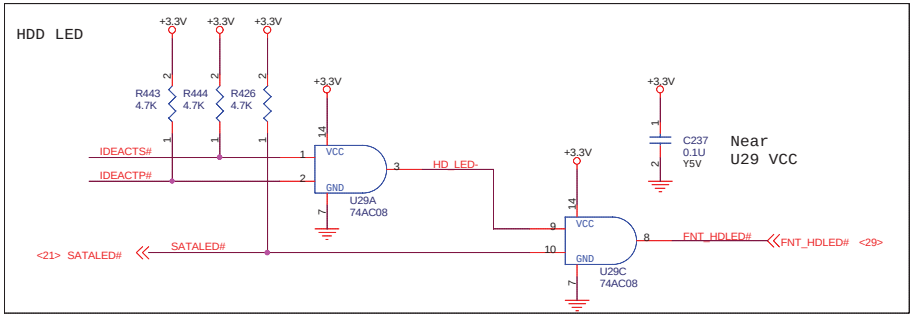


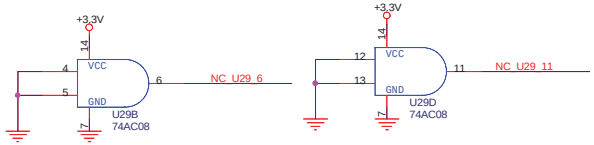




Serial ATA

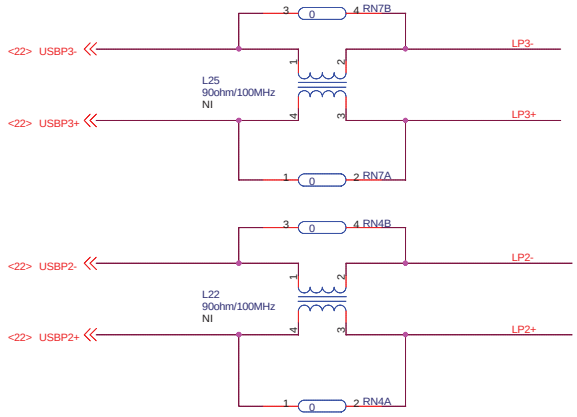




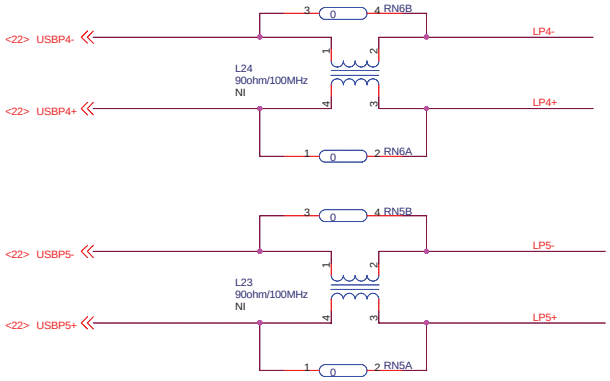


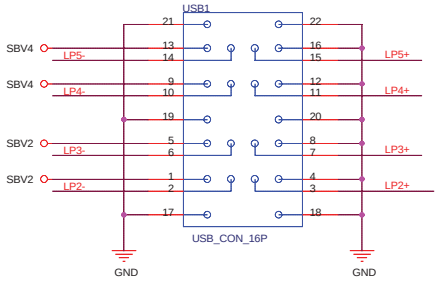
ASUSTeK COMPUTER INC	Title : IDE CONNECTOR	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 23 of 52	

Dual USB CONNECTOR Port 2 & 3



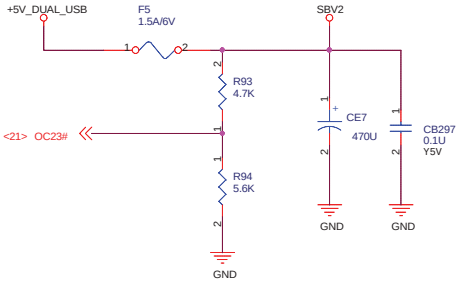
Dual USB CONNECTOR Port 4 & 5





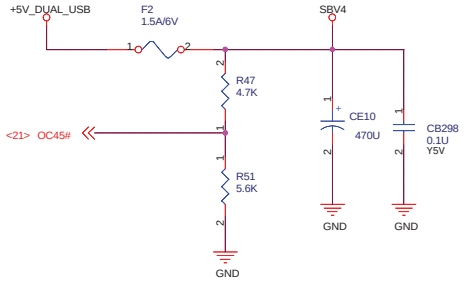
DELL Spec :

USB Wake-Up support S0/S1/S3

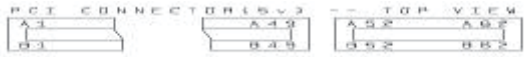


DELL Spec :

USB Wake-Up support S0/S1/S3

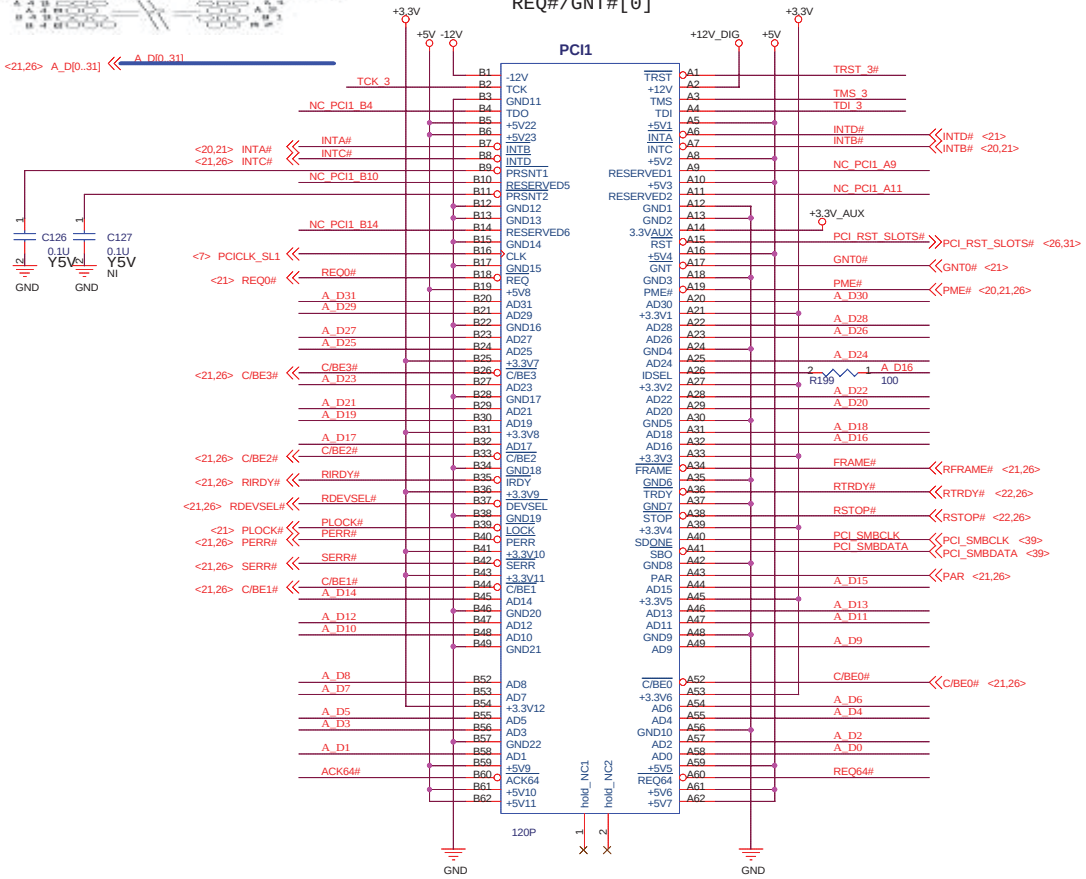


ASUSTeK COMPUTER INC	Title : USB2.0 CONNECTORS	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoneix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 24 of 52	

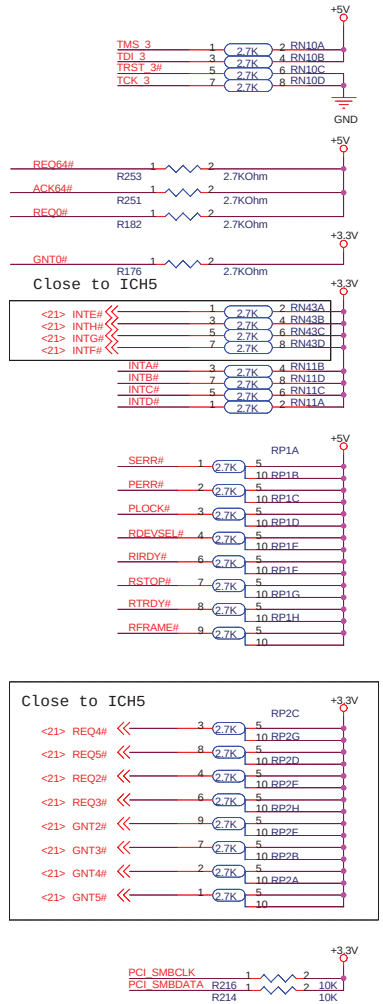


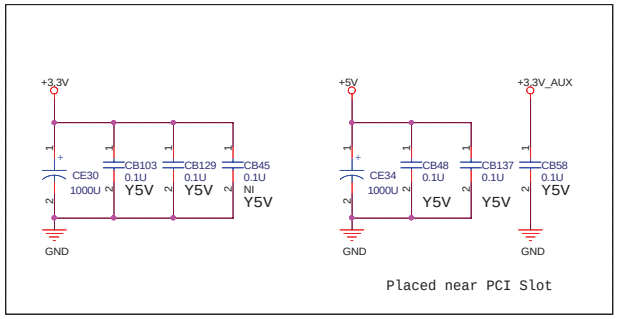
PCI SLOT

Device#:00h
INT#[D,A,B,C]
REQ#/GNT#[0]



PCI BUS RESTSTORS





CAD NOTE: PCI trace width / space = 5/7 , the ICH5 to 1st PCI length = 4" to 10" , 1st to 2rd PCI length = 1" , 2rd to 3th PCI length = 1".

PCI DEVICE	PCI REQ/GNT	PCI IDSEL	PCI Clocks	INTA on device mapped to INTx	Device Number
PCI SLOT 1	REQ/GNT 0	A_D16	PCICLK_SL1	INT DABC	0

ASUSTeK COMPUTER INC

Title : PCI SLOT 3

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

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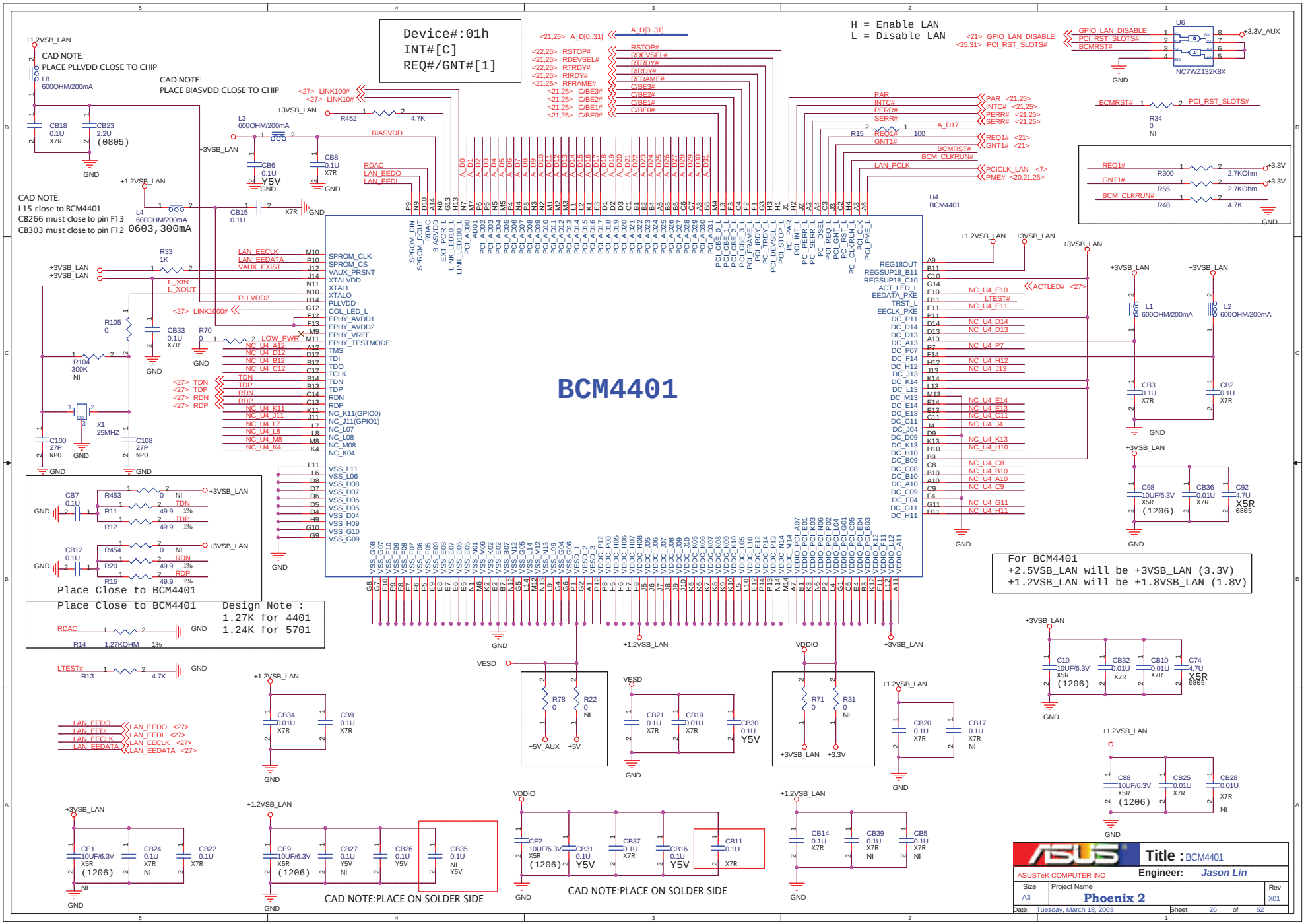
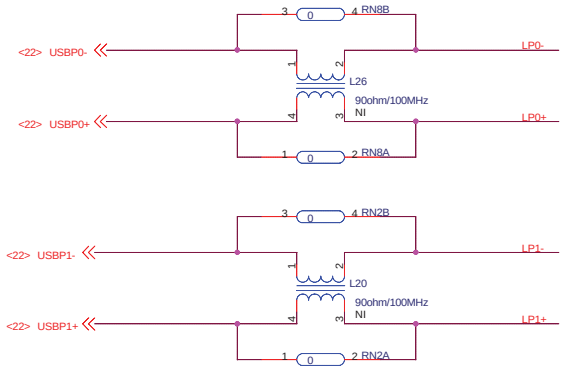


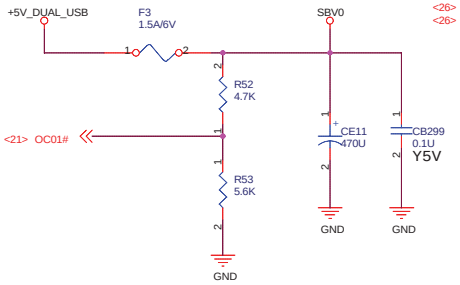


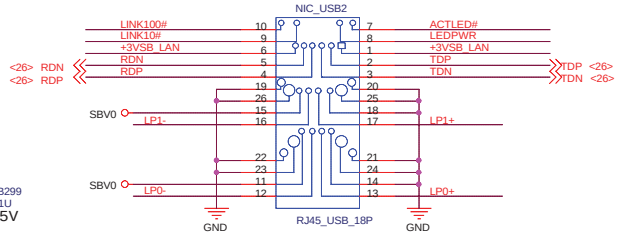
DELL Spec :

USB Wake-Up support S0/S1/S3

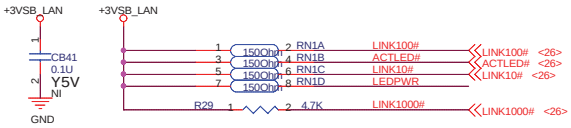
Speed LED (Dual Color LED)
Pin 9 + , Pin 10 - : Orange = 100Mbit
Pin 9 - , Pin 10 + : Green = 10Mbit

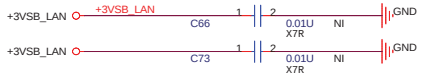
Active LED (Yellow)
Pin 7 -
Pin 8 +

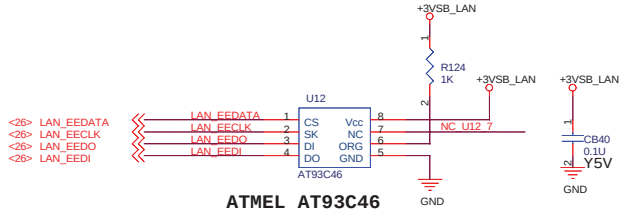




RJ45 + USB Combo
Include 10/100 Transformer

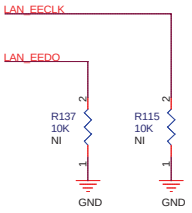






ATMEL AT93C46

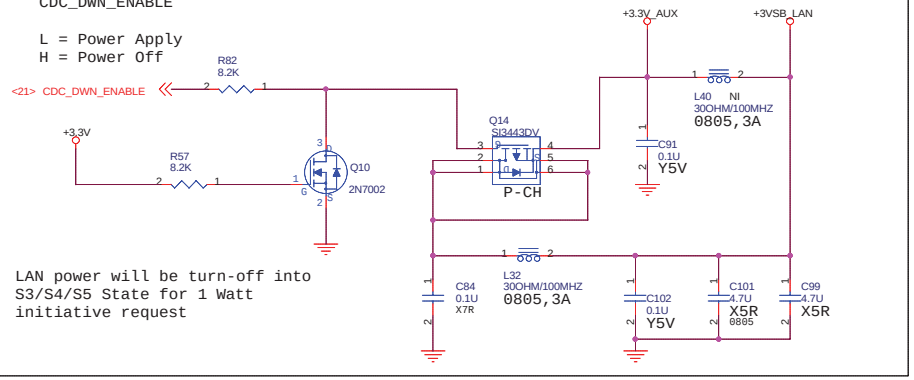
For BCM4401 SPROM SIZE



SPROM SIZE	R52	R50
1K	X	X
4K	X	V
16K	V	X

CDC_DWN_ENABLE

L = Power Apply
H = Power Off



LAN power will be turn-off into
S3/S4/S5 State for 1 Watt
initiative request

ASUSTeK COMPUTER INC

Title : RJ45 + USB + EEPROM

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

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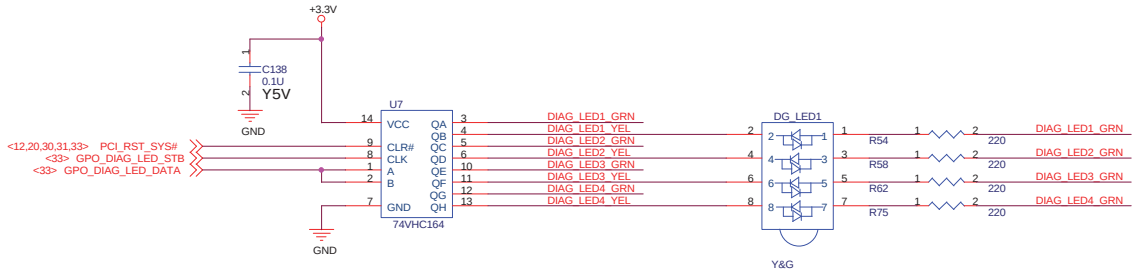


<Core Design>

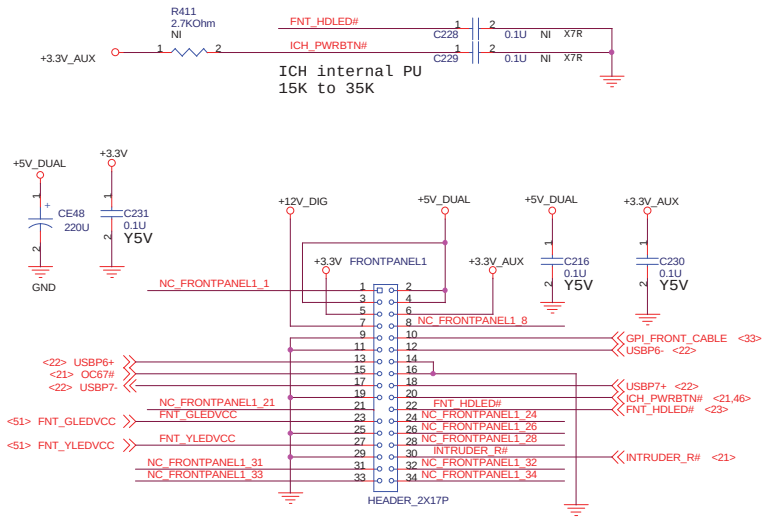
ASUStek Computer Inc.

Title : DIAGLED

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 28 of 52



<Core Design>

ASUStek Computer Inc.

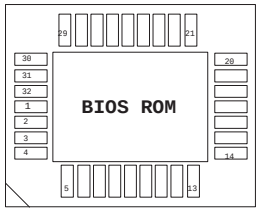
Title : Front Pannel

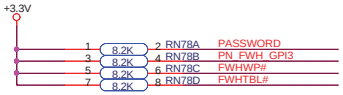
Engineer: Jason Lin

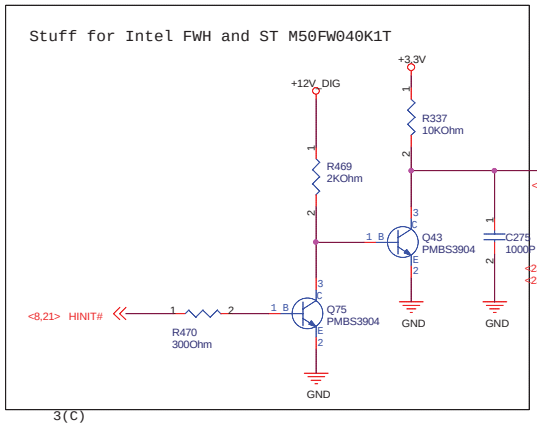
Size	Project Name	Rev
A3	Phoenix 2	X01

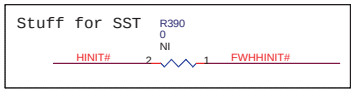
Date: Tuesday, March 18, 2003 Sheet 29 of 52

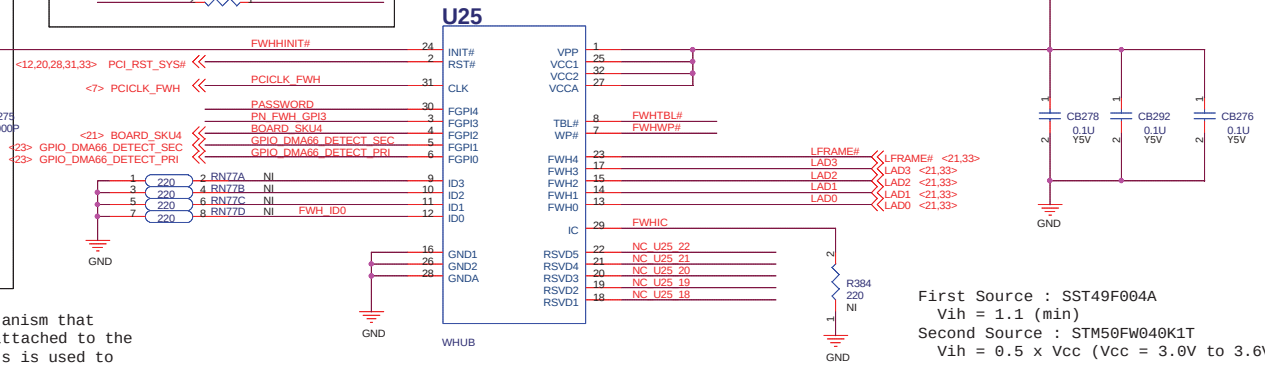
FWH BIOS ROM

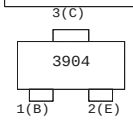






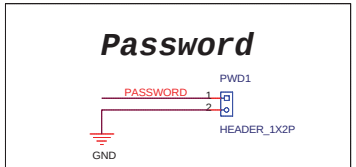


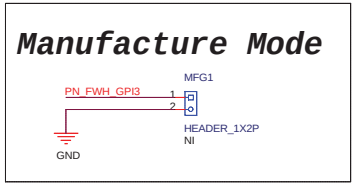




These four pins are part of the mechanism that allows Inputs multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0] = 0000 and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KW

First Source : SST49F004A
  Vih = 1.1 (min)
Second Source : STM50FW040K1T
  Vih = 0.5 x Vcc (Vcc = 3.0V to 3.6V)

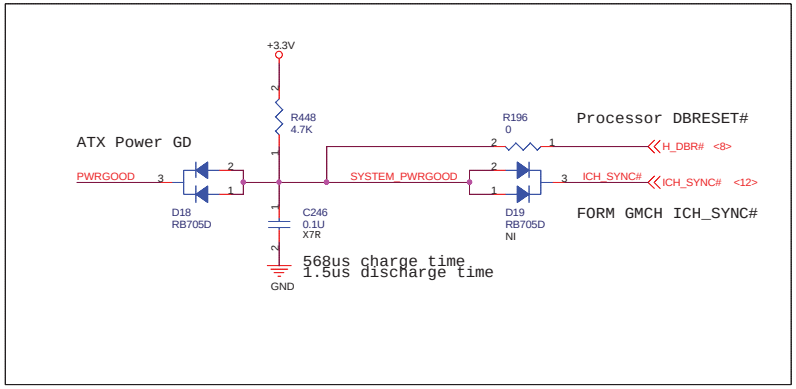


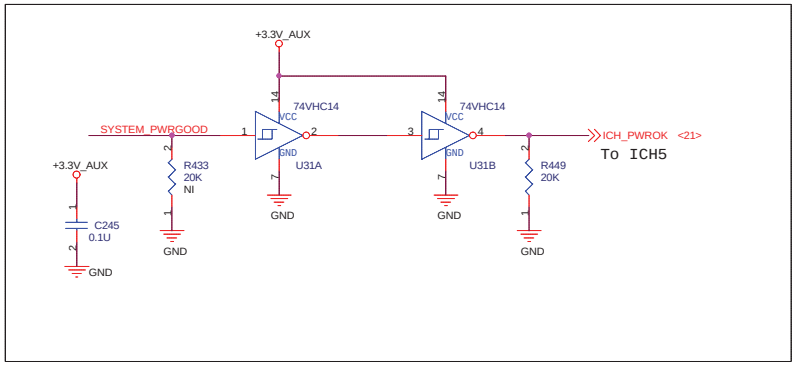


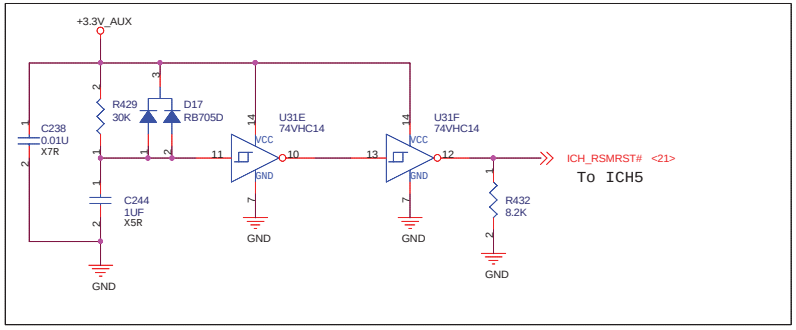
IC (Interface Configuration Pin) :
    This pin determines which interface is operational. When Configuration Pin held high, programmer mode is enabled and when held low, FWH mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation it cannot be left unconnected.

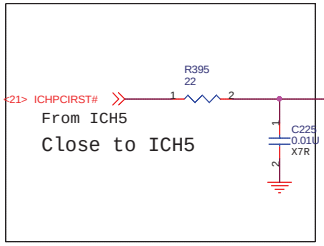
DESIGN NOTE:LEVEL SHIFTING FOR INIT# TO FWH (FOR INTEL FWH ONLY)

ASUSTeK COMPUTER INC	Title : FWH BIOS ROM	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 30 of 52	

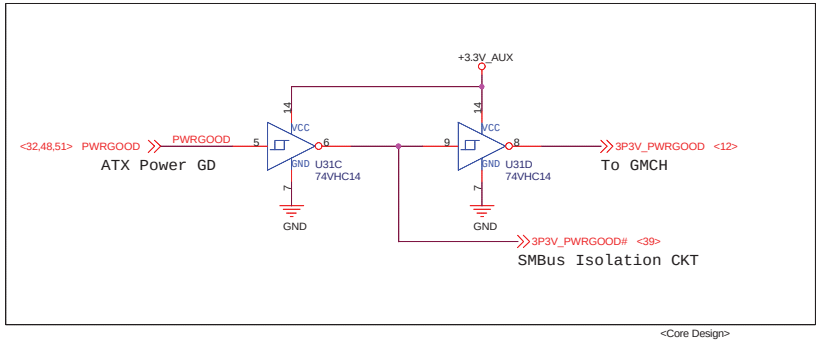






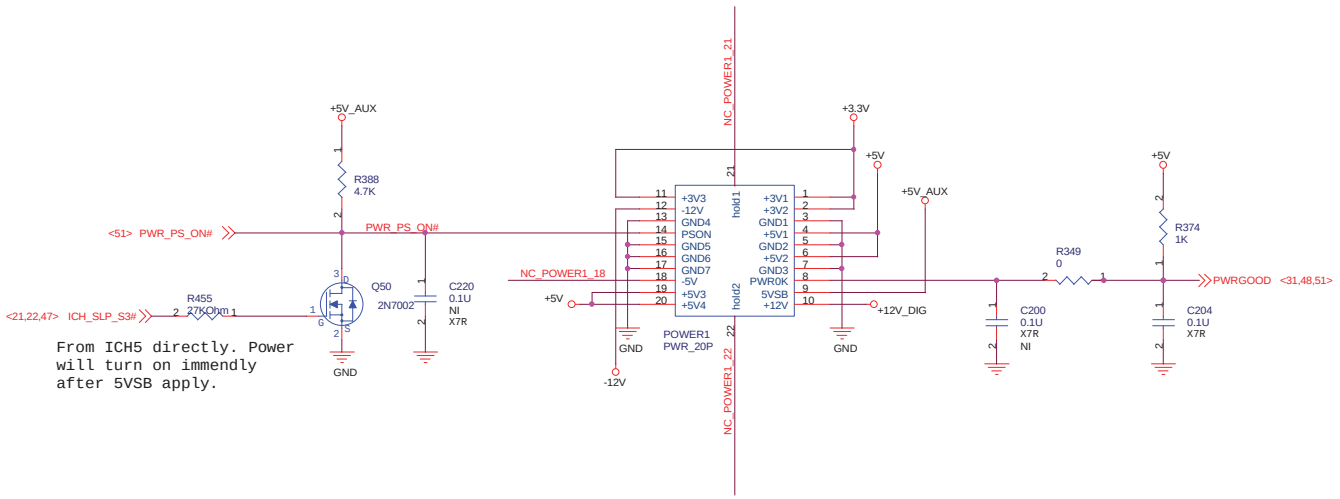


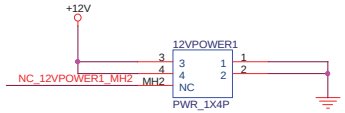
74AC08	VCC (V)	TA = +25°C			TA = 40°C to +85°C		
Symbol Parameter		Min	Typ	Max	Min	Max	
tPLH Propagation Delay	3.3	1.5	7.5	9.5	1.0	10.0	ns
	5.0	1.5	5.5	7.5	1.0	8.5	
tPHL Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
	5.0	1.5	5.5	7.0	1.0	7.5	

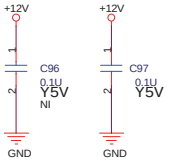


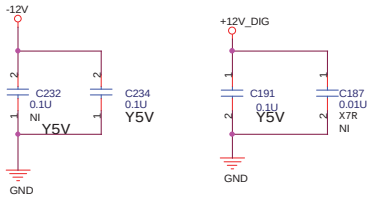
<Core Design>

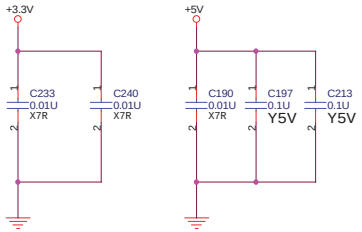
ASUSTek Computer Inc.	Title : POWER GOOD& RESET	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 31 of 52	

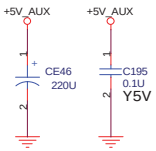


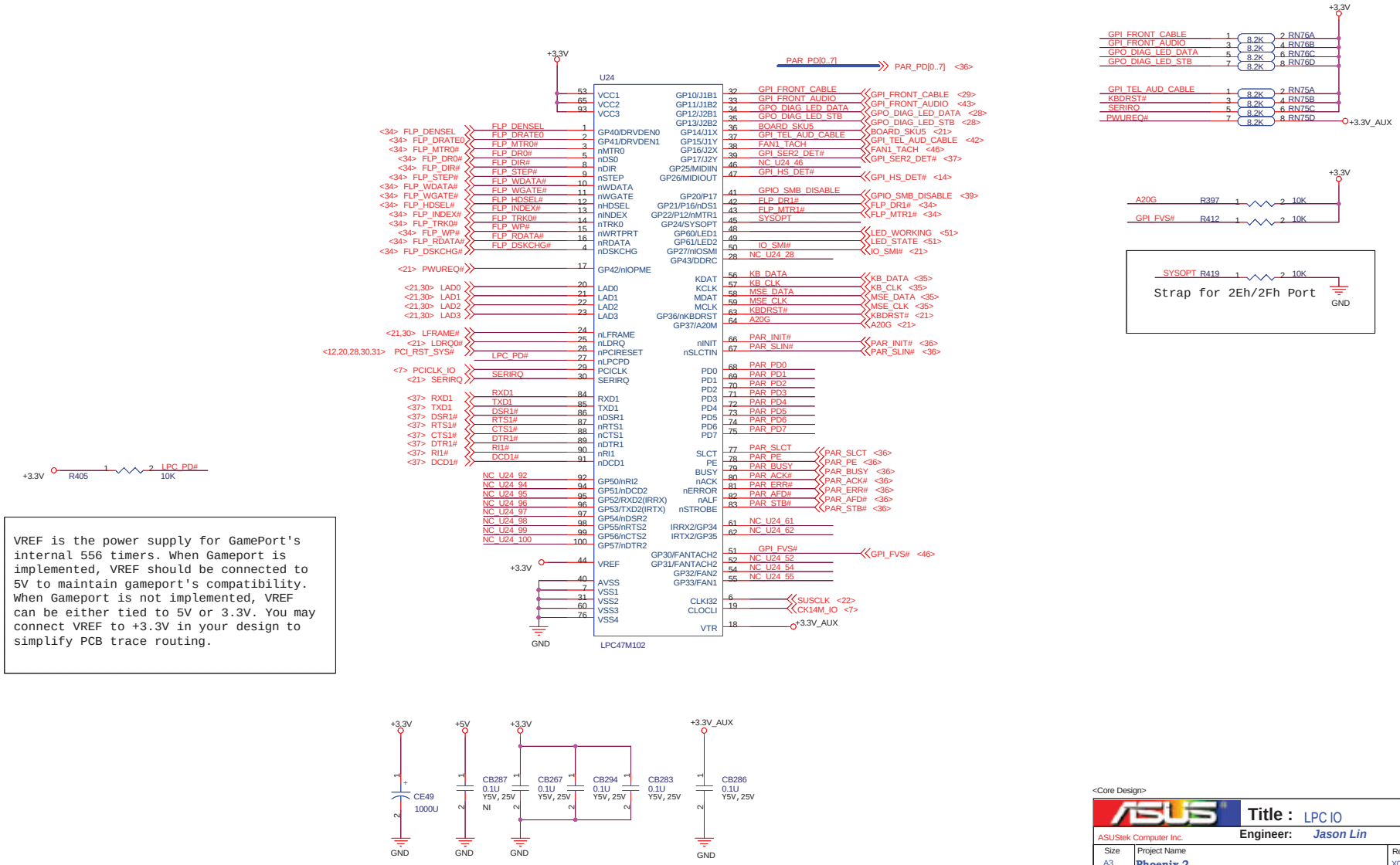












VREF is the power supply for GamePort's internal 556 timers. When Gameport is implemented, VREF should be connected to 5V to maintain gameport's compatibility. When Gameport is not implemented, VREF can be either tied to 5V or 3.3V. You may connect VREF to +3.3V in your design to simplify PCB trace routing.

<Core Design>

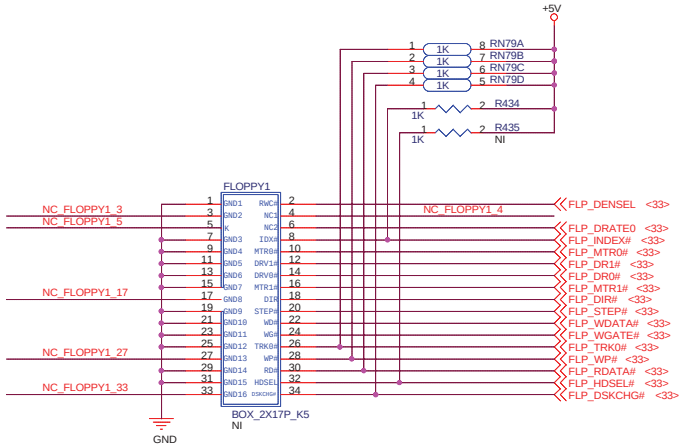
ASUSTek Computer Inc.

Title : LPC IO

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 33 of 52



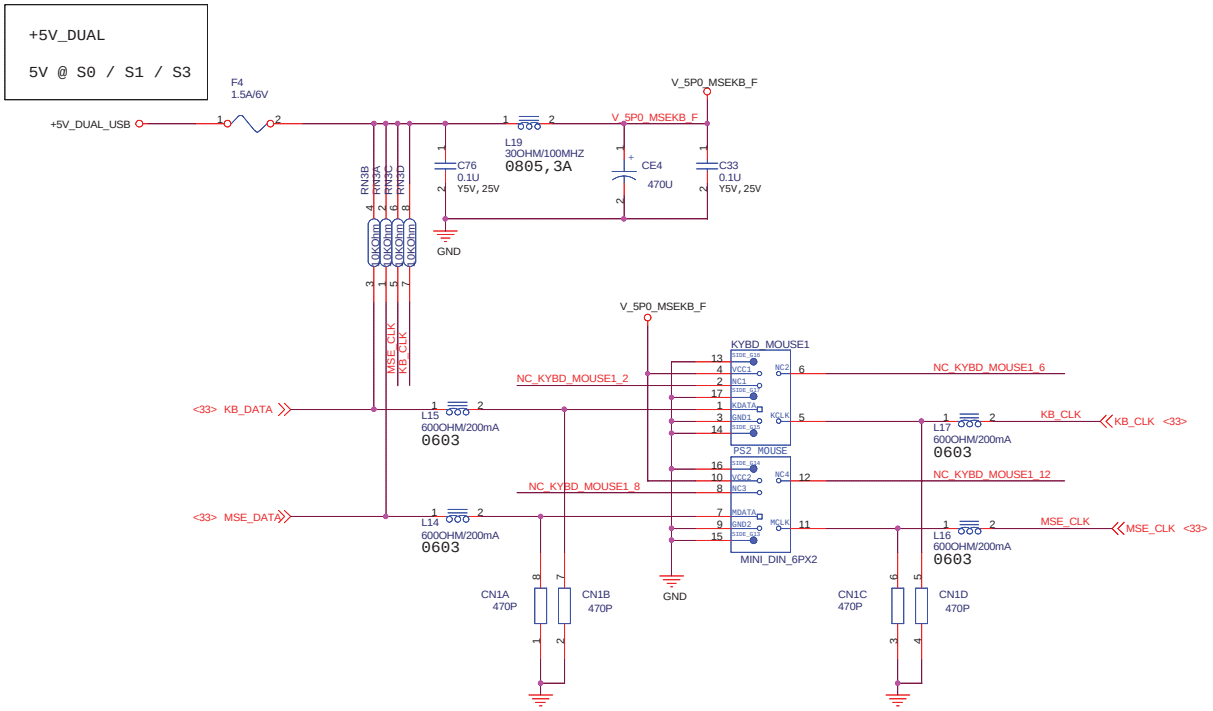
FLP_HDSEL# is already pulled up at FDD side. It is not necessary to pull up this signal at mother board side. However, I've seen this signal has a pull-up resistor in a few designs, probably for FDD compatibility. I think you may reserve the footprint of this pull-up resistor.

"FLP_INDEX#", "FLP_TRK0#", "FLP_WP#", FLP_RDATA#", "FLP_DSKCHG#" are input for 102 and these signals are of open drain type output from FDD. These 5 signals require 1K ohm pull-up resistor(to 5V) at mother board side.

<Core Design>

ASUStek Computer Inc.	Title : Floopy Disk	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 34 of 52	

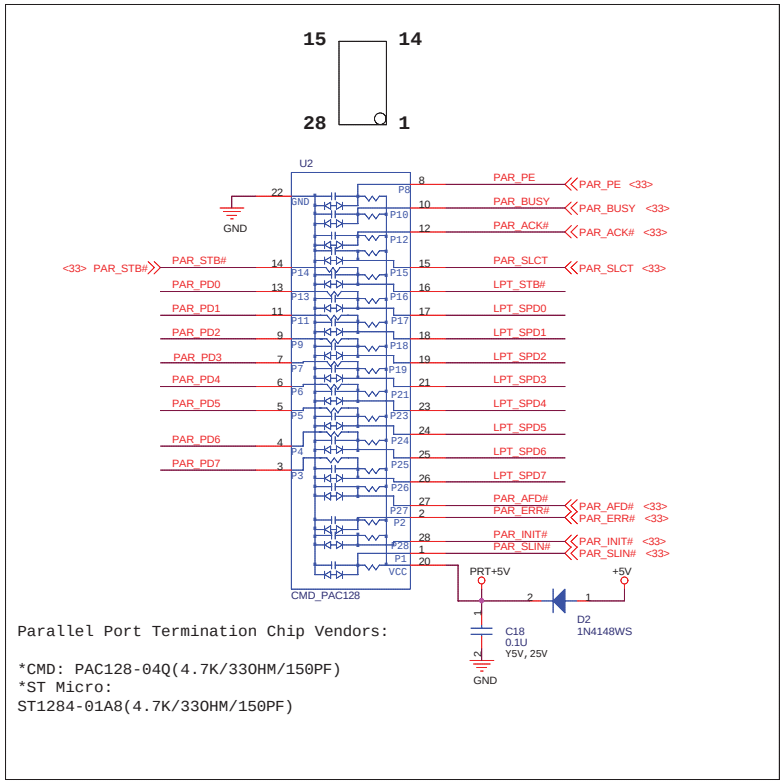
Keyboard & Mouse Port



<Core Design>

ASUSTek Computer Inc.	Title : KBRD,MOUSE,SPKR....	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 35 of 52	

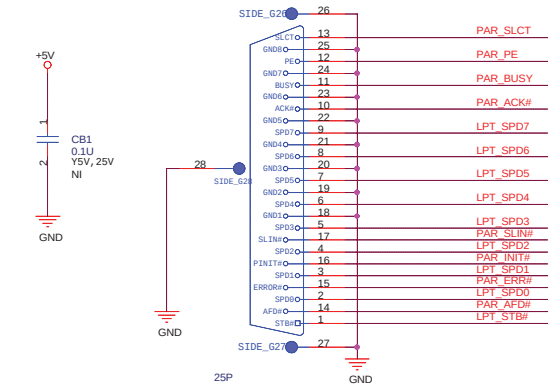
Parallel Port



Parallel Port Termination Chip Vendors:

*CMD: PAC128-04Q(4.7K/33OHM/150PF)
*ST Micro:
ST1284-01A8(4.7K/33OHM/150PF)

LPT PORT



<Core Design>

ASUSTek Computer Inc.

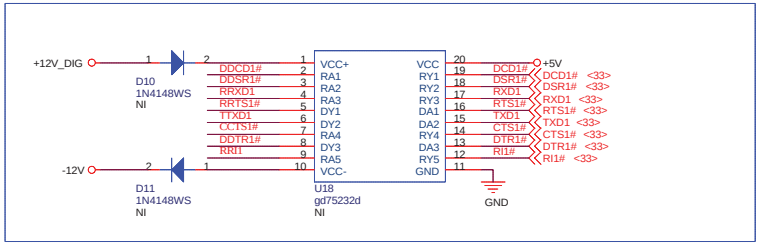
Title : PARALLEL PORT

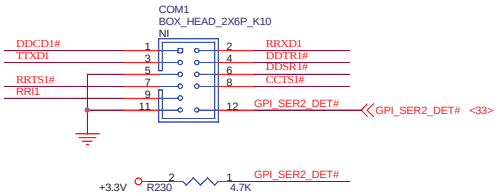
Engineer: Jason Lin

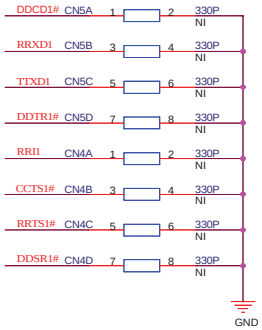
Size	Project Name	Rev
A3	Phoenix 2	X01

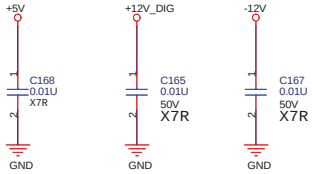
Date: Tuesday, March 18, 2003 Sheet 36 of 52

Serial Port



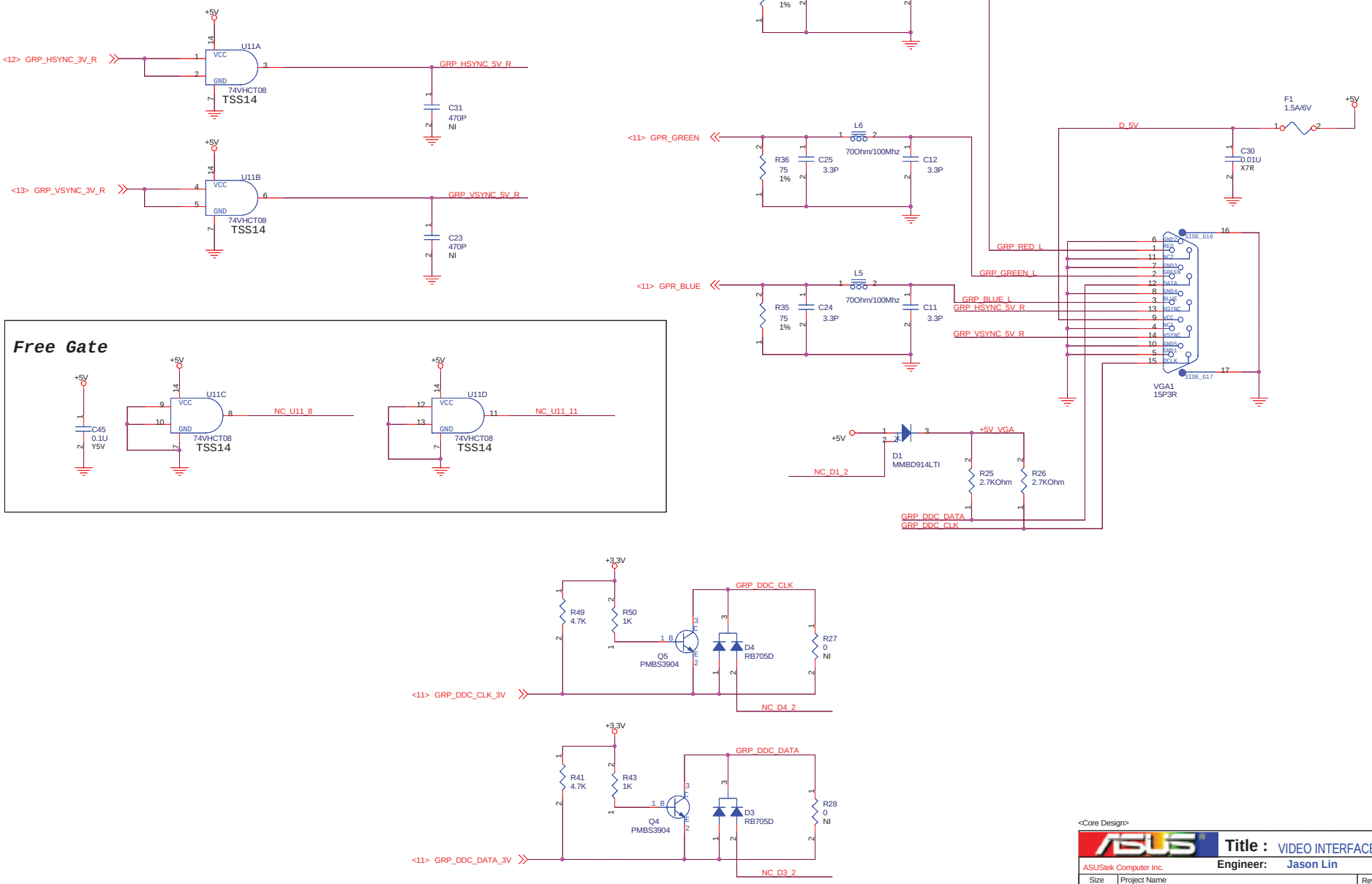






<core_design>
Title : SERIAL PORT
ASUStek Computer Inc.
Engineer: Jason Lin
Size: A3
Project Name: Phoenix 2
Rev: X01
Date: Tuesday, March 18, 2003
Sheet 37 of 52
</core_design>

Video Port



Free Gate

<Core Design>

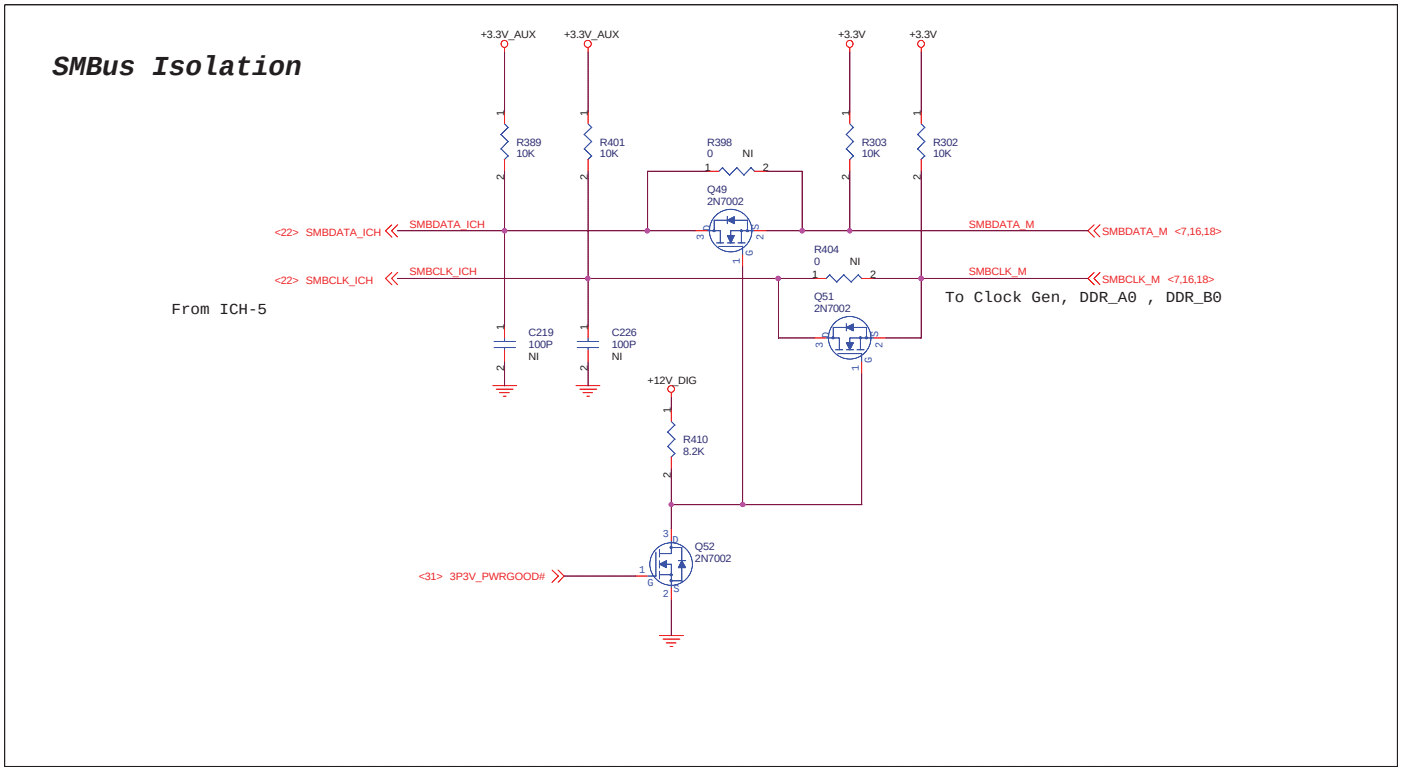
ASUStek Computer Inc.

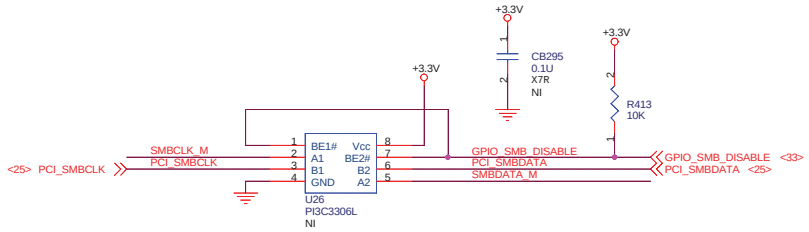
Title : VIDEO INTERFACE

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 38 of 52





<Core Design>

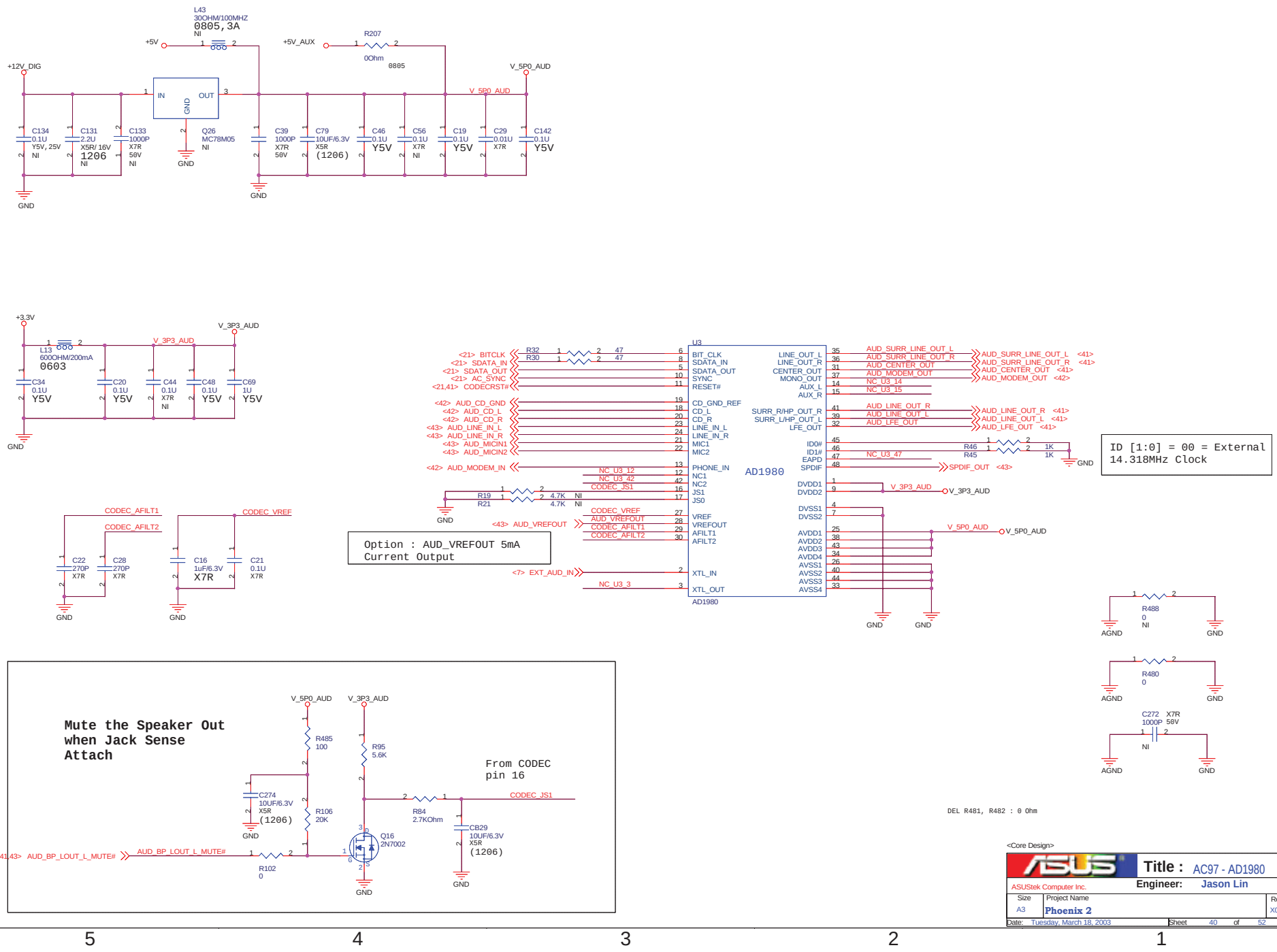
ASUStek Computer Inc.

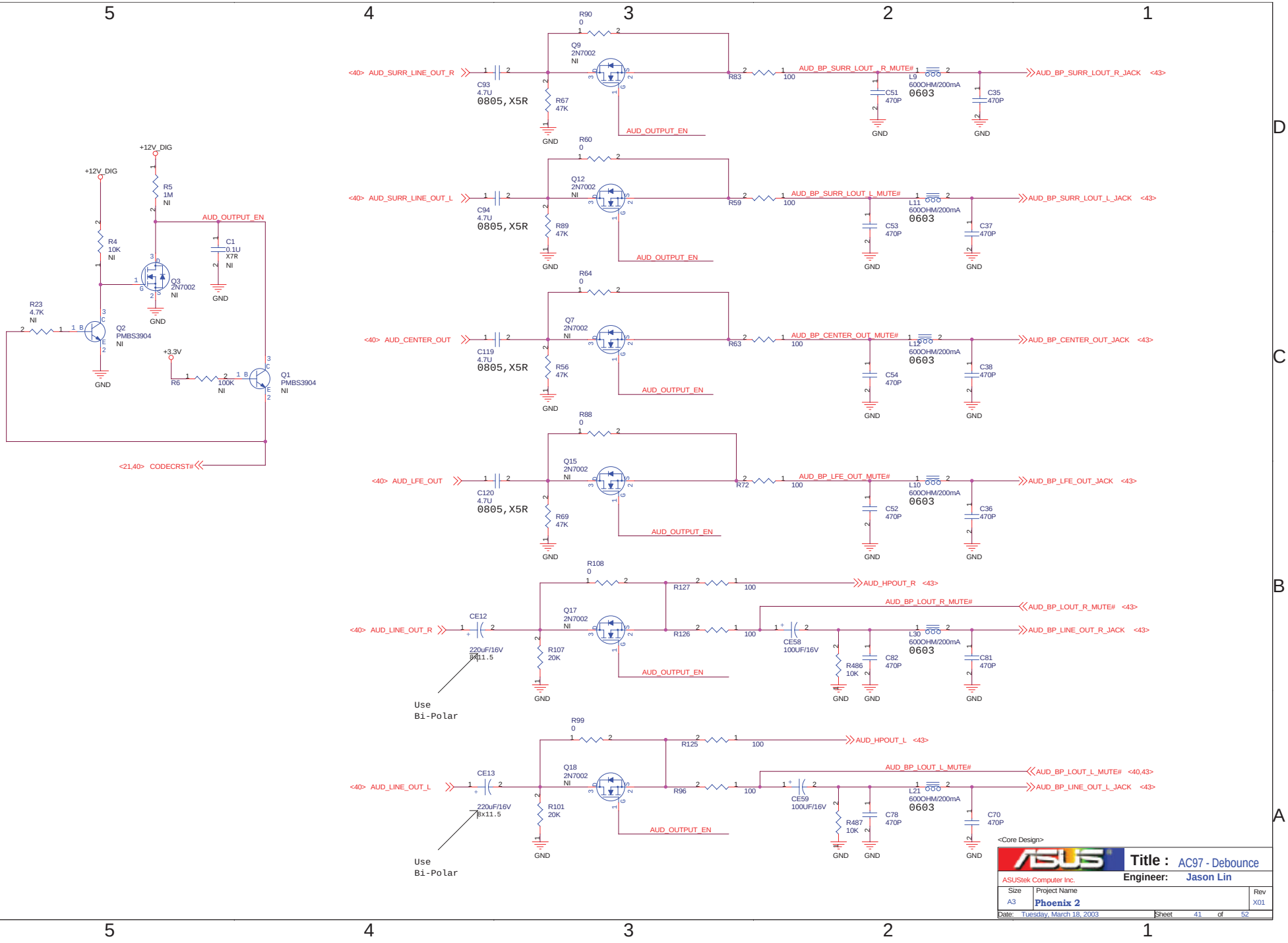
Title : SMBUS

Engineer: Jason Lin

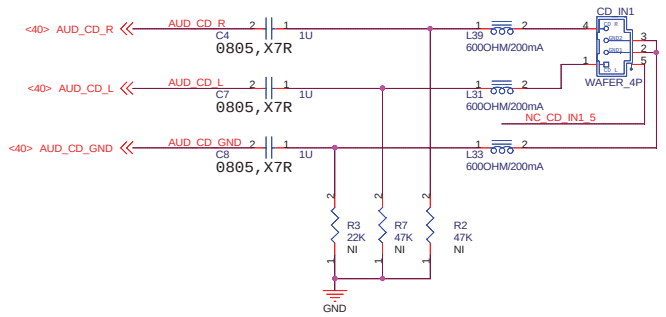
Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 39 of 52

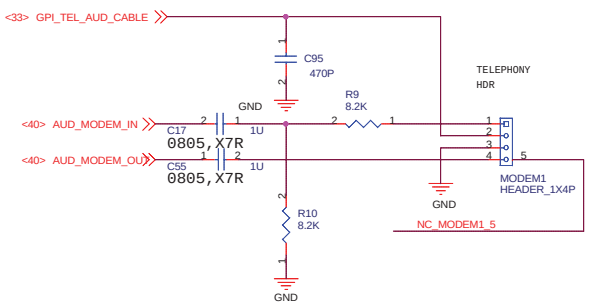




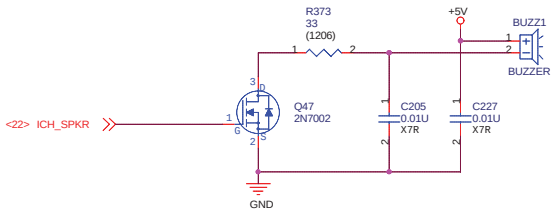
CD-IN Conn.



Telephone IN Conn.

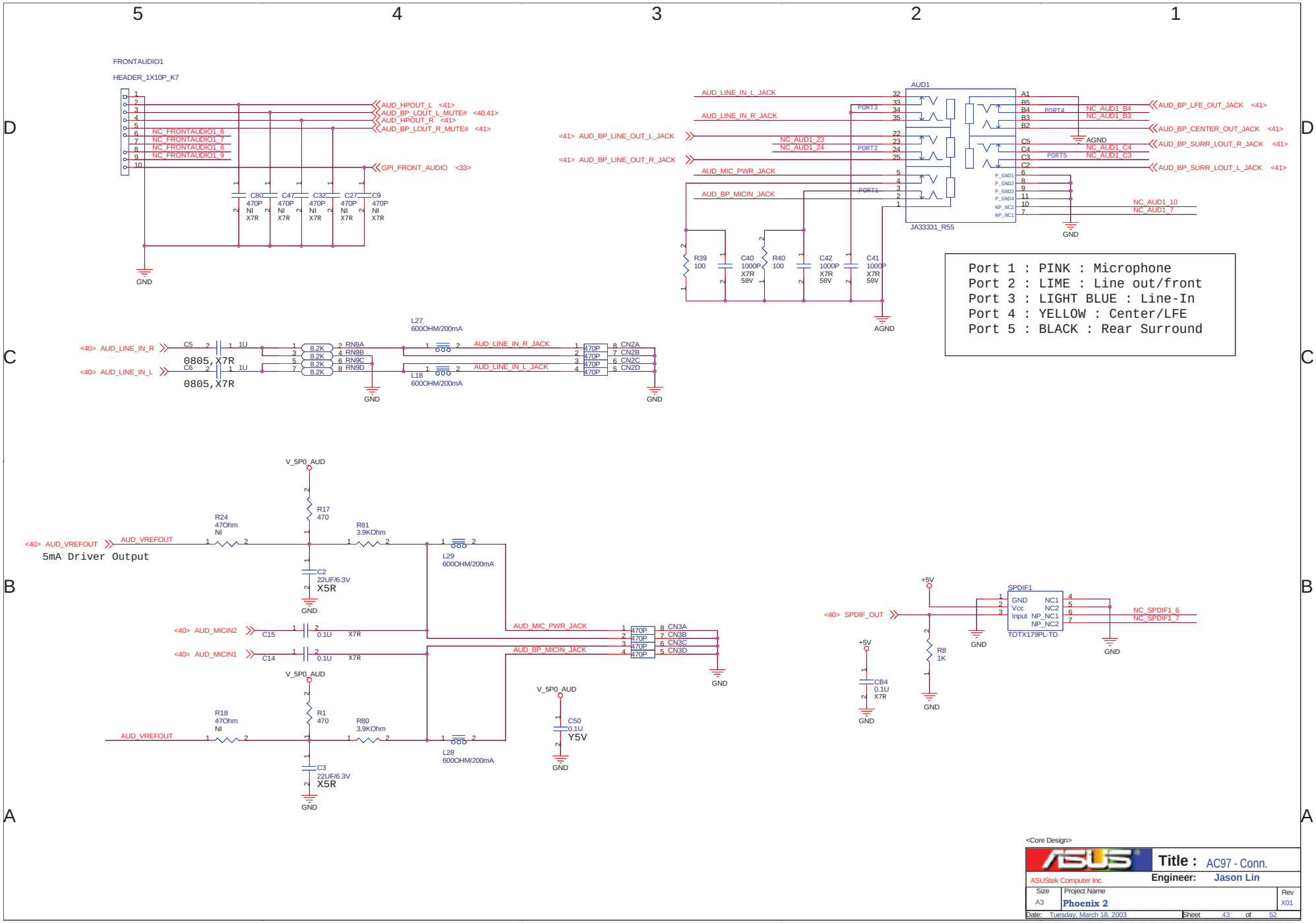


Onboard Buzzer



<Core Design>

ASUSTek Computer Inc.	Title : AC97 - AMP / Conn	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 42 of 52	



<Core Design>

ASUSTek Computer Inc.

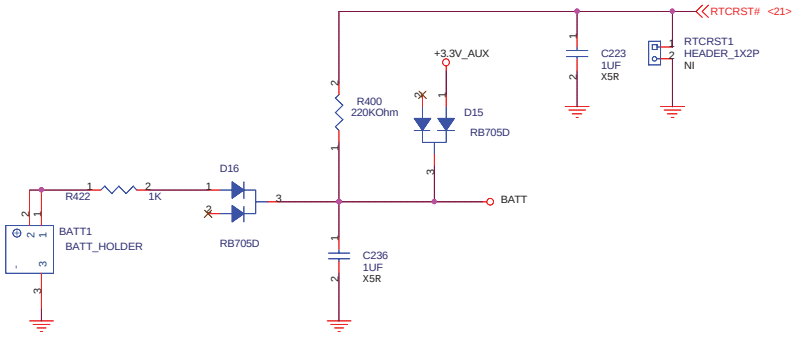
Title : AC97 - Conn.

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 43 of 52

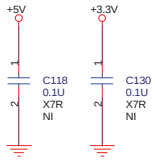
Battery

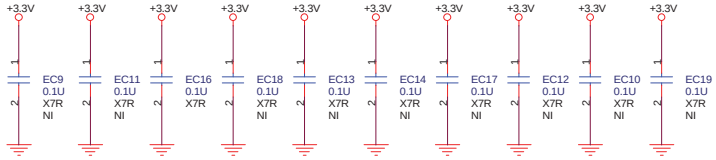


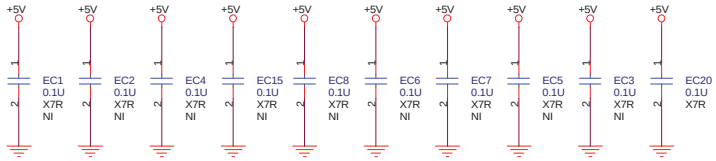
ATTENTION: OBTAIN SAFETY DEPT. APPROVAL BEFORE MODIFYING
CIRCUITRY IN THIS BOX.

<Core Design>

ASUStek Computer Inc.	Title : BATTERY	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 44 of 52	





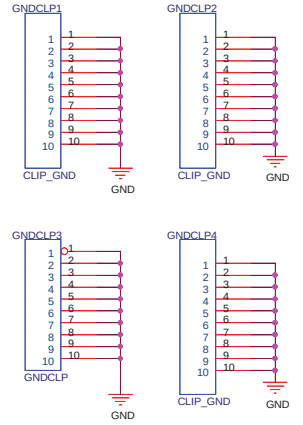


This page is left for EMI solution.

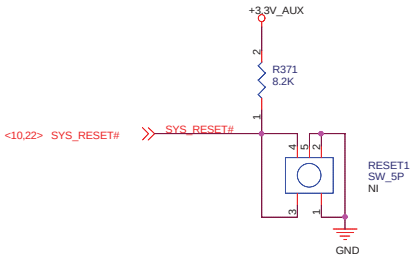
<Core Design>

ASUStek Computer Inc.	Title : EMI/DECOUPLING	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
Date: Tuesday, March 18, 2003	Sheet 45 of 52	

DELL M/B Claim

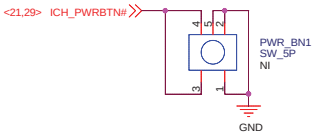


RESET BUTTOM



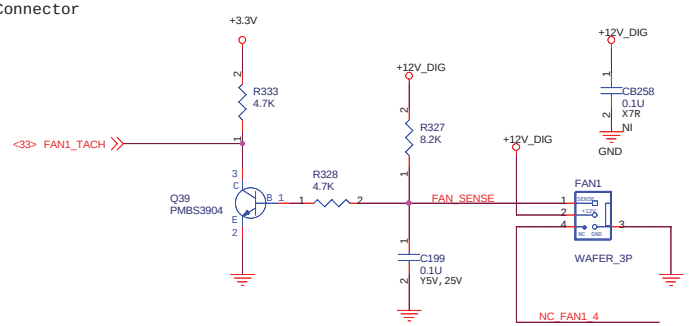
Proto Only

POWER BUTTOM

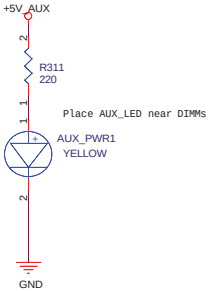


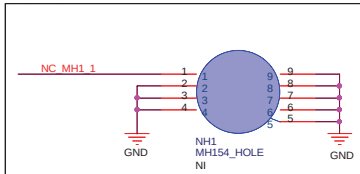
Proto Only

FAN Connector



Standby Power LED





<Core Design>

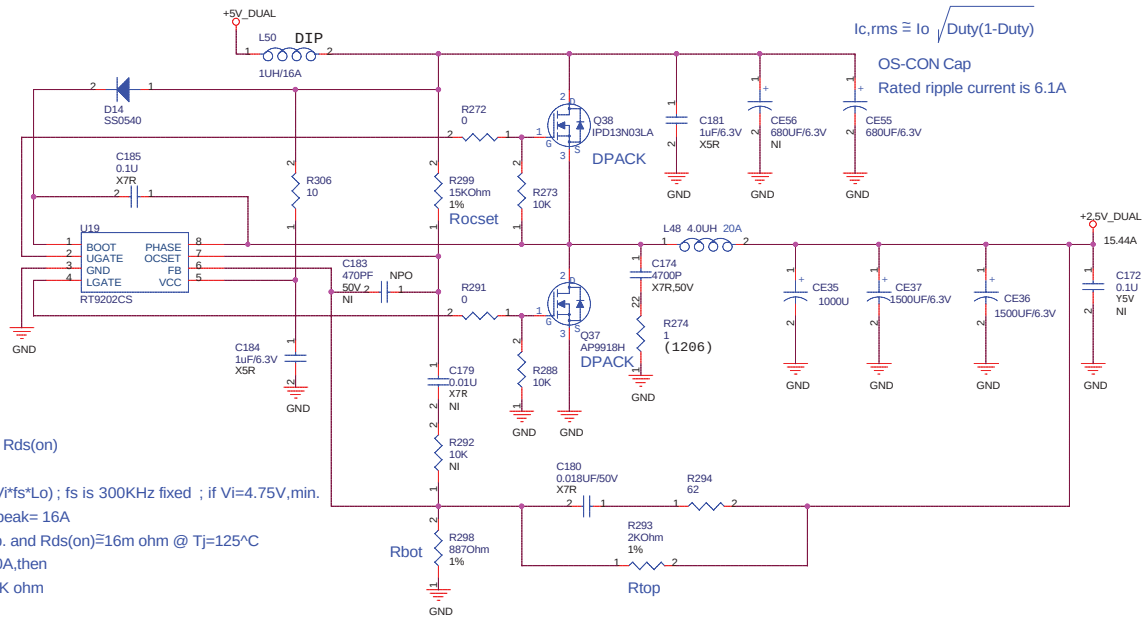
ASUStek Computer Inc.

Title : OTHER

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

Date: Tuesday, March 18, 2003 Sheet 46 of 52



Ic,rms ≅ Io √Duty(1-Duty)

OS-CON Cap

Rated ripple current is 6.1A

Multiplier for ripple current for electrolytic capacitor

(1) Temperature coefficient

Frequency	105	85	65 >=
Coefficient	1.0	1.7	2.1

+2.5V_DUAL

2.5V Dual Power @S0/S1/S3

Vo=0.8V(1+ Rtop/Rbot)

Rtop = 2K , Rbot = 909 Ohm, Vo = 2.56V

Rtop = 2K , Rbot = 887 Ohm, Vo = 2.60V

RT9202CS :

Ipeak= Iocset*Rocset / Rds(on)

Ipeak=Io+(delta IL/2)

delta IL≅(Vi-Vo)*Vo / (Vi*fs*Lo) ; fs is 300KHz fixed ; if Vi=4.75V,min.

then delta IL≅1A and Ipeak= 16A

also Iocset is 40uA Typ. and Rds(on)≅16m ohm @ Tj=125^C

The Ipeak is elected 20A,then

we get the Rocset=8.2K ohm

Notification : U19 Source Priority

1st:RT9202CS:06-008129000

2nd:ISL6520CB-T:06-008116011

3rd:ISL6520ACB-T:06-008116010

If the RT9202 is used in the +2.5V, please modify items as follows : R292=NC ; C179=NC ; C183=NC.

AP9918H Spec. :

Vds=20V , Vgs=+/- 12V , Rthj-c=2.6 ^C/W

Rds(on)=14m ohm @ Vgs=4.5V ,Id=18A

Qg=19nC , Qgs=1.5nC , Qgd=10.5nC Typ.

Ciss=500PF , Coss=310PF , Crss=125PF Typ.

CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD FOR DPAK(TO252) LET Tja OF 20C/W FOR 1.2A ON DDR VTT

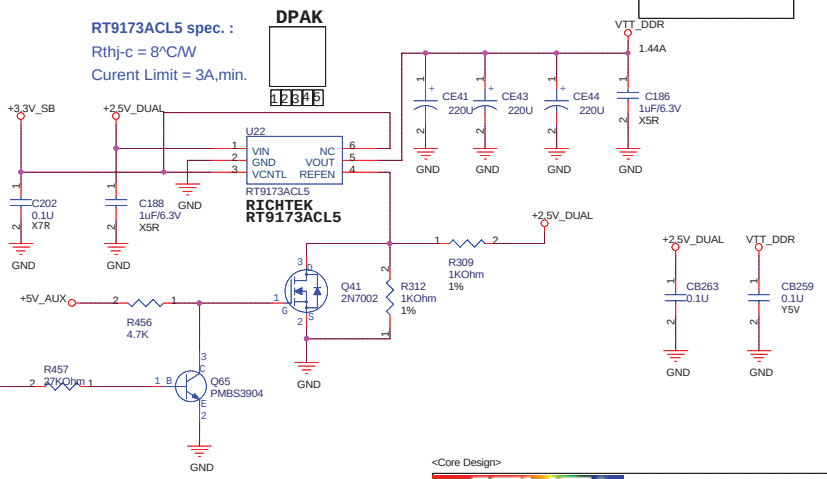
VTT_DDR

1.25V@S0/S1

RT9173ACL5 spec. :

Rthj-c = 8^C/W

Curent Limit = 3A,min.



Note:

Id=[(Tj,max-Tc)/Rds(on)*Rth(j-c)] That is continous current rating of Id without swithing losses present

Ploss,upper MOSFET=Pconduction+Pswitch+Pgate drive+Poutput

=Idrms1*Idrms1*Rds(on)+[(Qsw/Ig)Io*Vin*fs)]+Qg*Vg*fs+[(Qoss/2)*Vin*fs]; Qsw=Qgs2+Qgd

Ploss,lower MOSFET=Pconduction+Pgate drive+Poutput+Pbody diode

=Idrms2*Idrms2*Rds(on)+Qg*Vg*fs+[(Qoss/2)*Vin*fs]+Qrr*Vin*fs;

Id,rms1=IL,rms*√D ; Id,rms2=IL,rms*√1-D IL,rms=Io √{1+[(1/12)*[(1-D)*Vo/(Io*L*fs)]^2]}

<Core Design>

Title : 2.5VSTBY/1.25V

ASUSTek Computer Inc. Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

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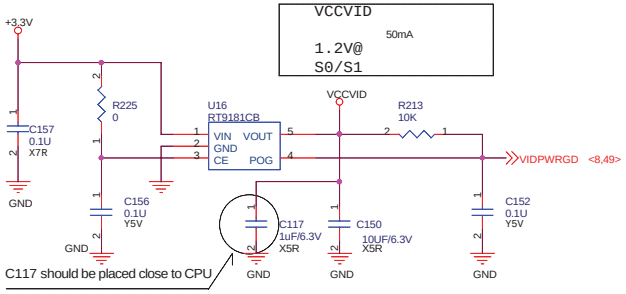
RT9181CB spec. :
Pd=570m W
Td(POG)=1 to 5mS; 2mS is Typical
Current Limit = 160mA @Rload=1 ohm

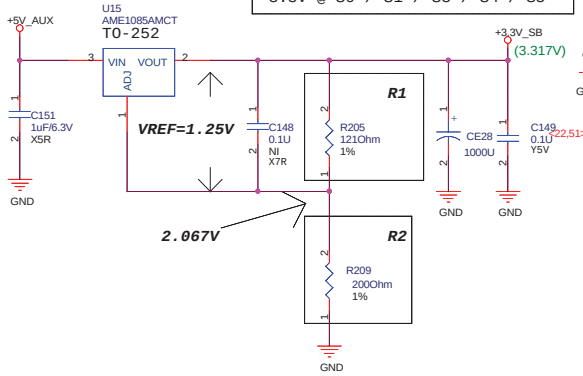
VCCVID
50mA
1.2V@
S0/S1



Notification : U16 Source Priority
1st:RT9181CB:06-007074210
2nd:MIC5258-1.2BM5:06-007095010
3rd:SN105125:06-00074110

AME1085AMCT spec. :
Dropout voltage=1.3V Typ. @ Io=10mA~3A
Ripple rejection ratio 72 dB Typ.
Rthj-c = 15^C / W

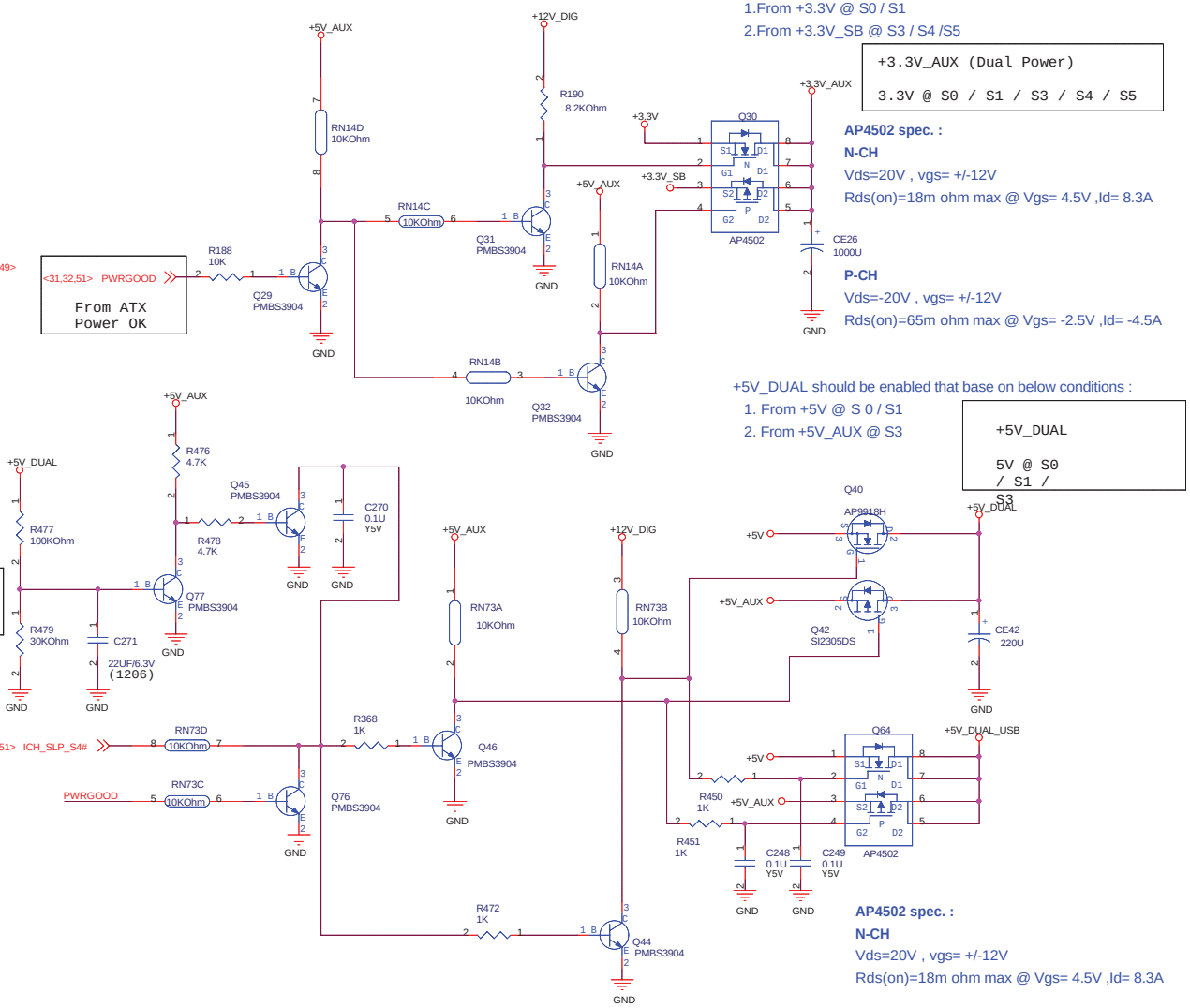
+3.3V_SB
3.3V @ S0 / S1 / S3 / S4 / S5



Notification : U45 Source Priority
1st:AME1085AMCT:06-007005430
2nd:AMS1085AMCT:06-007042120

$$Vout = Vref * (1 + R2 / R1) + Iadj * R2$$

$$Vref = 1.25V$$
$$Iadj = 50uA$$



+3.3V_AUX should be enabled that base on below conditions :
1.From +3.3V @ S0 / S1
2.From +3.3V_SB @ S3 / S4 /S5

+3.3V_AUX (Dual Power)
3.3V @ S0 / S1 / S3 / S4 / S5

AP4502 spec. :
N-CH
Vds=20V , vgs= +/-12V
Rds(on)=18m ohm max @ Vgs= 4.5V ,Id= 8.3A
P-CH
Vds=-20V , vgs= +/-12V
Rds(on)=65m ohm max @ Vgs= -2.5V ,Id= -4.5A

+5V_DUAL should be enabled that base on below conditions :
1. From +5V @ S 0 / S1
2. From +5V_AUX @ S3

+5V_DUAL
5V @ S0 / S1 / S3

AP4502 spec. :
N-CH
Vds=20V , vgs= +/-12V
Rds(on)=18m ohm max @ Vgs= 4.5V ,Id= 8.3A
P-CH
Vds=-20V , vgs= +/-12V
Rds(on)=65m ohm max @ Vgs= -2.5V ,Id= -4.5A

<Core Design>

ASUSTek Computer Inc.	Title : 5V&3V_DAUL/3V_AUX/1.2V	
	Engineer: Jason Lin	
Size: A3	Project Name: Phoenix 2	Rev: X01
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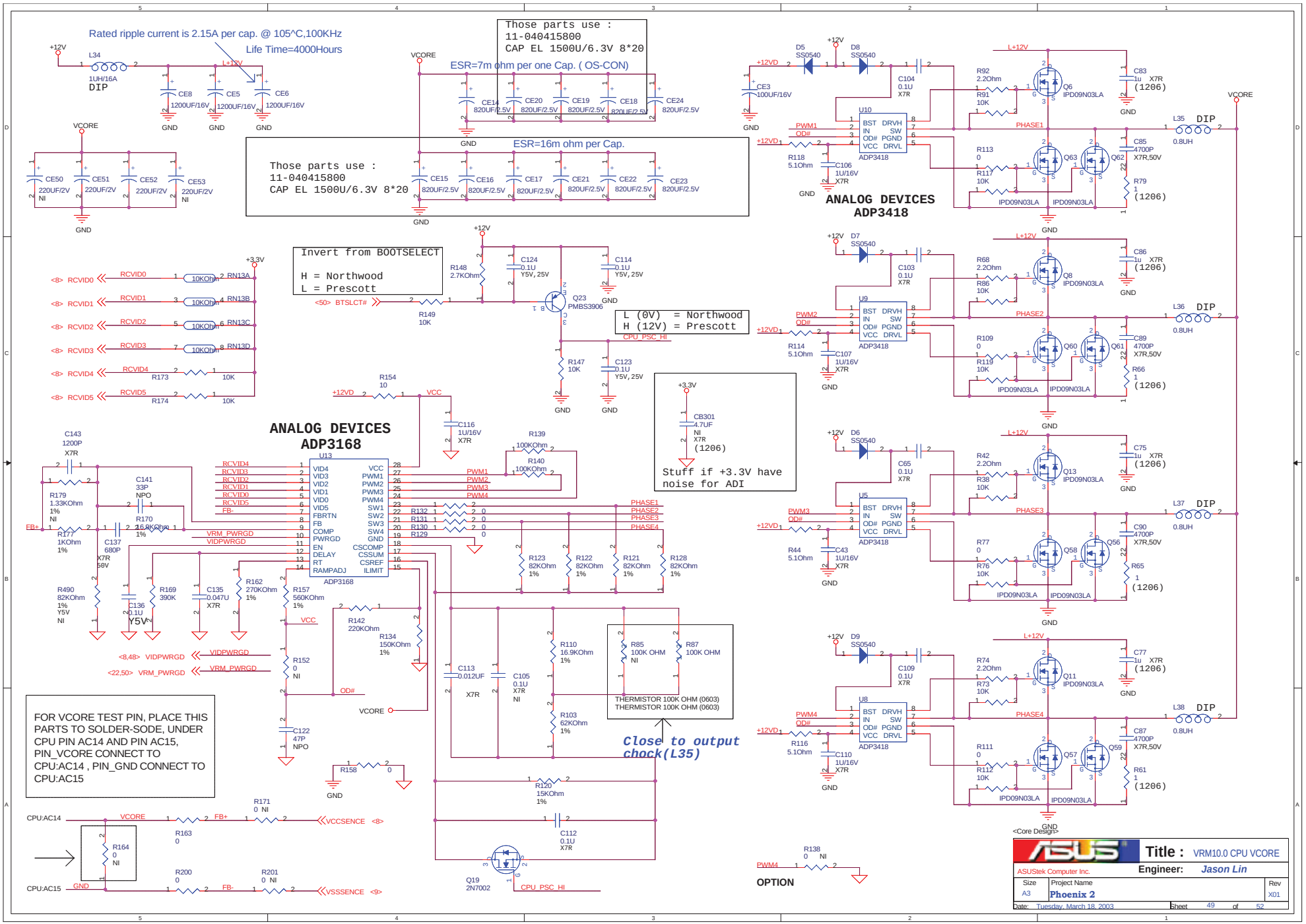

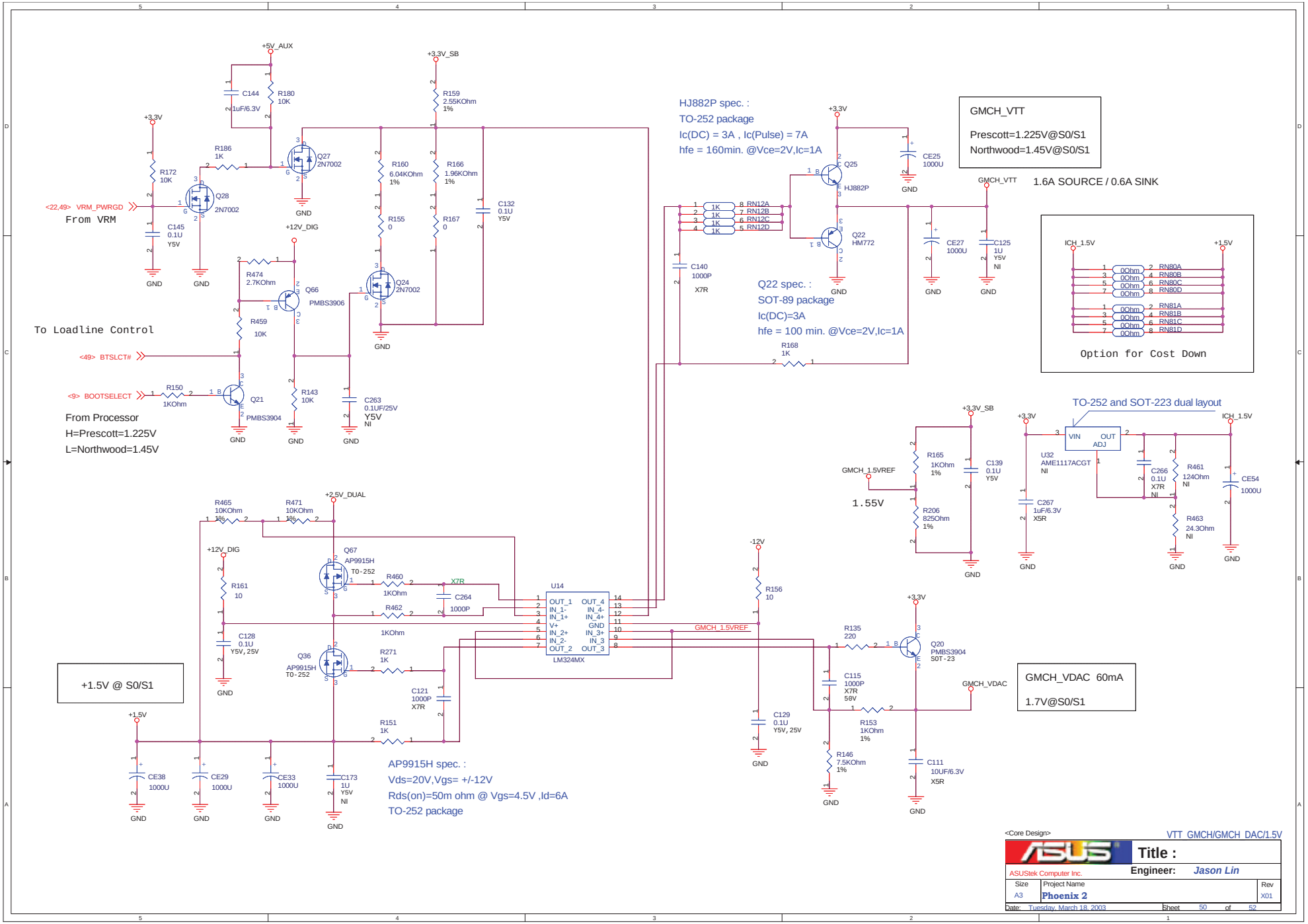

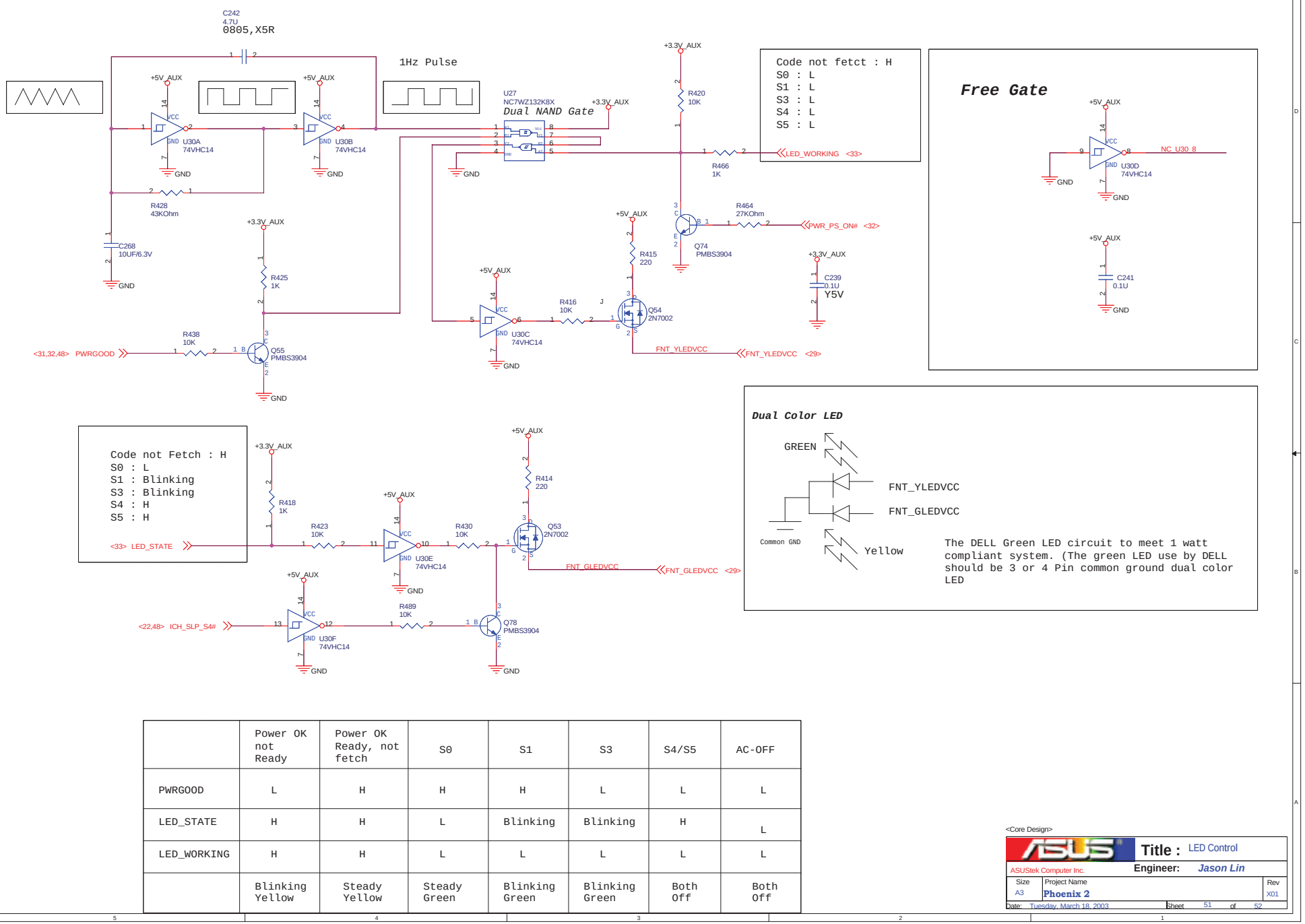

	Power OK not Ready	Power OK Ready, not fetch	S0	S1	S3	S4/S5	AC-OFF
PWRGOOD	L	H	H	H	L	L	L
LED_STATE	H	H	L	Blinking	Blinking	H	L
LED_WORKING	H	H	L	L	L	L	L
	Blinking Yellow	Steady Yellow	Steady Green	Blinking Green	Blinking Green	Both Off	Both Off

<Core Design>

ASUSTek Computer Inc.

Title : LED Control

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

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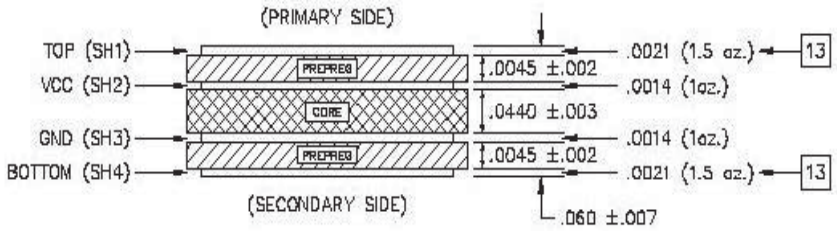
PCB Stackup Spec :



DETAIL A

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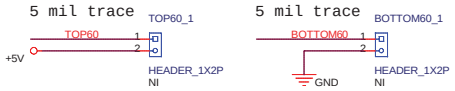
	BUS	STANDARD	HOST CLOCKS	ETHERNET/S-ATA	USB2.0	DDR DATA	DDR CLOCK
	TYPE	SINGLE	DIFFERENTIAL	DIFFERENTIAL	DIFFERENTIAL	SINGLE	DIFFERENTIAL
	TOLERANCE	60 OHMS TRACE	100 OHMS ±10%	100 OHMS ±10%	90 OHMS ±15%	50 OHMS ±15%	70 OHMS ±10%
	GEOMETRY (MILS)	TRACE WIDTH	TRACE/SPACE/TRACE	TRACE/SPACE/TRACE	TRACE/SPACE/TRACE	TRACE WIDTH	TRACE/SPACE/TRACE
DESIGN GEOMETRY	LAYER 1	5	6/10/6	6/10/6	7.5/7.5/7.5	7	8/5/8
	LAYER 2	VCC	VCC	VCC	VCC	VCC	VCC
	LAYER 3	GND	GND	GND	GND	GND	GND
	LAYER 4	5	6/10/6	6/10/6	7.5/7.5/7.5	7	8/5/8
	MEASUREMENT REQUIREMENTS	STACKUP	STACKUP	STACKUP	STACKUP	STACKUP	STACKUP

Impendence Control Test Trace



Reference to +5V power plane

Reference to ground plane

<Core Design>

ASUSTek Computer Inc.

Title : LED Control

Engineer: Jason Lin

Size	Project Name	Rev
A3	Phoenix 2	X01

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