INTEL 845PE Preliminary Customer Reference Schematics

Revision 1.01

NOT

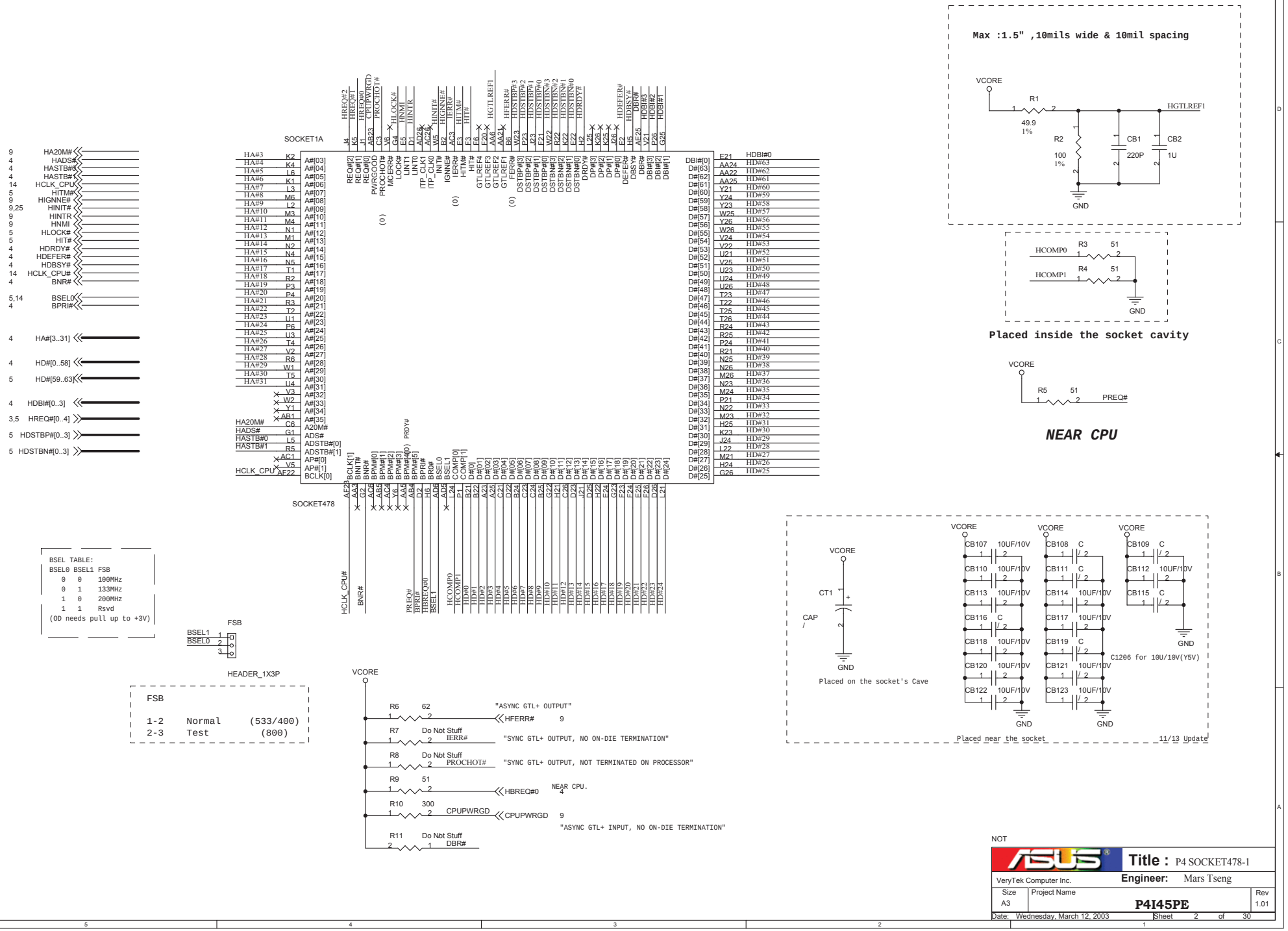
ASRock Computer Inc.

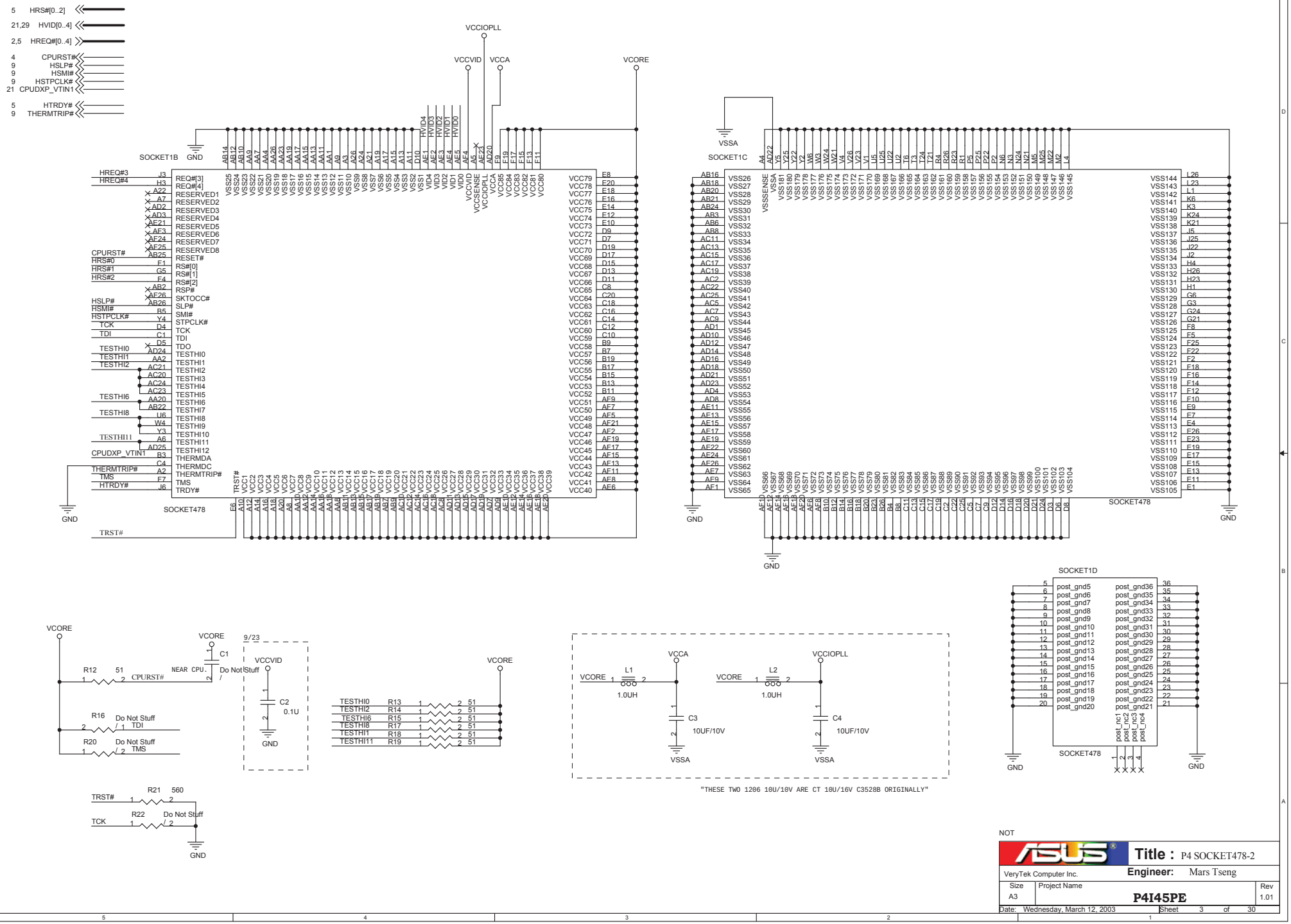
Title : COVER SHEET

Engineer: Mars Tseng

Size	Project Name	Rev
Custom	P4I45PE	1.01

Date: Wednesday, March 12, 2003 Sheet 1 of 30





NOT

ASUS	Title : P4 SOCKET478-2	
VeryTek Computer Inc.	Engineer: Mars Tseng	
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 3 of 30	

15 GADSTB0
15 GADSTB#0
15 GADSTB1
15 GADSTB#1
2 HADS#
15 AGPVREF_CG
14 HCLK_NB#
14 HCLK_NB
2 BNR#
2 BPRI#
2 HBREQ#0
3 CPURST#
2 HDBSY#
2 HDEFER#
2 HDRDY#

15 GST[0..2]

2 HDBI#[0..3]

2 HD#[0..58]

15 GAD[0..31]

15 GC/BE#[0..3]

2 HA#[3..31]

15 GDEVSEL#
15 GFRAME#
15 GGNT#
15 GIRDY#
15 GPAR
15 GREQ#
15 GSTOP#
15 GTRDY#
2 HASTB#0
2 HASTB#1

15 GSBSTB
15 GSBSTB#
15 GWBF#
14 66M_NB

15 GSBA[0..7]

15 GPIPE#

15 GRBF#

20 LB
20 LG
20 DDCCLK
20 DDCDATA
14 48M_VGA

U1A

HADS#	T36	ADS#	
GRCOMP	L2	AGP_RCOMP	
AGPVREF_CG	W2	AGP_VREF	
LB	G15	BLUE	
LB#	H16	BLUE#	
BNR#	T34	BNR#	
BPRI#	M34	BPRI#	
HBREQ#0	U33	BREQ0#	
CPURST#	D22	CPURST#	
HDBSY#	U31	DBSY#	
DDCCLK	D7	DDCA_CLK	
DDCDATA	C7	DDCA_DATA	
HDEFER#	N36	DEFER#	
HDBI#0	N33	DINV_0#	
HDBI#1	C35	DINV_1#	
HDBI#2	B33	DINV_2#	
HDBI#3	C26	DINV_3#	
HDRDY#	U36	DRDY#	
48M_VGA	D14	DREFCLK	
GAD0	V4	GAD_0	
GAD1	V2	GAD_1	
GAD2	W4	GAD_2	
GAD3	W5	GAD_3	
GAD4	U5	GAD_4	
GAD5	U4	GAD_5	
GAD6	U2	GAD_6	
GAD7	V3	GAD_7	
GAD8	T2	GAD_8	
GAD9	T3	GAD_9	
GAD10	T4	GAD_10	
GAD11	R2	GAD_11	
GAD12	R5	GAD_12	
GAD13	R7	GAD_13	
GAD14	T8	GAD_14	
GAD15	P3	GAD_15	
GAD16	P8	GAD_16	
GAD17	K4	GAD_17	
GAD18	K2	GAD_18	
GAD19	J2	GAD_19	
GAD20	M3	GAD_20	

BROOKDALE-G

HD_8#	J36	HD#8	
HD_7#	P35	HD#7	
HD_6#	L36	HD#6	
HD_5#	L33	HD#5	
HD_4#	R31	HD#4	
HD_3#	N34	HD#3	
HD_2#	R34	HD#2	
HD_1#	R33	HD#1	
HD_0#	T30	HD#0	
HCLKP	K30	HCLK_NB	
HCLKN	J31	HCLK_NB#	
HCC_VREF	P30	GTLREF_MCH	GTLREF_MCH 5
HADSTB_1#	AE30	HASTB#1	
HADSTB_0#	AB35	HASTB#0	
HA_VREF	AD30		
HA_31#	AG31	HA#31	
HA_30#	AG33	HA#30	
HA_29#	AH35	HA#29	
HA_28#	AE31	HA#28	
HA_27#	AG36	HA#27	
HA_26#	AC34	HA#26	
HA_25#	AF34	HA#25	
HA_24#	AE33	HA#24	
HA_23#	AF36	HA#23	
HA_22#	AE36	HA#22	
HA_21#	AD34	HA#21	
HA_20#	AF34	HA#20	
HA_19#	AD35	HA#19	
HA_18#	AD36	HA#18	
HA_17#	AE35	HA#17	
HA_16#	AC31	HA#16	
HA_15#	AC36	HA#15	
HA_14#	AB36	HA#14	
HA_13#	Y34	HA#13	
HA_12#	AB34	HA#12	
HA_11#	AC34	HA#11	
HA_10#	AA36	HA#10	
HA_9#	Y35	HA#9	
HA_8#	AC33	HA#8	
HA_7#	Y36	HA#7	

CAP SHOULD BE CLOSE TO GMCH PIN

VCORE — R23 49.9Ohm 1% — GTLREF_MCH

R24 100Ohm 1% — C5 0.1U X7R — GND — GND

12 MIL TRACE, 10 MIL SPACE

R25 40.2Ohm 1% — GRCOMP

GND

LB# — R300 40.2Ohm /845GE — C257 33P /845GE

LG# — R301 40.2Ohm /845GE — C258 33P /845GE

Place at the connector side

NOT

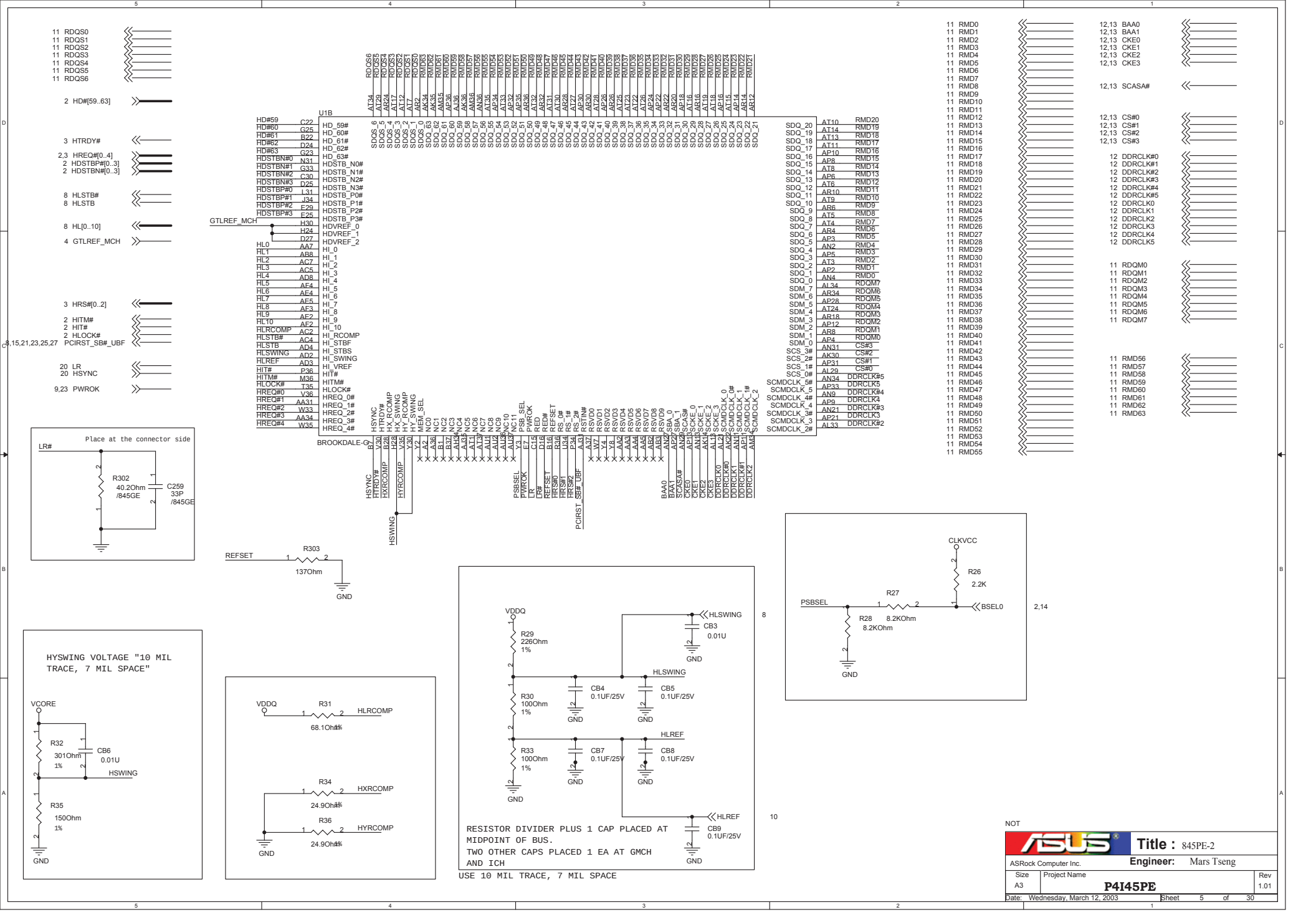
ASUS

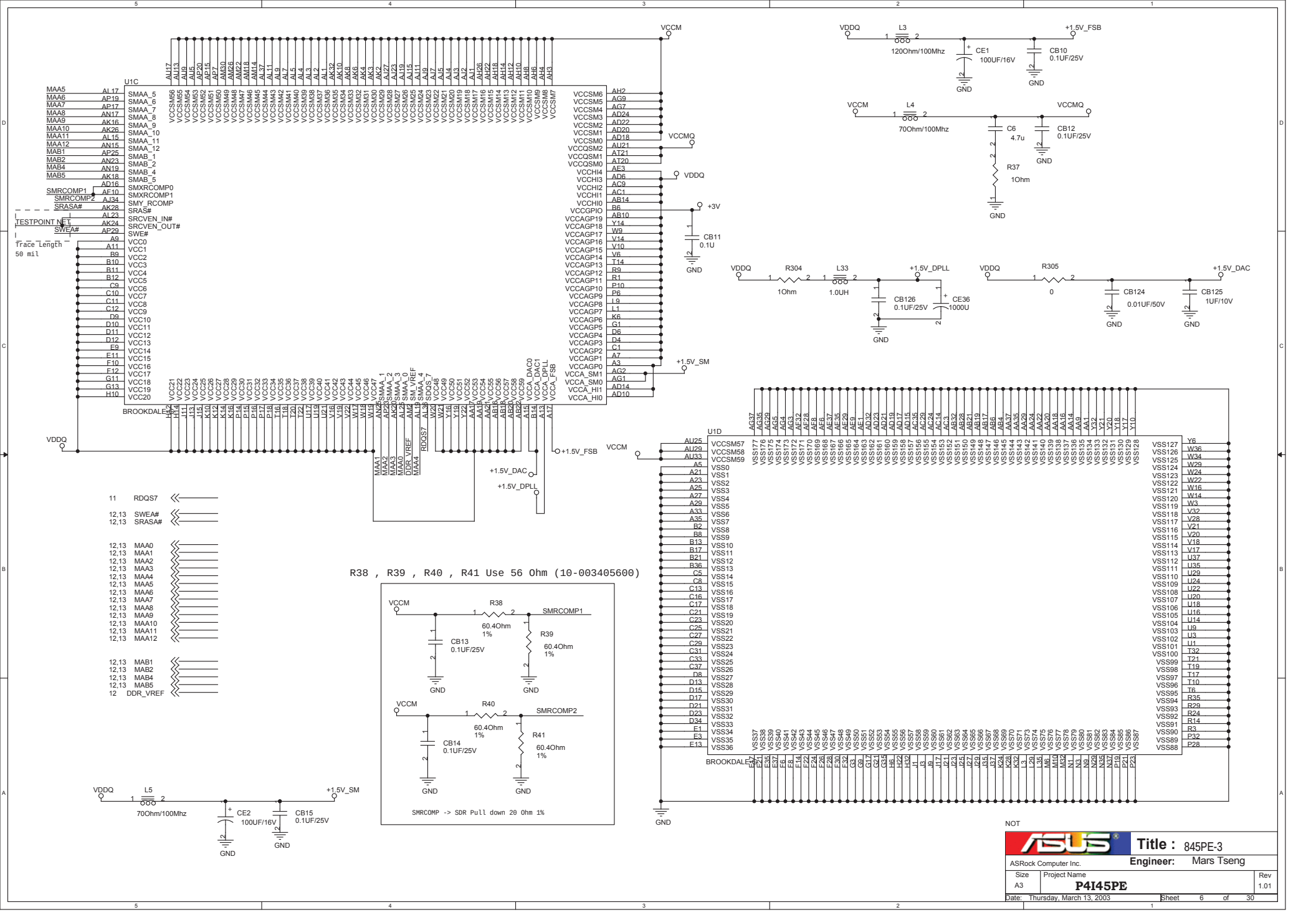
Title : 845PE-1

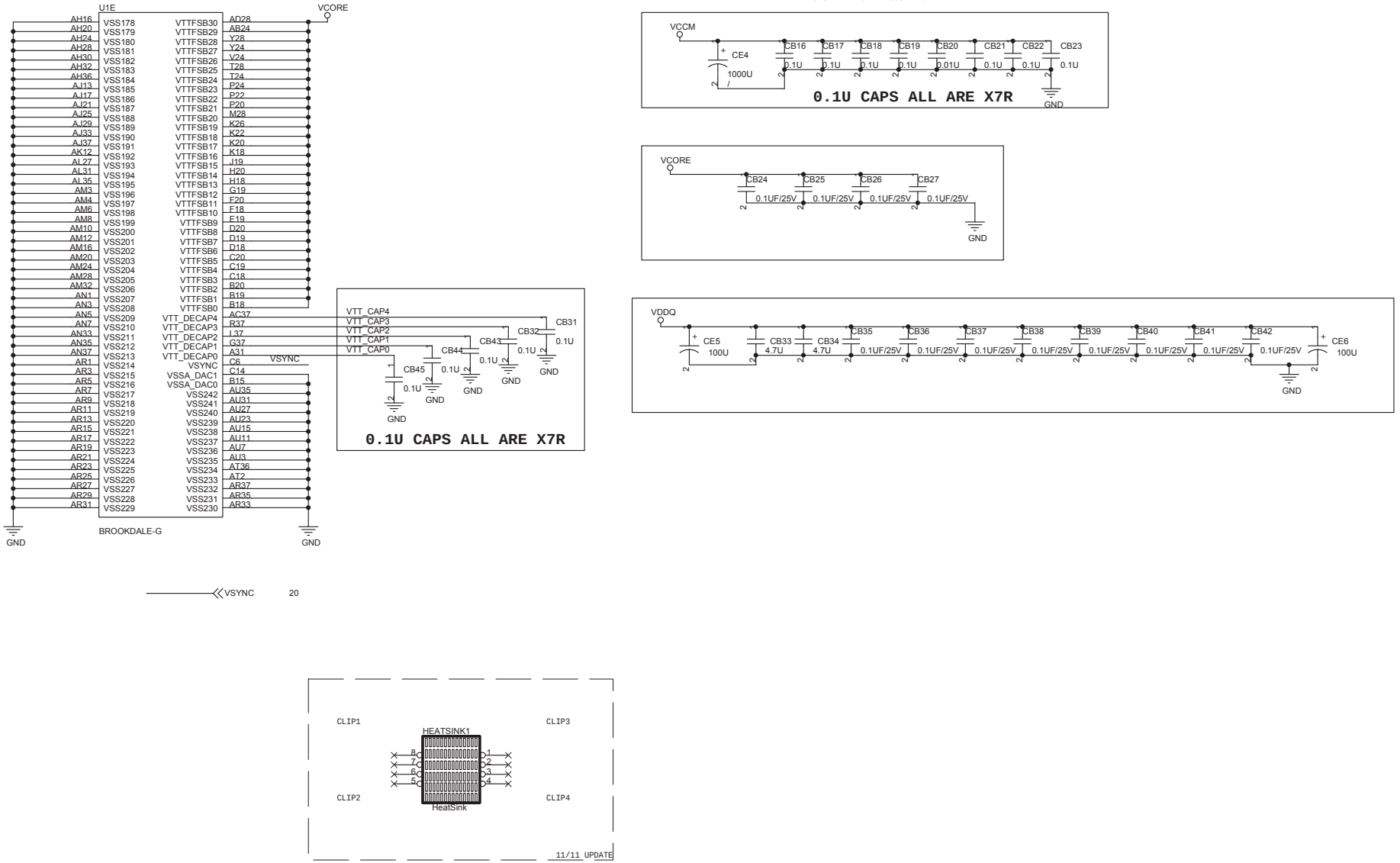
ASRock Computer Inc. Engineer: Mars Tseng

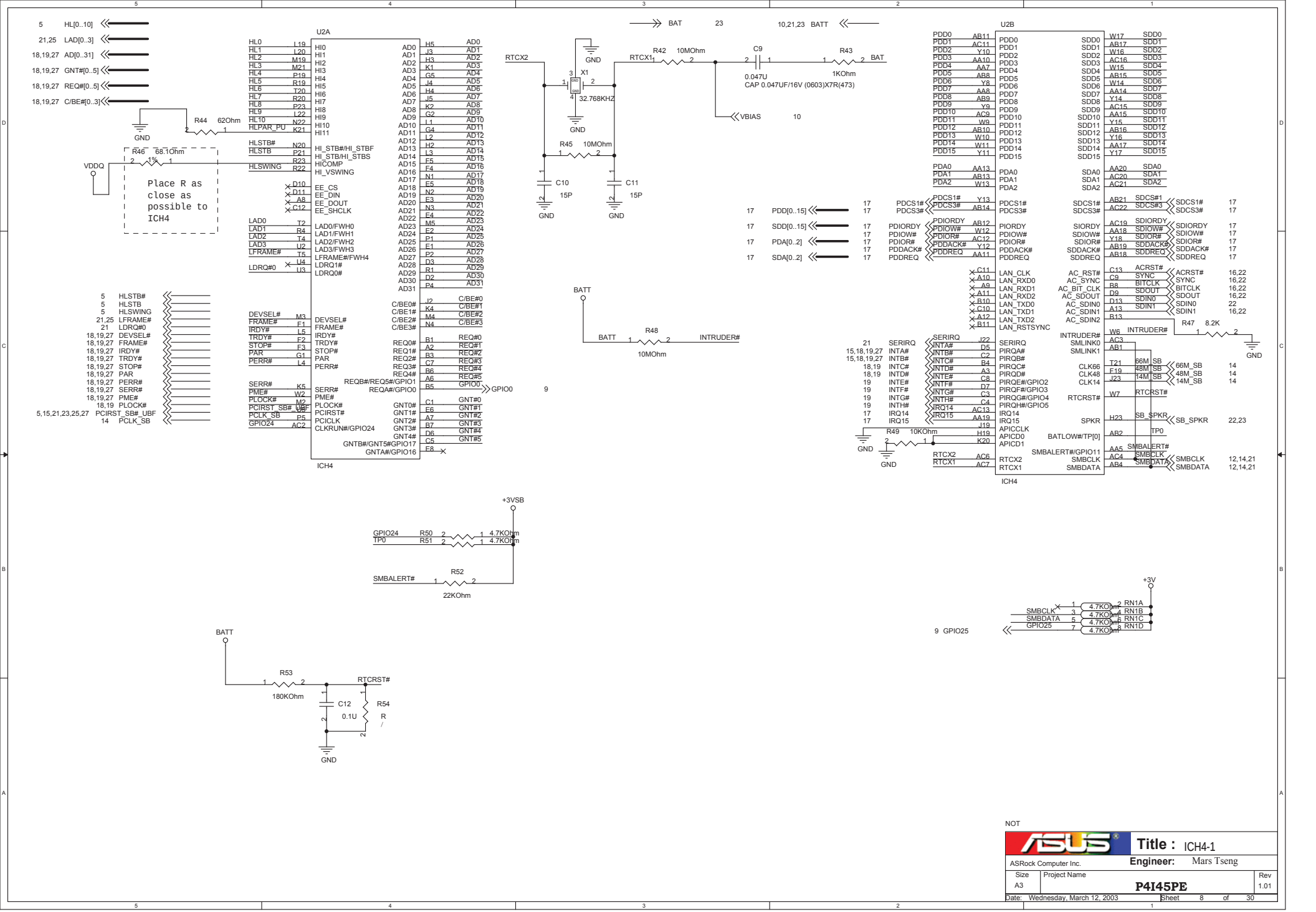
Size	Project Name	Rev
A3	P4I45PE	1.01

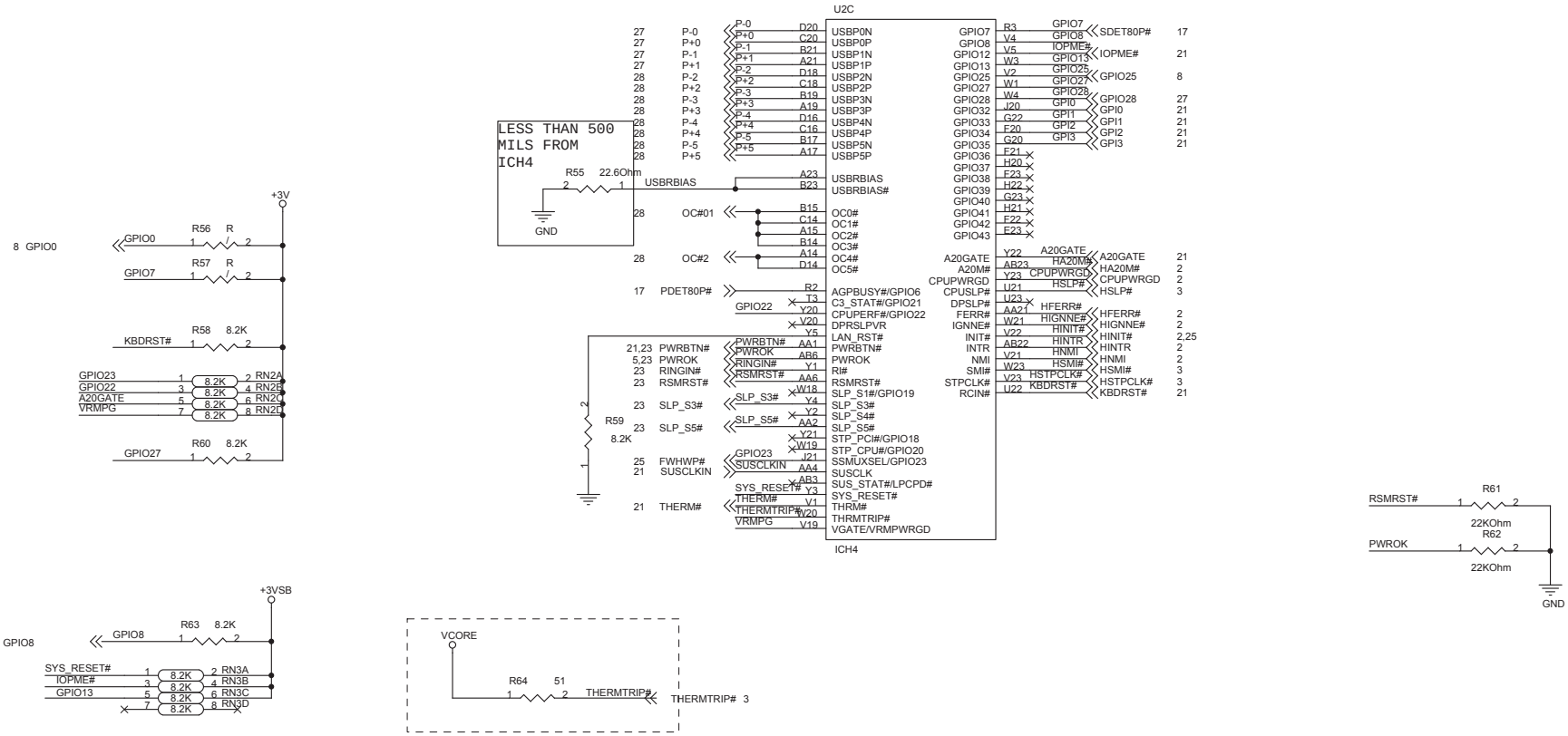
Date: Wednesday, March 12, 2003 Sheet 4 of 30





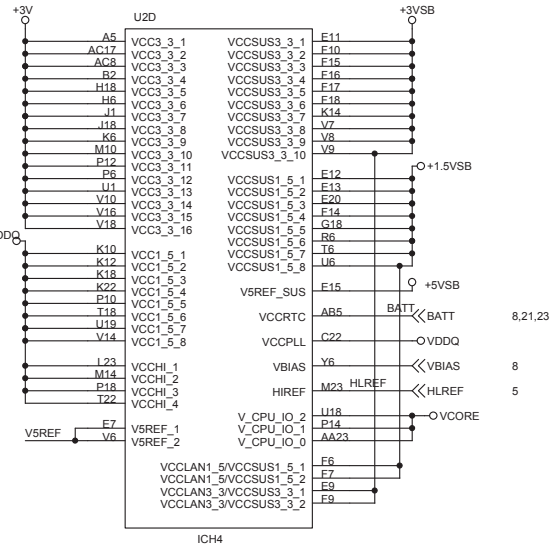


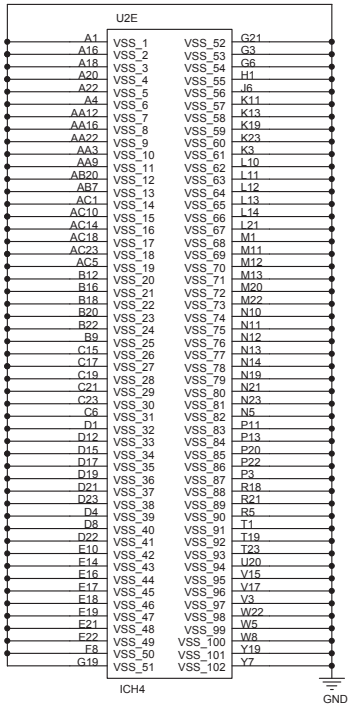


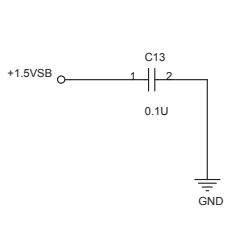


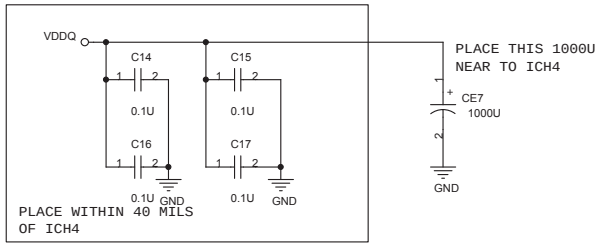
NOT

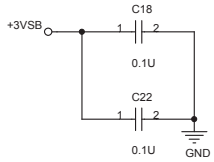
ASRock Computer Inc.	Title : ICH4-2	
	Engineer: Mars Tseng	
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 9 of 30	

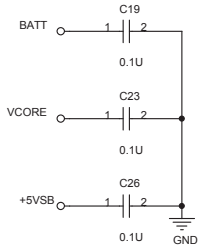


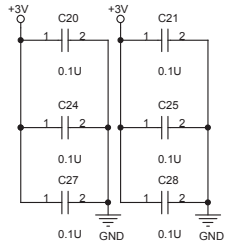


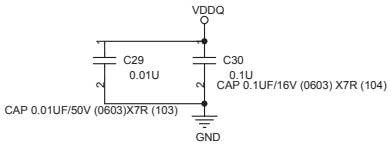


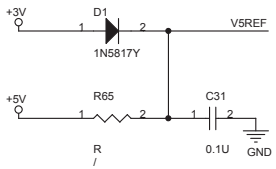








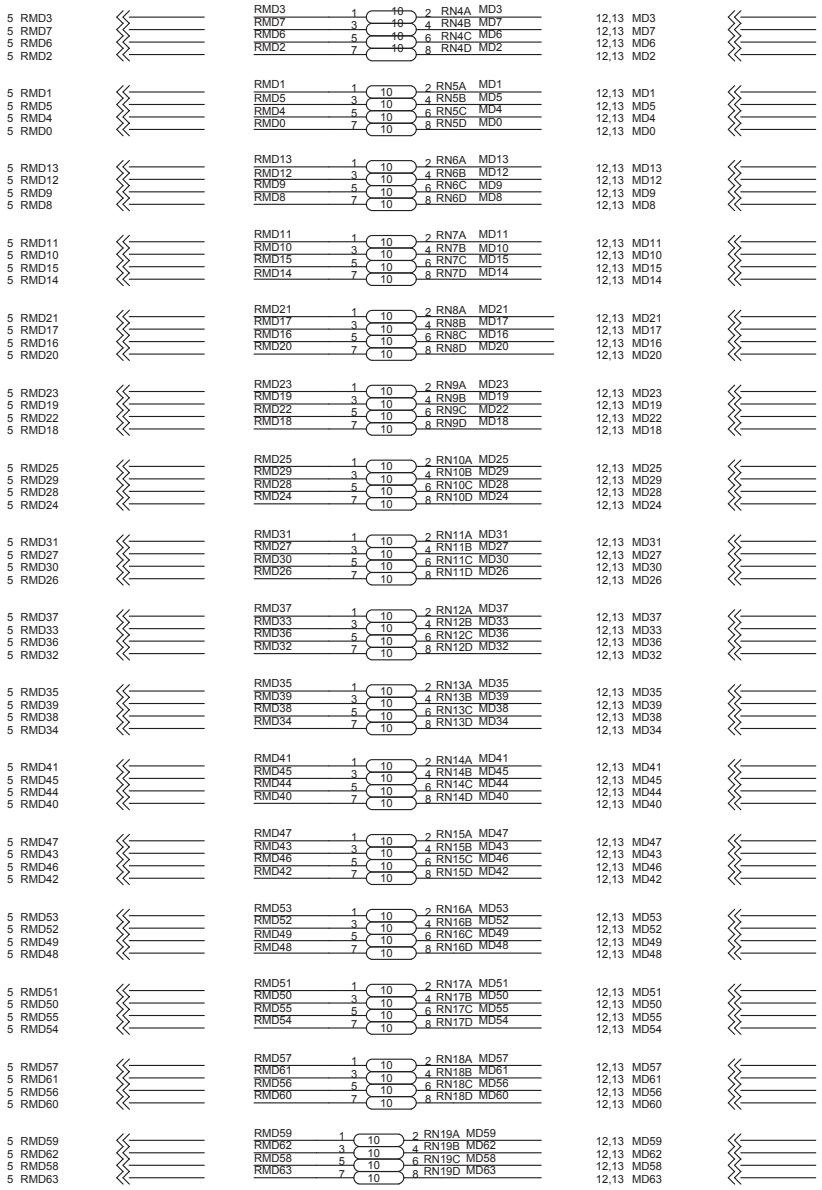


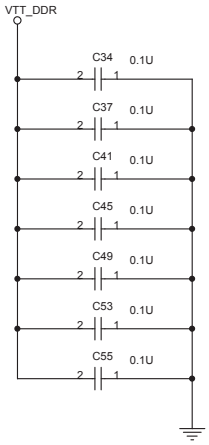


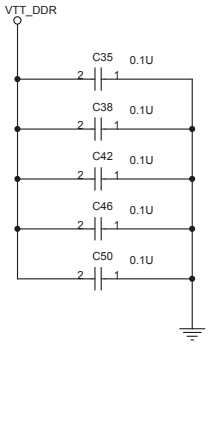
NOT

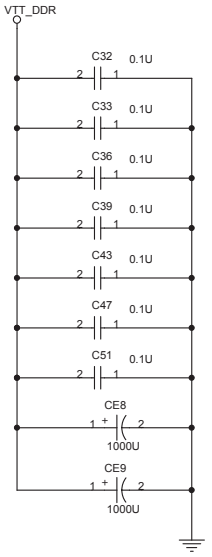
ASRock Computer Inc.	Title : ICH4-3	
	Engineer: Mars Tseng	
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 10 of 30	

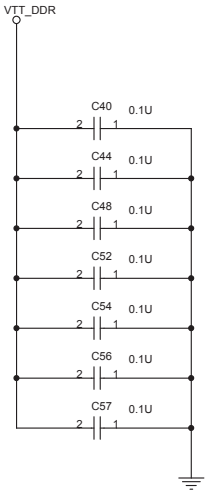
DDR Damping Resistor

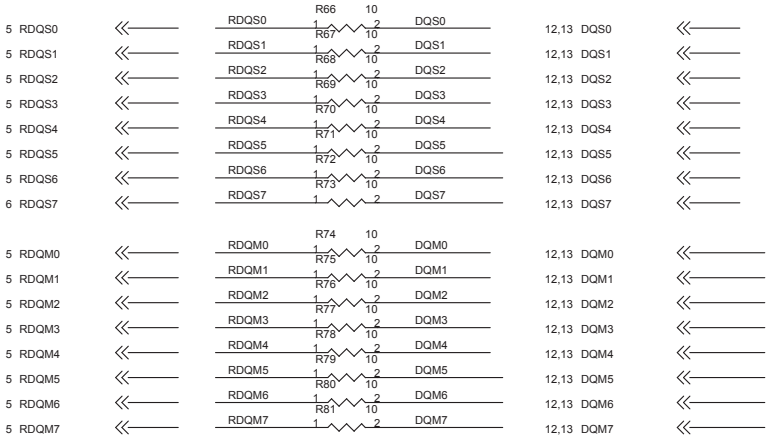






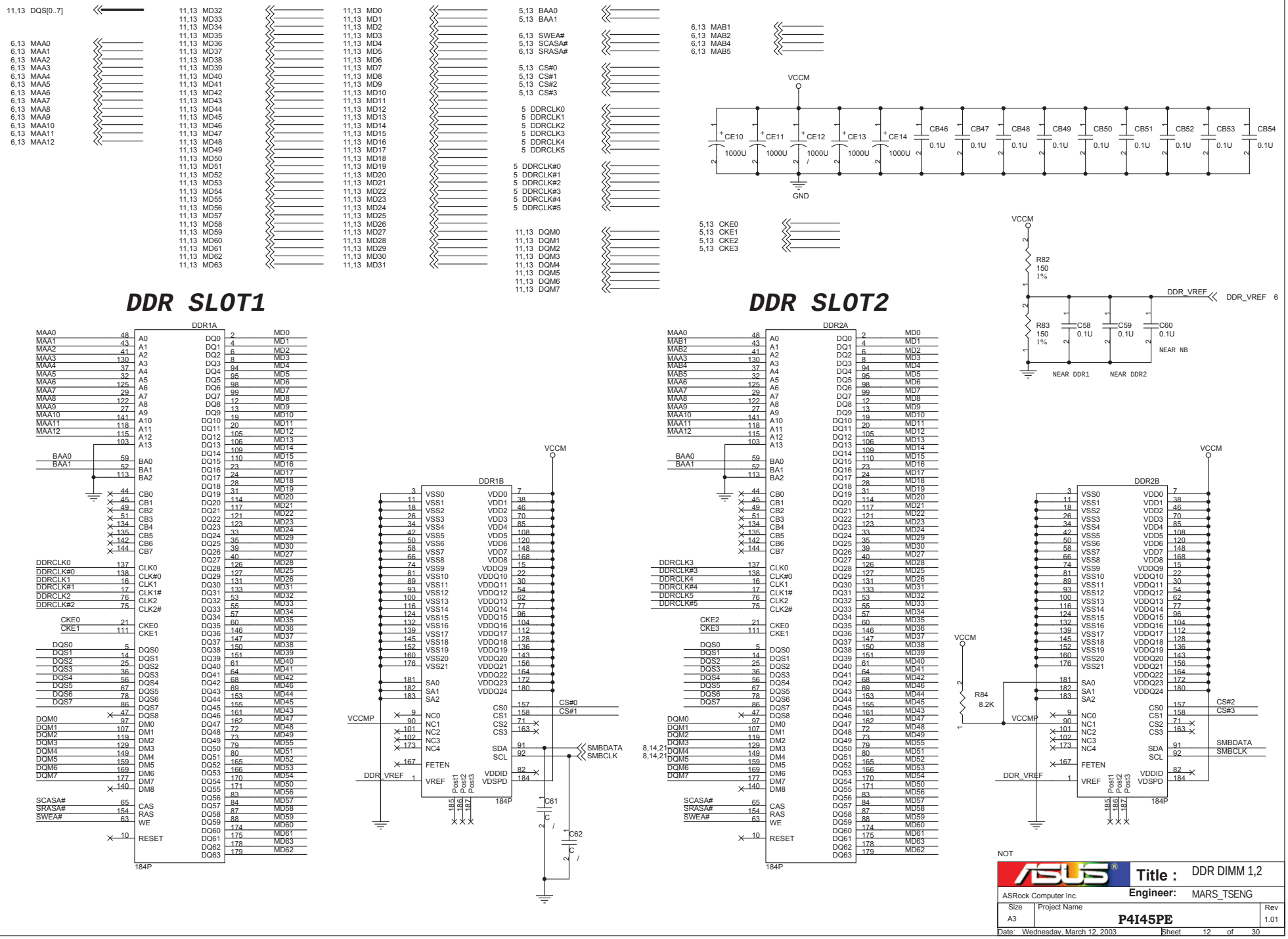


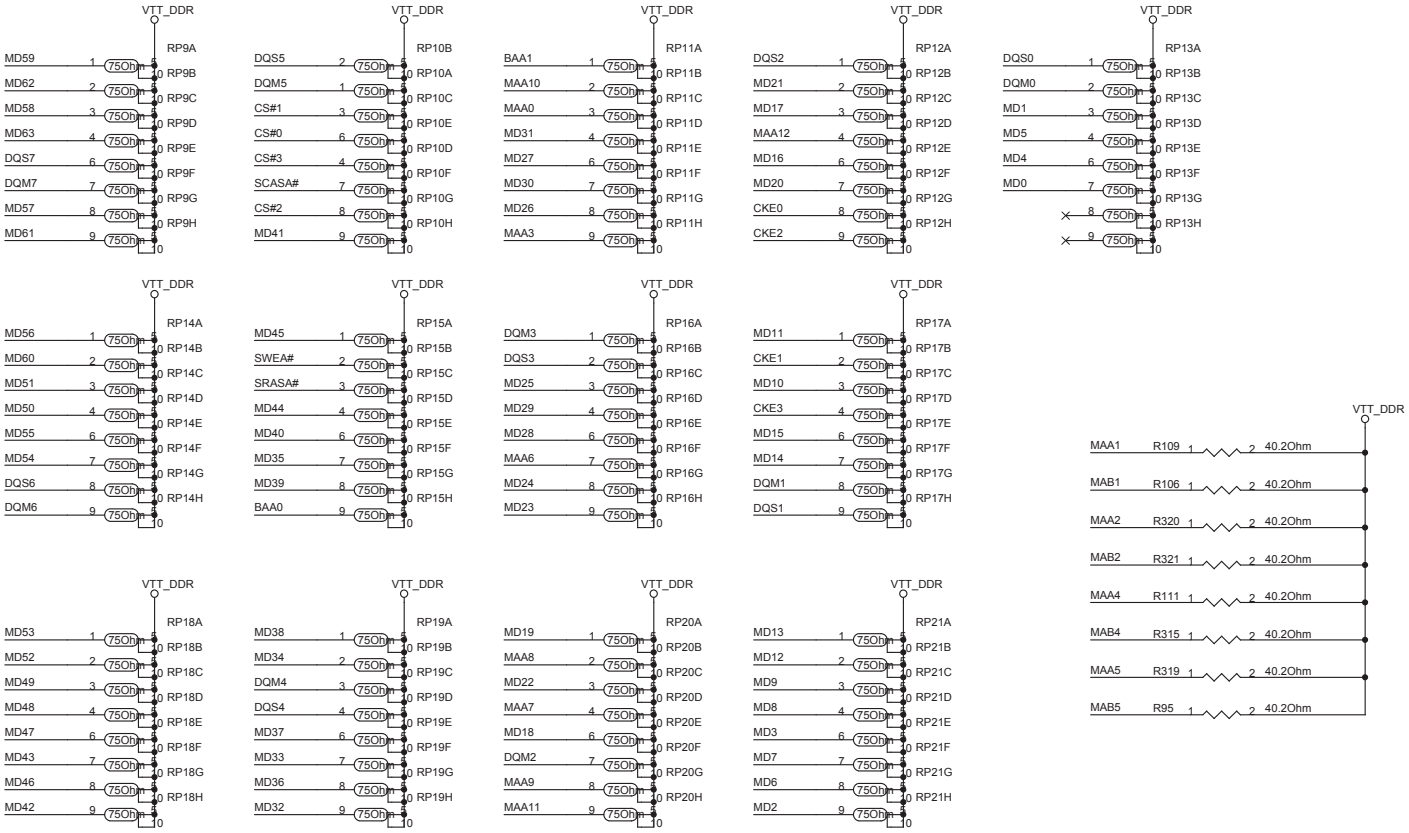




NOT

ASUS	Title :	DDR Damping
ASRock Computer Inc.	Engineer:	Mars Tseng
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 11 of 30	





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5,12 SCASA#
6,12 SRASA#

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11,12 DQM1
11,12 DQM2
11,12 DQM3
11,12 DQM4
11,12 DQM5
11,12 DQM6
11,12 DQM7

6,12 MAB1
6,12 MAB2
6,12 MAB4
6,12 MAB5

11,12 MD0
11,12 MD1
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11,12 MD61
11,12 MD62
11,12 MD63

5,12 CS#0
5,12 CS#1
5,12 CS#2
5,12 CS#3
5,12 CKE0
5,12 CKE1
5,12 CKE2
5,12 CKE3

6,12 MAA0
6,12 MAA1
6,12 MAA2
6,12 MAA3
6,12 MAA4
6,12 MAA5
6,12 MAA6
6,12 MAA7
6,12 MAA8
6,12 MAA9
6,12 MAA10
6,12 MAA11
6,12 MAA12

5,12 BAA0
5,12 BAA1

11,12 DQS[0..7]

NOT

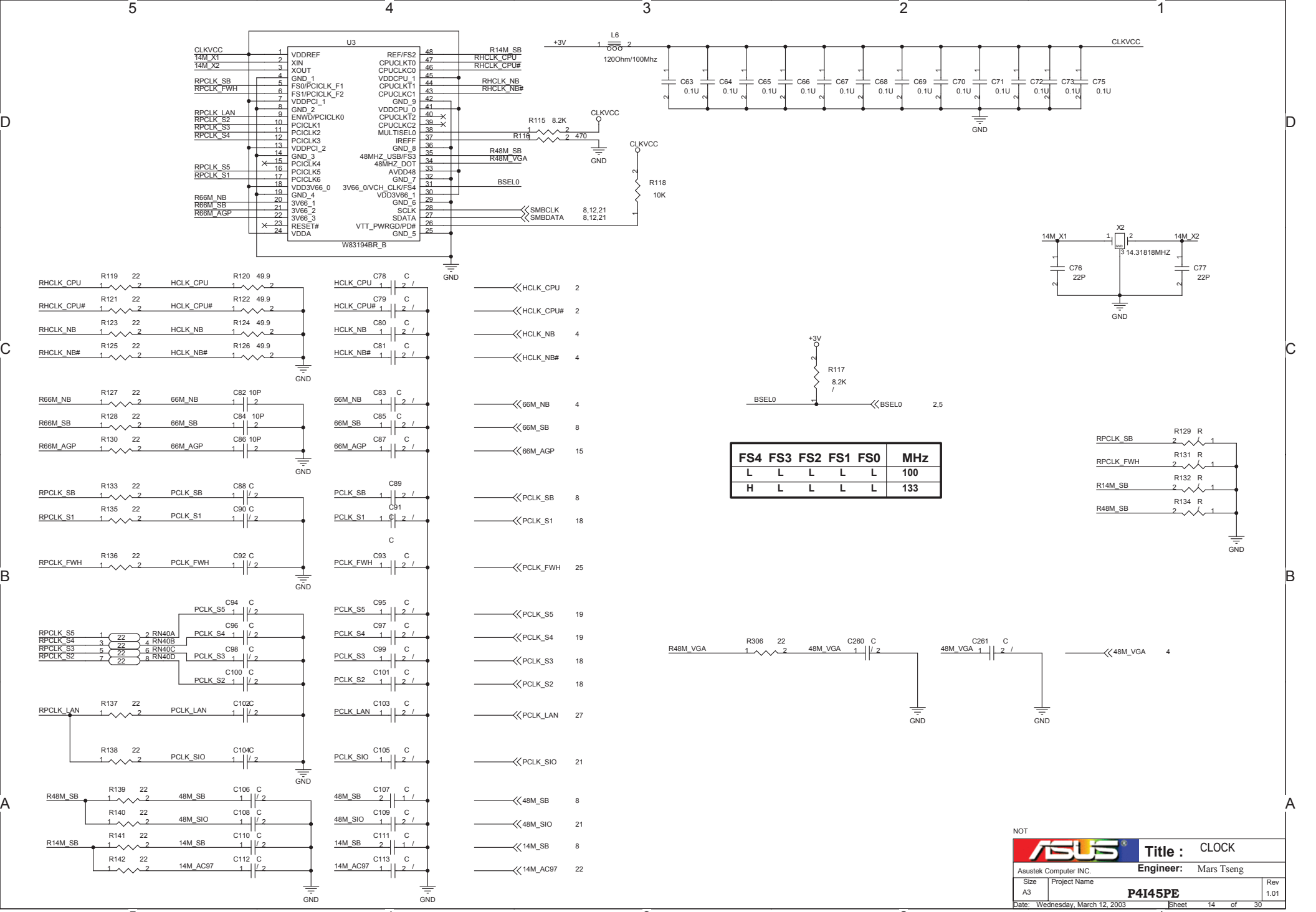
ASRock Computer Inc.

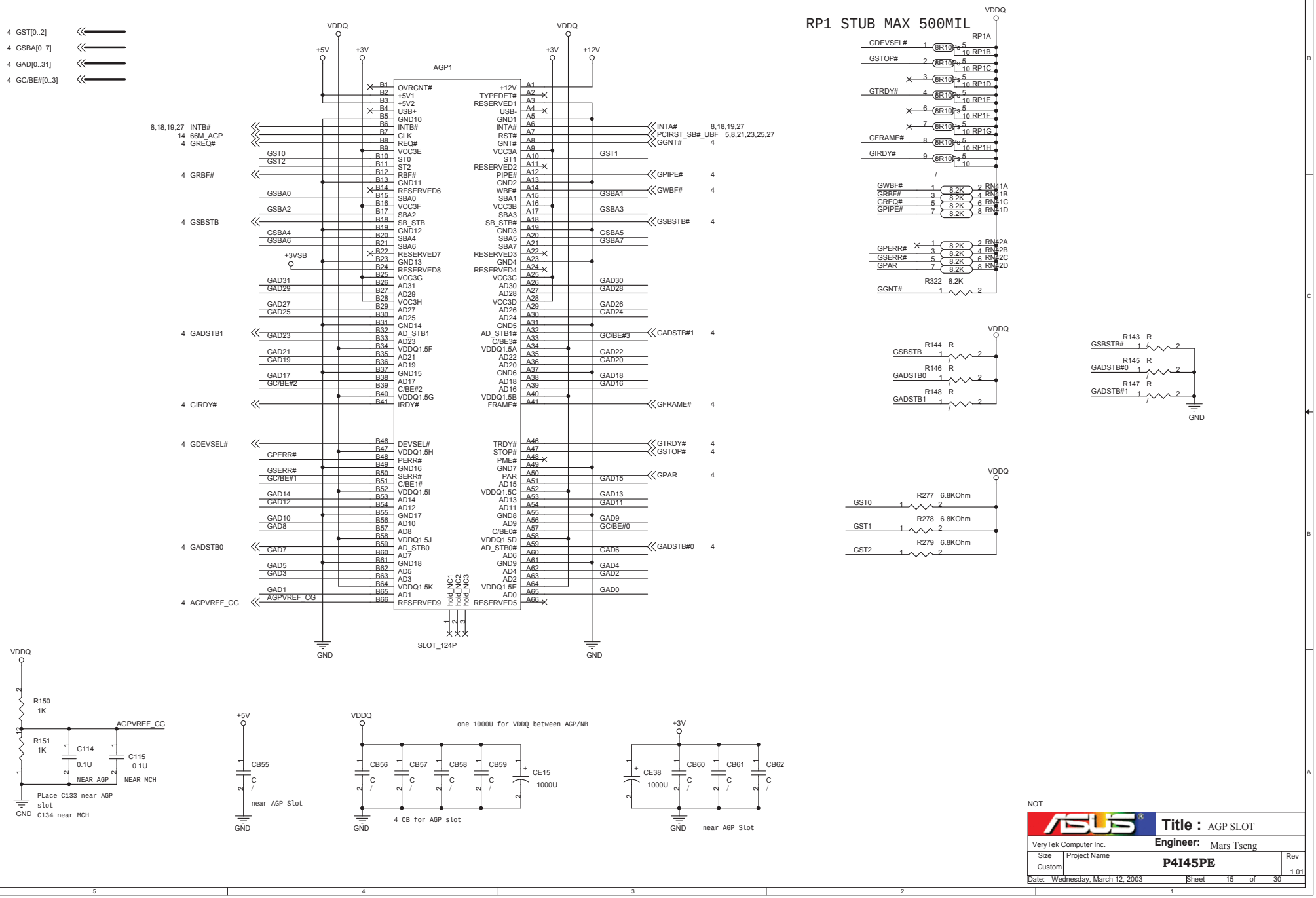
Title : DDR TERMINATION

Engineer: Mars Tseng

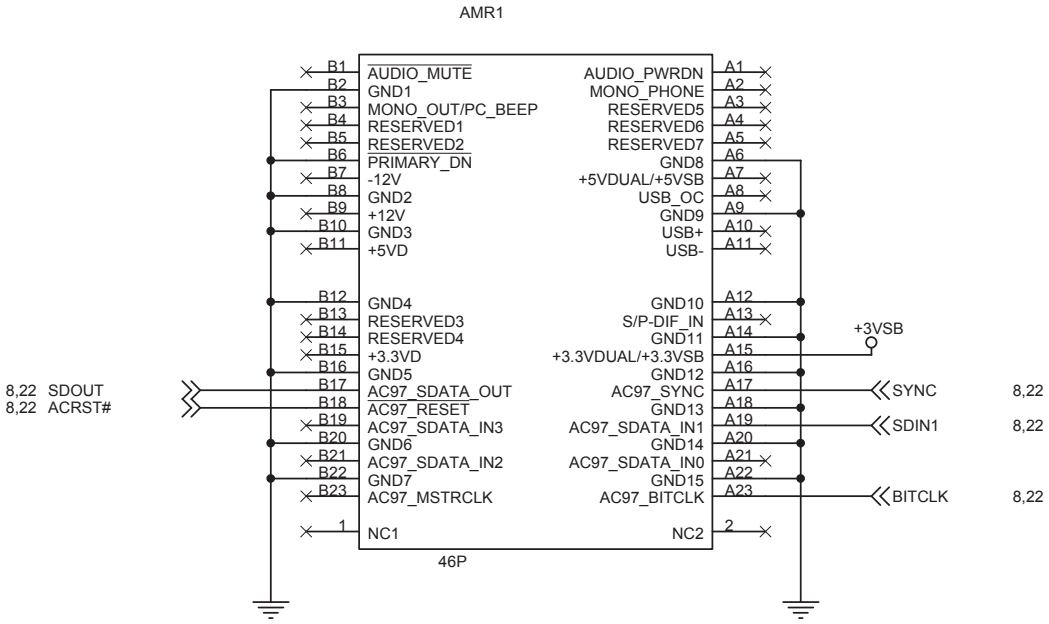
Size	Project Name	Rev
A3	P4I45PE	1.01

Date: Wednesday, March 12, 2003 Sheet 13 of 30





AMR SLOT

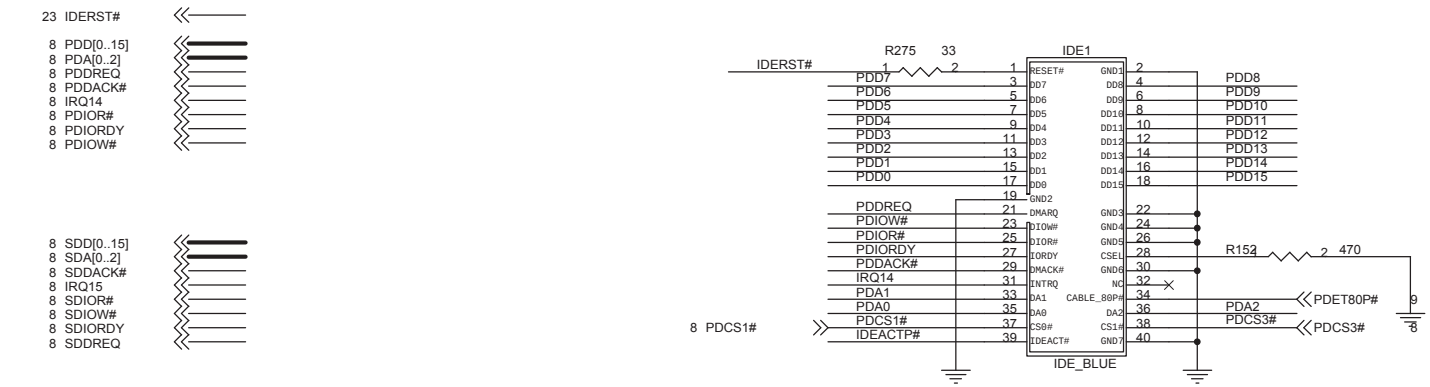


Note: This AMR Slot only support MODEM

NOT

ASRock Computer Inc.	Title : AMR SLOT	
	Engineer: Mars Tseng	
Size: A4	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 16 of 30	

IDE1



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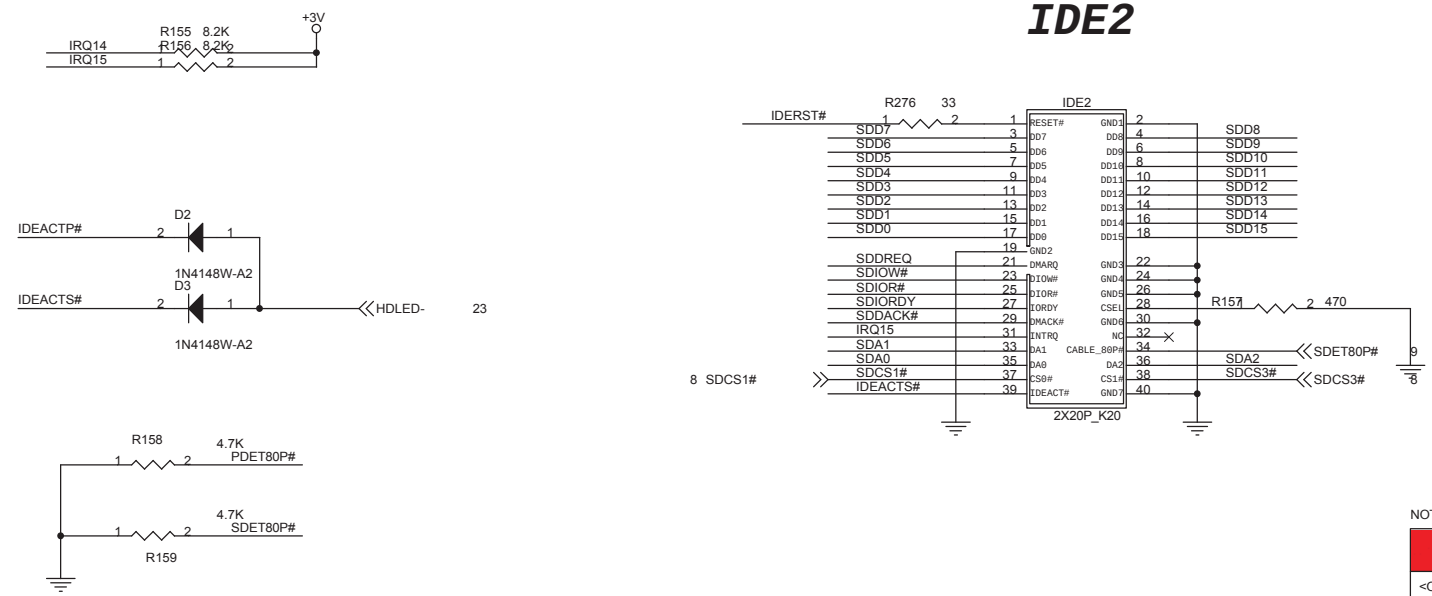


NOT

ASUS	Title :	IDE 1&2
<OrgName>	Engineer:	Mars Tseng
Size: Custom	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 17 of 30	

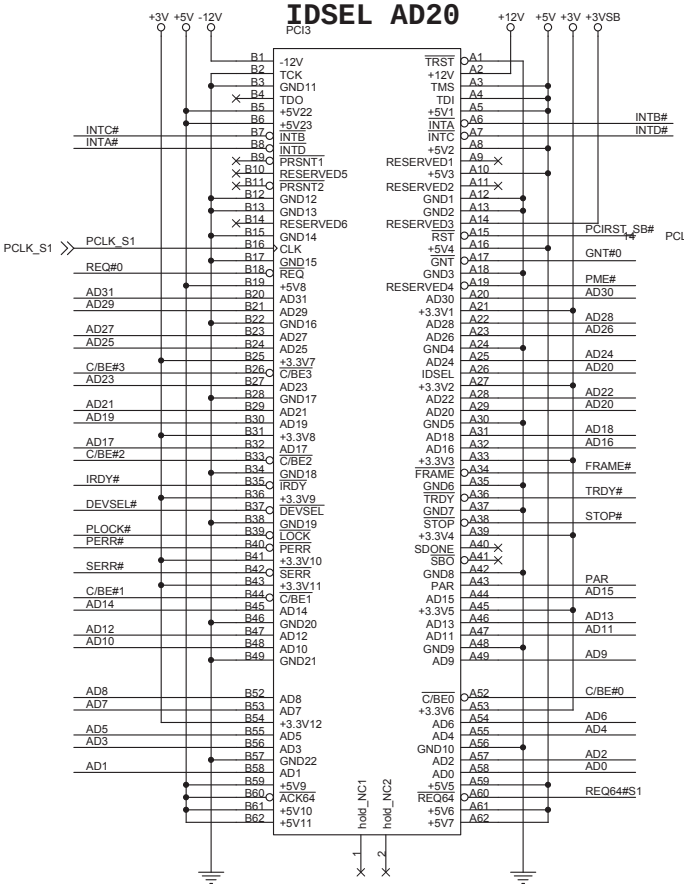
8,19,27 AD[0..31]
8,19,27 C/BE#[0..3]
19 REQ64#S[4..5]
8,19,27 DEVSEL#
8,19,27 IRDY#
8,19,27 STOP#
8,19,27 REQ#[0..5]
8,19,27 GNT#[0..5]

8,15,19,27 INTA#
8,15,19,27 INTB#
8,19 INTC#
8,19 INTD#
8,19,27 SERR#
8,19,27 PAR

8,19,27 PME#
19,23 PCIRST_SB#
8,19,27 FRAME#
8,19,27 TRDY#
8,19 PLOCK#
8,19,27 PERR#

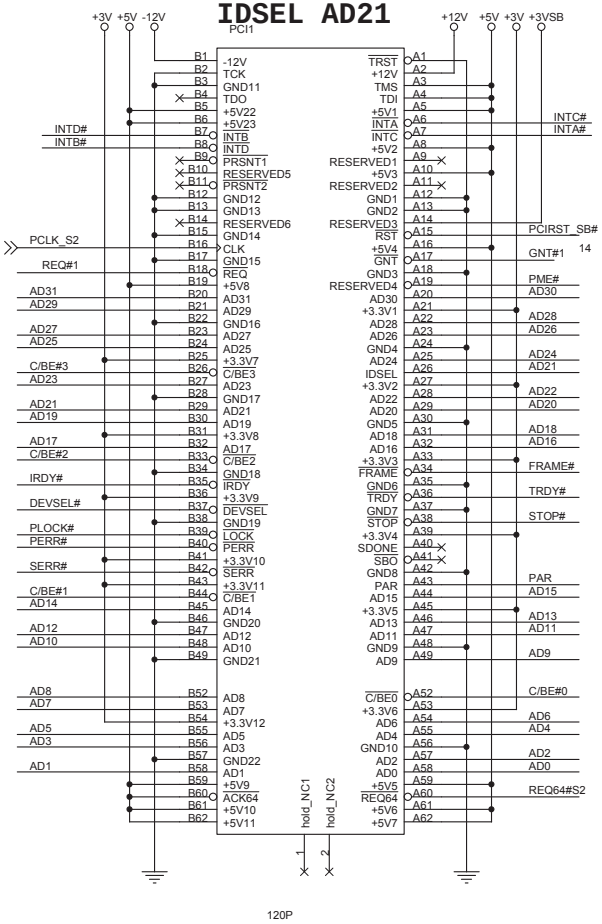
PCI SLOT1

BCDA
IDSEL AD20



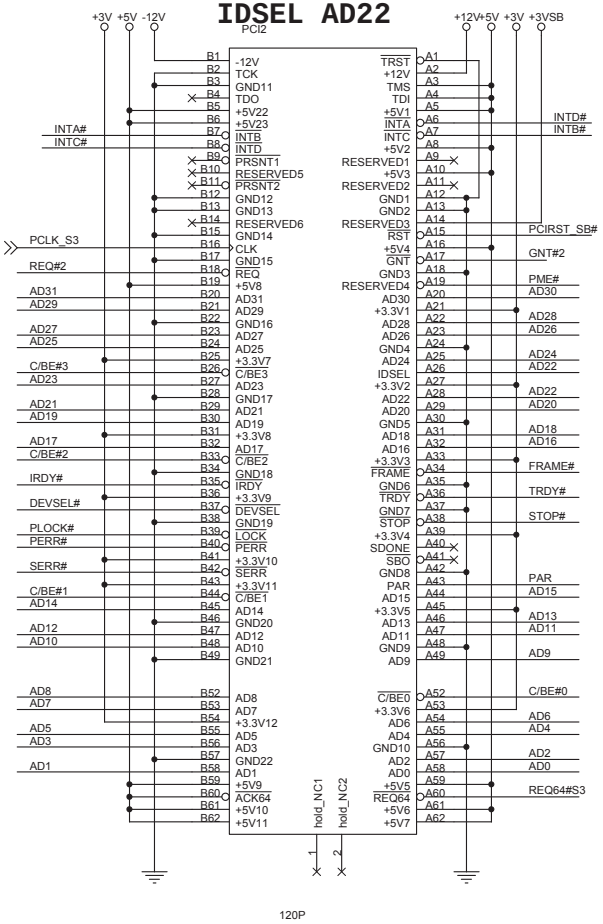
PCI SLOT2

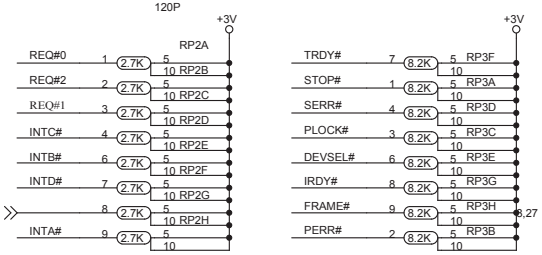
CDAB
IDSEL AD21

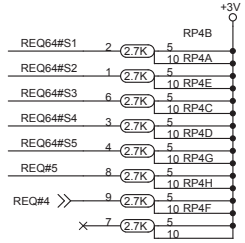


PCI SLOT3

DABC
IDSEL AD22







NOT

ASUS	Title : PCI SLOT 1,2,3	
<OrgName>	Engineer: Mars Tseng	
Size A3	Project Name P4I45PE	Rev 1.01
Date: Wednesday, March 12, 2003	Sheet 18 of 30	

8,18,27 AD[0..31]
8,18,27 C/BE#[0..3]
18 REQ64#S[4..5]
8,18,27 FRAME#
8,18,27 DEVSEL#
8,18,27 IRDY#
8,18,27 REQ#[0..5]
8,18,27 GNT#[0..5]

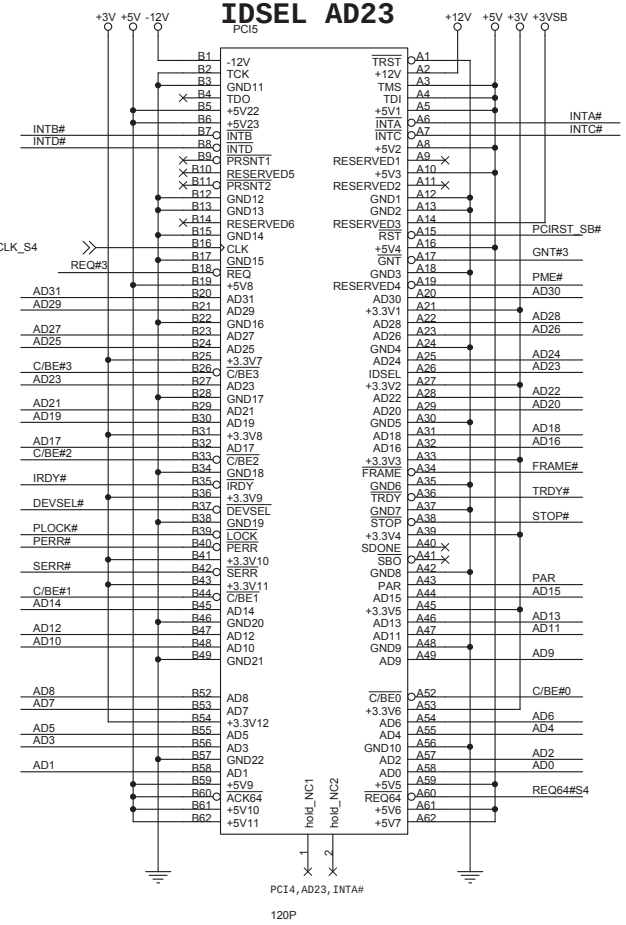
8,15,18,27 INTA#
8,15,18,27 INTB#
8,18 INTC#
8,18 INTD#
8,18,27 TRDY#
8,18 PLOCK#

8,18,27 PME#
18,23 PCIRST_SB#
8,18,27 SERR#
8,18,27 PAR
8,18,27 PERR#
8,18,27 STOP#

8 INTE#
8 INTF#
8 INTG#
8 INTH#

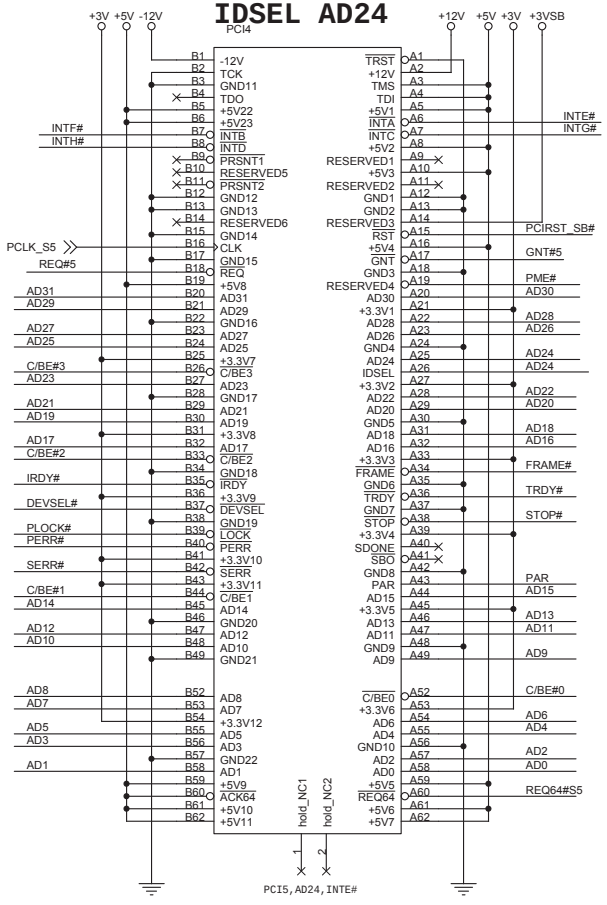
PCI SLOT4

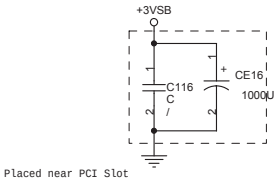
ABCD
IDSEL AD23

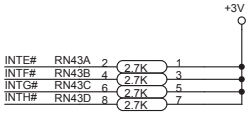


PCI SLOT5

EFGH
IDSEL AD24

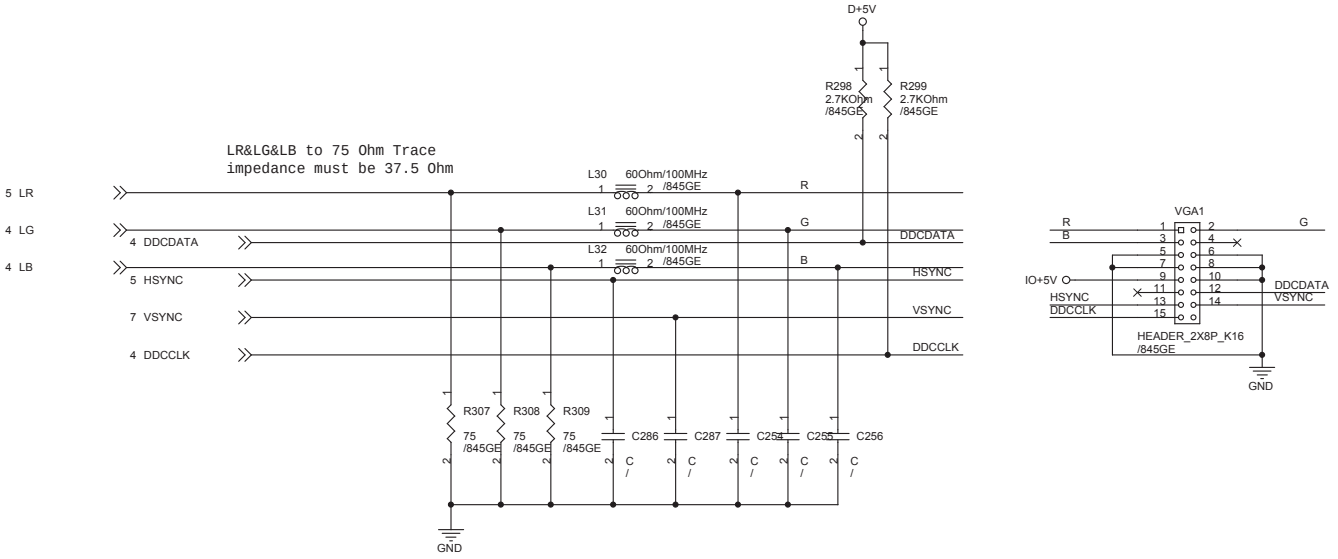






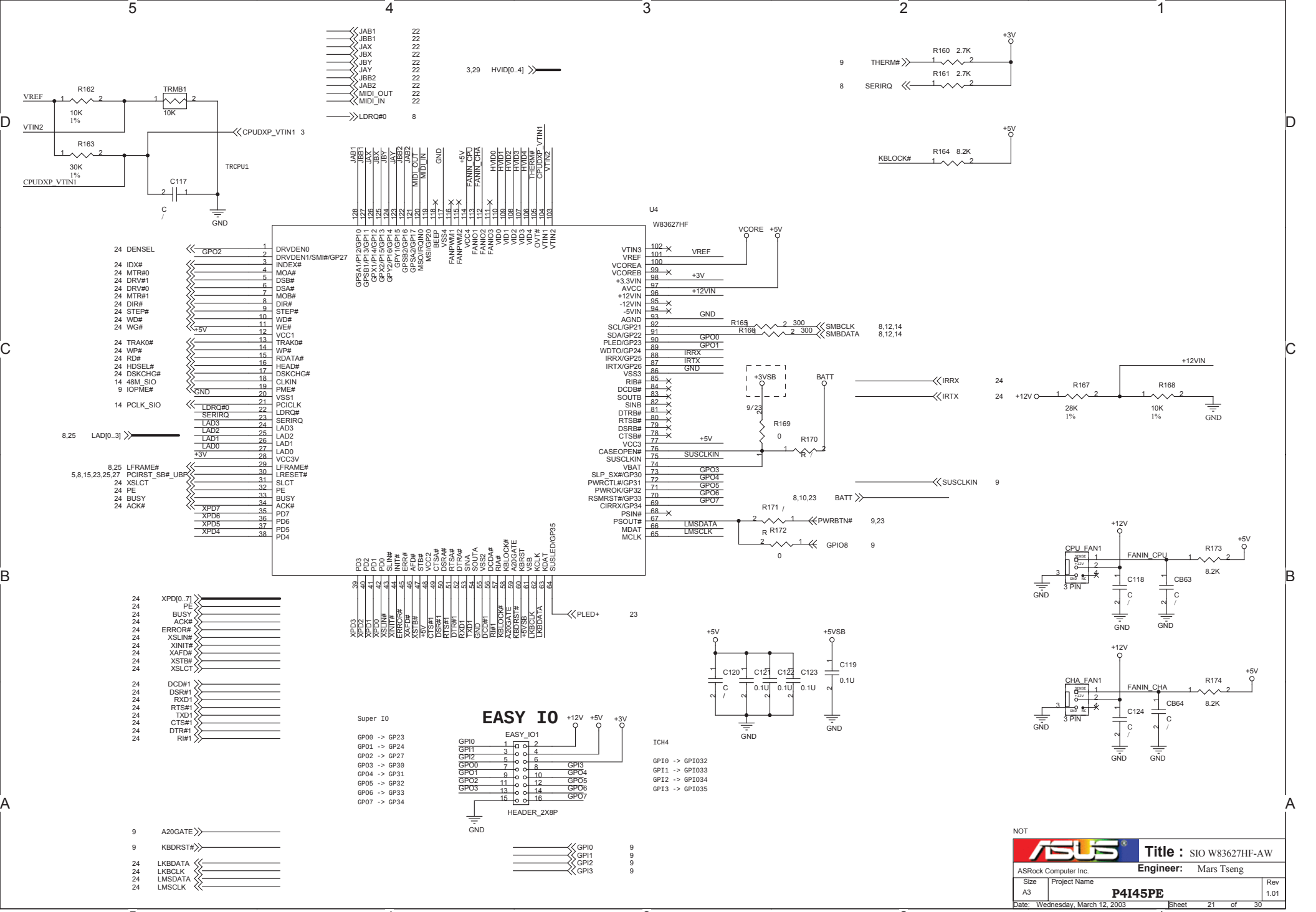
NOT

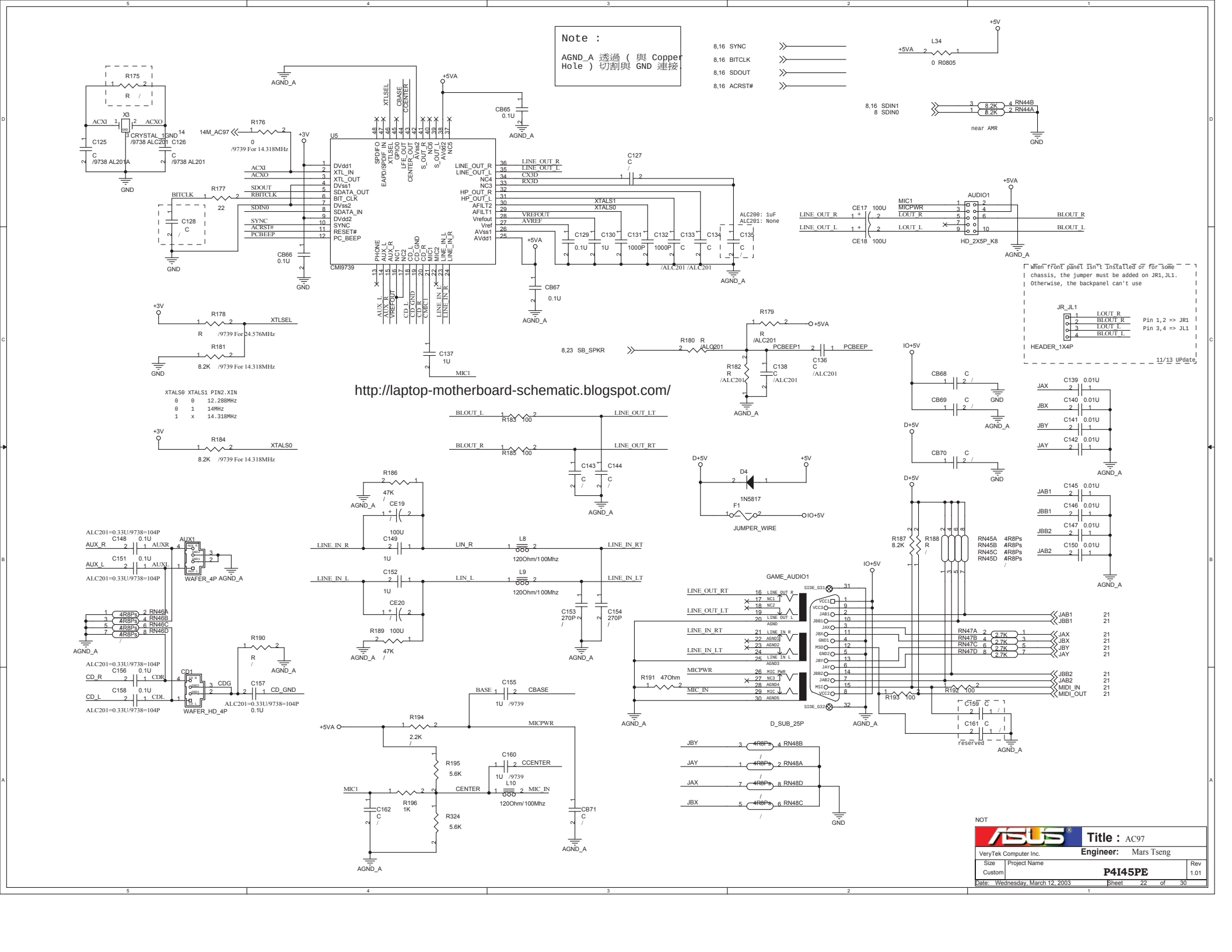
ASUS	Title :	PCI Slot 4,5
<OrgName>	Engineer:	Mars Tseng
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 19 of 30	

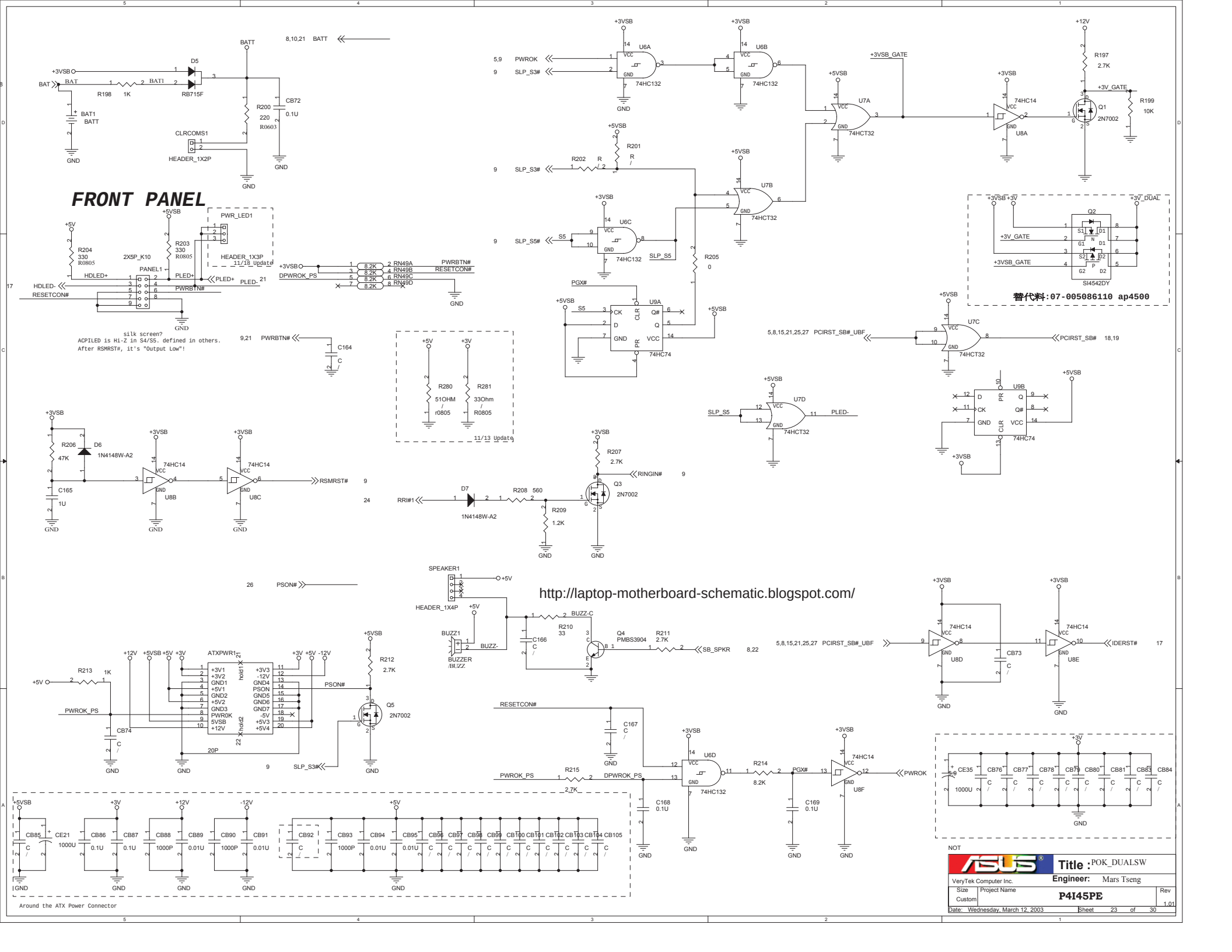


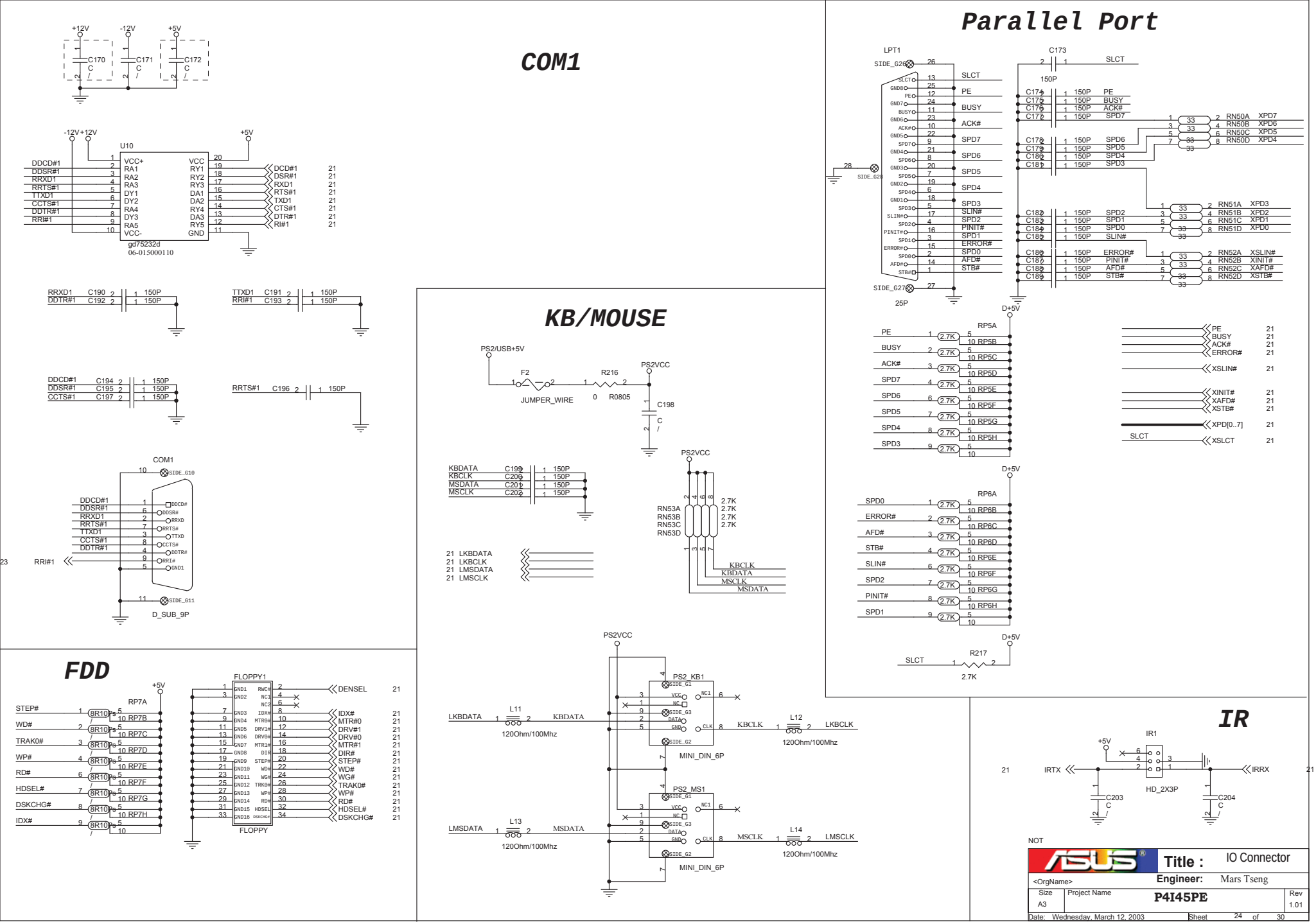
NOT

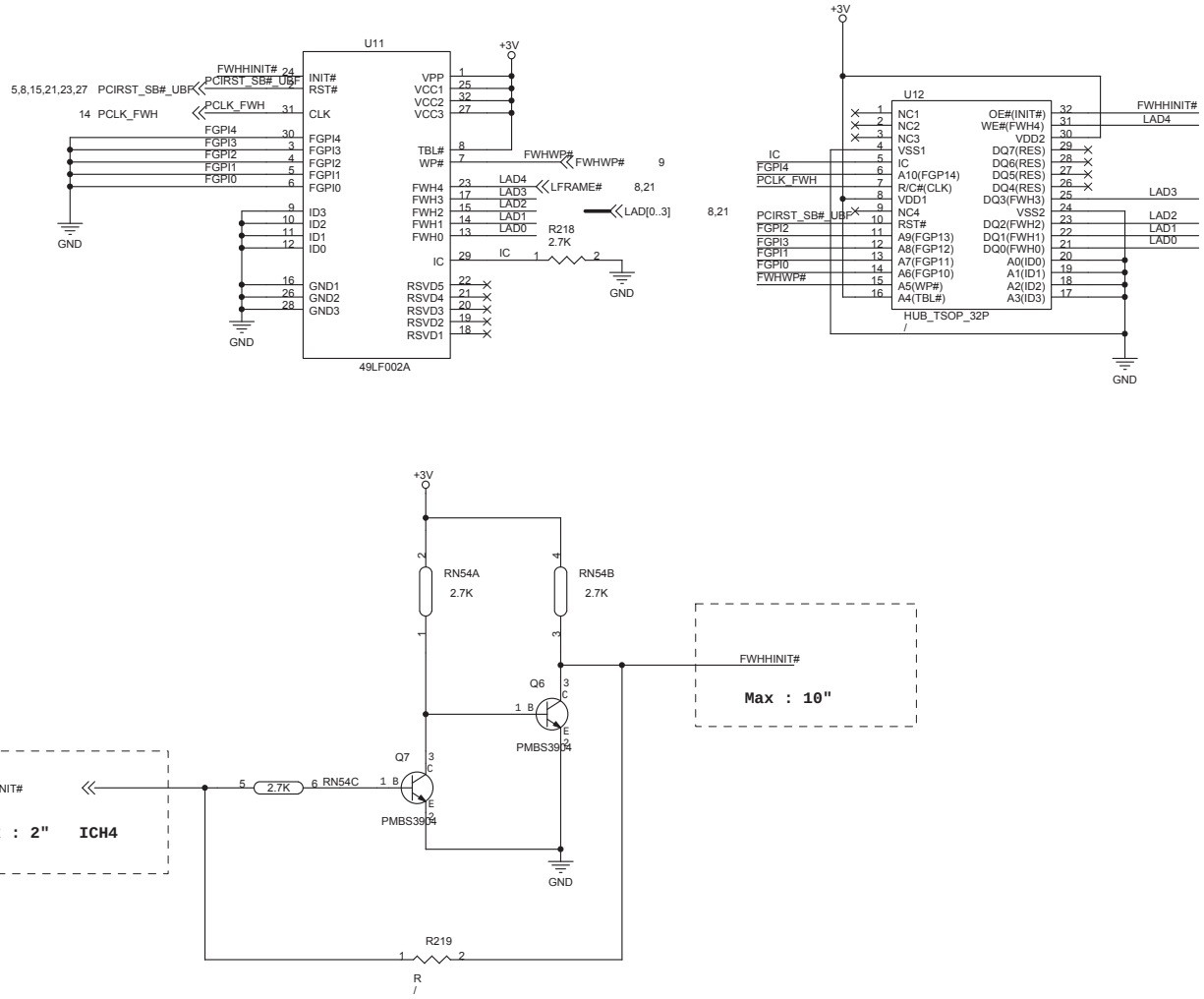
ASRock Computer Inc.	Title : VGA CONNECTOR	
	Engineer: MARS_TSENG	
Size: A3	Project Name: P4I45GL	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 20 of 30	




Note :
AGND_A 透過 (與 Copper Hole) 切割與 GND 連接.
8,16 SYNC
8,16 BITCLK
8,16 SDOUT
8,16 ACRST#
8,16 SDIN1
8 SDIN0
8,23 SB_SPKR
CMI9739
U5
http://laptop-motherboard-schematic.blogspot.com/
XTALS0 XTALS1 PIN2.XIN
0 0 12.288MHz
0 1 14MHz
1 x 14.318MHz
ALC200: 1uF
ALC201: None
When front panel isn't installed or for some chassis, the jumper must be added on JR1,JL1. Otherwise, the backpanel can't use
JR_JL1
HEADER_1X4P
11/13 UPdate
GAME_AUDIO1
D_SUB_25P
JUMPER_WIRE
Title : AC97
VeryTek Computer Inc.
Engineer: Mars Tseng
Project Name
P4I45PE
Rev 1.01
Date: Wednesday, March 12, 2003
Sheet 22 of 30

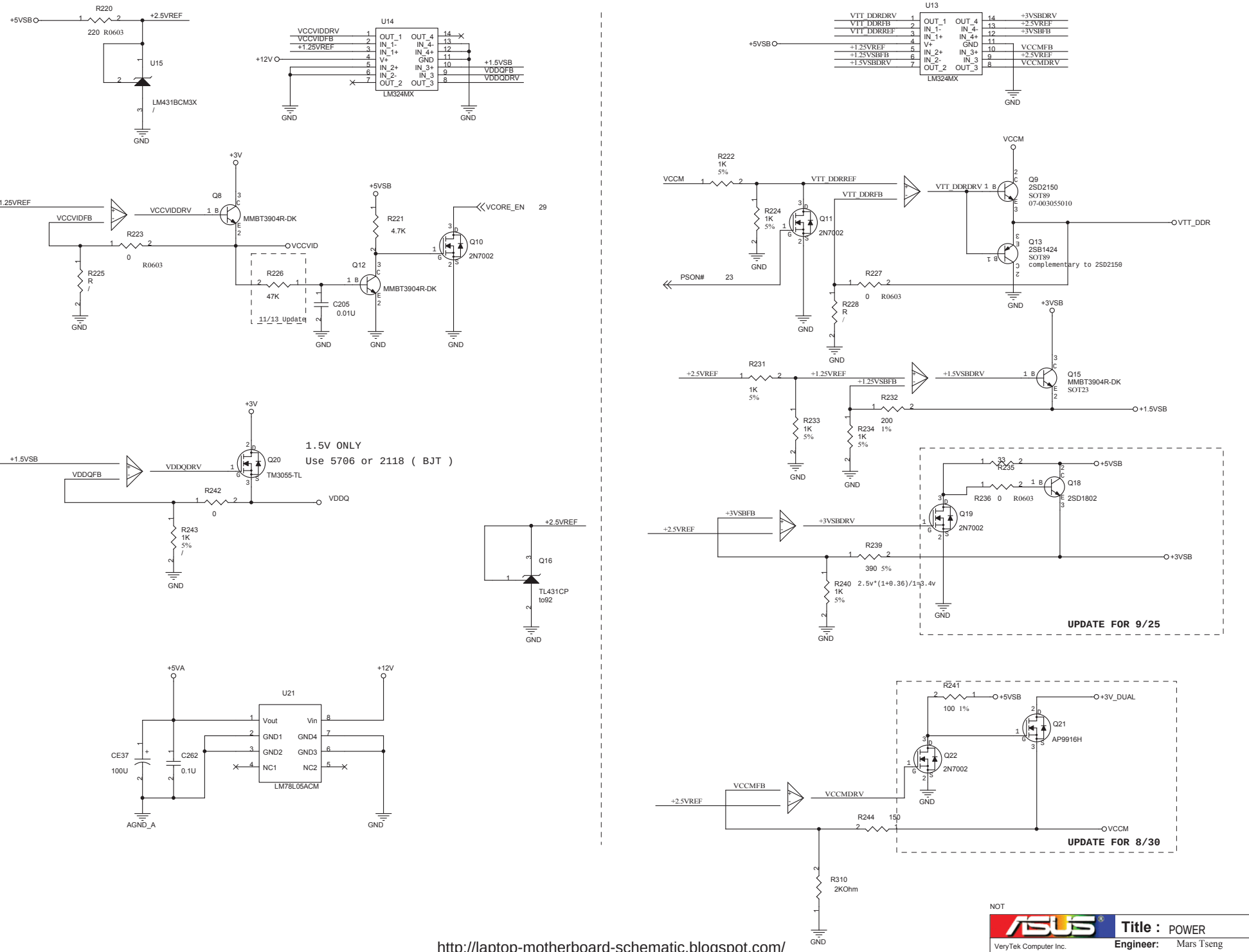

FRONT PANEL
silk screen?
ACPILED is Hi-Z in S4/S5. defined in others.
After RSMRST#, it's "Output Low"!
11/13 Update
http://laptop-motherboard-schematic.blogspot.com/
替代料:07-005086110 ap4500
Around the ATX Power Connector
Title : POK_DUALSW
VeryTek Computer Inc.
Engineer: Mars Tseng
Size: Custom
Project Name: P4I45PE
Rev: 1.01
Date: Wednesday, March 12, 2003
Sheet 23 of 30





NOT

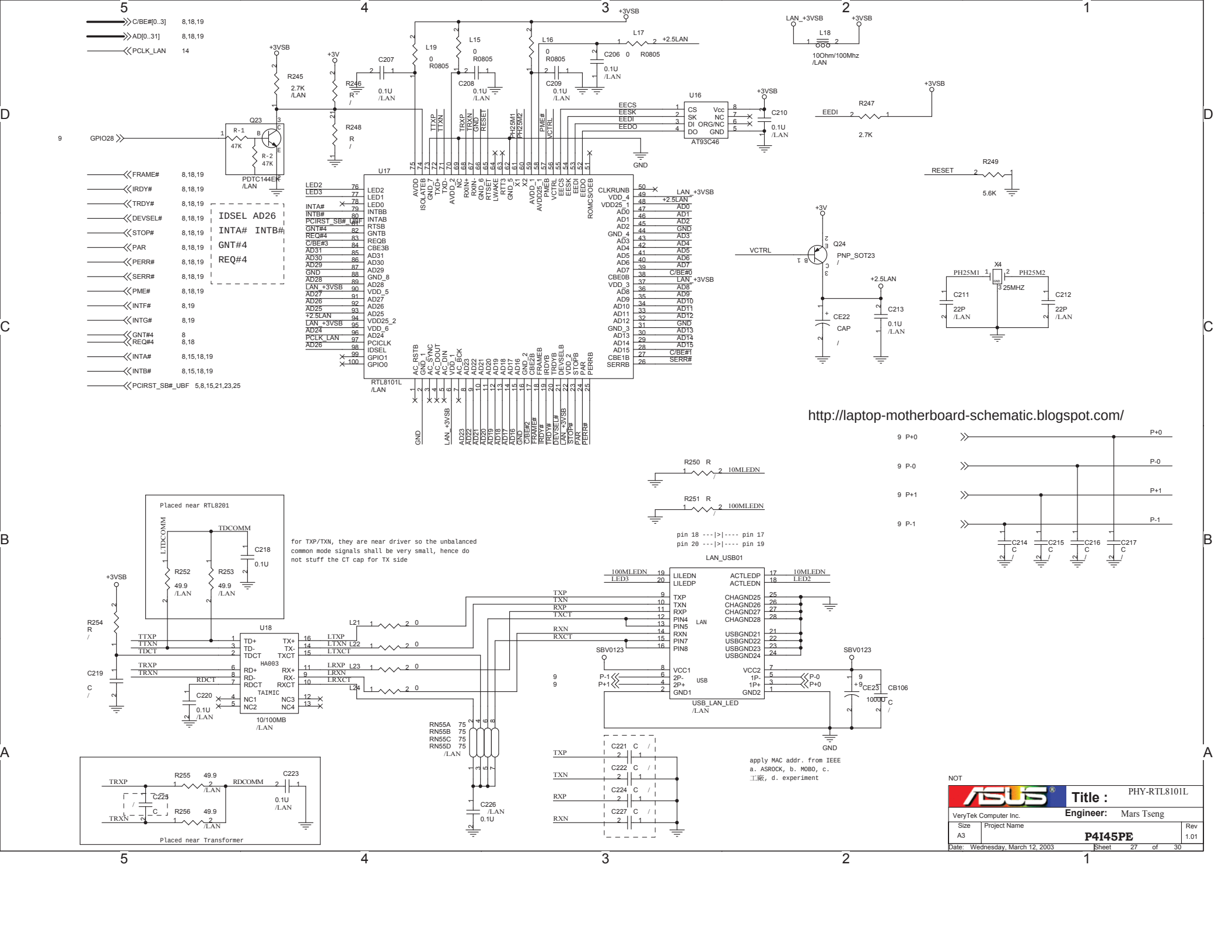
ASRock Computer Inc.	Title : FWH	
	Engineer: Mars Tseng	
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 25 of 30	

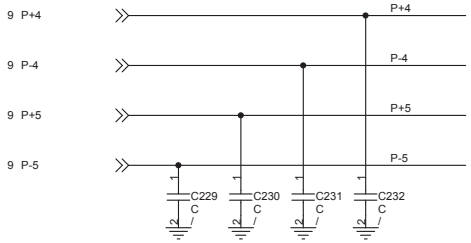


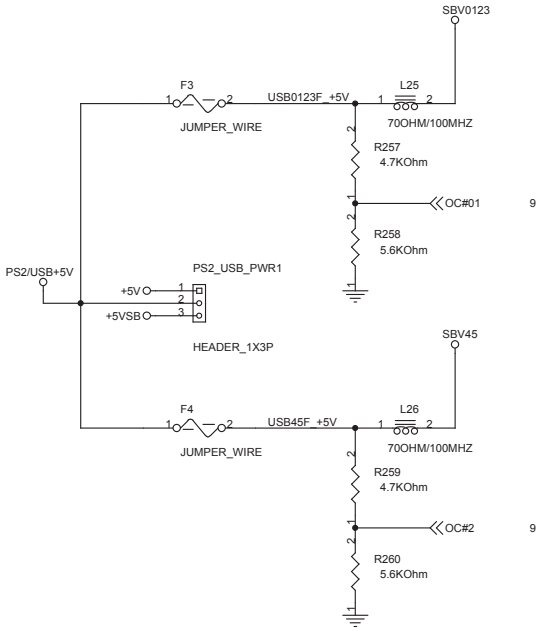
http://laptop-motherboard-schematic.blogspot.com/

NOT

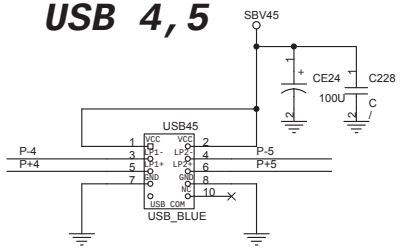
ASUS	Title : POWER	
VeryTek Computer Inc.	Engineer: Mars Tseng	
Size: Custom	Project Name: P4I45PE	Rev: 1.01
Date: Thursday, March 13, 2003	Sheet 26 of 30	

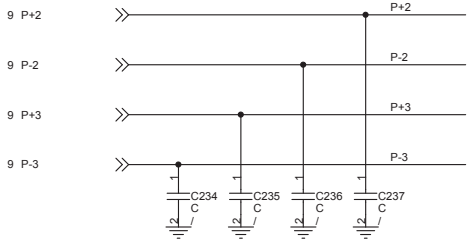

C/BE#[0..3] 8,18,19
AD[0..31] 8,18,19
PCLK_LAN 14
GPIO28
FRAME# 8,18,19
IRDY# 8,18,19
TRDY# 8,18,19
DEVSEL# 8,18,19
STOP# 8,18,19
PAR 8,18,19
PERR# 8,18,19
SERR# 8,18,19
PME# 8,18,19
INTF# 8,19
INTG# 8,19
GNT#4 8
REQ#4 8,18
INTA# 8,15,18,19
INTB# 8,15,18,19
PCIRST_SB#_UBF 5,8,15,21,23,25
IDSEL AD26
INTA# INTB#
GNT#4
REQ#4
U17
RTL8101L
/LAN
U16
AT93C46
Q23
Q24
PNP_SOT23
U18
HA003
TAIMIC
10/100MB
/LAN
LAN_USB01
USB_LAN_LED
/LAN
X4
25MHZ
Placed near RTL8201
Placed near Transformer
for TXP/TXN, they are near driver so the unbalanced
common mode signals shall be very small, hence do
not stuff the CT cap for TX side
pin 18 ---|>|---- pin 17
pin 20 ---|>|---- pin 19
apply MAC addr. from IEEE
a. ASROCK, b. MOBO, c.
工廠, d. experiment
http://laptop-motherboard-schematic.blogspot.com/
NOT
Title : PHY-RTL8101L
VeryTek Computer Inc.
Engineer: Mars Tseng
Size A3
Project Name P4I45PE
Rev 1.01
Date: Wednesday, March 12, 2003
Sheet 27 of 30



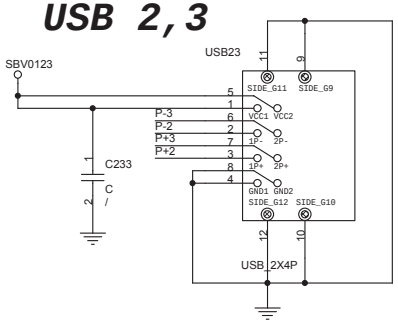


USB 4,5



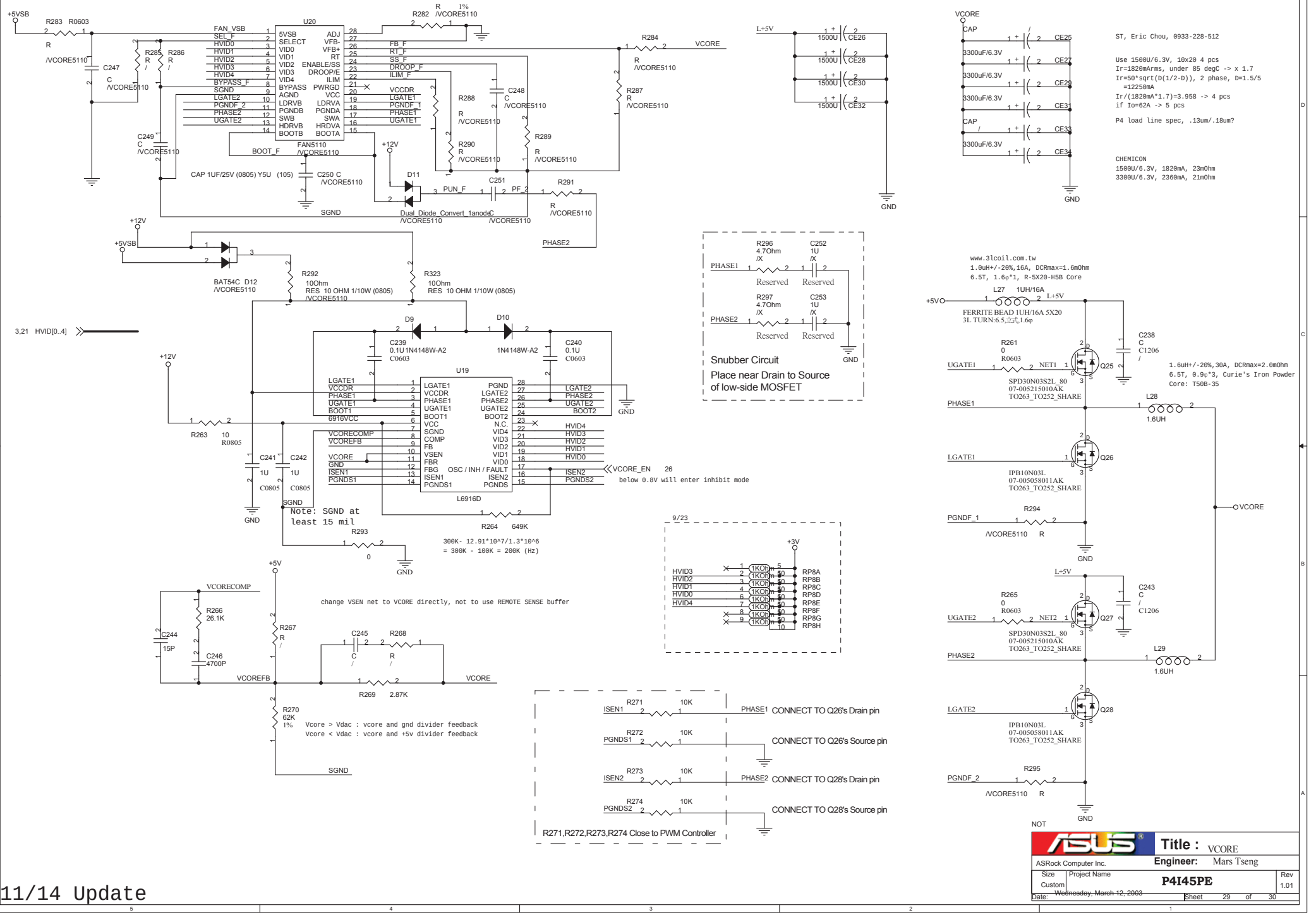


USB 2,3

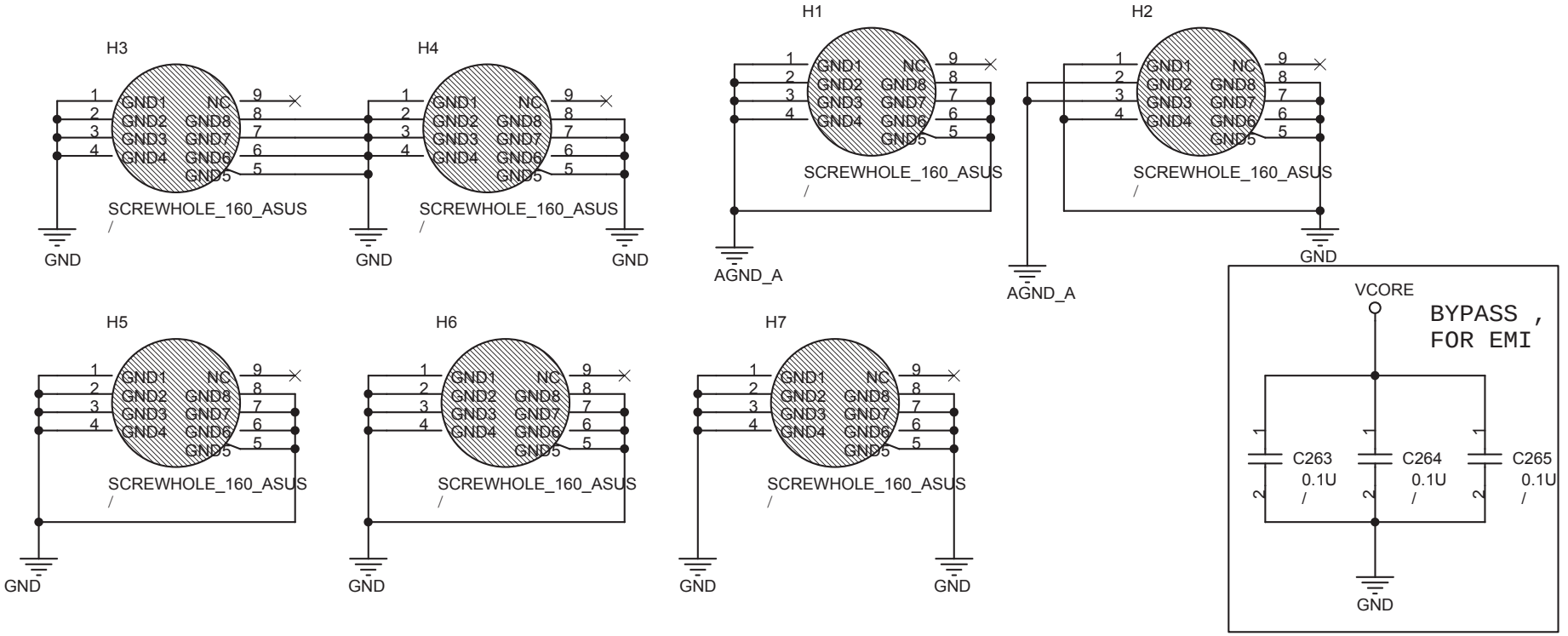


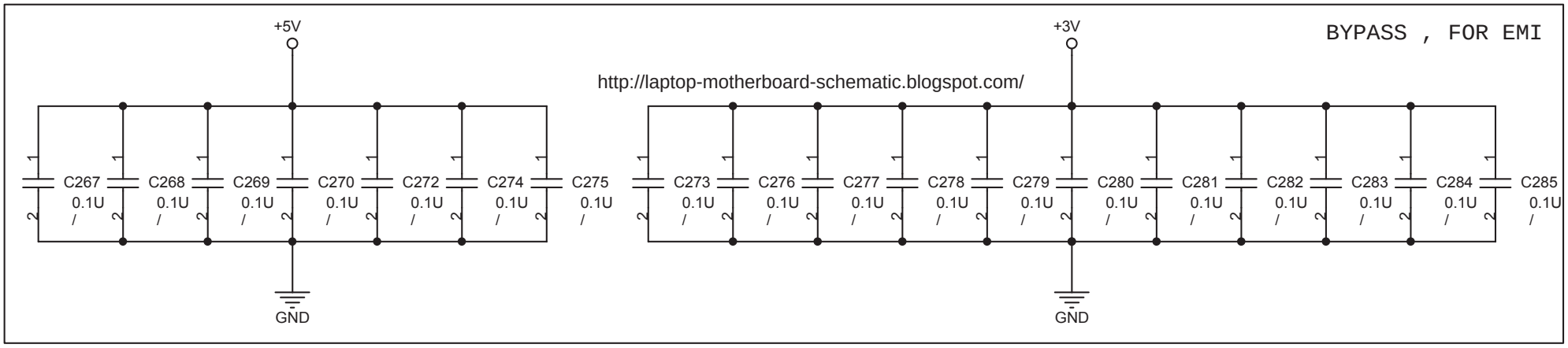
NOT

ASRock Computer Inc.	Title : USB PORT	
	Engineer: Mars Tseng	
Size: A3	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 28 of 30	



11/14 Update





NOT

Verytek Computer Inc.	Title : MECHANICAL Engineer: Mars Tseng	
Size: A	Project Name: P4I45PE	Rev: 1.01
Date: Wednesday, March 12, 2003	Sheet 30 of 30	