INTEL 845GL Preliminary Customer Reference Schematics

Revision 1.00

NOT

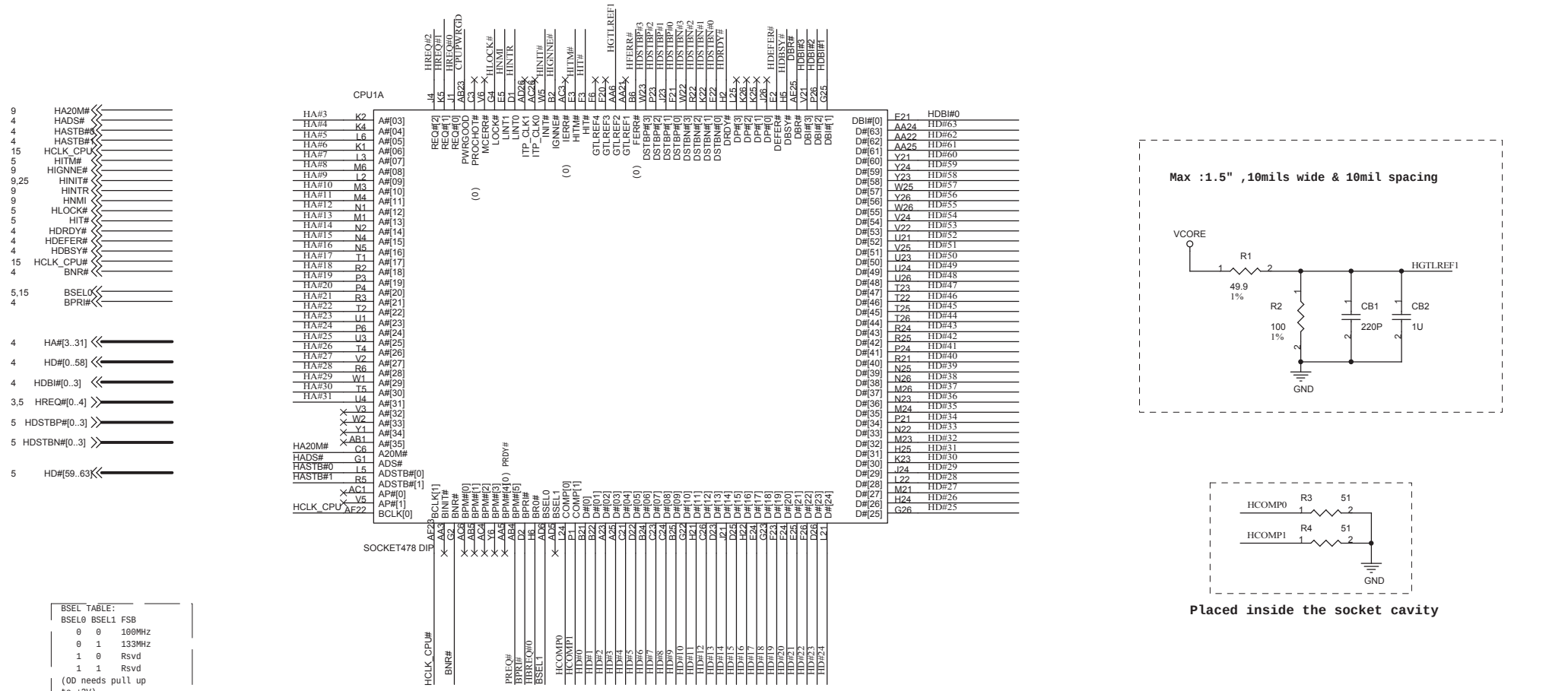
ASUS

Title : COVER SHEET

ASRock Computer Inc. Engineer: MARS_TSENG

Size	Project Name	Rev
Custom	P4I45GL	1.00

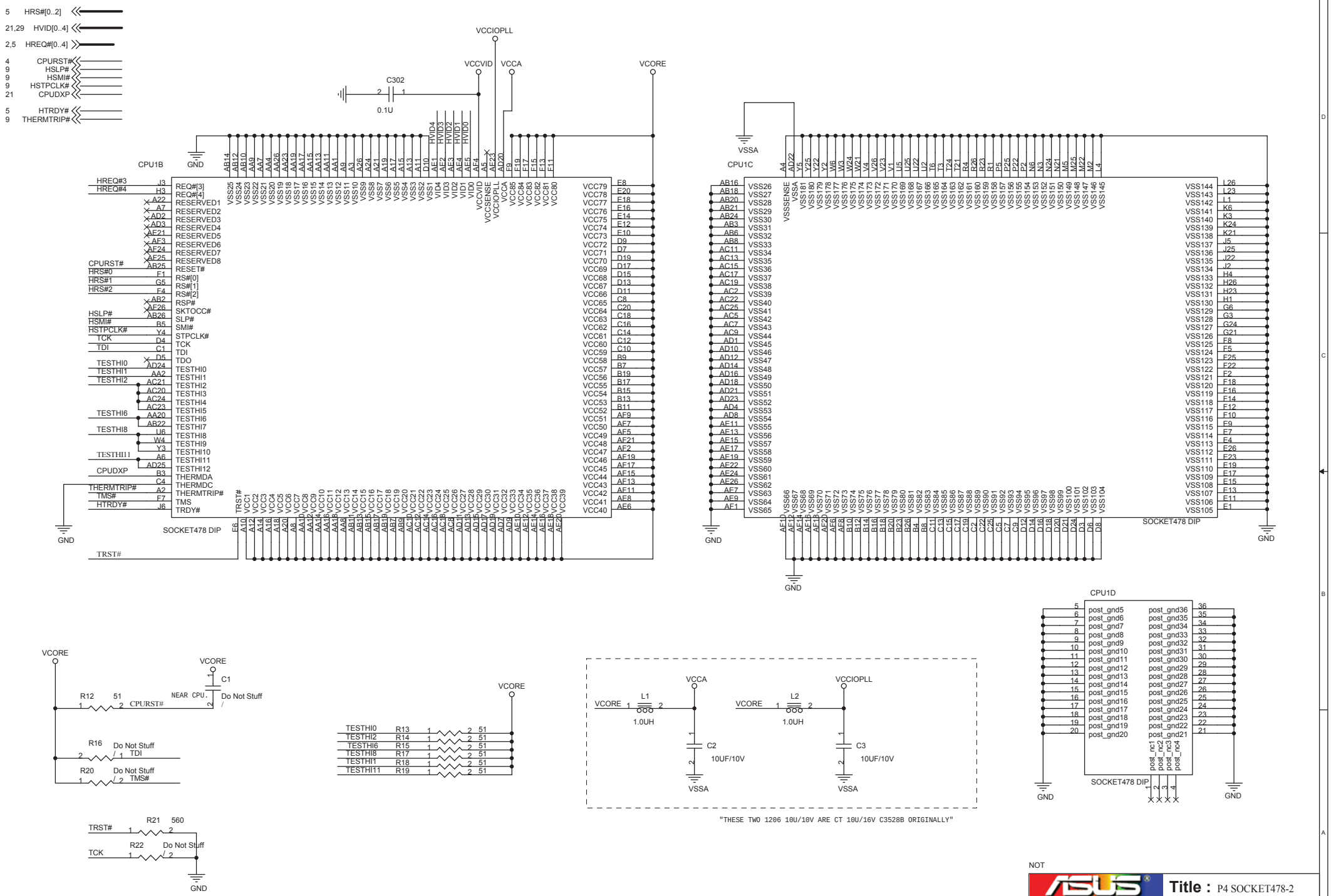
Date: Friday, January 17, 2003 Sheet 1 of 31



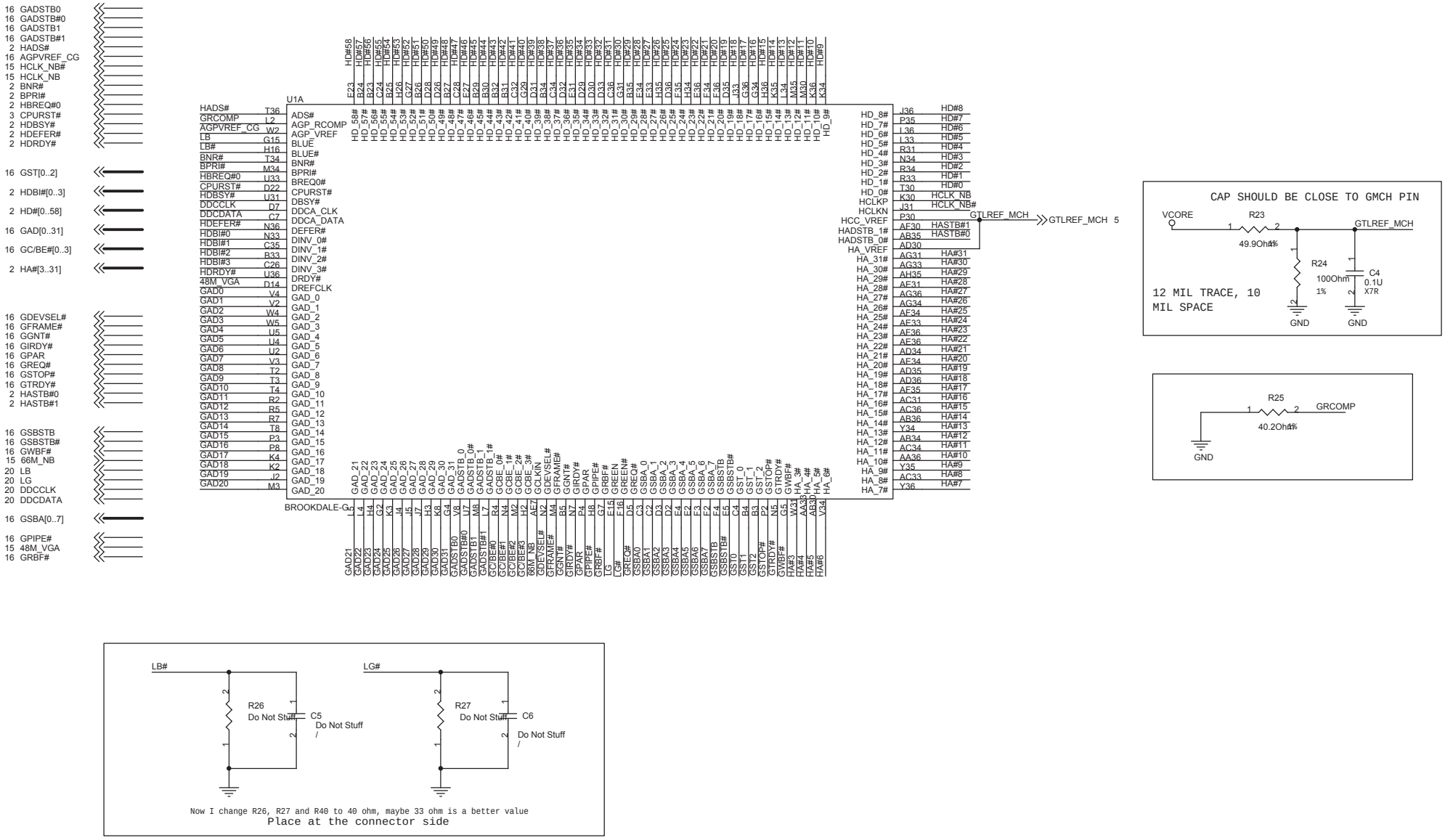
http://laptop-motherboard-schematic.blogspot.com/

NOT

ASUS	Title : P4 SOCKET478-1	
ASRock Computer Inc.	Engineer: MARS_TSENG	
Size A3	Project Name P4I45GL	Rev 1.00
Date: Friday, January 17, 2003	Sheet 2 of 31	

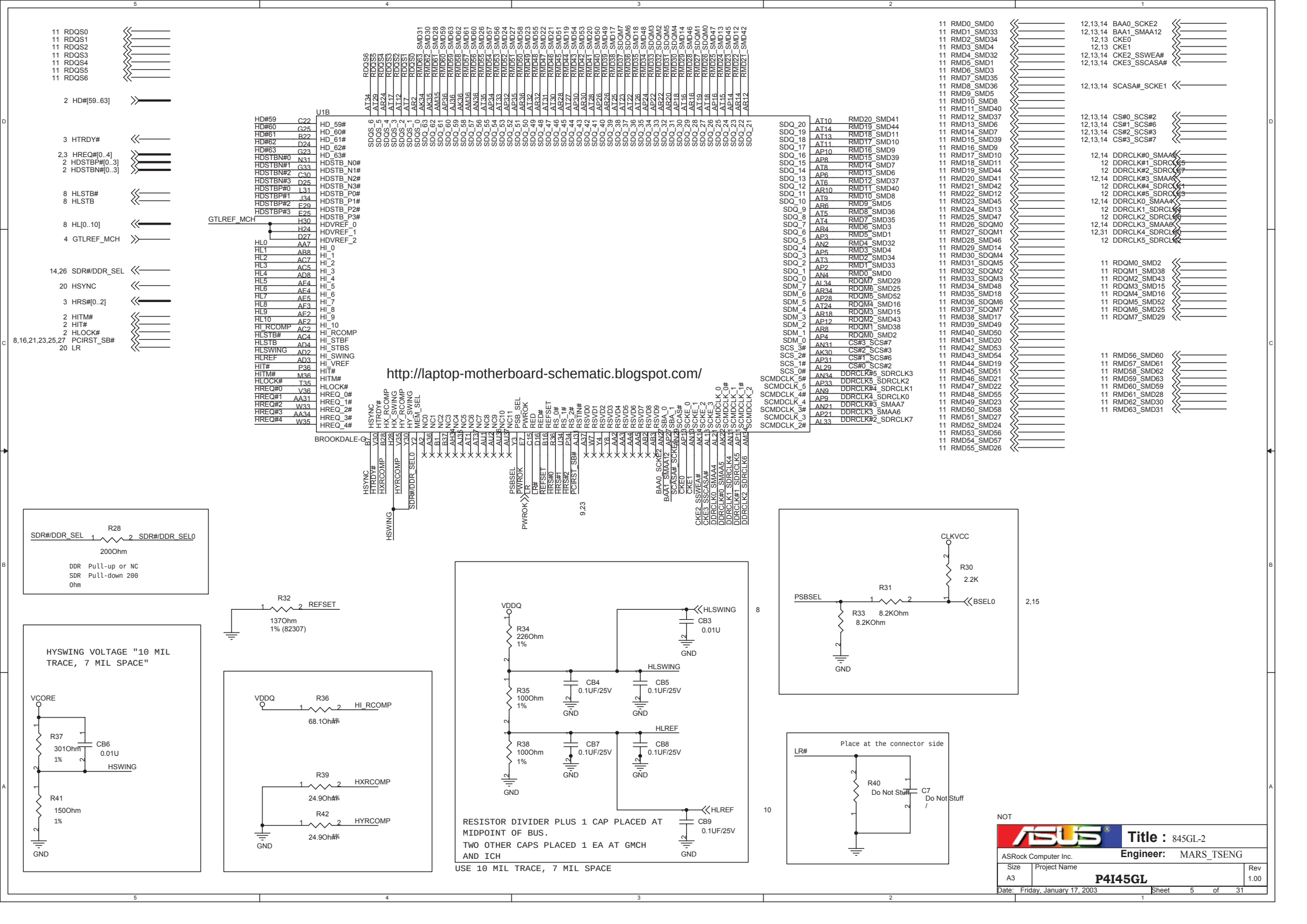


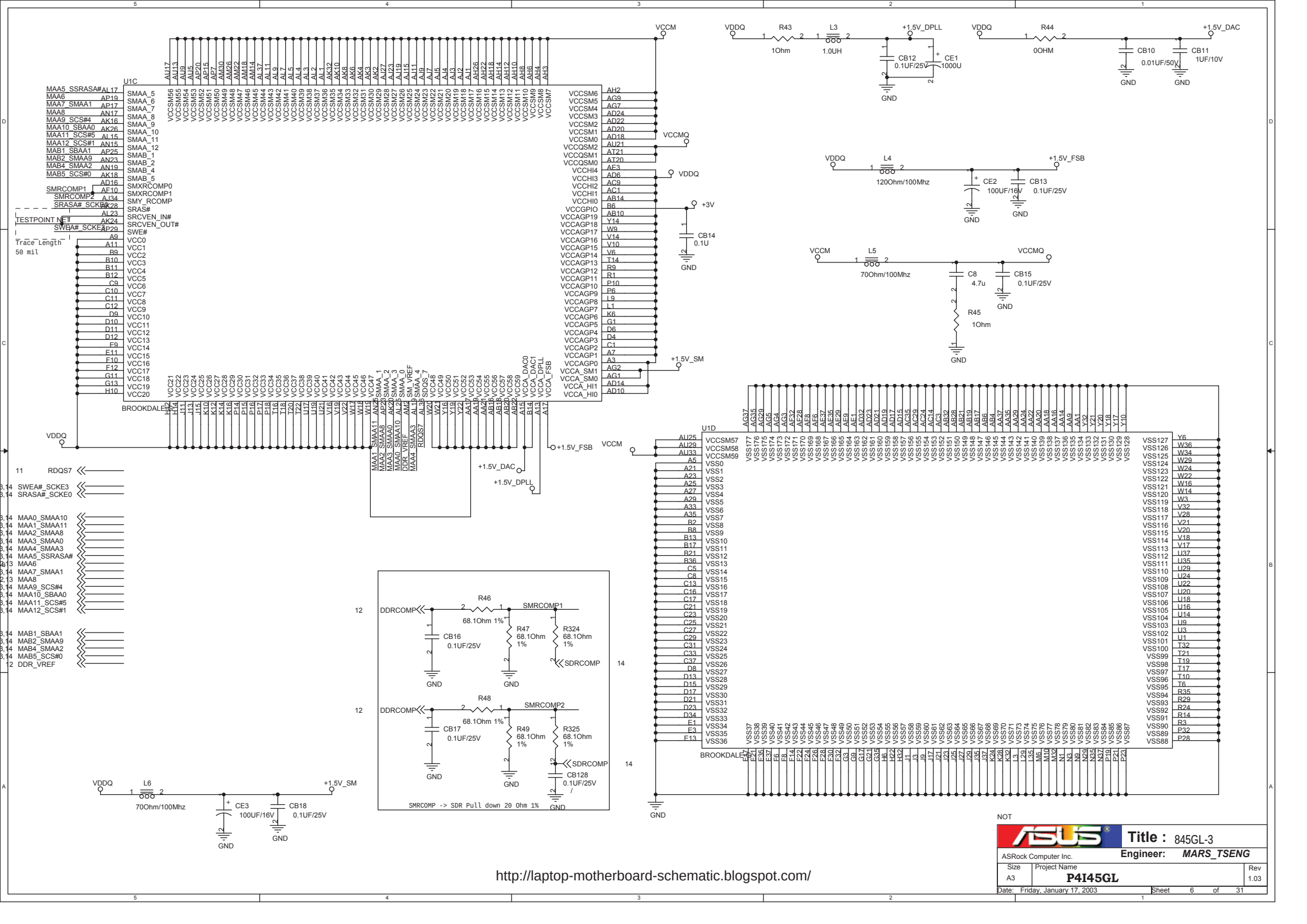
Title :	P4 SOCKET478-2
ASRock Computer Inc.	Engineer: MARS_TSENG
Size: A3	Project Name: P4I45GL
Rev: 1.00	
Date: Friday, January 17, 2003	Sheet 3 of 31



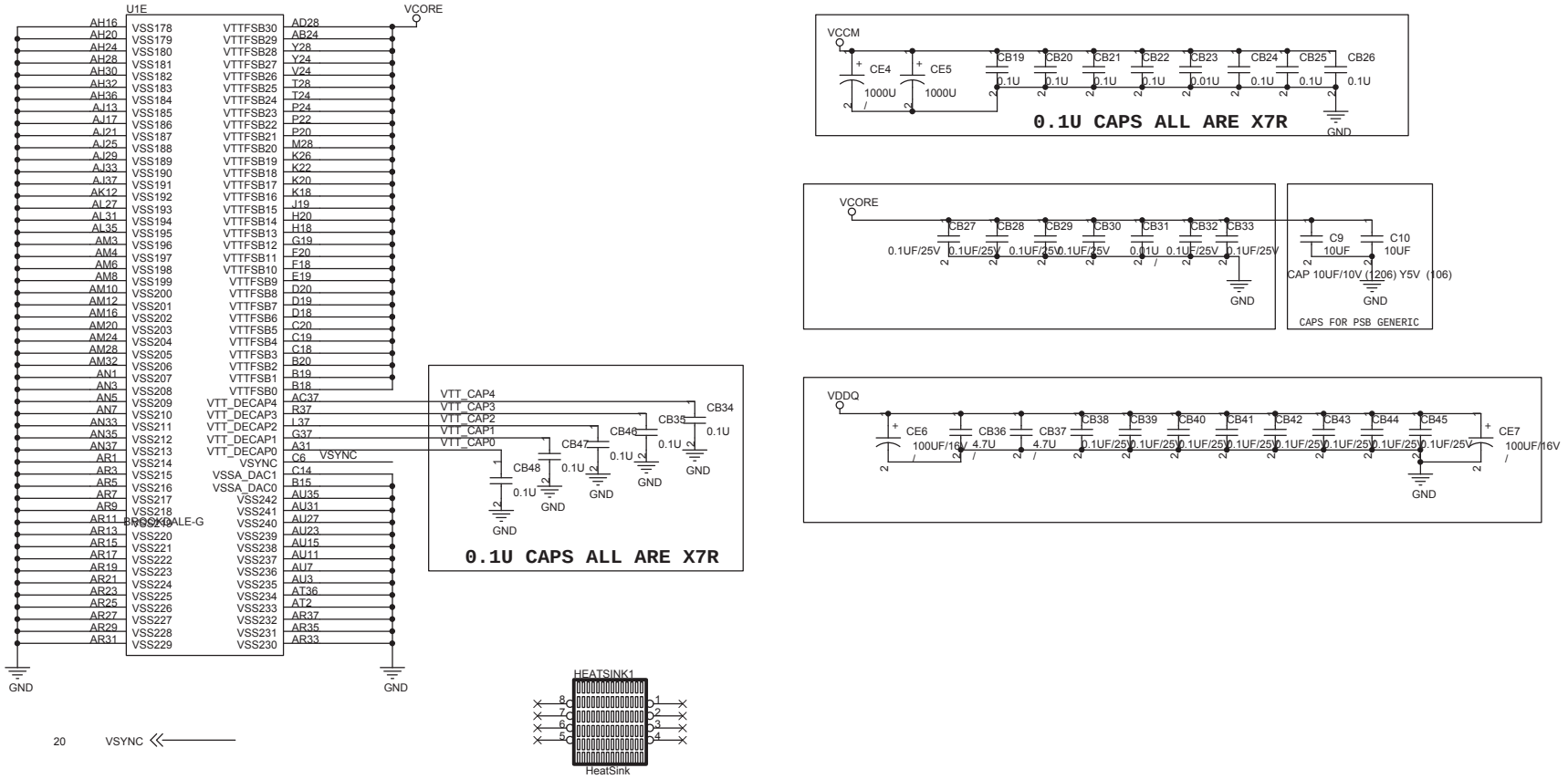
NOT

ASRock Computer Inc.	Title : 845GL-1	
	Engineer: MARS_TSENG	
Size: A3	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 4 of 31	


11 RDQS0
11 RDQS1
11 RDQS2
11 RDQS3
11 RDQS4
11 RDQS5
11 RDQS6
2 HD#[59..63]
3 HTRDY#
2,3 HREQ#[0..4]
2 HDSTBP#[0..3]
2 HDSTBN#[0..3]
8 HLSTB#
8 HLSTB
8 HL[0..10]
4 GTLREF_MCH
14,26 SDR#/DDR_SEL
20 HSYNC
3 HRS#[0..2]
2 HITM#
2 HIT#
2 HLOCK#
8,16,21,23,25,27 PCIRST_SB#
20 LR
U1B
BROOKDALE-G
GTLREF_MCH
http://laptop-motherboard-schematic.blogspot.com/
R28
SDR#/DDR_SEL
SDR#/DDR_SEL0
200Ohm
DDR Pull-up or NC
SDR Pull-down 200 Ohm
R32
REFSET
137Ohm
1% (82307)
HYSWING VOLTAGE "10 MIL TRACE, 7 MIL SPACE"
VCORE
R37
301Ohm
1%
CB6
0.01U
HSWING
R41
150Ohm
1%
GND
VDDQ
R36
HI_RCOMP
68.1Ohm
1%
R39
HXRCOMP
24.9Ohm
1%
R42
HYRCOMP
24.9Ohm
1%
GND
VDDQ
R34
226Ohm
1%
HLSWING
CB3
0.01U
GND
R35
100Ohm
1%
CB4
0.1UF/25V
CB5
0.1UF/25V
HLREF
R38
100Ohm
1%
CB7
0.1UF/25V
CB8
0.1UF/25V
HLREF
CB9
0.1UF/25V
RESISTOR DIVIDER PLUS 1 CAP PLACED AT MIDPOINT OF BUS.
TWO OTHER CAPS PLACED 1 EA AT GMCH AND ICH
USE 10 MIL TRACE, 7 MIL SPACE
8
10
CLKVCC
R30
2.2K
R31
PSBSEL
R33
8.2KOhm
8.2KOhm
BSEL0
2,15
Place at the connector side
LR#
R40
Do Not Stuff
C7
Do Not Stuff
NOT
Title : 845GL-2
ASRock Computer Inc.
Engineer: MARS_TSENG
Size A3
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 5 of 31

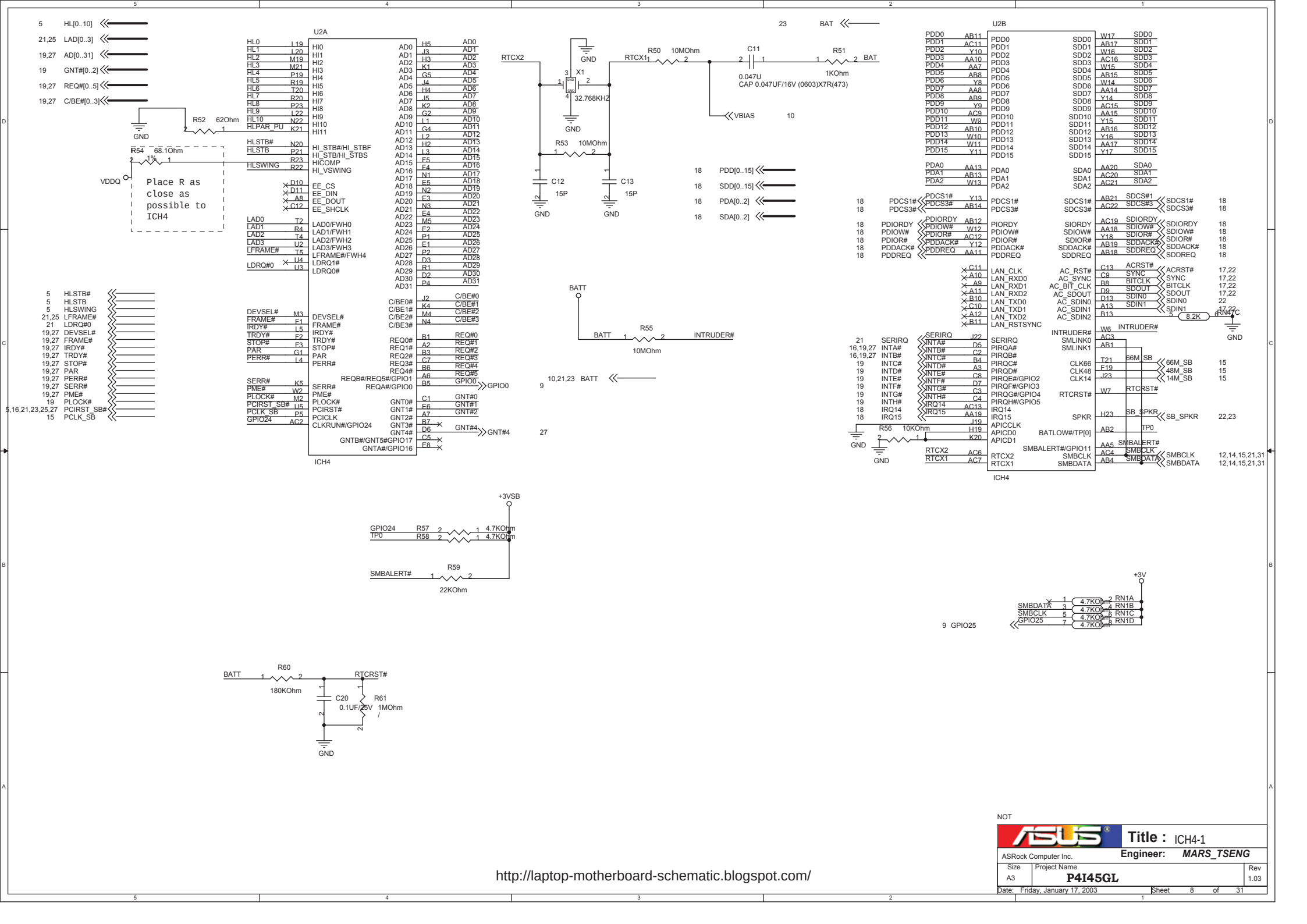


ASRock Computer Inc.	Title : 845GL-3	
	Engineer: *MARS_TSENG*	
Size: A3	Project Name: **P4I45GL**	Rev: 1.03
Date: Friday, January 17, 2003	Sheet 6 of 31	



NOT

ASRock Computer Inc.	Title : 845GL-4	
	Engineer: *MARS_TSENG*	
Size: A3	Project Name: **P4I45GL**	Rev: 1.03
Date: Friday, January 17, 2003	Sheet 7 of 31	



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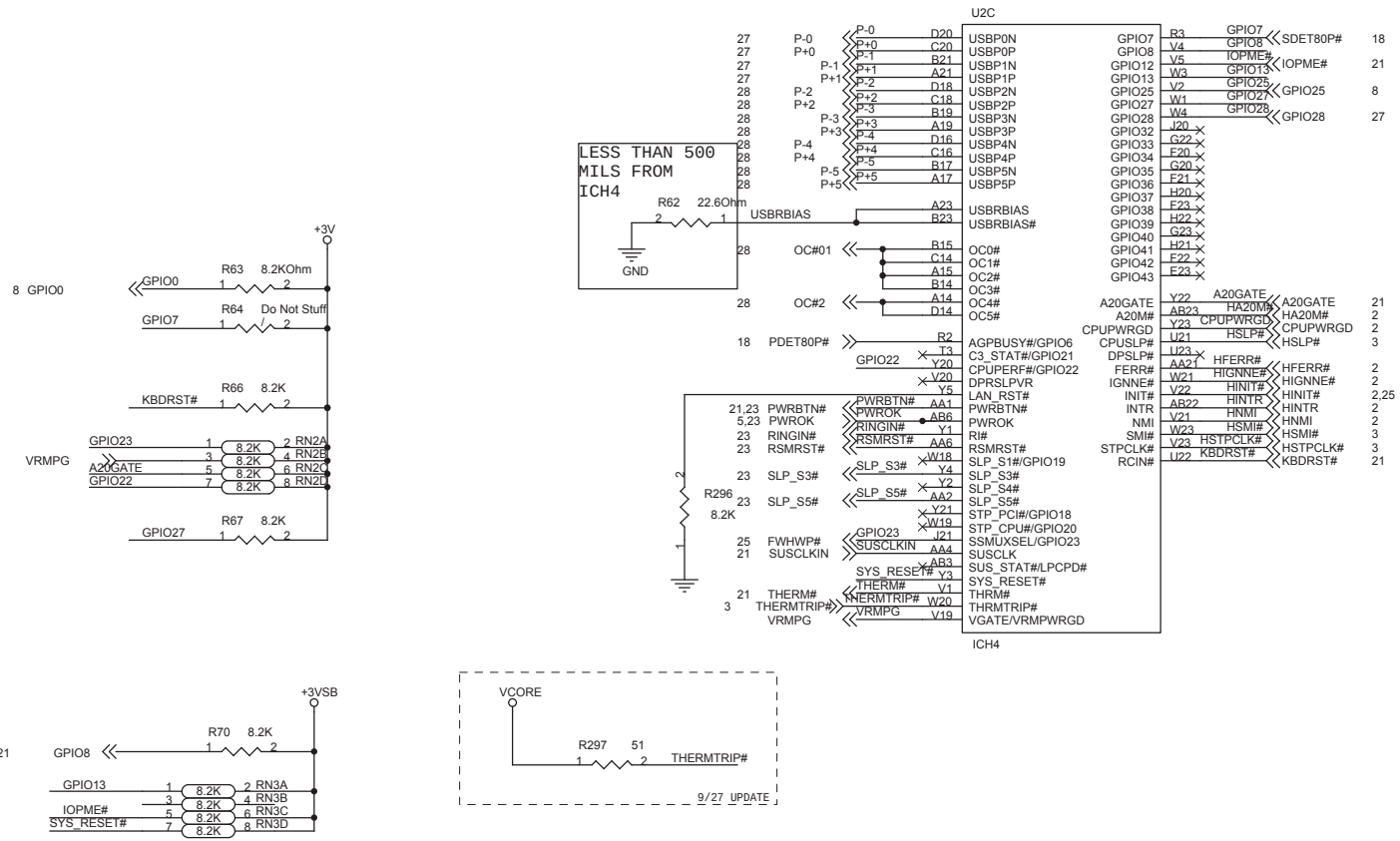
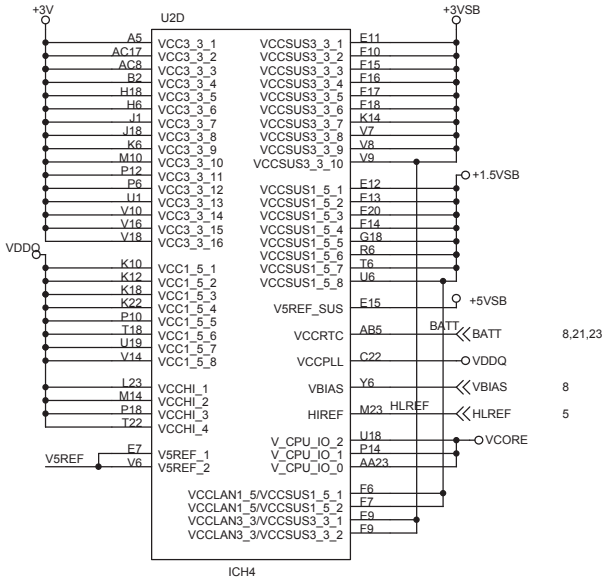
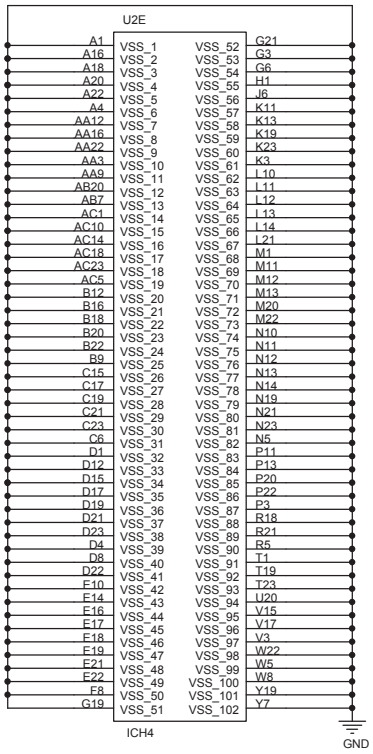
ASRock Computer Inc.	Title : ICH4-1	
	Engineer: *MARS_TSENG*	
Size: A3	Project Name: **P4I45GL**	Rev: 1.03
Date: Friday, January 17, 2003	Sheet 8 of 31	

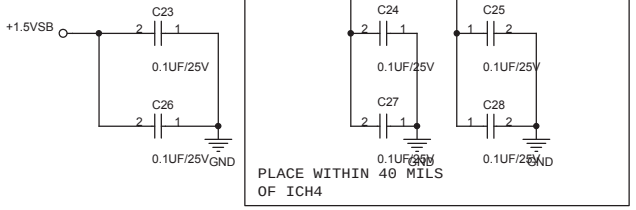


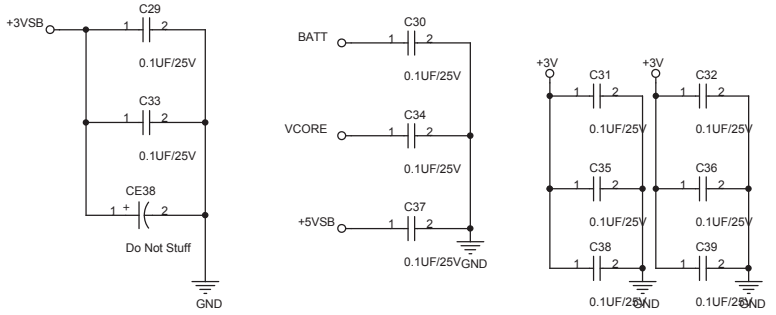
NOT

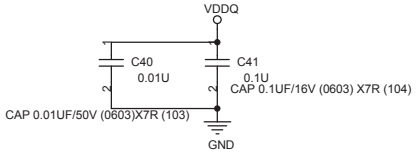
ASRock Computer Inc.	Title : ICH4-2	
	Engineer: *MARS_TSENG*	
Size: A3	Project Name: **P4I45GL**	Rev: 1.03
Date: Friday, January 17, 2003	Sheet 9 of 31	

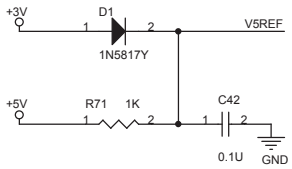








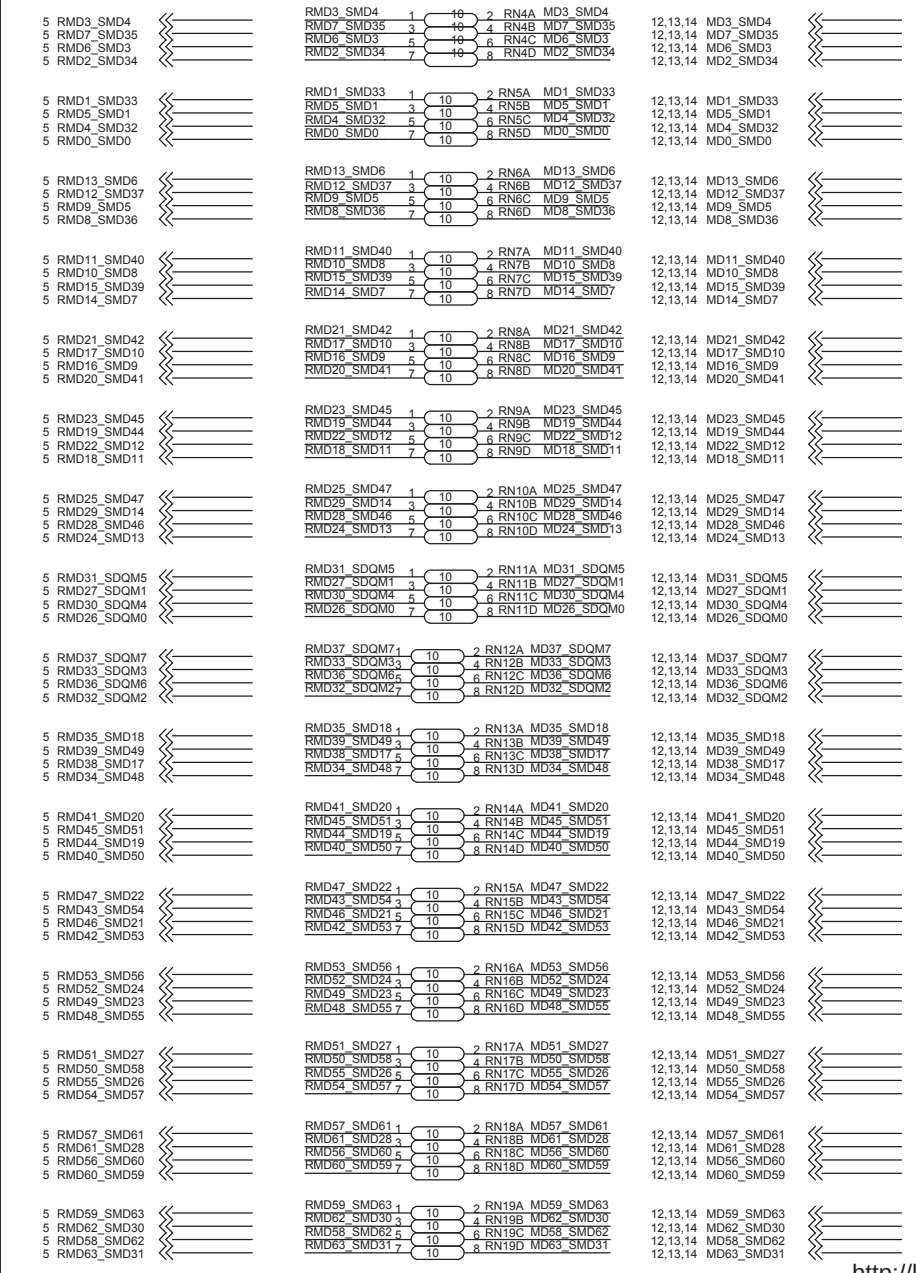


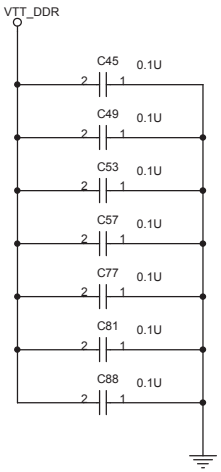


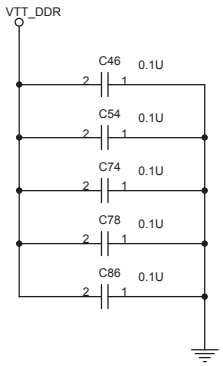
NOT

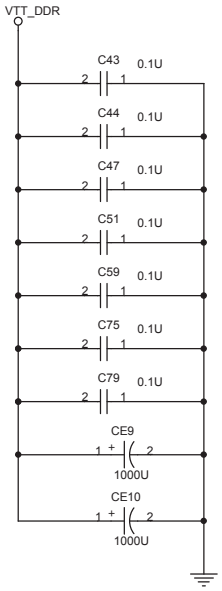
ASRock Computer Inc.	Title : ICH4-3	
	Engineer: *MARS_TSENG*	
Size: A3	Project Name: **P4I45GL**	Rev: 1.03
Date: Friday, January 17, 2003	Sheet 10 of 31	

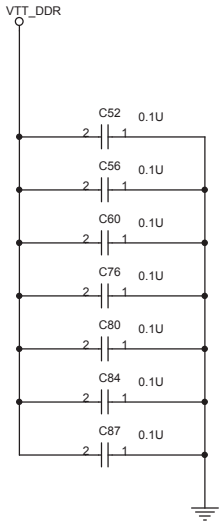
DDR Damping Resistor

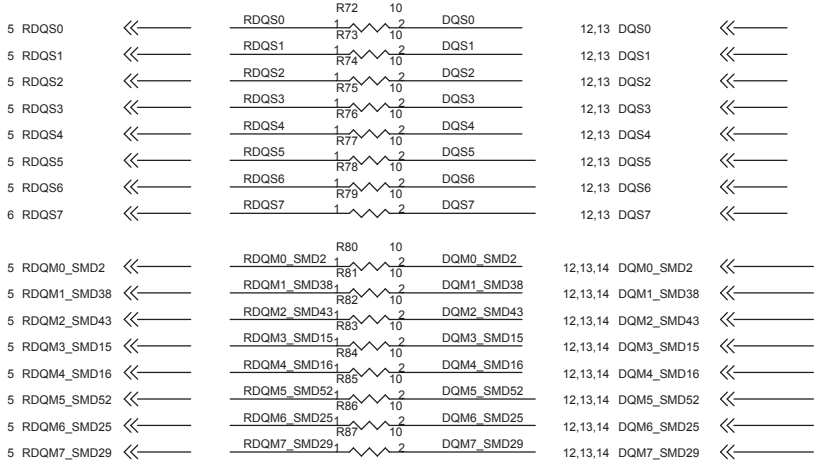






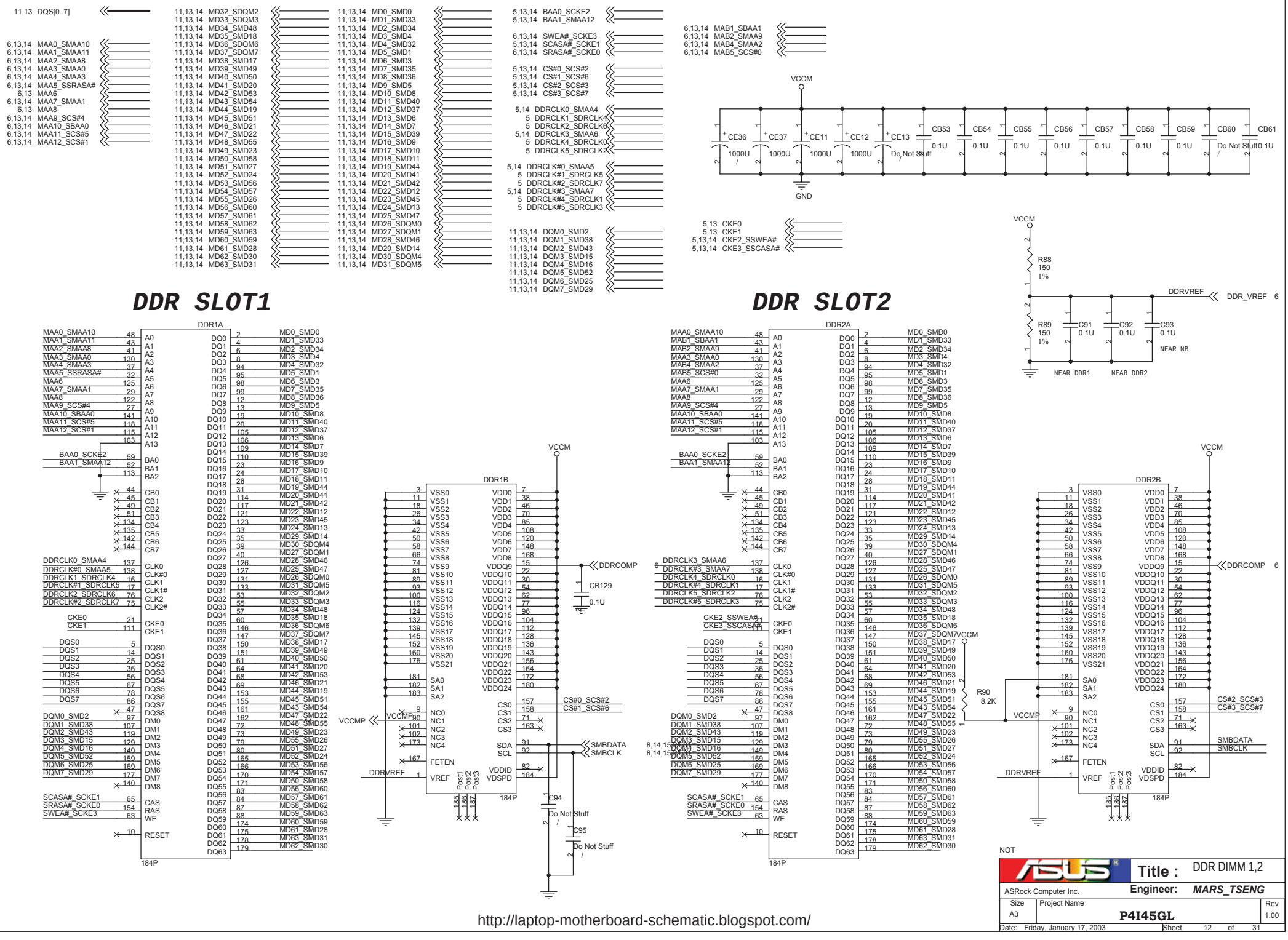




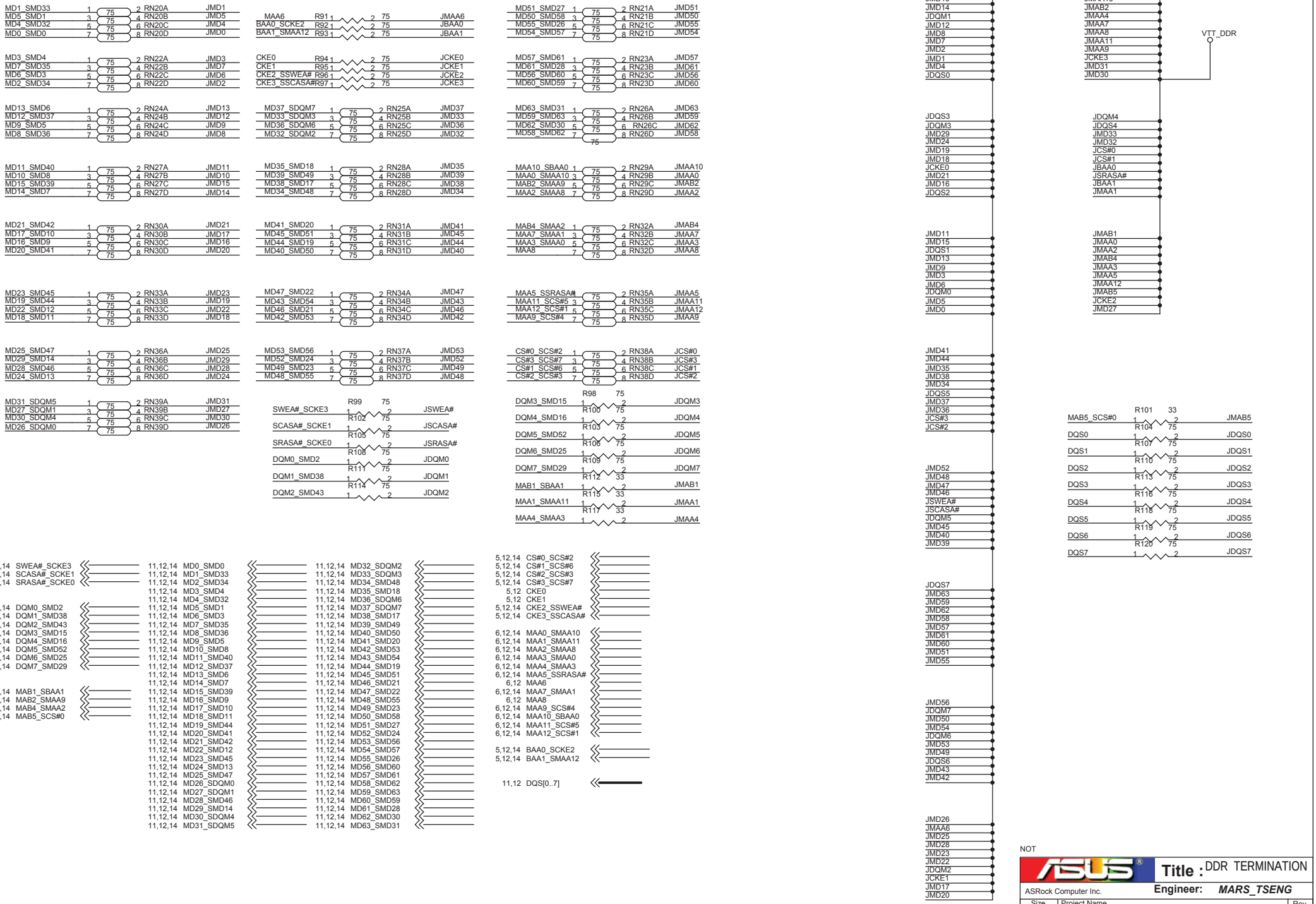


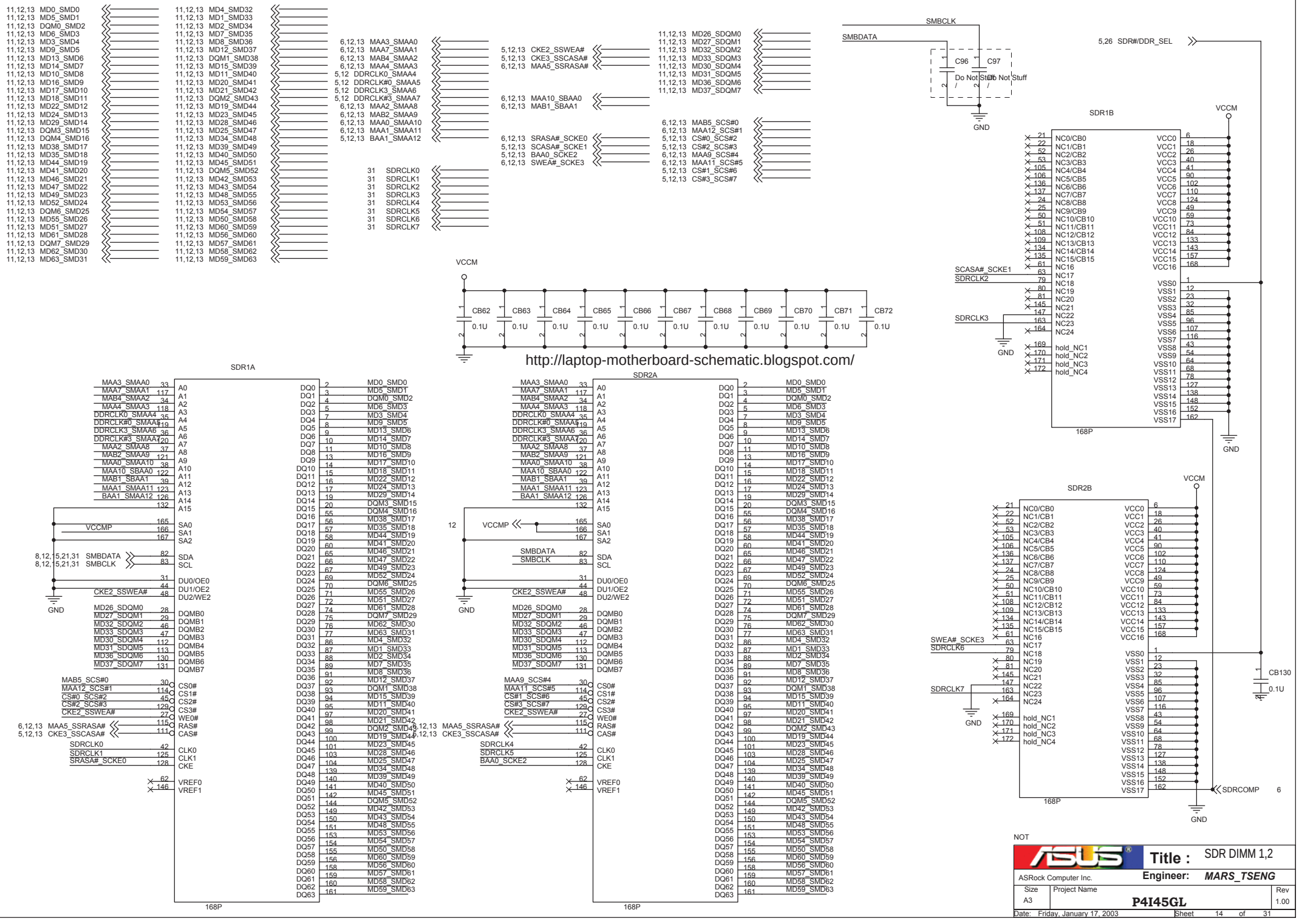
NOT

ASUS	Title : DDR Damping	
ASRock Computer Inc.	Engineer: MARS_TSENG	
Size: A3	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 11 of 31	



ASRock Computer Inc.	Title :	DDR DIMM 1,2	
	Engineer:	MARS_TSENG	
Size: A3	Project Name: P4I45GL		Rev: 1.00
Date: Friday, January 17, 2003	Sheet 12 of 31		

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11,12,13 MD13_SMD6
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11,12,13 MD52_SMD24
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11,12,13 MD55_SMD26
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11,12,13 MD63_SMD31
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11,12,13 MD1_SMD33
11,12,13 MD2_SMD34
11,12,13 MD7_SMD35
11,12,13 MD8_SMD36
11,12,13 MD12_SMD37
11,12,13 DQM1_SMD38
11,12,13 MD15_SMD39
11,12,13 MD11_SMD40
11,12,13 MD20_SMD41
11,12,13 MD21_SMD42
11,12,13 DQM2_SMD43
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11,12,13 MD25_SMD47
11,12,13 MD34_SMD48
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11,12,13 MD40_SMD50
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11,12,13 MD43_SMD54
11,12,13 MD48_SMD55
11,12,13 MD53_SMD56
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11,12,13 MD60_SMD59
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11,12,13 MD57_SMD61
11,12,13 MD58_SMD62
11,12,13 MD59_SMD63
6,12,13 MAA3_SMAA0
6,12,13 MAA7_SMAA1
6,12,13 MAB4_SMAA2
6,12,13 MAA4_SMAA3
5,12 DDRCLK0_SMAA4
5,12 DDRCLK#0_SMAA5
5,12 DDRCLK3_SMAA6
5,12 DDRCLK#3_SMAA7
6,12,13 MAA2_SMAA8
6,12,13 MAB2_SMAA9
6,12,13 MAA0_SMAA10
6,12,13 MAA1_SMAA11
5,13,13 BAA1_SMAA12
31 SDRCLK0
31 SDRCLK1
31 SDRCLK2
31 SDRCLK3
31 SDRCLK4
31 SDRCLK5
31 SDRCLK6
31 SDRCLK7
5,12,13 CKE2_SSWEA#
5,12,13 CKE3_SSCASA#
6,12,13 MAA5_SSRASA#
6,12,13 MAA10_SBAA0
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5,12,13 SCASA#_SCKE1
5,12,13 BAA0_SCKE2
6,12,13 SWEA#_SCKE3
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6,12,13 MAA12_SCS#1
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6,12,13 MAA9_SCS#4
6,12,13 MAA11_SCS#5
5,12,13 CS#1_SCS#6
5,12,13 CS#3_SCS#7
SMBCLK
SMBDATA
C96
C97
Do Not Stuff
Do Not Stuff
GND
5,26 SDR#/DDR_SEL
SDR1B
VCCM
SCASA#_SCKE1
SDRCLK2
SDRCLK3
NC0/CB0
NC1/CB1
NC2/CB2
NC3/CB3
NC4/CB4
NC5/CB5
NC6/CB6
NC7/CB7
NC8/CB8
NC9/CB9
NC10/CB10
NC11/CB11
NC12/CB12
NC13/CB13
NC14/CB14
NC15/CB15
NC16
NC17
NC18
NC19
NC20
NC21
NC22
NC23
NC24
hold_NC1
hold_NC2
hold_NC3
hold_NC4
VCC0
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
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VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
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SDR1A
SDR2A
SDR2B
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MAA7_SMAA1
MAB4_SMAA2
MAA4_SMAA3
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DDRCLK#0_SMAA5
DDRCLK3_SMAA6
DDRCLK#3_SMAA7
MAA2_SMAA8
MAB2_SMAA9
MAA0_SMAA10
MAA10_SBAA0
MAB1_SBAA1
MAA1_SMAA11
BAA1_SMAA12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
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A12
A13
A14
A15
VCCMP
SA0
SA1
SA2
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8,12,15,21,31 SMBCLK
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SCL
DU0/OE0
DU1/OE2
DU2/WE2
CKE2_SSWEA#
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MD27_SDQM1
MD32_SDQM2
MD33_SDQM3
MD30_SDQM4
MD31_SDQM5
MD36_SDQM6
MD37_SDQM7
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DQMB1
DQMB2
DQMB3
DQMB4
DQMB5
DQMB6
DQMB7
MAB5_SCS#0
MAA12_SCS#1
CS#0_SCS#2
CS#2_SCS#3
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CS0#
CS1#
CS2#
CS3#
WE0#
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CLK1
CKE
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VREF1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
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DQ63
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DQM0_SMD2
MD6_SMD3
MD3_SMD4
MD9_SMD5
MD13_SMD6
MD14_SMD7
MD10_SMD8
MD16_SMD9
MD17_SMD10
MD18_SMD11
MD22_SMD12
MD24_SMD13
MD29_SMD14
DQM3_SMD15
DQM4_SMD16
MD38_SMD17
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MD53_SMD56
MD54_SMD57
MD50_SMD58
MD60_SMD59
MD56_SMD60
MD57_SMD61
MD58_SMD62
MD59_SMD63
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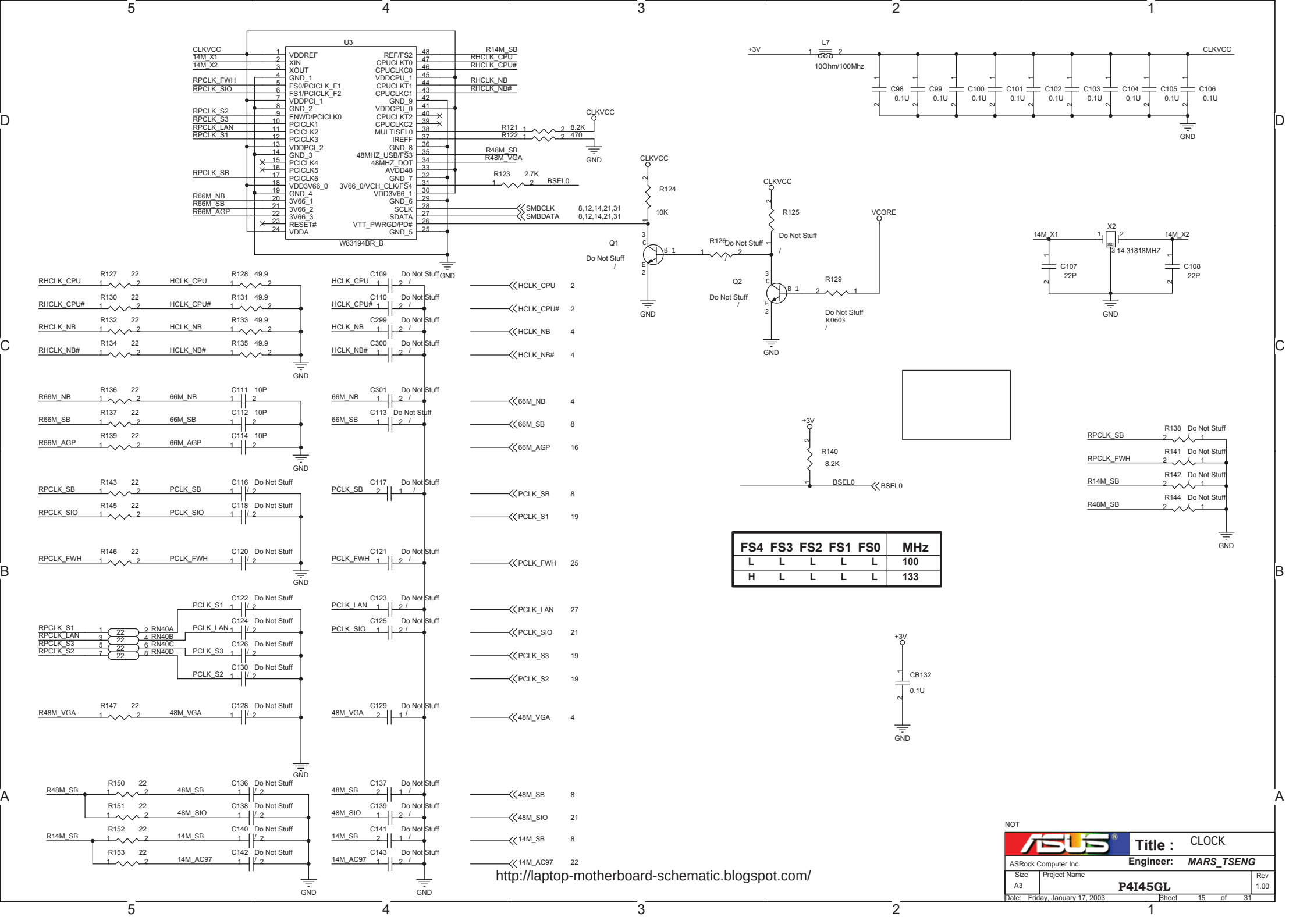
12 VCCMP
SWEA#_SCKE3
SDRCLK6
SDRCLK7
CB130
0.1U
SDRCOMP
6
NOT
Title : SDR DIMM 1,2
ASRock Computer Inc.
Engineer: MARS_TSENG
Size A3
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 14 of 31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W83194BR_B
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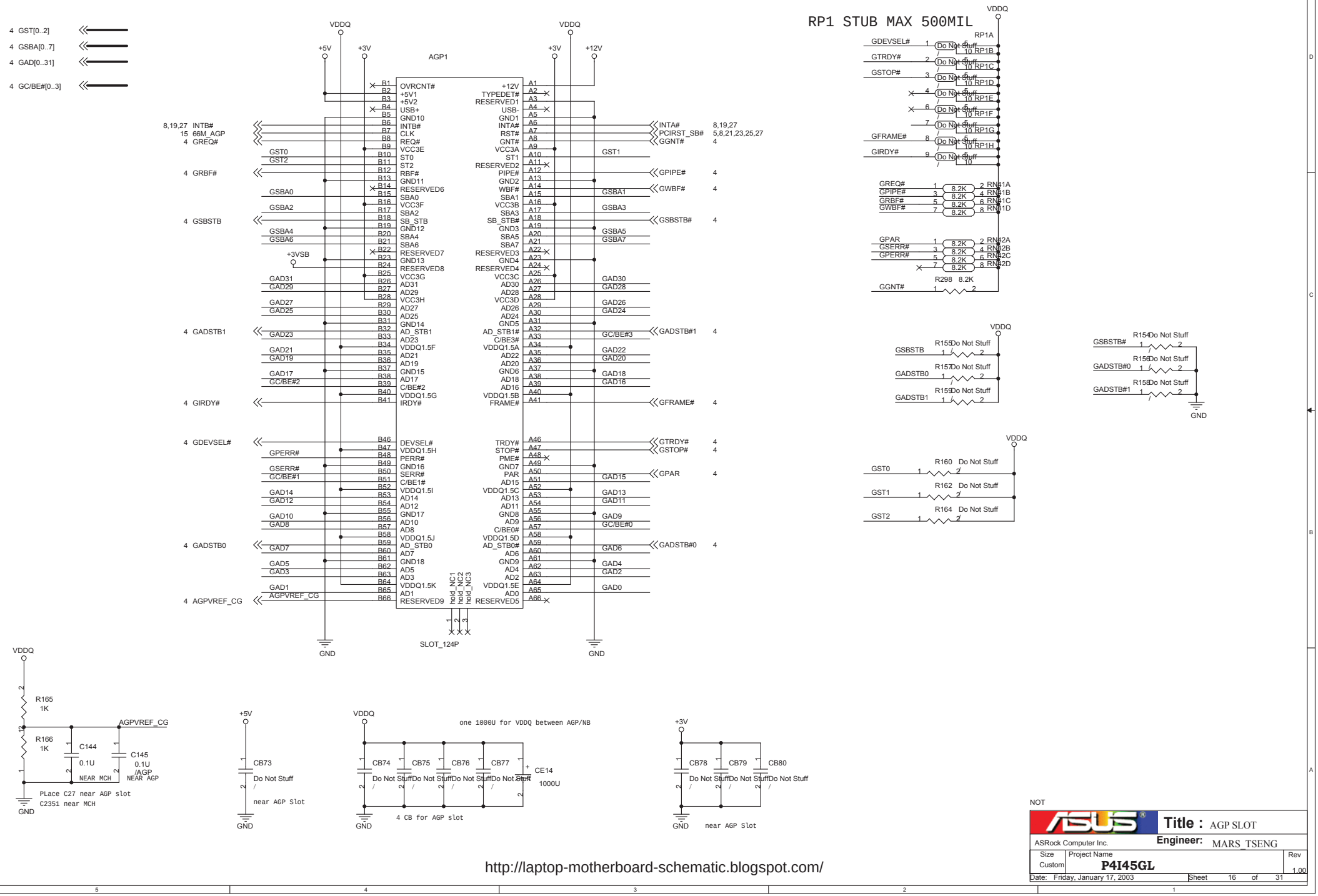
14M_X1
14M_X2
RPCLK_FWH
RPCLK_SIO
RPCLK_S2
RPCLK_S3
RPCLK_LAN
RPCLK_S1
RPCLK_SB
R66M_NB
R66M_SB
R66M_AGP
VDDREF
XIN
XOUT
GND_1
FS0/PCICLK_F1
FS1/PCICLK_F2
VDDPCI_1
GND_2
ENWD/PCICLK0
PCICLK1
PCICLK2
PCICLK3
VDDPCI_2
GND_3
PCICLK4
PCICLK5
PCICLK6
VDD3V66_0
GND_4
3V66_1
3V66_2
3V66_3
RESET#
VDDA
REF/FS2
CPUCLKT0
CPUCLKC0
VDDCPU_1
CPUCLKT1
CPUCLKC1
GND_9
VDDCPU_0
CPUCLKT2
CPUCLKC2
MULTISEL0
IREFF
GND_8
48MHZ_USB/FS3
48MHZ_DOT
AVDD48
GND_7
3V66_0/VCH_CLK/FS4
VDD3V66_1
GND_6
SCLK
SDATA
VTT_PWRGD/PD#
GND_5
R14M_SB
RHCLK_CPU
RHCLK_CPU#
RHCLK_NB
RHCLK_NB#
R48M_SB
R48M_VGA
R121 8.2K
R122 470
R123 2.7K
BSEL0
SMBCLK
SMBDATA
8,12,14,21,31
8,12,14,21,31
GND
+3V
L7
10Ohm/100Mhz
C98 0.1U
C99 0.1U
C100 0.1U
C101 0.1U
C102 0.1U
C103 0.1U
C104 0.1U
C105 0.1U
C106 0.1U
R124 10K
Q1
Do Not Stuff
R125 Do Not Stuff
R126 Do Not Stuff
Q2
R129 Do Not Stuff
R0603
VCORE
X2
14.31818MHZ
C107 22P
C108 22P
R127 22
R128 49.9
R130 22
R131 49.9
R132 22
R133 49.9
R134 22
R135 49.9
HCLK_CPU
HCLK_CPU#
HCLK_NB
HCLK_NB#
C109 Do Not Stuff
C110 Do Not Stuff
C299 Do Not Stuff
C300 Do Not Stuff
R136 22
R137 22
R139 22
66M_NB
66M_SB
66M_AGP
C111 10P
C112 10P
C114 10P
C301 Do Not Stuff
C113 Do Not Stuff
R140 8.2K
R143 22
R145 22
R146 22
PCLK_SB
PCLK_SIO
PCLK_FWH
C116 Do Not Stuff
C118 Do Not Stuff
C120 Do Not Stuff
C117 Do Not Stuff
C121 Do Not Stuff
PCLK_S1
PCLK_LAN
PCLK_S3
PCLK_S2
RN40A
RN40B
RN40C
RN40D
C122 Do Not Stuff
C124 Do Not Stuff
C126 Do Not Stuff
C130 Do Not Stuff
C123 Do Not Stuff
C125 Do Not Stuff
R147 22
48M_VGA
C128 Do Not Stuff
C129 Do Not Stuff
R150 22
R151 22
R152 22
R153 22
48M_SB
48M_SIO
14M_SB
14M_AC97
C136 Do Not Stuff
C138 Do Not Stuff
C140 Do Not Stuff
C142 Do Not Stuff
C137 Do Not Stuff
C139 Do Not Stuff
C141 Do Not Stuff
C143 Do Not Stuff
R138 Do Not Stuff
R141 Do Not Stuff
R142 Do Not Stuff
R144 Do Not Stuff
CB132 0.1U
FS4 FS3 FS2 FS1 FS0 MHz
L L L L L 100
H L L L L 133
http://laptop-motherboard-schematic.blogspot.com/
NOT
Title : CLOCK
ASRock Computer Inc.
Engineer: MARS_TSENG
Size A3
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 15 of 31



NOT

ASRock Computer Inc.

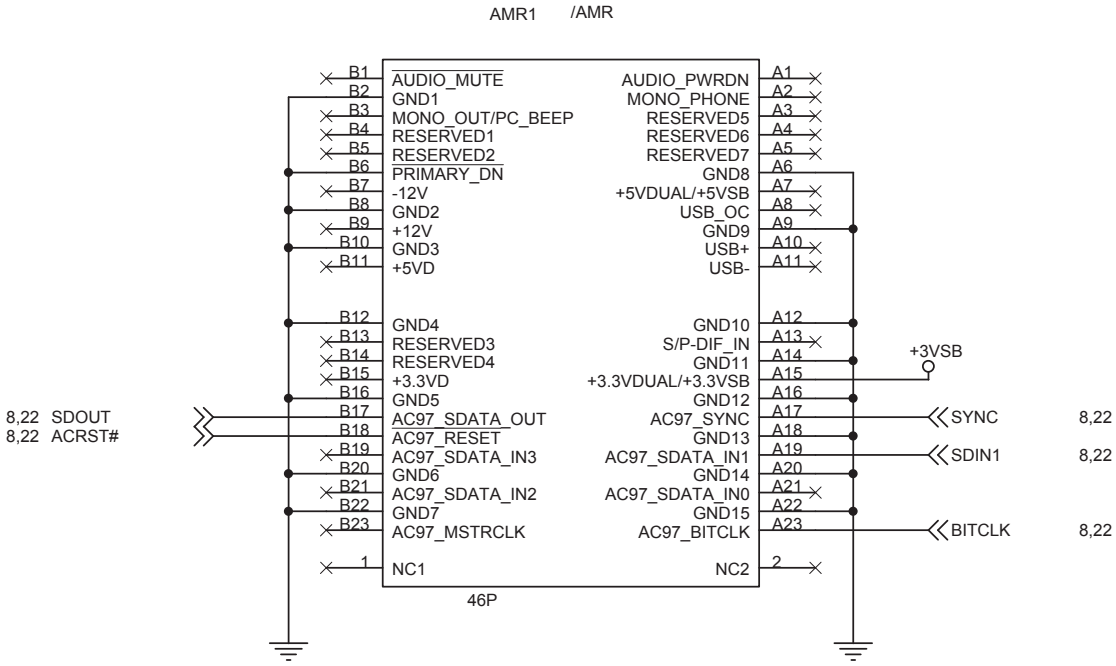
Title : AGP SLOT

Engineer: MARS_TSENG

Size	Project Name	Rev
Custom	P4I45GL	1.00

Date: Friday, January 17, 2003 Sheet 16 of 31

AMR SLOT

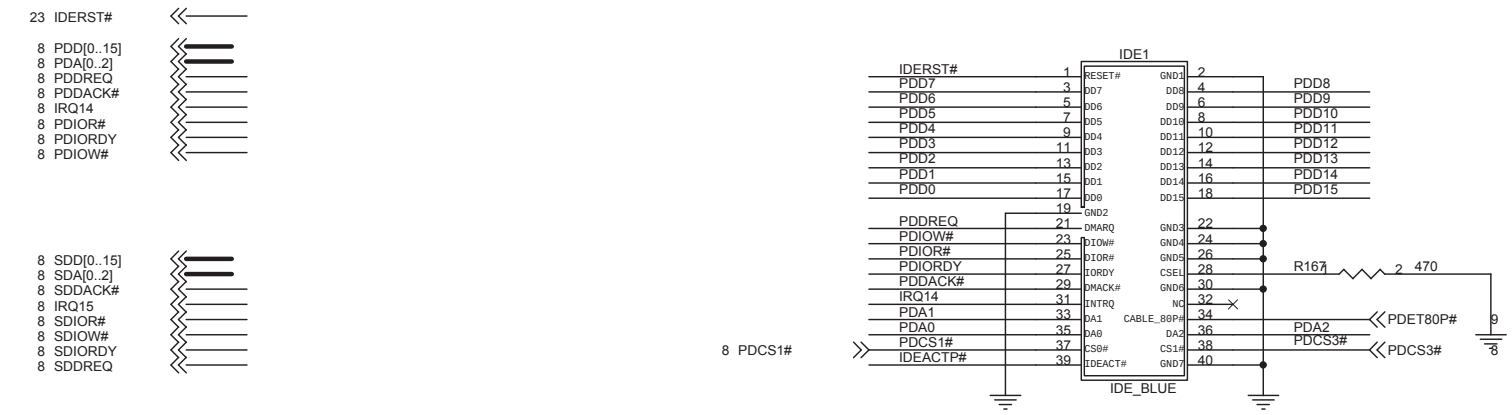


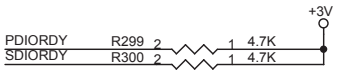
Note: This AMR Slot only support MODEM

NOT

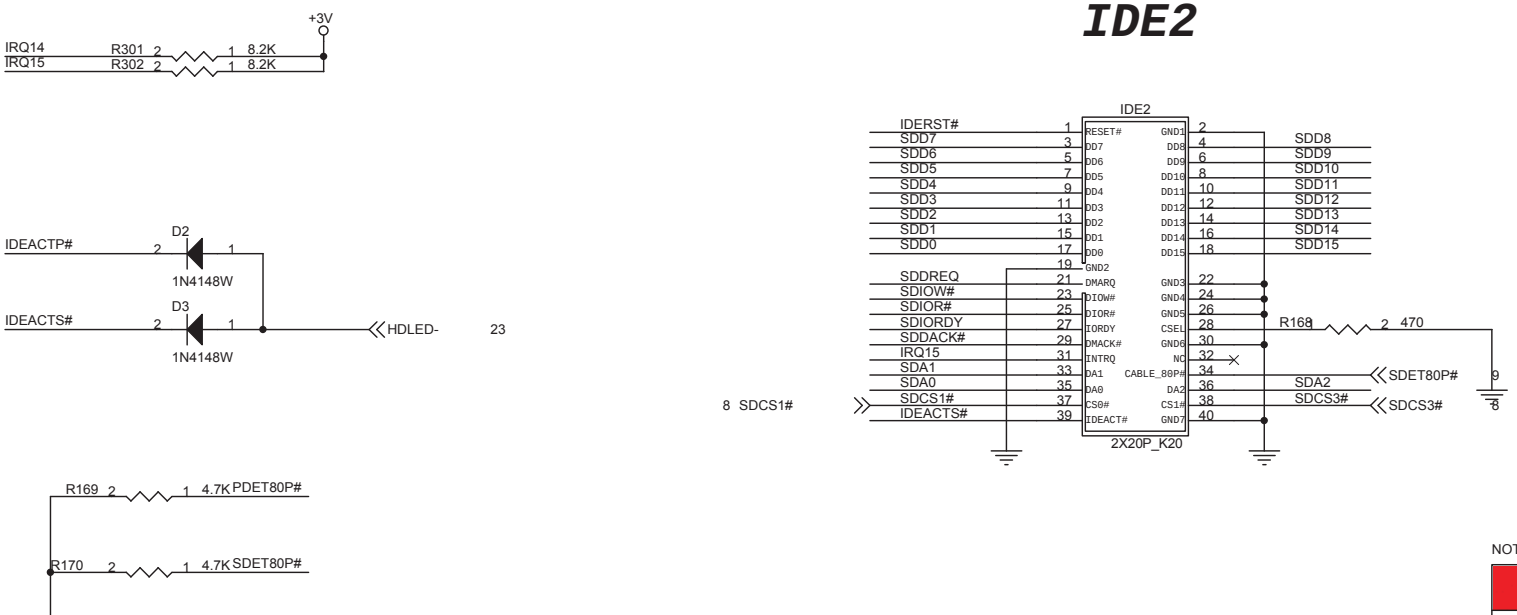
ASRock Computer Inc.	Title : AMR SLOT	
	Engineer: MARS_TSENG	
Size: A4	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 17 of 31	

IDE1





IDE2



NOT

ASUS	Title :	IDE 1&2
ASRock Computer Inc.	Engineer:	MARS_TSENG
Size: Custom	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 18 of 31	

8,27 AD[0..31]
8,27 C/BE#[0..3]

8,27 DEVSEL#
8,27 IRDY#
8,27 STOP#

8,27 REQ#[0..5]

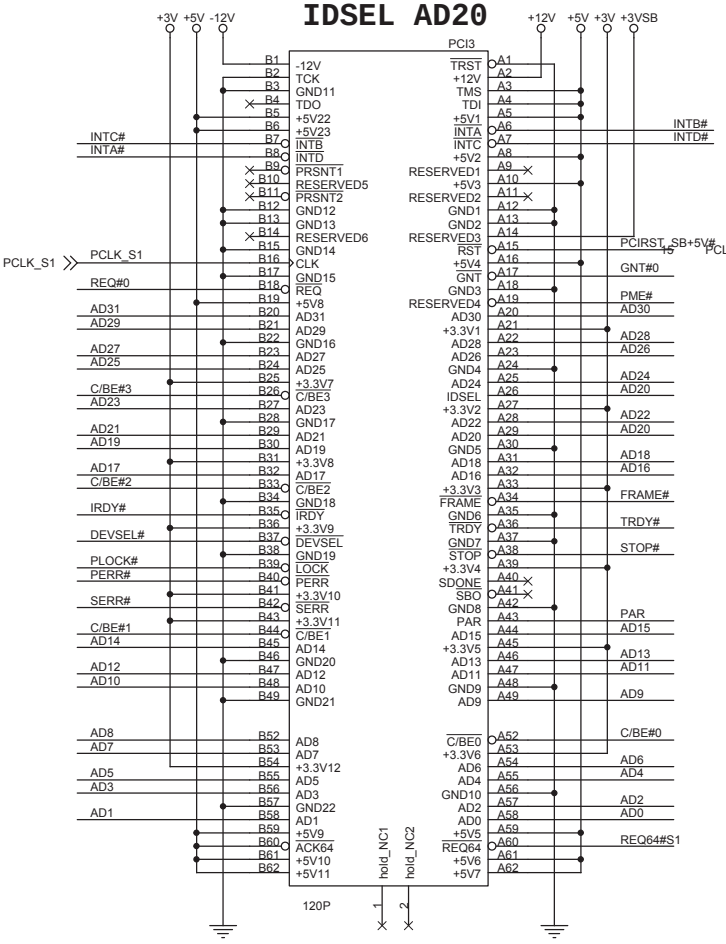
8 GNT#[0..2]

8,16,27 INTA#
8,16,27 INTB#
8 INTC#
8 INTD#
8,27 SERR#
8,27 PAR

8,27 PME#
23 PCIRST_SB+5V#
8,27 FRAME#
8,27 TRDY#
8 PLOCK#
8,27 PERR#

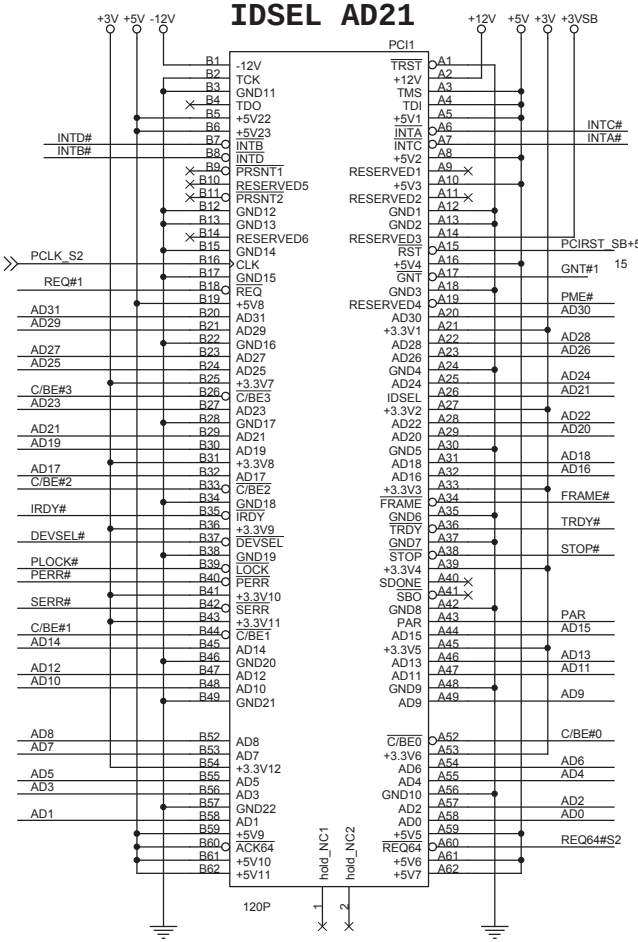
PCI SLOT1

BCDA
IDSEL AD20



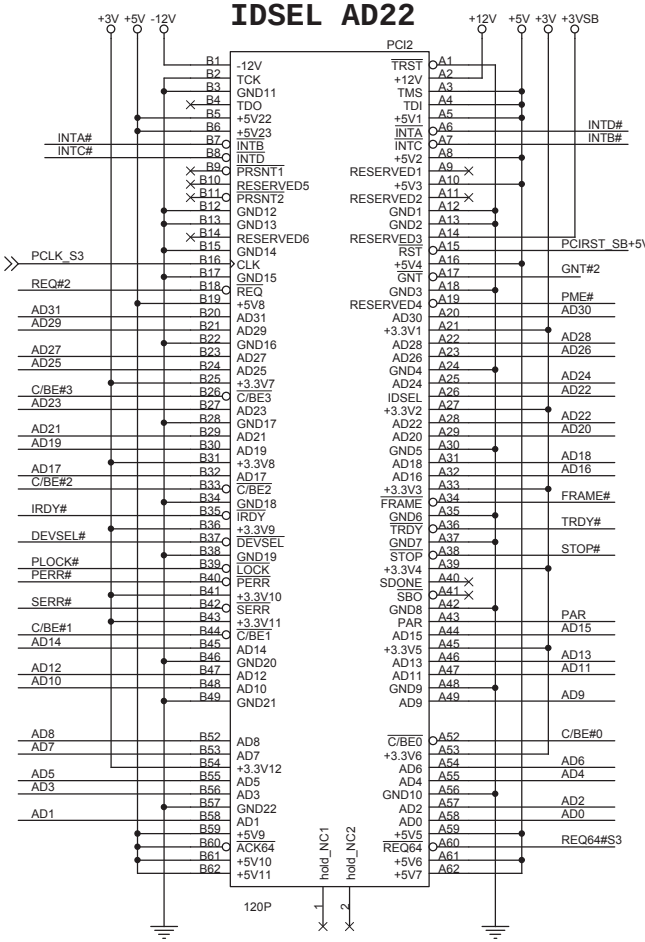
PCI SLOT2

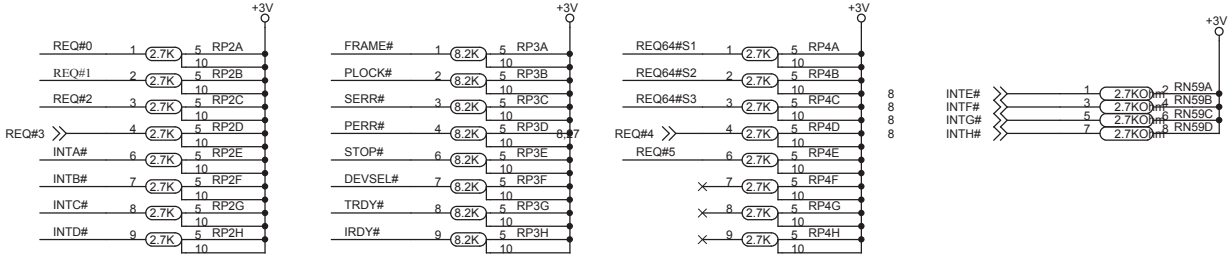
CDAB
IDSEL AD21



PCI SLOT3

DABC
IDSEL AD22





NOT

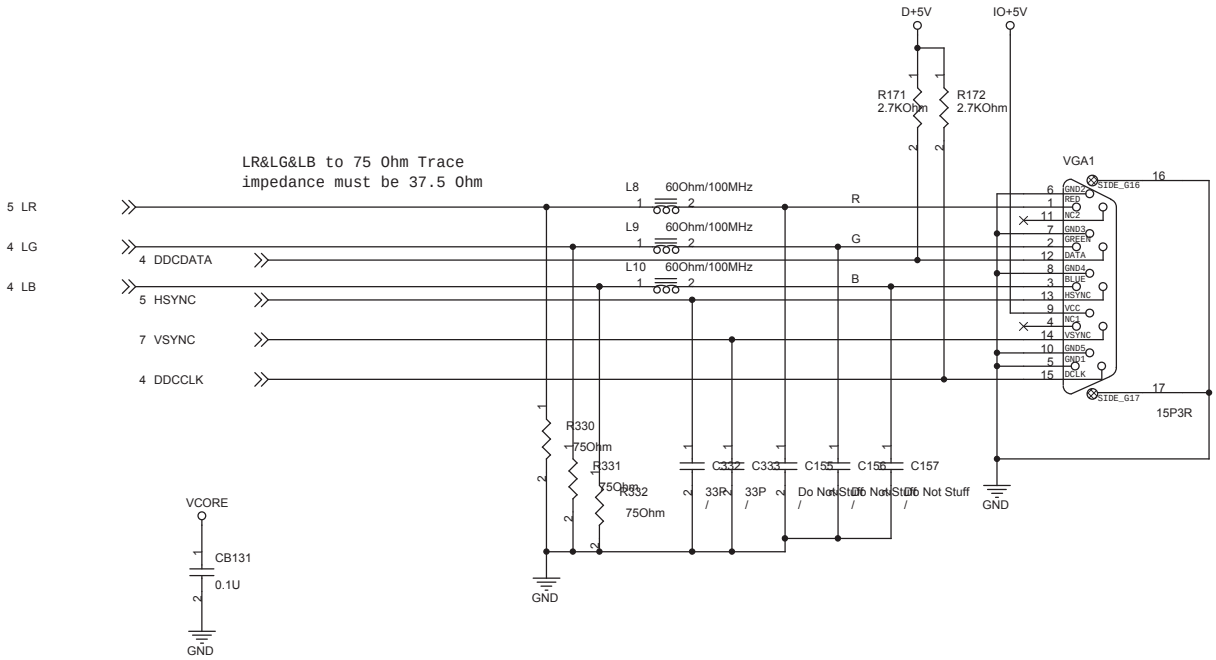
ASRock Computer Inc.

Title : PCI SLOT 1,2,3

Engineer: MARS_TSENG

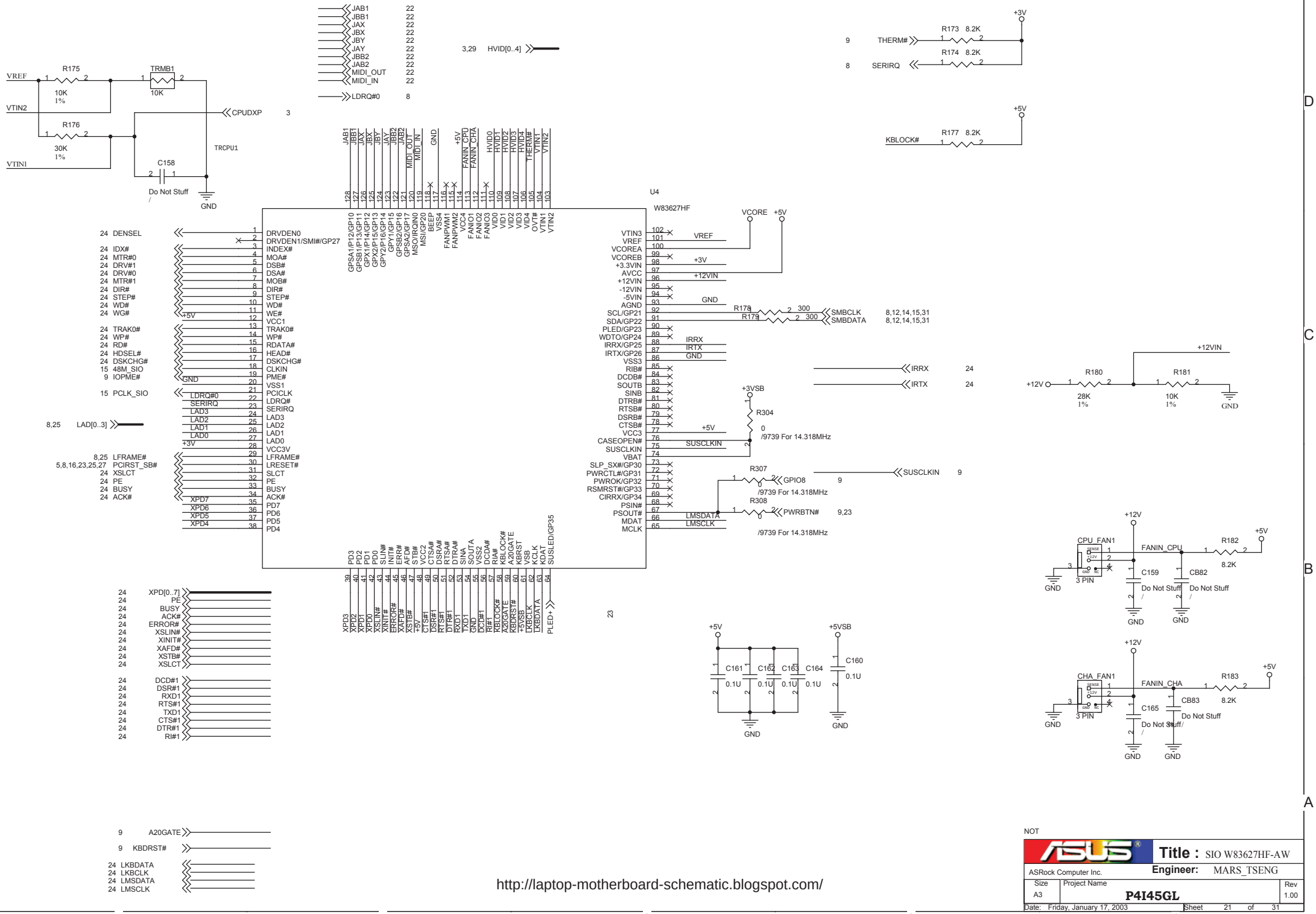
Size	Project Name	Rev
A3	P4I45GL	1.00

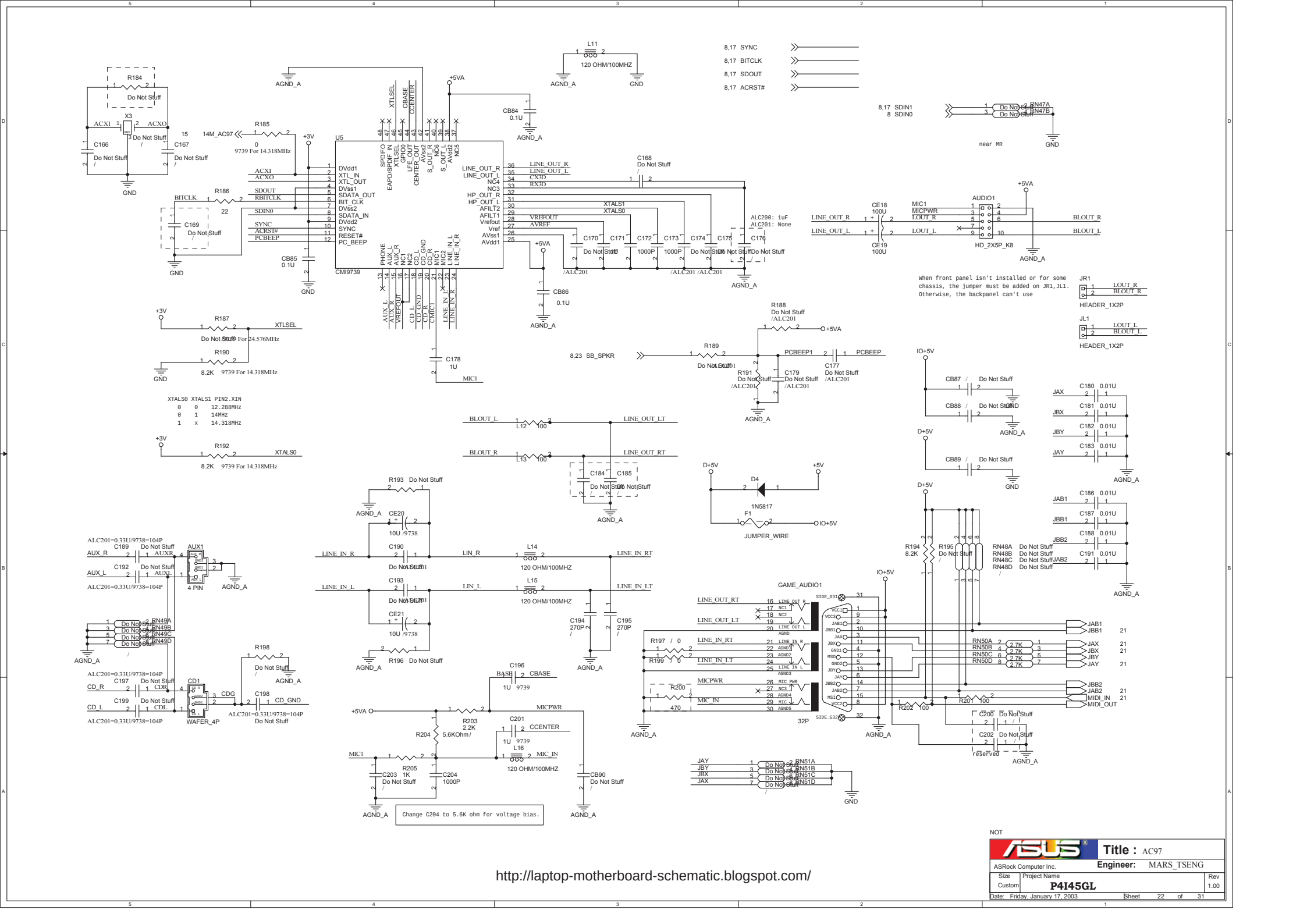
Date: Friday, January 17, 2003 Sheet 19 of 31

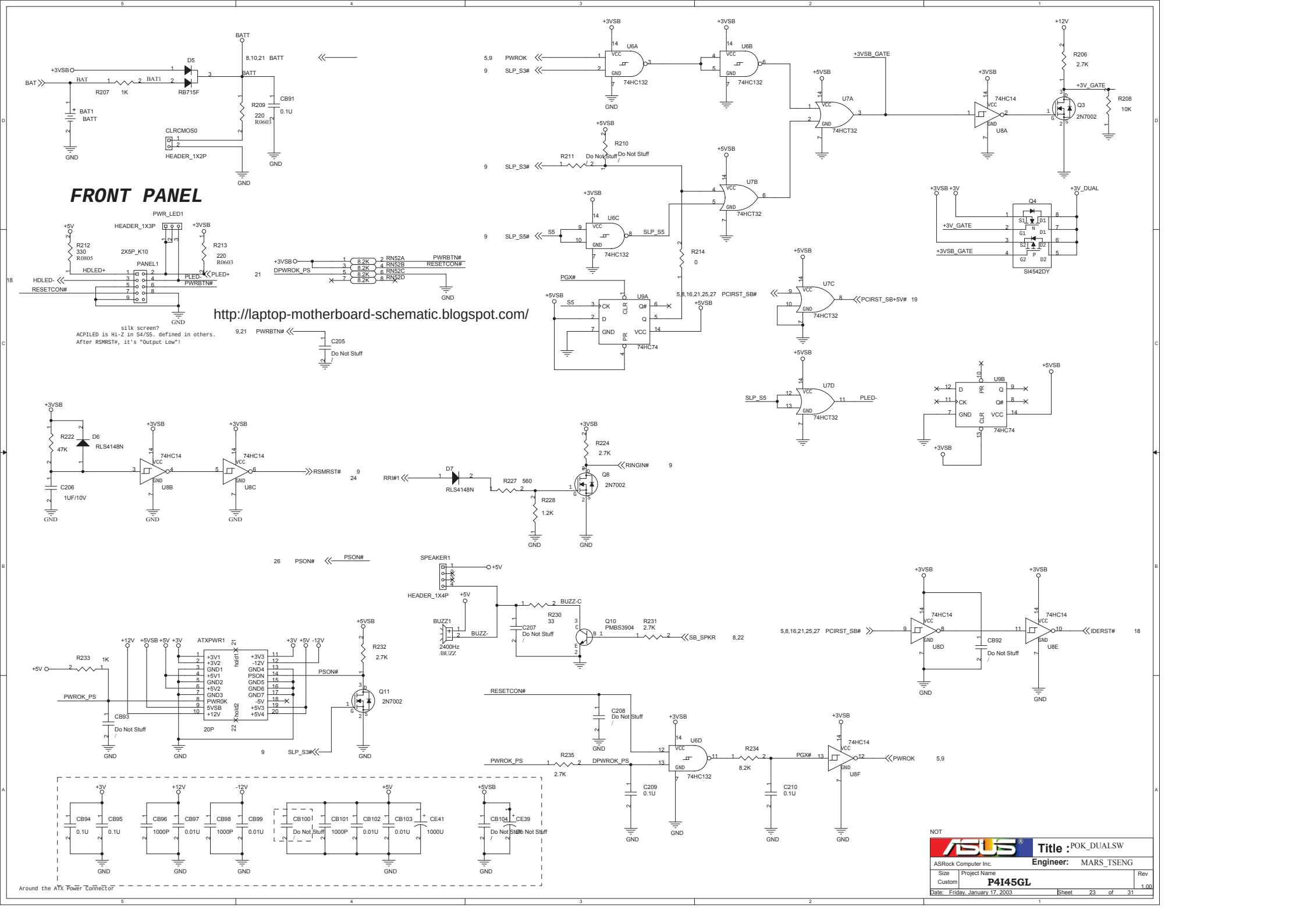


NOT

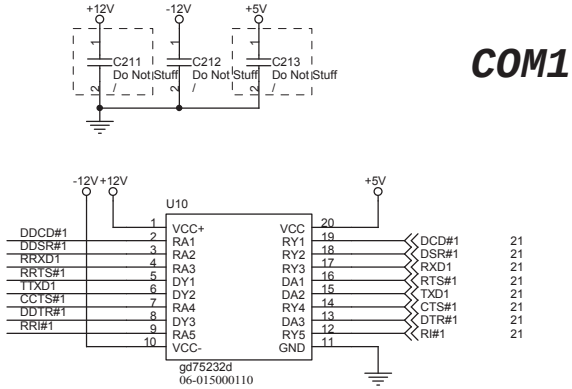
ASUS	Title : VGA CONNECTOR	
ASRock Computer Inc.	Engineer: MARS_TSENG	
Size: A3	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 20 of 31	


JAB1 22
JBB1 22
JAX 22
JBX 22
JBY 22
JAY 22
JBB2 22
JAB2 22
MIDI_OUT 22
MIDI_IN 22
LDRQ#0 8
3,29 HVID[0..4]
+3V
R173 8.2K
9 THERM#
R174 8.2K
8 SERIRQ
+5V
KBLOCK#
R177 8.2K
VREF
R175 10K 1%
TRMB1 10K
VTIN2
R176 30K 1%
VTIN1
CPUDXP 3
TRCPU1
C158
Do Not Stuff
GND
U4
W83627HF
VCORE +5V
VREF
+3V
+12VIN
GND
SMBCLK 8,12,14,15,31
SMBDATA 8,12,14,15,31
IRRX 24
IRTX 24
+3VSB
R304 0 /9739 For 14.318MHz
SUSCLKIN 9
R307 0 /9739 For 14.318MHz
GPIO8 9
R308 0 /9739 For 14.318MHz
PWRBTN# 9,23
LMSDATA
LMSCLK
+12VIN
R180 28K 1%
R181 10K 1%
24 DENSEL
24 IDX#
24 MTR#0
24 DRV#1
24 DRV#0
24 MTR#1
24 DIR#
24 STEP#
24 WD#
24 WG#
24 TRAK0#
24 WP#
24 RD#
24 HDSEL#
24 DSKCHG#
15 48M_SIO
9 IOPME#
15 PCLK_SIO
8,25 LAD[0..3]
8,25 LFRAME#
5,8,16,23,25,27 PCIRST_SB#
24 XSLCT
24 PE
24 BUSY
24 ACK#
XPD[0..7]
24 XPD[0..7]
24 PE
24 BUSY
24 ACK#
24 ERROR#
24 XSLIN#
24 XINIT#
24 XAFD#
24 XSTB#
24 XSLCT
24 DCD#1
24 DSR#1
24 RXD1
24 RTS#1
24 TXD1
24 CTS#1
24 DTR#1
24 RI#1
9 A20GATE
9 KBDRST#
24 LKBDATA
24 LKBCLK
24 LMSDATA
24 LMSCLK
+5V
+5VSB
C161 0.1U
C162 0.1U
C163 0.1U
C164 0.1U
C160 0.1U
GND
CPU_FAN1
FANIN_CPU
R182 8.2K
C159 Do Not Stuff
CB82 Do Not Stuff
3 PIN
CHA_FAN1
FANIN_CHA
R183 8.2K
CB83 Do Not Stuff
C165 Do Not Stuff
http://laptop-motherboard-schematic.blogspot.com/
NOT
Title : SIO W83627HF-AW
ASRock Computer Inc.
Engineer: MARS_TSENG
Size A3
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 21 of 31

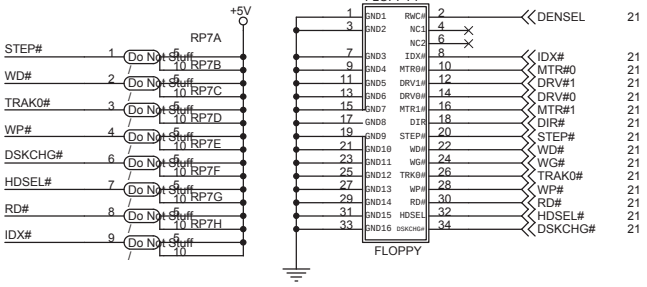

U5
CMI9739
ALC201: 1uF
ALC201: None
When front panel isn't installed or for some chassis, the jumper must be added on JR1,JL1. Otherwise, the backpanel can't use
XTALS0 XTALS1 PIN2.XIN
0 0 12.288MHz
0 1 14MHz
1 x 14.318MHz
Change C204 to 5.6K ohm for voltage bias.
Title : AC97
ASRock Computer Inc.
Engineer: MARS_TSENG
Project Name
P4I45GL
Size Custom
Rev 1.00
Date: Friday, January 17, 2003
Sheet 22 of 31
http://laptop-motherboard-schematic.blogspot.com/


FRONT PANEL
http://laptop-motherboard-schematic.blogspot.com/
silk screen?
ACPILED is Hi-Z in S4/S5. defined in others.
After RSMRST#, it's "Output Low"!
Around the ATX Power Connector
Title : POK_DUALSW
ASRock Computer Inc.
Engineer: MARS_TSENG
Size Custom
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 23 of 31

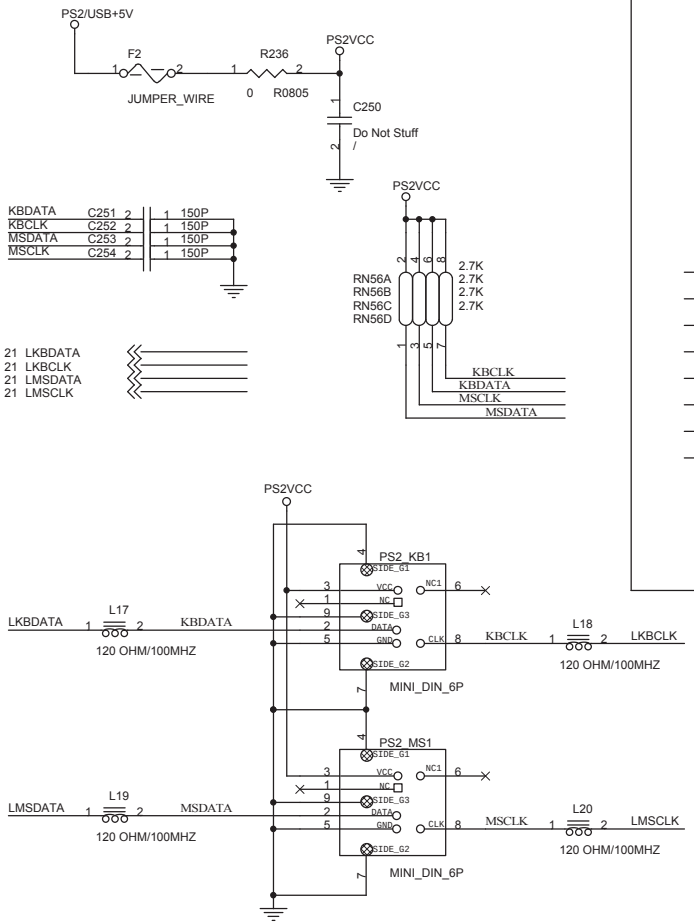
COM1



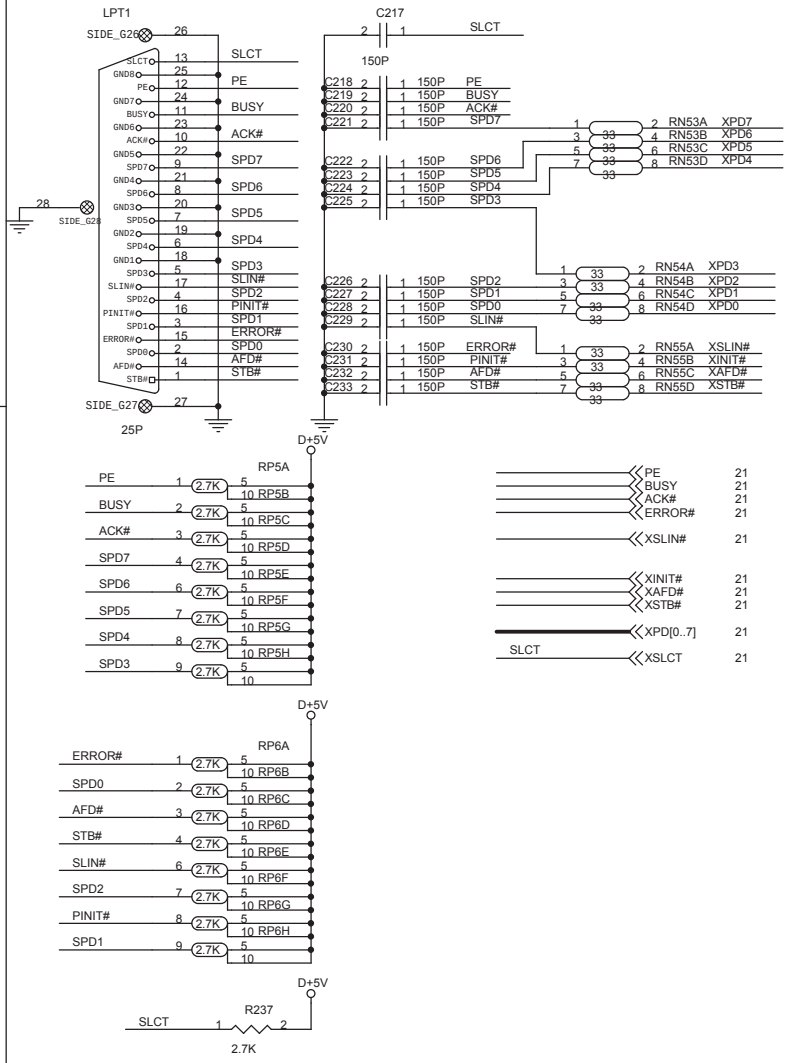
FDD



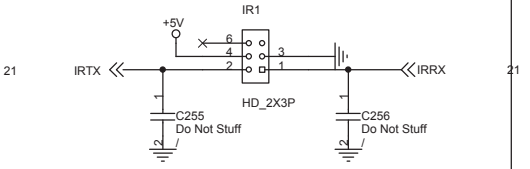
KB/MOUSE



Parallel Port

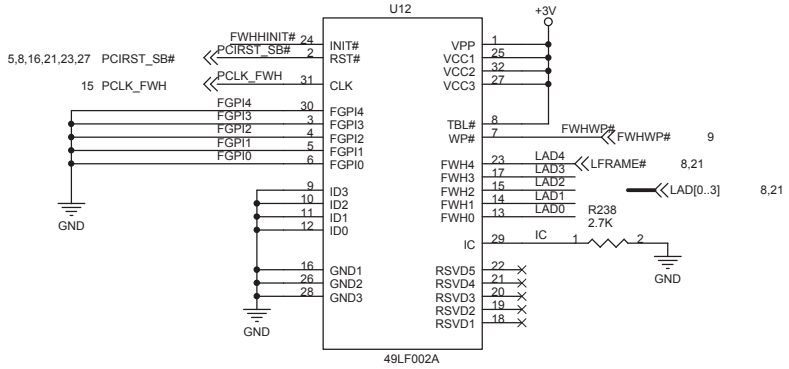


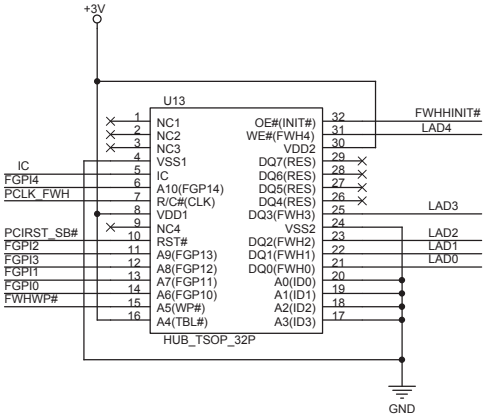
IR

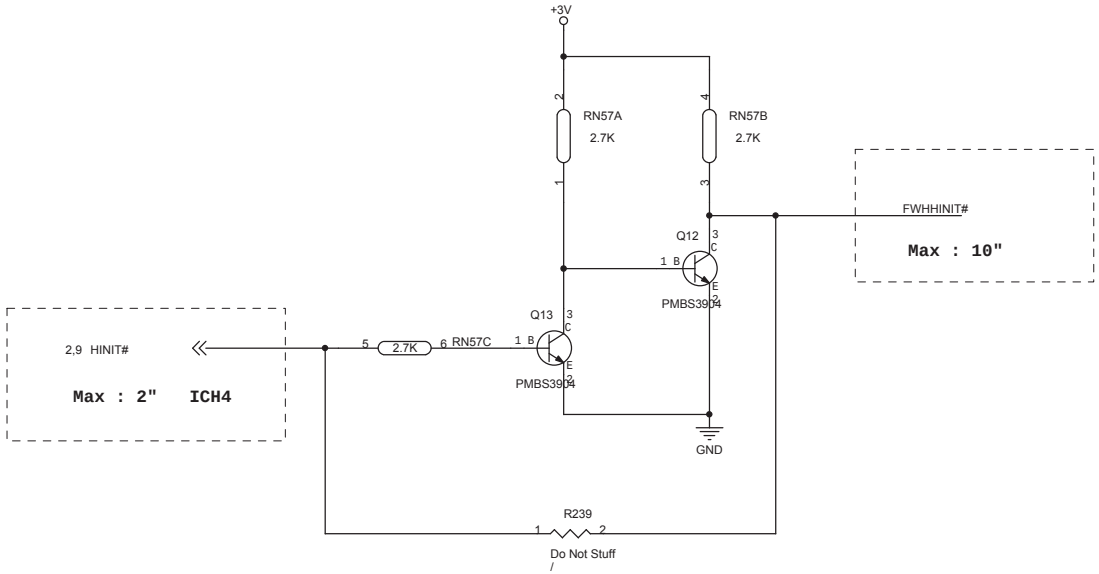


NOT

ASUS	Title :	IO Connector
ASRock Computer Inc.	Engineer:	MARS_TSENG
Size A3	Project Name: P4I45GL	Rev 1.00
Date: Friday, January 17, 2003	Sheet 24 of 31	







NOT

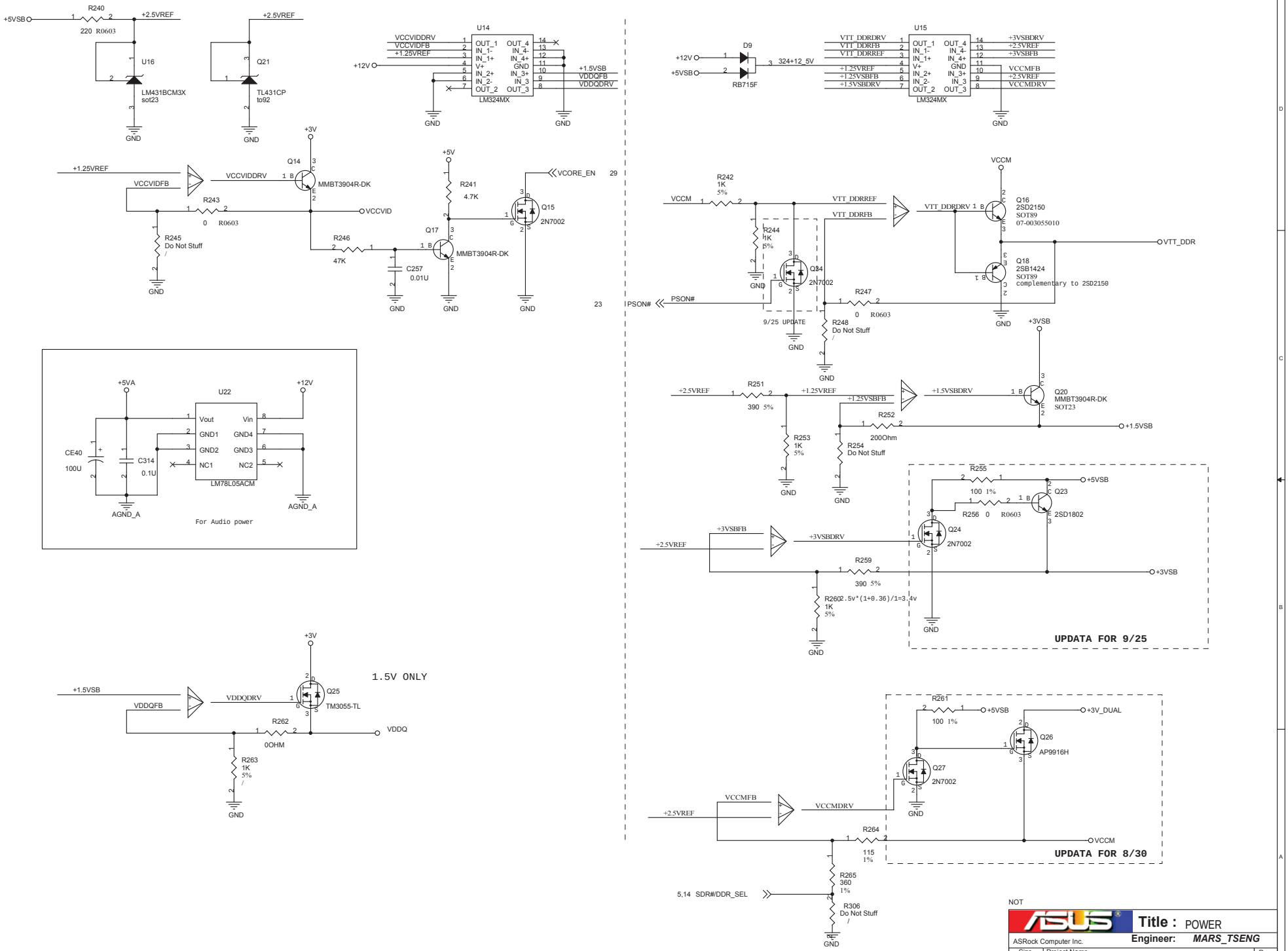
ASRock Computer Inc.

Title : FWH

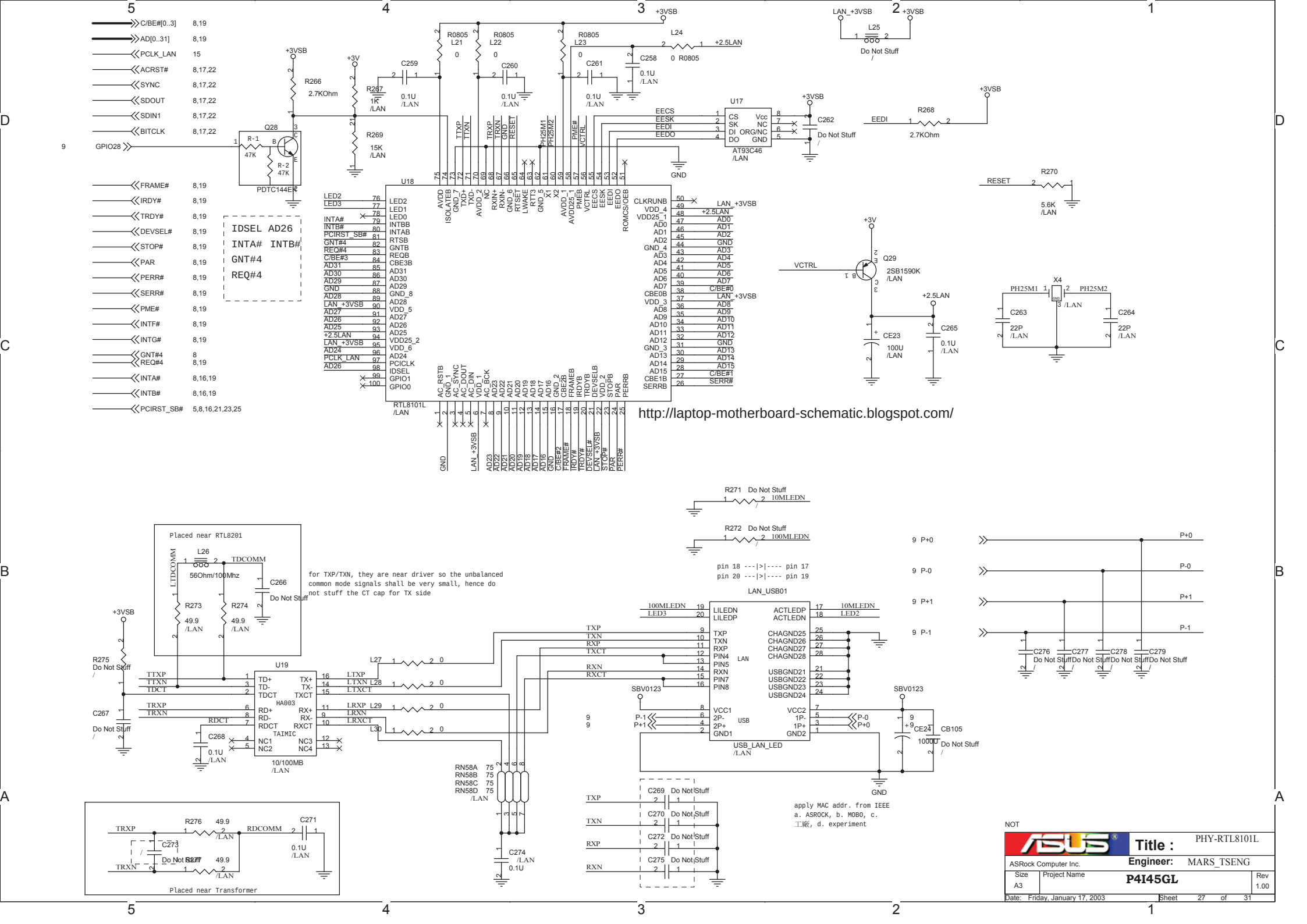
Engineer: MARS_TSENG

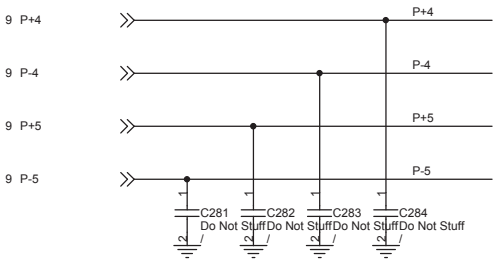
Size	Project Name	Rev
A3	P4I45GL	1.00

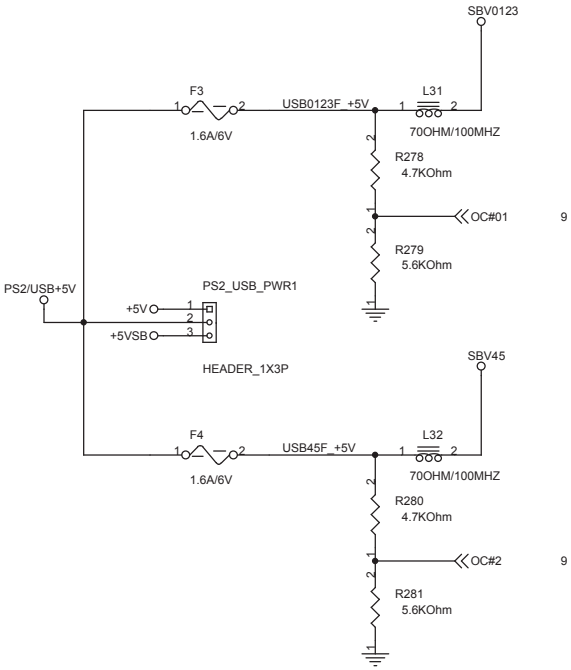
Date: Friday, January 17, 2003 Sheet 25 of 31



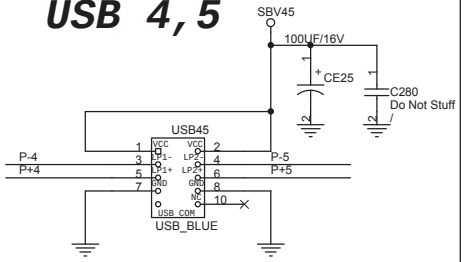
ASRock Computer Inc.	Title : POWER	
	Engineer: MARS_TSENG	
Size: Custom	Project Name: P4I45GL	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 26 of 31	

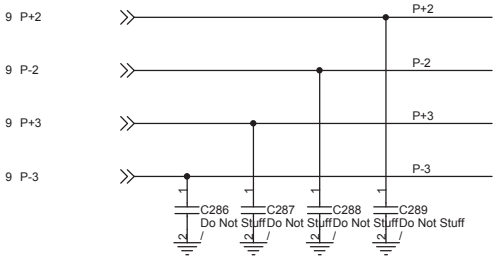

C/BE#[0..3] 8,19
AD[0..31] 8,19
PCLK_LAN 15
ACRST# 8,17,22
SYNC 8,17,22
SDOUT 8,17,22
SDIN1 8,17,22
BITCLK 8,17,22
GPIO28
FRAME# 8,19
IRDY# 8,19
TRDY# 8,19
DEVSEL# 8,19
STOP# 8,19
PAR 8,19
PERR# 8,19
SERR# 8,19
PME# 8,19
INTF# 8,19
INTG# 8,19
GNT#4 8
REQ#4 8,19
INTA# 8,16,19
INTB# 8,16,19
PCIRST_SB# 5,8,16,21,23,25
IDSEL AD26
INTA# INTB#
GNT#4
REQ#4
Q28
PDTC144EK
R266 2.7KOhm
R267 1K /LAN
R269 15K /LAN
R-1 47K
R-2 47K
R0805 L21 0
R0805 L22 0
R0805 L23 0
L24 +2.5LAN
L25 Do Not Stuff /
C258 0.1U /LAN
C259 0.1U /LAN
C260 0.1U /LAN
C261 0.1U /LAN
U17 AT93C46 /LAN
EECS EESK EEDI EEDO
C262 Do Not Stuff /
R268 2.7KOhm
EEDI
U18 RTL8101L /LAN
R270 5.6K /LAN
RESET
Q29 2SB1590K /LAN
VCTRL
CE23 100U /LAN
C265 0.1U /LAN
X4
C263 22P /LAN
C264 22P /LAN
PH25M1 PH25M2
R271 Do Not Stuff 10MLEDN
R272 Do Not Stuff 100MLEDN
pin 18 ---|>|---- pin 17
pin 20 ---|>|---- pin 19
LAN_USB01
USB_LAN_LED /LAN
SBV0123
CE24 10000 Do Not Stuff /
CB105
C276 C277 C278 C279 Do Not Stuff
P+0 P-0 P+1 P-1
Placed near RTL8201
L26 56Ohm/100Mhz
C266 Do Not Stuff
R273 49.9 /LAN
R274 49.9 /LAN
for TXP/TXN, they are near driver so the unbalanced common mode signals shall be very small, hence do not stuff the CT cap for TX side
U19 HA003 TAIMIC 10/100MB /LAN
R275 Do Not Stuff /
C267 Do Not Stuff /
C268 0.1U /LAN
L27 L28 L29 L30
RN58A RN58B RN58C RN58D 75 /LAN
C269 C270 C272 C275 Do Not Stuff
C274 /LAN 0.1U
apply MAC addr. from IEEE
a. ASROCK, b. MOBO, c. 工廠, d. experiment
Placed near Transformer
R276 49.9 /LAN
R277 49.9 /LAN
C271 0.1U /LAN
C273 Do Not Stuff /
http://laptop-motherboard-schematic.blogspot.com/
NOT
ASRock Computer Inc.
Title : PHY-RTL8101L
Engineer: MARS_TSENG
Size A3
Project Name P4I45GL
Rev 1.00
Date: Friday, January 17, 2003
Sheet 27 of 31



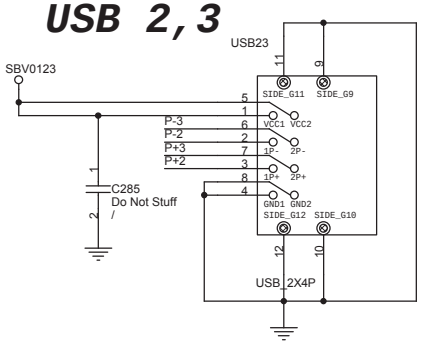


USB 4,5



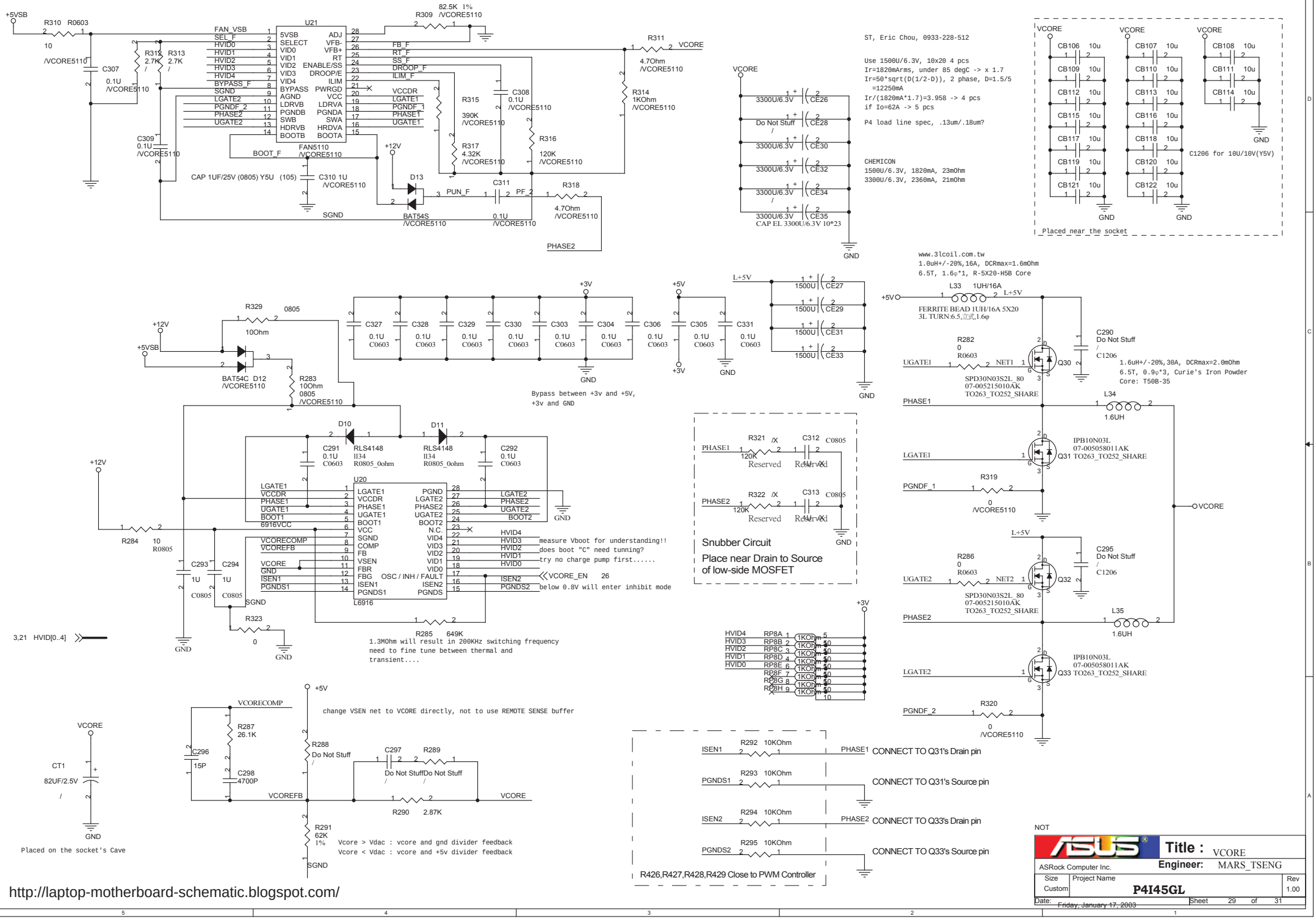


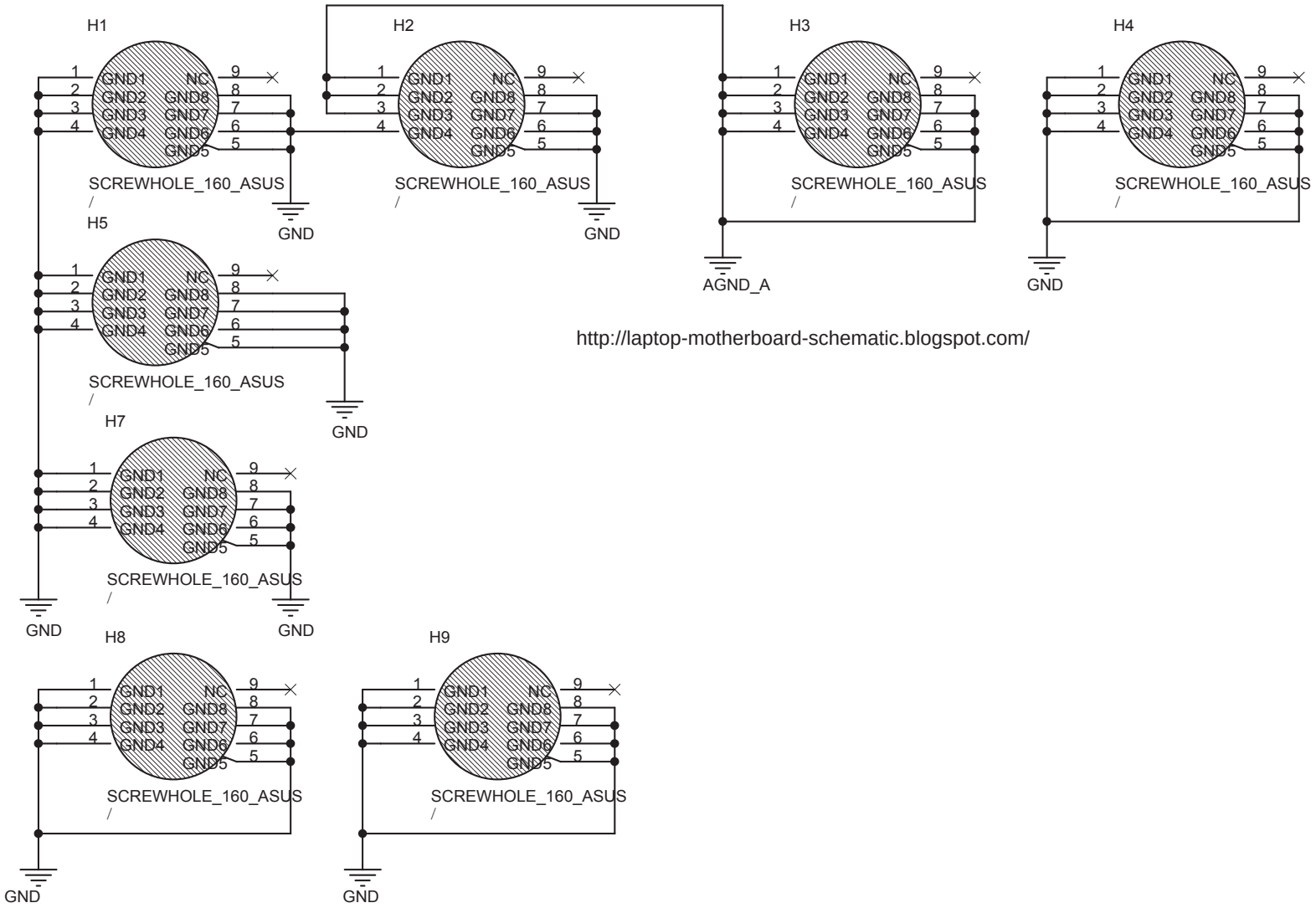
USB 2,3



NOT

ASRock Computer Inc.	Title : USB PORT	
	Engineer: MARS_TSENG	
Size: A3	Project Name: P4I45GL	Rev: 0.1
Date: Friday, January 17, 2003	Sheet 28 of 31	

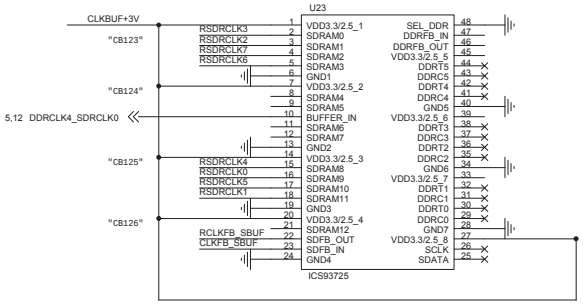


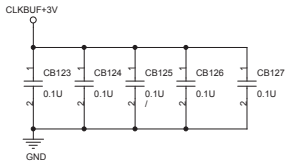


http://laptop-motherboard-schematic.blogspot.com/

NOT

ASRock Computer Inc.	Title : MECHANICAL	
	Engineer: *MARS_TSENG*	
Size: A	Project Name: **P4I45GL**	Rev: 1.00
Date: Friday, January 17, 2003	Sheet 30 of 31	



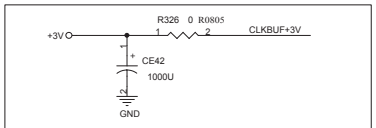



```
ddr dimm x8:
  double side, 6+6+(4+2*cap)
  single side, 3+3+(2+1*cap)
ddr dimm x16:
  double side, ?
  single side, ?
```

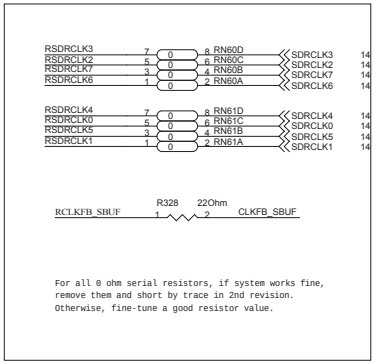
```
P4S533-VM 1.01

DCLK0  2769mil
DCLK0# 2805mil
DCLK1  2738mil
DCLK1# 2707mil
DCLK2  2861mil
DCLK2# 2802mil
DCLK3  2842mil
DCLK3# 2838mil
DCLK4  2775mil
DCLK4# 2765mil
DCLK5  2821mil
DCLK5# 2843mil

SDCLK  5366mil(繞)
FWDSDCLKO  4452mil(shortest)
FBCLKIN  9033mil(繞)

MD4(3987mil)+MDD4(881mil)
MA14(3421mil)+MAA14(953mil)
MD60(2485mil)+MDD60(856mil)
MD59(1748mil)+MDD59(1859mil)
AVG(MD) ~ 2867mil
```

```
CPUCLK  5285mil
CPUCLK# 5196mil
NBHCLK  3639mil
NBHCLK# 3627mil
NBZCLK  5651mil
SBZCLK 5679mil
NBAGPCLK 4217mil
AGPCLK 1628mil(+3.5")
961PCLK 6154mil(沒繞,最長)
SIOPCLK 5189mil(TOL
1000mil)
```

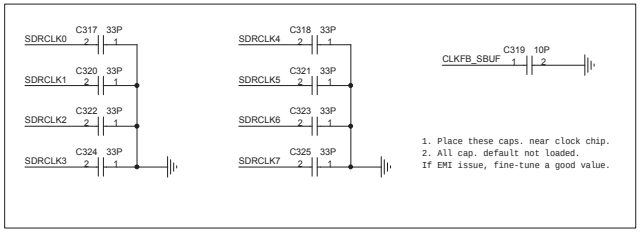
1. Place first cap. near clock chip and second one near the destination.
2. For PCI CLK, place the cap. near clock chip.
3. All cap default not loaded. If EMI has problem, we can try to load the cap. near clock chip.
4. SDRCLK and DDRCLK shall try 33P in source cap. for better driving.



1. R108 and R109 can be replaced by ferrite bead if necessary. These two resistors can't be removed and replaced by trace.
2. For CYPRESS, default load R108, R112 and R113.
3. For ICS, default load R109, R112 and R113.
R112 and R113 needs to change to 0 ohm resistors for ICS chip.
4. Be careful of the jitter for using 2 4.3ohm for CYPRESS chip.



For all 0 ohm serial resistors, if system works fine, remove them and short by trace in 2nd revision.
Otherwise, fine-tune a good resistor value.



1. Place these caps. near clock chip.
2. All cap. default not loaded.
If EMI issue, fine-tune a good value.

NOT

ASROCK Computer Inc.	Title : SDR ZDB	
	Engineer: *Ren-Jian Wang*	
Size: C	Project Name: **P4I45GL**	Rev: 1.0
Date: Friday, January 17, 2003	Sheet 31 of 31	