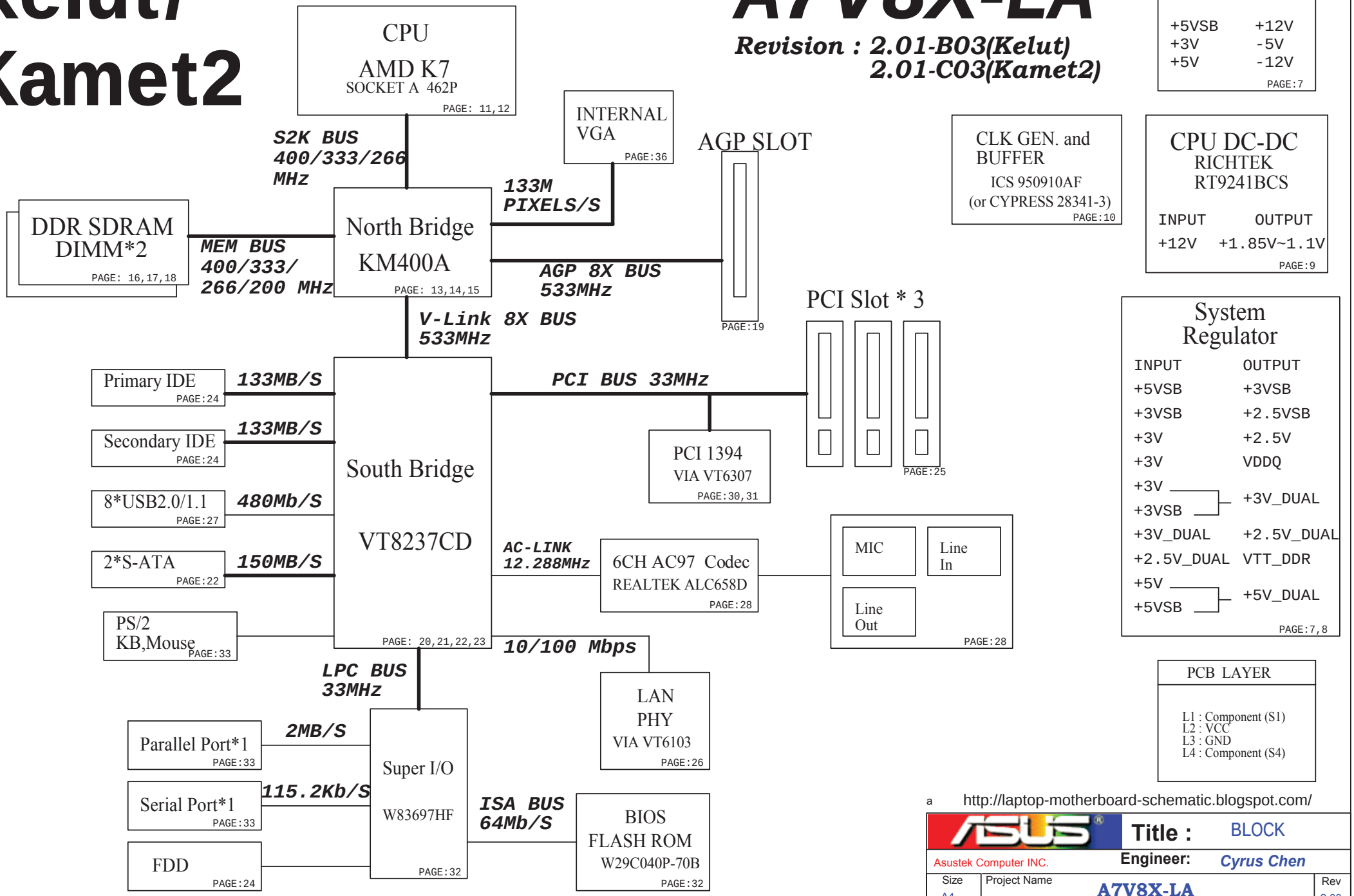
Kelut/ Kamet2

A7V8X-LA

Revision : 2.01-B03(Kelut)
2.01-C03(Kamet2)



ATX Power

+5VSB	+12V
+3V	-5V
+5V	-12V

PAGE:7

CLK GEN. and BUFFER

ICS 950910AF
(or CYPRESS 28341-3)
PAGE:10

CPU DC-DC

RICHTEK
RT9241BCS

INPUT	OUTPUT
+12V	+1.85V~1.1V

PAGE:9

System Regulator

INPUT	OUTPUT
+5VSB	+3VSB
+3VSB	+2.5VSB
+3V	+2.5V
+3V	VDDQ
+3V +3VSB	+3V_DUAL
+3V_DUAL	+2.5V_DUAL
+2.5V_DUAL	VTT_DDR
+5V +5VSB	+5V_DUAL

PAGE:7,8

PCB LAYER

L1 : Component (S1)
L2 : VCC
L3 : GND
L4 : Component (S4)

Asustek Computer INC.	Title : BLOCK	
	Engineer: Cyrus Chen	
Size: A4	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 1 of 40	

Sheet Index

Sheet	Sheet Title	Description
1	BLOCK	BLOCK
2	CONTENT	SHEET INDEX & HISTORY OF MAIN BOARD VERSION
3	CLOCK DISTRIBUTION	CLOCK DISTRIBUTION
4	RESET MAP	RESET MAP
5	POWER CONSUMPTION	POWER CONSUMPTION
6	POWER SUPPLY BLOCK DIAGRAM	POWER SUPPLY BLOCK DIAGRAM
7	ATX & SYS PWR	ATX & SYS PWR
8	SYS PWR	SYS PWR
9	CPU PWR	CPU PWR
10	CLOCK	CLOCK GEN. ICS 950910AF
11	CPU_1	CPU (AMD K7 SOCKET A 462P)
12	CPU_2	CPU (AMD K7 SOCKET A 462P)
13	NORTH BRIDGE_1	HOST BUS
14	NORTH BRIDGE_2	MEMORY PART
15	NORTH BRIDGE_3	AGP, VLINK, VGA
16	DDR DAMPING	SERIES RESISTOR
17	DDR DIMM	DDR SOCKET 1 , 2
18	DDR TERMINATION	TERMINATION
19	AGP8X	AGP 8X SLOT
20	VT8237_1	IDE, USB0-5, POWER&GND
21	VT8237_2	PCI , MII , AC97 INTERFACE
22	VT8237_3	SATA , USB6,7 INTERFACE
23	VT8237_4	STRAPING, PULL-UP RESISTOR
24	IDE & FLOPPY	IDE1,IDE2 CONNECTOR & FLOPPY
25	PCI SLOT	PCI SLOT 1,2,3
26	LAN PHY	VIA VT6103
27	USB PORT	USB CONNECTOR
28	AC97 AUDIO CODEC	REALTEK ALC658D
29	BOM TABLE OF CODEC	BOM TABLE OF CODEC
30	IEEE1394	VIA VT6307
31	IEEE1394 CONNECTOR	IEEE1394 CONNECTOR
32	SUPER IO	Windbond W83697HF
33	KB,MOUSE & IO CONNECTOR	KB,MOUSE & IO CONNECTOR
34	FID & VID	FID & VID
35	FAN	FAN
36	VGA CONNECTOR	VGA CONNECTOR
37	PANEL & AS016	PANEL & AS016
38	EMI CAP. & SCREW HOLES	EMI CAP. & SCREW HOLES
39	INI & ID TABLE	INI & ID TABLE
40	GPIO TABLE	GPIO TABLE

Revision History

Date	Version	Change Note
92.6.3	1.02	1. Fix LAN LED issue 2. Fix power noise issue

a

ASUSTEK COMPUTER INC	Title : CONTENT	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
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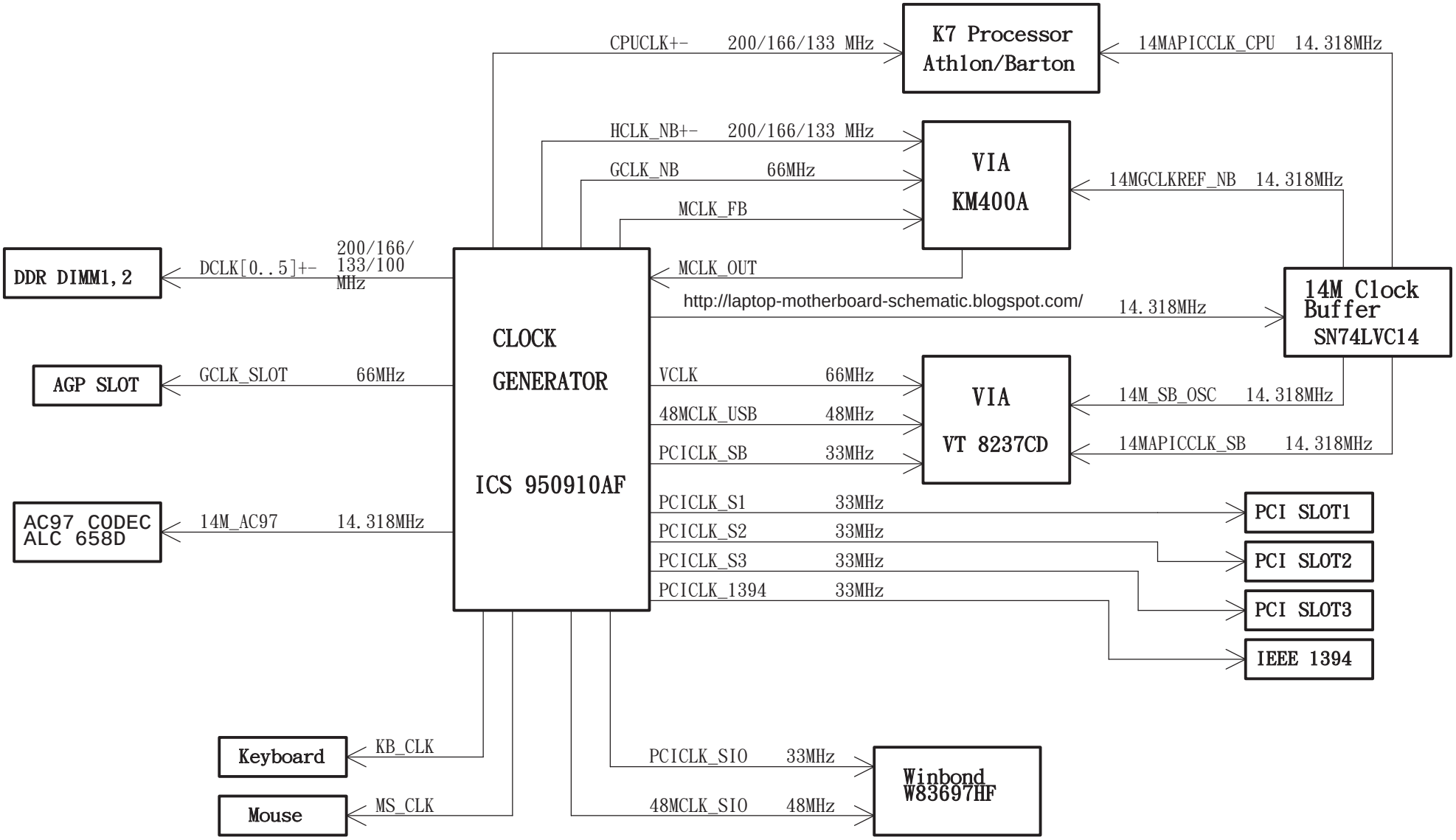
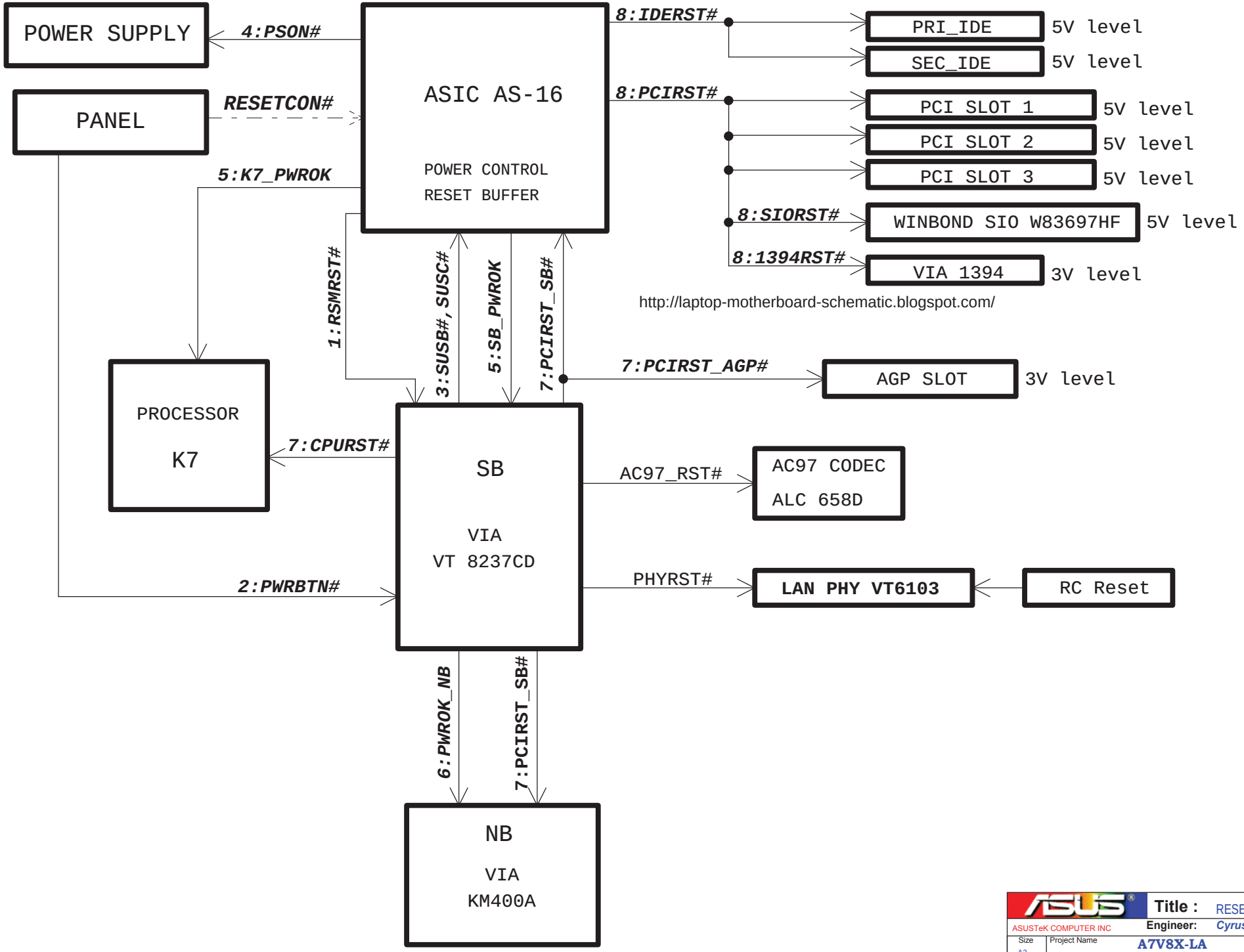


a

ASUSTEK COMPUTER INC.	Title : CLOCK DISTRIBUTION	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 3 of 40	



ASUSTeK COMPUTER INC	Title : RESET MAP	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 4 of 40	

ATX POWER

CWT-300W

+5V	30A 150W
+3V	14A 46.2W
+12V	15A 180W
+5VSB	2A 10W
-12V	0.5A 6W
-5V	0.5A 2.5W

AMD Athlon

VCORE (1.6~1.7V) — 48A

KM400A

VCORE	
VDDQ(+1.5V)	
+2.5V	2.5A(NB+SB)
+3V	
+2.5VSB	
+2.5V_DUAL	

VT8237

BATT(+3V)	
+2.5V	2.5A(NB+SB)
+3V	
+2.5VSB	
+3VSB	

DDR DIMM X 2

VTT_DDR(+1.25V)	0.9A/each
+2.5V_DUAL	3A/each

AGP SLOT

VDDQ(+1.5V)	2A
+3V	6A
+5V	2A
+12V	1A
+3VSB	0.375A

PCI SLOT X 3

+3V	7.6A/each
+5V	5A/each
+12V	0.5A/each
-12V	0.1A/each
+3VSB	0.375A/each

LAN PHY(VT6103)

+3VSB

SIO(W83697HF)

BATT
VCORE
+3V
+5V
+12V
+5VSB

1394(VT6307)

+12V	
+3VSB	
+3V_DUAL	

USB PORT X 8

+5V	0.5A/each
+5VSB	0.04A/each

PS2 KB/MS

+5V	0.3A 1.5W
+5VSB	0.1A 5W

HD

+5V	0.7A 3.5W
+12V	0.7A 8.4W

CD ROM

+5V	0.7A 3.5W
+12V	0.7A 8.4W

FLOPPY

+5V	0.475A 2.8W
+12V	0.25A 3W

a

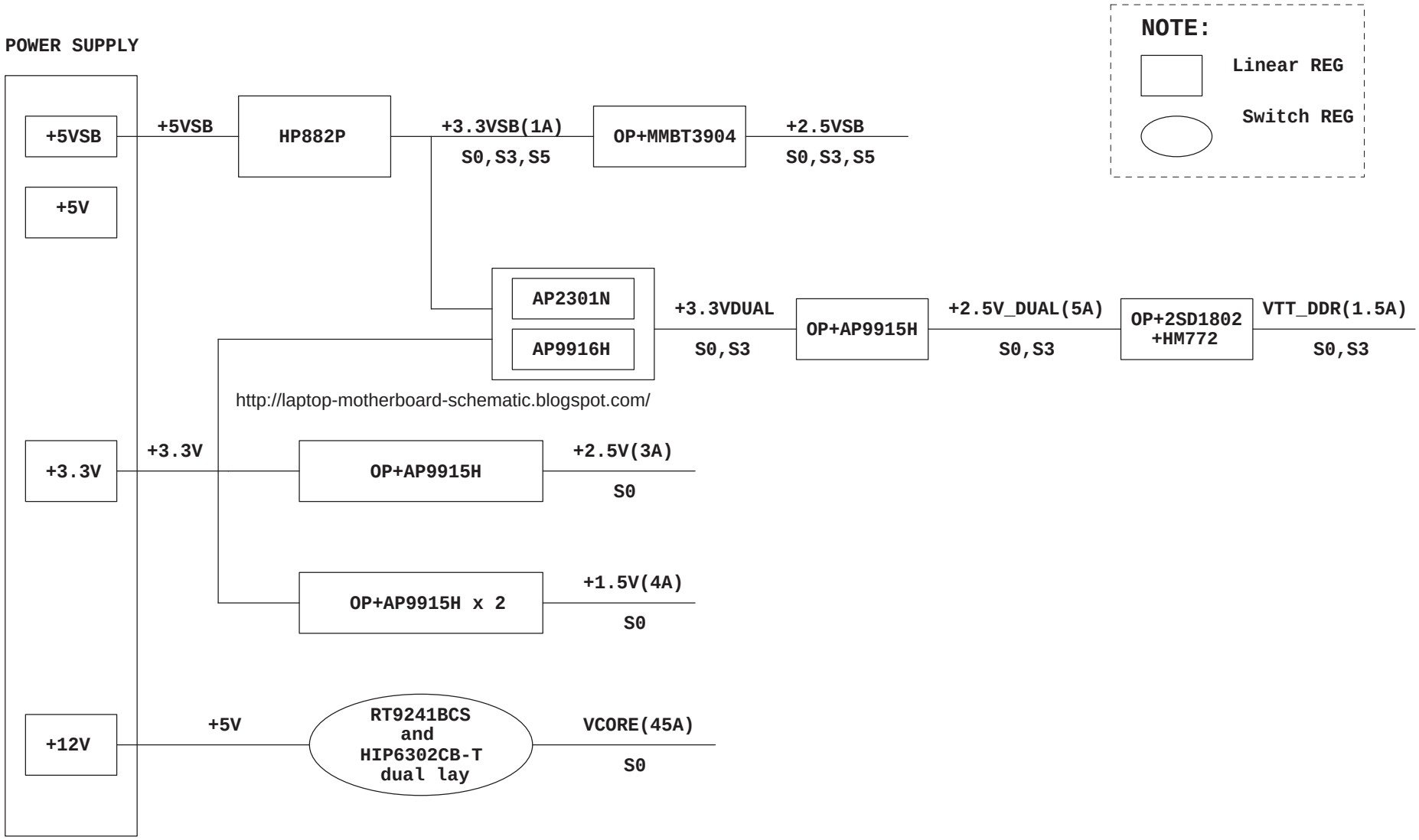
ASUS

Title : Power consumption

<OrgName> Engineer: Cyrus Chen

Size	Project Name	Rev
B	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 5 of 40



a

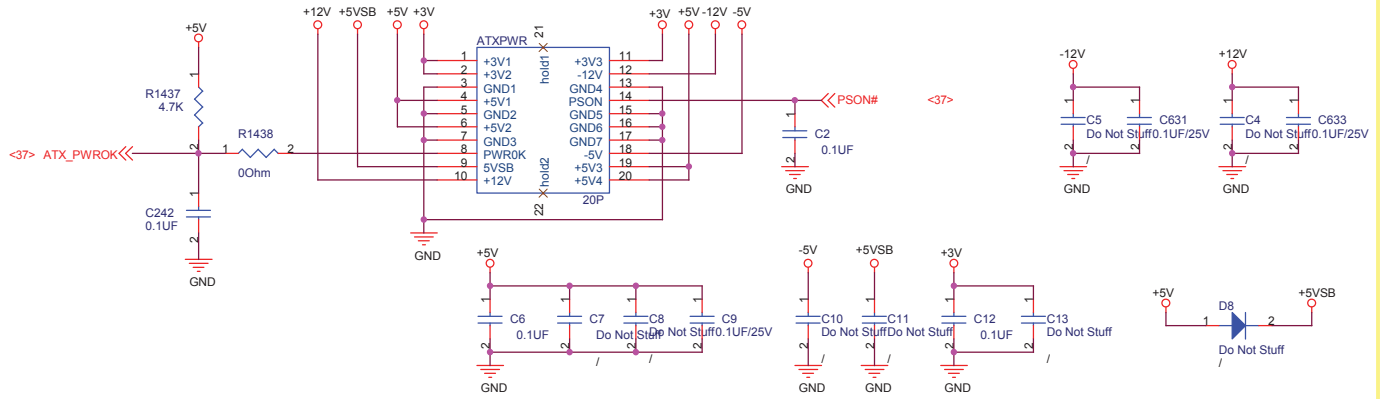
Title : POWER SUPPLY

Asustek Computer INC. Engineer: Cyrus Chen

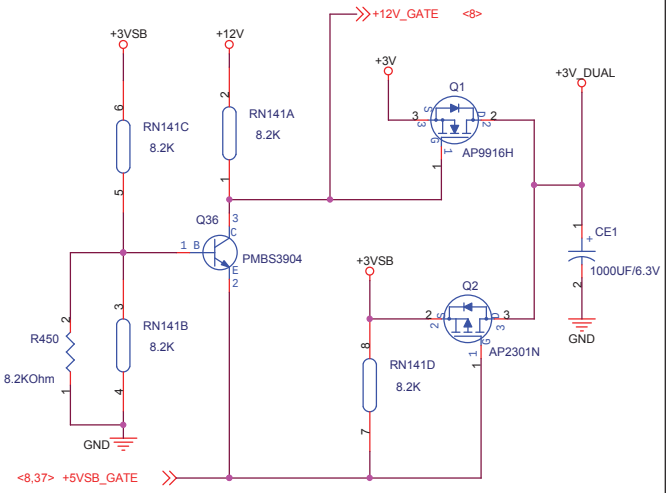
Size	Project Name	Rev
A3	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 6 of 40

ATX POWER



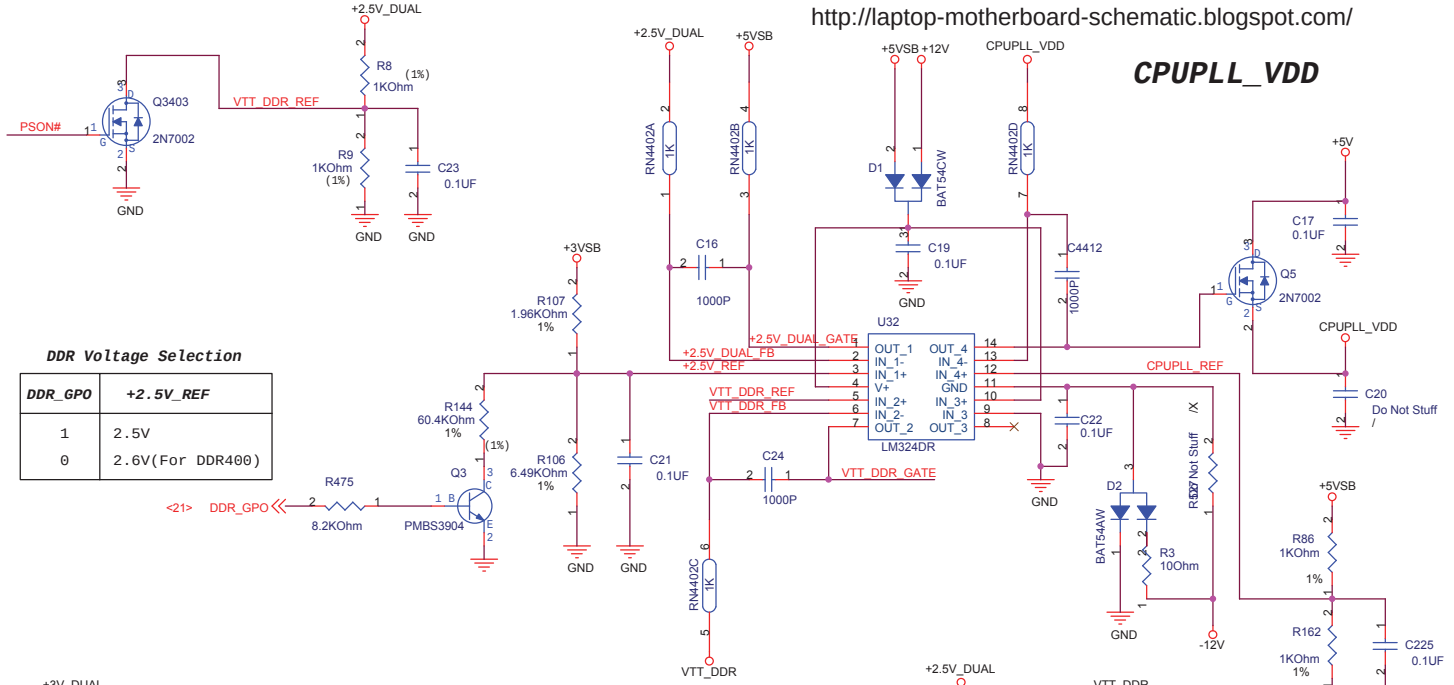
+3V and +3VSB DUAL SWITCH



STATE	S0,S1	S3	S4,S5
+5VSB_GATE	1	0	1

http://laptop-motherboard-schematic.blogspot.com/

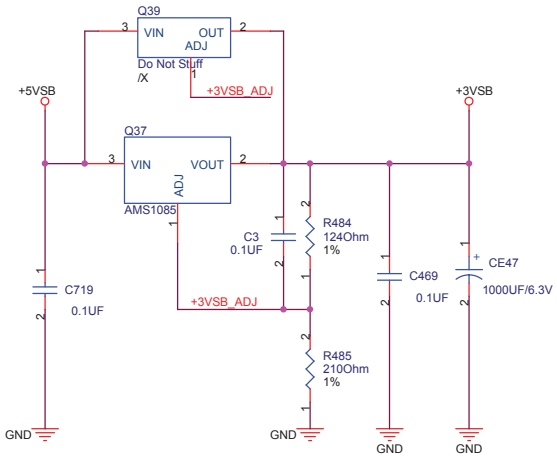
CPUPLL_VDD



DDR Voltage Selection

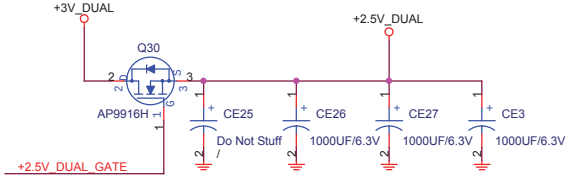
DDR_GPO	+2.5V_REF
1	2.5V
0	2.6V(For DDR400)

+5VSB ==> +3VSB

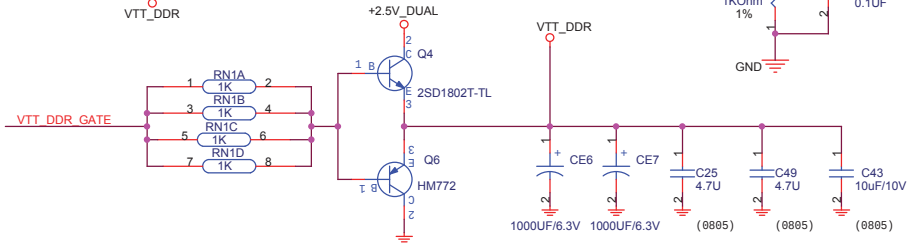


AMS1085 AND AMS2910 DUAL LAY

+3V_DUAL ==> +2.5V_DUAL

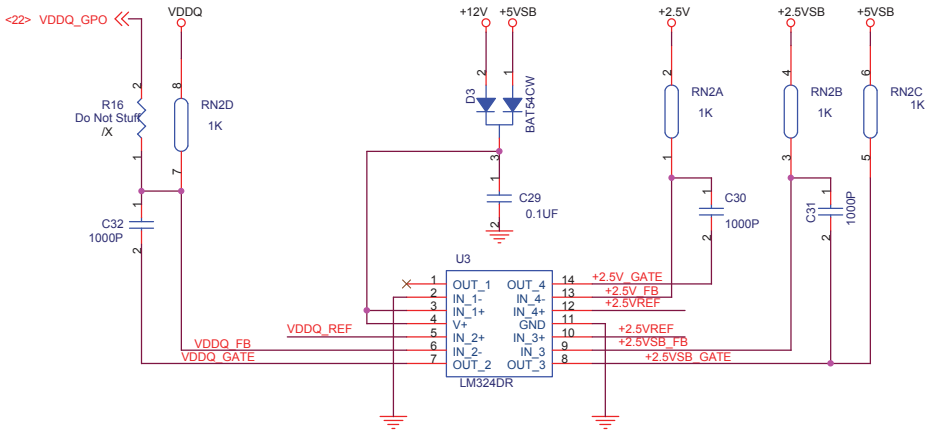


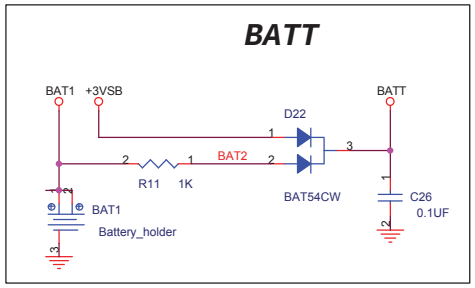
+2.5V_DUAL ==> VTT_DDR

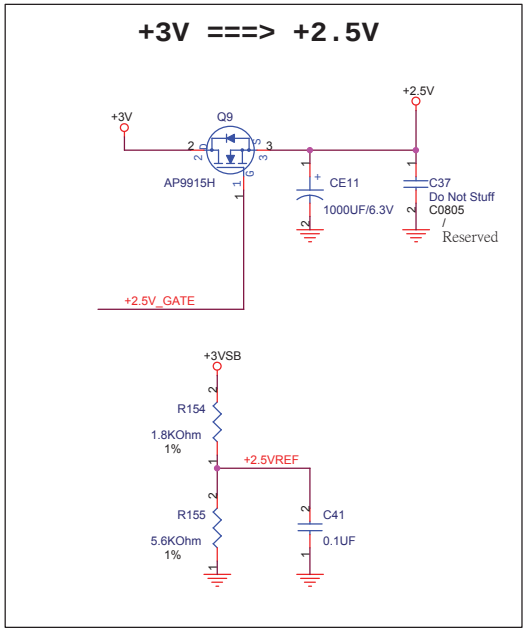


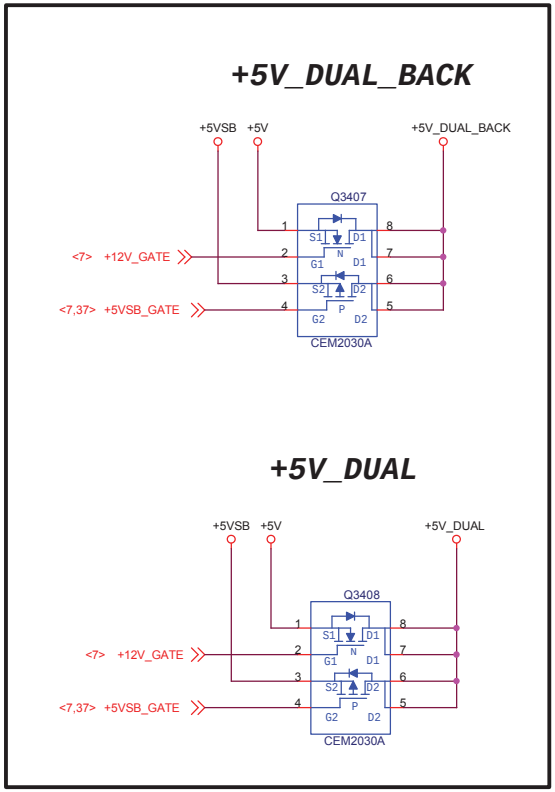
Reserved

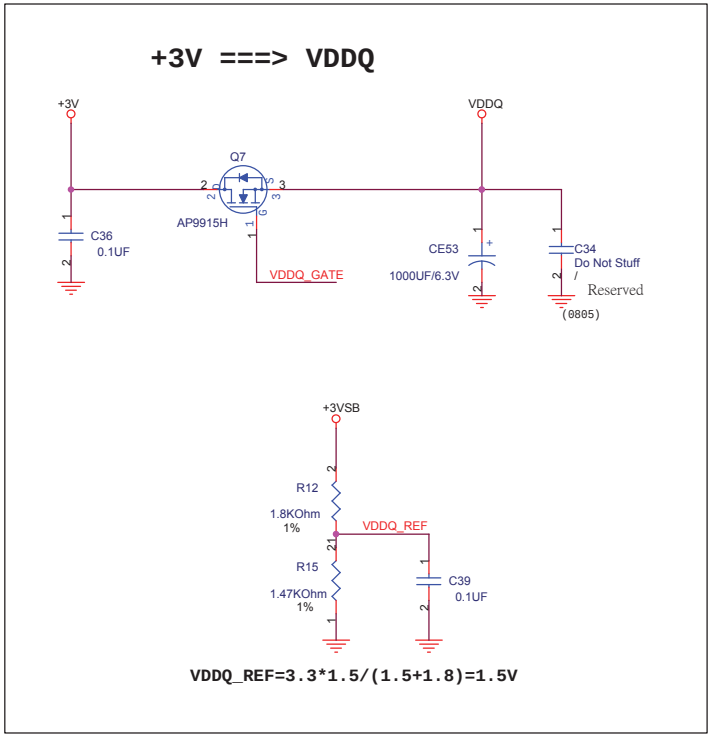
a			
ASUS	Title :	ATX & SYS PWR	
<OrgName>	Engineer:	Cyrus Chen	
Size A3	Project Name	A7V8X-LA	Rev 2.00
Date: Monday, October 13, 2003	Sheet 7	of 40	

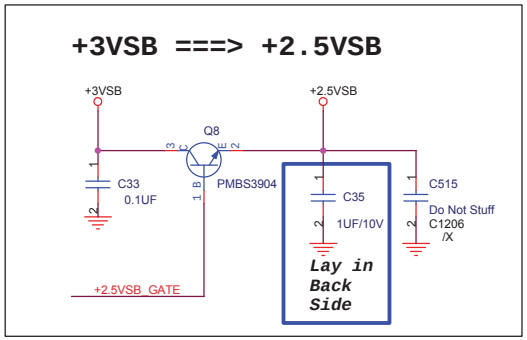












INCREASE Q7, Q9 POLYGON

a

ASUS	Title :	SYS PWR
<OrgName>	Engineer:	Cyrus Chen
Size A3	Project Name	A7V8X-LA
Rev 2.00		
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Vcore we use HIP6302 and RT9241 dual lay.
Normally used RT9241

PWM CONTROLLER

U34 /X

K7_VID4 K7_VID3 K7_VID2 K7_VID1 K7_VID0 VCORECOMP VCOREFB VCORE_EN_R

VID4 VID3 VID2 VID1 VID0 COMP FB FS/DIS VCC PGOOD ISEN1 PWM1 PWM2 ISEN2 VSEN GND

VCC+5V VRMPG1 ISP1 PWM1 PWM2 ISP2 VCOREFB FB-

Do Not Stuff

R82 Do Not Stuff R0805 /X Reserved

R459 10Ohm R0805

C674 1U

R465 750Ohm

R109 0Ohm

+5VSB +5V FB+ FB-

R98 4.7KOhm

C678 Do Not Stuff /

R468 Do Not Stuff /

R104 Do Not Stuff /

R464 12.1KOhm

C676 22P NP0

C677 0.033U X7R

R477 332KOhm /X

ATX12V POWER_CON_4P MH2

CPU_12V C28 0.1UF/25V

CPU_12V R463 10Ohm R0805

Adjust Voltage diff. between VCC and PVCC

U36 RT9602CS PWM DRIVER

PWM1 PWM2 GND LGATE1 PVCC LGATE2 PGND

VCC PHASE1 UGATE1 BOOT1 BOOT2 UGATE2 PHASE2

C685 1u C686 0.1U C687 0.1U

CAP 0.1UF/16V (0603) X7R (104)

http://laptop-motherboard-schematic.blogspot.com/

U35 RT9241BCS

K7_VID4 K7_VID3 K7_VID2 K7_VID1 K7_VID0 VCORECOMP VCOREFB VCORE_EN_R DVD S.S

VID4 VID3 VID2 VID1 VID0 COMP FB ADJ DVD SS VDD PGOOD ISP1 PWM1 PWM2 ISP2 VSEN GND ISN1 ISN2

VCC+5V VRMPGT ISP1 PWM1 PWM2 ISP2 VCOREFB FB- ISN1 ISN2

CPU_12V R480 12.1KOhm

R105 1.8KOhm

C682 0.1U X7R

<34> K7_VID[0..4]

DVD setting
(0.191/1.8)*(1.8+12.1)=9.1894V

CPU_12V L1 1UH L+12V

C42 1u CAP 1U/16V (1206) X7R (105)

UGATE1 R20 4.3Ohm RUGATE1

Q11 AP70T03H Q10 Do Not Stuff /X Reserved

R23 10K

PHASE1 L2 1.6UH/30A

P1 JP5 Do Not Stuff /

JP5 place near Q11 D pin

LGATE1 RLGATE1 R24 0Ohm

Q12 STD90NH02L Q13 Do Not Stuff /X Reserved

R27 10K

G1 JP3 Do Not Stuff /

JP3 place near Q12 S pin

L+12V C48 1u CAP 1U/16V (1206) X7R (105)

UGATE2 R36 4.3Ohm RUGATE2

Q14 AP70T03H Q15 Do Not Stuff /X Reserved

R38 10K

PHASE2 L3 1.6UH/30A

P2 JP8 Do Not Stuff /

JP8 place near Q14 D pin

LGATE2 RLGATE2 R39 0Ohm

Q16 STD90NH02L Q17 Do Not Stuff /X Reserved

R41 10K

G2 JP4 Do Not Stuff /

JP4 place near Q16 S pin

VCORE

Vcore:
Static loading spec is 48A
@1.75V +/- 50mV
Dynamic loading spec is
30A/us +150mV -100mV

ISP2 R112 3.9KOhm P2

ISP1 R113 3.9KOhm P1

ISN2 R116 3.9KOhm G2

ISN1 R132 3.9KOhm G1

VCORE

CB1 CB3 CB5 CB7 CB9 10UF/10V

CB2 CB4 CB6 CB8 CB10 10UF/10V

Do Not Stuff/

Placed near the socket(1206)

CE12 CE14 CE8 CE28 CE15 CE17 CE18 CE20 1500UF/6.3V

Do Not Stuff /

CAP EL 1500UF/6.3V 8*20

Placed near the socket

L+12V CE13 CE16 CE19 1200UF/16V

CAP EL 1200U/16V 10*25

PHASE1 PHASE2 R43 R45 1Ohm C51 C52 4700P R46 R47 0

Snubber Circuit

Place near Drain to Source of low-side MOSFET

CAP 4700PF/50V (0603)X7R (472)

RES 1 OHM 1/4W (1206)

<11> VCOREFB+ <11> VCOREFB-

VCORE JP1 JP2 Do Not Stuff

R49 R51 Do Not Stuff Reserved

VCORE_P8

Place near CPU Pin M8 P8

R44 10Ohm R50 10Ohm

C53 Do Not Stuff / Reserved

FB+ FB-

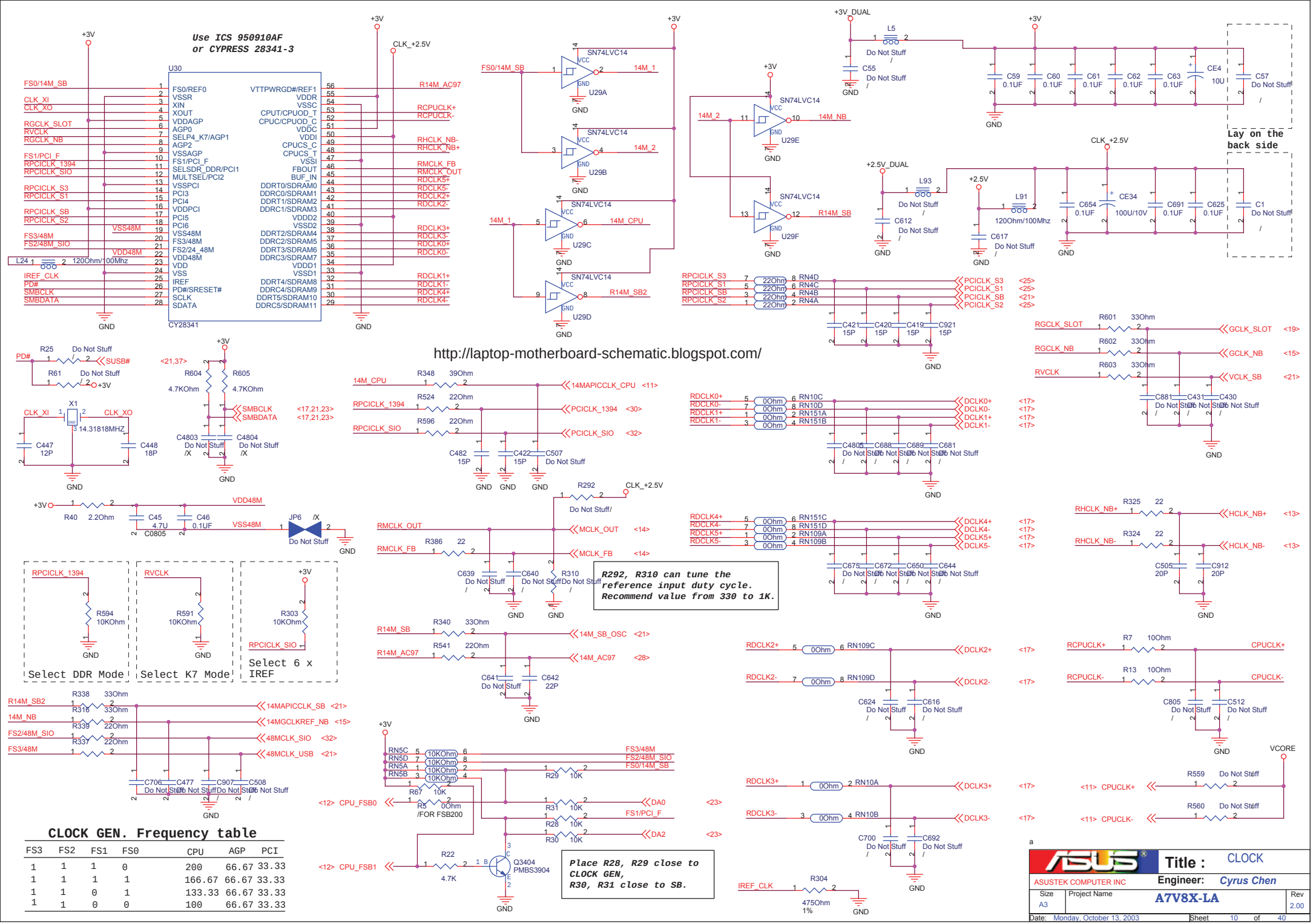
a

Title : CPU PWR

<OrgName> Engineer: Cyrus Chen

Size A3 | Project Name A7V8X-LA | Rev 2.00

Date: Monday, October 13, 2003 Sheet 9 of 40



CLOCK GEN. Frequency table

FS3	FS2	FS1	FS0	CPU	AGP	PCI
1	1	1	0	200	66.67	33.33
1	1	1	1	166.67	66.67	33.33
1	1	0	1	133.33	66.67	33.33
1	1	0	0	100	66.67	33.33

ASUSTEK COMPUTER INC

Title : CLOCK

Engineer: Cyrus Chen

Size: A3 | Project Name: A7V8X-LA | Rev: 2.00

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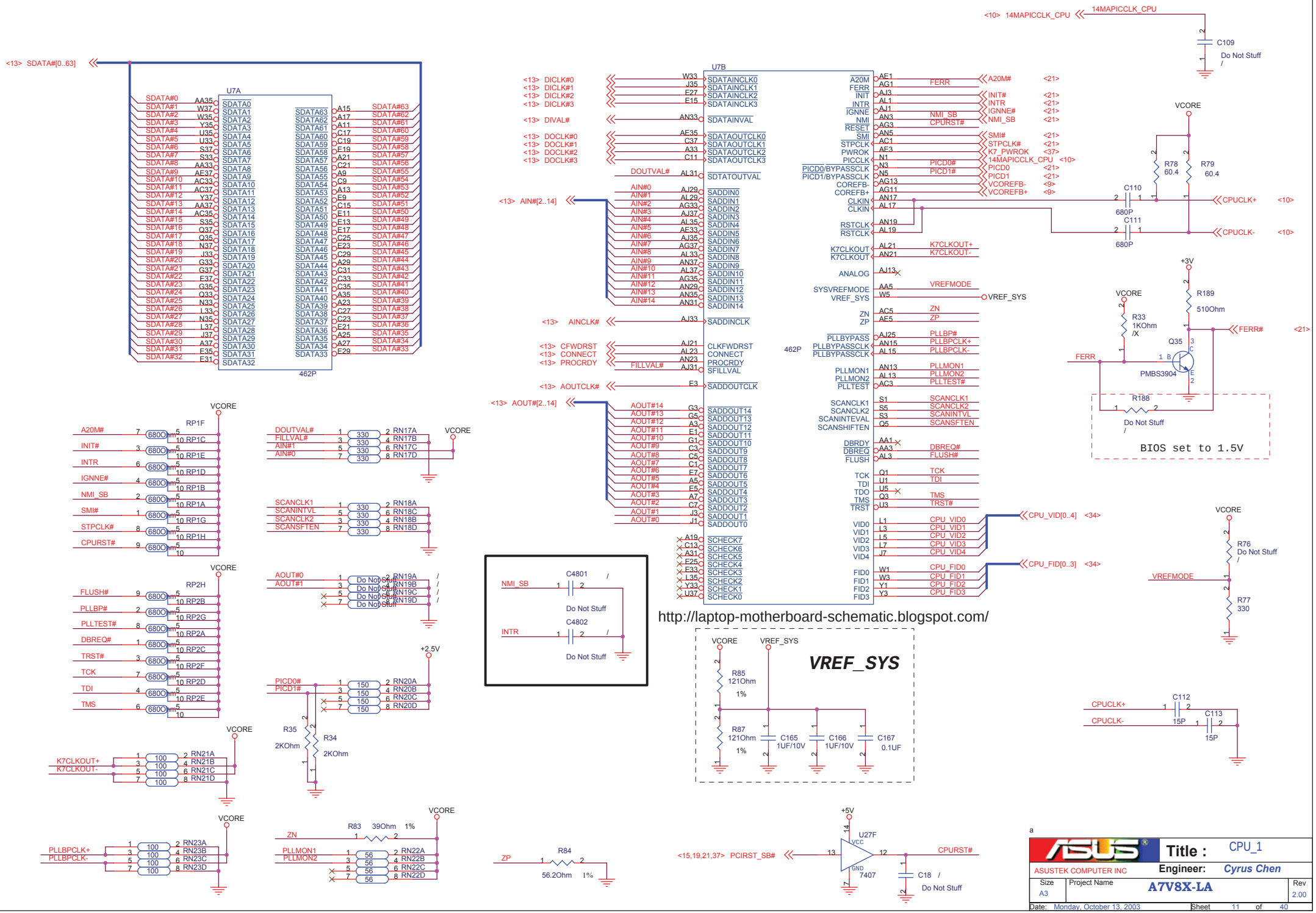
U7A
462P
U7B
462P
RP1F
RP2H
VCORE
+2.5V
+3V
+5V
VREF_SYS
BIOS set to 1.5V
Do Not Stuff
PMBS3904
http://laptop-motherboard-schematic.blogspot.com/
Title : CPU_1
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
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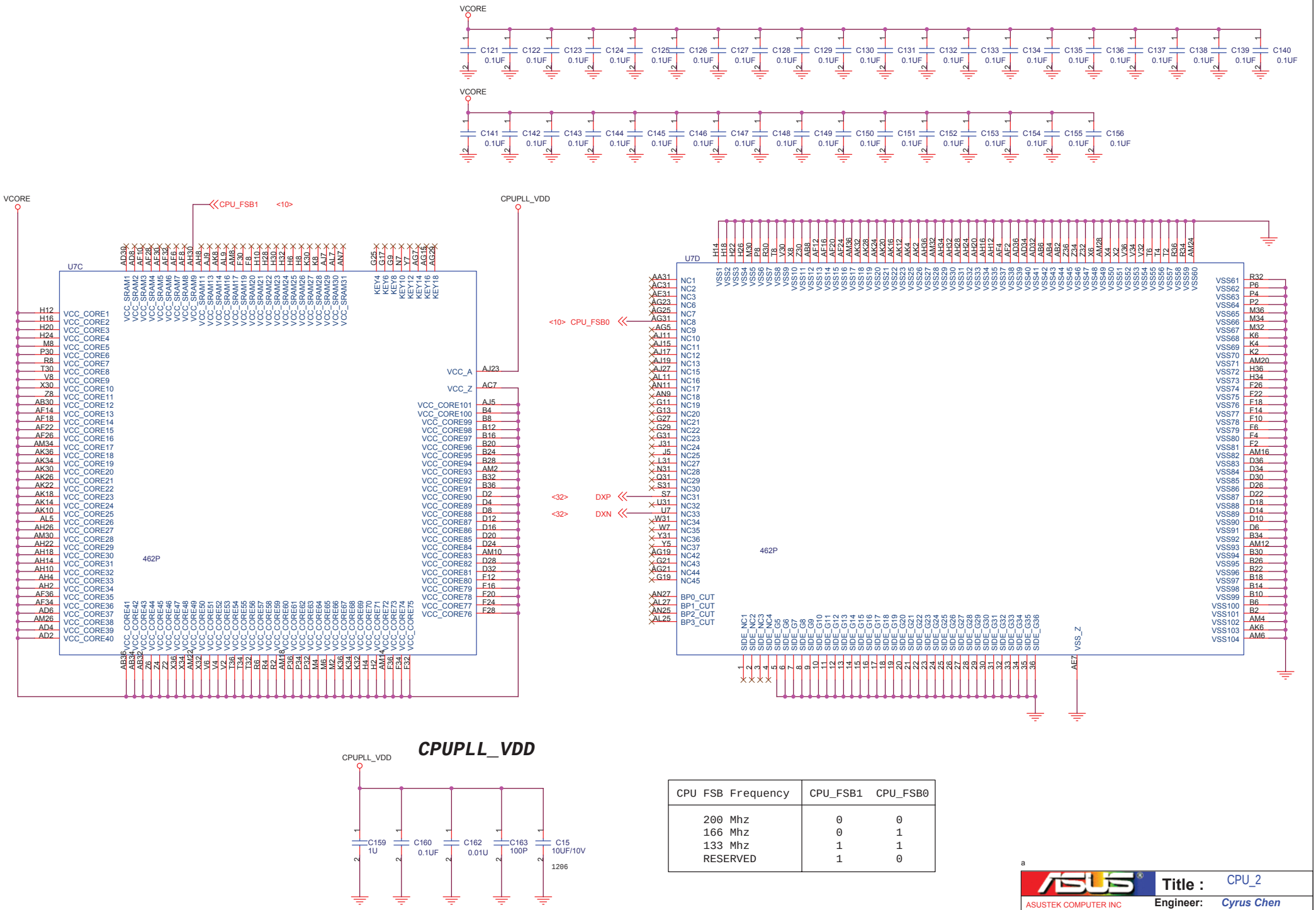


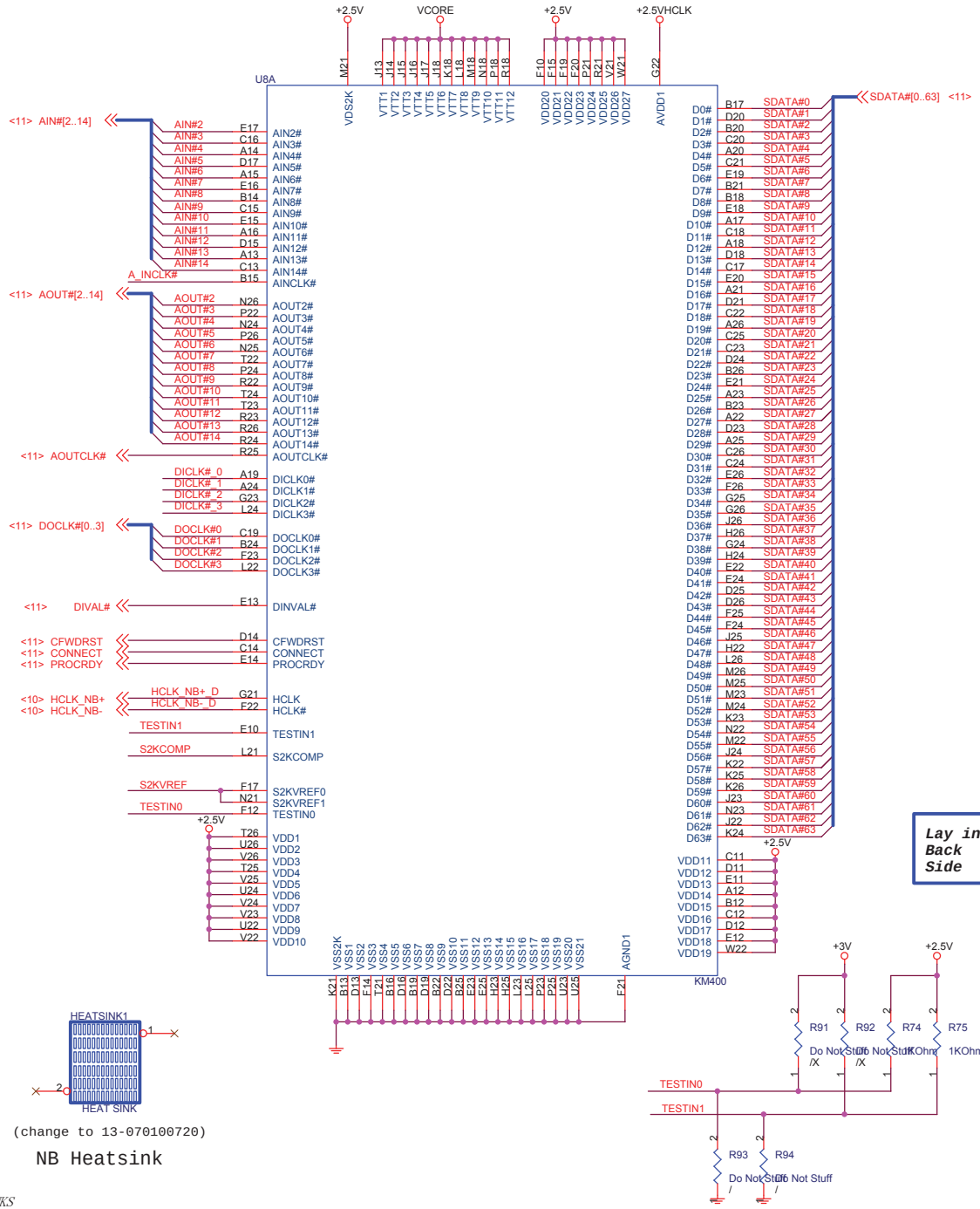
CPUPLL_VDD

CPU FSB Frequency	CPU_FSB1	CPU_FSB0
200 Mhz	0	0
166 Mhz	0	1
133 Mhz	1	1
RESERVED	1	0

a

ASUSTEK COMPUTER INC	Title : CPU_2	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 12 of 40	

NORTH BRIDGE 1 of 3 (HOST BUS)

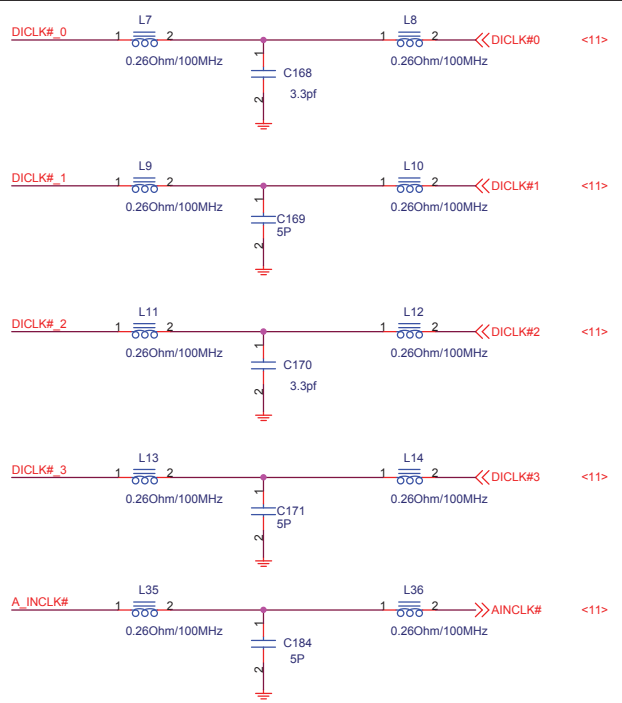


(change to 13-070100720)

NB Heatsink

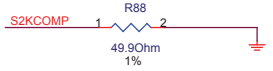
Change L7, L8, L11, L12 to 09-023100010

LCL FILTER



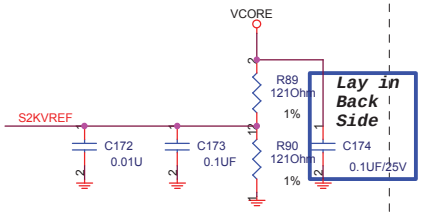
http://laptop-motherboard-schematic.blogspot.com/

S2K BUS COMPENSATION

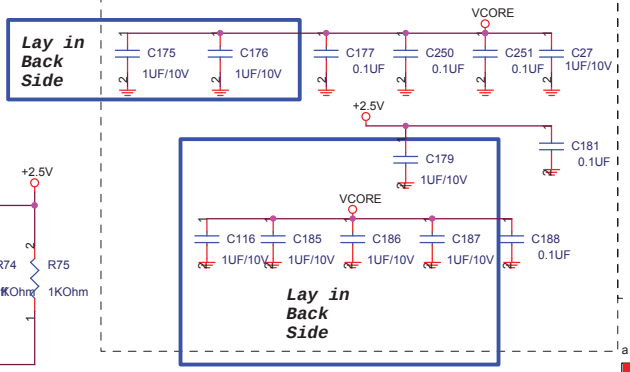


R88 ==> 300 Ohm 1% for KM400
49.9 Ohm 1% for KM400A

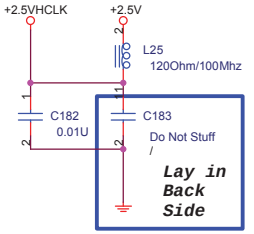
NORTH BRIDGE S2K REFERENCE VOTAGE (1/2VCORE)



VCCH : HOST CPU INTERFACE POWER



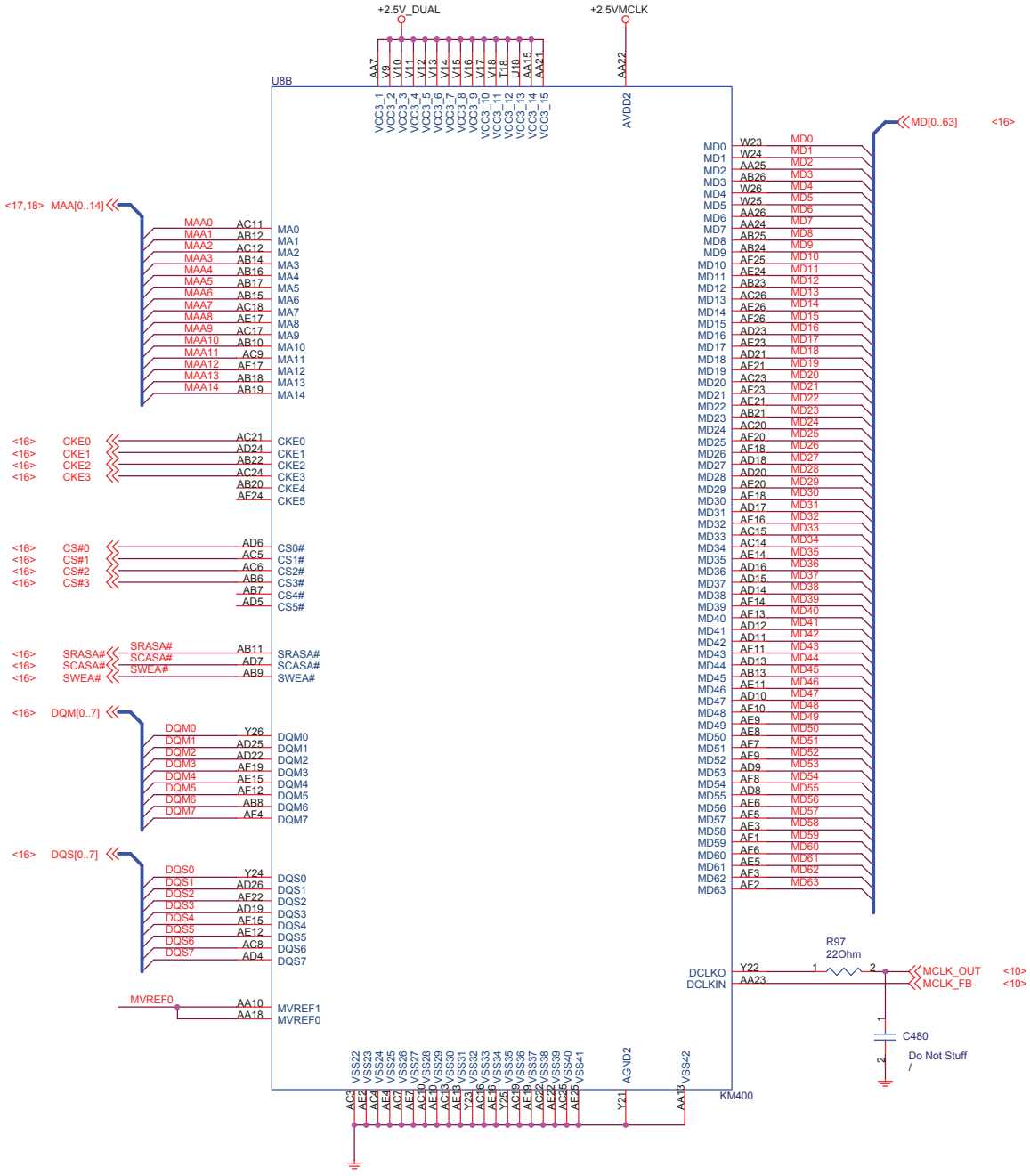
AVDDHCLK/AGNDHCLK : POWER/GROUND FOR INTERNAL CPU CLOCK LOGIC



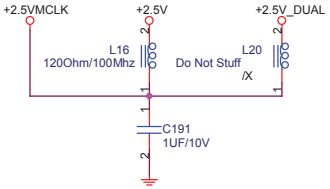
ASUSTEK COMPUTER INC.	Title : NORTH BRIDGE_1		
	Engineer: Cyrus Chen		
Size A3	Project Name A7V8X-LA		Rev 2.00
Date: Monday, October 13, 2003	Sheet 13 of 40		

BANKS

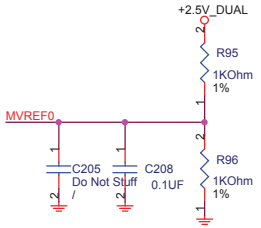
NORTH BRIDGE 2 of 3 (MEMORY)



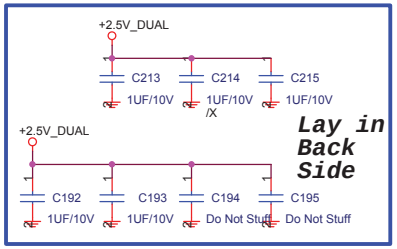
AVMCLK/AGNDMCLK : POWER/GROUND FOR DRAM CLCOK DESKEW CIRCUIT

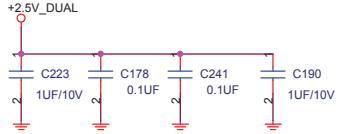


MVERF0/1 : SSTL_2 RECEIVER VREF FOR DDR



VCC3 : +2.5V LEVEL POWER

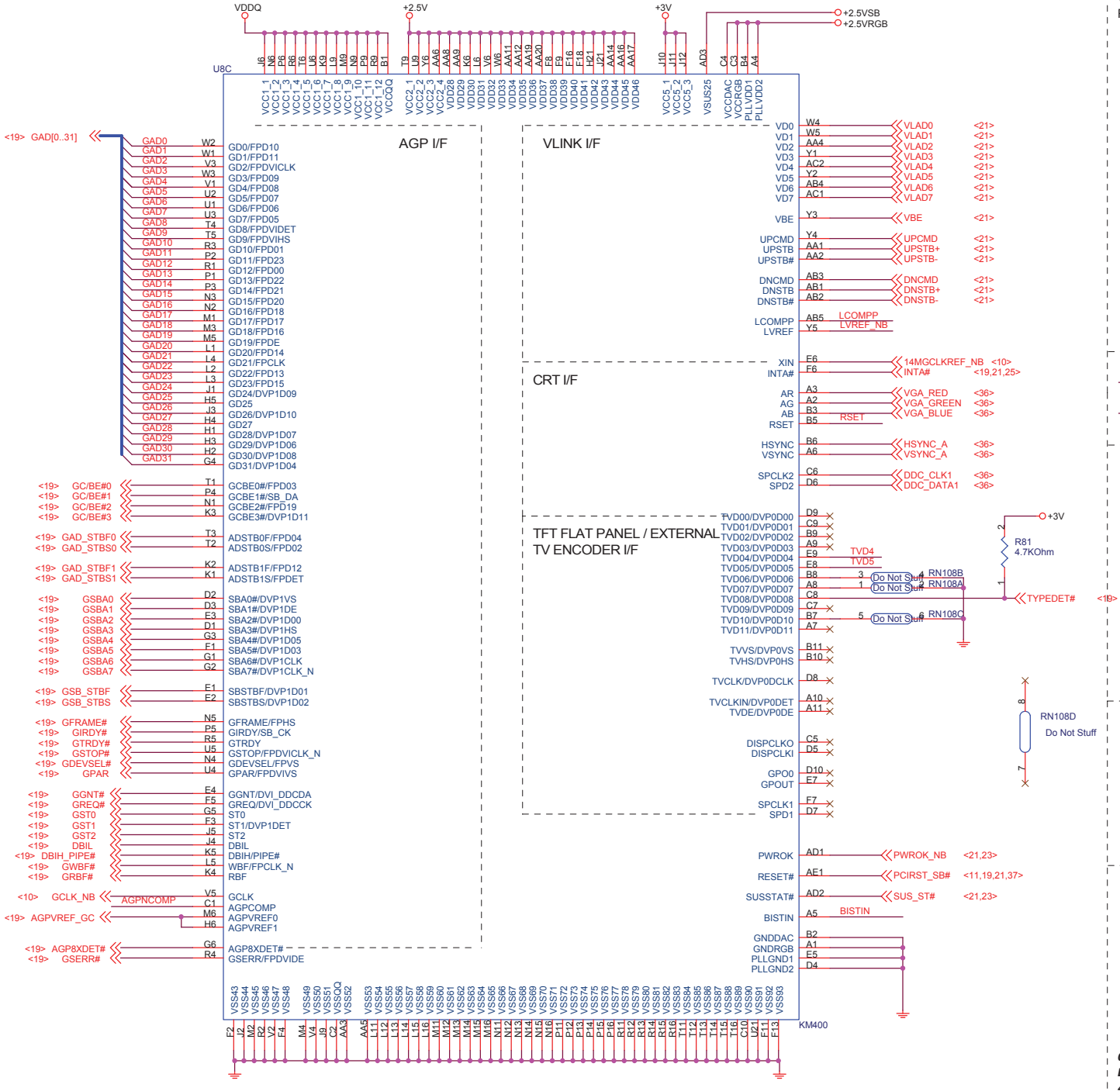




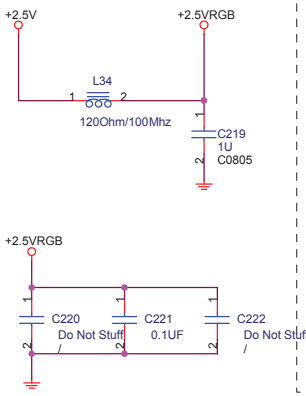
ASUSTEK COMPUTER INC.	Title : NORTH BRIDGE_2	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 14 of 40	

BANKS

NORTH BRIDGE 3 of 3 (AGP,VLINK,VGA)

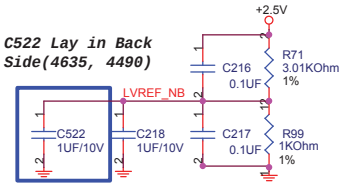


VCCDAC/VCCRGB : RAMDAC POWER/ RGB OUTPUT POWER

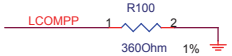


VLINK

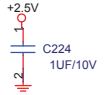
1. VLINK REFERENCE VOLTAGE 0.625V

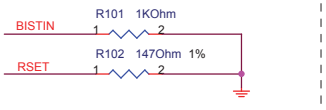


2. VLINK P-CHANNEL COMPENSATION



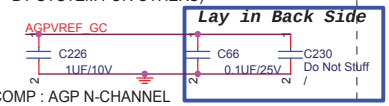
3. VLINK INTERFACE POWER : VCCVL



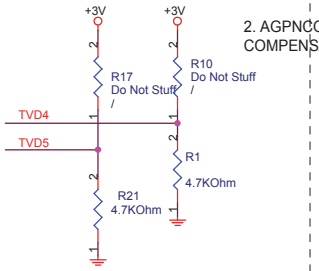


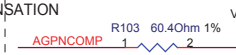
AGP

1. AGPVREF (PROVIDED BY AGP 8X CARD OR BY SYSTEM FOR OTHERS)

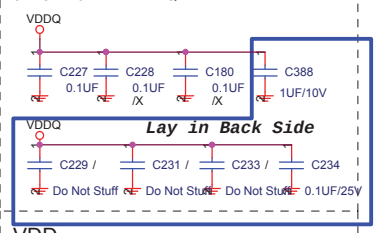


2. AGPNCOMP : AGP N-CHANNEL COMPENSATION



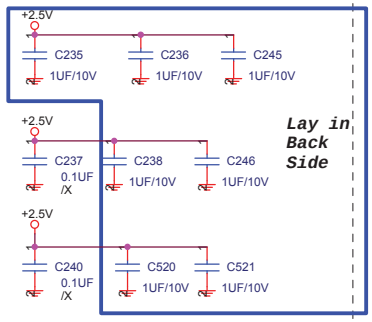


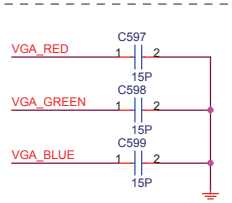
3. AGP POWER : VDDQ

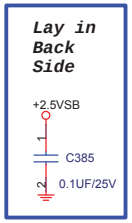


VDD

+2.5V NORTH BRIDGE VCORE







C520 Lay in Back side(4570, 4530)
C521 Lay in Back side(4670, 4530)

C385 Lay in Back Side(5140, 4130)

ASUSTEK COMPUTER INC.	Title : NORTH BRIDGE_3		
	Engineer: Cyrus Chen		
Size: A3	Project Name: A7V8X-LA		Rev: 2.00
Date: Monday, October 13, 2003	Sheet 15 of 40		

BANKS

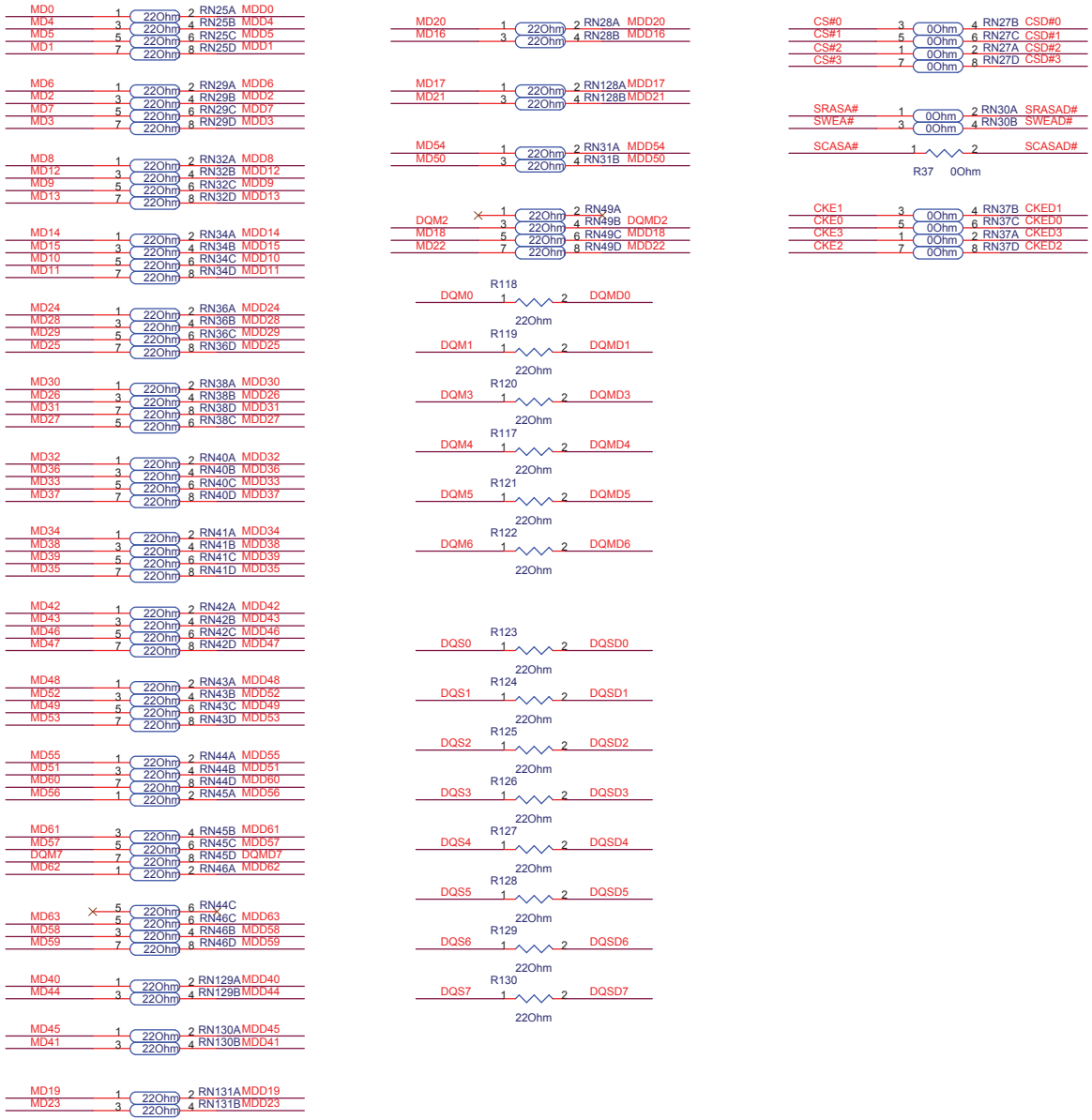
DDR Damping Resistor

<14> MD[0..63]
<14> DQS[0..7]
<14> DQM[0..7]

<14> CS#[0..3]
<14> CKE[0..3]
<14> SRASA#
<14> SCASA#
<14> SWEA#

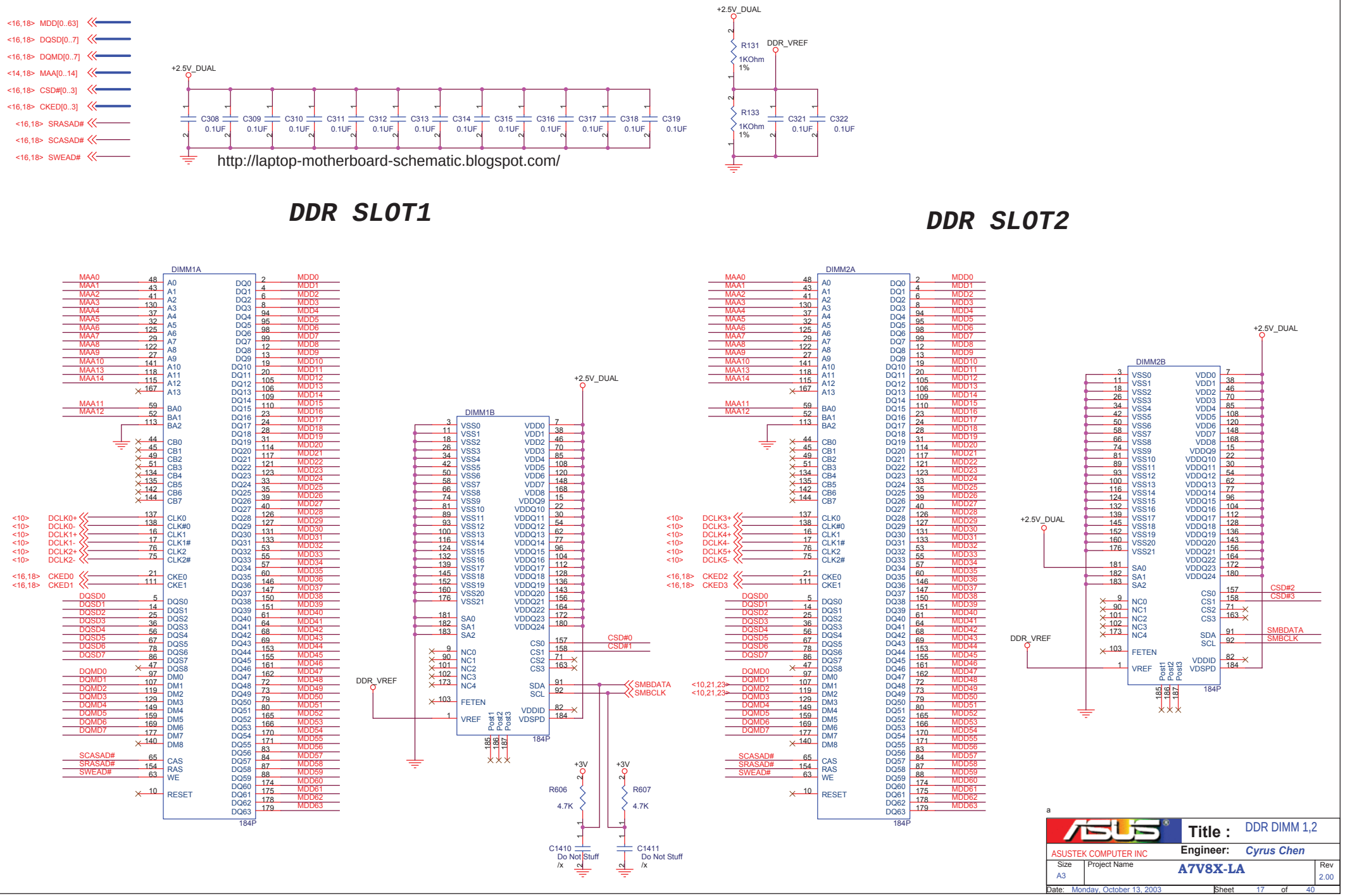
MDD[0..63] <17,18>
DQSD[0..7] <17,18>
DQMD[0..7] <17,18>

CSD#[0..3] <17,18>
CKED[0..3] <17,18>
SRASAD# <17,18>
SCASAD# <17,18>
SWEAD# <17,18>

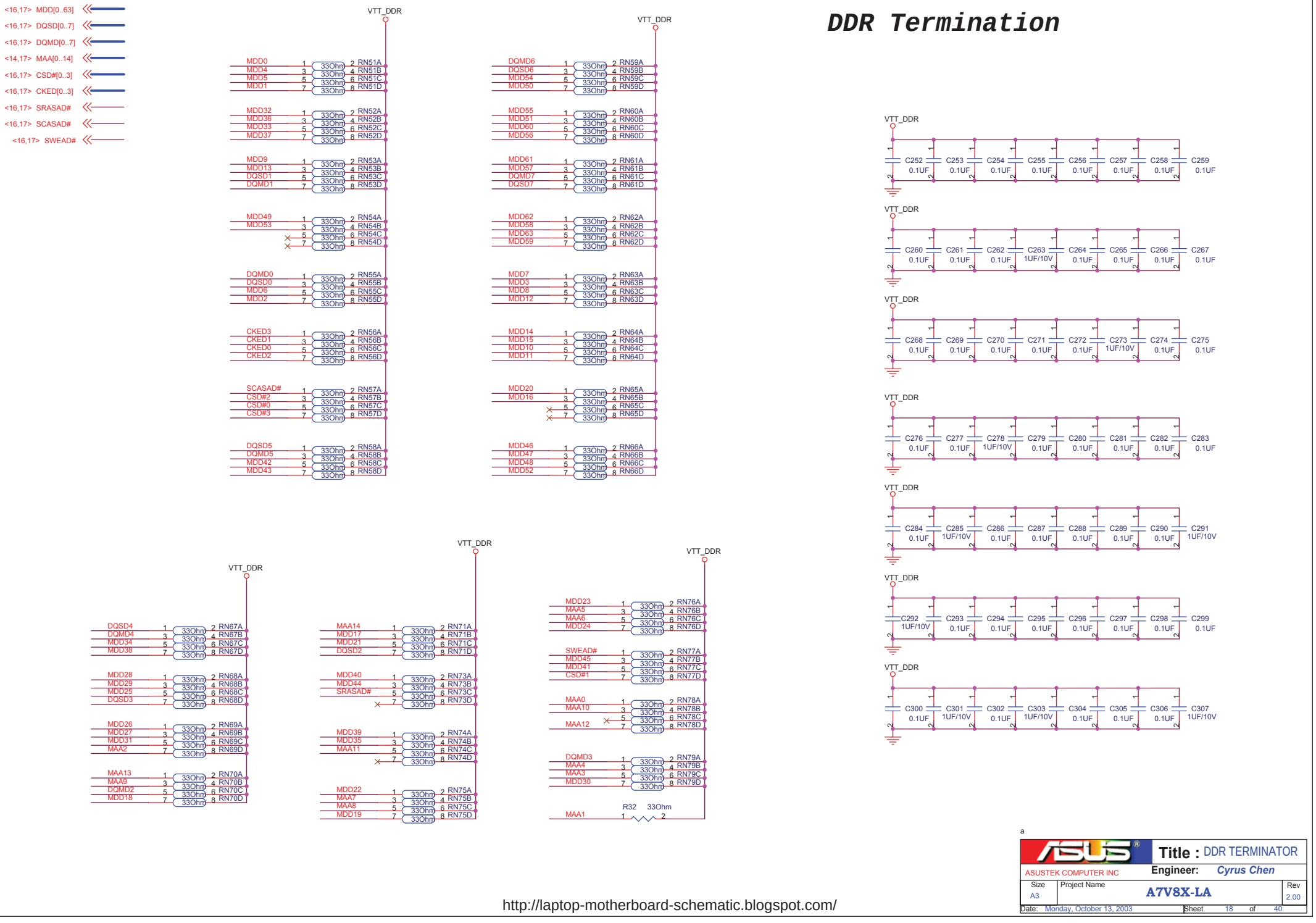


a

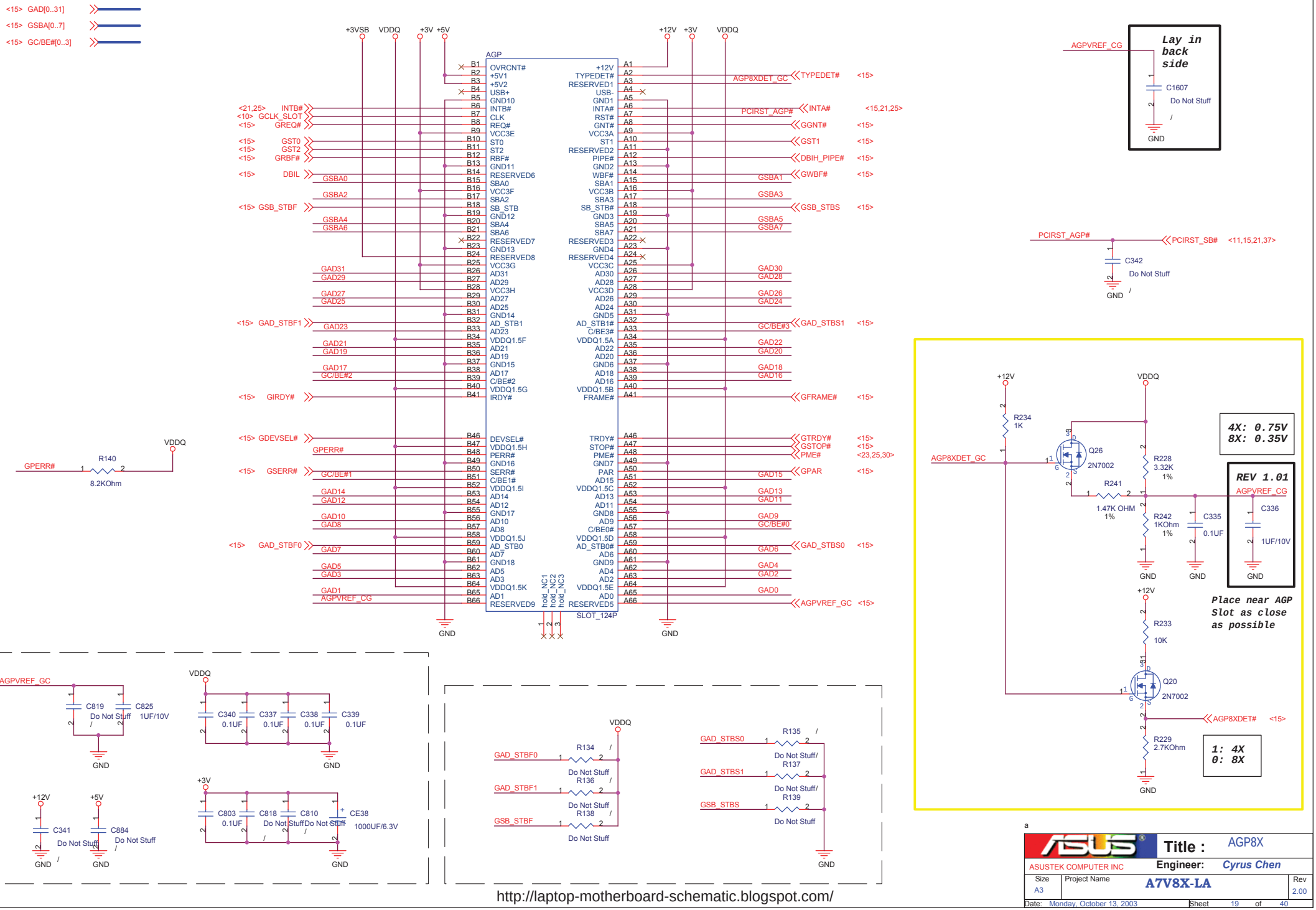
ASUS	Title :	DDR DAMPING
ASUSTEK COMPUTER INC	Engineer:	Cyrus Chen
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 16 of 40	

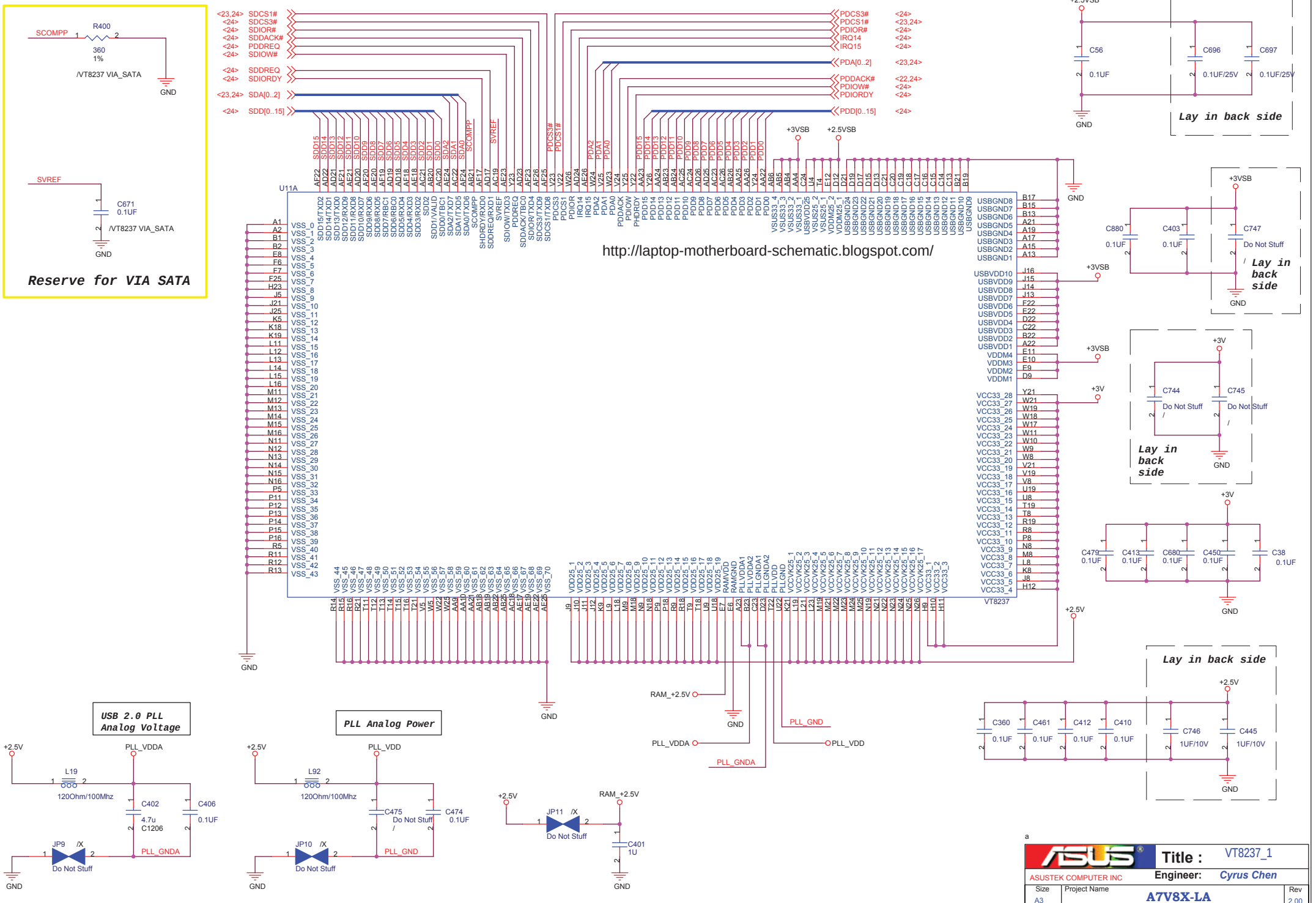

<16,18> MDD[0..63]
<16,18> DQSD[0..7]
<16,18> DQMD[0..7]
<14,18> MAA[0..14]
<16,18> CSD#[0..3]
<16,18> CKED[0..3]
<16,18> SRASAD#
<16,18> SCASAD#
<16,18> SWEAD#
+2.5V_DUAL
C308 0.1UF
C309 0.1UF
C310 0.1UF
C311 0.1UF
C312 0.1UF
C313 0.1UF
C314 0.1UF
C315 0.1UF
C316 0.1UF
C317 0.1UF
C318 0.1UF
C319 0.1UF
http://laptop-motherboard-schematic.blogspot.com/
+2.5V_DUAL
R131 1KOhm 1%
DDR_VREF
R133 1KOhm 1%
C321 0.1UF
C322 0.1UF
DDR SLOT1
DDR SLOT2
DIMM1A
DIMM1B
DIMM2A
DIMM2B
184P
DDR_VREF
+3V
R606 4.7K
R607 4.7K
C1410 Do Not Stuff /x
C1411 Do Not Stuff /x
CSD#0
CSD#1
CSD#2
CSD#3
SMBDATA
SMBCLK
Title : DDR DIMM 1,2
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
Sheet 17 of 40

DDR Termination



ASUSTEK COMPUTER INC	Title : DDR TERMINATOR	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 18 of 40	




Reserve for VIA SATA
SCOMPP
R400
360
1%
/VT8237 VIA_SATA
GND
SVREF
C671
0.1UF
/VT8237 VIA_SATA
GND
U11A
VT8237
http://laptop-motherboard-schematic.blogspot.com/
+3VSB
+2.5VSB
+2.5V
+3V
C56
0.1UF
C696
0.1UF/25V
C697
0.1UF/25V
Lay in back side
C880
0.1UF
C403
0.1UF
C747
Do Not Stuff
C744
Do Not Stuff
C745
Do Not Stuff
C479
0.1UF
C413
0.1UF
C680
0.1UF
C450
0.1UF
C38
0.1UF
C360
0.1UF
C461
0.1UF
C412
0.1UF
C410
0.1UF
C746
1UF/10V
C445
1UF/10V
USB 2.0 PLL Analog Voltage
L19
120Ohm/100Mhz
C402
4.7u
C1206
C406
0.1UF
JP9 /X
Do Not Stuff
PLL_GNDA
PLL Analog Power
L92
120Ohm/100Mhz
C475
Do Not Stuff
C474
0.1UF
JP10 /X
Do Not Stuff
PLL_VDD
PLL_VDDA
PLL_GNDA
PLL_GND
RAM_+2.5V
JP11 /X
Do Not Stuff
C401
1U
ASUSTEK COMPUTER INC
Title : VT8237_1
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
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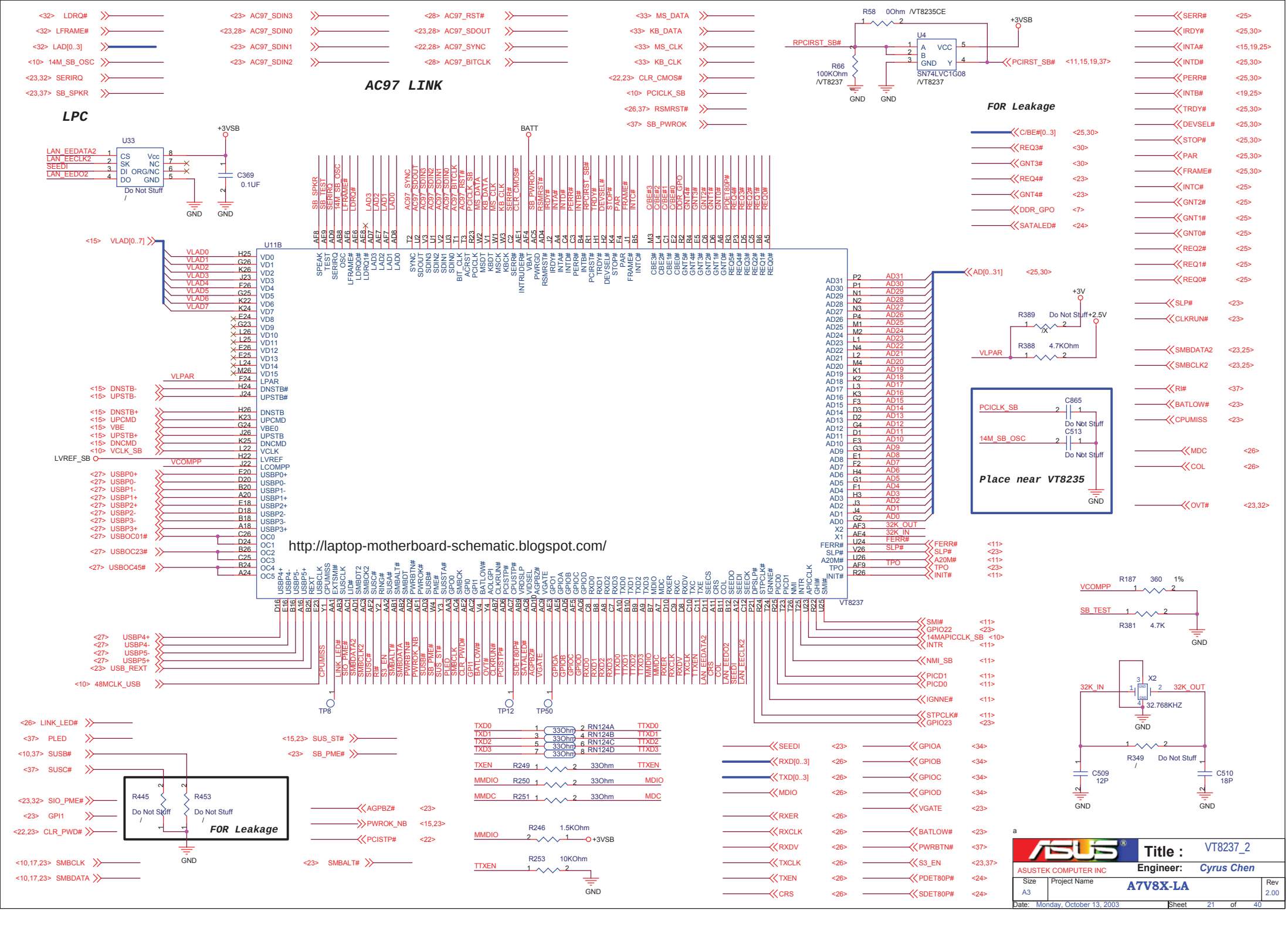
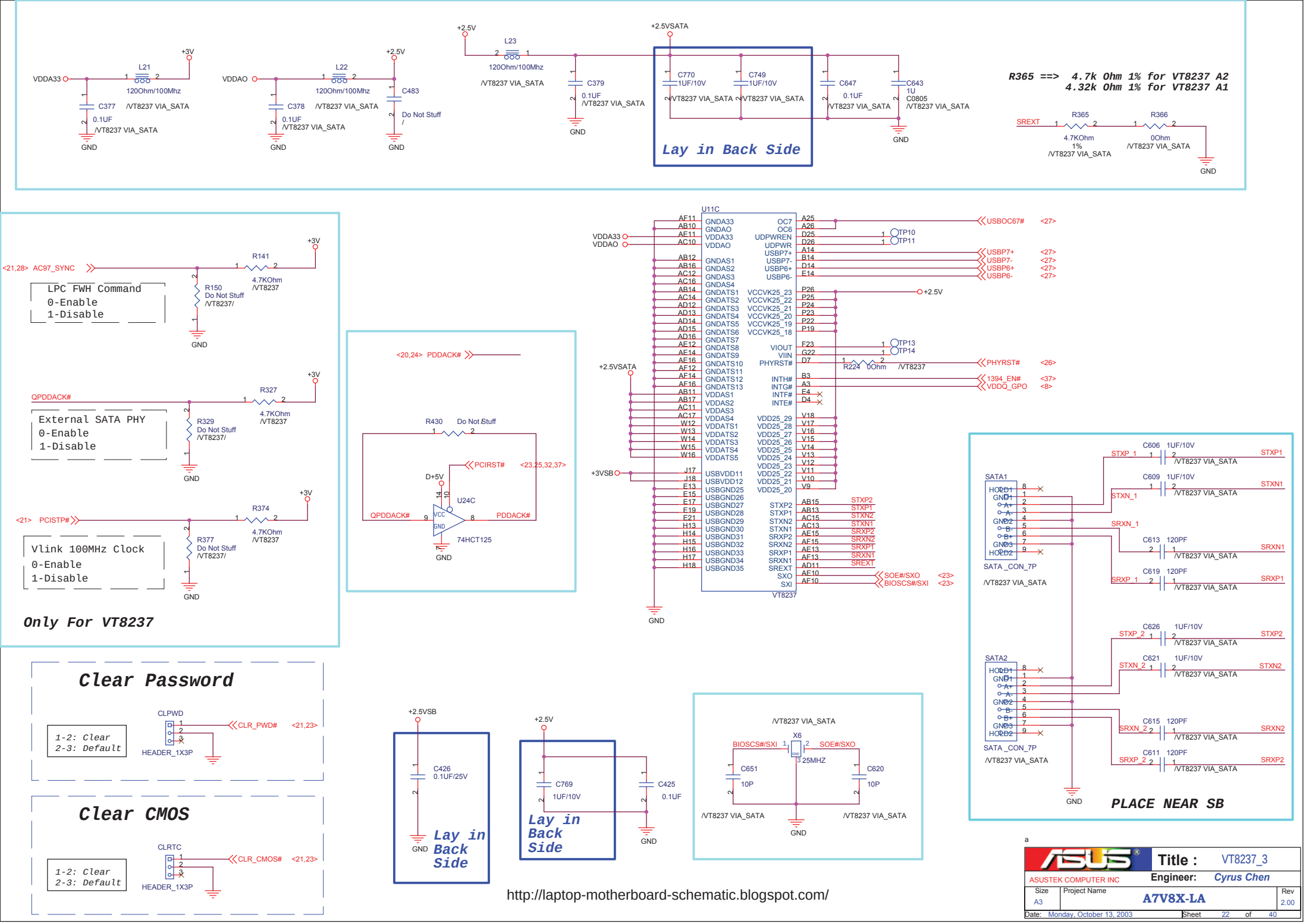

AC97 LINK
LPC
FOR Leakage
FOR Leakage
Place near VT8235
http://laptop-motherboard-schematic.blogspot.com/
VT8237
U11B
U33
U4
Title : VT8237_2
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
Sheet 21 of 40


R365 ==> 4.7k Ohm 1% for VT8237 A2
4.32k Ohm 1% for VT8237 A1
Lay in Back Side
LPC FWH Command
0-Enable
1-Disable
External SATA PHY
0-Enable
1-Disable
Vlink 100MHz Clock
0-Enable
1-Disable
Only For VT8237
Clear Password
1-2: Clear
2-3: Default
Clear CMOS
1-2: Clear
2-3: Default
PLACE NEAR SB
http://laptop-motherboard-schematic.blogspot.com/
Title : VT8237_3
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
A7V8X-LA
Monday, October 13, 2003

Hardware Strapping

For VT8235CE

For VT8237CD

R608 4.7KOhm, R609 4.7KOhm — SMBCLK <10,17,21>, SMBDATA <10,17,21>
C4806 Do Not Stuff /X, C4807 Do Not Stuff /X — GND

R610 4.7KOhm, R611 4.7KOhm — SMBCLK2 <21,25>, SMBDATA2 <21,25>
C4808 Do Not Stuff /X, C4809 Do Not Stuff /X — GND

RP10A
<21> TPO — 4.7KOhm — 10 RP10B
<21> AGPBZ# — 4.7KOhm — 10 RP10D
<21> VGATE — 4.7KOhm — 10 RP10C
<21> SLP# — 4.7KOhm — 10 RP10G
<21,32> SERIRQ — 4.7KOhm — 10 RP10F
<21,37> SB_SPKR — 4.7KOhm — 10 RP10E
<21> GPIO23 — 4.7KOhm — 10 RP10H
<21> GPIO22 — 4.7KOhm — 10

RP9A
<21> SB_PME# — 4.7KOhm — 10 RP9B
<21> CPUMISS — 4.7KOhm — 10 RP9C
<21,37> S3_EN — 4.7KOhm — 10 RP9D
<15,21> SUS_ST# — 4.7KOhm — 10 RP9E
<21> SMBALT# — 4.7KOhm — 10 RP9F
<21> GPI1 — 4.7KOhm — 10 RP9G
<21,32> SIO_PME# — 4.7KOhm — 10 RP9H
<21> BATLOW# — 4.7KOhm — 10
<15,21> PWROK_NB — R345 4.7KOhm

GPI1 — R48 220Ohm /KM400/ — GND

<21> USB_REXT — R152 5.1KOhm 1% — R255 470Ohm 1% — GND

<21,28> AC97_SDIN0 — R146 8.2KOhm
<21> CLKRUN# — RN87A 8.2KOhm
<21> AC97_SDIN2 — RN87D 8.2KOhm
<21> AC97_SDIN3 — RN87B 8.2KOhm
<21> AC97_SDIN1 — RN87C 8.2KOhm — GND

<21> REQ4# — RN72D 4.7KOhm
<21> GNT4# — RN72C 4.7KOhm
RN72B 4.7KOhm
RN72A 4.7KOhm
<21,32> OVT# — R344 4.7KOhm

LVREF_SB

+2.5V — R311 3.01KOhm 1% — C456 Do Not Stuff / — LVREF_SB
R307 1KOhm 1% — C457 0.1UF — GND

The Voltage level of LVREF_SB is 0.625V

DA1 =>

Strapping Information Select

0 : from hardware strapping
1 : from boot rom

DA1 — R479 Do Not Stuff/ — GND
+3V — R184 4.7KOhm

DA2, DA0 =>

CPU FSB Frequency	DA2	DA0
200 Mhz	1	0
166 Mhz	1	1
133 Mhz	0	1
100 Mhz	0	0

<10> DA2
<10> DA0

For 8237CD, Eliminate LAN EEPROM
1/0 : Enable/Disable

<21> SEEDI — R289 4.7KOhm /VT8237 — +3V
R18 Do Not Stuff/VT8237/ — GND

DCS1# =>

For 8235CE, Eliminate LAN EEPROM
0/1 : Enable/Disable

For 8237CD, SATA Mode Select
0 : Master Slave Mode
1 : Master Master Mode
Set "0" when use external SATA PHY

DCS1# — R470 4.7KOhm /VT8237 — +3V
R486 Do Not Stuff/VT8235CE — GND

BIOSCS# LPC ROM Select (for 8235CE)
0 : disable LPC ROM (default)
1 : enable LPC ROM

<22> BIOSCS#/SXI — R387 Do Not Stuff/VT8235CE — +3V

AC97_SDOUT => Auto reboot (for 8237CD)
0 : enable
1 : disable

<21,28> AC97_SDOUT — R149 4.7KOhm /VT8237 — +3V
R52 Do Not Stuff/VT8237/ — GND

SOE#/SXO => Auto reboot (for 8235CE)
0 : enable
1 : disable

<22> SOE#/SXO — R385 Do Not Stuff/VT8235CE — +3V
R383 Do Not Stuff/VT8235CE/ — GND

<21,22> CLR_PWD# — R369 1MOhm — BATT
<21,22> CLR_CMOS# — R373 1MOhm

http://laptop-motherboard-schematic.blogspot.com/

R428 Do Not Stuff — PCIRST# <22,25,32,37> — U49A 74HCT125 — DA0 — QDA0
R449 Do Not Stuff — PCIRST# — U49B 74HCT125 — DA1 — QDA1
C2009 0.1UF — GND
R451 Do Not Stuff — PCIRST# — U49C 74HCT125 — DA2 — QDA2
R458 Do Not Stuff — PCIRST# — U49D 74HCT125 — DCS1# — QDCS1#

QDA0 — Do Not Stuff — RN3904A /VT8235CE — SDA0
QDA1 — Do Not Stuff — RN3904B /VT8235CE — SDA1
QDA2 — Do Not Stuff — RN3904C /VT8235CE — SDA2
QDCS1# — Do Not Stuff — RN3904D /VT8235CE — SDCS1#

QDA0 — 0Ohm — RN3903C /VT8237 — PDA0
QDA1 — 0Ohm — RN3903B /VT8237 — PDA1
QDA2 — 0Ohm — RN3903A /VT8237 — PDA2
QDCS1# — 0Ohm — RN3903D /VT8237 — PDCS1#

R6 Do Not Stuff
+5V_DUAL — R69 4.7KOhm — SB_PME#
+3VSB — R68 4.7KOhm
Q19 2N7002
Q18 2N7002
<19,25,30> PME# — GND

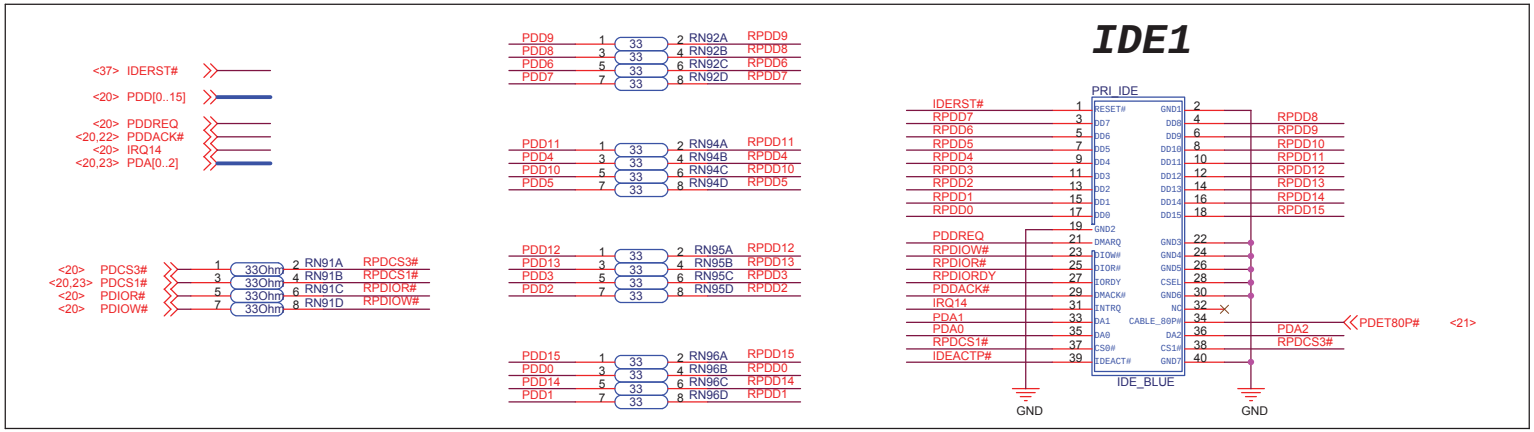
PDA[0..2] <20,24> — PDCS1# <20,24>
SDA[0..2] <20,24> — SDCS1# <20,24>

a

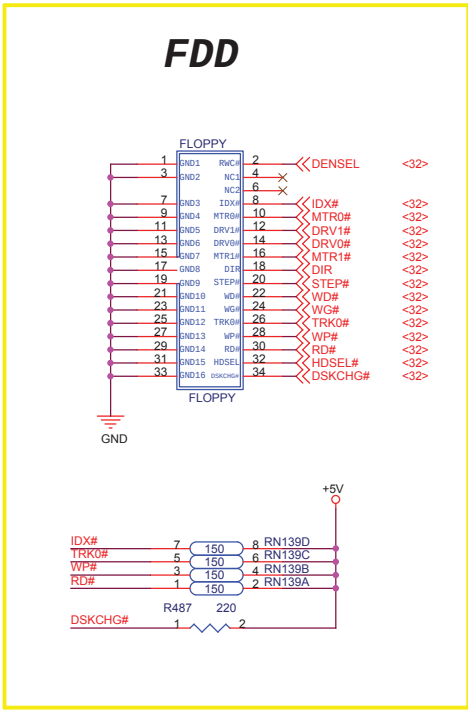
ASUSTeK COMPUTER INC

Title :	VT8237_4
Engineer:	Cyrus Chen
Size: A3	Project Name: A7V8X-LA
Rev:	2.00
Date: Monday, October 13, 2003	Sheet 23 of 40

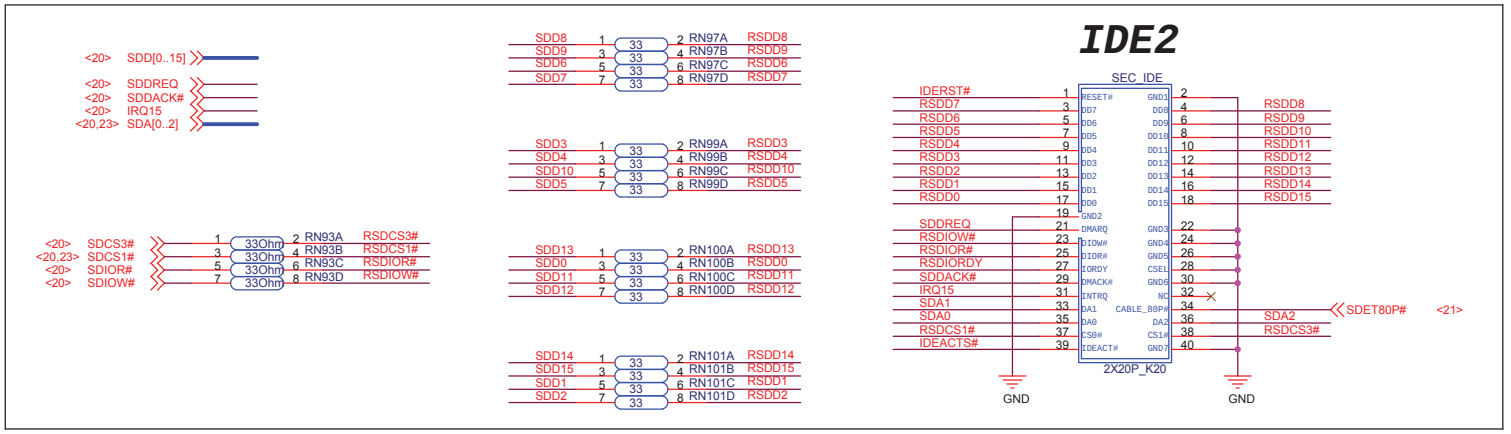
IDE1



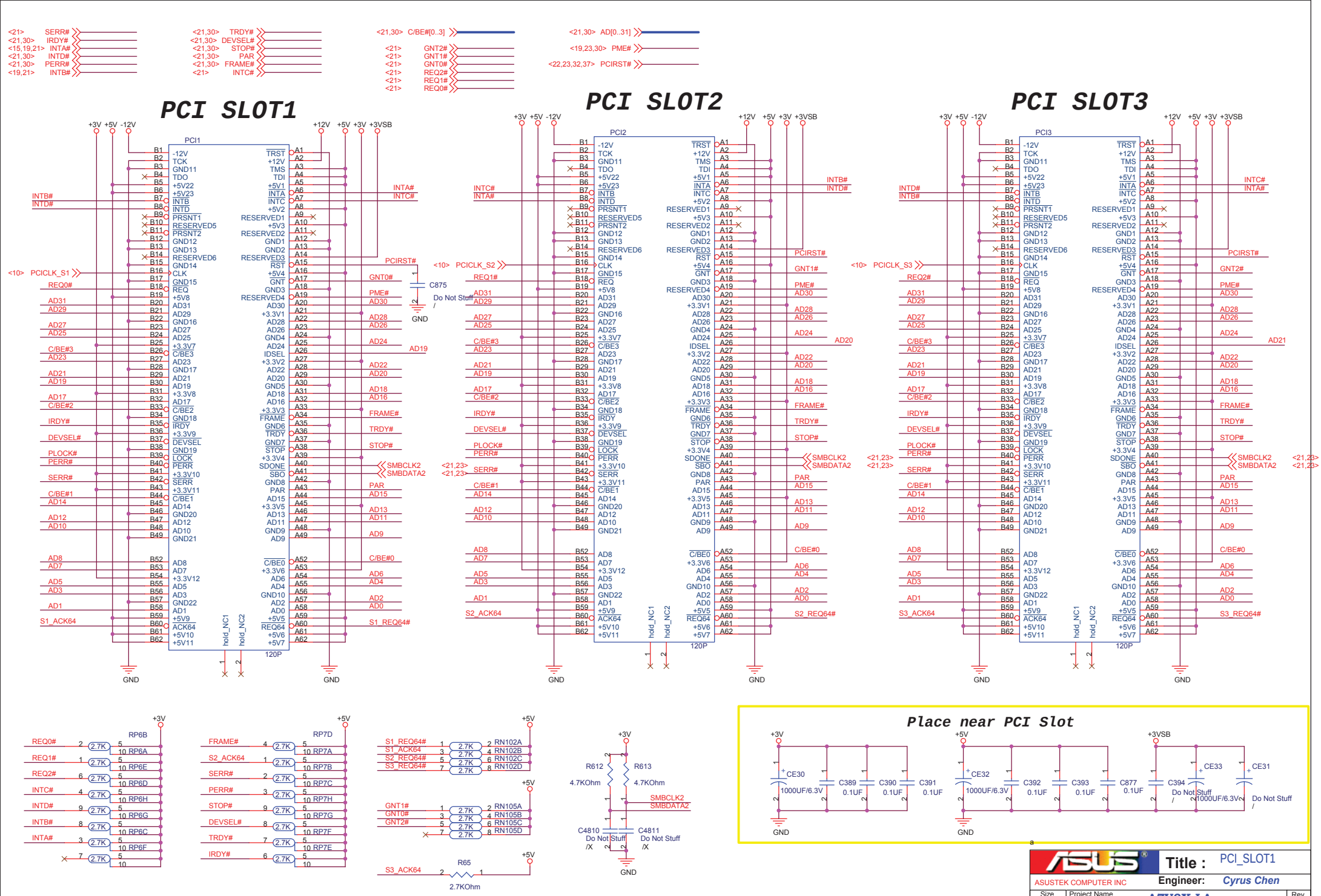
FDD



IDE2



ASUSTEK COMPUTER INC	Title : IDE & FLOPPY	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 24 of 40	


PCI SLOT1
PCI SLOT2
PCI SLOT3
Place near PCI Slot
Title : PCI_SLOT1
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
Project Name A7V8X-LA
Size A3
Rev 2.00
Date: Monday, October 13, 2003
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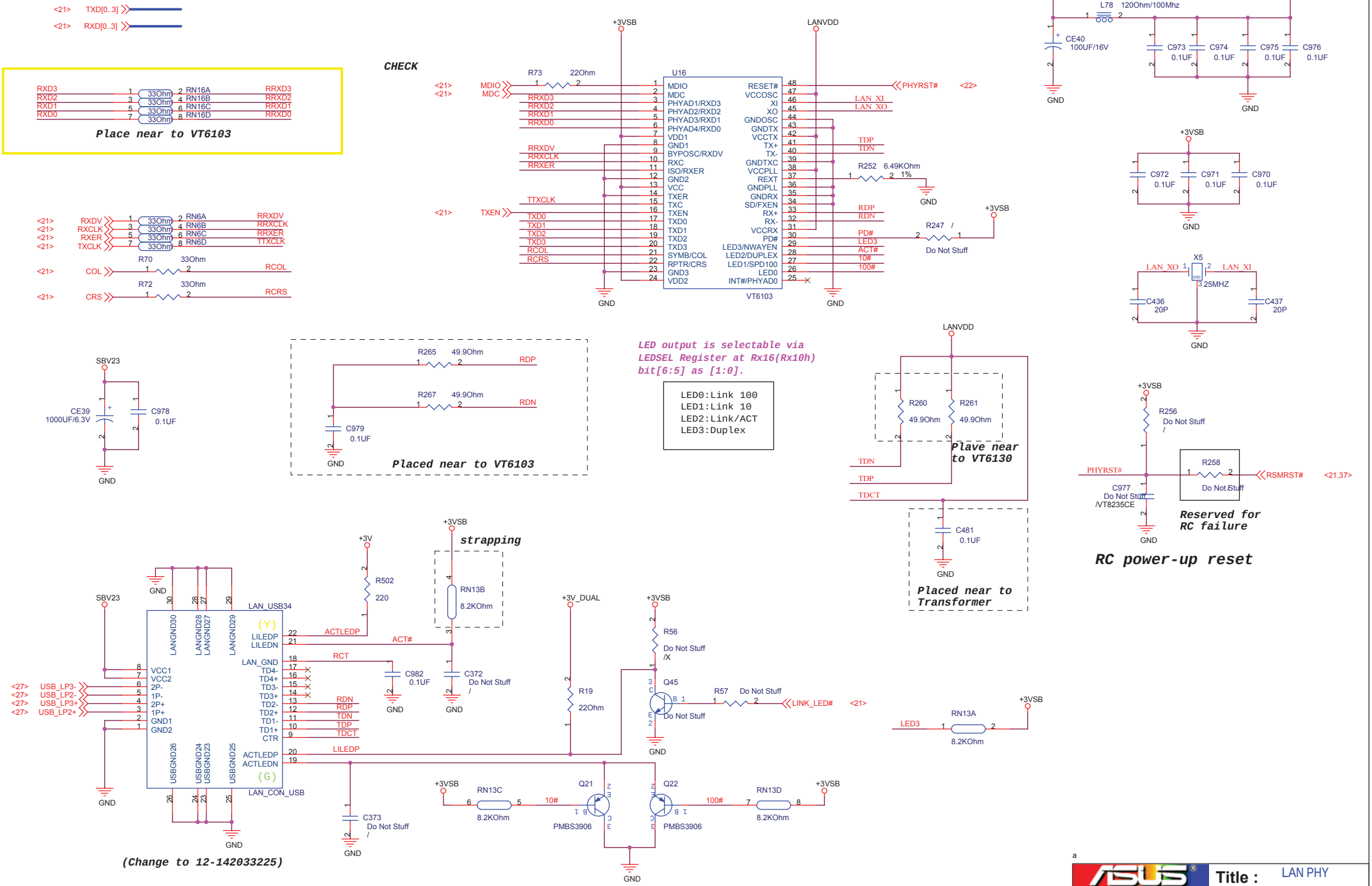
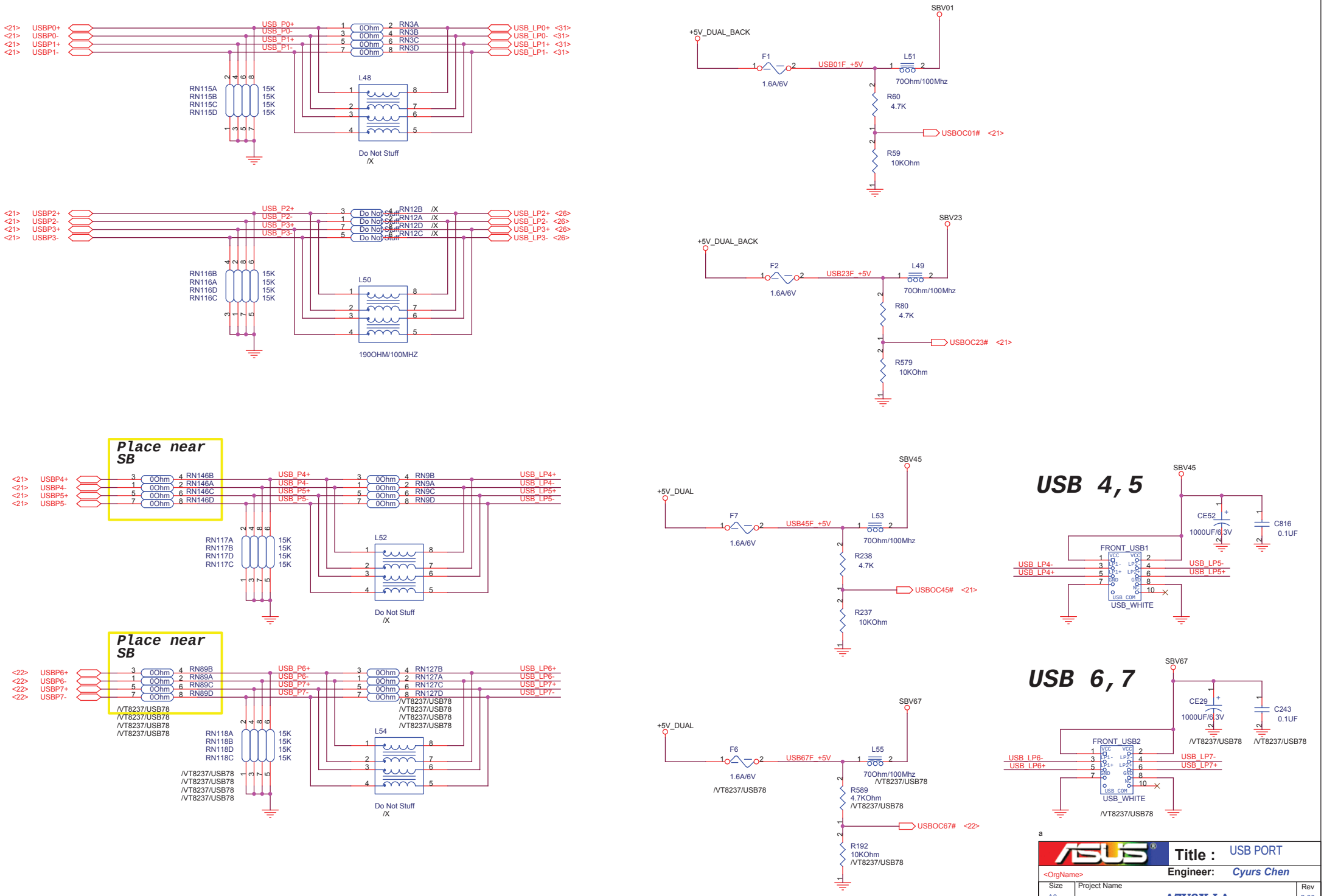
http://laptop-motherboard-schematic.blogspot.com/





a

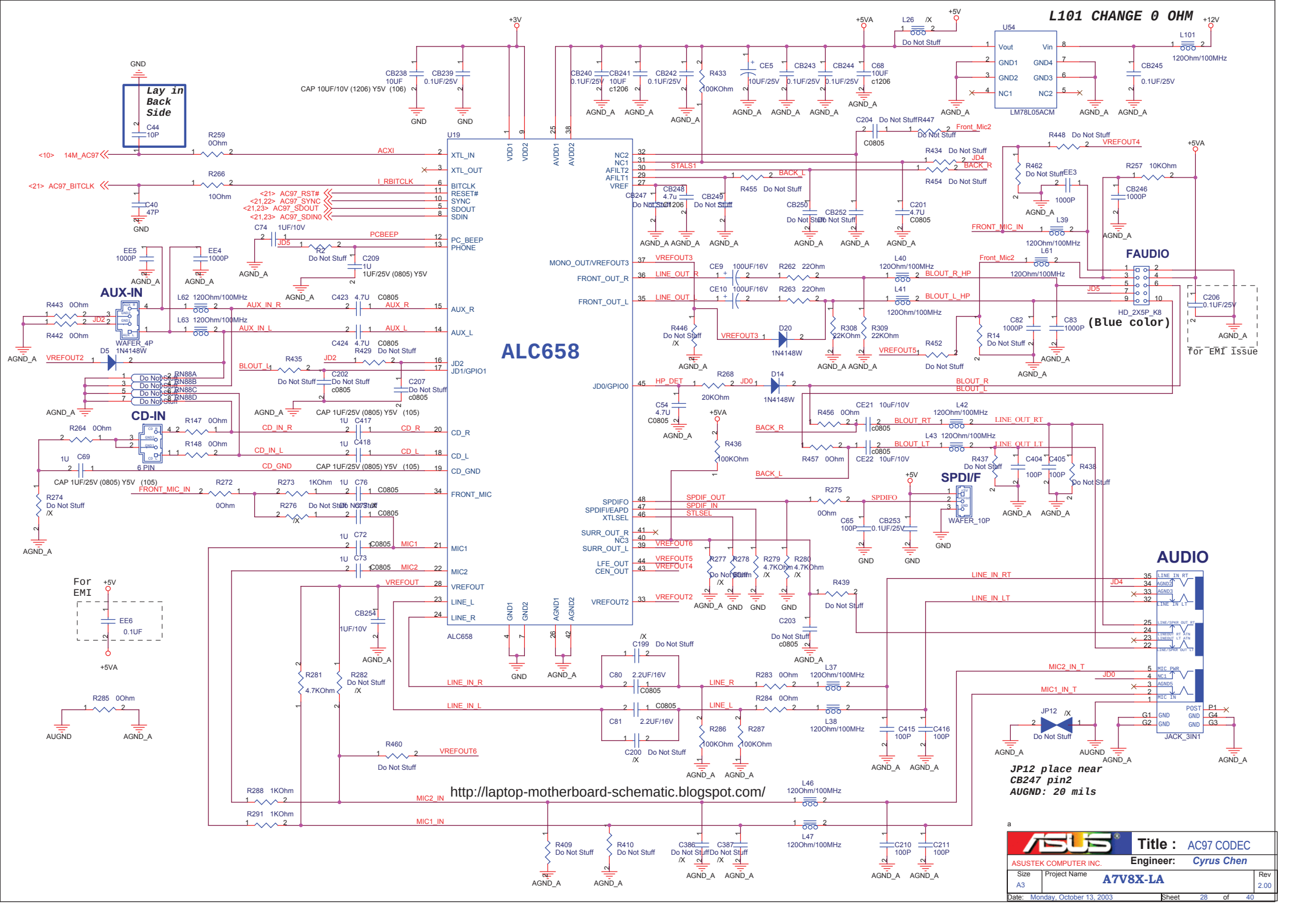
Title : USB PORT

<OrgName>

Engineer: Cyurs Chen

Size	Project Name	Rev
A3	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 27 of 40


L101 CHANGE 0 OHM
ALC658
AUX-IN
CD-IN
SPDI/F
AUDIO
FAUDIO
(Blue color)
for EMI issue
Lay in Back Side
For EMI
JP12 place near CB247 pin2
AUGND: 20 mils
http://laptop-motherboard-schematic.blogspot.com/
Title : AC97 CODEC
ASUSTEK COMPUTER INC.
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
Sheet 28 of 40

The difference table of the ALC650F, ALC658C, ALC658D+JS, and ALC658D+UAJ

	D5	R443	R442	R2	C209	R429	C207	RN88	R288	R291	R281	R282	R460	R409	R410
650F	X	0OHM	0OHM	X	1U(0805)	X	X	X	1K	1K	4.7K	X	X	X	X
658C	X	0OHM	0OHM	X	1U(0805)	X	X	X	1K	1K	4.7K	X	X	X	X
658D+JS	X	X	X	20K	4.7U(0805)	20K	4.7U(0805)	22K	0OHM	0OHM	2.2K	X	2.2K	22K	22K
658D+UAJ	1N4148	X	X	20K	4.7U(0805)	20K	4.7U(0805)	22K	0OHM	0OHM	2.2K	X	2.2K	22K	22K

	R462	R14	CB250	R448	R455	CB249	R286	R287	R433	C204	R447	CB252	R434	R454	C201
650F	X	X	1000P	X	X	1000P	100K	100K	X	X	X	1U	X	X	1U(0805)
658C	X	X	X	X	X	X	100K	100K	X	X	X	X	X	X	X
658D+JS	22K	22K	X	2.2K	0OHM	X	22K	22K	100K	1U	0OHM	X	20K	0OHM	4.7U(0805)
658D+UAJ	22K	22K	X	2.2K	0OHM	X	22K	22K	100K	1U	0OHM	X	20K	0OHM	4.7U(0805)

	R452	R257	R262	R263	D20	R456	R457	R437	R438	R436	R435	R439	D14	C202	C203
650F	X	10K	22OHM	22OHM	X	0OHM	0OHM	X	X	X	X	X	1N4148	X	X
658C	X	10K	22OHM	22OHM	X	0OHM	0OHM	X	X	X	X	X	1N4148	X	X
658D+JS	2.2K	X	0OHM	0OHM	X	X	X	22K	22K	100K	20K	20K	X	4.7U(0805)	4.7U(0805)
658D+UAJ	2.2K	X	0OHM	0OHM	1N4148	X	X	22K	22K	100K	20K	20K	X	4.7U(0805)	4.7U(0805)

a

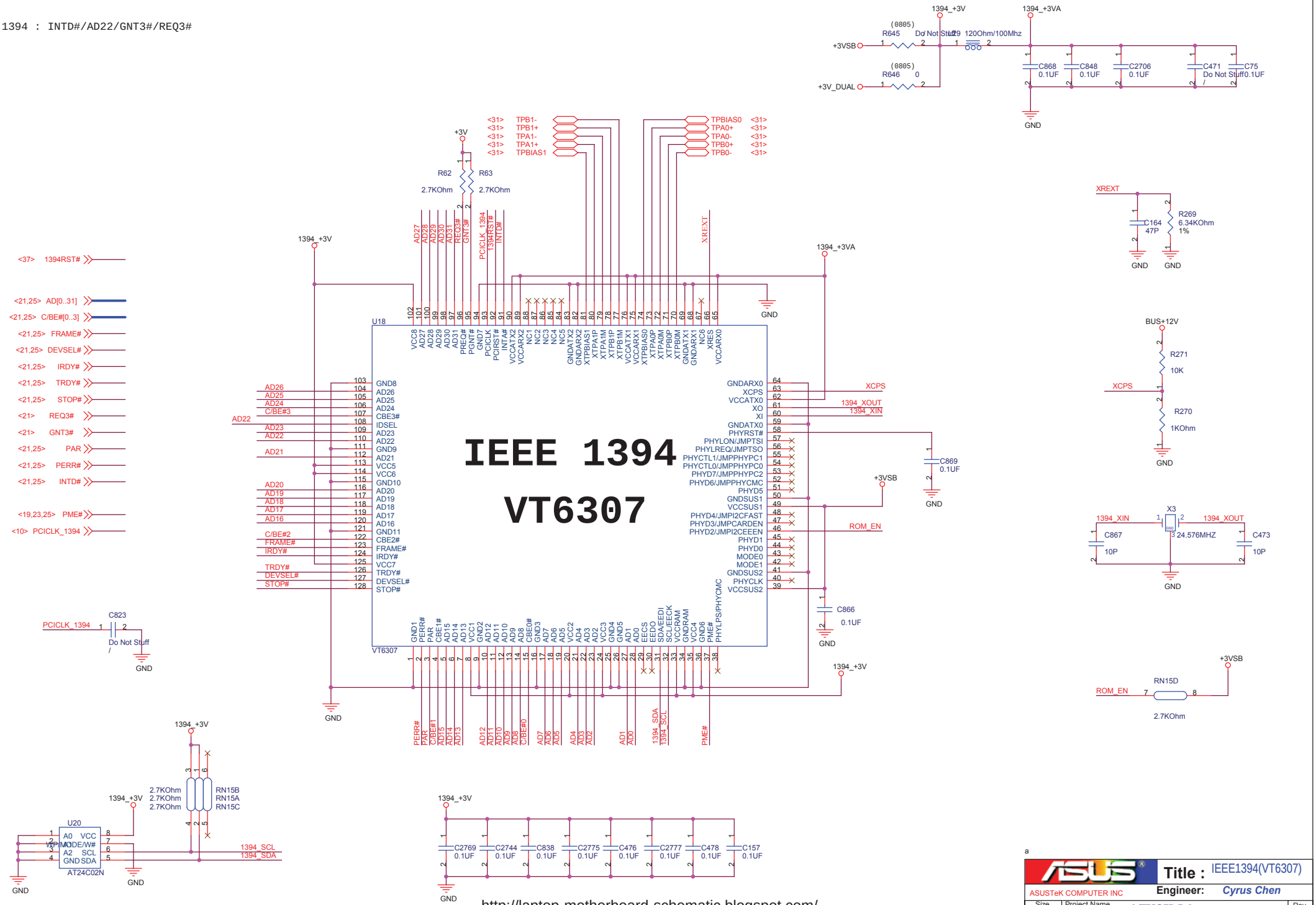
Title : BOM TABLE OF CODEC

<OrgName> Engineer: Cyrus Chen

Size	Project Name	Rev
A3	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 29 of 40

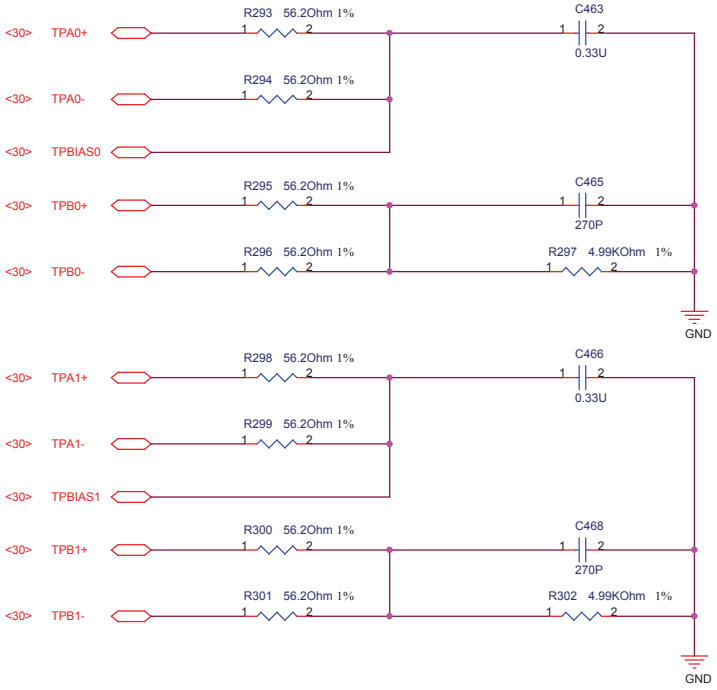
1394 : INTD#/AD22/GNT3#/REQ3#

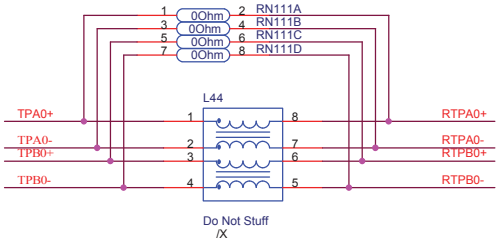


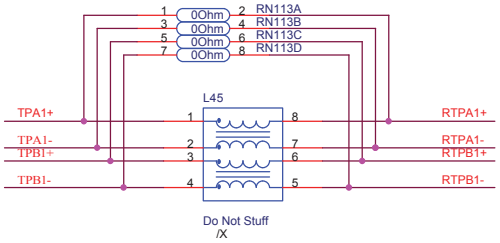
http://laptop-motherboard-schematic.blogspot.com/

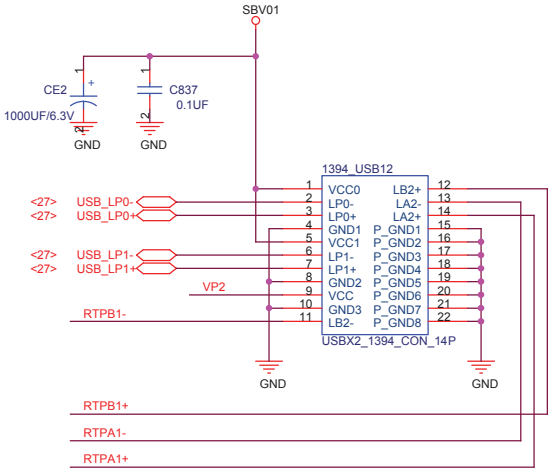
a

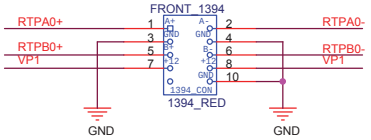
ASUSTeK COMPUTER INC	Title : IEEE1394(VT6307)	
	Engineer: Cyrus Chen	
Size A3	Project Name A7V8X-LA	Rev 2.00
Date: Monday, October 13, 2003	Sheet 30 of 40	

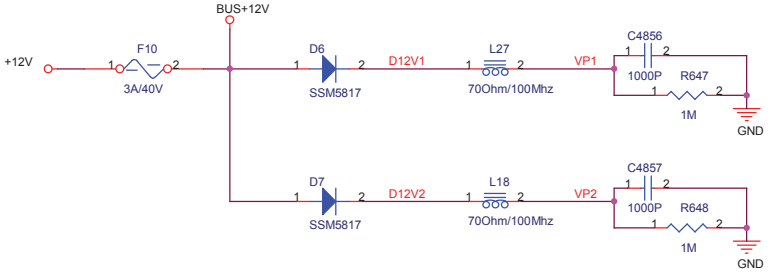


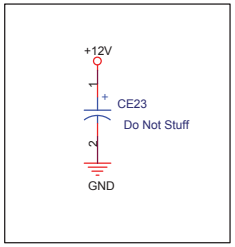






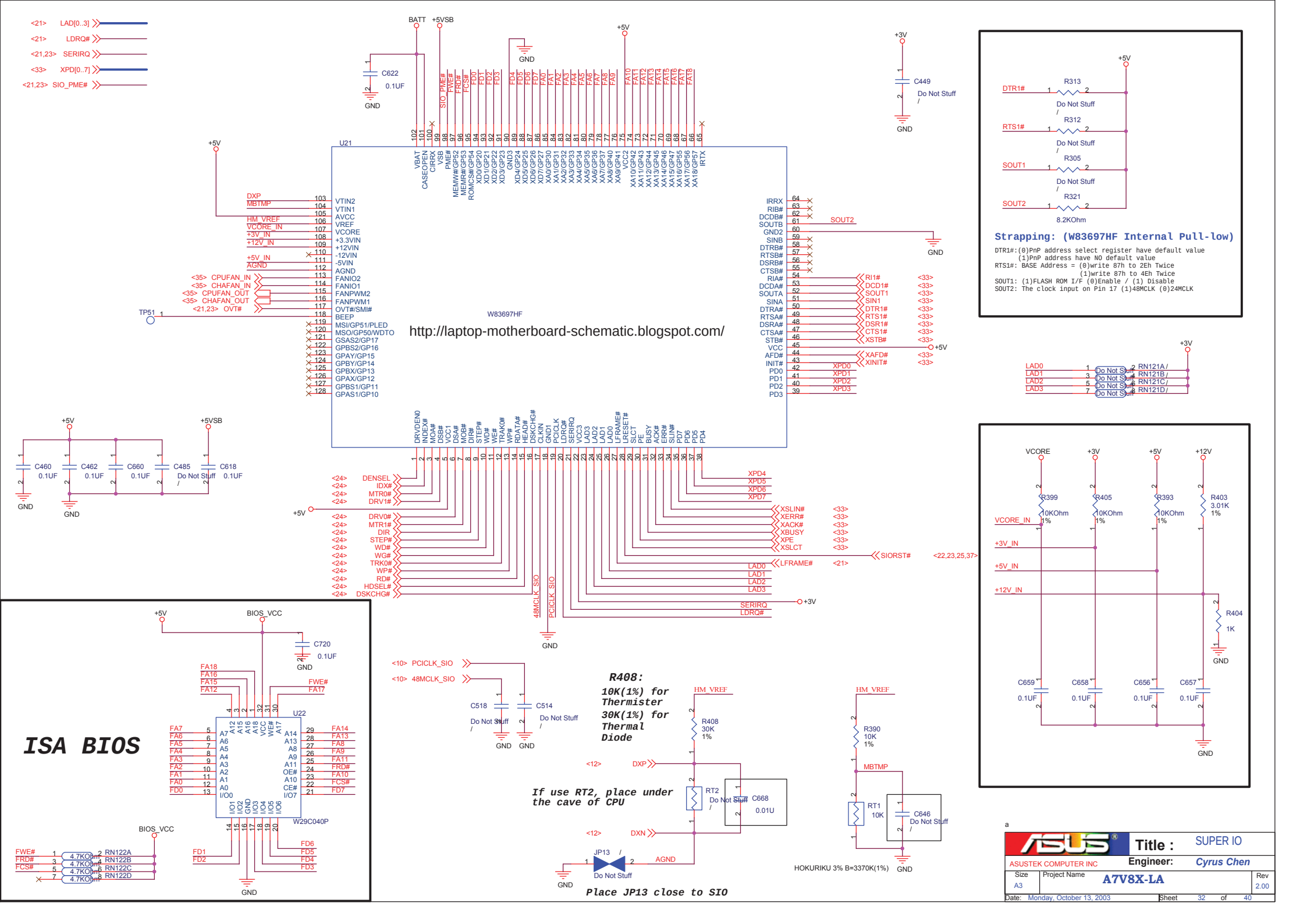


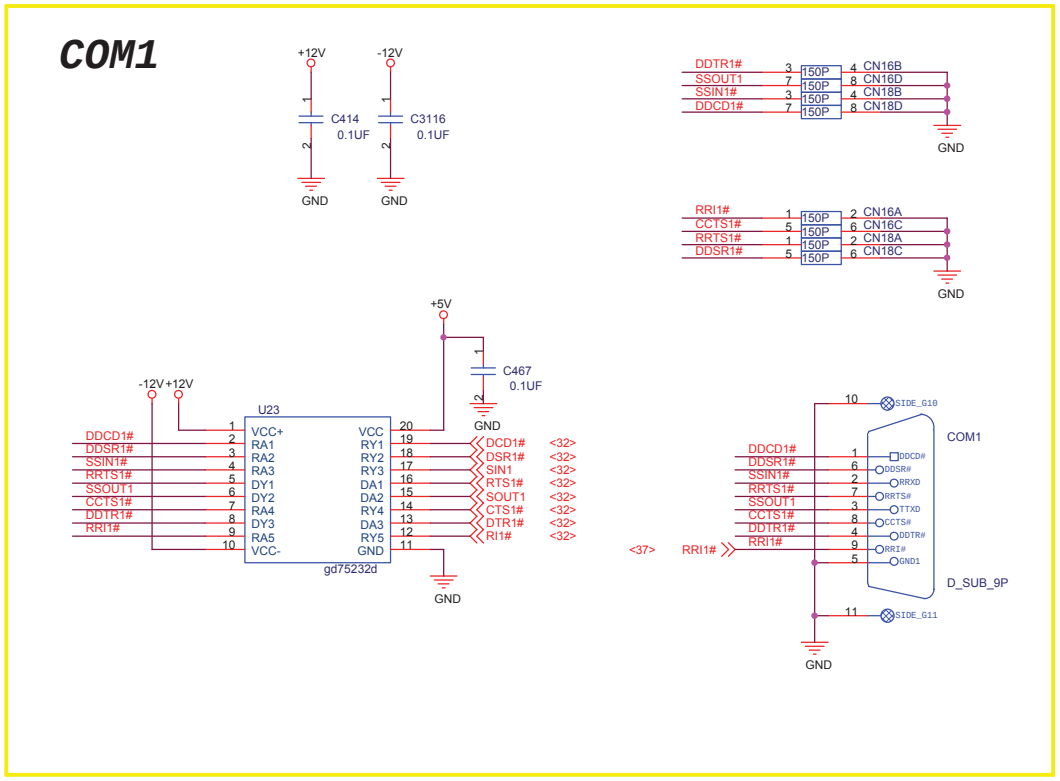


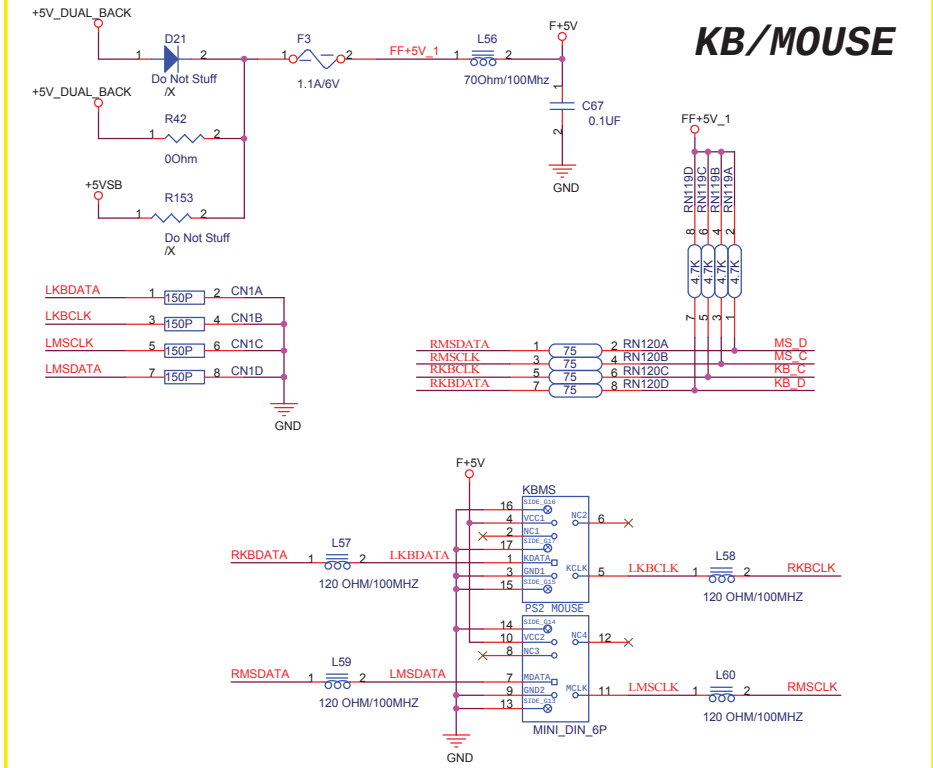


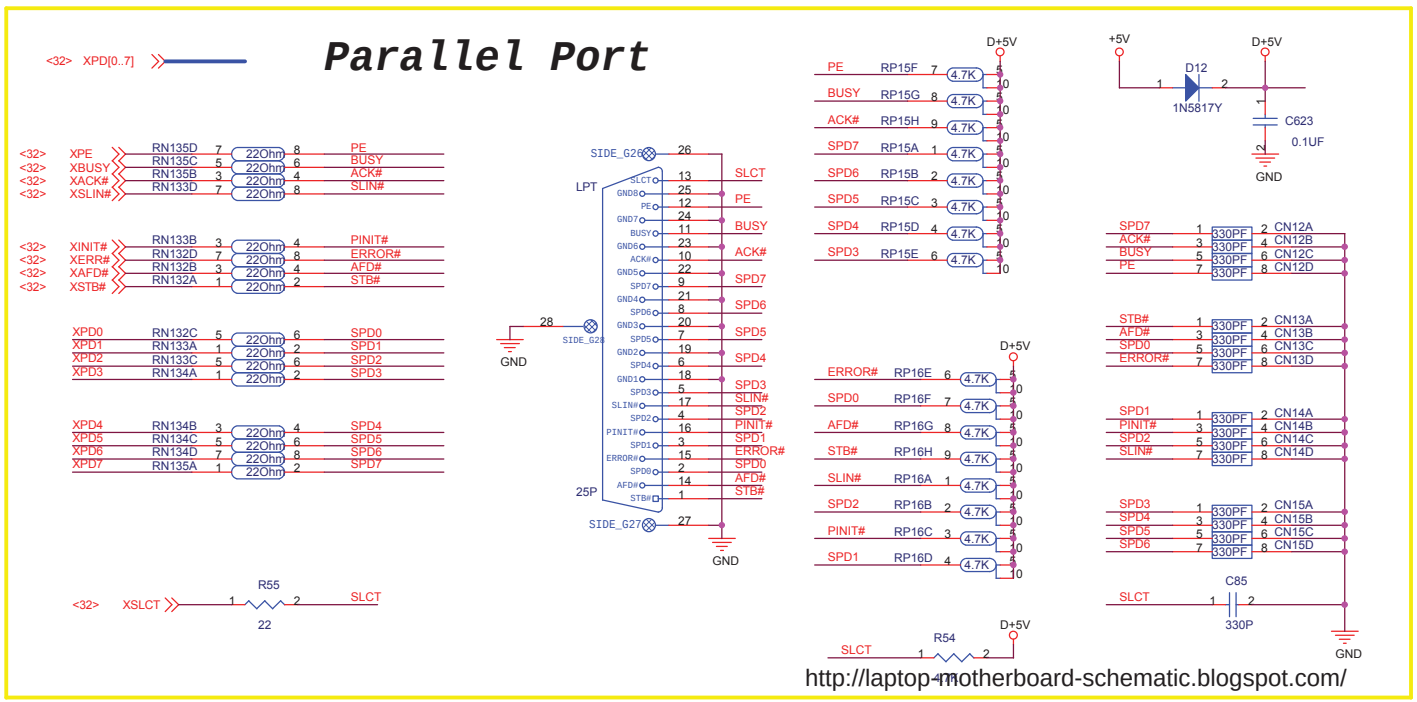
a

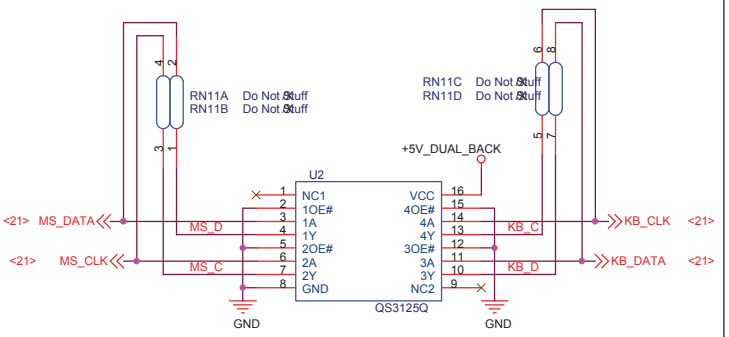
ASUSTEK COMPUTER INC	Title : IEEE1394 CON.	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 31 of 40	


W83697HF
http://laptop-motherboard-schematic.blogspot.com/
ISA BIOS
W29C040P
Strapping: (W83697HF Internal Pull-low)
DTR1#:(0)PnP address select register have default value
(1)PnP address have NO default value
RTS1#: BASE Address = (0)write 87h to 2Eh Twice
(1)write 87h to 4Eh Twice
SOUT1: (1)FLASH ROM I/F (0)Enable / (1) Disable
SOUT2: The clock input on Pin 17 (1)48MCLK (0)24MCLK
R408:
10K(1%) for Thermister
30K(1%) for Thermal Diode
If use RT2, place under the cave of CPU
Place JP13 close to SIO
HOKURIKU 3% B=3370K(1%)
Title : SUPER IO
ASUSTEK COMPUTER INC
Engineer: Cyrus Chen
Size A3
Project Name A7V8X-LA
Rev 2.00
Date: Monday, October 13, 2003
Sheet 32 of 40









http://laptop-motherboard-schematic.blogspot.com/

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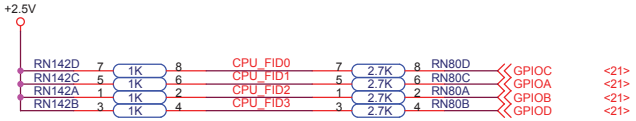
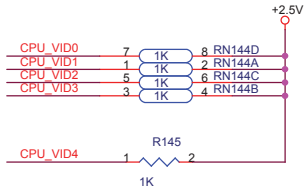
ASUSTEK COMPUTER INC	Title : KB,MS & IO CON.	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 33 of 40	

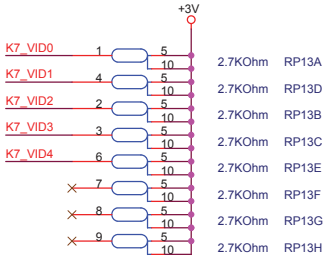
FID

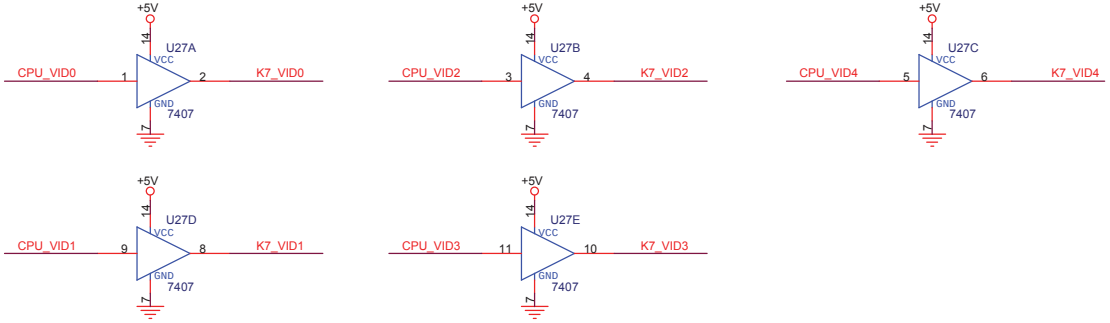


GPIO [D,B,A,C]=> CPU Clock Multiplier			
0000	11	1000	7
0001	11.5	1001	7.5
0010	12	1010	8
0011	12.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	10.5

VID



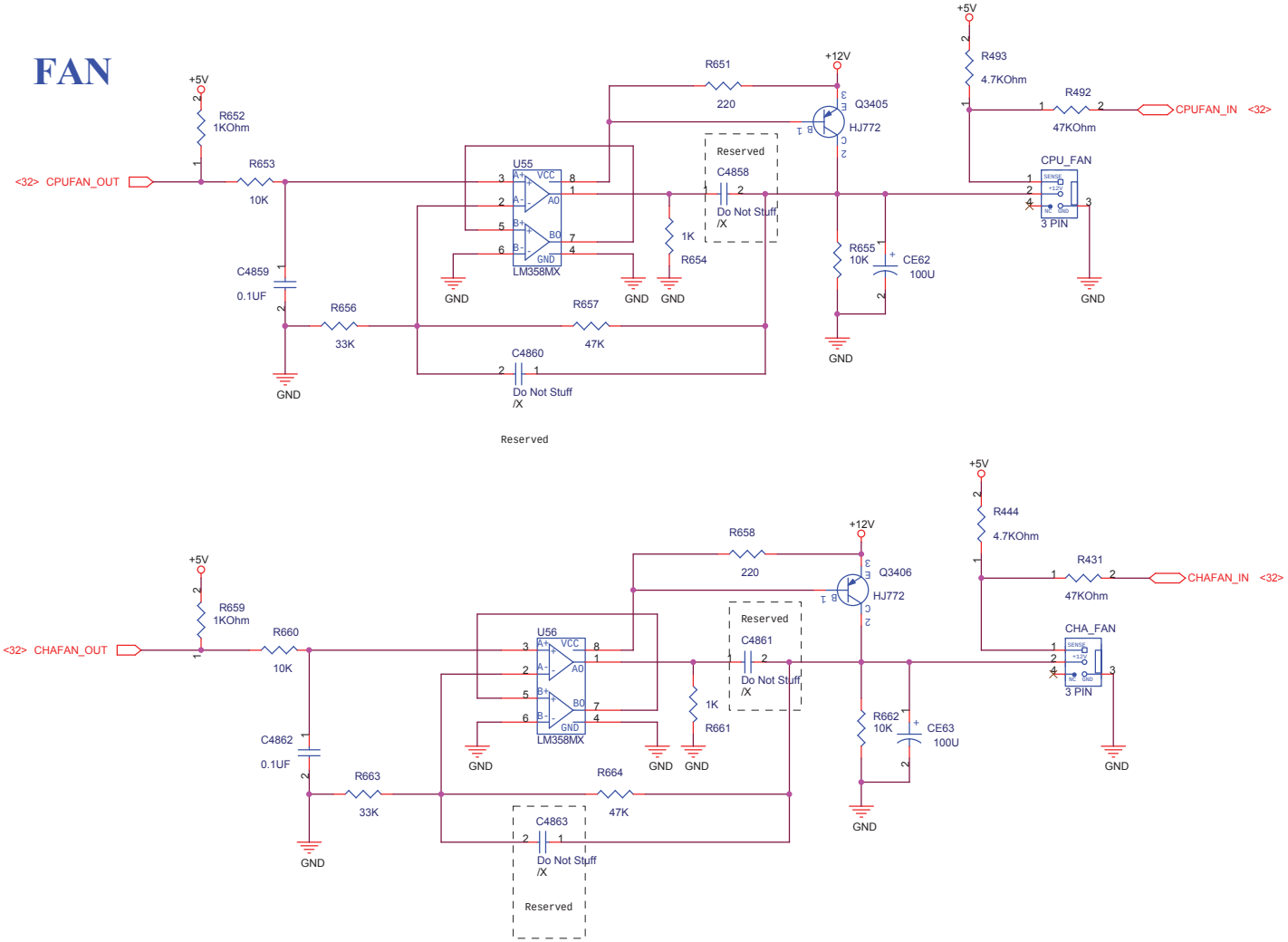




a

ASUSTek Computer Inc.	Title :	FID & VID	
	Engineer:	Cyrus Chen	
Size: A3	Project Name: A7V8X-LA		Rev: 2.00
Date: Monday, October 13, 2003	Sheet 34 of 40		

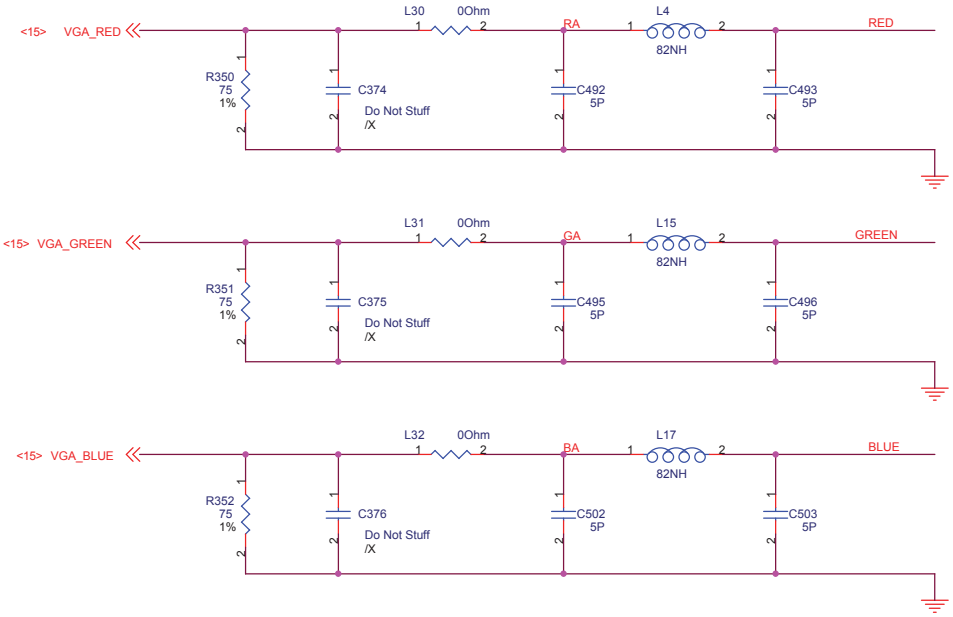
FAN

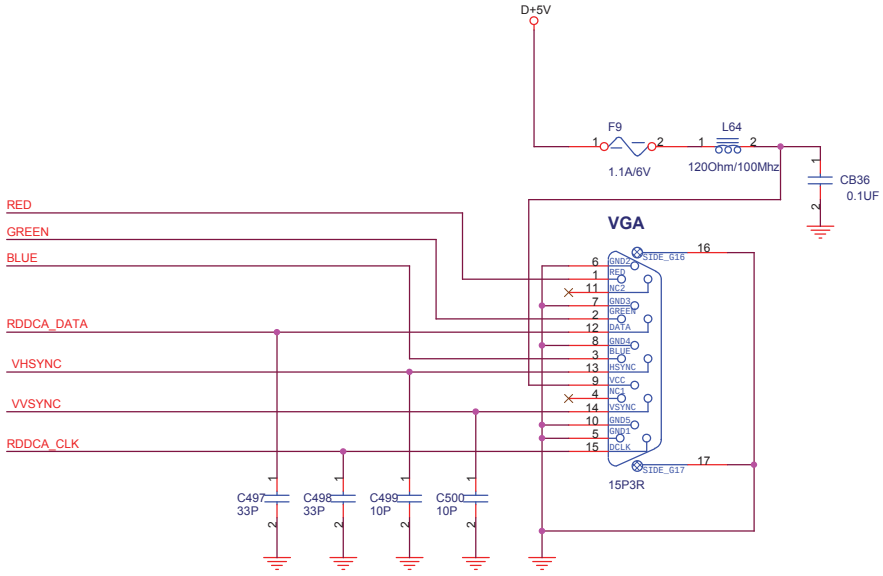


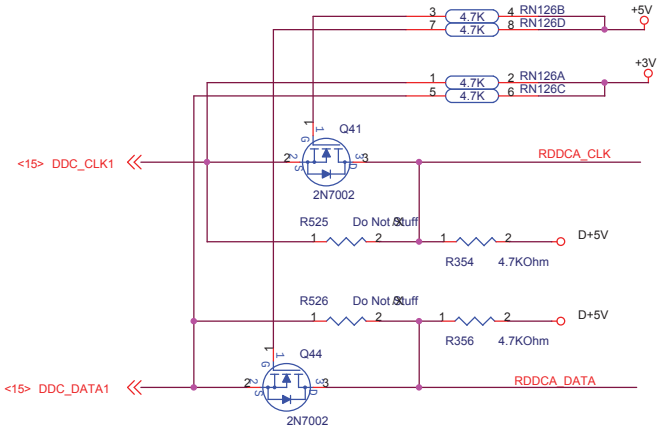
a

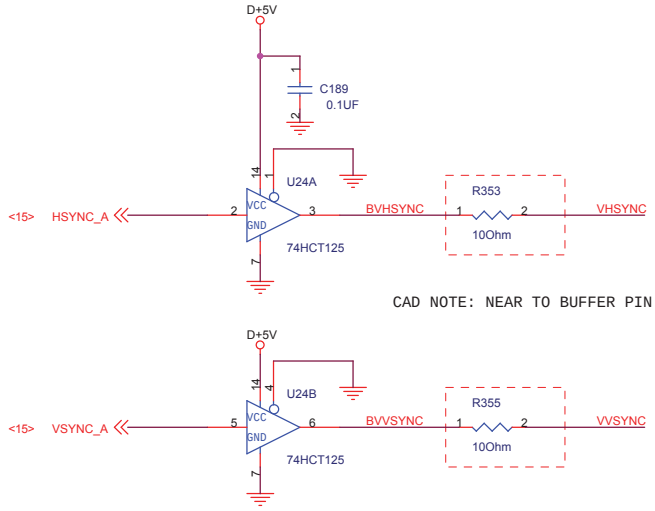
ASUSTEK COMPUTER INC.	Title : FAN	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 35 of 40	

C:10pF 11-033010000
L:68NH 09-023681200
C:22pF 11-033022000
L:68NH 09-023681200
C:10pF 11-033010000









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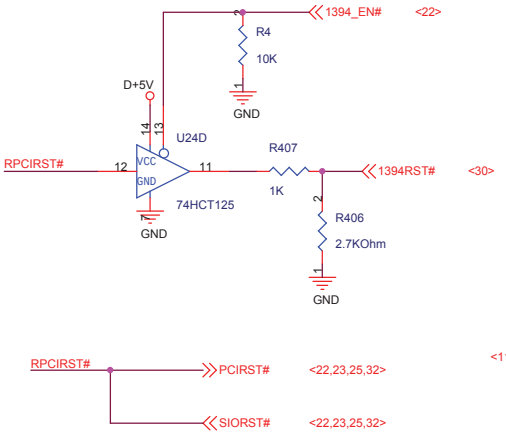
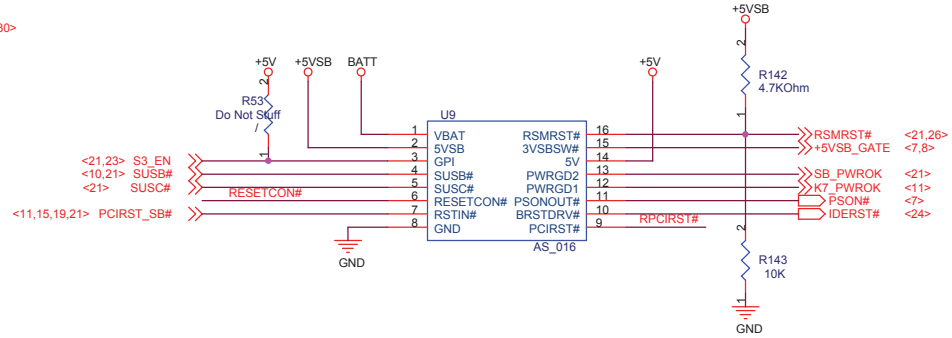
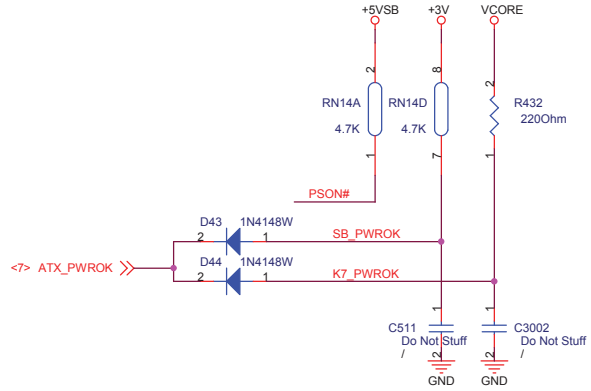
ASUSTEK COMPUTER INC	Title : VGA CONNECTOR	
	Engineer: Cyrus Chen	
Size A3	Project Name A7V8X-LA	Rev 2.00
Date: Monday, October 13, 2003	Sheet 36 of 40	

GPI:
Default LOW in S0/S1/S4/S5(S3_EN low)
Before Enter S3, BIOS need to program high(S3_EN high)

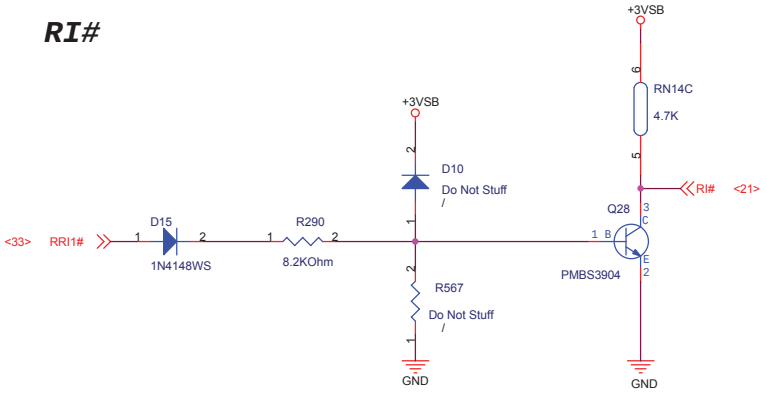


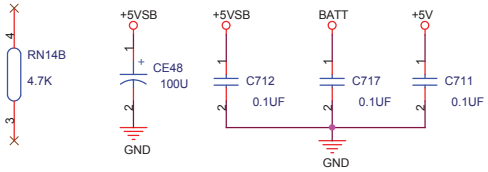


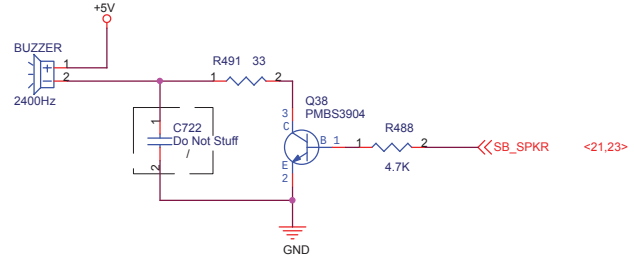


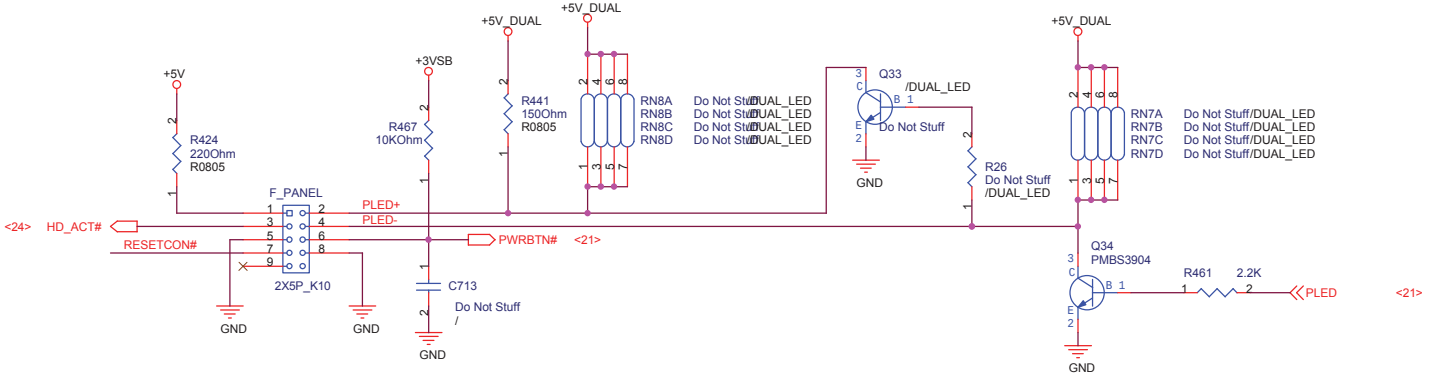
C511, C3002 place near SB, CPU side
For adjust the delay of PWROK

RI#





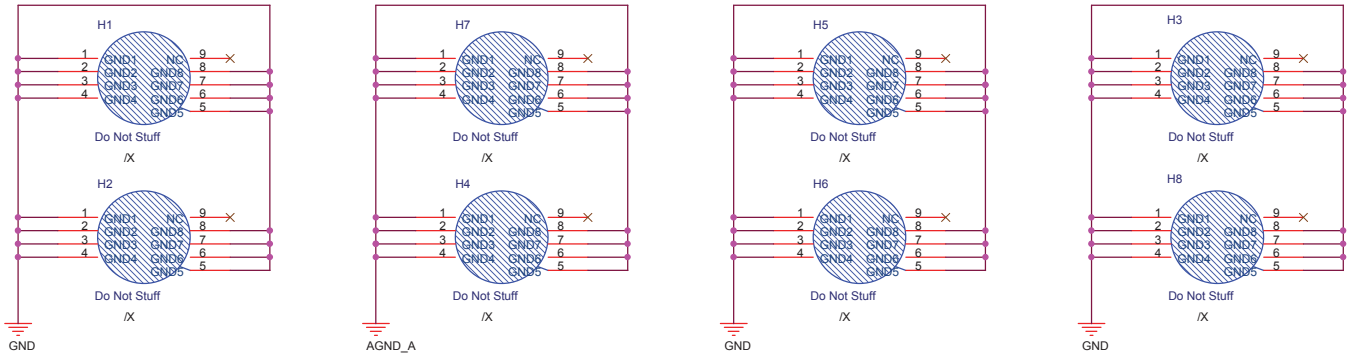


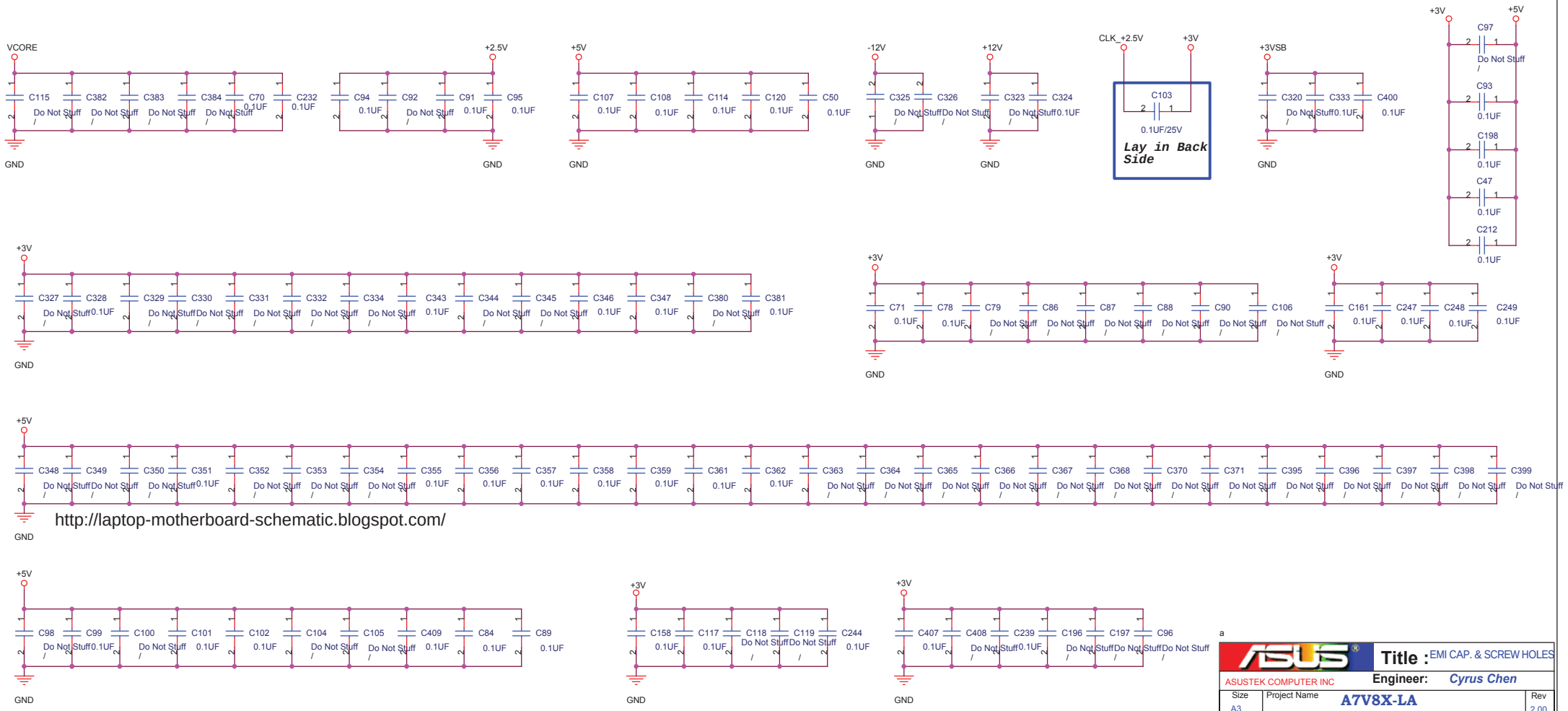


PCB print FRONT_PANEL
beside F_PANEL

a

ASUSTEK COMPUTER INC	Title : PANEL & AS016	
	Engineer: Cyrus Chen	
Size: A3	Project Name: A7V8X-LA	Rev: 2.00
Date: Monday, October 13, 2003	Sheet 37 of 40	





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ASUSTEK COMPUTER INC

Title : EMI CAP. & SCREW HOLES

Engineer: Cyrus Chen

Size	Project Name	Rev
A3	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 38 of 40

INT TABLE

DEVICE	INTA	INTB	INTC	INTD
PCI SLOT 1	INTA#	INTB#	INTC#	INTD#
PCI SLOT 2	INTB#	INTC#	INTD#	INTA#
PCI SLOT 3	INTC#	INTD#	INTA#	INTB#
AGP SLOT	INTA#	INTB#		
C.R.T.(KM400)	INTA#			
1394	INTD#			

IDSEL TABLE

DEVICE	IDSEL
PCI SLOT 1	AD19
PCI SLOT 2	AD20
PCI SLOT 3	AD21
1394	AD22

VT8237 Function Summary

DEVICE	FUNC	Function Description
15 (0FH)	0	Serial ATA Controller
15 (0FH)	1	Parallel ATA Controller
16 (10H)	0	USB 1.1 Ports 0-1
16 (10H)	1	USB 1.1 Ports 2-3
16 (10H)	2	USB 1.1 Ports 4-5
16 (10H)	3	USB 1.1 Ports 6-7
16 (10H)	4	USB 2.0 Ports 0-7
16 (10H)	5	USB 2.0 Communications
17 (11H)	0	Bus Control and Power Mgmt
17 (11H)	5	AC97 Audio Codec Controller
17 (11H)	6	MC97 Modem Codec Controller
18 (12H)	0	VIA LAN Controller

a

ASUSTek Computer Inc.

Title : INT & ID TABLE

Engineer: Cyrus Chen

Size	Project Name	Rev
A3	A7V8X-LA	2.00

Date: Monday, October 13, 2003 Sheet 39 of 40

GPI TABLE

CHIP	GPIO	PIN	FUNCTION	DEFAULT	OUTPUT	POWER
VT8237CD	GPI0	GPI0	CLR_PWD#	GPI	NO	VBAT
VT8237CD	GPI1	GPI1	GPI	GPI	NO	+3VSB
VT8237CD	GPI3	RI#	RI#	RING#	NO	+3VSB
VT8237CD	GPI4	LID#	SIO_PME#	LID#	NO	+3VSB
VT8237CD	GPI5	BATLOW#		BATLOW#	NO	+3VSB
VT8237CD	GPI6	AGPBZ#		AGPBZ#	NO	+3V
VT8237CD	GPI7	REQ5#	PDET80P#	GPI	NO	+3V
VT8237CD	GPIO8	VGATE		GPI	PUSH/PULL	+3V
VT8237CD	GPI9	UDPWR		GPI	NO	+3V
VT8237CD	GPIO12	INTE#		GPI	PUSH/PULL	+3V
VT8237CD	GPIO13	INTF#		GPI	PUSH/PULL	+3V
VT8237CD	GPIO14	INTG#		GPI	PUSH/PULL	+3V
VT8237CD	GPIO15	INTH#		GPI	PUSH/PULL	+3V
VT8237CD	GPI16	INTRUDER#	CLR_CMOS#	INTRUDER#	PUSH/PULL	VBAT
VT8237CD	GPI17	CPUMISS		CPUMISS	NO	+3V
VT8237CD	GPI18	AOLGPI	THRM#	GPI	NO	+3VSB
VT8237CD	GPIO20	SDIN2	SDIN2	SDIN2	OD	+3V
VT8237CD	GPIO21	SDIN3	SDIN3	SDIN3	OD	+3V
VT8237CD	GPIO22	GHI#	GPIO22	GPI	OD	+3V
VT8237CD	GPIO23	DPSLP	GPIO23	GPI	OD	+3V
VT8237CD	GPIO26	SMBDT2	SMBDT2	GPI	OD	+3VSB
VT8237CD	GPIO27	SMBCK2	SMBCK2	GPI	OD	+3VSB
VT8237CD	GPIO28	VIDSEL	SATALED#	GPI	OD	+3V
VT8237CD	GPIO29	VRDSLP	SDET80P#	GPI	OD	+3V

GPO TABLE

CHIP	GPIO	PIN	FUNCTION	DEFAULT	OUTPUT	POWER
VT8237CD	GPO0	GPO0	PLED	GPO	PUSH/PULL	+3VSB
VT8237CD	GPO1	GPO1		GPO1	PUSH/PULL	+3VSB
VT8237CD	GPO2	SUSA#	S3_EN	SUSA#	PUSH/PULL	+3VSB
VT8237CD	GPO3	SUS_ST#	SUS_ST#	SUS_ST#	PUSH/PULL	+3VSB
VT8237CD	GPO4	SUSCLK	LINK_LED#	SUSCLK	PUSH/PULL	+3VSB
VT8237CD	GPO5	CPUSTP#		CPUSTP#	PUSH/PULL	+3V
VT8237CD	GPO6	PCISLP#	STRAPPING	PCISLP#	PUSH/PULL	+3V
VT8237CD	GPO7	GNT5#	DDR_GPO	GPO	PUSH/PULL	+3V
VT8237CD	GPIO12	INTE#		GPI12	PUSH/PULL	+3V
VT8237CD	GPIO13	INTF#		GPI13	PUSH/PULL	+3V
VT8237CD	GPIO14	INTG#	VDDQ_GPO	GPI14	PUSH/PULL	+3V
VT8237CD	GPIO15	INTH#	1394_EN#	GPI15	PUSH/PULL	+3V
VT8237CD	GPIO30	GPIOC	STRAPPING	GPI30	PUSH/PULL	+3V
VT8237CD	GPIO24	GPIOA	STRAPPING	GPI24	PUSH/PULL	+3V
VT8237CD	GPIO25	GPIOB	STRAPPING	GPI25	PUSH/PULL	+3V
VT8237CD	GPIO31	GPIOD	STRAPPING	GPI31	PUSH/PULL	+3V
VT8237CD	GPIO20	SDIN2	SDIN2	SDIN2	OD	+3V
VT8237CD	GPIO21	SDIN3	SDIN3	SDIN3	OD	+3V
VT8237CD	GPIO22	GHI#	GPIO22	GPI	OD	+3V
VT8237CD	GPIO23	DPSLP	GPIO23	GPI	OD	+3V
VT8237CD	GPIO26	SMBDT2	SMBDT2	GPI	OD	+3VSB
VT8237CD	GPIO27	SMBCK2	SMBCK2	GPI	OD	+3VSB
VT8237CD	GPIO28	VIDEL		GPI	OD	+3V
VT8237CD	GPIO29	VRDSLP		GPI	OD	+3V

a

ASUSTek Computer Inc.

Title : GPIO

Engineer: Cyrus Chen

Size	Project Name	Rev
A3	A7V8X-LA	2.00

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