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36	RGMII LAN 88E1116 PHY0
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38	HD AUDIO CODEC
39	W83627EHF SuperI/O
40	MCP55P CORE&DDRII Power
41	PWR SEQU & VID BUFFER
42	OVP & CPUFAN + PROCHOT
43	Dual LAN + USB CONN
44	FP-USB CONN
45	PWR CON/F-PNL/VBAT/SPKR
46	.K/M+LPC+Bios+FDC+IDE
47	MOUNTING HOLES&FIDUCIALS&etc
48	

ABIT

KN9 SLI V0.1

MCP55P	MCP55 Ultra	MCP55S
PCIE controller x6 x16,x8,x1,x1,x1,x1	PCIE controller x6 x16,x1,x1,x1,x1	PCIE controller x5 x16,x1,x1,x1,x1
SATA controller x3	SATA controller x2	SATA controller x2
MAC0 RGMII & all MAC1 RGMII only	MAC0 RGMII & all	MAC0 RGMII & all
SSID：1C20	SSID：1C20	SSID：1C20

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Title: COVER

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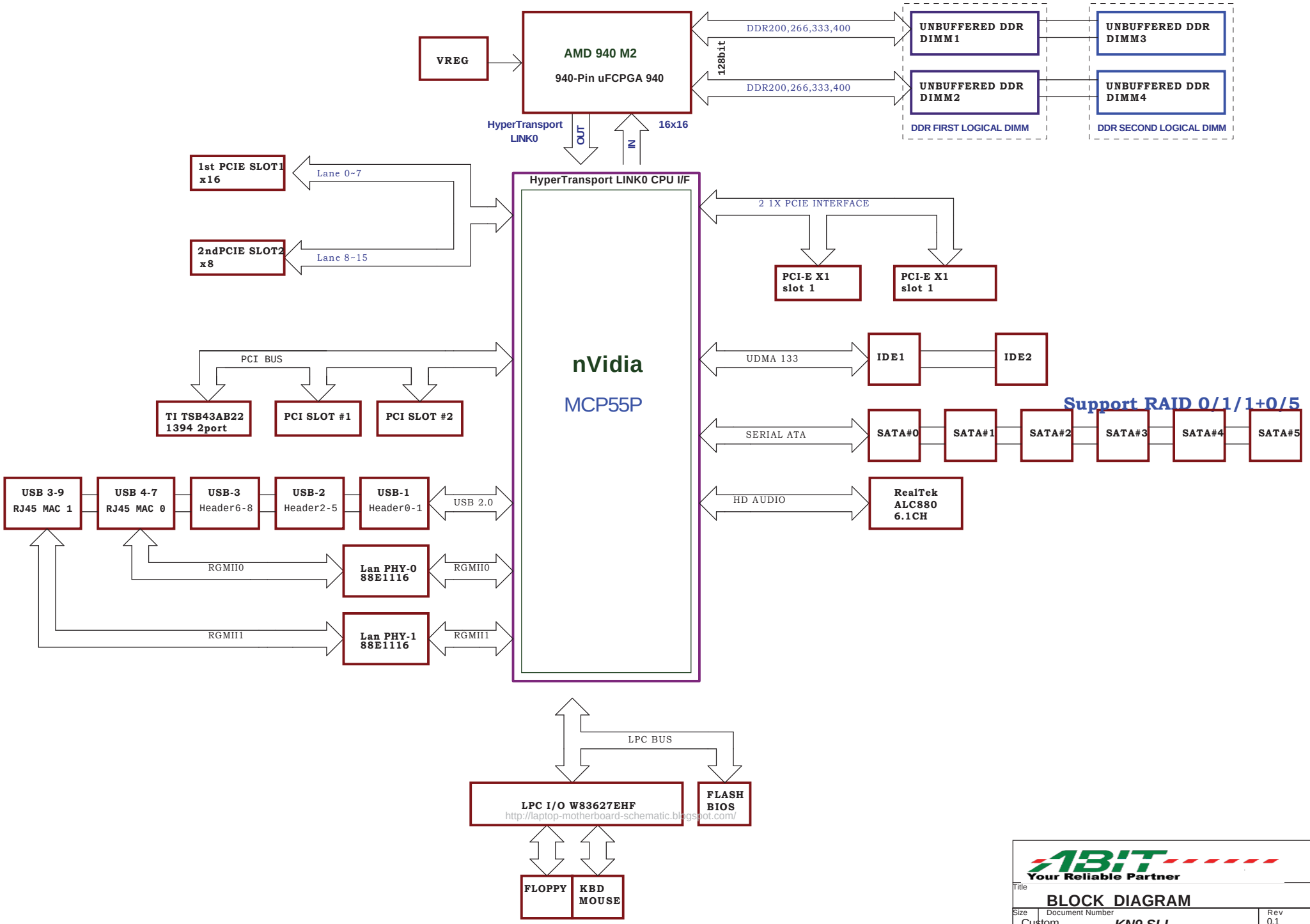

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Title: BLOCK DIAGRAM		
Size: Custom	Document Number: KN9 SLI	Rev: 0.1
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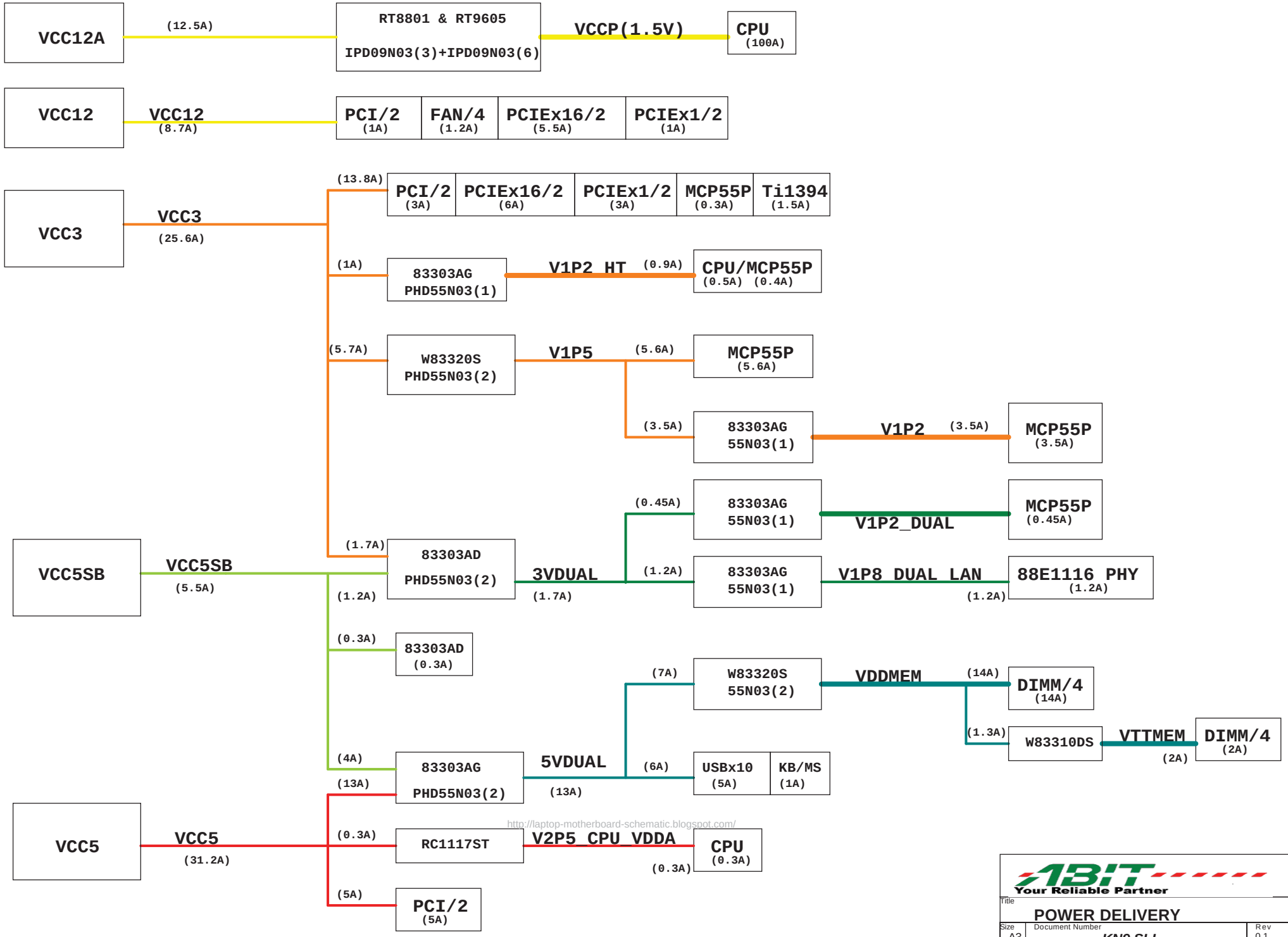

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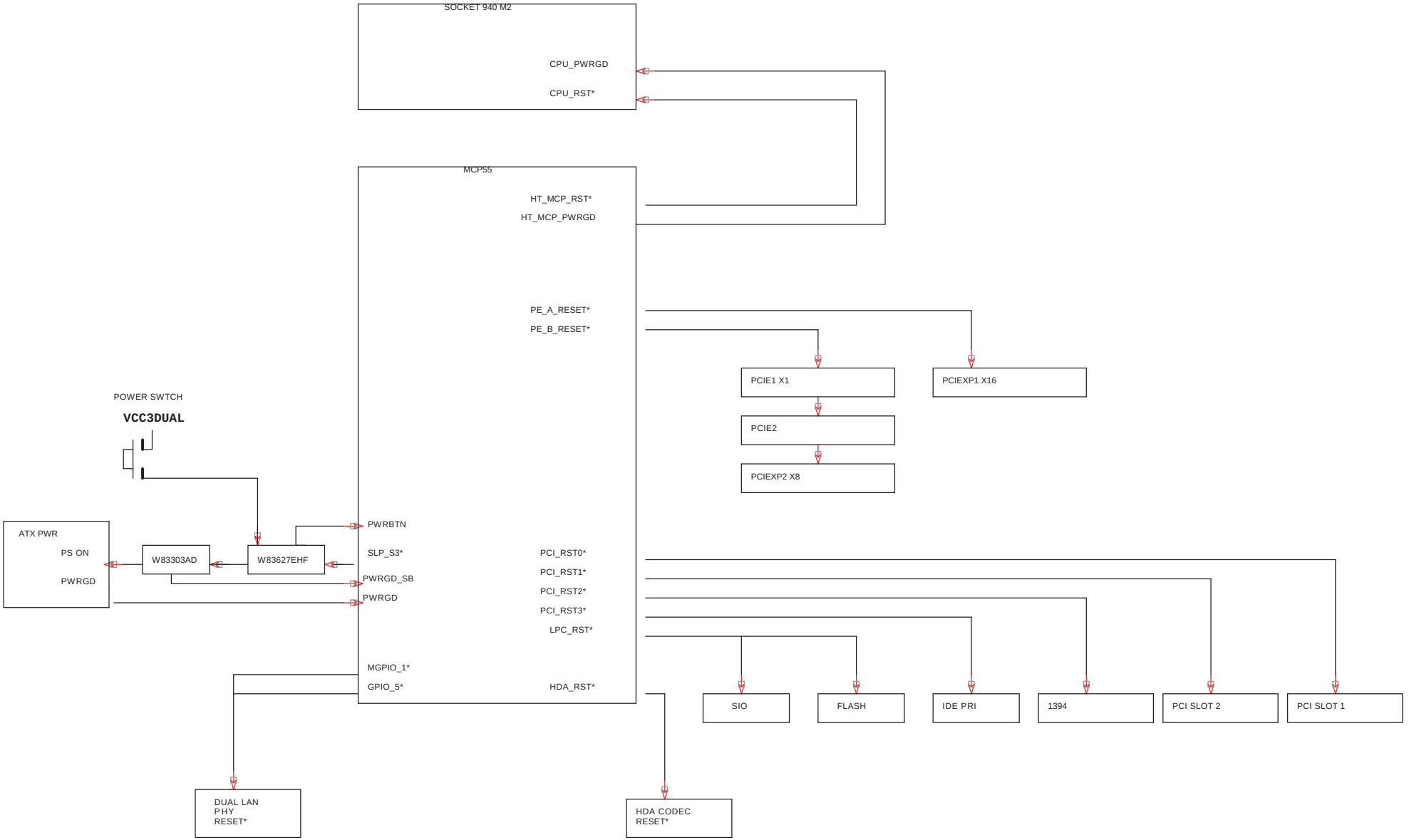
Title: POWER DELIVERY		
Size: A3	Document Number: KN9 SLI	Rev: 0.1
Date: Friday, March 31, 2006	Sheet 3 of 47	



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Title: RESET DIAGRAM

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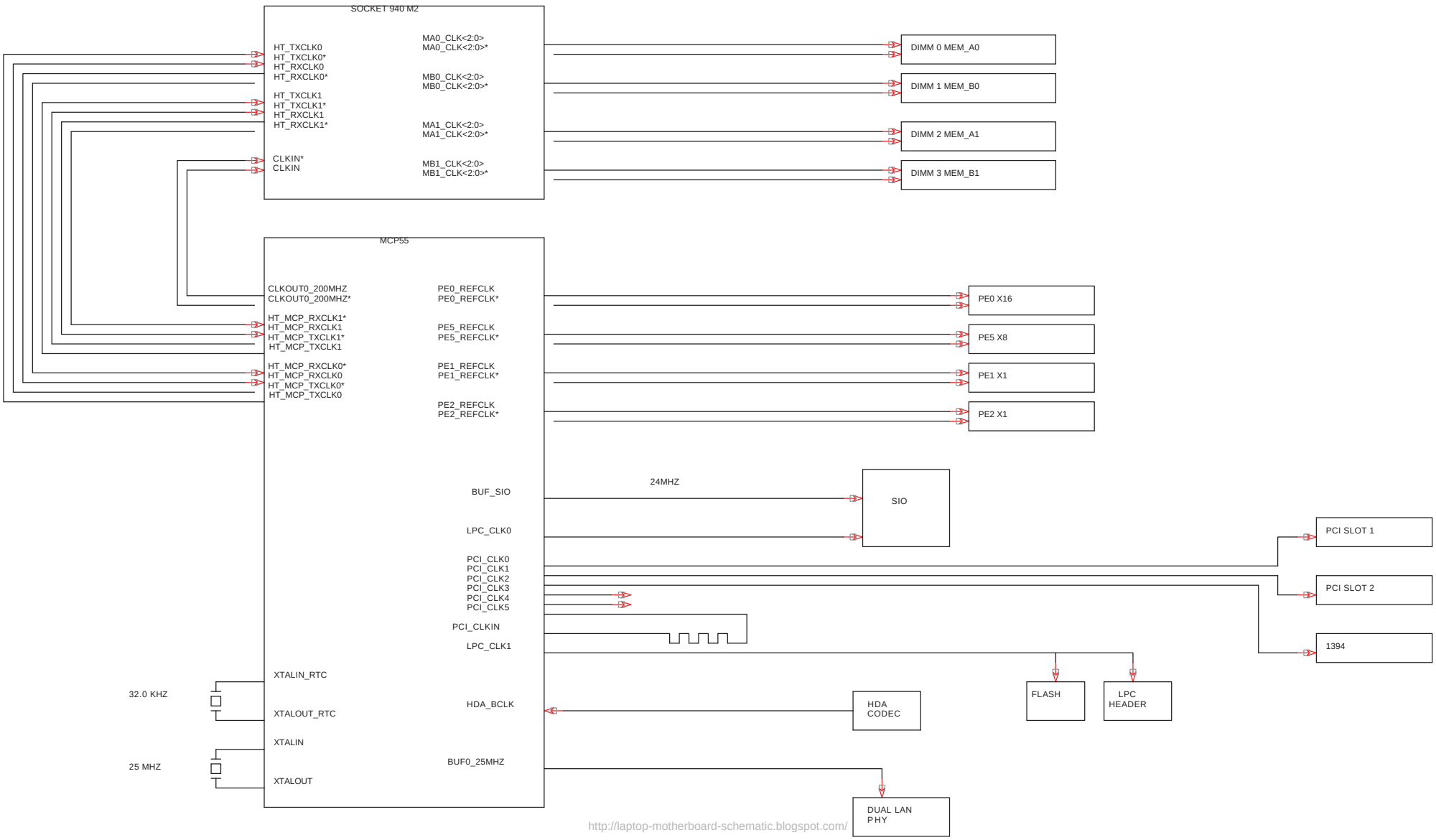

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Title: CLOCK DIAGRAM

Size	Document Number	Rev
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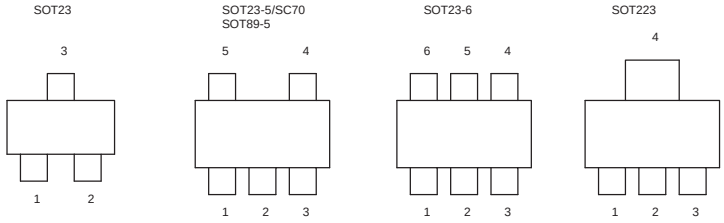
CPU VID TABLE	
VID	VOLTAGE
000000	1.5500V
000001	1.5250V
000010	1.5000V
000011	1.4750V
000100	1.4500V
000101	1.4250V
000110	1.4000V
000111	1.3750V
001000	1.3500V
001001	1.3250V
001010	1.3000V
001011	1.2750V
001100	1.2500V
001101	1.2250V
001110	1.2000V
001111	1.1750V
010000	1.1500V
010001	1.1250V
010010	1.1000V
010011	1.0750V
010100	1.0500V
010101	1.0250V
010110	1.0000V
010111	0.9750V
011000	0.9500V
011001	0.9250V
011010	0.9000V
011011	0.8750V
011100	0.8500V
011101	0.8250V
011110	0.8000V
011111	0.7750V
100000	0.7625V
100001	0.7500V
100010	0.7375V
100011	0.7250V
100100	0.7125V
100101	0.7000V
100110	0.6875V
100111	0.6750V
101000	0.6625V
101001	0.6500V
101010	0.6375V
101011	0.6250V
101100	0.6125V
101101	0.6000V
101110	0.5875V
101111	0.5750V
110000	0.5625V
110001	0.5500V
110010	0.5375V
110011	0.5250V
110100	0.5125V
110101	0.5000V
110110	0.4875V
110111	0.4750V
111000	0.4625V
111001	0.4500V
111010	0.4375V
111011	0.4250V
111100	0.4125V
111101	0.4000V
111110	0.3875V
111111	0.3750V

SMBUS ADDRESS MAP		
DEVICE	BUS#	ADDRESS
DIMM 1 MEM_A0	0	1010 000 = 0X50
DIMM 2 MEM_B0	0	1010 001 = 0X51
DIMM 3 MEM_A1	0	1010 010 = 0X52
DIMM 4 MEM_B1	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
1394	1	ARP
PE5 SLOT 4	1	ARP
PE2 SLOT 5	1	ARP
PE1 SLOT 6	1	ARP
PE0 SLOT 7	1	ARP

PCI INTERRUPT/IDSEL MAP								
BACK PANEL SLOT	BUS#	DEV#	IDSEL	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
1	01	0X06	26	INTY*	INTZ*	INTW*	INTX*	4/4
2	01	0X07	25	INTX*	INTY*	INTZ*	INTW*	3/3
3	01	0X08	24	INTW*	INTX*	INTY*	INTZ*	2/2

PCI DEVICE MAP					
DEVICE	BUS#	DEV#	FUNCTION	VENDOR ID	DEVICE ID
AMD CPU					
HT CONFIG	0	0X18	0	0X1022	0X1100
ADDR MAP CONFIG	0	0X18	1	0X1022	0X1101
DRMA CTL & CONFIG	0	0X18	2	0X1022	0X1102
MISC CONFIG	0	0X18	3	0X1022	0X1103
MCP55					
LDT	0	0X00	0		0X0369
LPC	0	0X01	0		0X0360 - 0X367
SMBUS2	0	0X01	1		0X0368
SHAPE TRIM	0	0X01	2		0X036A
PMU	0	0X01	3		0X036B
USB 1.1	0	0X02	0		0X036C
USB 2.0	0	0X02	1		0X036D
IDE	0	0X04	0		0X036E
SATA	0	0X05	0		0X037E
SATA RAID	0	0X05	0		0X037F
PCI-PCI BRIDGE	0	0X06	0		0X0370
PCI SLOT 1	1	0X06	ARB	ARB	ARB
PCI SLOT 2	1	0X07	ARB	ARB	ARB
PCI SLOT 3	1	0X08	ARB	ARB	ARB
AUDIO CODEC	0	0X06	1		0X0371
MAC	0	0X08	0		0X0372 / 0X0373
MAC	0	0X09	0		0X0372 / 0X0373
PE X8+VC1	0	0X0A	0		0X0376
PE X4	0	0X0B	0		0X0374
PE X4	0	0X0C	0		0X0374
PE X4+VC1	0	0X0D	0		0X0378
PE X8	0	0X0E	0		0X0375
PE X16	0	0X0F	0		0X0377



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Title: DEVICE TABLES

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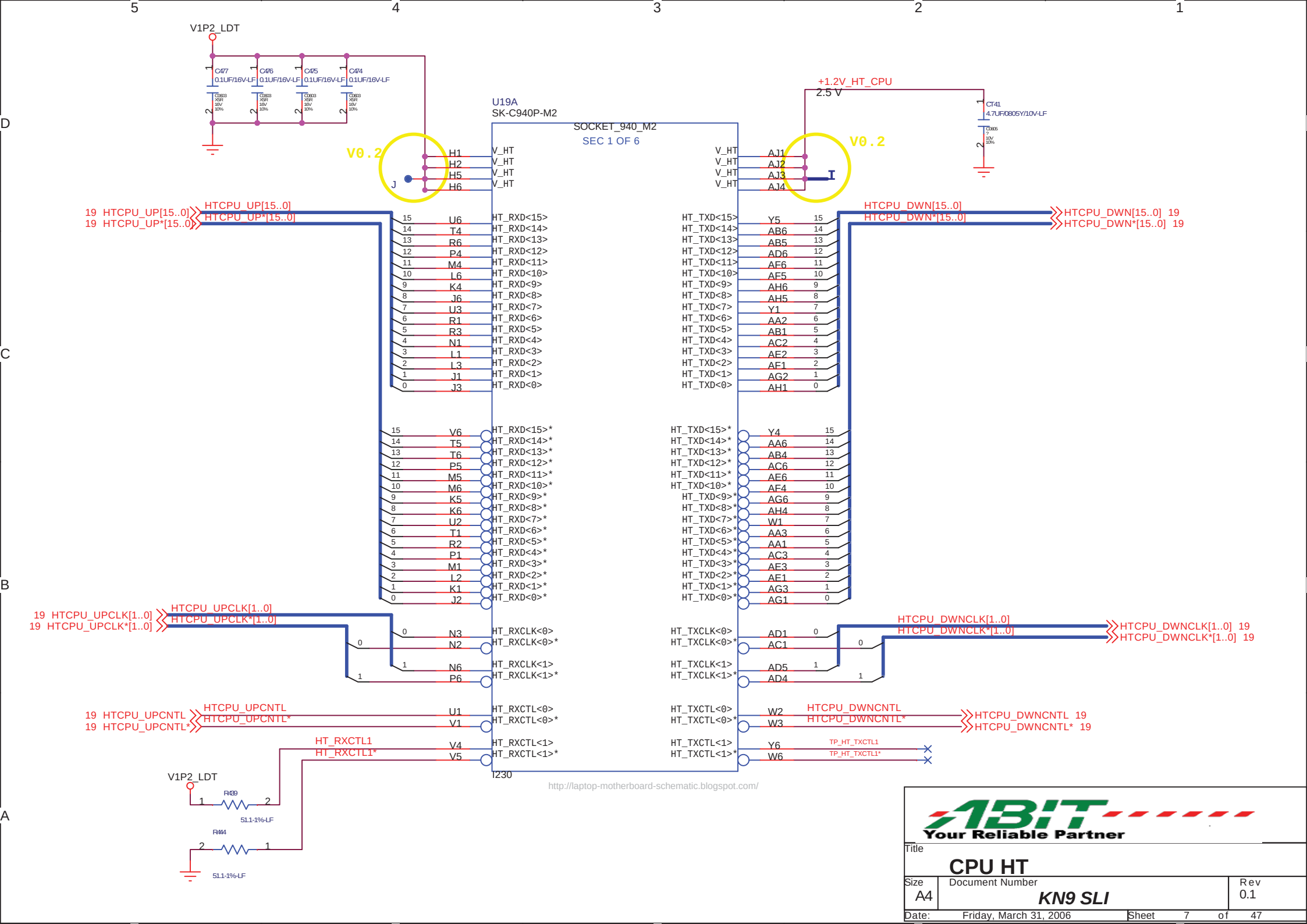
V1P2_LDT
C477 0.1UF/16V-LF
C476 0.1UF/16V-LF
C475 0.1UF/16V-LF
C474 0.1UF/16V-LF
U19A
SK-C940P-M2
SOCKET_940_M2
SEC 1 OF 6
V0.2
+1.2V_HT_CPU
2.5 V
CT41 4.7UF/0805Y/10V-LF
HTCPU_UP[15..0]
HTCPU_UP*[15..0]
HTCPU_DWN[15..0]
HTCPU_DWN*[15..0]
HTCPU_UPCLK[1..0]
HTCPU_UPCLK*[1..0]
HTCPU_DWNCLK[1..0]
HTCPU_DWNCLK*[1..0]
HTCPU_UPCNTL
HTCPU_UPCNTL*
HTCPU_DWNCNTL
HTCPU_DWNCNTL*
HT_RXCTL1
HT_RXCTL1*
R439 511-1%-LF
R444 511-1%-LF
TP_HT_TXCTL1
TP_HT_TXCTL1*
I230
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CPU HT
KN9 SLI
Size A4
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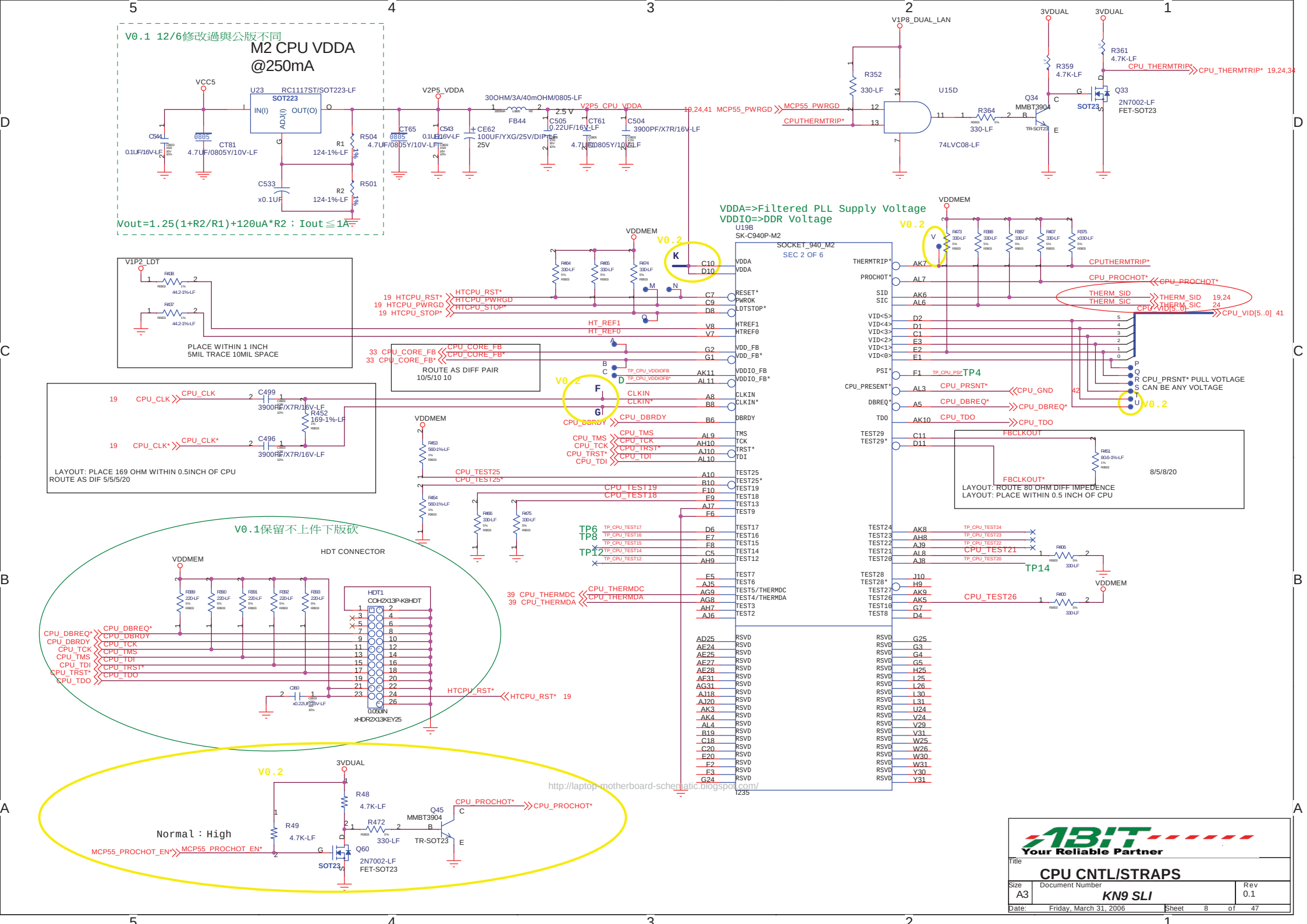
V0.1 12/6修改過與公版不同
M2 CPU VDDA
@250mA
Vout=1.25(1+R2/R1)+120uA*R2 : Iout≦1A
VDDA=>Filtered PLL Supply Voltage
VDDIO=>DDR Voltage
PLACE WITHIN 1 INCH
5MIL TRACE 10MIL SPACE
ROUTE AS DIFF PAIR
10/5/10 10
LAYOUT: PLACE 169 OHM WITHIN 0.5INCH OF CPU
ROUTE AS DIF 5/5/5/20
CPU_PRSNT* PULL VOTLAGE
CAN BE ANY VOLTAGE
LAYOUT: ROUTE 80 OHM DIFF IMPEDENCE
LAYOUT: PLACE WITHIN 0.5 INCH OF CPU
V0.1保留不上件下版砍
HDT CONNECTOR
Normal : High
SOCKET_940_M2
SEC 2 OF 6
U19B
SK-C940P-M2
74LVC08-LF
2N7002-LF
FET-SOT23
MMBT3904
TR-SOT23
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CPU CNTL/STRAPS
KN9 SLI
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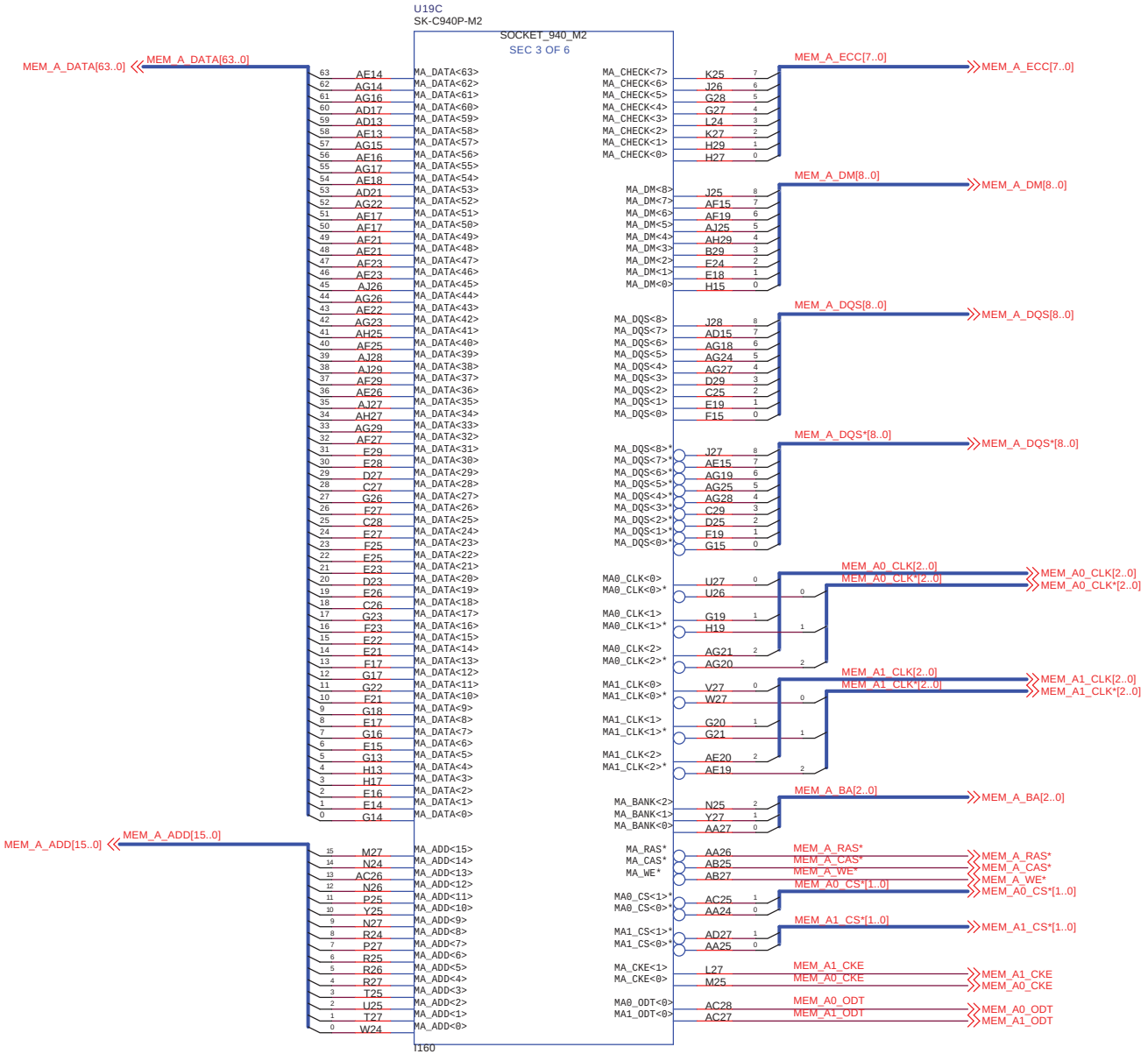

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Title: CPU MEM_A

Size	Document Number	Rev
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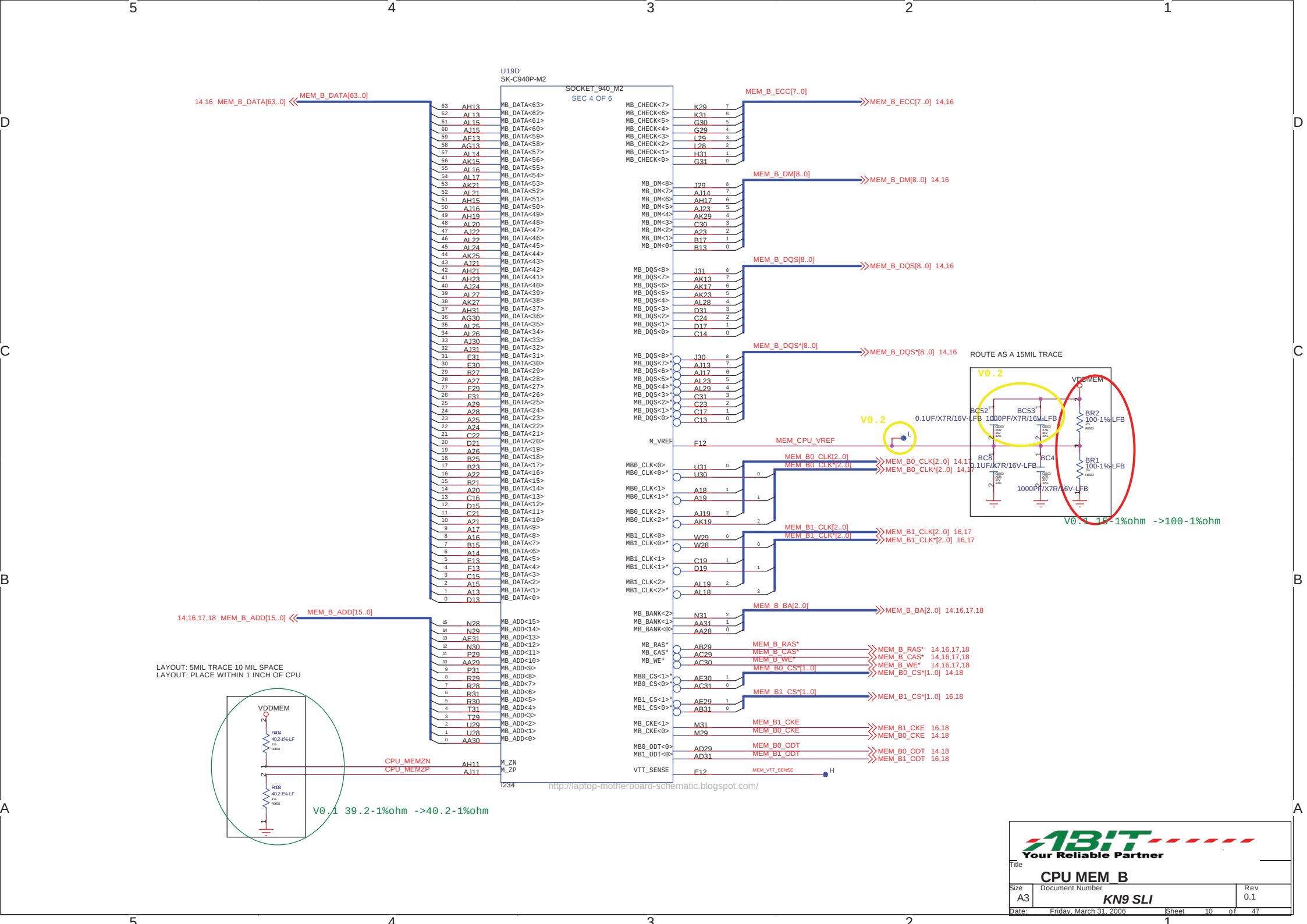
U19D
SK-C940P-M2
SOCKET_940_M2
SEC 4 OF 6
14,16 MEM_B_DATA[63..0]
MEM_B_DATA[63..0]
MEM_B_ECC[7..0]
MEM_B_ECC[7..0] 14,16
MEM_B_DM[8..0]
MEM_B_DM[8..0] 14,16
MEM_B_DQS[8..0]
MEM_B_DQS[8..0] 14,16
MEM_B_DQS*[8..0]
MEM_B_DQS*[8..0] 14,16
ROUTE AS A 15MIL TRACE
V0.2
VDDMEM
BC52
BC53
BR2
100-1%-LFB
0.1UF/X7R/16V-LFB
1000PF/X7R/16V-LFB
BC8
BC4
BR1
M_VREF
MEM_CPU_VREF
MEM_B0_CLK[2..0]
MEM_B0_CLK*[2..0]
MEM_B0_CLK[2..0] 14,17
MEM_B0_CLK*[2..0] 14,17
MEM_B1_CLK[2..0]
MEM_B1_CLK*[2..0]
MEM_B1_CLK[2..0] 16,17
MEM_B1_CLK*[2..0] 16,17
MEM_B_BA[2..0]
MEM_B_BA[2..0] 14,16,17,18
MEM_B_RAS*
MEM_B_CAS*
MEM_B_WE*
MEM_B_RAS* 14,16,17,18
MEM_B_CAS* 14,16,17,18
MEM_B_WE* 14,16,17,18
MEM_B0_CS*[1..0]
MEM_B0_CS*[1..0] 14,18
MEM_B1_CS*[1..0]
MEM_B1_CS*[1..0] 16,18
MEM_B1_CKE
MEM_B0_CKE
MEM_B1_CKE 16,18
MEM_B0_CKE 14,18
MEM_B0_ODT
MEM_B1_ODT
MEM_B0_ODT 14,18
MEM_B1_ODT 16,18
MEM_VTT_SENSE
V0.1 15-1%ohm ->100-1%ohm
14,16,17,18 MEM_B_ADD[15..0]
MEM_B_ADD[15..0]
LAYOUT: 5MIL TRACE 10 MIL SPACE
LAYOUT: PLACE WITHIN 1 INCH OF CPU
VDDMEM
R804
40.2-1%-LF
R808
40.2-1%-LF
CPU_MEMZN
CPU_MEMZP
V0.1 39.2-1%ohm ->40.2-1%ohm
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ABIT
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Title
CPU MEM_B
Size
A3
Document Number
KN9 SLI
Rev
0.1
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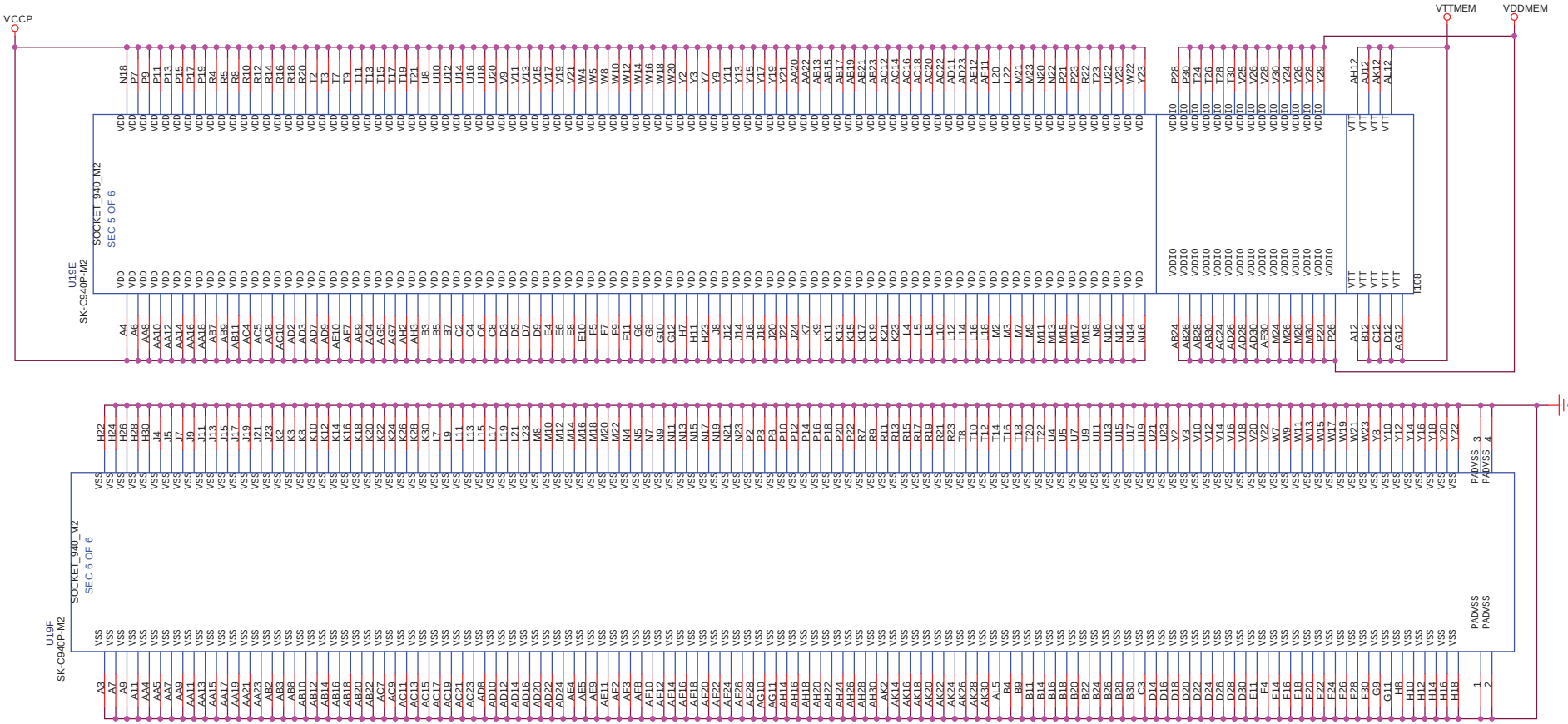

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Title: CPU MEM/GND

Size	Document Number	Rev
A3	KN9 SLI	0.1

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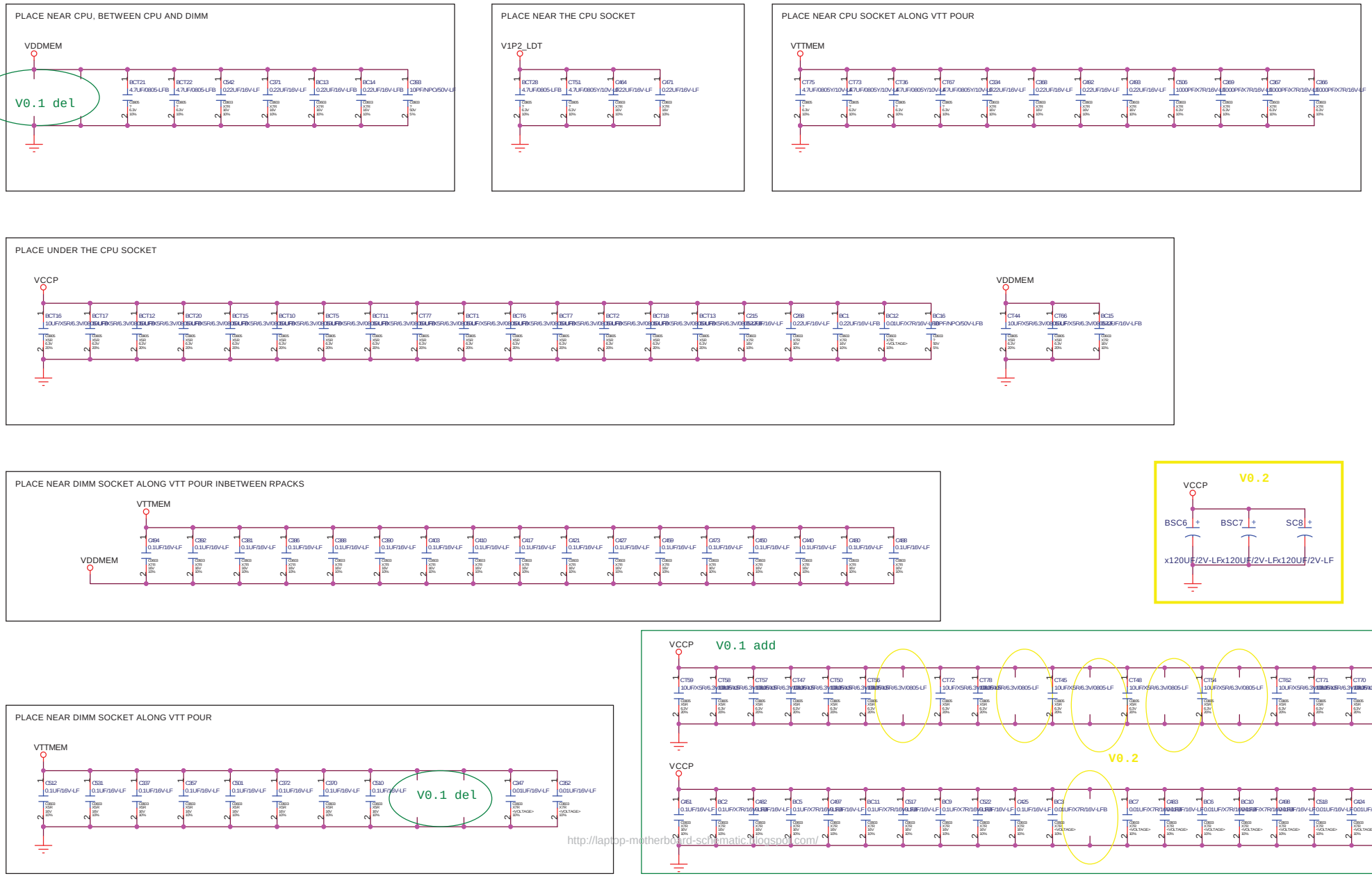

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Title

CPU DECOUPLING

Size	Document Number	Rev
A3	*KN9 SLI*	0.1

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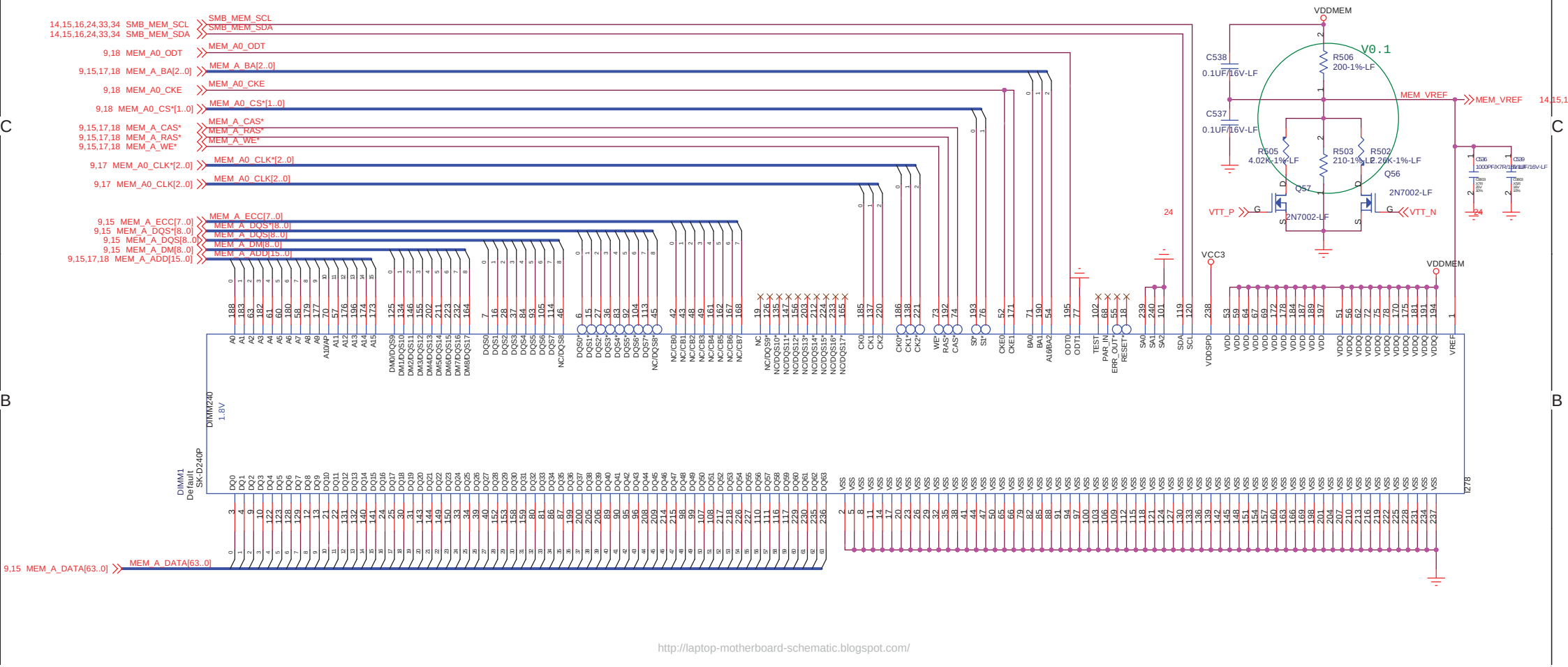
VTT_P	VTT_N	VTT_VREF
0	0	(VDDR / 2)*102%_0.922
0	1	(VDDR / 2)*98%_0.882
1	0	(VDDR / 2)*100%_0.899 *
1	1	(VDDR / 2)*96%_0.856

DIMM 1

CLOSEST DIMM TO CPU
CHANNEL "A" LOWER 64 BITS



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Title: MEM_A0 DIMM1(0..63)

Size	Document Number	Rev
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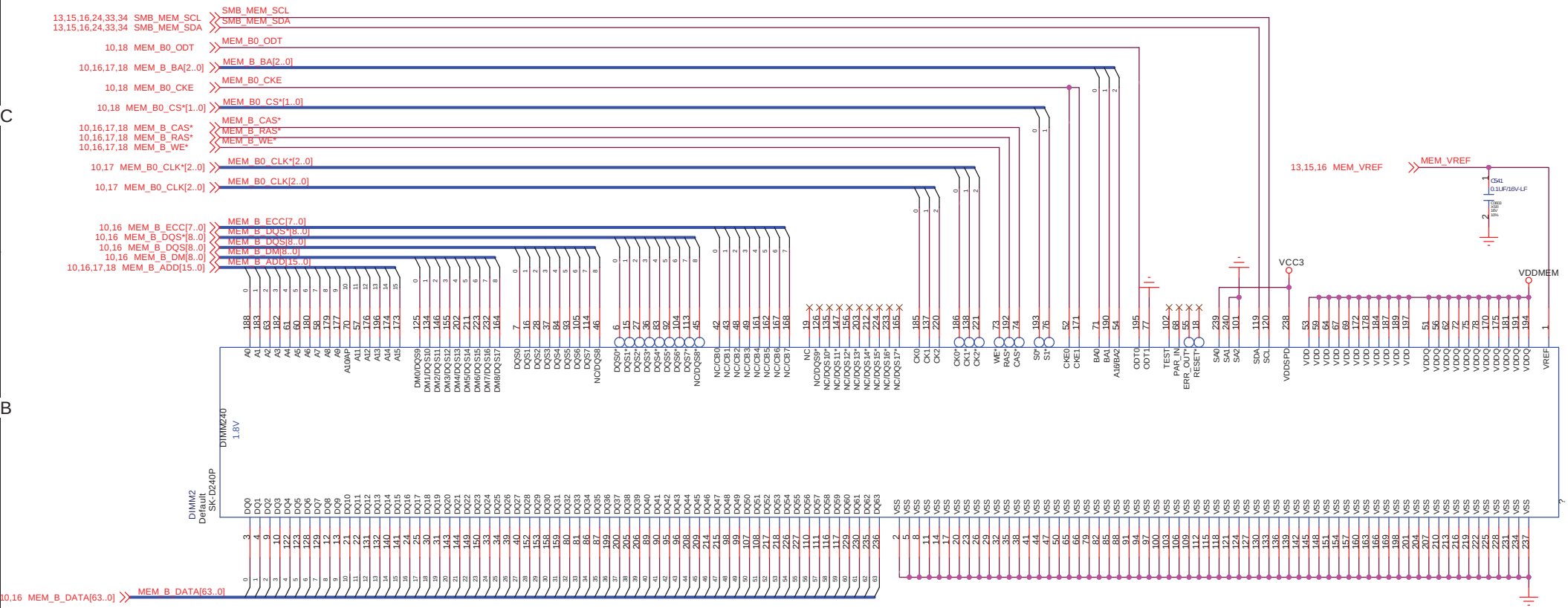
DIMM 2

CHANNEL "B" UPPER 64 BITS



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Title: MEM_B0 DIMM2(64..127)

Size	Document Number	Rev
A3	KN9 SLI	0.1

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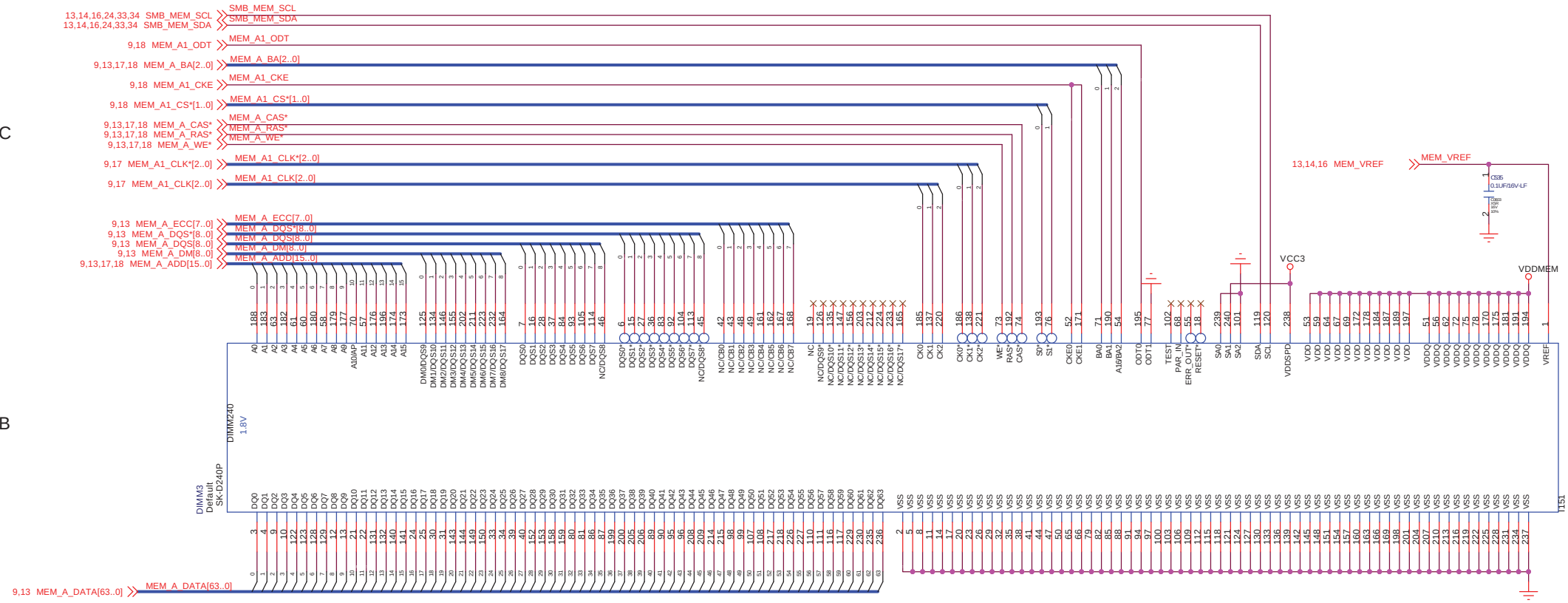
DIMM 3

CHANNEL "A" LOWER 64 BITS



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Title: MEM_A1 DIMM3(0..63)

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A3	KN9 SLI	0.1

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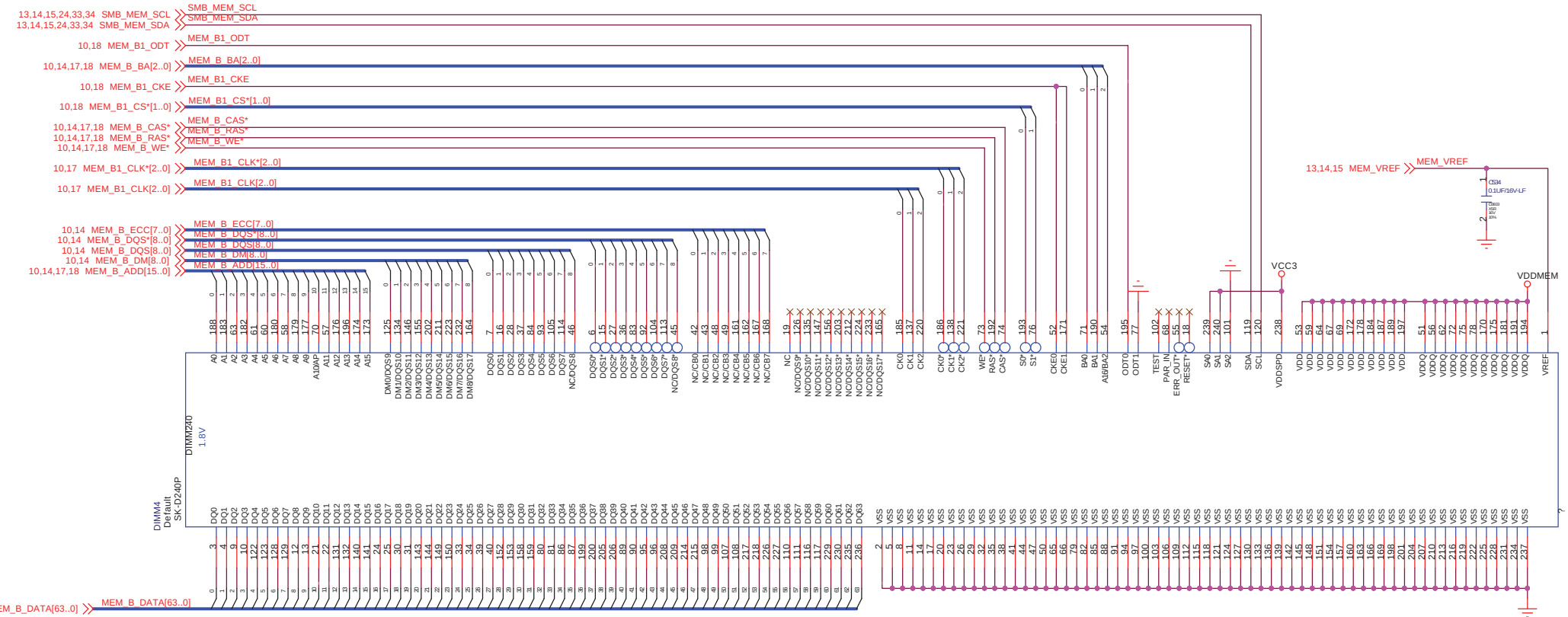
DIMM 4

CHANNEL "B" UPPER 64 BITS
FURTHEST DIMM TO CPU



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Title: MEM_B1 DIMM4(64..127)

Size	Document Number	Rev
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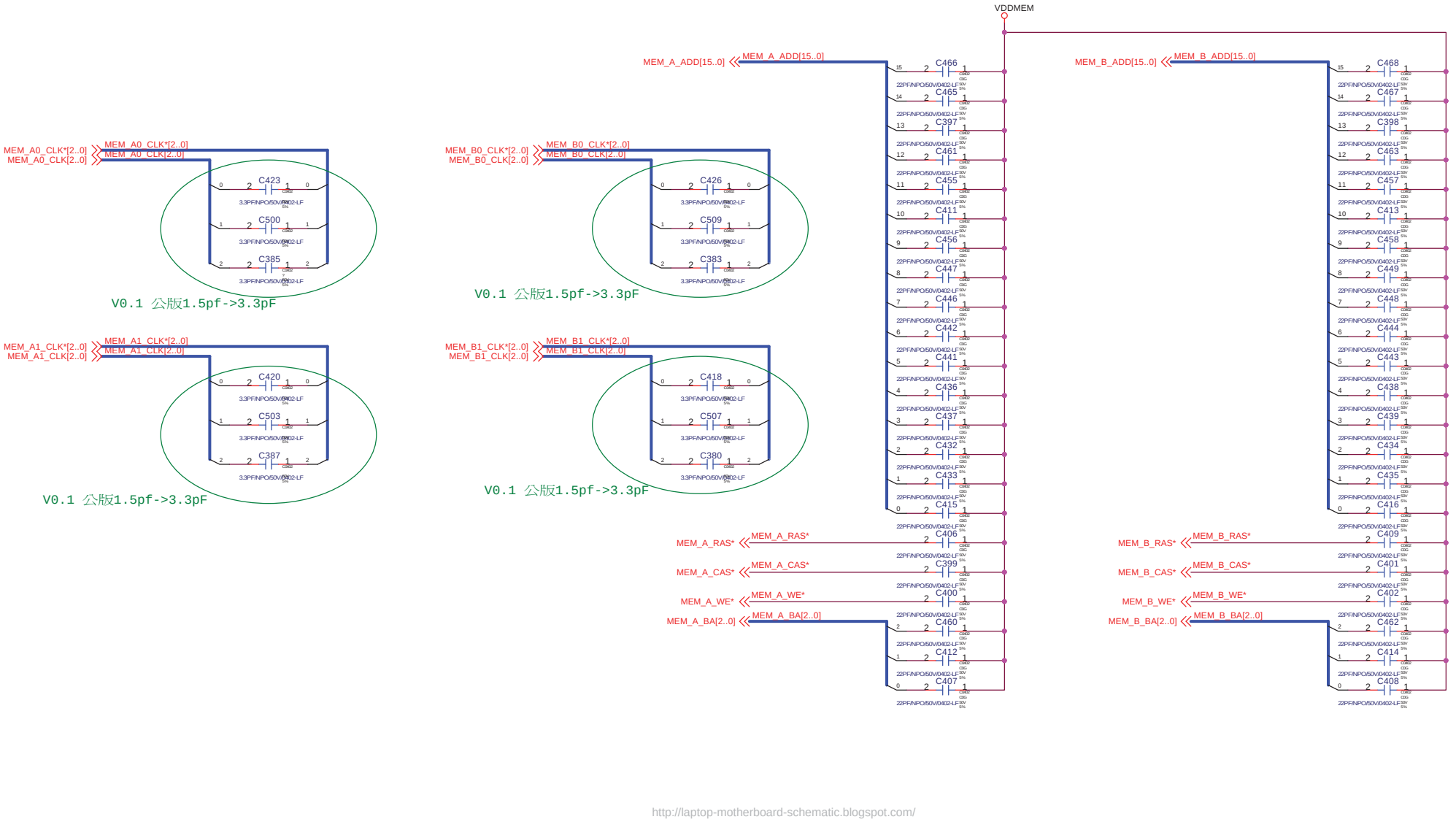
PLACE ALL PARTS BETWEEN CPU AND DIMM



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Title: MEM ADD/CTL CTT TERMINATION

Size	Document Number	Rev
A3	KN9 SLI	0.1

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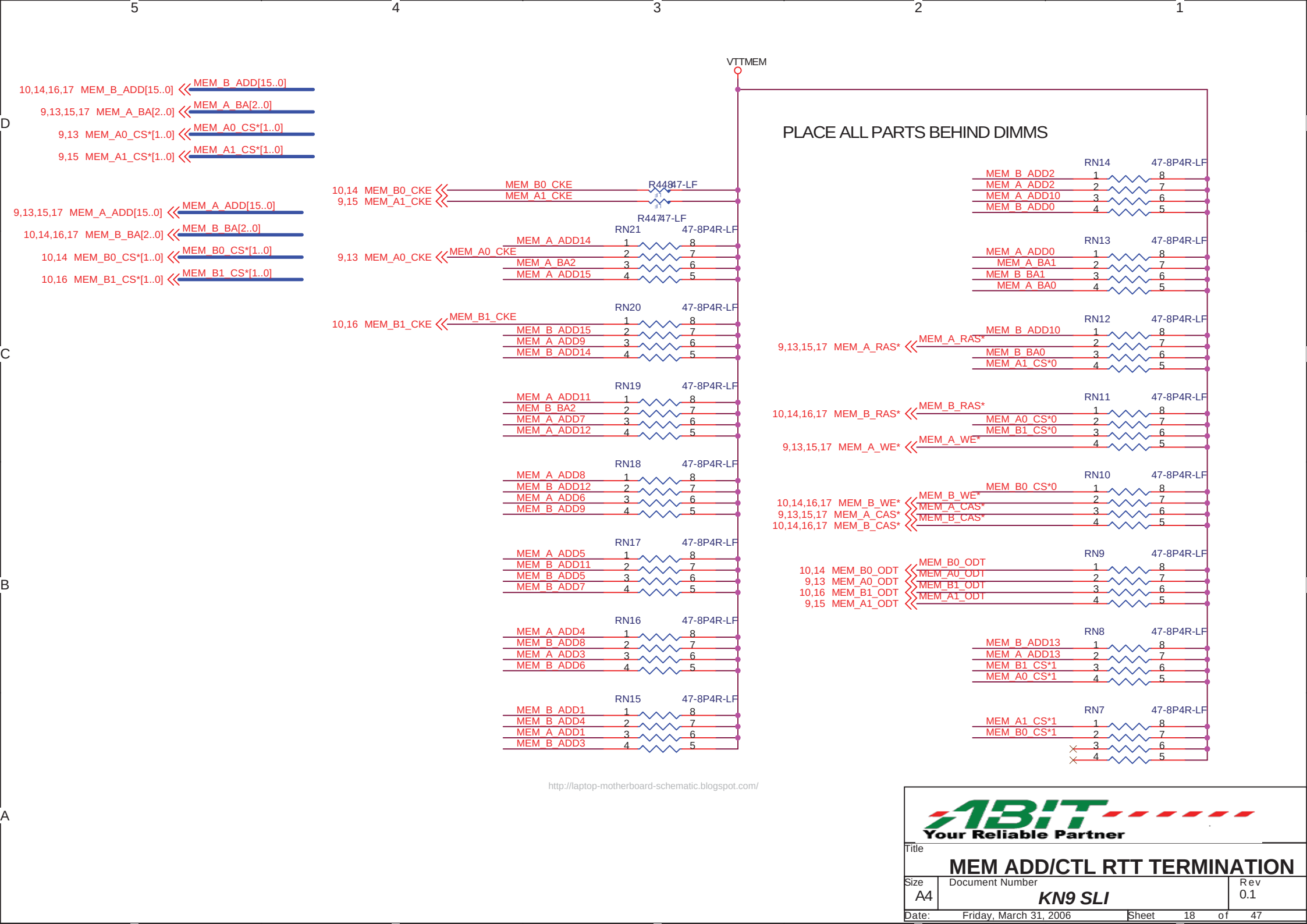
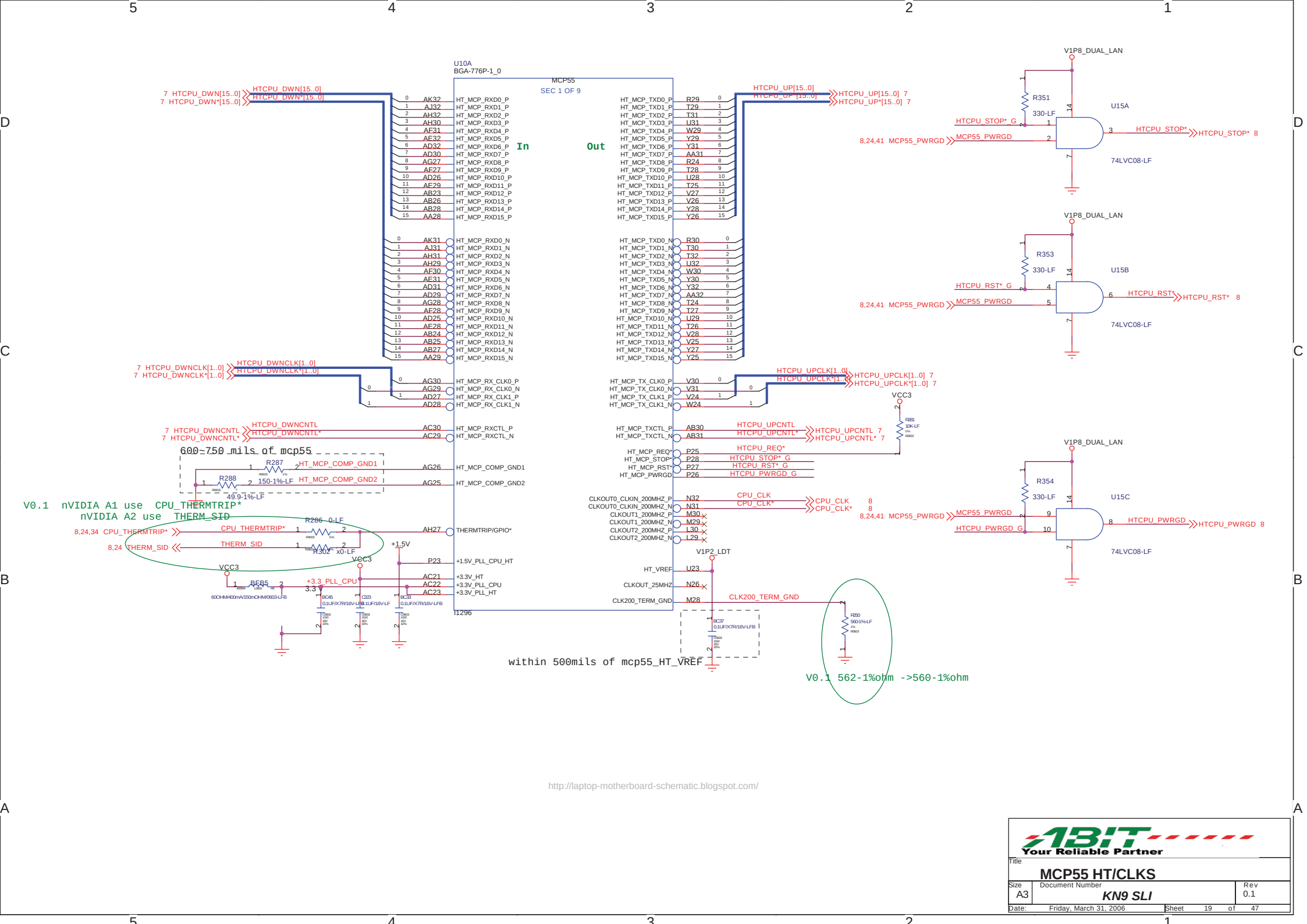
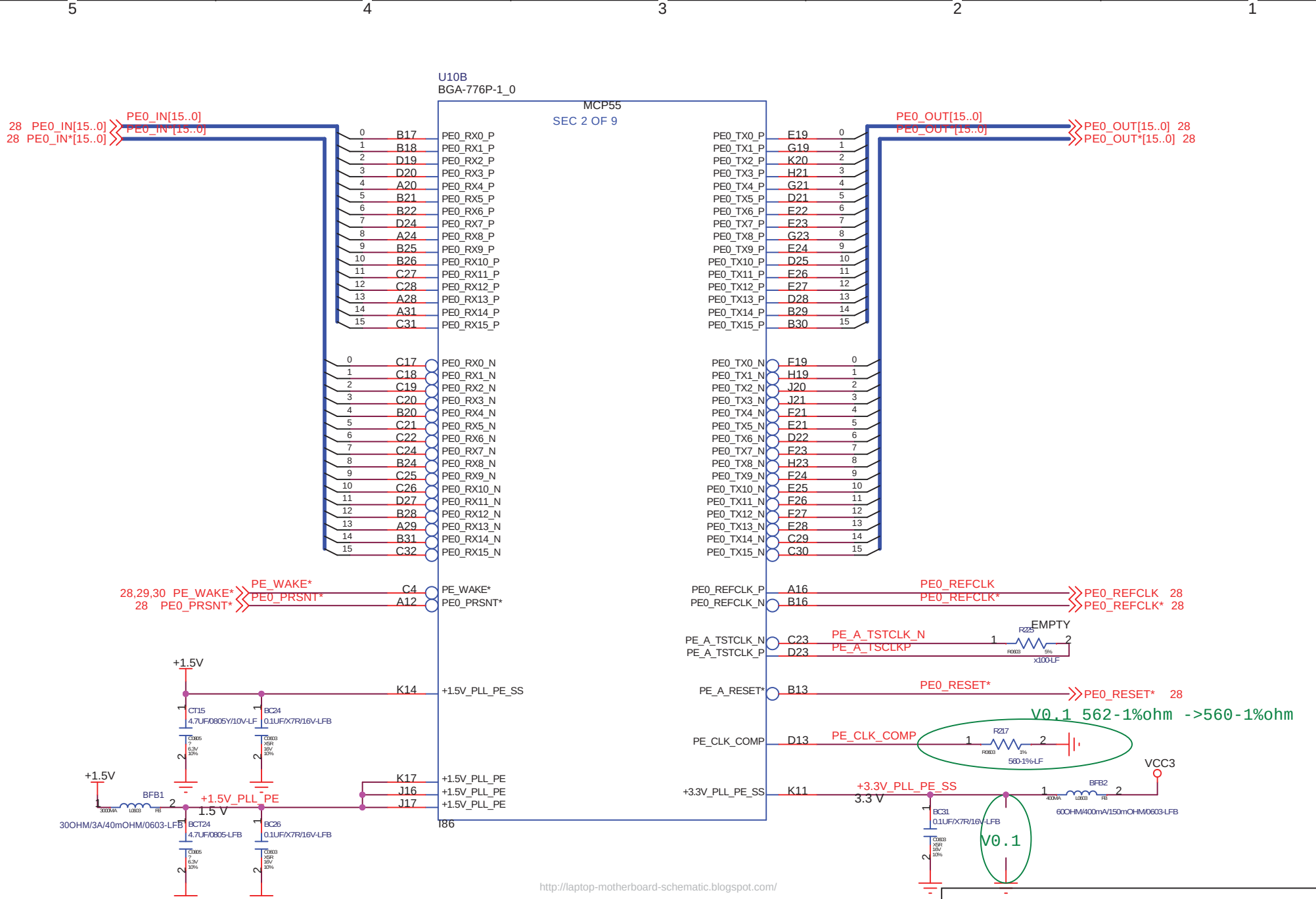

5
4
3
2
1
D
C
B
A
VTTMEM
PLACE ALL PARTS BEHIND DIMMS
10,14,16,17 MEM_B_ADD[15..0]
9,13,15,17 MEM_A_BA[2..0]
9,13 MEM_A0_CS*[1..0]
9,15 MEM_A1_CS*[1..0]
9,13,15,17 MEM_A_ADD[15..0]
10,14,16,17 MEM_B_BA[2..0]
10,14 MEM_B0_CS*[1..0]
10,16 MEM_B1_CS*[1..0]
MEM_B_ADD[15..0]
MEM_A_BA[2..0]
MEM_A0_CS*[1..0]
MEM_A1_CS*[1..0]
MEM_A_ADD[15..0]
MEM_B_BA[2..0]
MEM_B0_CS*[1..0]
MEM_B1_CS*[1..0]
10,14 MEM_B0_CKE
9,15 MEM_A1_CKE
MEM_B0_CKE
MEM_A1_CKE
R448 47-LF
R447 47-LF
RN21 47-8P4R-LF
9,13 MEM_A0_CKE
MEM_A0_CKE
MEM_A_ADD14
MEM_A_BA2
MEM_A_ADD15
RN20 47-8P4R-LF
10,16 MEM_B1_CKE
MEM_B1_CKE
MEM_B_ADD15
MEM_A_ADD9
MEM_B_ADD14
RN19 47-8P4R-LF
MEM_A_ADD11
MEM_B_BA2
MEM_A_ADD7
MEM_A_ADD12
RN18 47-8P4R-LF
MEM_A_ADD8
MEM_B_ADD12
MEM_A_ADD6
MEM_B_ADD9
RN17 47-8P4R-LF
MEM_A_ADD5
MEM_B_ADD11
MEM_B_ADD5
MEM_B_ADD7
RN16 47-8P4R-LF
MEM_A_ADD4
MEM_B_ADD8
MEM_A_ADD3
MEM_B_ADD6
RN15 47-8P4R-LF
MEM_B_ADD1
MEM_B_ADD4
MEM_A_ADD1
MEM_B_ADD3
RN14 47-8P4R-LF
MEM_B_ADD2
MEM_A_ADD2
MEM_A_ADD10
MEM_B_ADD0
RN13 47-8P4R-LF
MEM_A_ADD0
MEM_A_BA1
MEM_B_BA1
MEM_A_BA0
RN12 47-8P4R-LF
9,13,15,17 MEM_A_RAS*
MEM_A_RAS*
MEM_B_ADD10
MEM_B_BA0
MEM_A1_CS*0
RN11 47-8P4R-LF
10,14,16,17 MEM_B_RAS*
9,13,15,17 MEM_A_WE*
MEM_B_RAS*
MEM_A0_CS*0
MEM_B1_CS*0
MEM_A_WE*
RN10 47-8P4R-LF
10,14,16,17 MEM_B_WE*
9,13,15,17 MEM_A_CAS*
10,14,16,17 MEM_B_CAS*
MEM_B0_CS*0
MEM_B_WE*
MEM_A_CAS*
MEM_B_CAS*
RN9 47-8P4R-LF
10,14 MEM_B0_ODT
9,13 MEM_A0_ODT
10,16 MEM_B1_ODT
9,15 MEM_A1_ODT
MEM_B0_ODT
MEM_A0_ODT
MEM_B1_ODT
MEM_A1_ODT
RN8 47-8P4R-LF
MEM_B_ADD13
MEM_A_ADD13
MEM_B1_CS*1
MEM_A0_CS*1
RN7 47-8P4R-LF
MEM_A1_CS*1
MEM_B0_CS*1
http://laptop-motherboard-schematic.blogspot.com/
ABIT
Your Reliable Partner
Title
MEM ADD/CTL RTT TERMINATION
Size
A4
Document Number
KN9 SLI
Rev
0.1
Date: Friday, March 31, 2006
Sheet 18 of 47

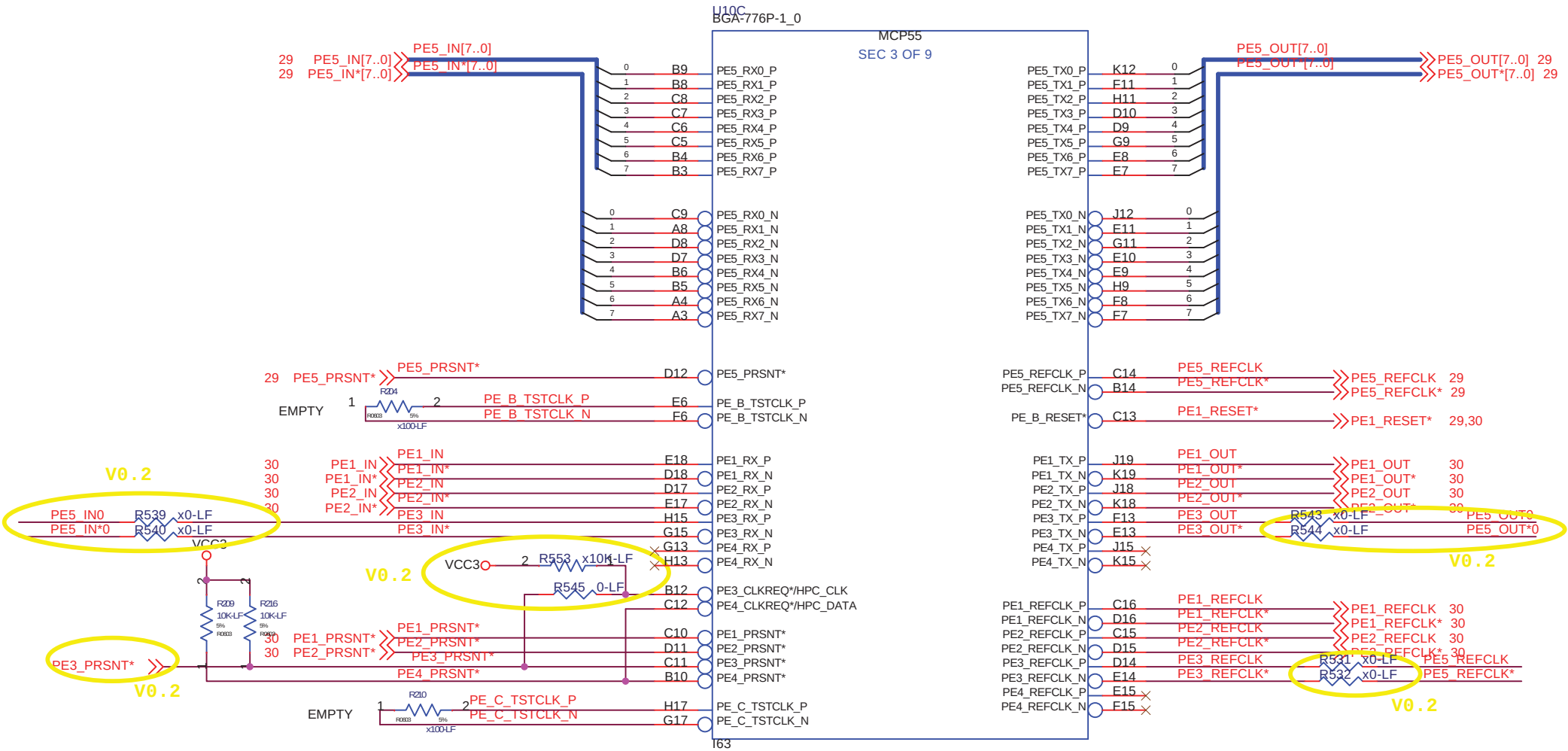


Title	MCP55 HT/CLKS
Size	A3
Document Number	KN9 SLI
Rev	0.1
Date:	Friday, March 31, 2006
Sheet	19 of 47



Your Reliable Partner

Title	MCP55 PEX X16	
Size: A4	Document Number: *KN9 SLI*	Rev: 0.1
Date: Friday, March 31, 2006	Sheet 20 of 47	



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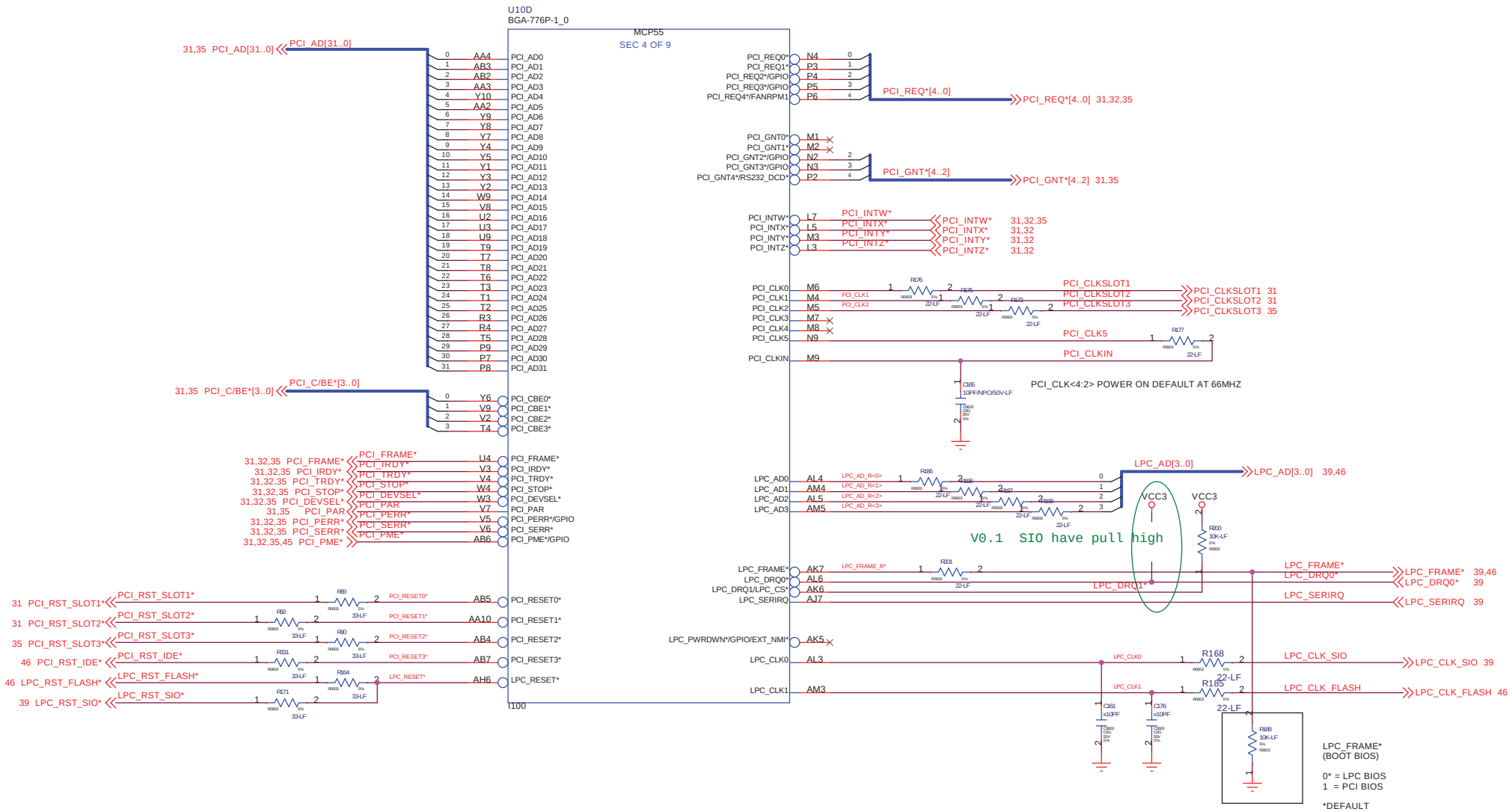
Title: MCP55 PEX X8 & X1'S

Size	Document Number	Rev
A4	KN9 SLI	0.1

Date: Friday, March 31, 2006 Sheet 21 of 47


U10D
BGA-776P-1_0
MCP55
SEC 4 OF 9
PCI_AD[31..0]
PCI_C/BE*[3..0]
PCI_REQ*[4..0]
PCI_GNT*[4..2]
PCI_CLKSLOT1
PCI_CLKSLOT2
PCI_CLKSLOT3
PCI_CLKIN
PCI_CLK5
PCI_CLK<4:2> POWER ON DEFAULT AT 66MHZ
LPC_AD[3..0]
V0.1 SIO have pull high
LPC_FRAME*
LPC_DRQ0*
LPC_SERIRQ
LPC_CLK_SIO
LPC_CLK_FLASH
LPC_FRAME*
(BOOT BIOS)
0* = LPC BIOS
1 = PCI BIOS
*DEFAULT
PCI_RST_SLOT1*
PCI_RST_SLOT2*
PCI_RST_SLOT3*
PCI_RST_IDE*
LPC_RST_FLASH*
LPC_RST_SIO*
http://laptop-motherboard-schematic.blogspot.com/
Your Reliable Partner
MCP55 PCI
KN9 SLI
A3
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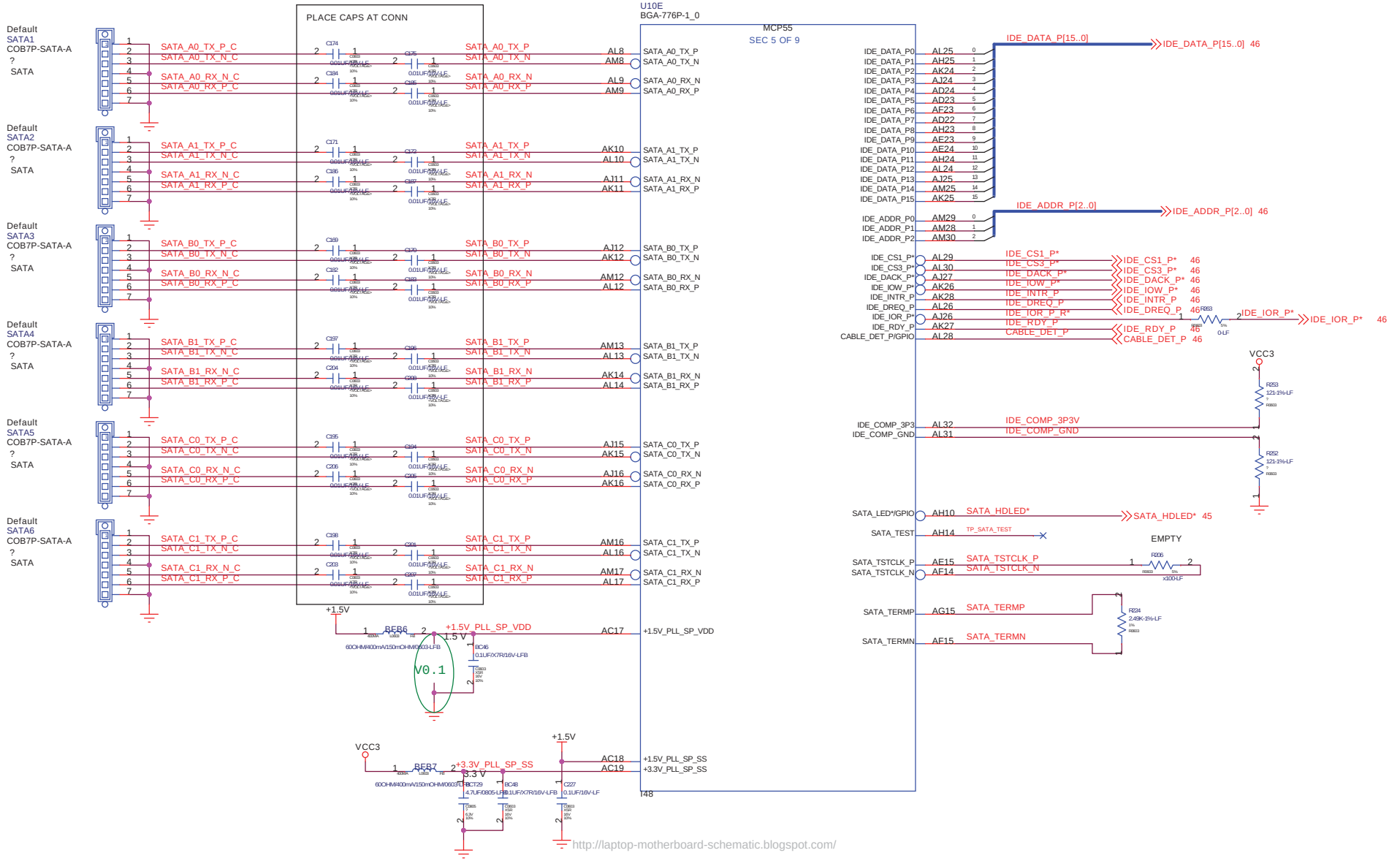
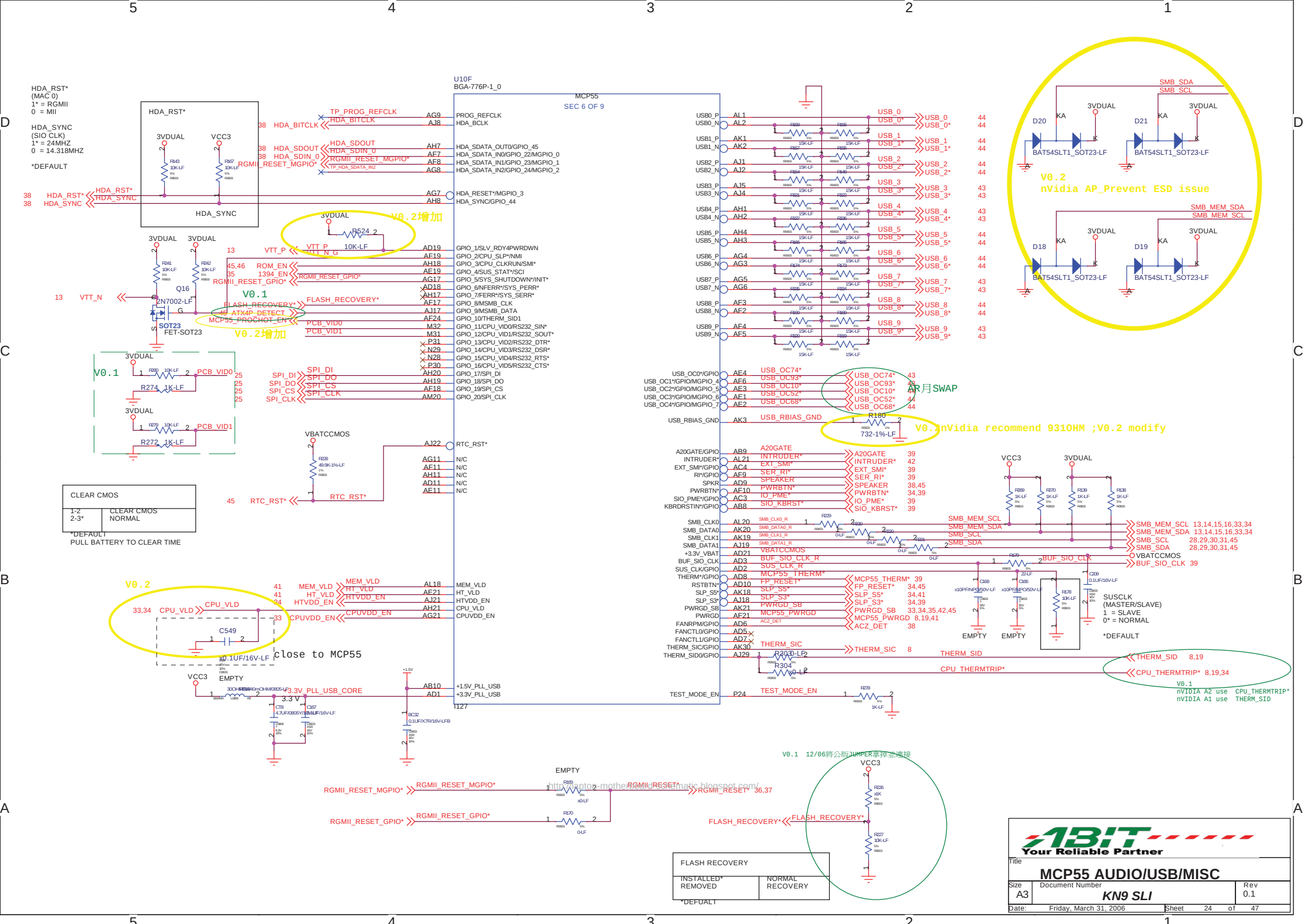
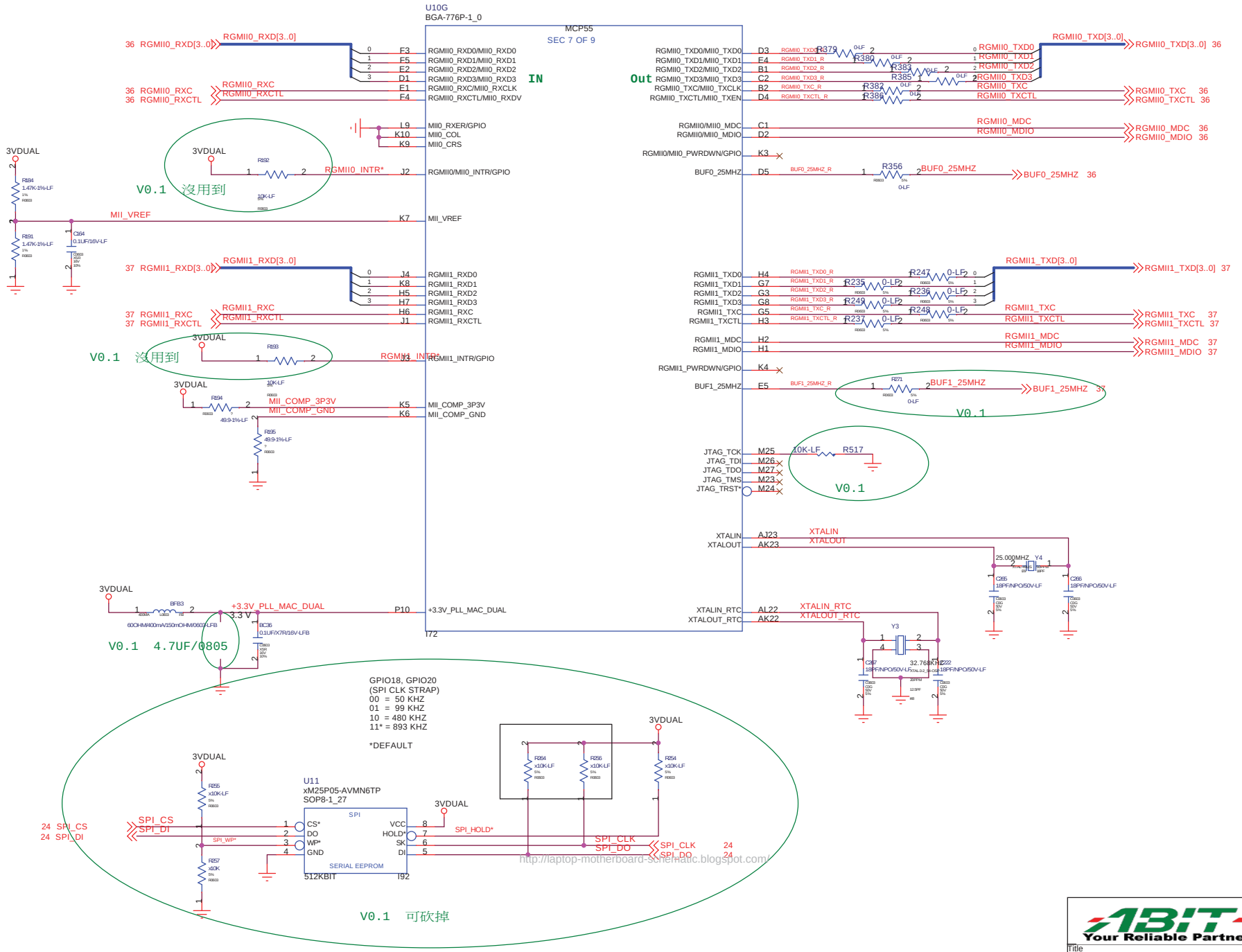
47



Title	MCP55 SATA & IDE	
Size: A3	Document Number: KN9 SLI	Rev: 0.1
Date: Friday, March 31, 2006	Sheet 23 of 47	


HDA_RST*
(MAC 0)
1* = RGMII
0 = MII
HDA_SYNC
(SIO CLK)
1* = 24MHZ
0 = 14.318MHZ
*DEFAULT
U10F
BGA-776P-1_0
MCP55
SEC 6 OF 9
V0.2增加
V0.1
V0.2
nVidia AP_Prevent ESD issue
AR月SWAP
V0.3nVidia recommend 931OHM ;V0.2 modify
CLEAR CMOS
1-2 CLEAR CMOS
2-3* NORMAL
*DEFAULT
PULL BATTERY TO CLEAR TIME
close to MCP55
SUSCLK
(MASTER/SLAVE)
1 = SLAVE
0* = NORMAL
*DEFAULT
V0.1 12/06將公版JUMPER拿掉並連接
FLASH RECOVERY
INSTALLED*
REMOVED
NORMAL
RECOVERY
*DEFAULT
http://laptop-motherboard-schematic.blogspot.com/
ABIT
Your Reliable Partner
MCP55 AUDIO/USB/MISC
KN9 SLI
Friday, March 31, 2006



Title	MCP55 DUAL RGMII
Size	A3
Document Number	KN9 SLI
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Date:	Friday, March 31, 2006
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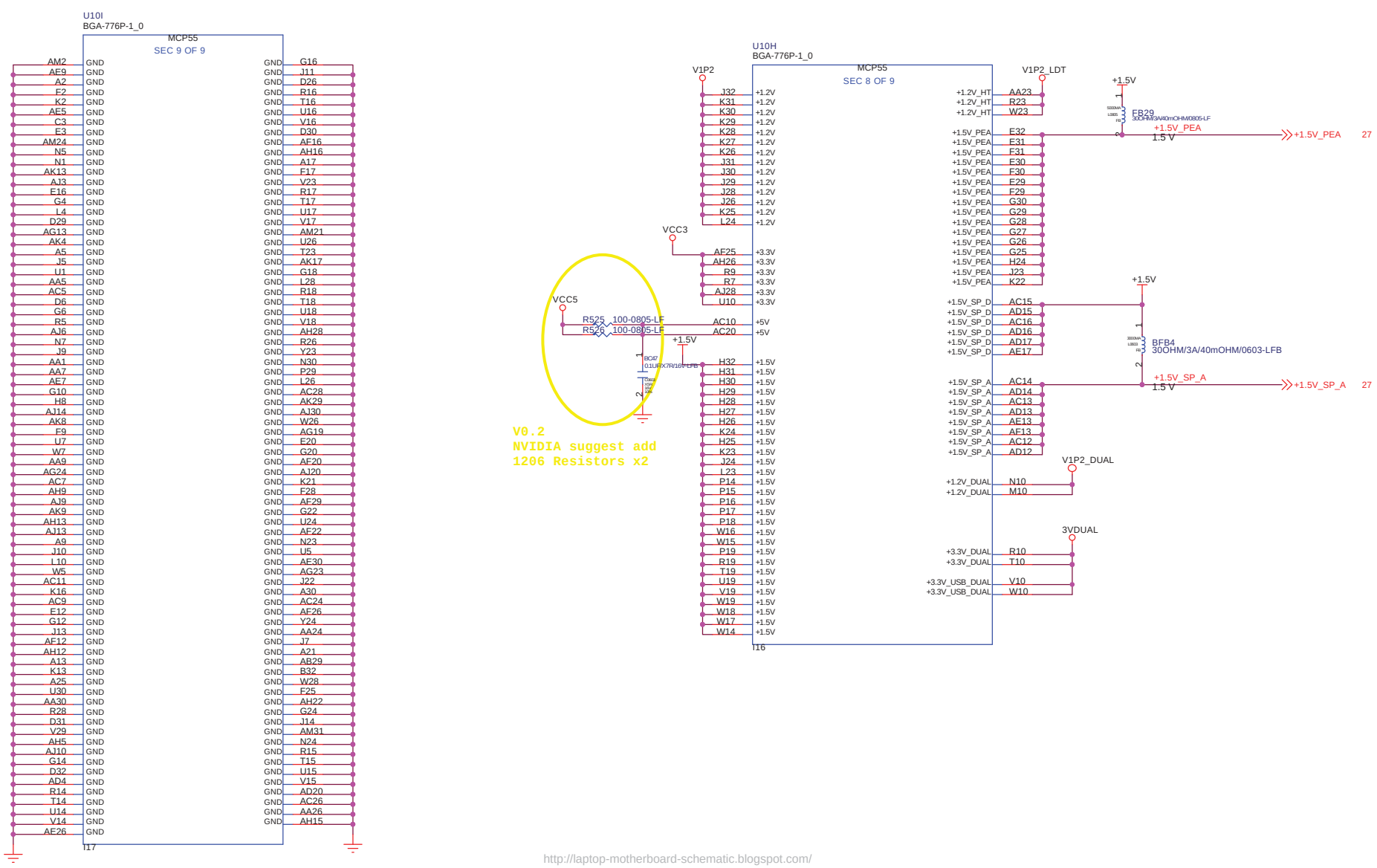

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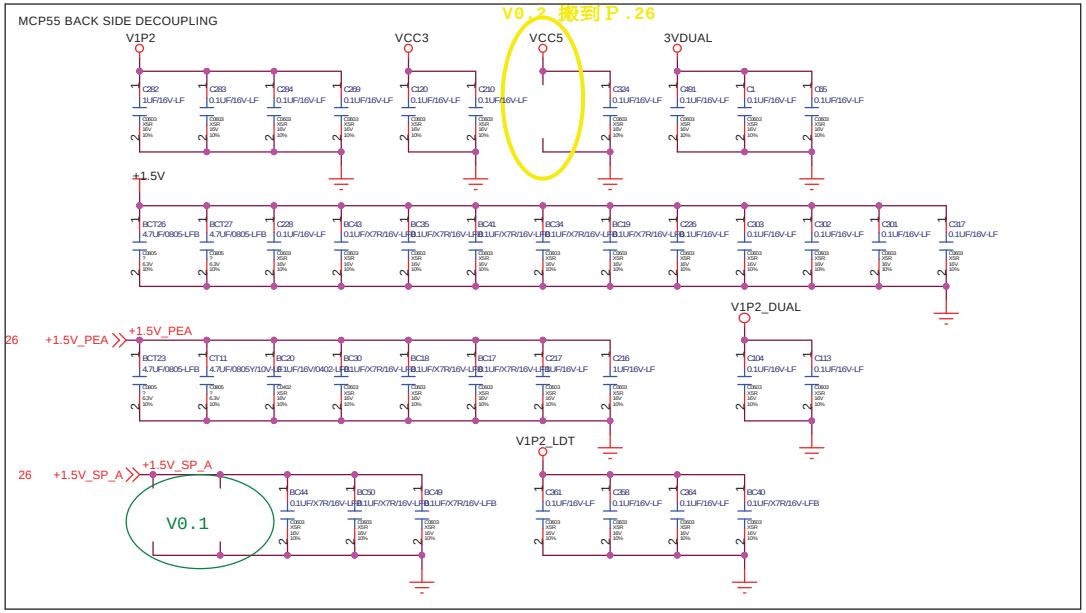
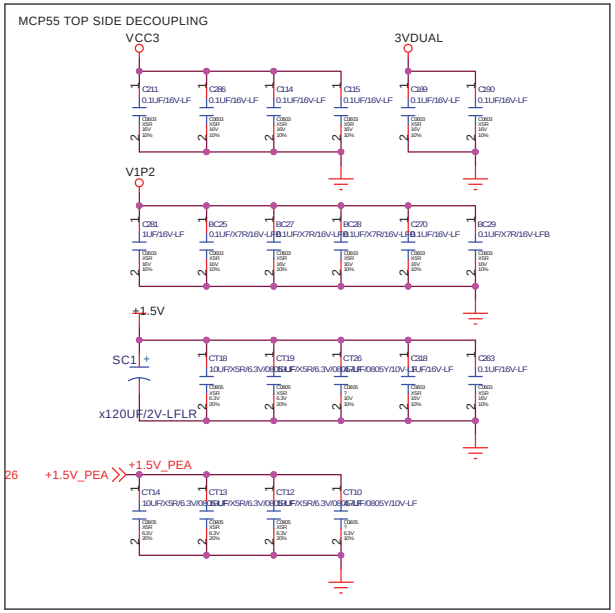
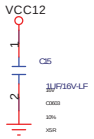
Title	MCP55 PWR/GND	
Size: A3	Document Number: KN9 SLI	Rev: 0.1
Date: Friday, March 31, 2006	Sheet 26 of 47	





MCP55 INTERNAL PULL-UP/PULL-DOWN	
PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V



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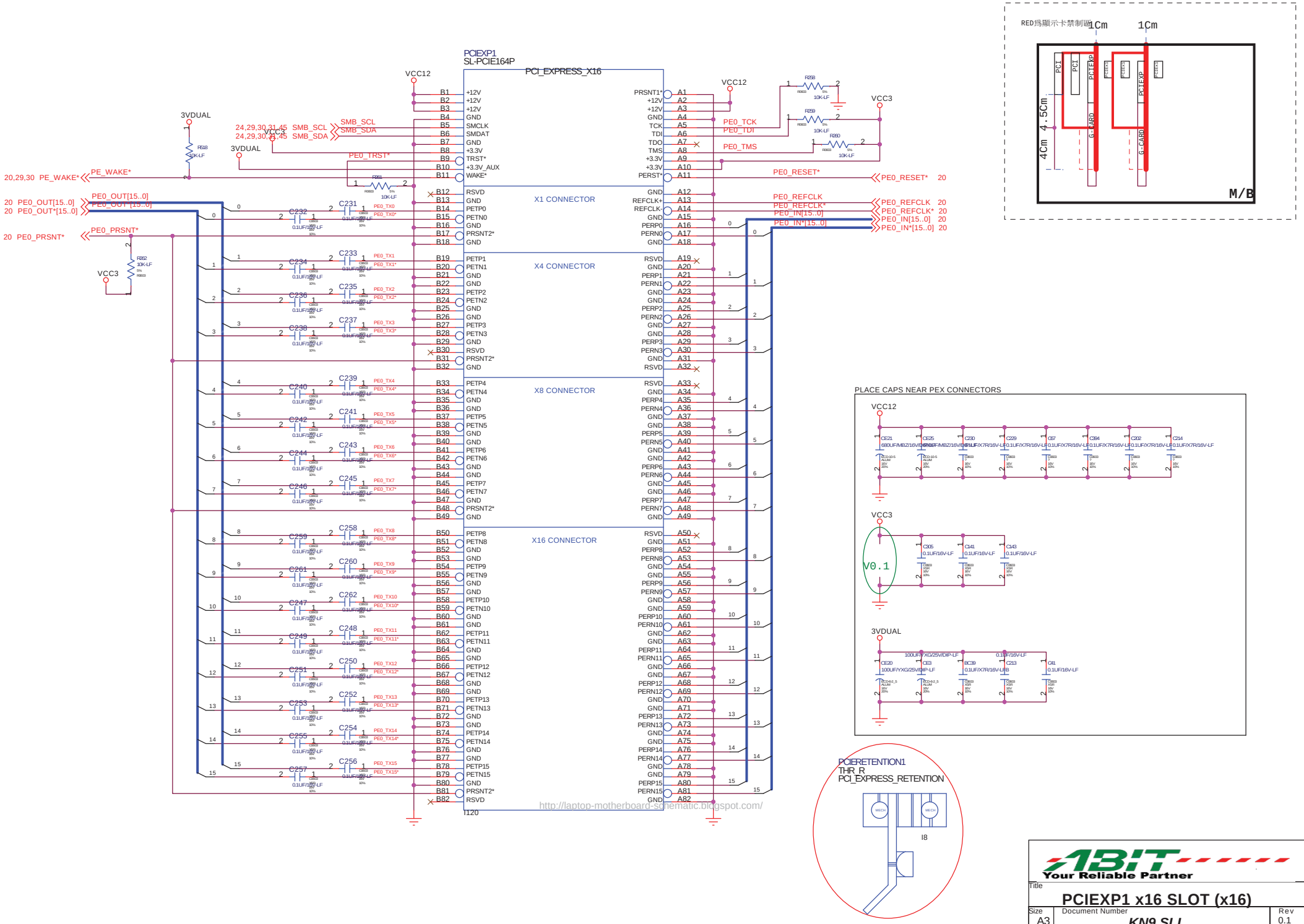
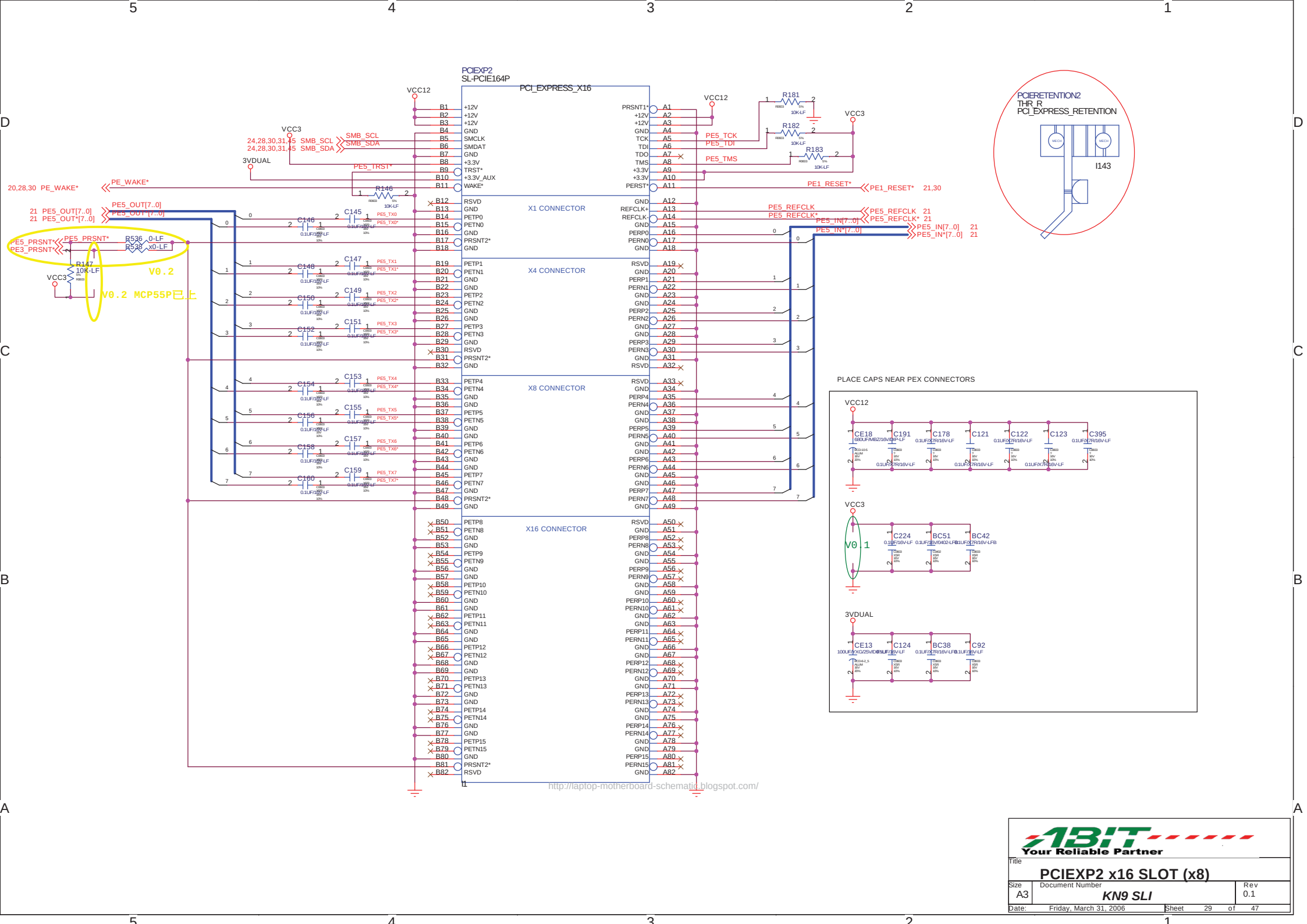
Title: MCP55 DECOUPLING

Size	Document Number	Rev
A3	KN9 SLI	0.1

Date: Friday, March 31, 2006 Sheet 27 of 47


PCIEXP1
SL-PCIE164P
PCI_EXPRESS_X16
X1 CONNECTOR
X4 CONNECTOR
X8 CONNECTOR
X16 CONNECTOR
VCC12
VCC3
3VDUAL
PE_WAKE*
PE0_OUT[15..0]
PE0_OUT*[15..0]
PE0_PRSNT*
PE0_TRST*
PE0_TCK
PE0_TDI
PE0_TMS
PE0_RESET*
PE0_REFCLK
PE0_REFCLK*
PE0_IN[15..0]
PE0_IN*[15..0]
SMB_SCL
SMB_SDA
RED為顯示卡禁制區
1Cm
4.5Cm
M/B
PLACE CAPS NEAR PEX CONNECTORS
V0.1
PCIERETENTION1
THR_R
PCI_EXPRESS_RETENTION
I8
I120
http://laptop-motherboard-schematic.blogspot.com/
ABIT
Your Reliable Partner
PCIEXP1 x16 SLOT (x16)
KN9 SLI
Friday, March 31, 2006



Title	PCIEXP2 x16 SLOT (x8)
Size	A3
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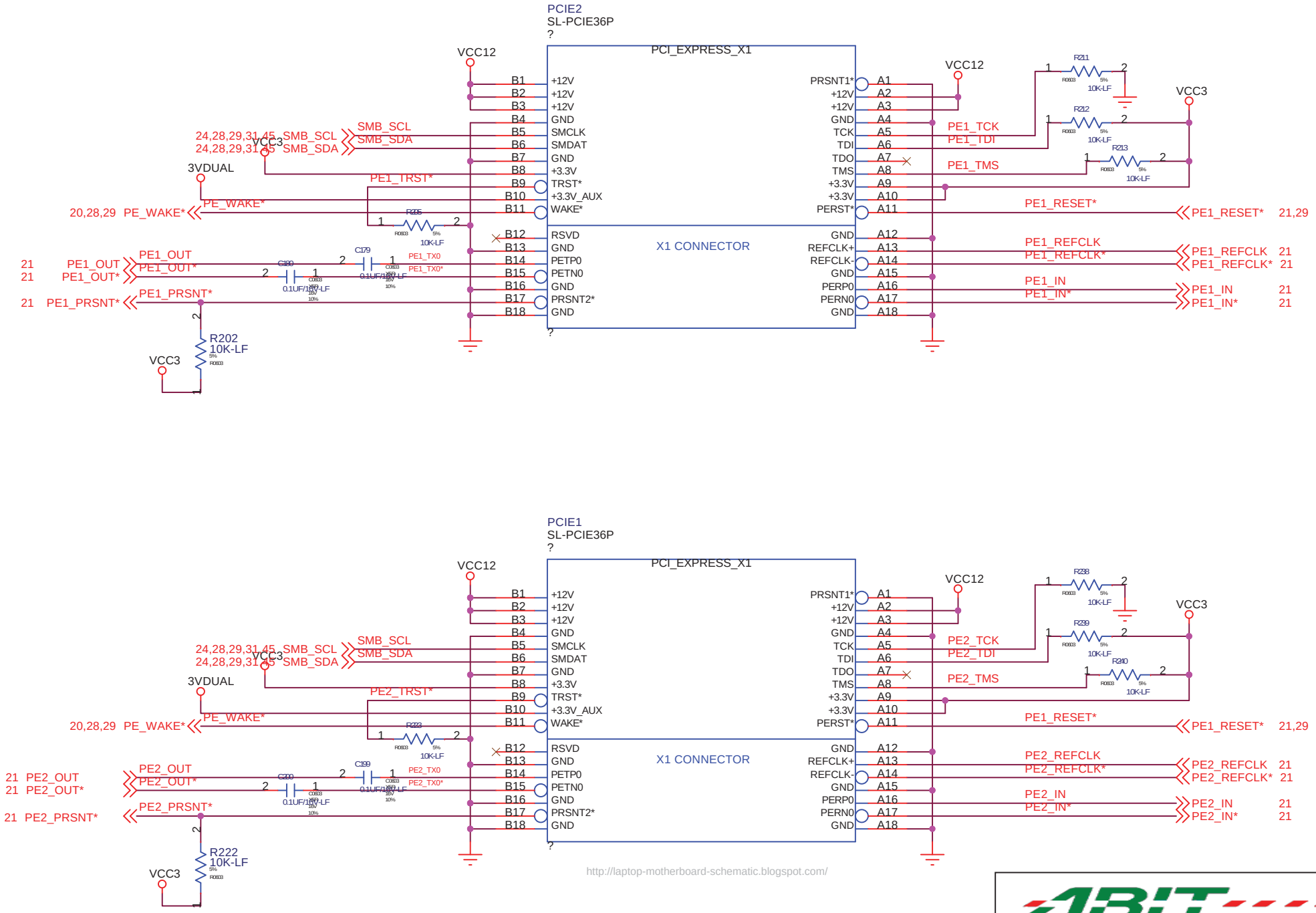

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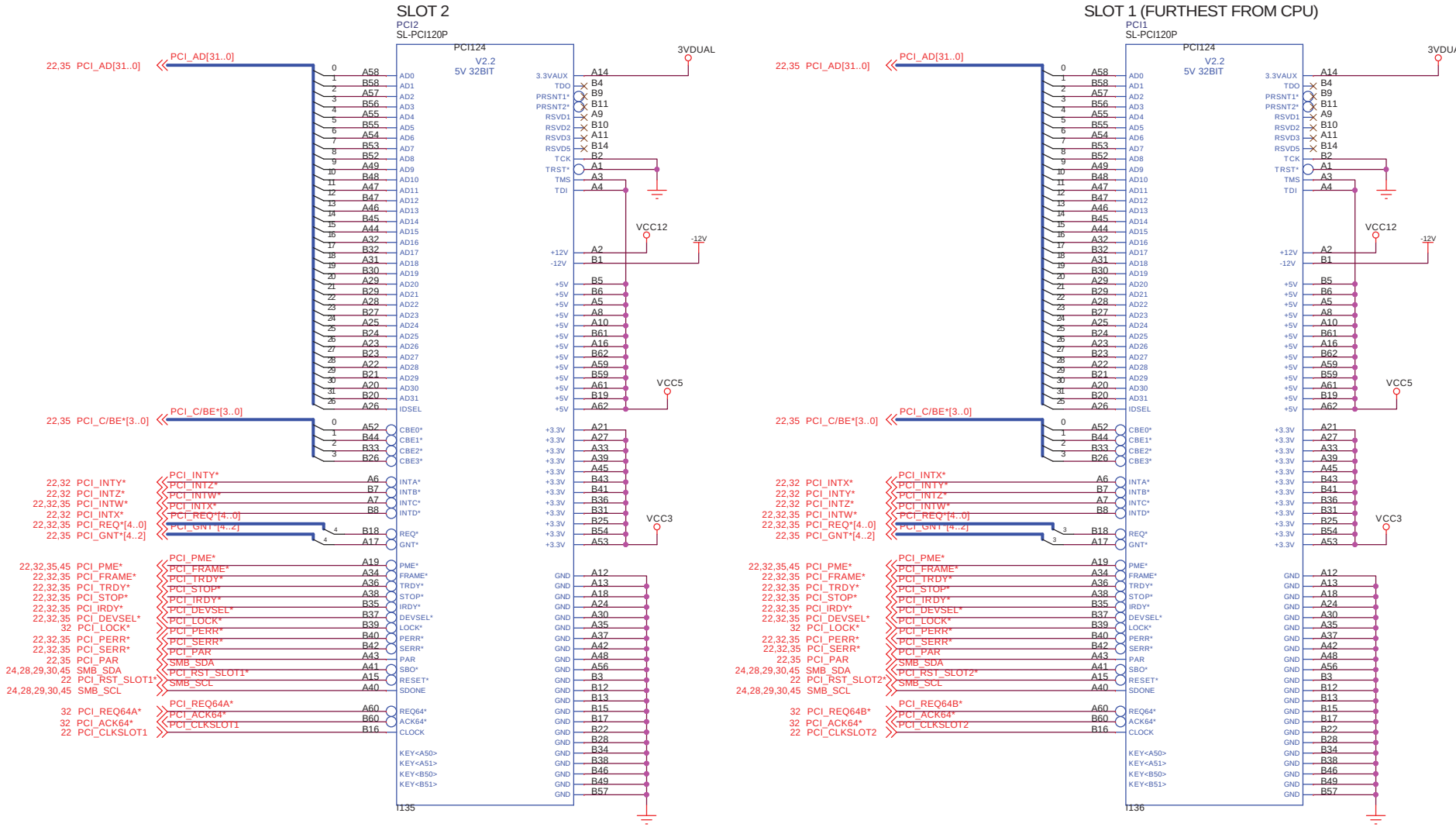
Title: PCIE 1 & 2 SLOT (x1)

Size	Document Number	Rev
A4	KN9 SLI	0.1

Date: Friday, March 31, 2006 Sheet 30 of 47



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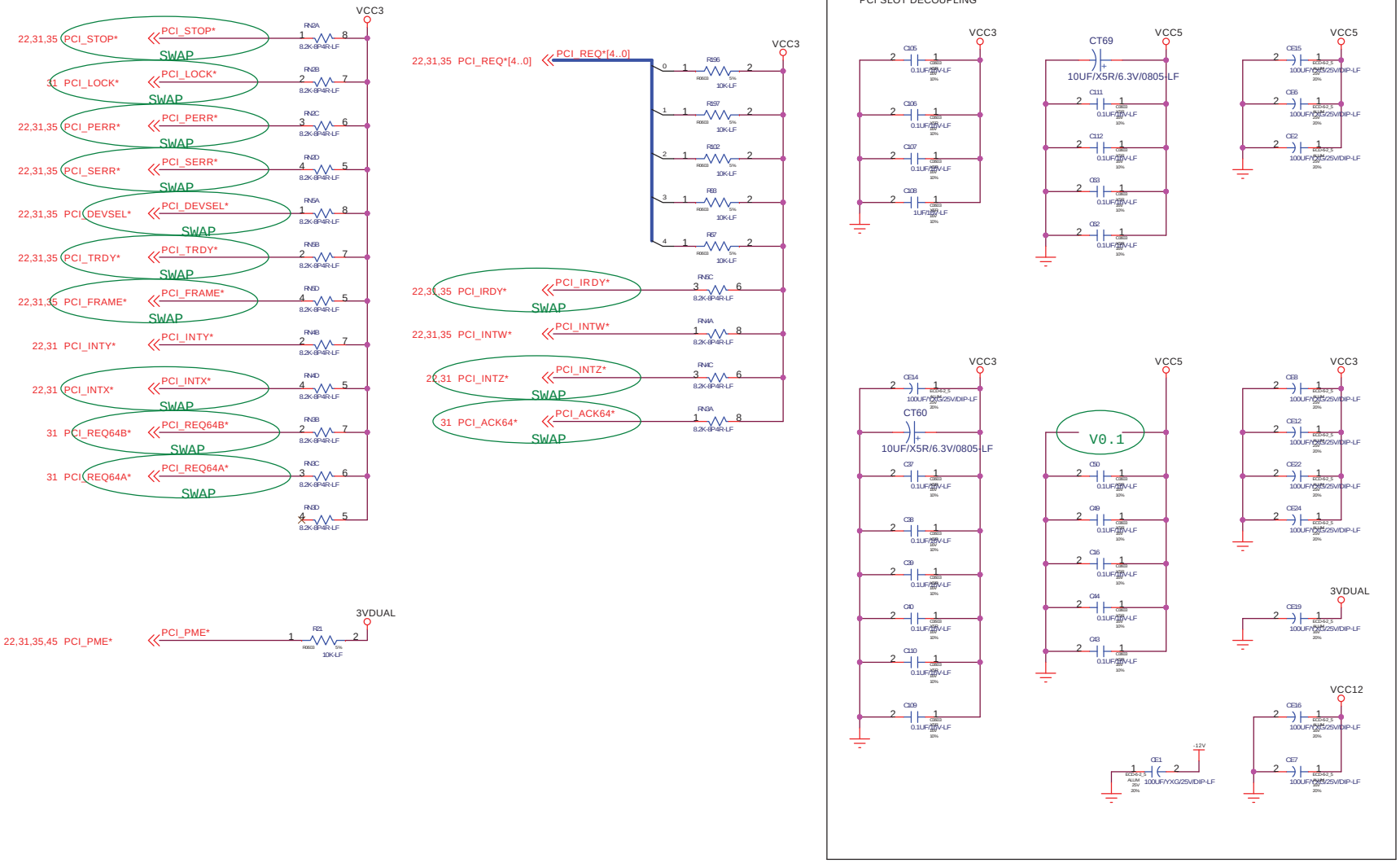
Title: PCI 1 & 2 SLOT

Size	Document Number	Rev
A3	KN9 SLI	0.1

Date: Friday, March 31, 2006 Sheet 31 of 47



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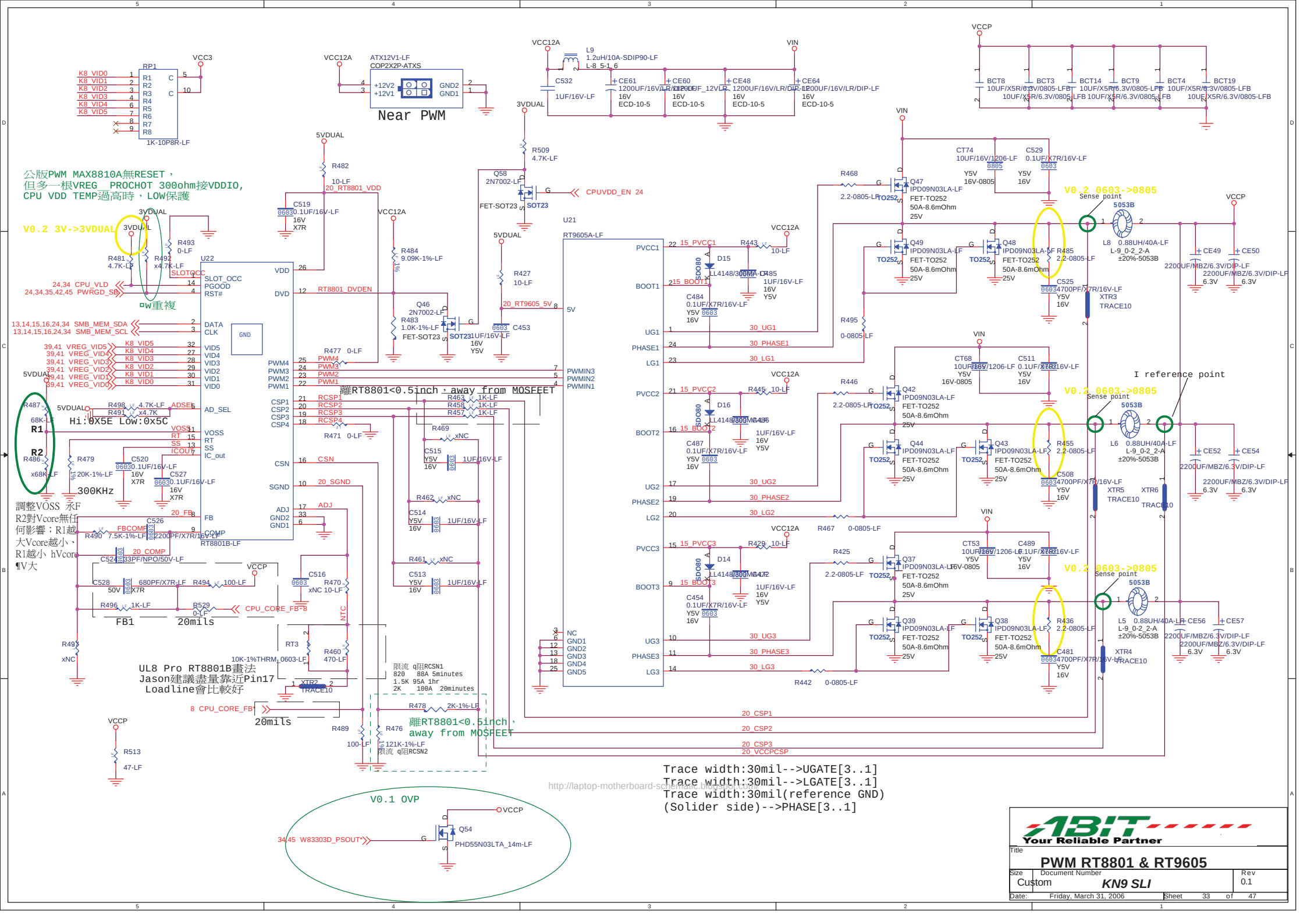
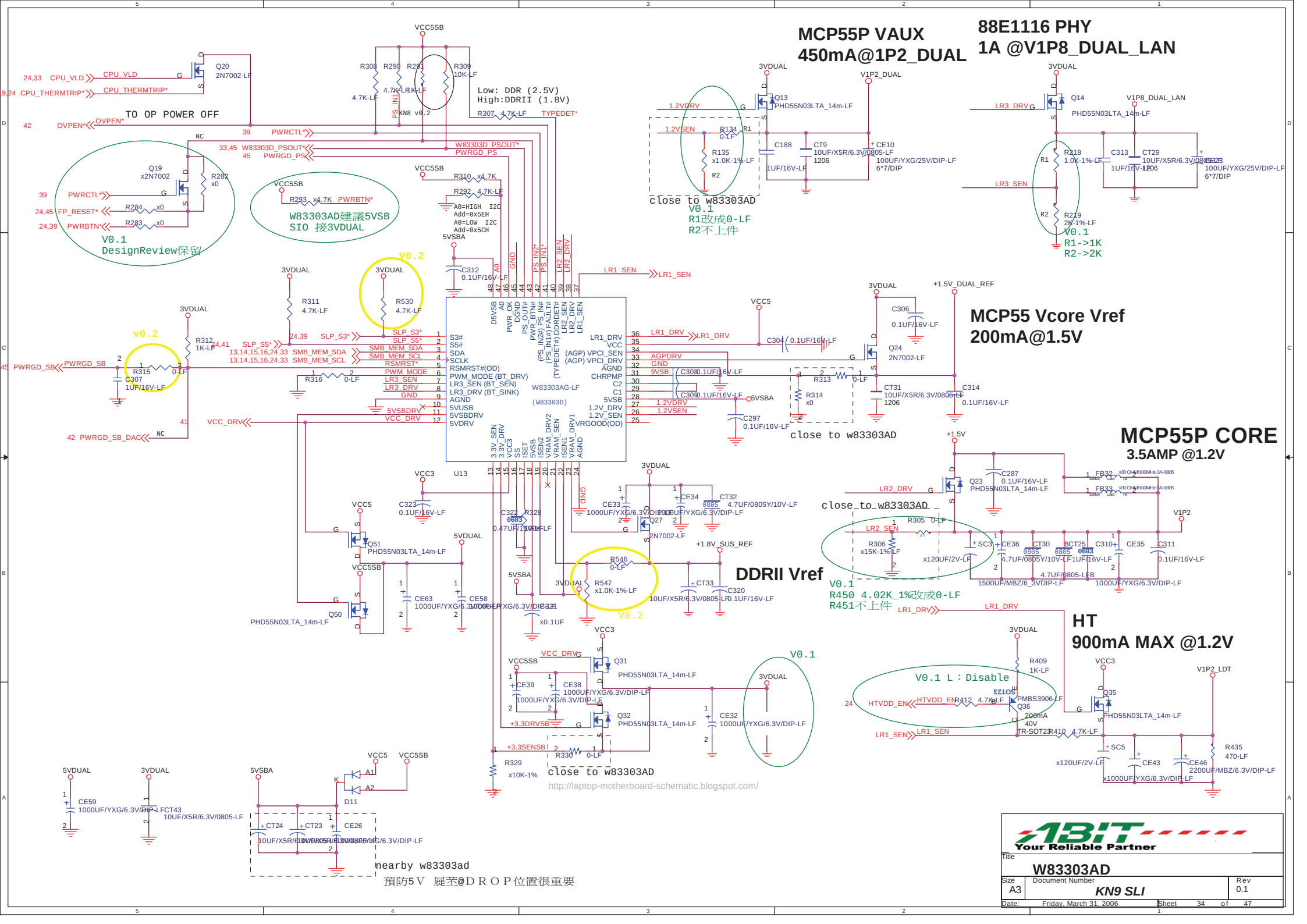
Title: PCI TERM/DECOUPLING

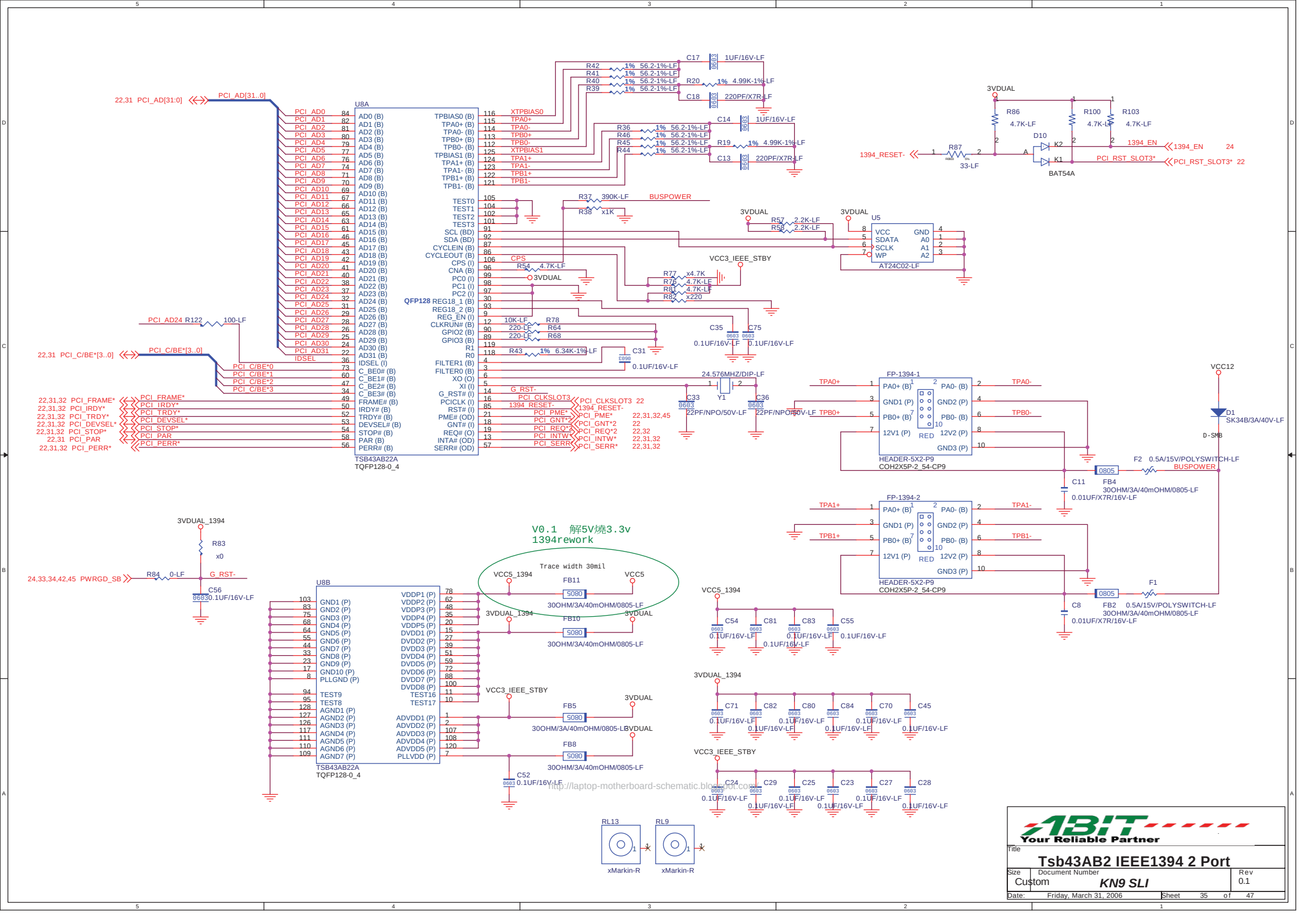
Size	Document Number	Rev
A3	KN9 SLI	0.1

Date: Friday, March 31, 2006 Sheet 32 of 47



Title	PWM RT8801 & RT9605
Size	Custom
Document Number	KN9 SLI
Rev	0.1
Date:	Friday, March 31, 2006
Sheet	33 of 47


MCP55P VAUX
450mA@1P2_DUAL
88E1116 PHY
1A @V1P8_DUAL_LAN
MCP55 Vcore Vref
200mA@1.5V
MCP55P CORE
3.5AMP @1.2V
DDRII Vref
HT
900mA MAX @1.2V
TO OP POWER OFF
Low: DDR (2.5V)
High:DDRII (1.8V)
W83303AD建議5VSB
SIO 接3VDUAL
V0.1
DesignReview保留
V0.2
close to w83303AD
V0.1
R1改成0-LF
R2不上件
V0.1
R1->1K
R2->2K
V0.1
R450 4.02K_1%改成0-LF
R451不上件
V0.1 L : Disable
nearby w83303ad
預防5V 屣茎@D R O P位置很重要
http://laptop-motherboard-schematic.blogspot.com/
W83303AD
KN9 SLI
Your Reliable Partner
Friday, March 31, 2006
Sheet 34 of 47


U8A
TSB43AB22A
TQFP128-0_4
U8B
TSB43AB22A
TQFP128-0_4
V0.1 解5V燒3.3v
1394rework
Trace width 30mil
U5
AT24C02-LF
FP-1394-1
FP-1394-2
HEADER-5X2-P9
COH2X5P-2_54-CP9
BAT54A
D-SMB
SK34B/3A/40V-LF
24.576MHZ/DIP-LF
xMarkin-R
xMarkin-R
http://laptop-motherboard-schematic.blogspot.com/
ABIT
Your Reliable Partner
Title
Tsb43AB2 IEEE1394 2 Port
Size
Custom
Document Number
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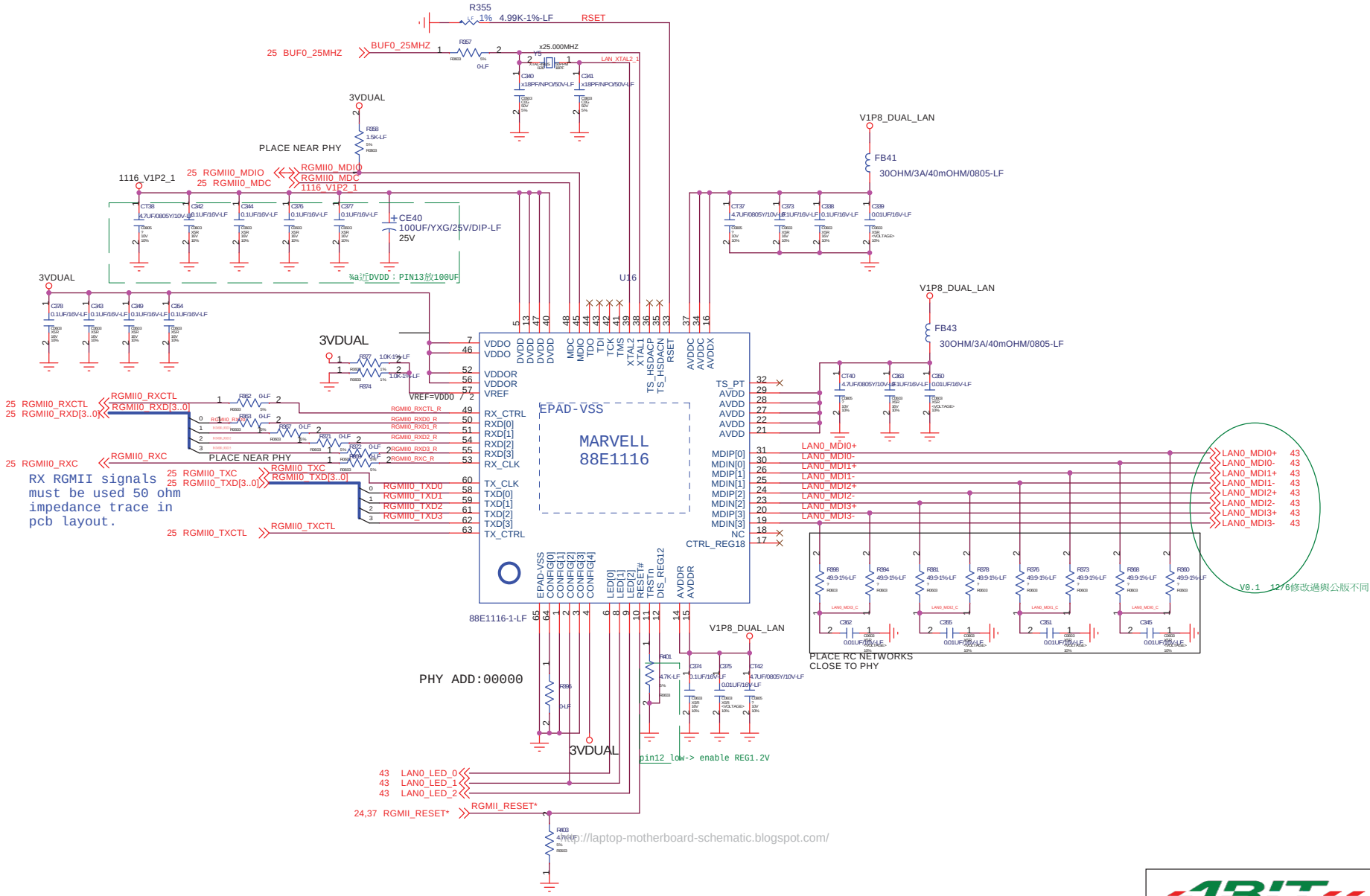

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Title

RGMII LAN 88E1116 PHY0

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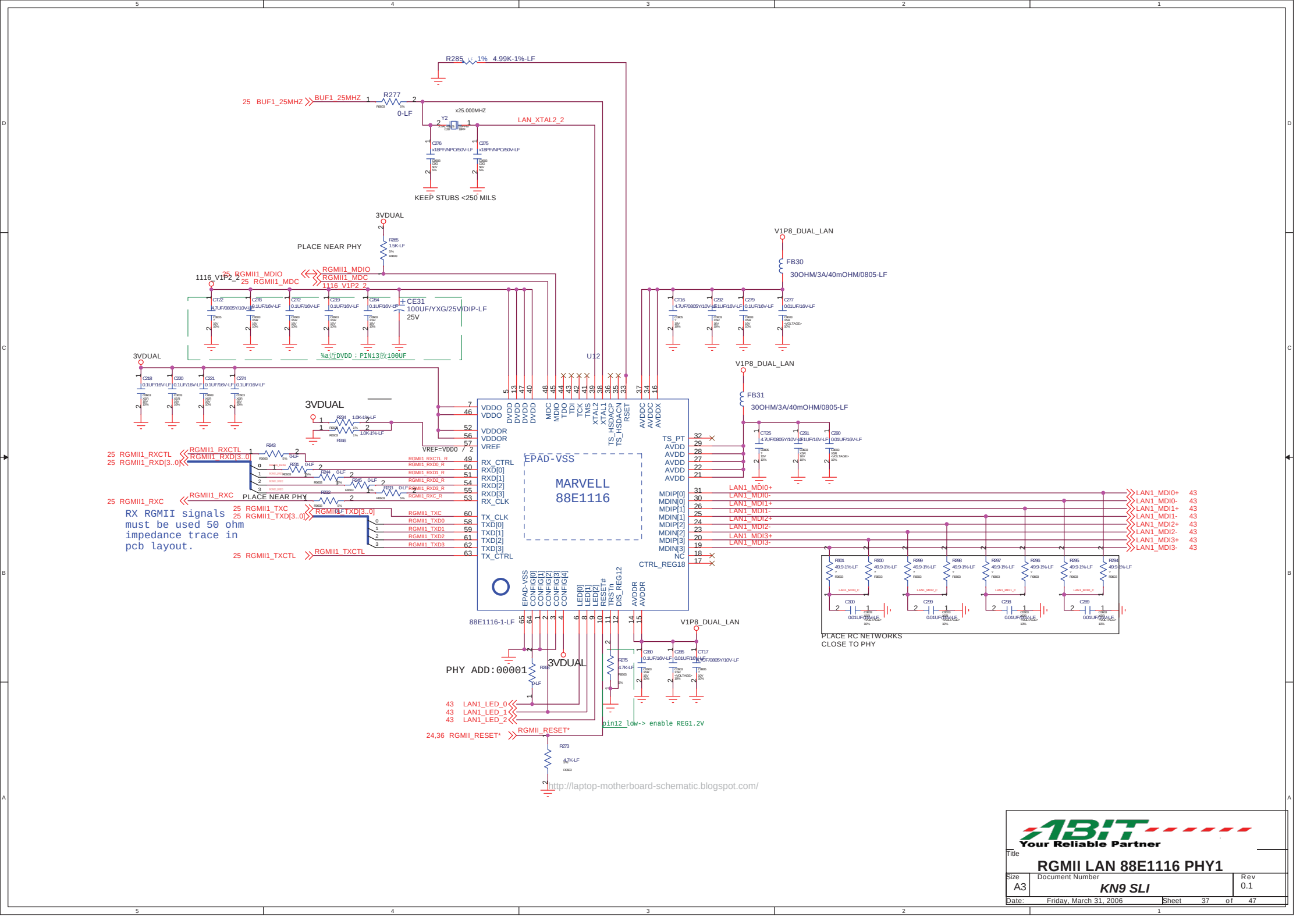
R285 1% 4.99K-1%-LF
25 BUF1_25MHZ
BUF1_25MHZ
R277
0-LF
x25.000MHZ
Y2
LAN_XTAL2_2
C276 x18PF/NPO/50V-LF
C275 x18PF/NPO/50V-LF
KEEP STUBS <250 MILS
3VDUAL
PLACE NEAR PHY
R265 1.5K-LF
25 RGMII1_MDIO
25 RGMII1_MDC
RGMII1_MDIO
RGMII1_MDC
1116 V1P2 2
CT22 4.7UF/0805Y/10V-LF
C278 0.1UF/16V-LF
C272 0.1UF/16V-LF
C219 0.1UF/16V-LF
C264 0.1UF/16V-LF
CE31 100UF/YXG/25V/DIP-LF 25V
DVDD : PIN13/37/100UF
V1P8_DUAL_LAN
FB30
30OHM/3A/40mOHM/0805-LF
CT16 4.7UF/0805Y/10V-LF
C292 0.1UF/16V-LF
C279 0.1UF/16V-LF
C277 0.01UF/16V-LF
U12
C218 0.1UF/16V-LF
C220 0.1UF/16V-LF
C221 0.1UF/16V-LF
C274 0.1UF/16V-LF
R234 1.0K-1%-LF
R246 1.0K-1%-LF
VREF=VDD0 / 2
FB31
30OHM/3A/40mOHM/0805-LF
CT25 4.7UF/0805Y/10V-LF
C291 0.1UF/16V-LF
C290 0.01UF/16V-LF
25 RGMII1_RXCTL
25 RGMII1_RXD[3..0]
RGMII1_RXCTL
RGMII1_RXD[3..0]
R243 0-LF
R228 0-LF
R244 0-LF
R245 0-LF
R223 0-LF
25 RGMII1_RXC
RGMII1_RXC
PLACE NEAR PHY
R222 0-LF
25 RGMII1_TXC
25 RGMII1_TXD[3..0]
RGMII1_TXD[3..0]
25 RGMII1_TXCTL
RGMII1_TXCTL
RX RGMII signals must be used 50 ohm impedance trace in pcb layout.
RGMII1_RXCTL_R
RGMII1_RXD0_R
RGMII1_RXD1_R
RGMII1_RXD2_R
RGMII1_RXD3_R
RGMII1_RXC_R
RGMII1_TXC
RGMII1_TXD0
RGMII1_TXD1
RGMII1_TXD2
RGMII1_TXD3
VDDO
VDDO
VDDOR
VDDOR
VREF
RX_CTRL
RXD[0]
RXD[1]
RXD[2]
RXD[3]
RX_CLK
TX_CLK
TXD[0]
TXD[1]
TXD[2]
TXD[3]
TX_CTRL
DVDD
MDC
MDIO
TDO
TDI
TCK
TMS
XTAL2
XTAL1
TS_HSDACP
TS_HSDACN
RSET
AVDDC
AVDDC
AVDDX
EPAD-VSS
MARVELL
88E1116
TS_PT
AVDD
MDIP[0]
MDIN[0]
MDIP[1]
MDIN[1]
MDIP[2]
MDIN[2]
MDIP[3]
MDIN[3]
NC
CTRL_REG18
LAN1_MDI0+
LAN1_MDI0-
LAN1_MDI1+
LAN1_MDI1-
LAN1_MDI2+
LAN1_MDI2-
LAN1_MDI3+
LAN1_MDI3-
R301 49.9-1%-LF
R300 49.9-1%-LF
R299 49.9-1%-LF
R298 49.9-1%-LF
R297 49.9-1%-LF
R296 49.9-1%-LF
R295 49.9-1%-LF
R294 49.9-1%-LF
C300 0.01UF/50V-LF
C299 0.01UF/50V-LF
C298 0.01UF/50V-LF
C289 0.01UF/50V-LF
PLACE RC NETWORKS CLOSE TO PHY
EPAD-VSS
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
LED[0]
LED[1]
LED[2]
RESET#
TRS TH
DIS_REG12
AVDDR
AVDDR
88E1116-1-LF
V1P8_DUAL_LAN
C280 0.1UF/16V-LF
C295 0.01UF/16V-LF
CT17 4.7UF/0805Y/10V-LF
PHY ADD:00001
3VDUAL
R275 4.7K-LF
R233 0-LF
43 LAN1_LED_0
43 LAN1_LED_1
43 LAN1_LED_2
pin12 low-> enable REG1.2V
24,36 RGMII_RESET*
RGMII_RESET*
R273 4.7K-LF
http://laptop-motherboard-schematic.blogspot.com/
ABIT Your Reliable Partner
Title
RGMII LAN 88E1116 PHY1
Size A3
Document Number KN9 SLI
Rev 0.1
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VCC5A NORMAL VOLTAGE = 4.7V (2%)

GND GND_AUDIO

priority of first close to PIN25,38

priority of first close to PIN1,9

For RT9167 R1:NC; R2:NC; C1:0.1uF

For RT9179 R1:3.01K_1%; R2:1K_1%; C1:0.1uF

ALC880-LF,REV:H
3139-00-0021
ALC882M-LF,REV:B1
3139-00-0020

FB13

pin 47

50 mils wide

pin 12

ALC882M CODEC

60-100mils gap isolation

GND_AUDIO

AUDIO1B AUDIO1A

GND_EMI_AUDIO

GND

For PCB Layout copper area and placement

xFB28

FRONT PANEL AUDIO

V0.2 for 885共用

V0.2

close to sense pin & away from analog trace
(the best choice is botton side)

VREF Decouple Caps
1) Place close to codec as possible as you can.
2) Signal trace routed through or beneath is forbidden.

Place close to OPT-IN1.

Don't stuff this bead.
Or it will degrade audio quality.

GND_AUDIO GND_EMI_AUDIO

GND_AUDIO GND_EMI_AUDIO

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Title: HD AUDIO CODEC

Size	Document Number	Rev
A3	KN9 SLI	0.1

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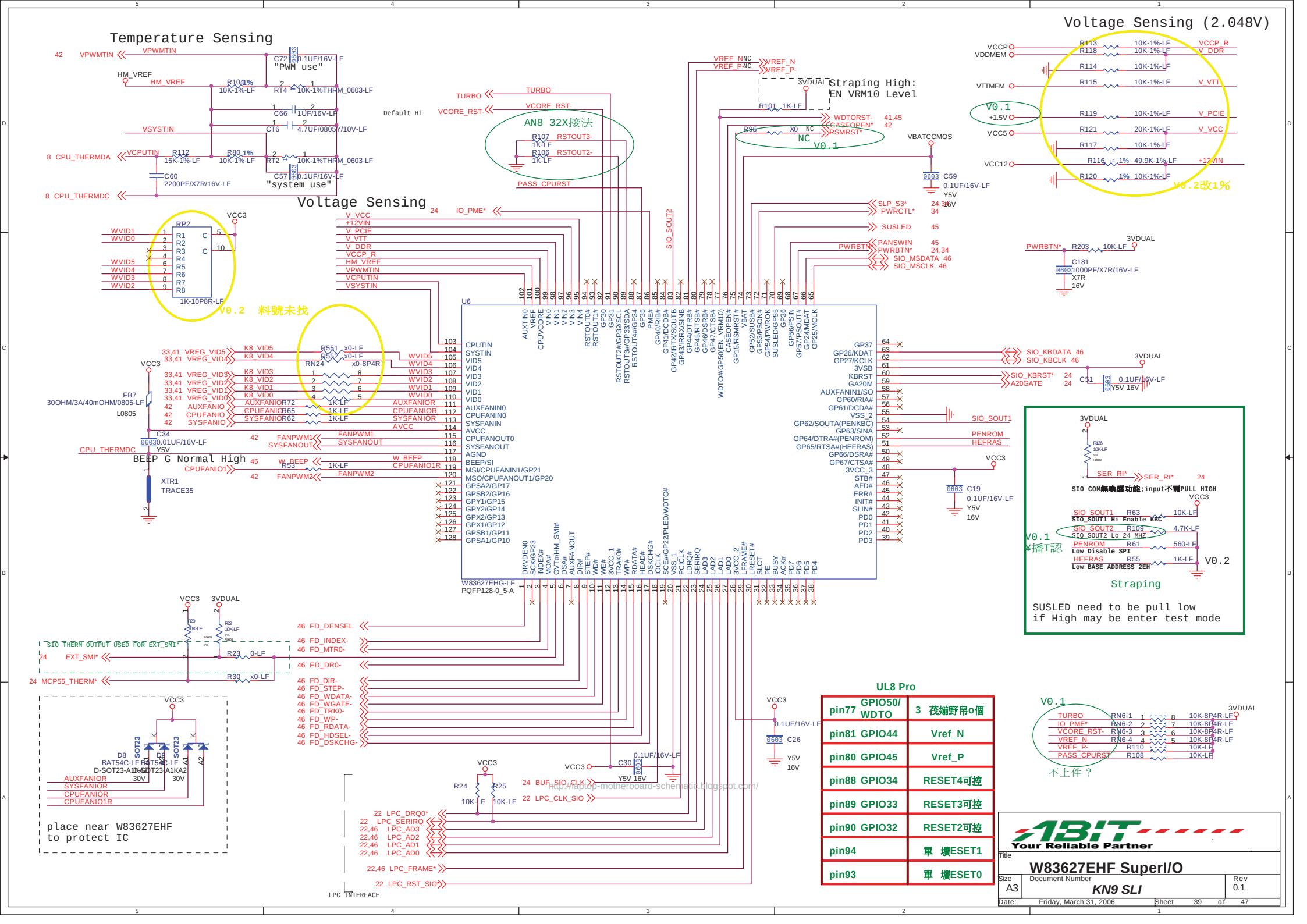
Temperature Sensing
"PWM use"
"system use"
Voltage Sensing
Voltage Sensing (2.048V)
Straping High:
EN_VRM10 Level
AN8 32X接法
NC
V0.1
V0.2 料號未找
V0.2改1%
BEEP G Normal High
SIO THERM OUTPUT USED FOR EXT_SMI
place near W83627EHF
to protect IC
W83627EHG-LF
PQFP128-0_5-A
LPC INTERFACE
Straping
SUSLED need to be pull low
if High may be enter test mode
SIO COM無喚醒功能;input不需PULL HIGH
SIO_SOUT1 Hi Enable KBC
SIO_SOUT2 Lo 24 MHZ
Low Disable SPI
Low BASE ADDRESS 2EH
V0.1
V0.2
不上件？
UL8 Pro
pin77 GPIO50/WDTO 3 茂嫦野帛o個
pin81 GPIO44 Vref_N
pin80 GPIO45 Vref_P
pin88 GPIO34 RESET4可控
pin89 GPIO33 RESET3可控
pin90 GPIO32 RESET2可控
pin94 單 壩ESET1
pin93 單 壩ESET0
http://laptop-motherboard-schematic.blogspot.com/
ABIT Your Reliable Partner
Title
W83627EHF SuperI/O
Size A3
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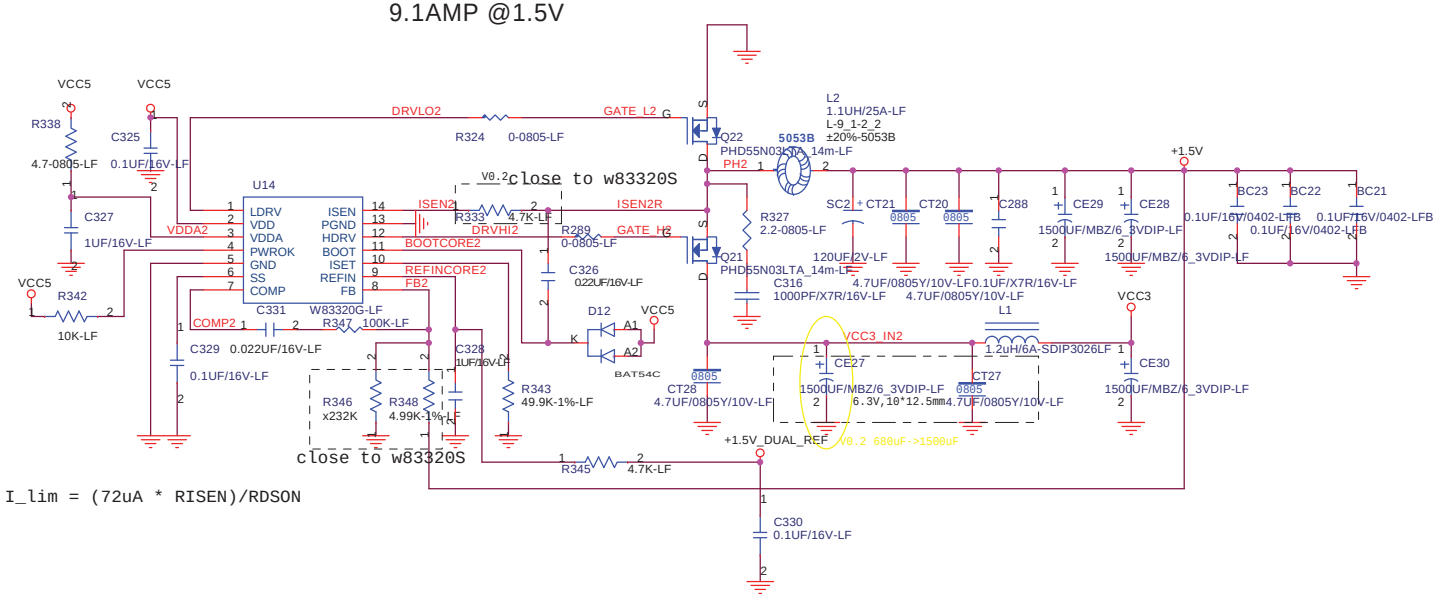
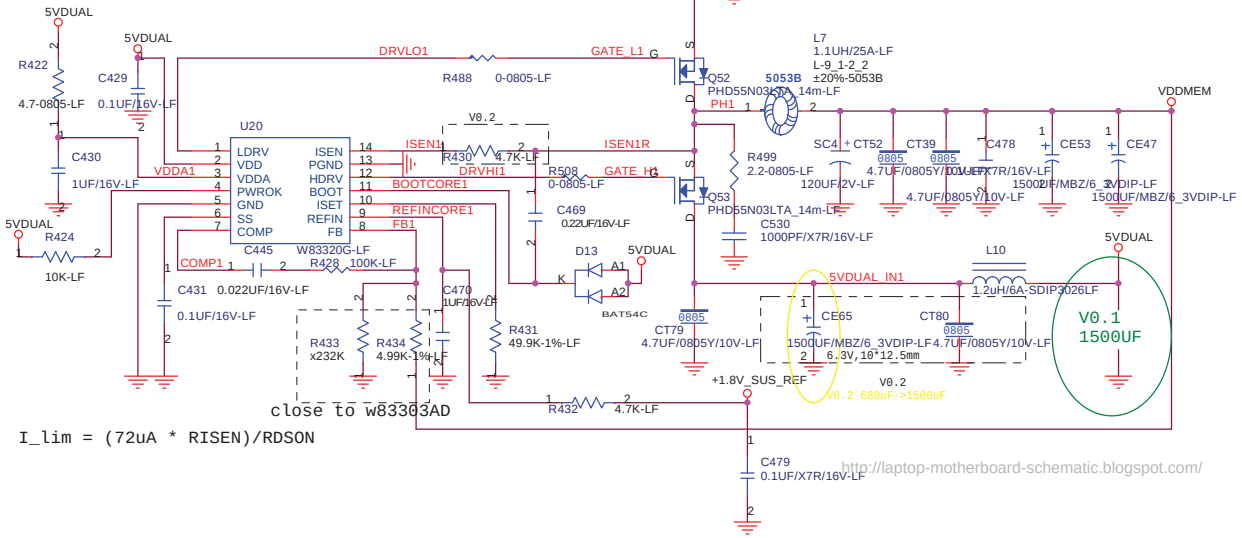
MCP55P CORE

9.1AMP @1.5V



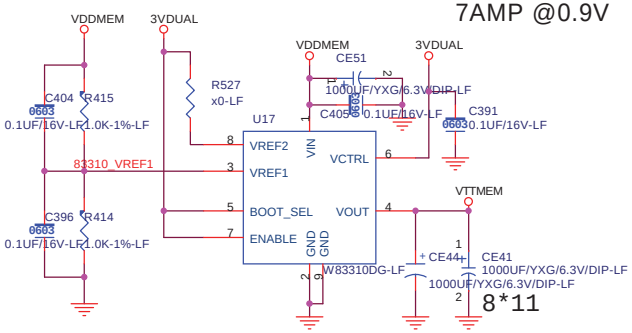
DDRII

22AMP @1.8V



DDRII Vref

7AMP @0.9V



MEM VTT Power module

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Title: MCP55P CORE & DDRII Power		
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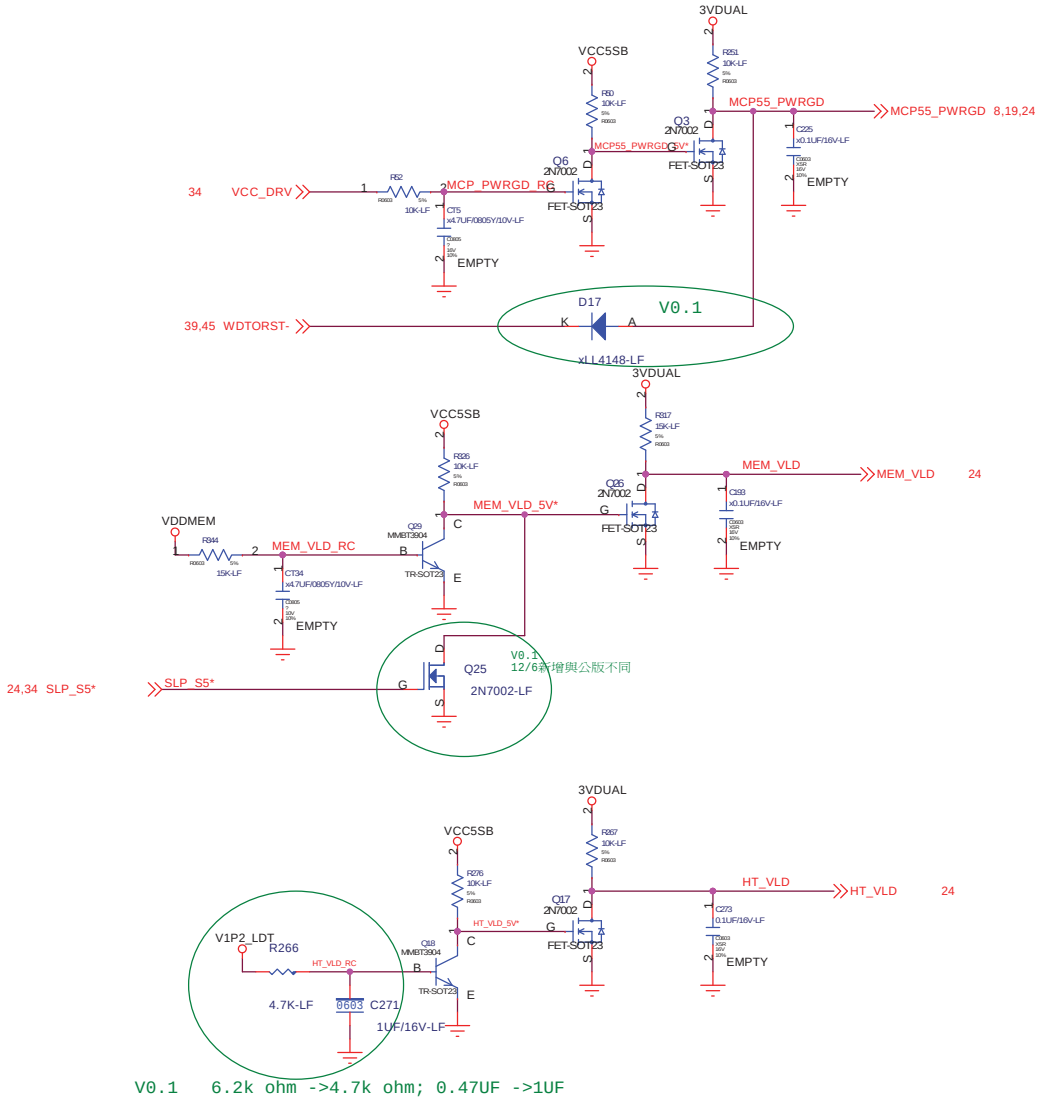
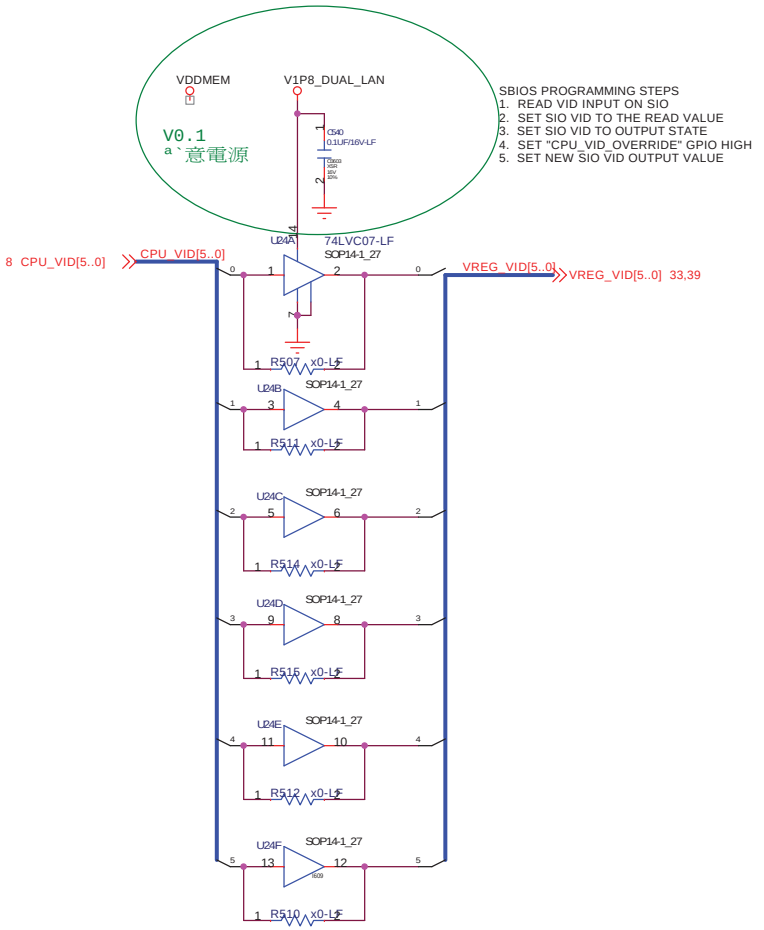


V0.1 6.2k ohm ->4.7k ohm; 0.47UF ->1UF



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Title: PWR SEQU & VID BUFFER

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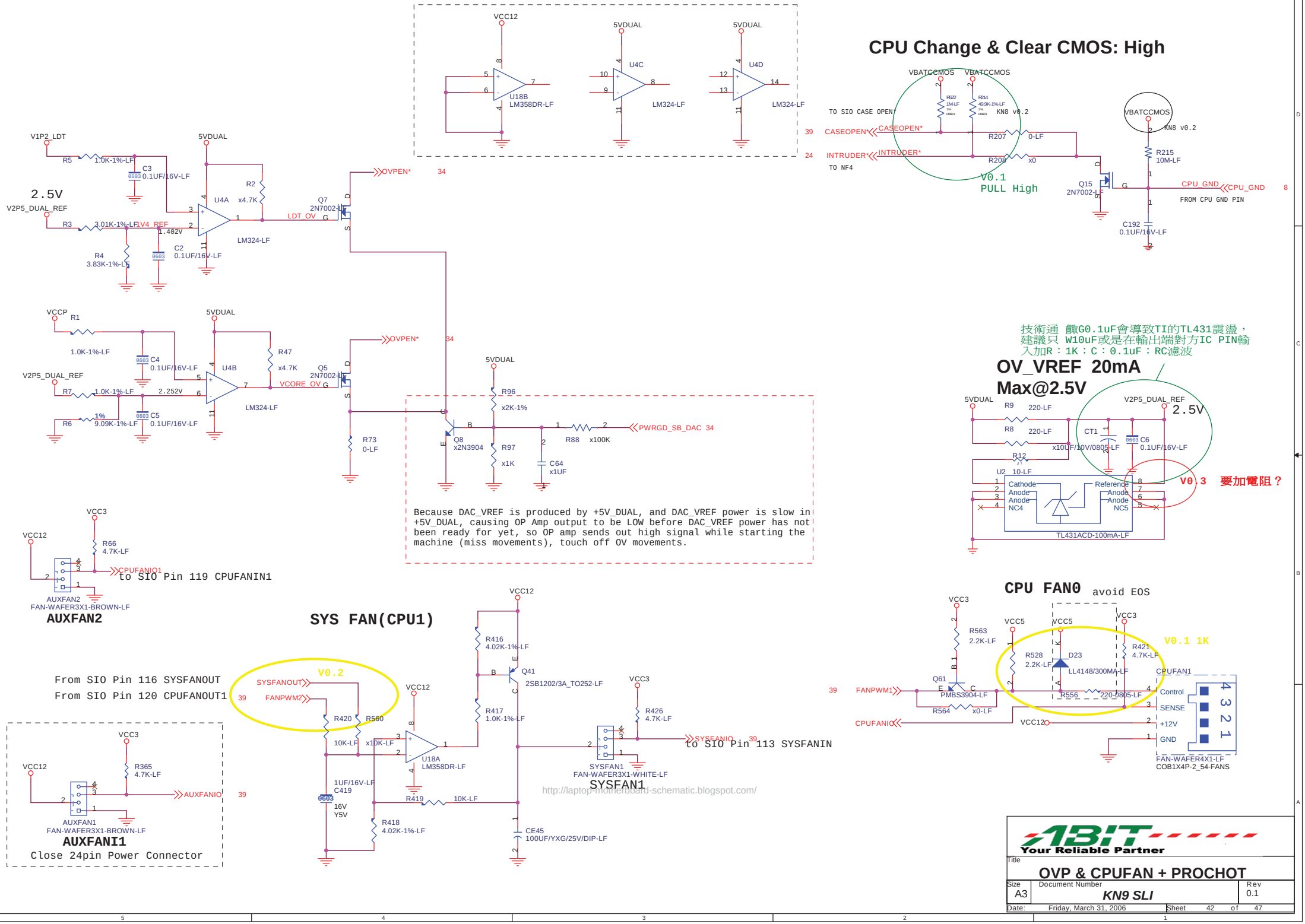
CPU Change & Clear CMOS: High
VCC12
5VDUAL
U18B
LM358DR-LF
U4C
LM324-LF
U4D
LM324-LF
VBATCCMOS
TO SIO CASE OPEN
KN8 v0.2
CASEOPEN*
INTRUDER*
TO NF4
R207
0-LF
R208
x0
V0.1
PULL High
Q15
2N7002-LF
R215
10M-LF
CPU_GND
FROM CPU GND PIN
C192
0.1UF/16V-LF
V1P2_LDT
R5
1.0K-1%-LF
C3
0.1UF/16V-LF
2.5V
V2P5_DUAL_REF
R3
3.01K-1%-LF
LV4_REF
1.402V
R4
3.83K-1%-LF
C2
0.1UF/16V-LF
U4A
LM324-LF
R2
x4.7K
Q7
2N7002-LF
LDT_OV
OVPEN*
VCCP
R1
1.0K-1%-LF
C4
0.1UF/16V-LF
R7
1.0K-1%-LF
2.252V
R6
1%
9.09K-1%-LF
C5
0.1UF/16V-LF
U4B
LM324-LF
R47
x4.7K
Q5
2N7002-LF
VCORE_OV
R73
0-LF
R96
x2K-1%
Q8
x2N3904
R97
x1K
C64
x1UF
R88
x100K
PWRGD_SB_DAC
Because DAC_VREF is produced by +5V_DUAL, and DAC_VREF power is slow in +5V_DUAL, causing OP Amp output to be LOW before DAC_VREF power has not been ready for yet, so OP amp sends out high signal while starting the machine (miss movements), touch off OV movements.
技術通 麒G0.1uF會導致TI的TL431震盪，
建議只 W10uF或是在輸出端對方IC PIN輸
入加R：1K；C：0.1uF；RC濾波
OV_VREF 20mA
Max@2.5V
R9
220-LF
R8
220-LF
CT1
x10UF/10V/0805-LF
C6
0.1UF/16V-LF
R12
10-LF
U2
TL431ACD-100mA-LF
V0.3 要加電阻？
VCC3
VCC12
R66
4.7K-LF
CPUFANIO1
to SIO Pin 119 CPUFANIN1
AUXFAN2
FAN-WAFER3X1-BROWN-LF
AUXFAN2
SYS FAN(CPU1)
From SIO Pin 116 SYSFANOUT
From SIO Pin 120 CPUFANOUT1
V0.2
SYSFANOUT
FANPWM2
R420
R560
10K-LF
x10K-LF
U18A
LM358DR-LF
R416
4.02K-1%-LF
Q41
2SB1202/3A_TO252-LF
R417
1.0K-1%-LF
R426
4.7K-LF
SYSFANIO
to SIO Pin 113 SYSFANIN
SYSFAN1
FAN-WAFER3X1-WHITE-LF
SYSFAN1
1UF/16V-LF
C419
16V
Y5V
R419
10K-LF
R418
4.02K-1%-LF
CE45
100UF/YXG/25V/DIP-LF
CPU FAN0 avoid EOS
R563
2.2K-LF
R528
2.2K-LF
D23
LL4148/300MA-LF
R421
4.7K-LF
V0.1 1K
Q61
PMBS3904-LF
R564
x0-LF
R556
220-0805-LF
FANPWM1
CPUFANIO
CPUFAN1
Control
SENSE
+12V
GND
FAN-WAFER4X1-LF
COB1X4P-2_54-FANS
AUXFANIO
AUXFAN1
FAN-WAFER3X1-BROWN-LF
AUXFANI1
Close 24pin Power Connector
http://laptop-motherboard-schematic.blogspot.com/
ABIT
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OVP & CPUFAN + PROCHOT
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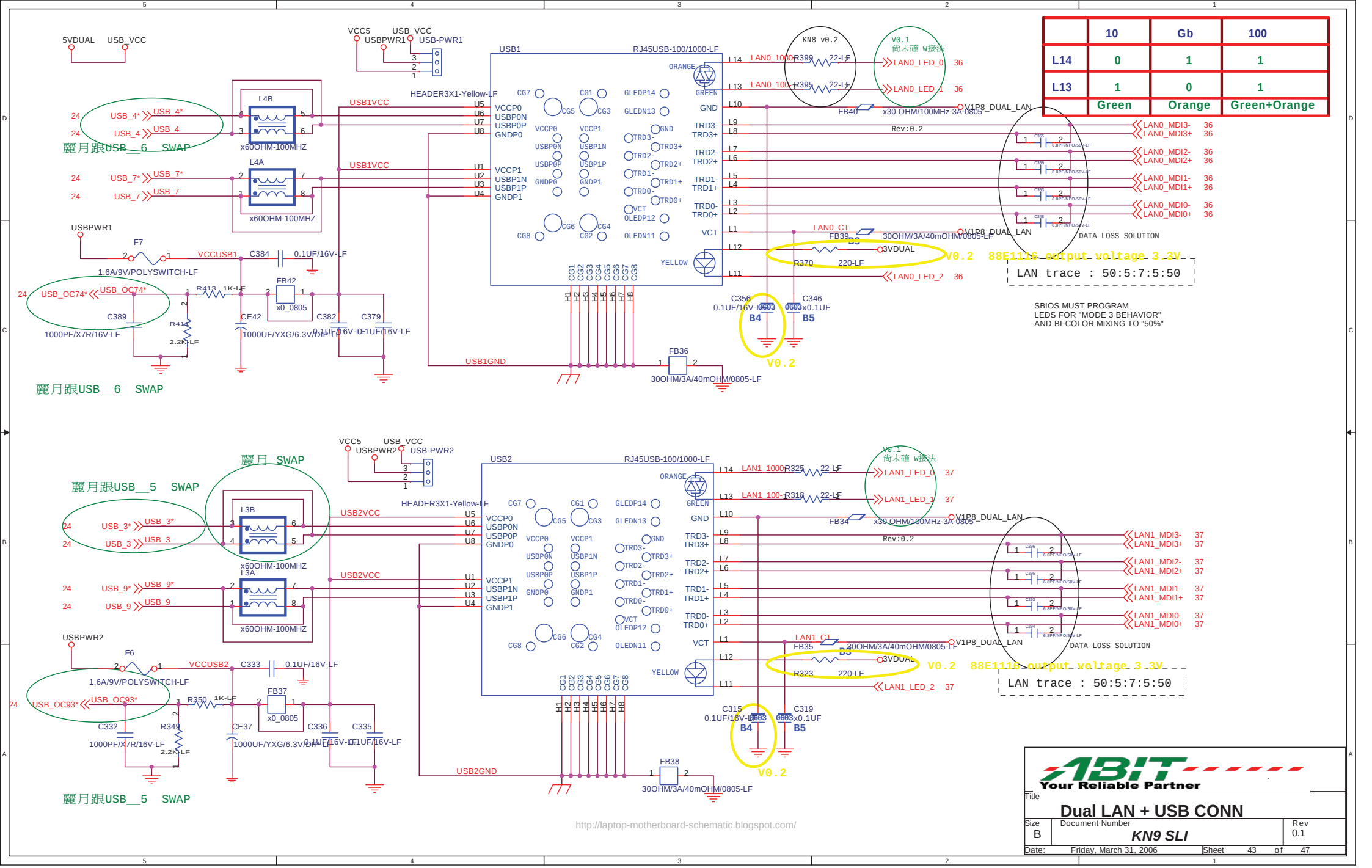
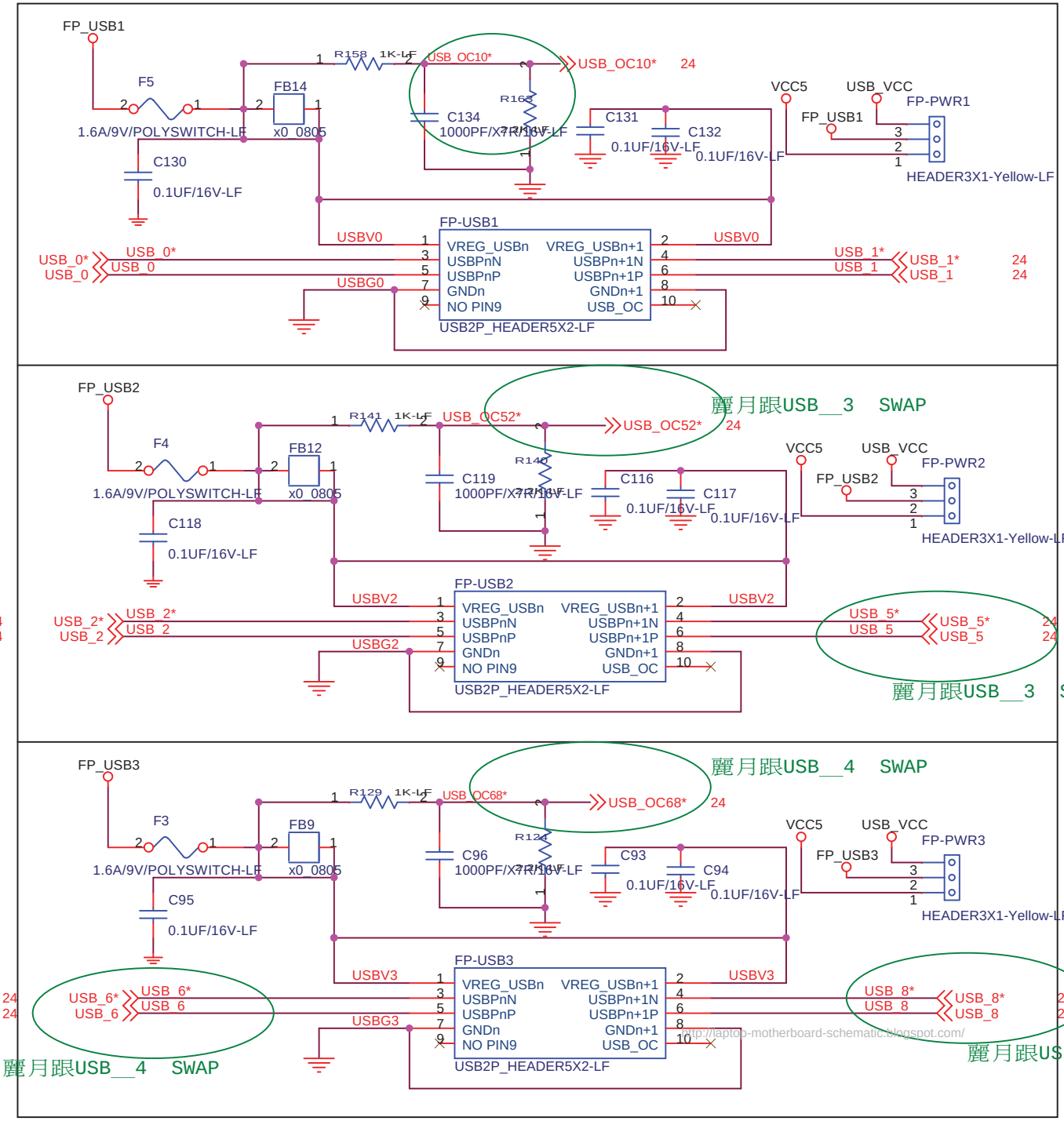


	10	Gb	100
L14	0	1	1
L13	1	0	1
	Green	Orange	Green+Orange



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Title: FP-USB CONN

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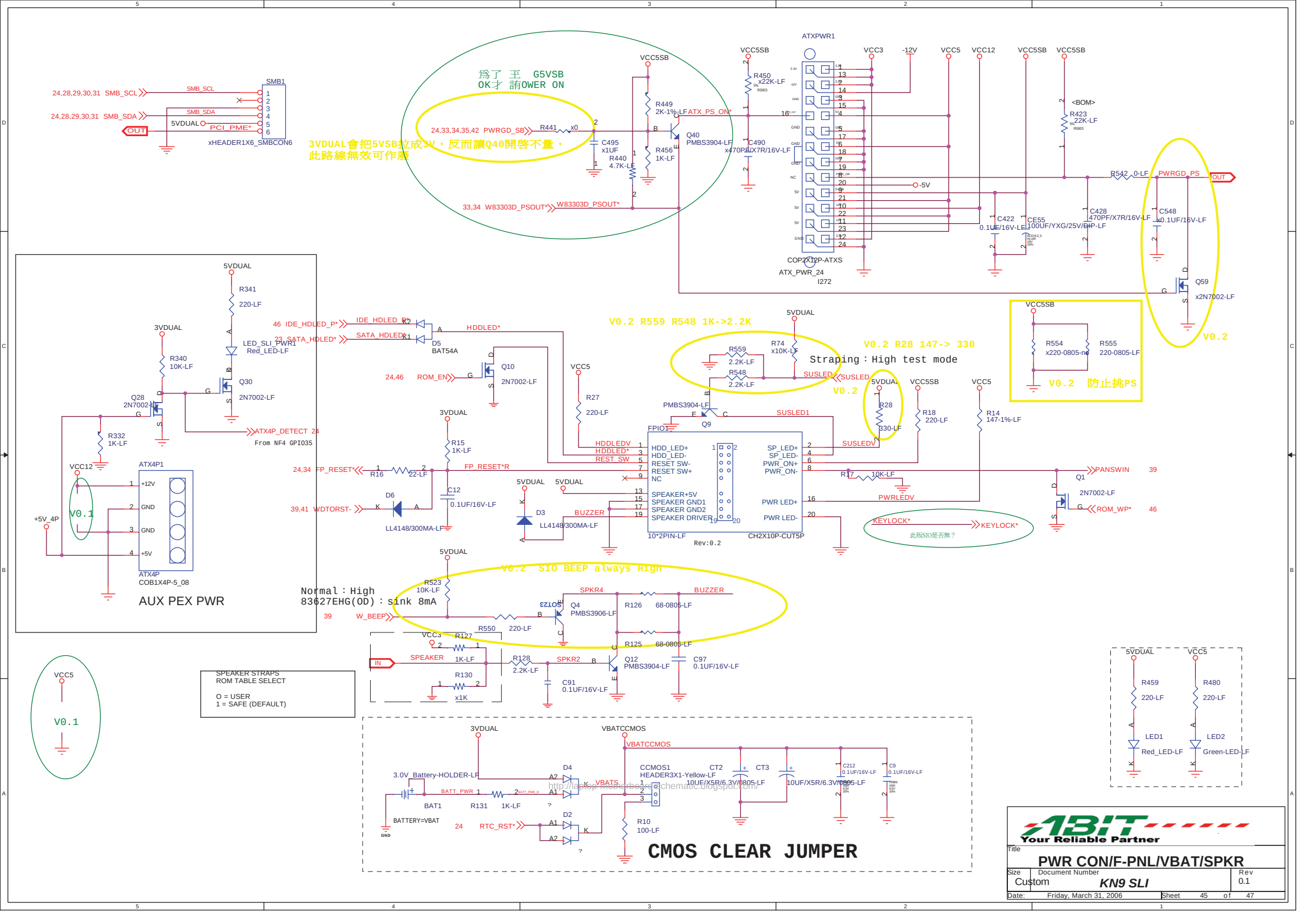
SMB1
SMB_SCL
SMB_SDA
PCI_PME*
OUT
xHEADER1X6_SMBCON6
為了 王 G5VSB
OK才 請OWER ON
3VDUAL會把5VSB拉成3V，反而讓Q40開啓不量，
此路線無效可作廢
PWRGD_SB
W83303D_PSOUT*
ATX_PS_ON*
Q40
PMBS3904-LF
ATXPWR1
COP2X12P-ATXS
ATX_PWR_24
I272
-5V
PWRGD_PS
Q59
x2N7002-LF
V0.2
V0.2 R559 R548 1K->2.2K
V0.2 R28 147-> 330
Straping：High test mode
V0.2 防止挑PS
R554
R555
220-0805-LF
SUSLED
SUSLED1
SUSLEDV
FPIO1
10*2PIN-LF
CH2X10P-CUT5P
Rev:0.2
HDD_LED+
HDD_LED-
RESET SW-
RESET SW+
SPEAKER+5V
SPEAKER GND1
SPEAKER GND2
SPEAKER DRIVER
SP_LED+
SP_LED-
PWR_ON+
PWR_ON-
PWR LED+
PWR LED-
PANSWIN
ROM_WP*
PWRLEDV
KEYLOCK*
此版SIO是否無？
V0.2 SIO BEEP always High
Normal：High
83627EHG(OD)：sink 8mA
W_BEEP
SPKR4
SPKR2
BUZZER
SPEAKER
SPEAKER STRAPS
ROM TABLE SELECT
O = USER
1 = SAFE (DEFAULT)
AUX PEX PWR
ATX4P1
ATX4P
COB1X4P-5_08
From NF4 GPIO35
CMOS CLEAR JUMPER
3.0V_Battery-HOLDER-LF
BAT1
BATTERY=VBAT
CCMOS1
HEADER3X1-Yellow-LF
http://laobp.blogspot.com/
LED1
Red_LED-LF
LED2
Green-LED-LF
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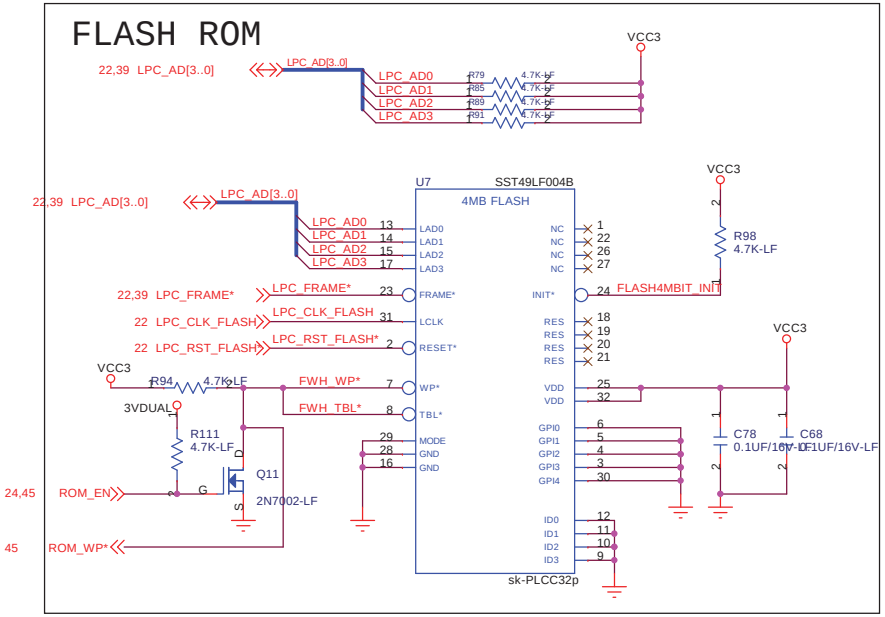
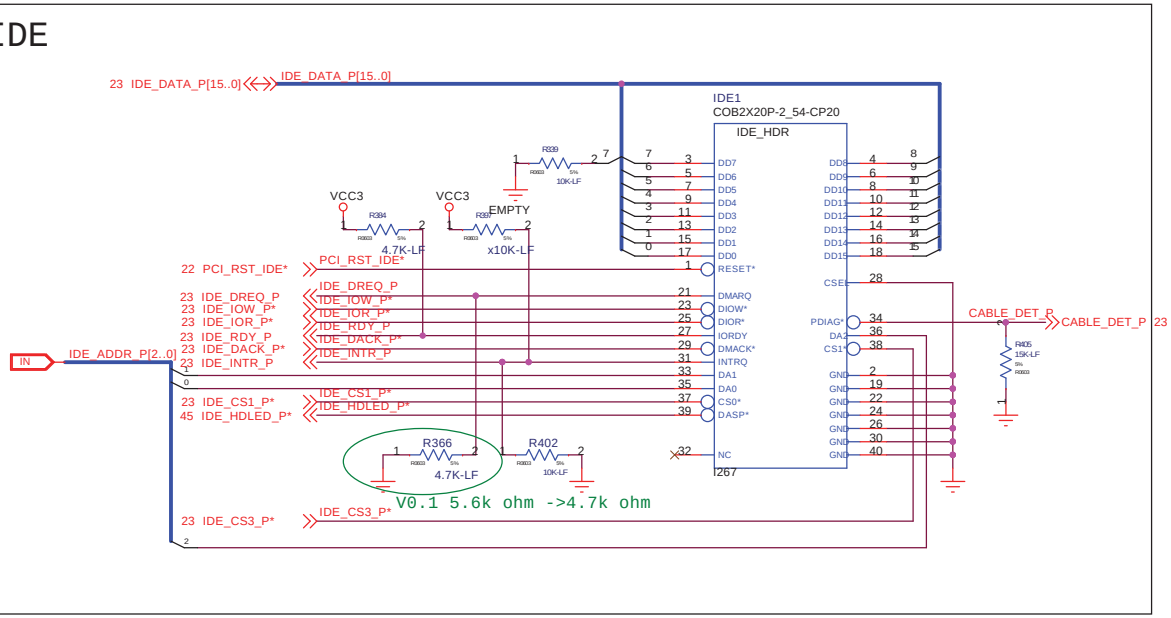
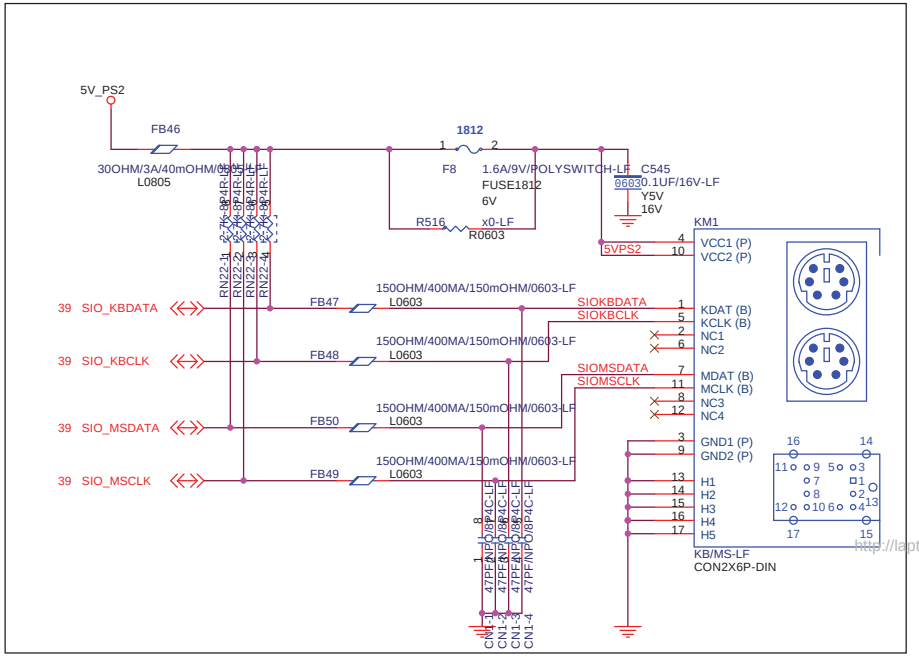
FLASH ROM

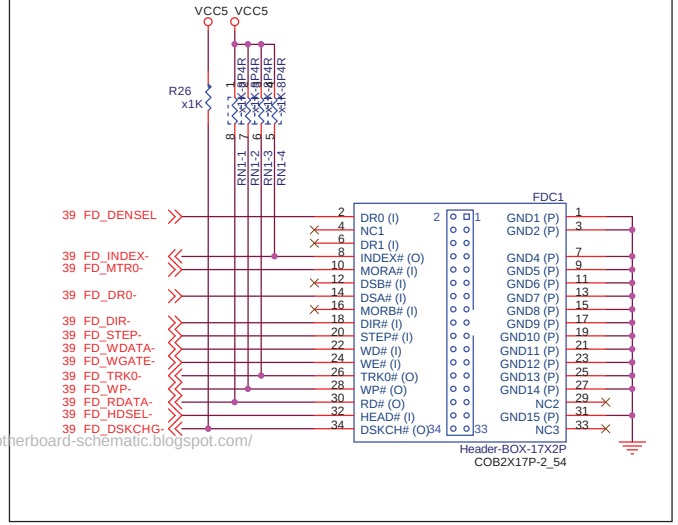


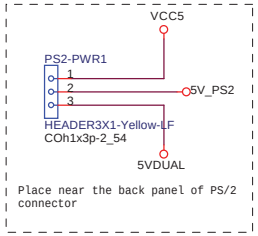
IDE



FLOPPY CONNECTOR







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Title: K/M+LPC+Bios+FDC+IDE

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USB-PWR1-5 JUMPER

USB-PWR1(2-3)-LF USB-PWR2(2-3)-LF FP-PWR1(2-3)-LF FP-PWR2(2-3)-LF FP-PWR3(2-3)-LF

JUMPER-2PIN-YELLOW-LF

CCMOS JUMPER

CCMOS1(1-2)-LF

JUMPER-2PIN-YELLOW-LF

FP-AUDIO JUMPER

LABEL

LABEL1

LABEL
PhoenixBIOS
D686 BIOS
PHOENIX 1998

BIOS LABEL

BIOS

FWH1

PM49FL004T
FLASH ROM
4M BIT
32PIN PLCC

BIOS

PS2-PWR1(1-2)1

JUMPER-2PIN-YELLOW-LF
PCB Footprint

N1

FAN_KIT-L

FAN_KIT-R

FAN KIT 51.5*11.5mm

PWM_HSINK1 PWM_HEATSINK-HALF

HSINK-L HSINK-R

1 2 3 4

BAT1

3V_BATTERY

M2RETENTION1

M2-Retention-LF

JW1

JUMP WIRE

Only for 14.318MHz XTAL use

FILE1

BIOS Firmware
Data File

BIOS FIRMWARE1

FILE2

1394 Firmware
Data File

1394 FIRMWARE1

FILE3

AC2005 Firmware
Data File

1394 FIRMWARE1

RL7 RL14 RL1 RL4 RL24

RL3 RL8 RL22 RL5 RL6 RL2

RL23 RL17 RL20 RL12 RL21 RL11

RL19 RL16 RL18 RL15 RL10 RL25

xMarkin-R

VCC12 VCC12 VCC12 VCC12 VCC12 VCC12 VCC12 VCC12

470 ohm_1206

CLED

SLED

AN8 SLI

RED為顯示卡禁制區 1Cm 1Cm

4Cm 4.5Cm

PCI PCI PCIEXP PCIEXP PCIEXP

G-CARD G-CARD

M/B

CUPON1 CUPON2 VCC5

NC CUPON1 CUPON2 NC

xHeader-2X1P xHeader-2X1P

M1 M2 M12

x4MMH

M5 M8 M7 M3 M6 M9 M11 M4 M10

xM8_3X4G

PSU & Derivatives

V3P3SB
V2P5SB
V1P5SB
VBATDUAL
VBAT VBATCCMOS
+1.2V_DUAL V1P2_DUAL

CPU, DDR, NB, SB

+V_CPU VCCP
+1.8V_SUS VDDMEM
+0.9V_SUS VTTMEM
V1P5_GMCH
V1P5_NB
V1P5_ICH
+12V V1P2

Platform

V1P2_VTT
+1.2V_HT V1P2_LDT
+2.5V V2P5_VDDA
V1P5_PCIE
V2P5_MISC
V2P5_LAN
V1P8_LAN

-12V -12V
5VDUAL +5V_DUAL
3VDUAL +3.3V_DUAL
VCC5SB +5V_STBY

VCC5 +5V
VCC12 +12V
VCC12A +12V_ATXP
VCC3 +3.3V

AN8 32X nvidia

8W欧

+1.2V_DUAL_LAN V1P2_DUAL_LAN

+1.8V_DUAL_LAN V1P8_DUAL_LAN

-鴎誨x JCㄉ

JC q的規範

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Title: MOUNTING HOLES&FIDUCIALS&etc

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