MS-9849 uATX Version: 0A

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35/G33 North Bridge
Intel ICH9 South Bridge

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635
LAN -- INTEL NINEVEH/EKRON
HD Audio Codec -- ALC888
DVI Controller -- SII1364A(2PORT)
PCIE to PATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

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Custom	COVER SHEET	0A

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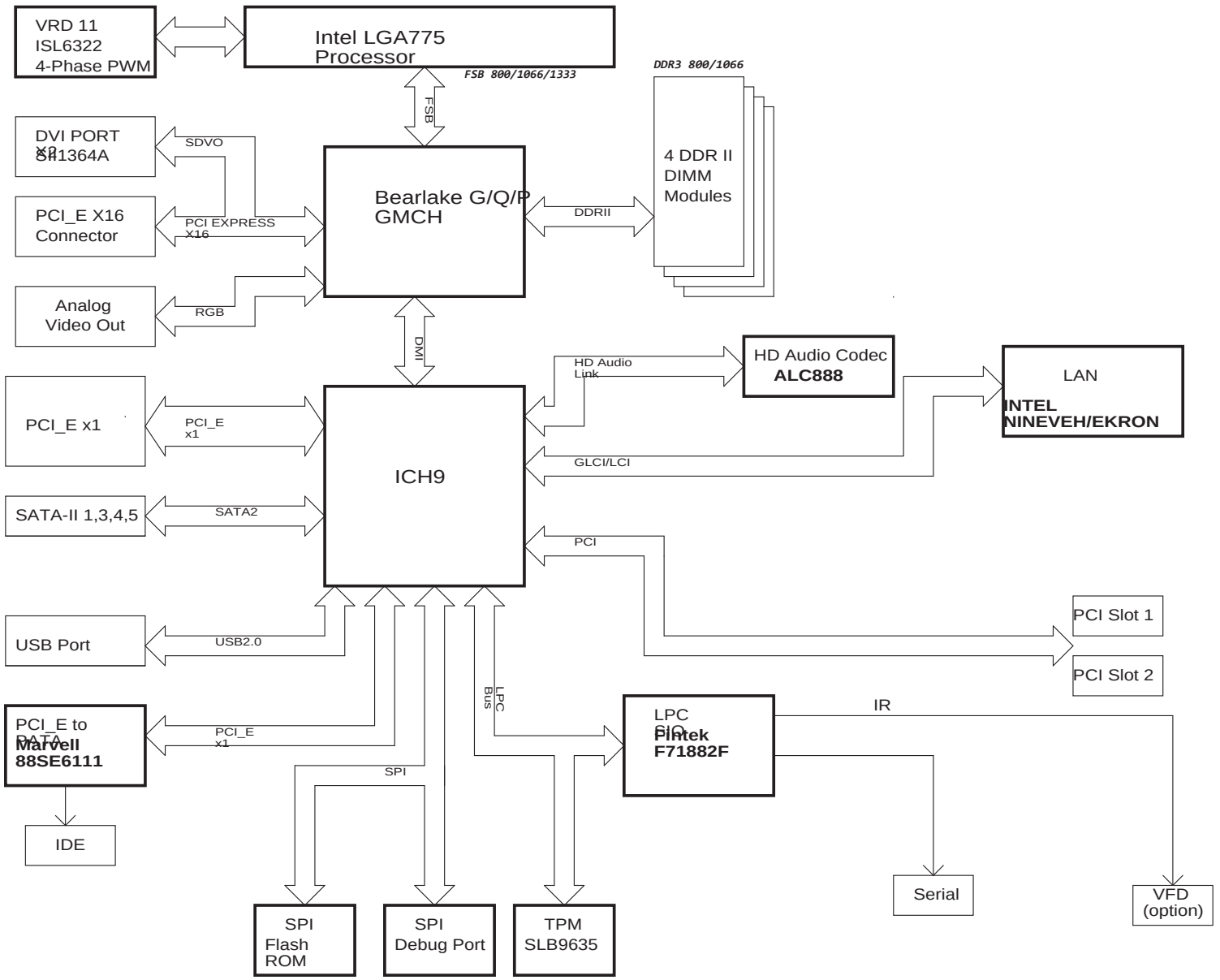
Block Diagram



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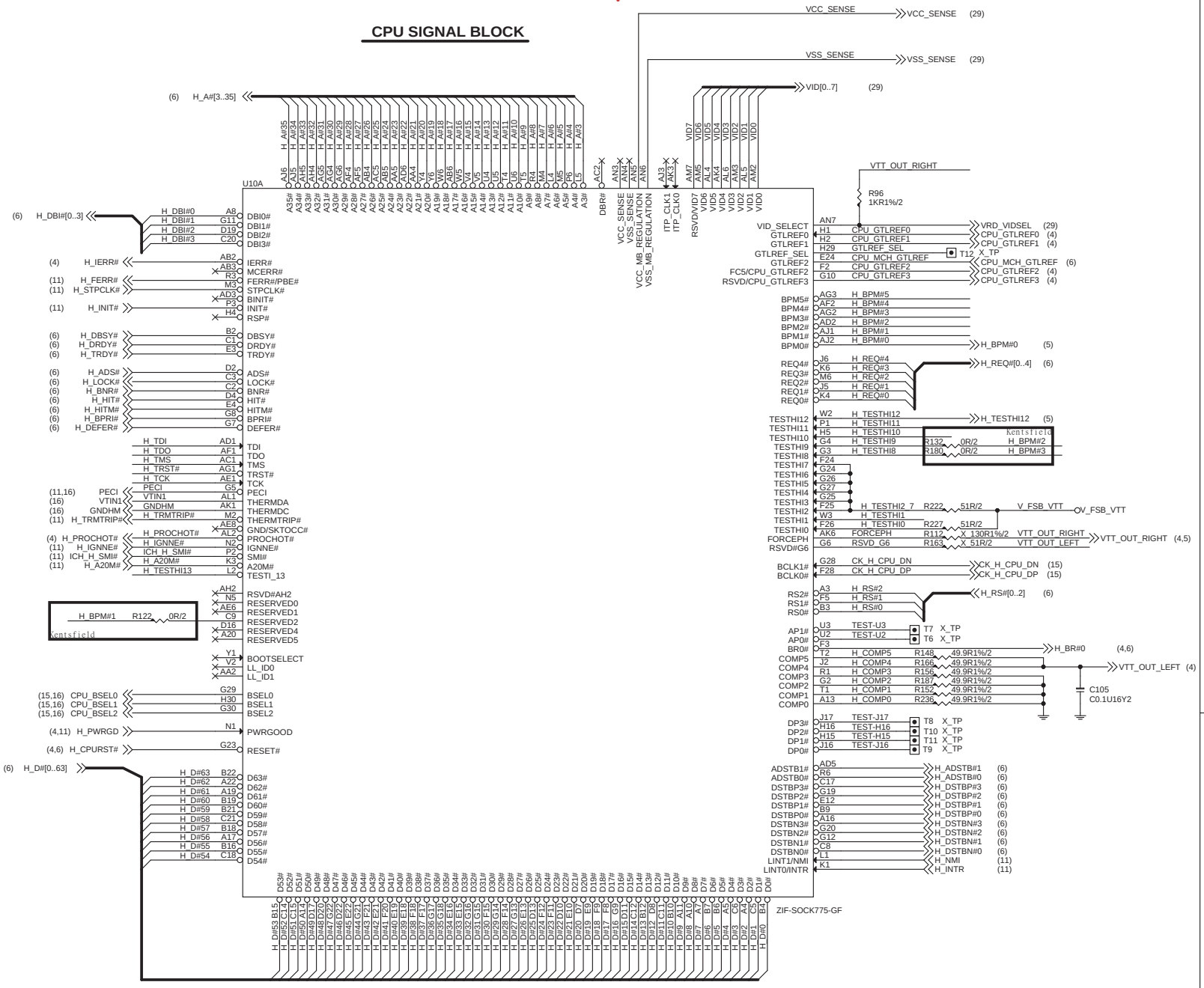
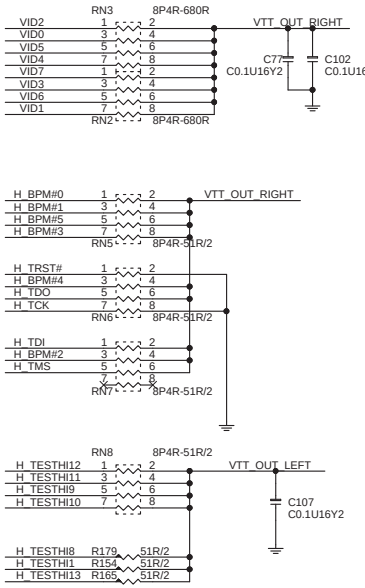
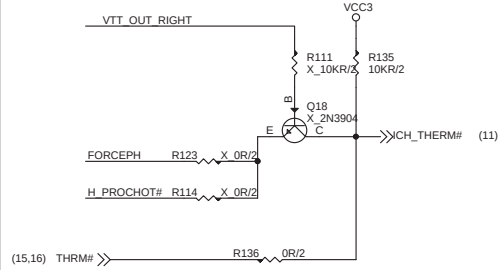
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



Thermal TRIP



MSI	MICRO-STAR INT'L CO.,LTD	
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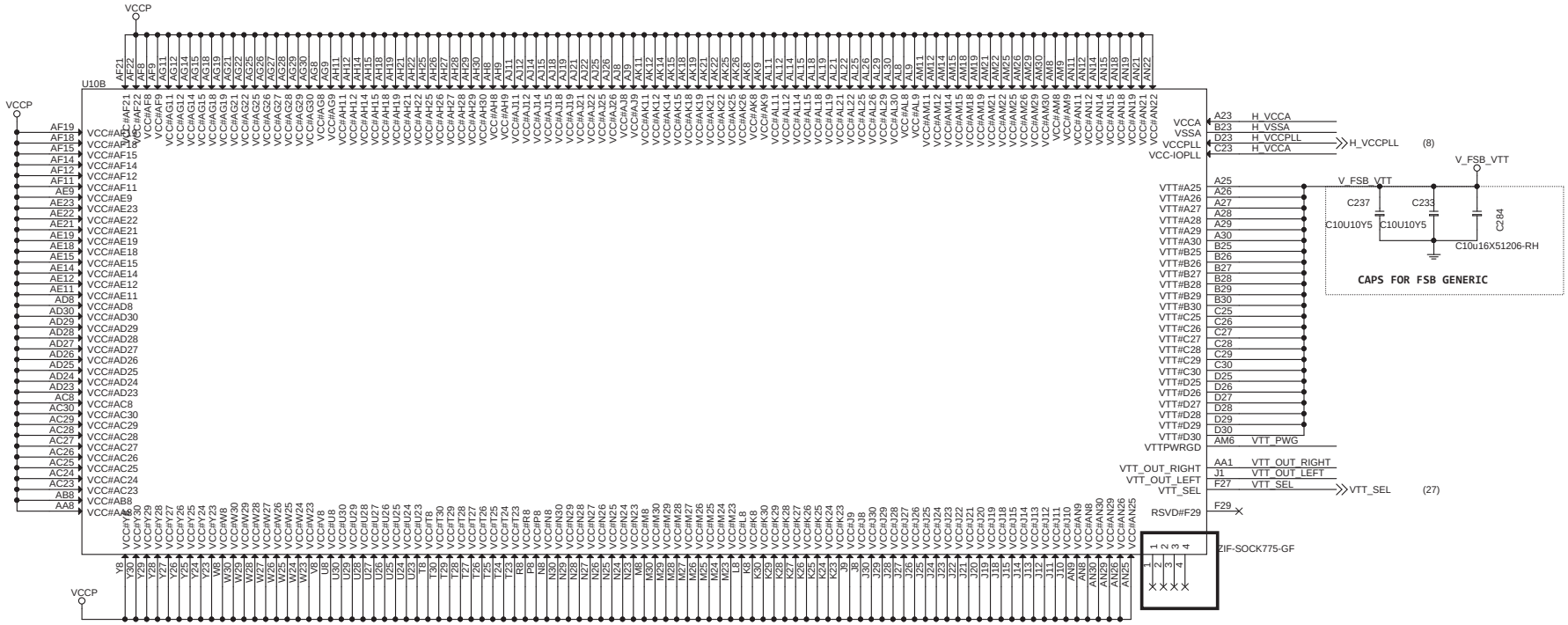
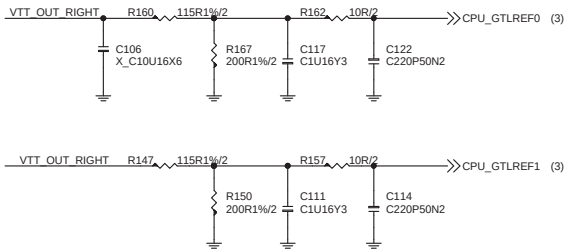
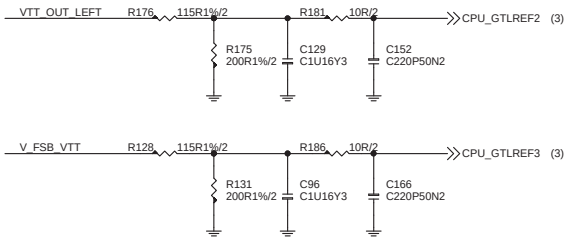
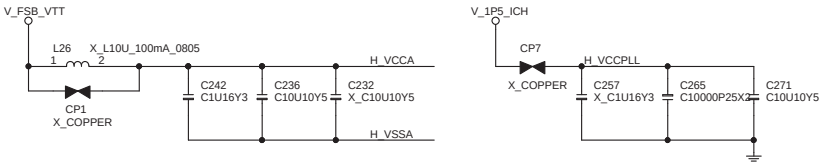


*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)

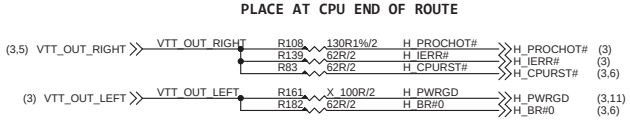




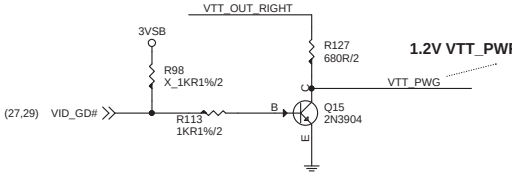
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

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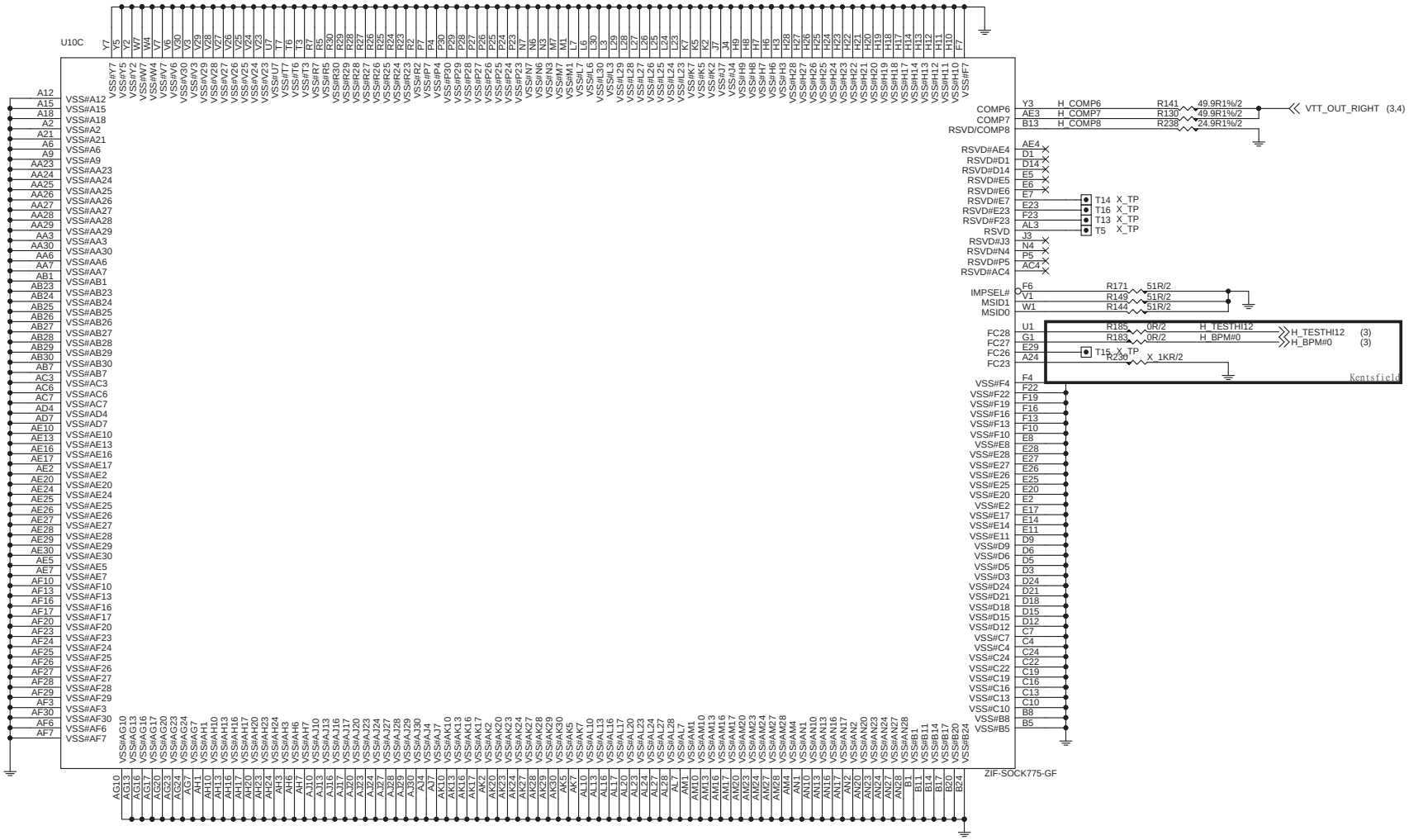

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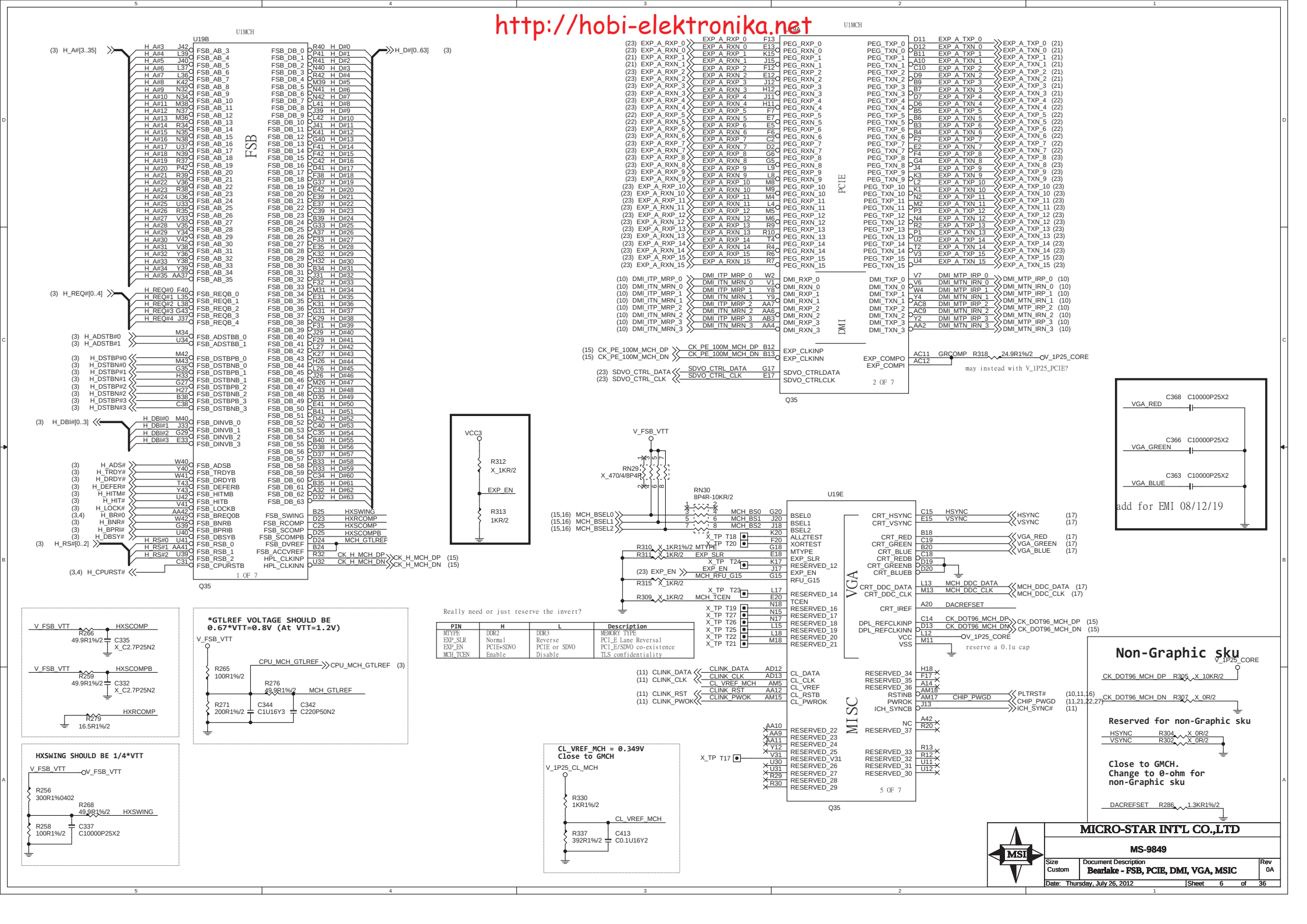

PIN	H	L	Description
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	PCIE+SDVO	PCIE or SDVO	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

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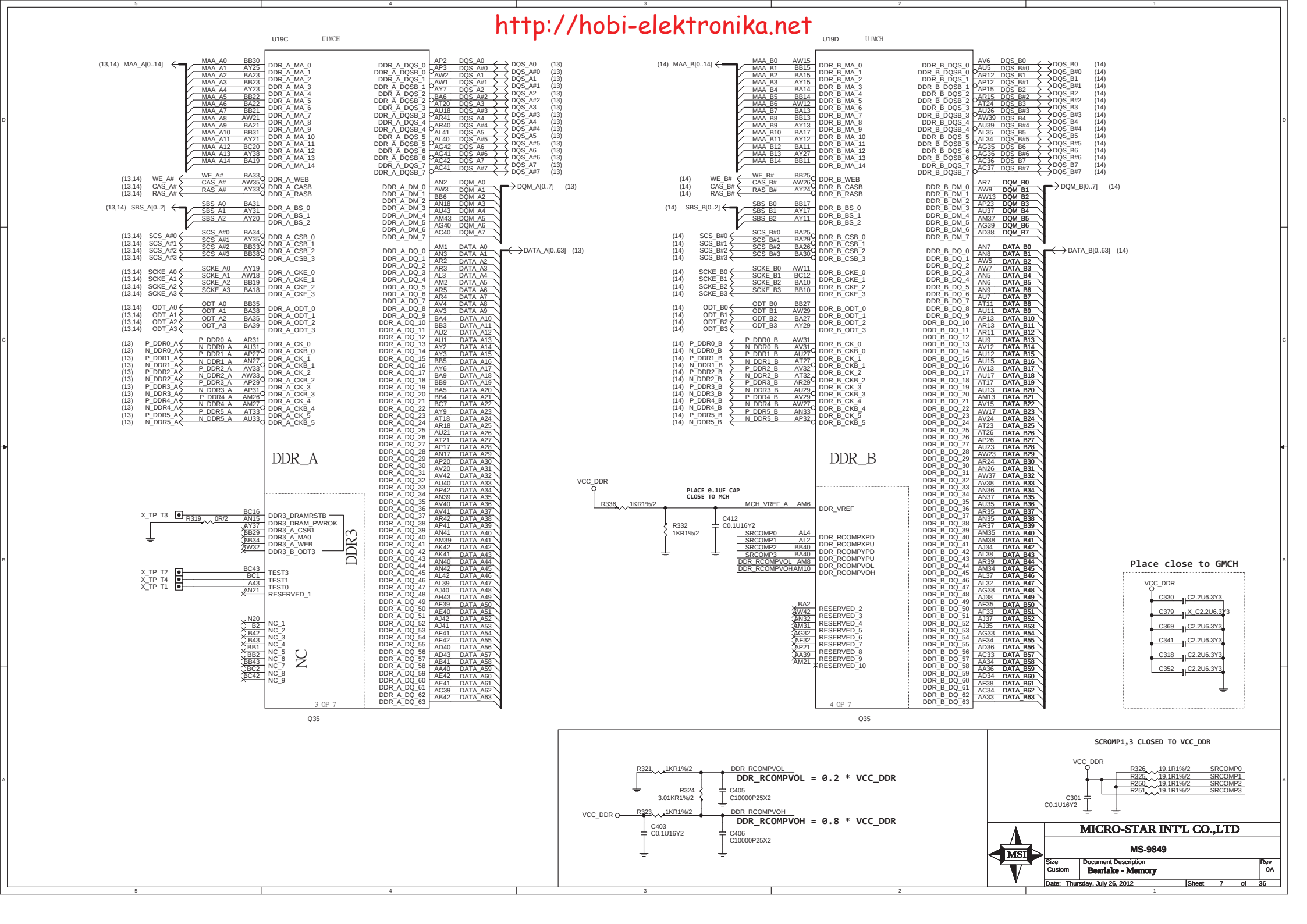
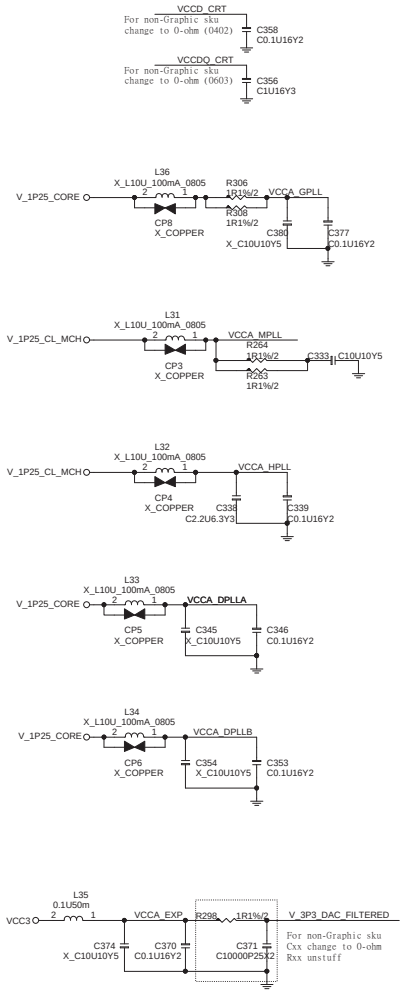
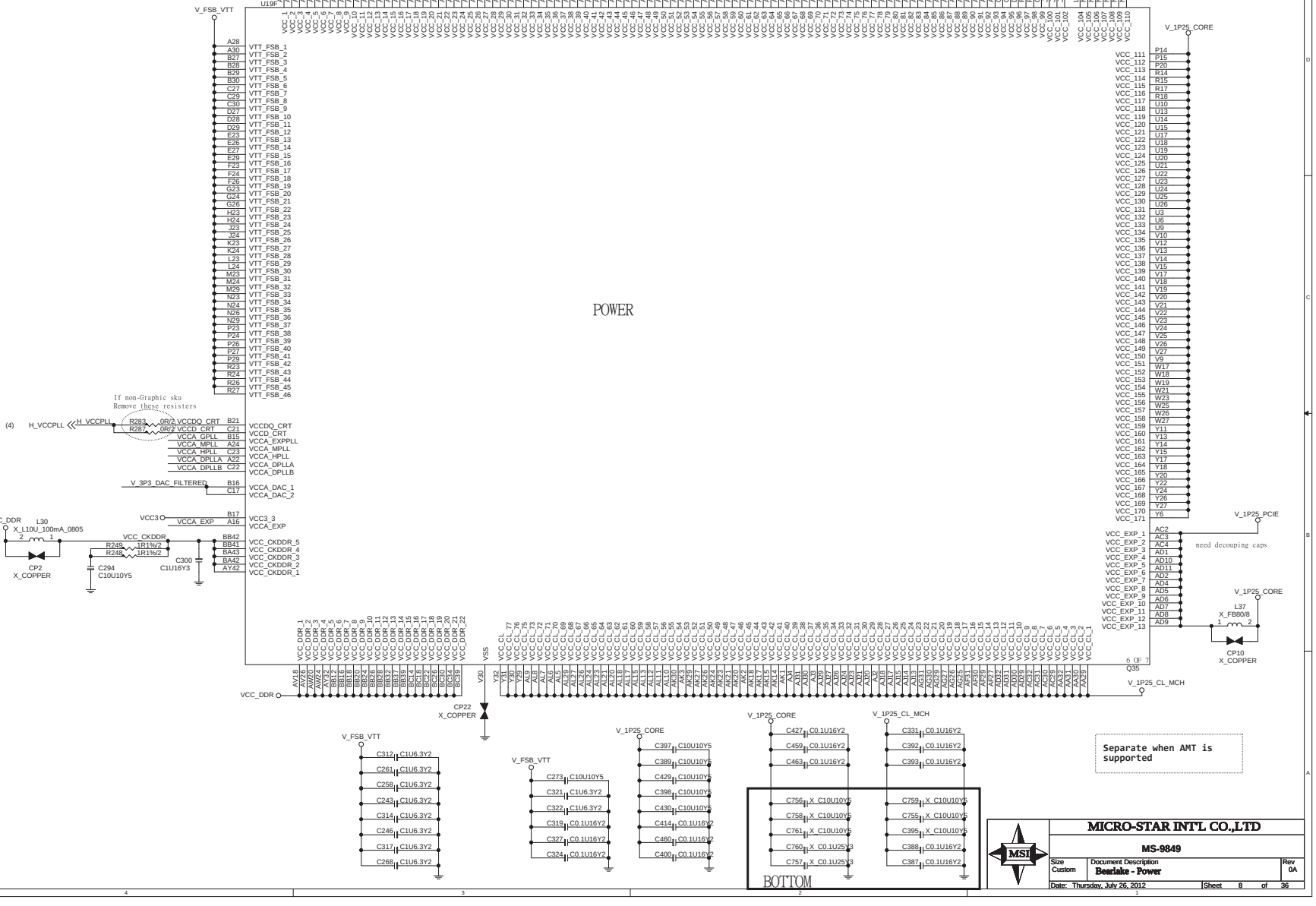


NB POWER





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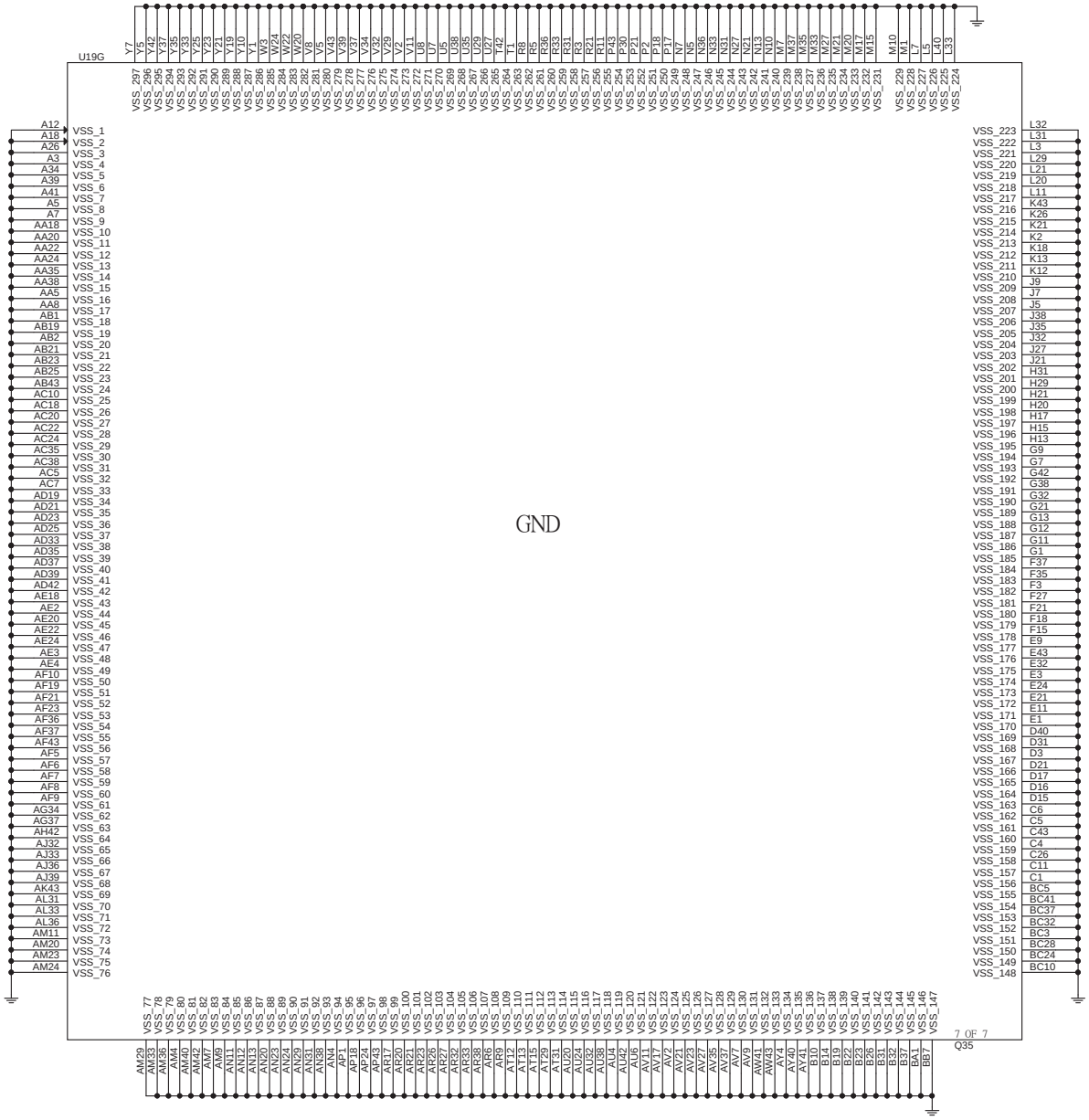

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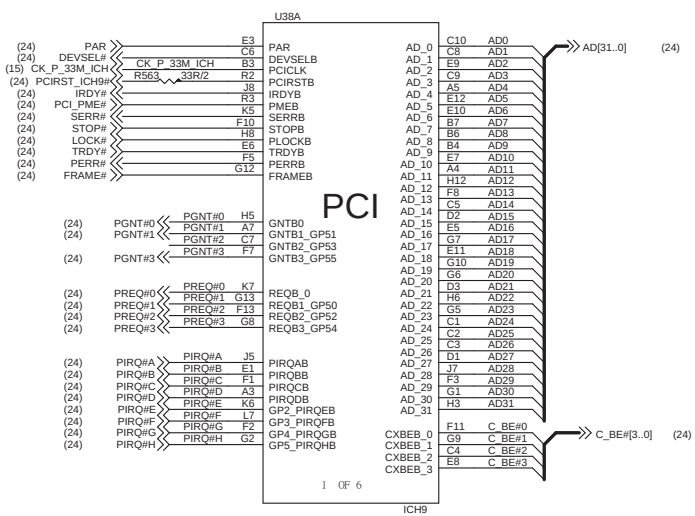
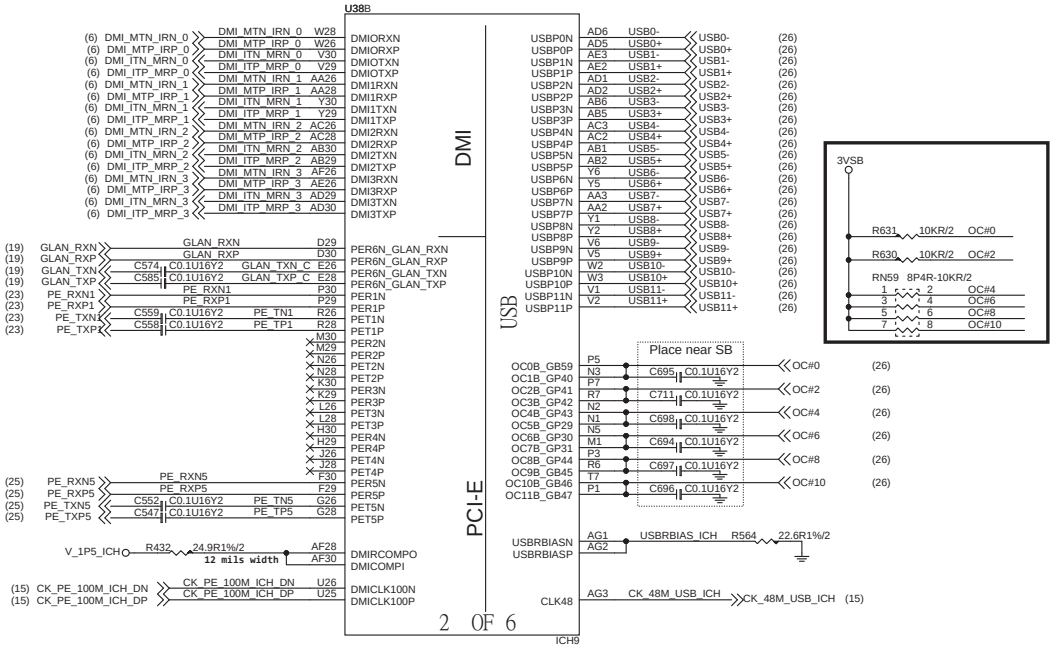
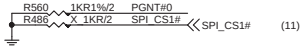


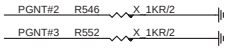


SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

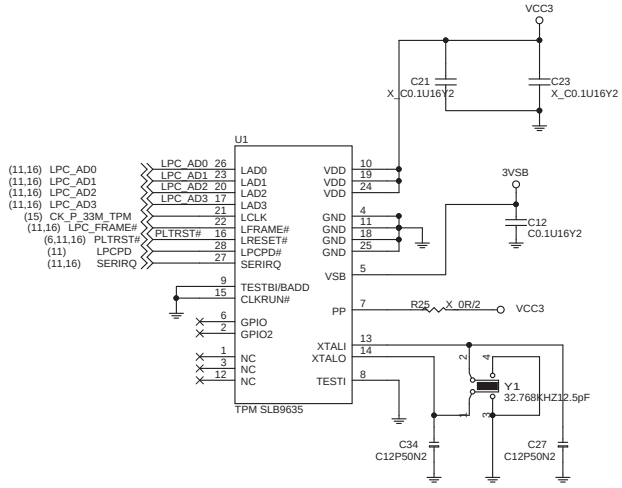
PGNT#[3:0]Internal Pull-up



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X

TPM - Security Controller



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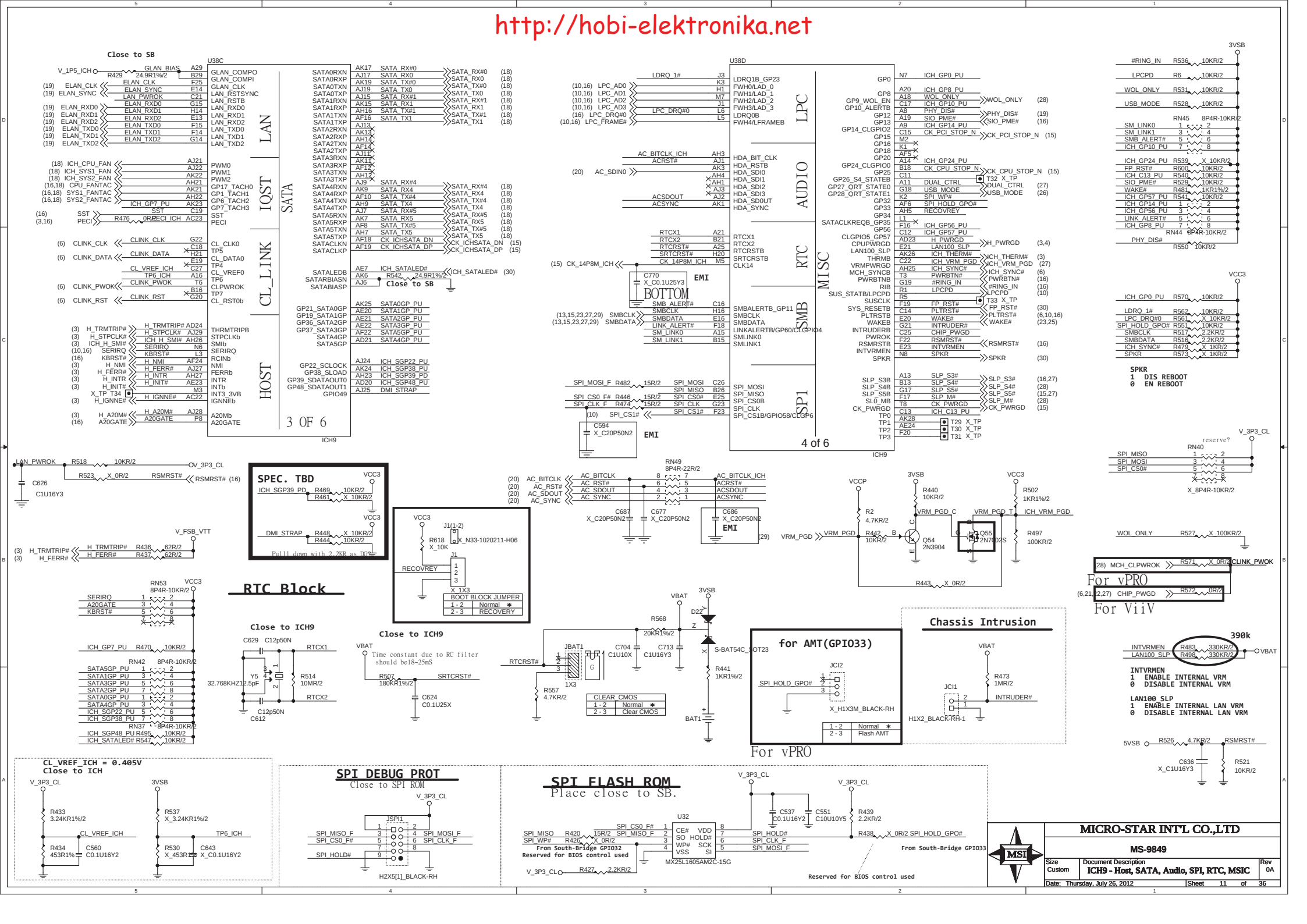
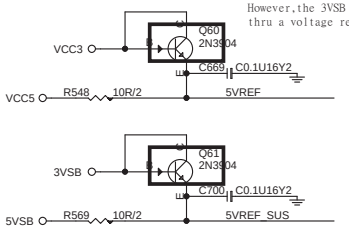
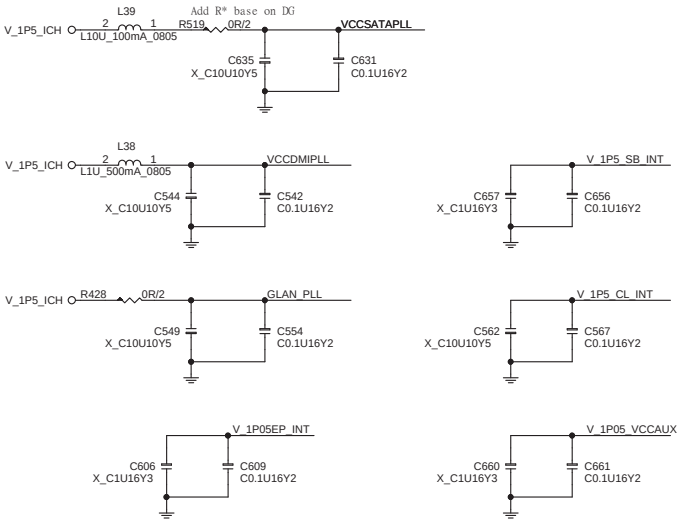


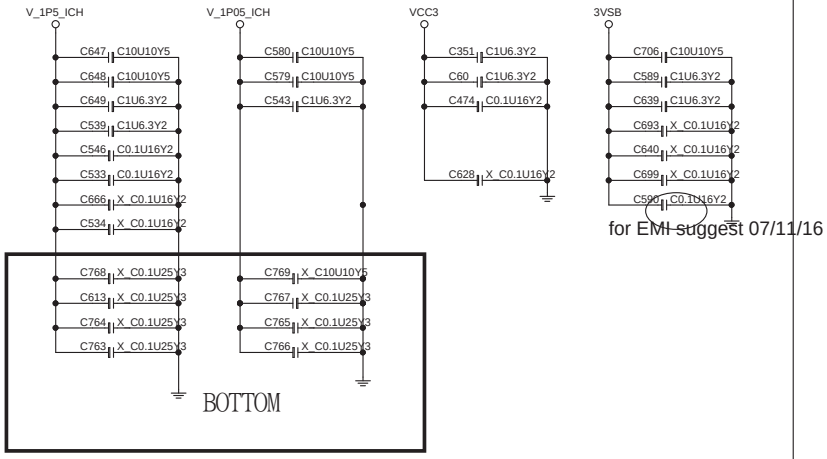
5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.

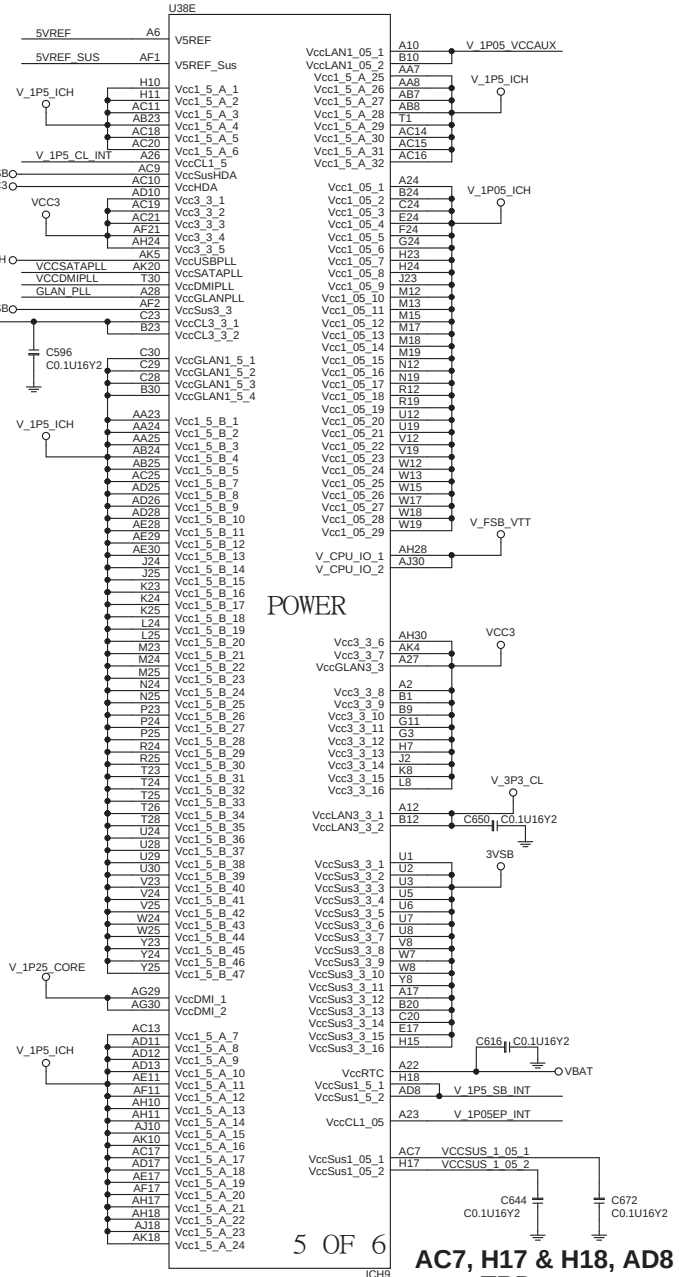


SB POWER

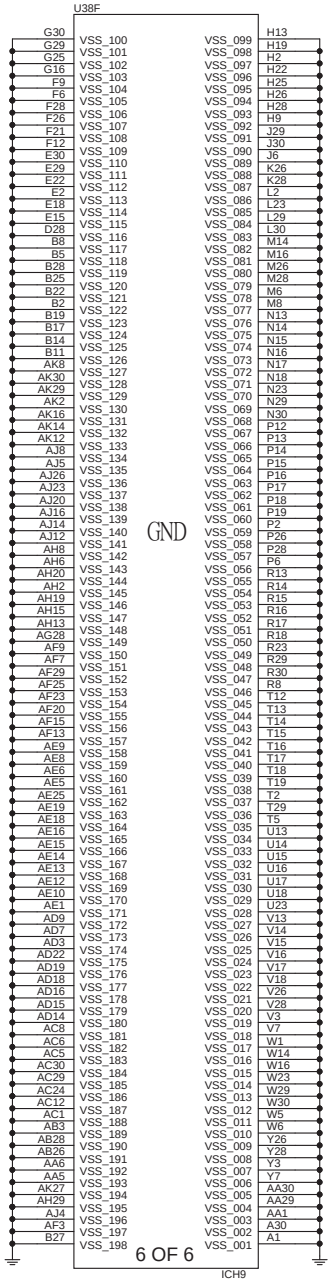




for EMI suggest 07/11/16



AC7, H17 & H18, AD8 spec TBD



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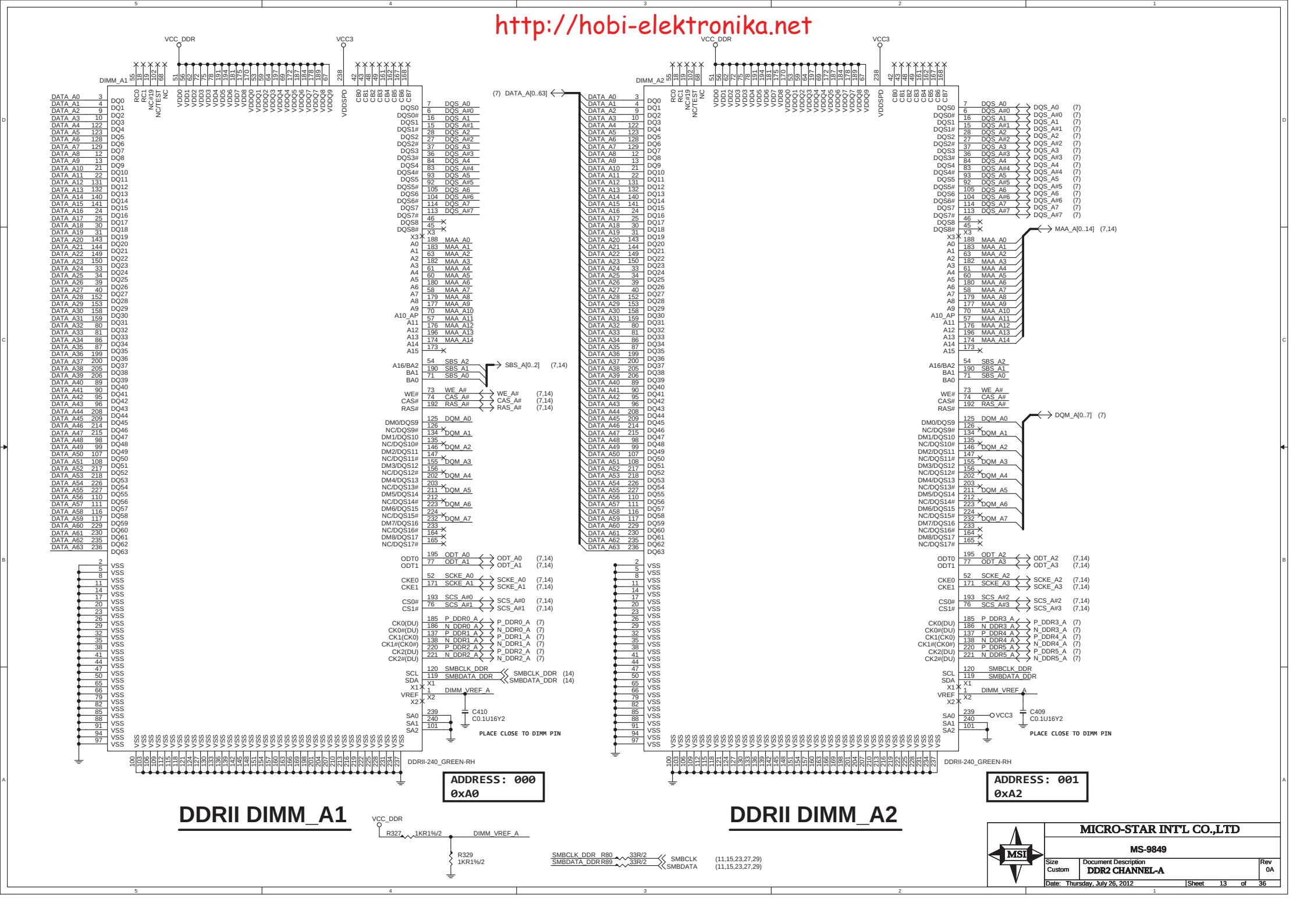

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Size	Document Description	Rev
Custom	DDR2 CHANNEL-A	0A

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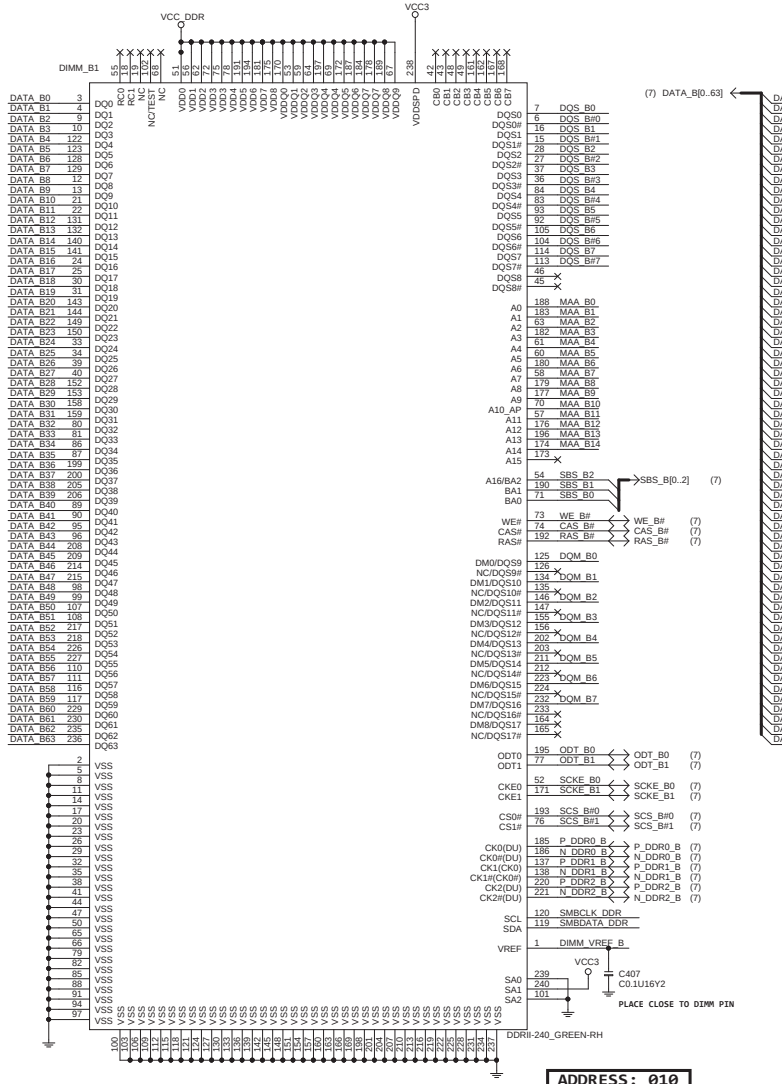
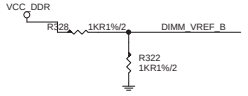
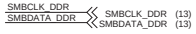
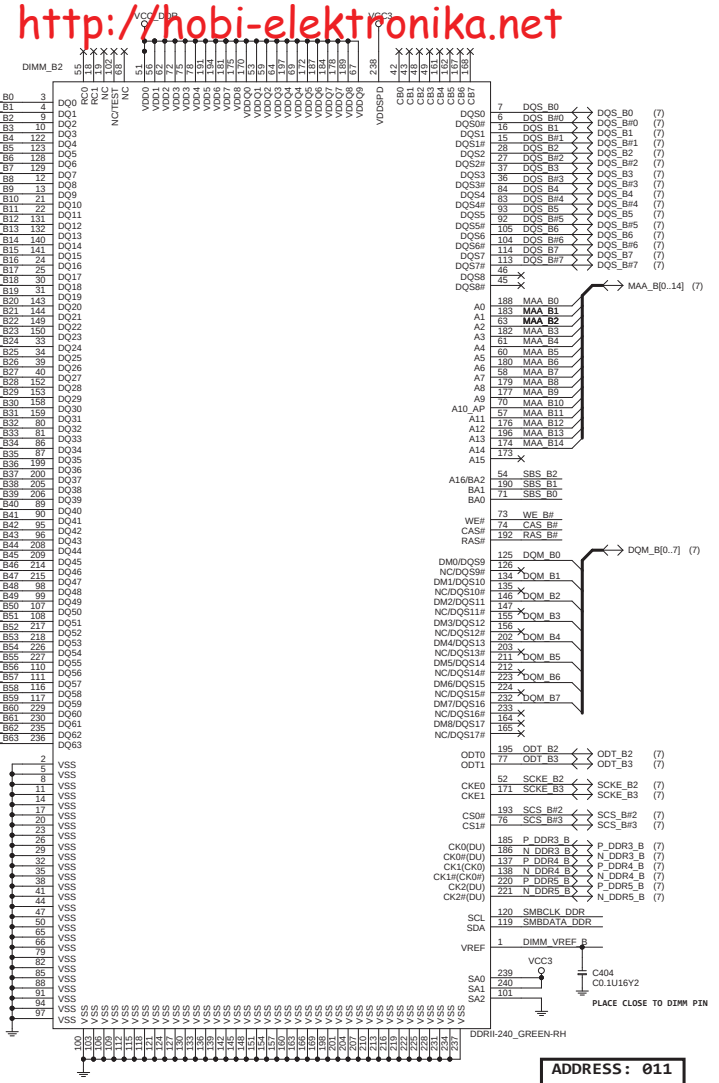


DDRII DIMM_B1

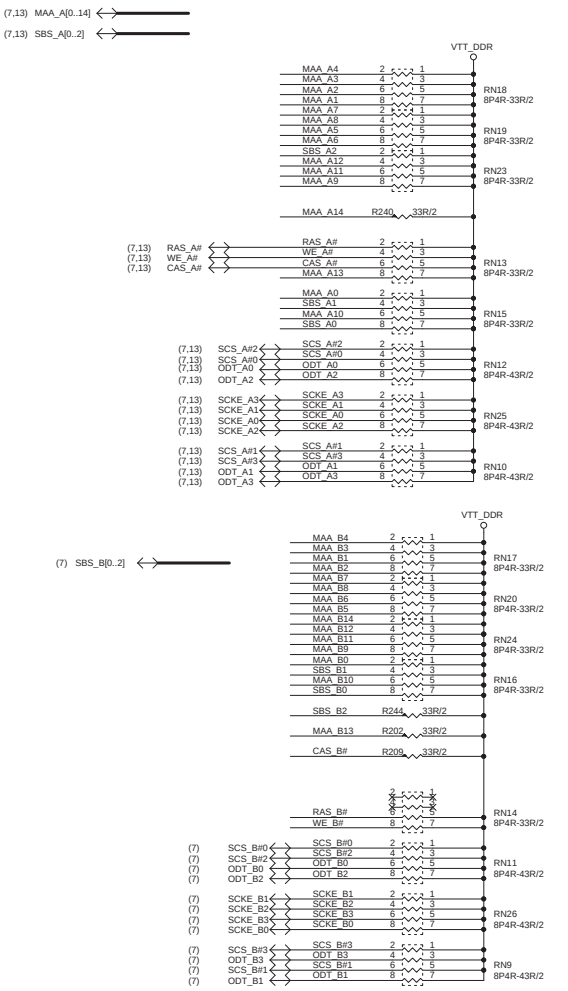






DDRII DIMM_B2

DDR II Termination



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Size: Custom	Document Description: DDR2 CHANNEL-B/DDR II Termination
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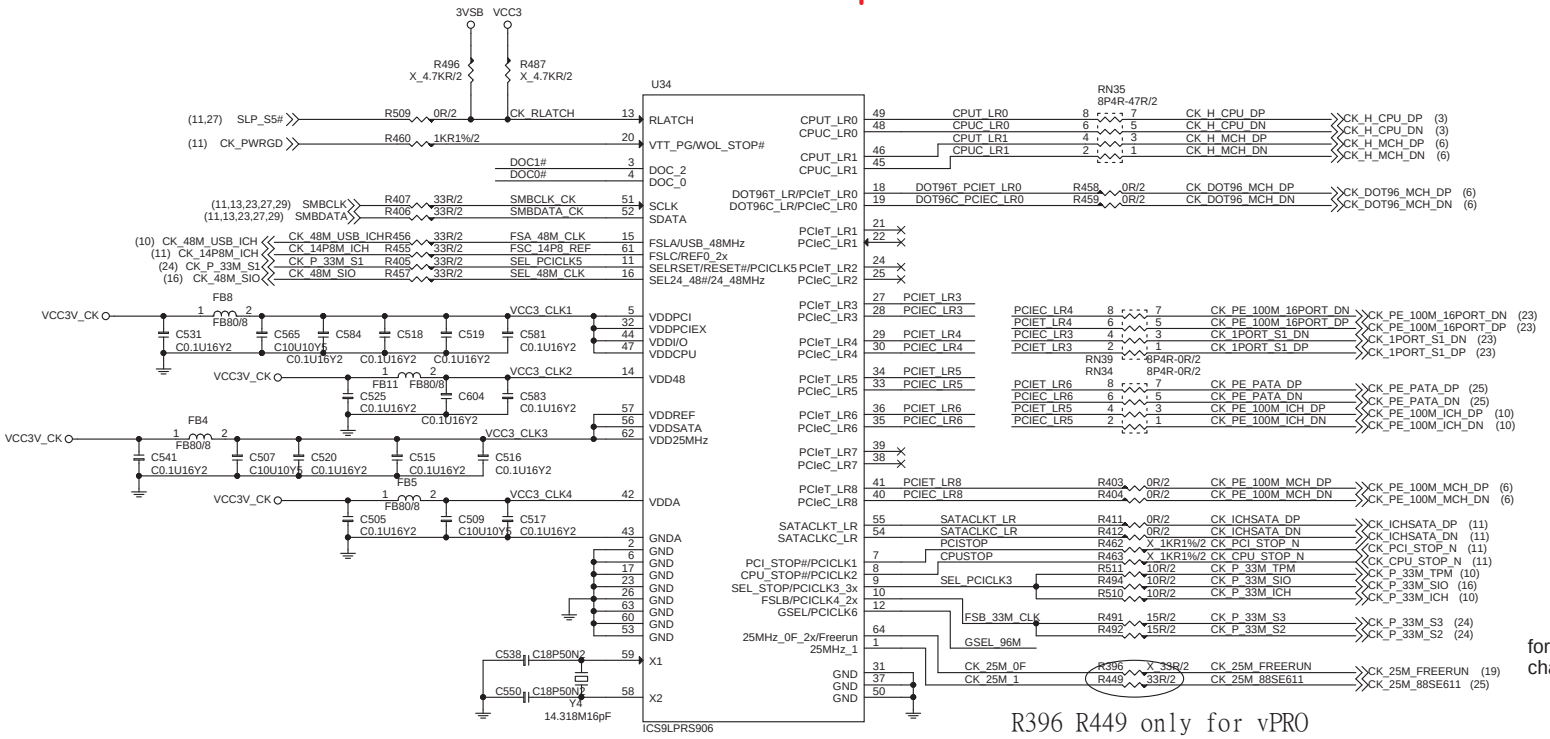
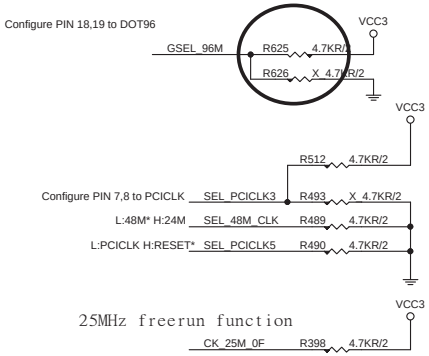
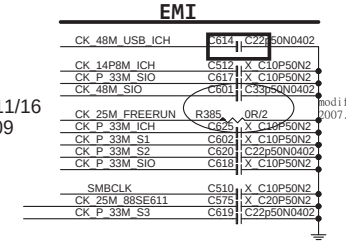


CLOCK GEN STRAPING



EMI

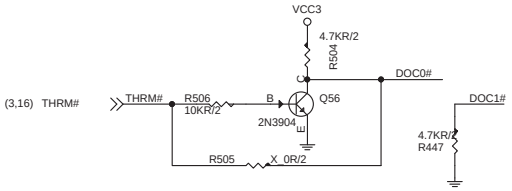


for EMI suggest 07/11/16
change C395 to R609

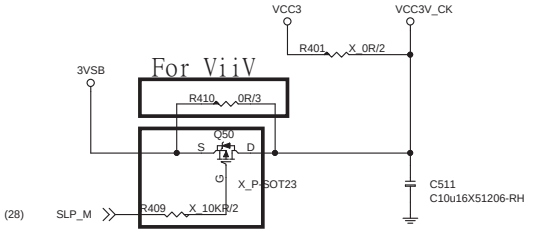
modify C490,c503 to 33pf for 2007.12.28

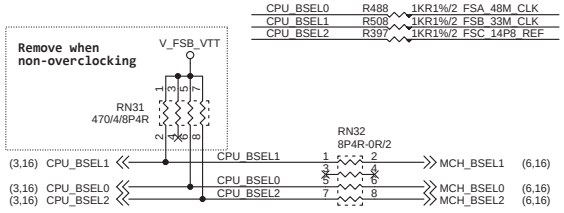
0	0	0	266 MHz (1066)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
1	0	0	333 MHz (1333)
1	1	0	400 MHZ (1600)

D.O.T



AMT POWER





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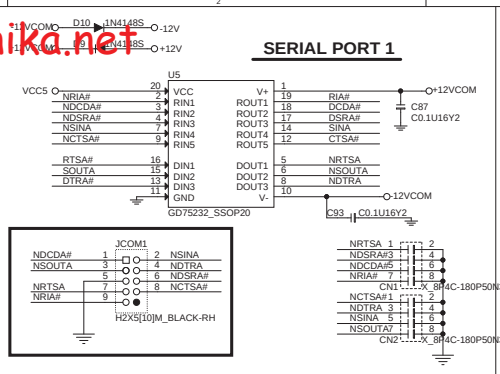
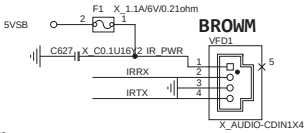
Remove serial port1 08/12/04

SERIAL PORT 1

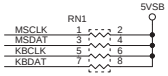


Front LCD (SERIAL PORT 2)

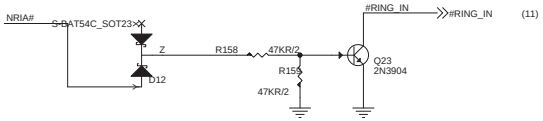


Remove FLOPPY CONNECTOR 08/12/04

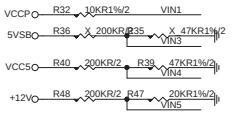
REMOVE PS2 KEYBOARD & MOUSE CONNECTOR

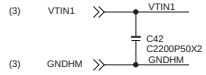


Ring IN Circuit



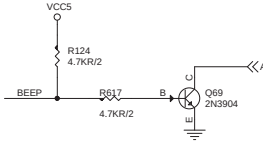
Thermal Resistor



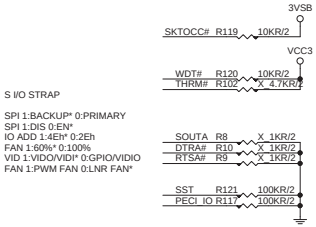


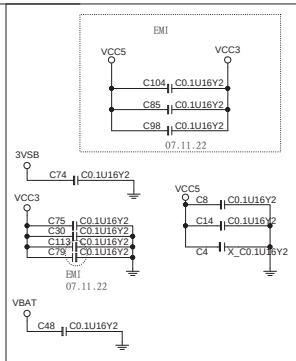
Remove parallel ports 08/12/04

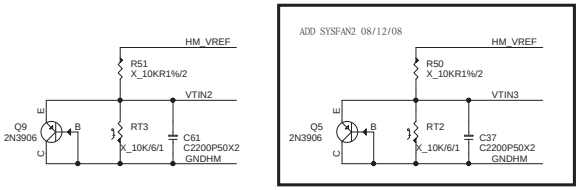
BEEP



LPC I/O STRAPPING RESISTOR







MICRO-STAR INTL CO.,LTD
MS-9849
Size: Custom
Document Description: SIO-Fintek F71882F/COM/LPT/FDD
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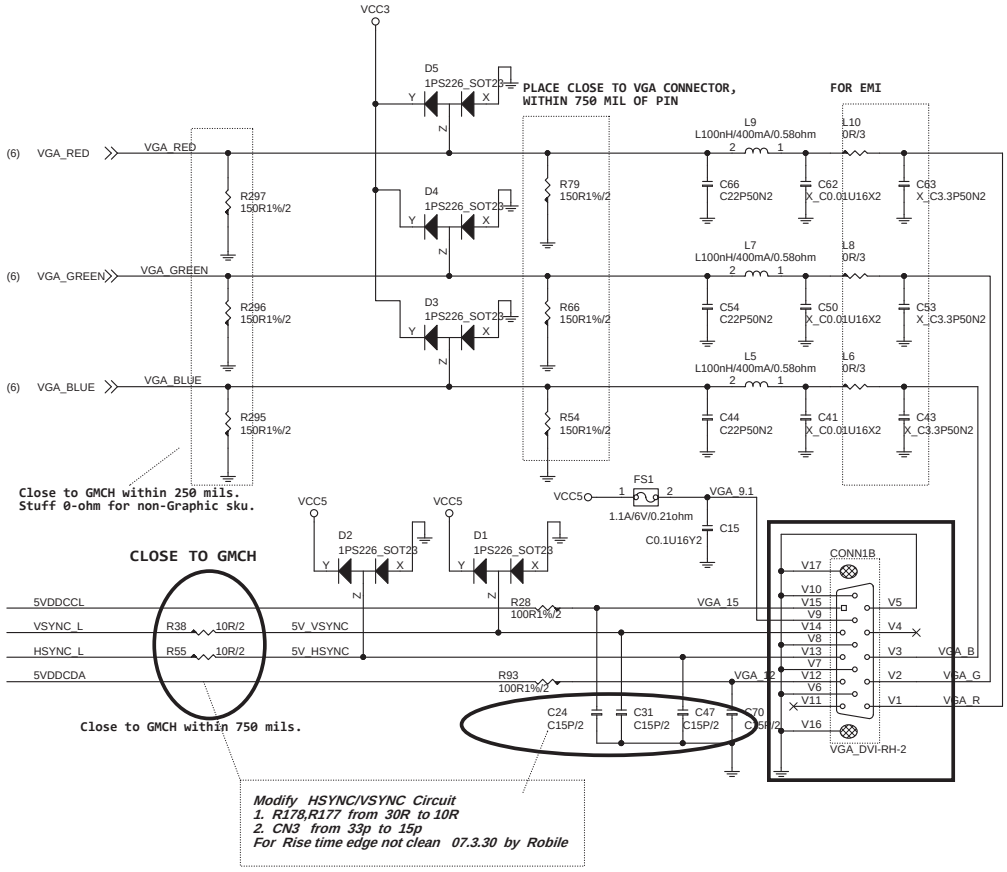
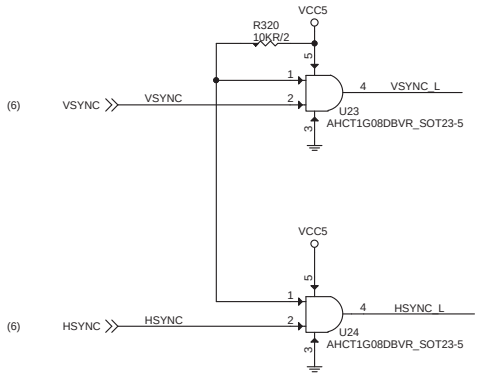
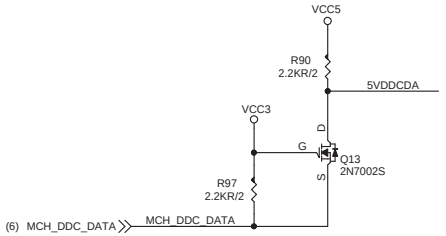
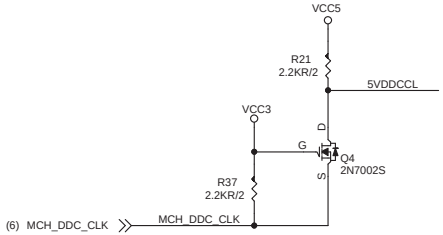
Video Connector









MICRO-STAR INT'L CO.,LTD		
MS-9849		
Size: Custom	Document Description: VGA	Rev: 0A
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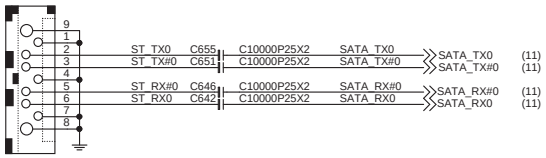
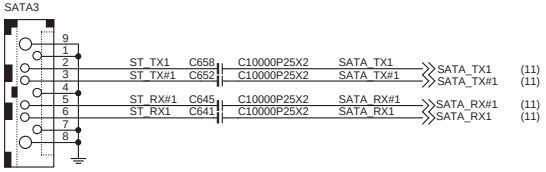
SATA2



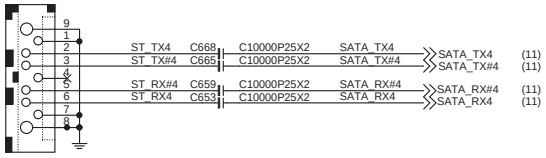
X_CONN-SATA10P_PURPLE

SATA3



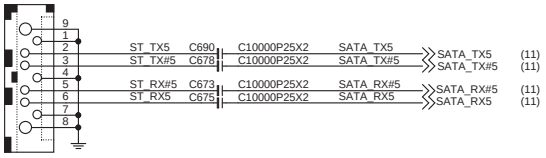
CONN-SATA10P_PURPLE

SATA1



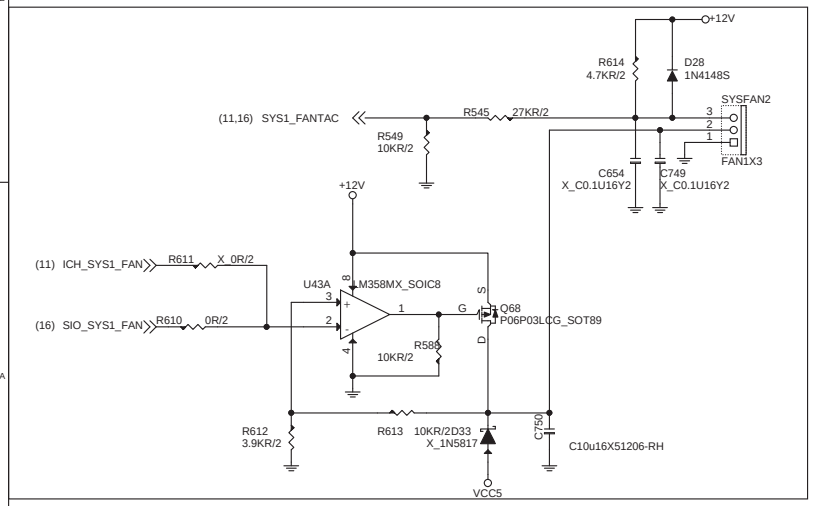
CONN-SATA10P_PURPLE

SATA4

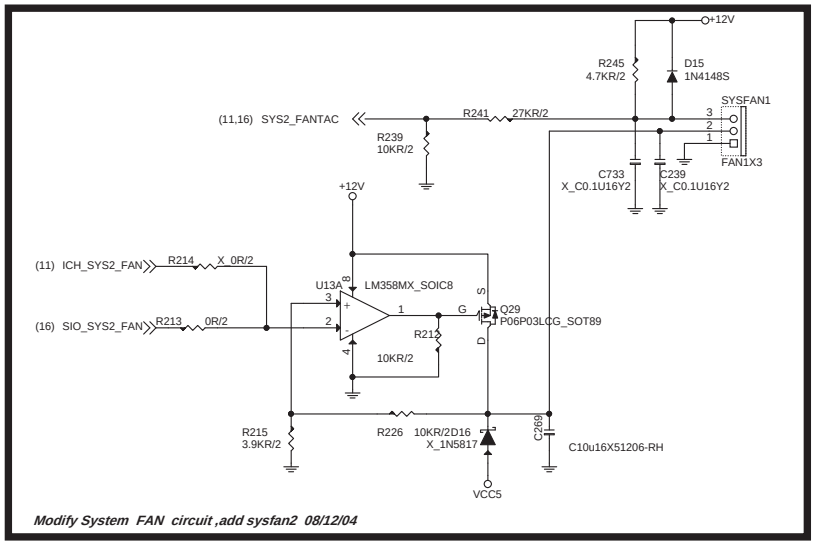


X_CONN-SATA10P_PURPLE

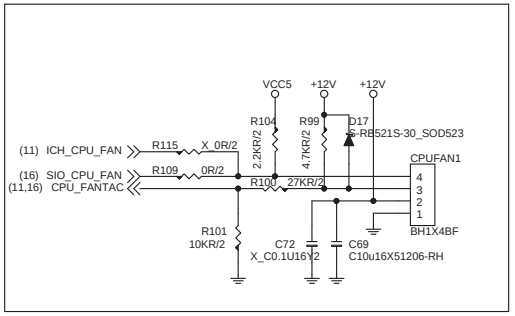
FAN-COUNTROL CIRCUIT



Modify System FAN circuit & Remove PWR_FAN for spec need 3pin DC Smart FAN 07.3.30 by Robile



Modify System FAN circuit ,add sysfan2 08/12/04



MICRO-STAR INT'L CO.,LTD

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Custom	SATA Ports and Fan Control	0A

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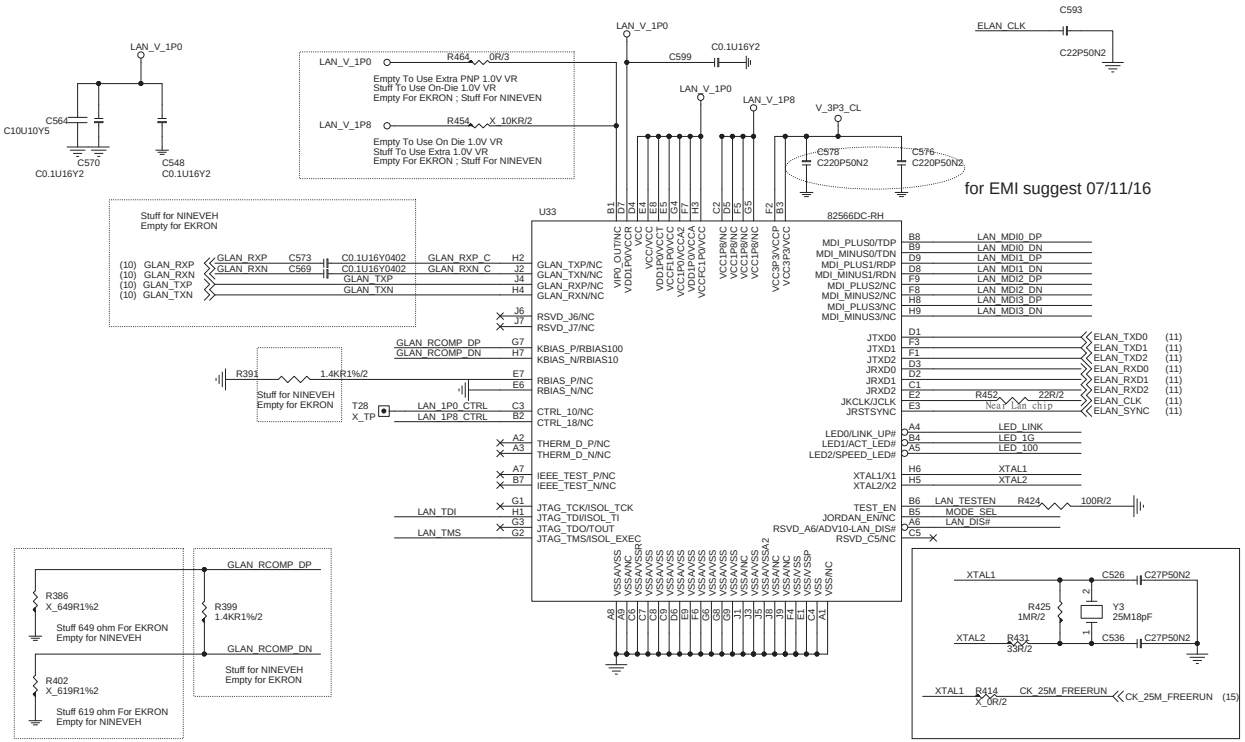
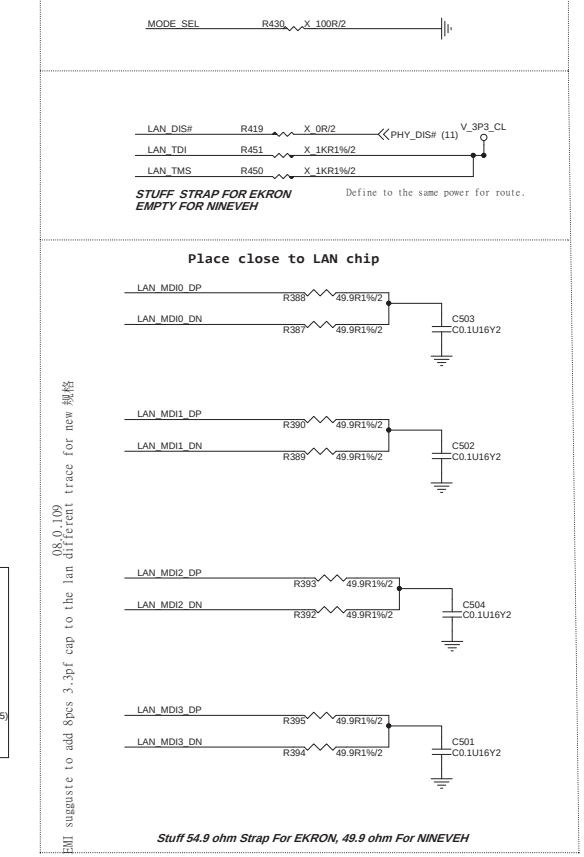
LAN - NINEVEH/EKRON

Change LAN chip to 82566DC,LAN Conn to N58-22F0221-S42 08.12.04





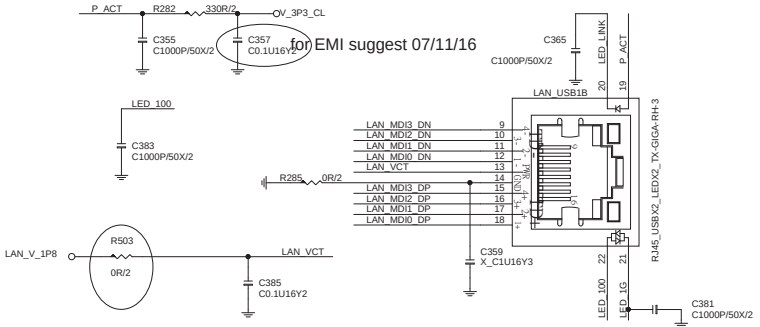
Intel 82556DM
For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multiport teaming,RSS,Intel Stable Image Platform Program drivers.
Intel 82556DC
For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
Basic 10/100 Ethernet connection.

B06-8256605-IY6
FOR NECP CONSIGN,CHIP LAN,INTEL/82566DM,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256615-I06
,CHIP LAN,INTEL/82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256205-I06
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

LAN CONNECTOR

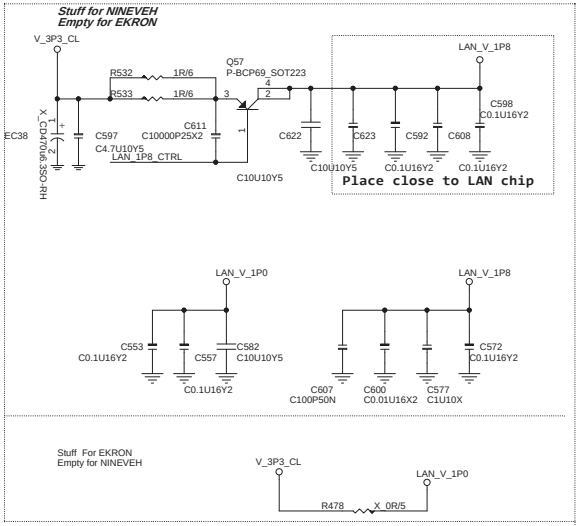


Speed LED Type
1000Mbps : Orange
100Mbps : Green
10Mbps : LED off

YELLOW : For Active/Link

ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

Giga-Lan	10/100-Lan
N58-22F0221-S42	**N58-22F0061-S42** **N58-22F0061-F02**
Link Green Active Blinking 1000 Yellow 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19 — 20 Yellow	19 — 20 Yellow
21 Orange — 22 Green	21 — 22 Green



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Size: Custom	Document Description: LAN NINEVEH/EKRON
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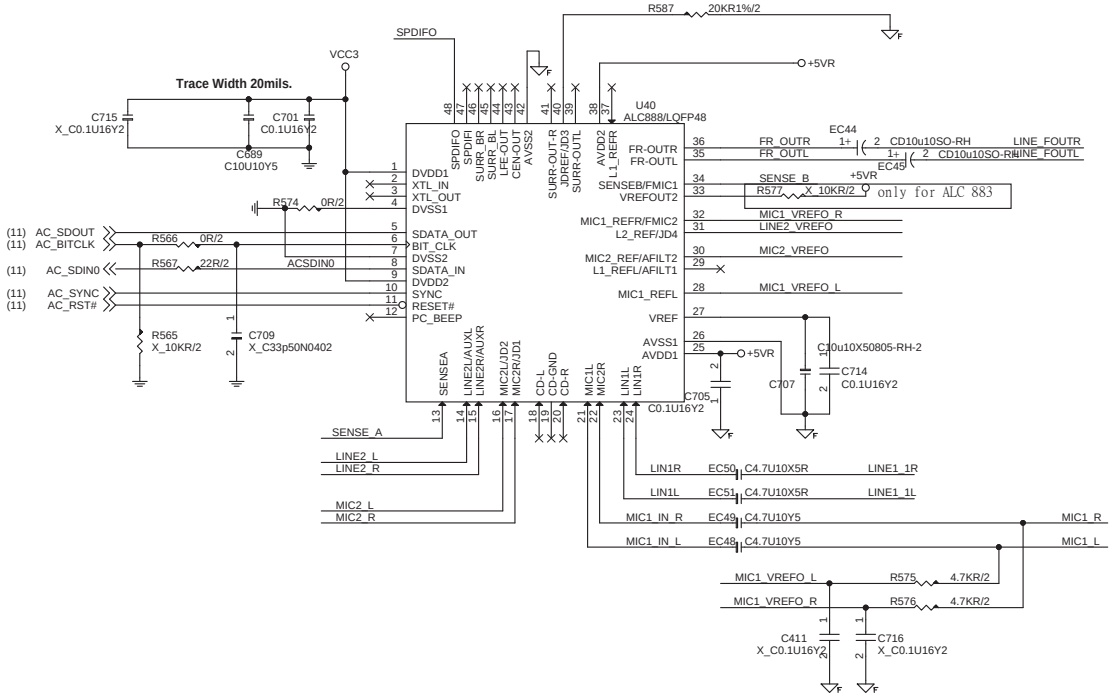
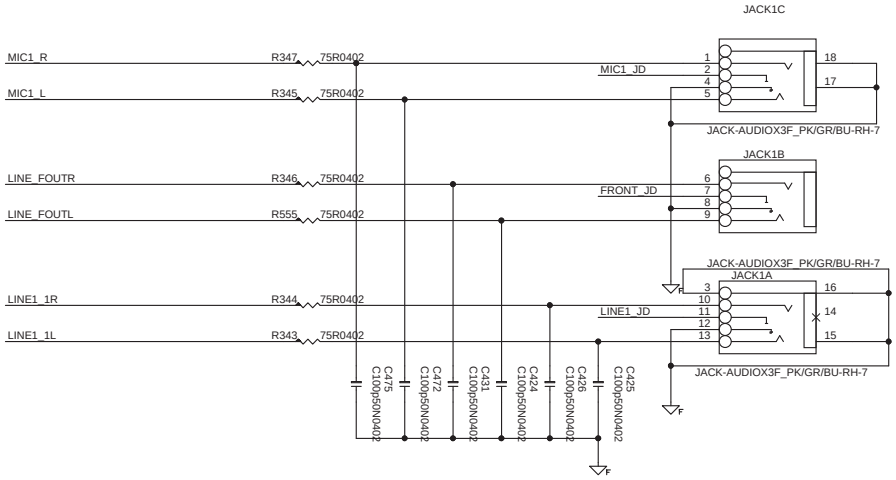
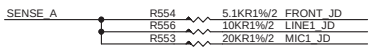
ALC888 CODEC



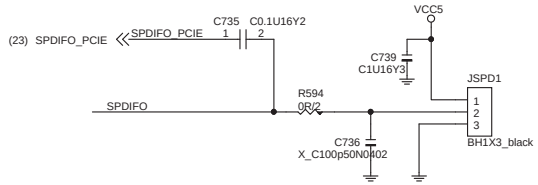
ALC888 JACK



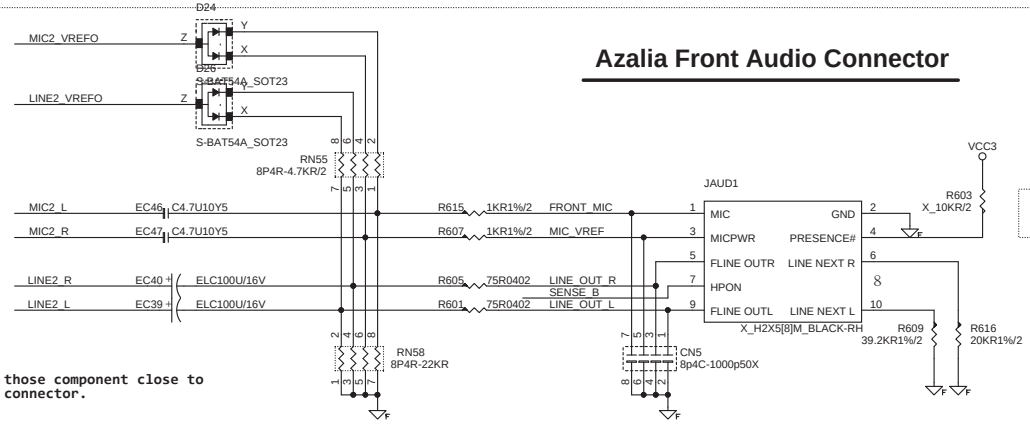
ALC888 JACK DETECT



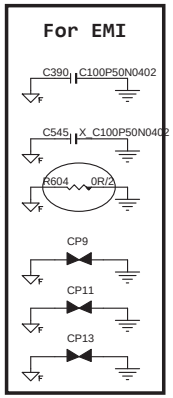
SPDIF_OUT



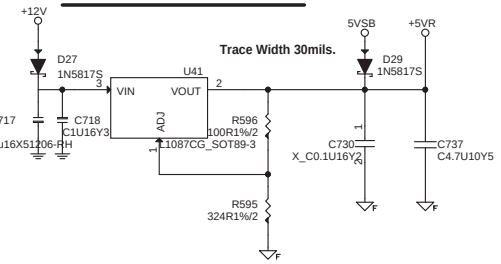
Azalia Front Audio Connector



for EMI suggest R498上件



AUDIO CODE REGULATORS



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-9849	
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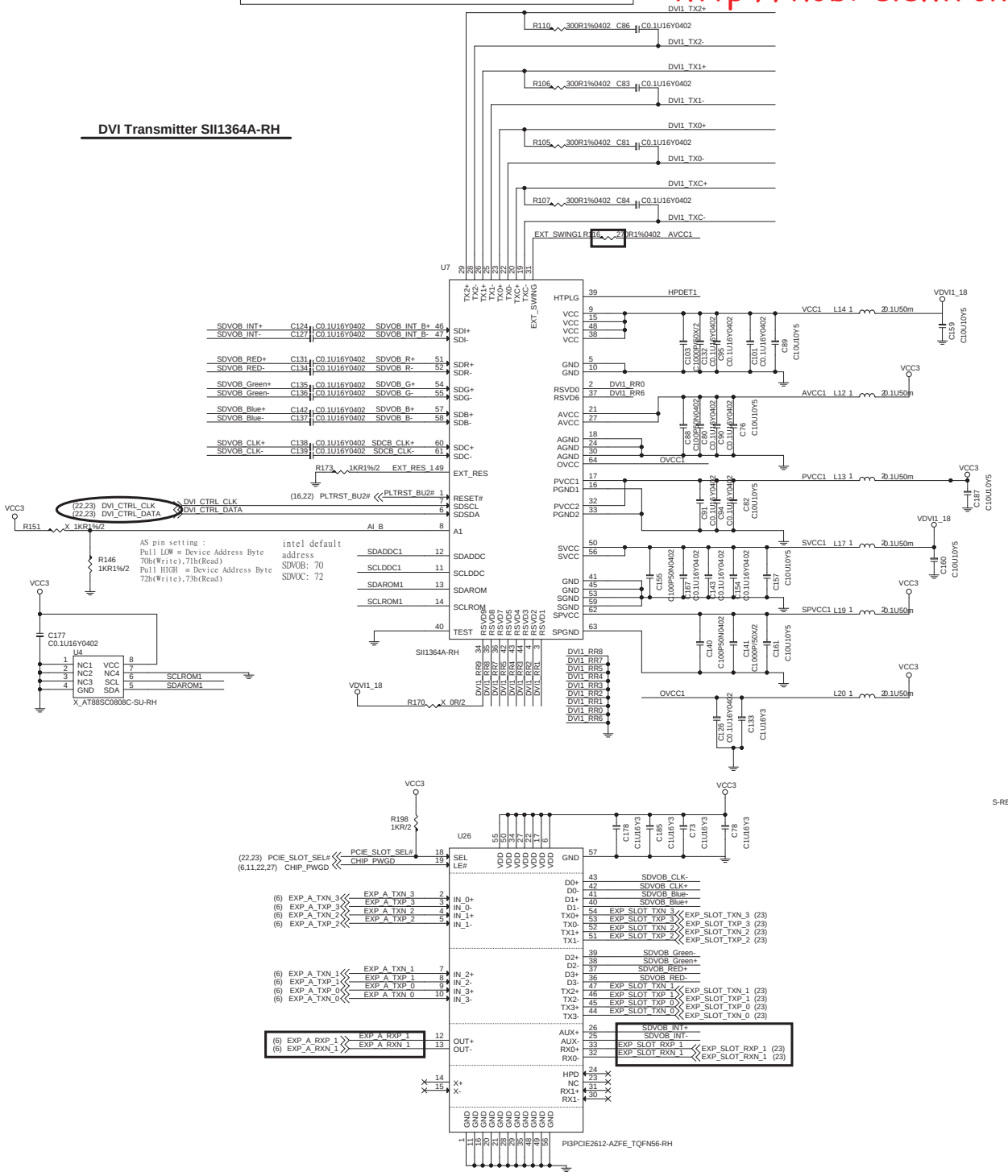
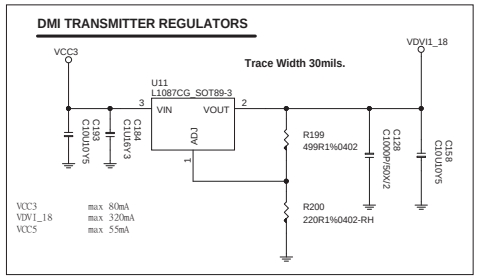
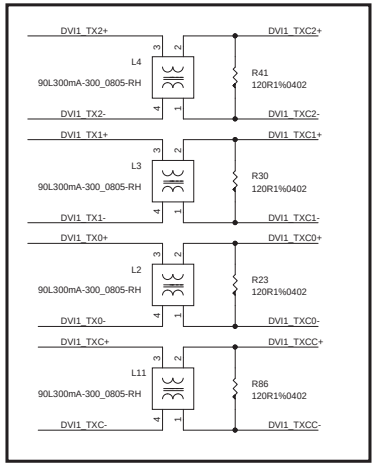
Change cap to C11-1042042-Y01 --090304

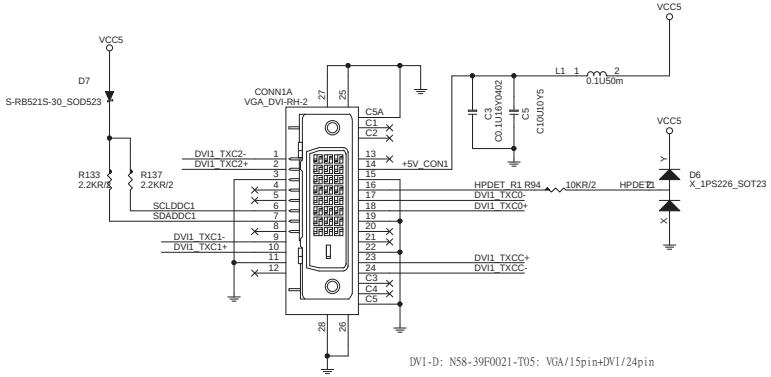
DVI Transmitter SII1364A-RH







FOR EMI 08/12/18



Title	DVI_1 SIL1364A	
Size C	Document Number MS-9849	Rev 0A
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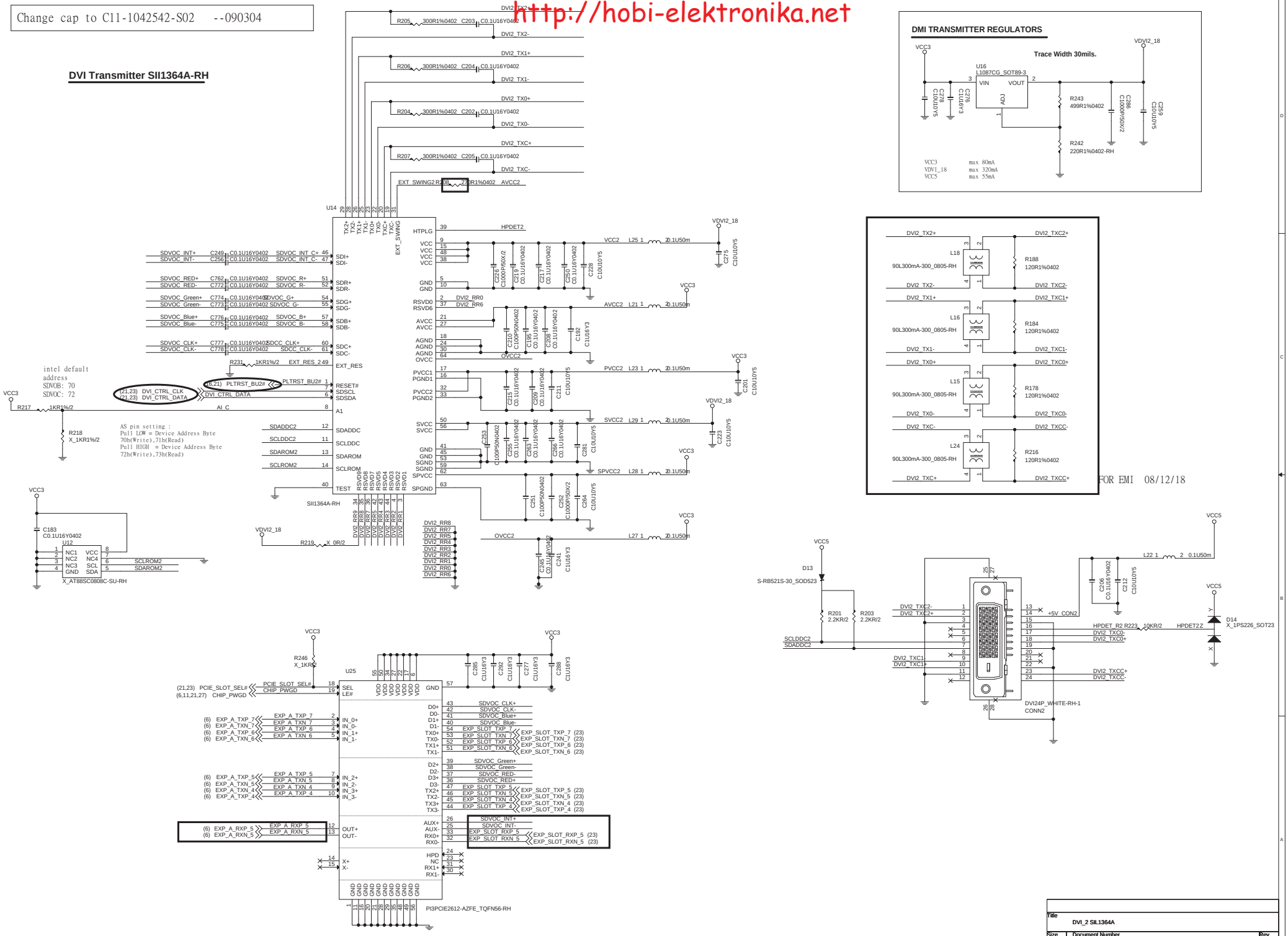
Change cap to C11-1042542-S02 --090304

DVI Transmitter SII1364A-RH

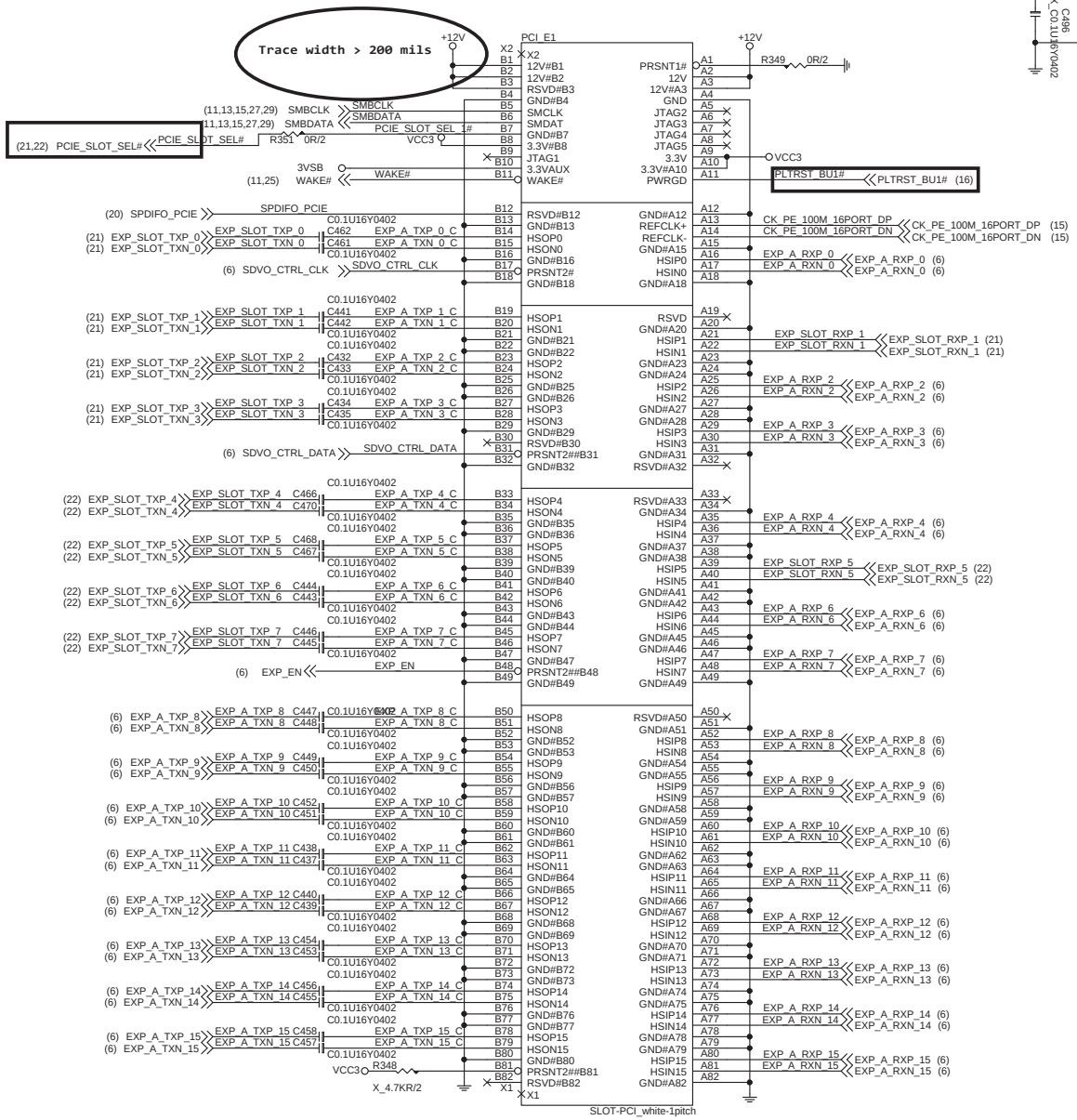


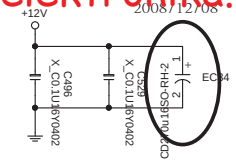
FOR EMI 08/12/18

Change cap to C11-1042542-S02
--090304

PCI_Express X16 Slot

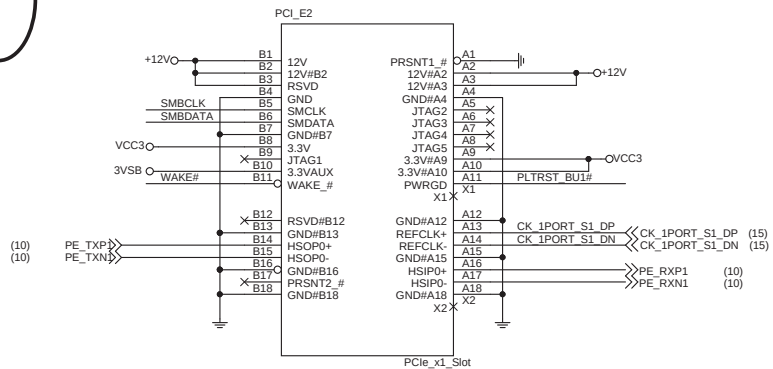
Trace width > 200 mils

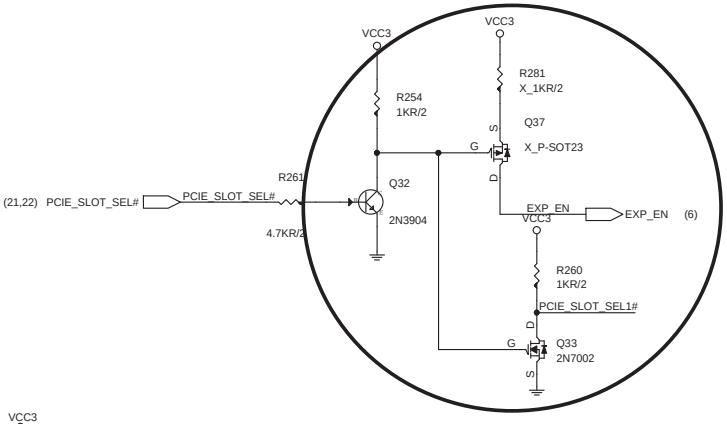


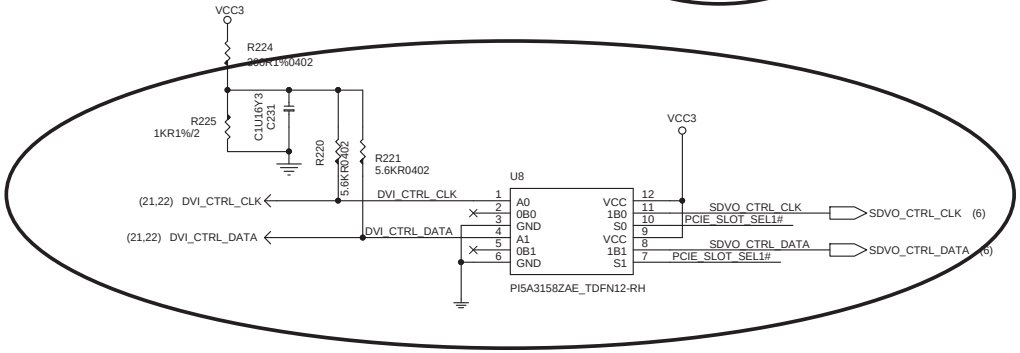


Delete PCI_E2
2008/12/08

PCI_Express X4 Slot
(Share with PCI_E x1 Slots)







modify SDVI IIC circuit to aviod PCIE x16 graphic card can't display issue
2008/12/08

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MS-9849		
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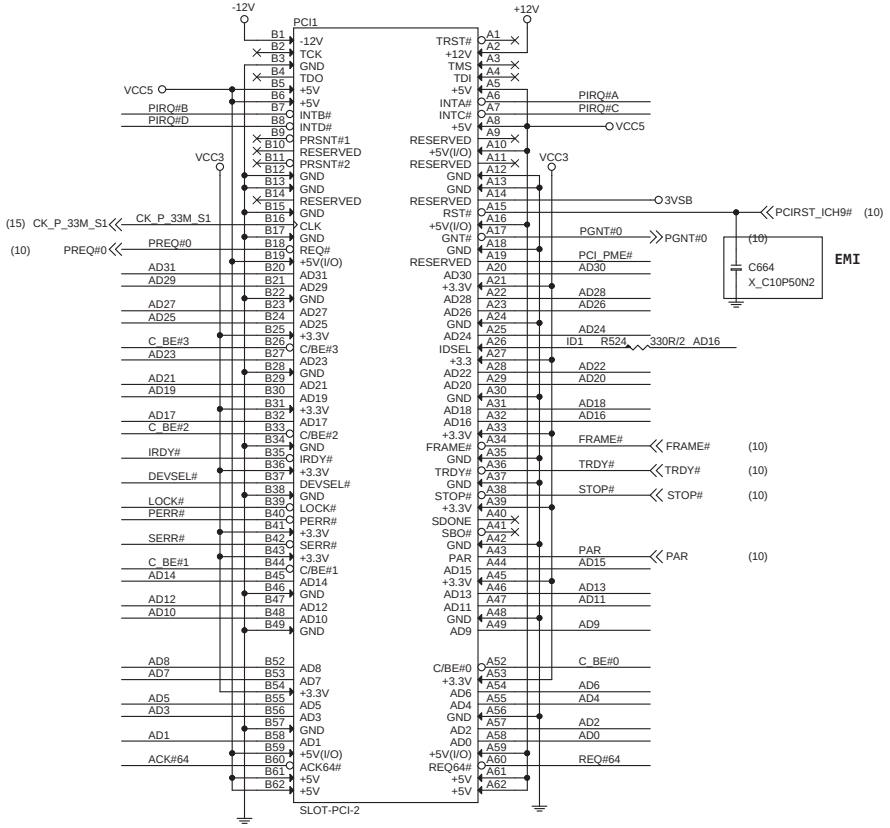
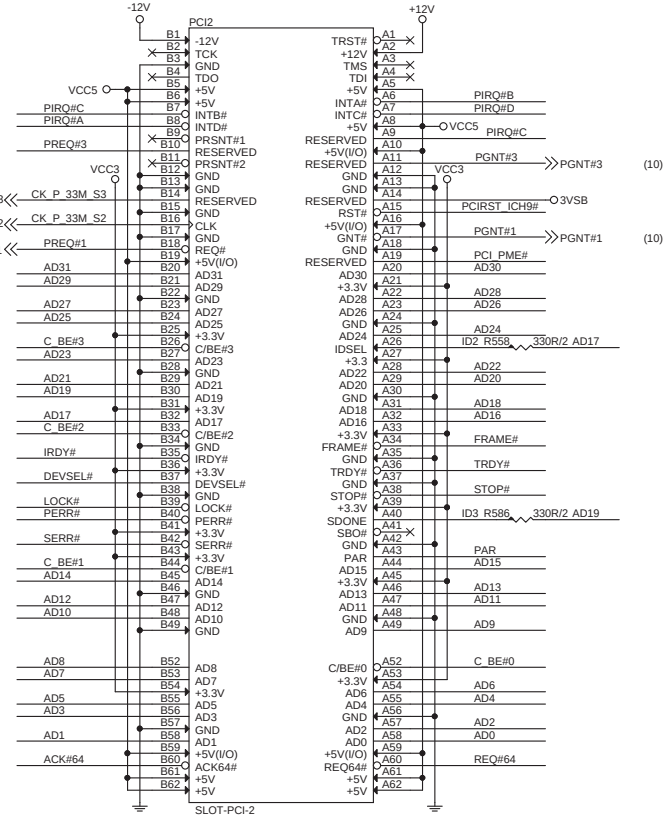
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

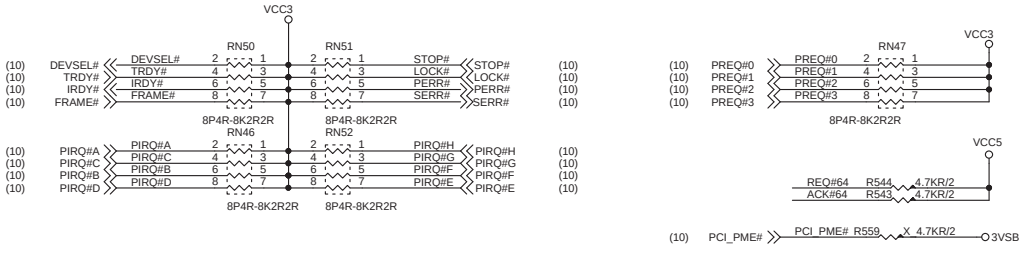
(10) AD[31..0]
(10) C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

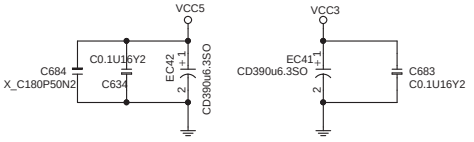


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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MS-9849		
Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 0A
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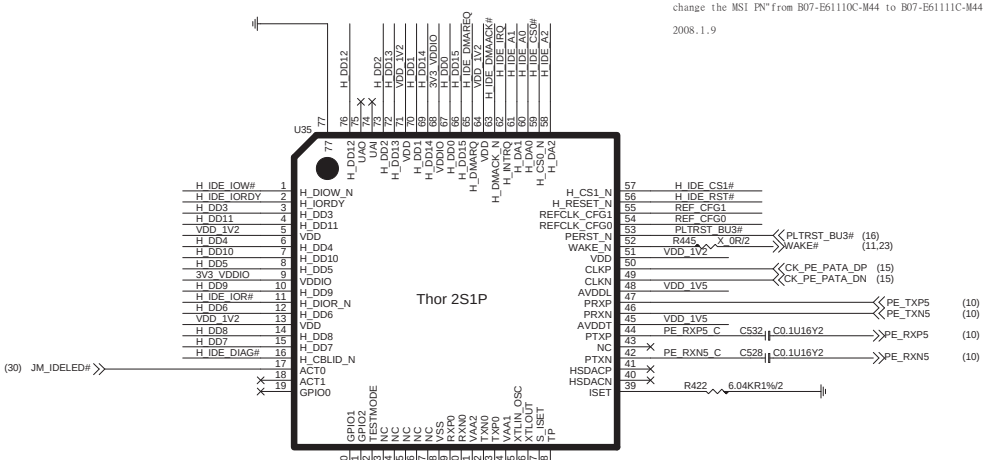
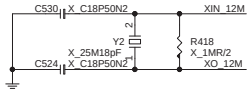
Hi-Speed PCIE to SATA/PATA Bridge

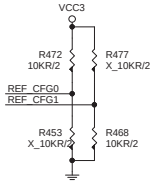
change the MSI PN"from B07-E61110C-M44 to B07-E61111C-M44

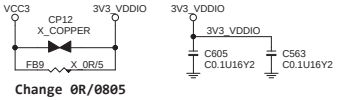
2008.1.9





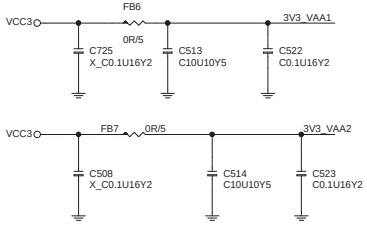
REF_CFG[1:0] =
00:20MHz
01:25MHz

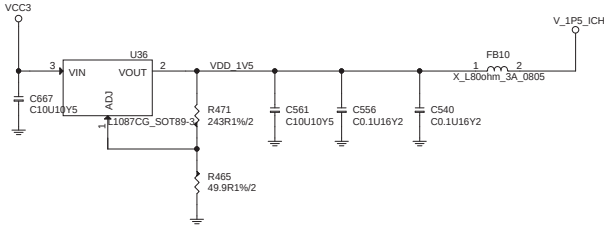


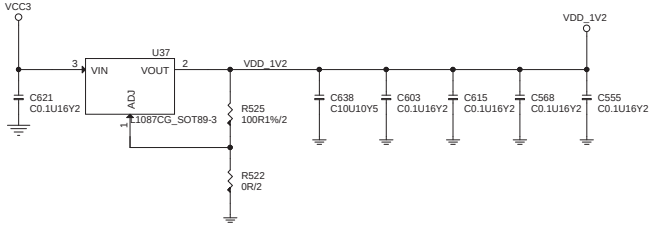


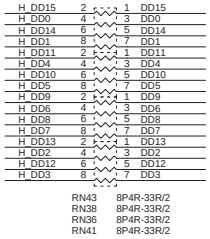
Change 0R/0805

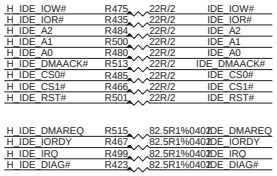
L02-8008074-J07 FOR BEAD

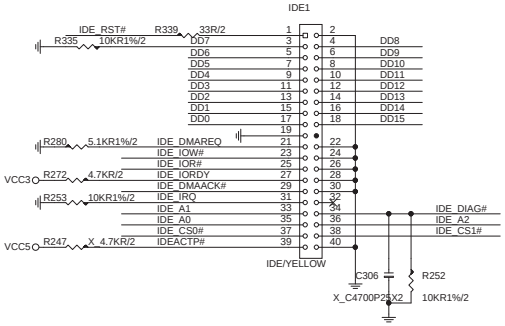












Remove SATA2 08/12/04

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Custom	Marvell 88SE6111 PCIE to PATA/SATA	0A

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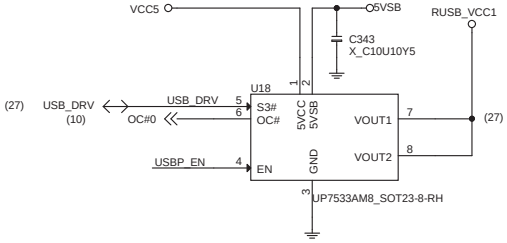
Rear USB Connector

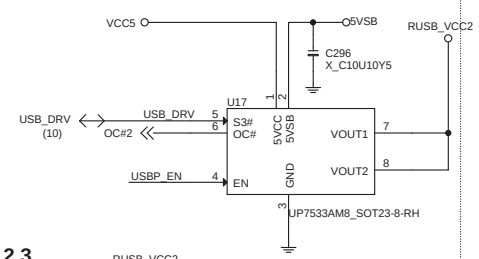
Front USB Connector

USB POWER FOR PORT 0,1



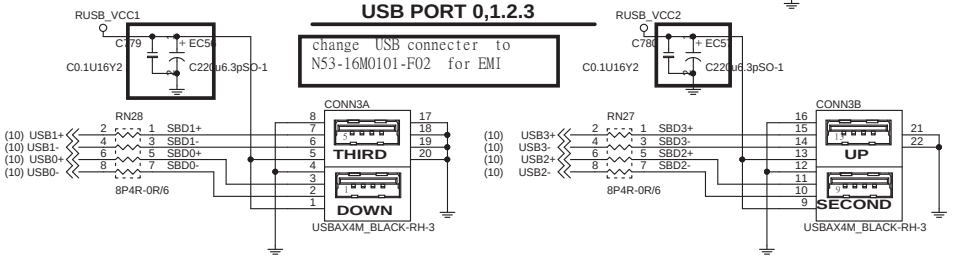
USB POWER FOR PORT 2,3,

NEAR CONNECTOR



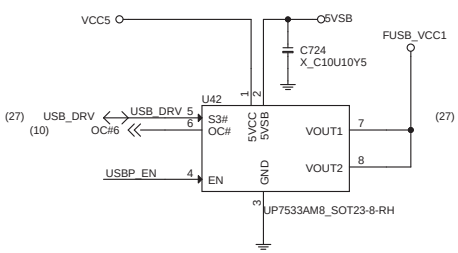
USB PORT 0,1,2,3

change USB connecter to
N53-16M0101-F02 for EMI



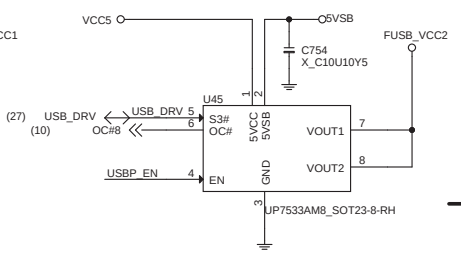
USB POWER FOR PORT 6,7

NEAR CONNECTOR

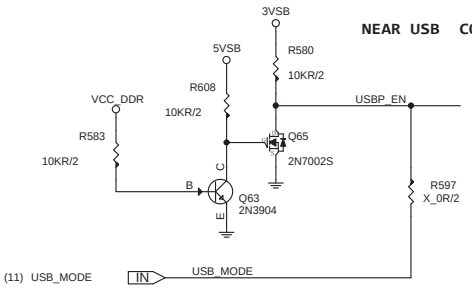


USB POWER FOR PORT 6,7

NEAR CONNECTOR

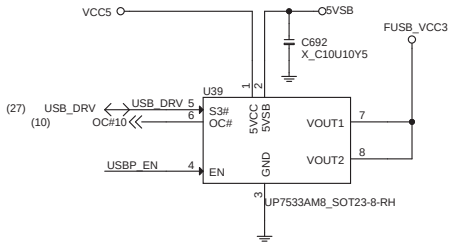


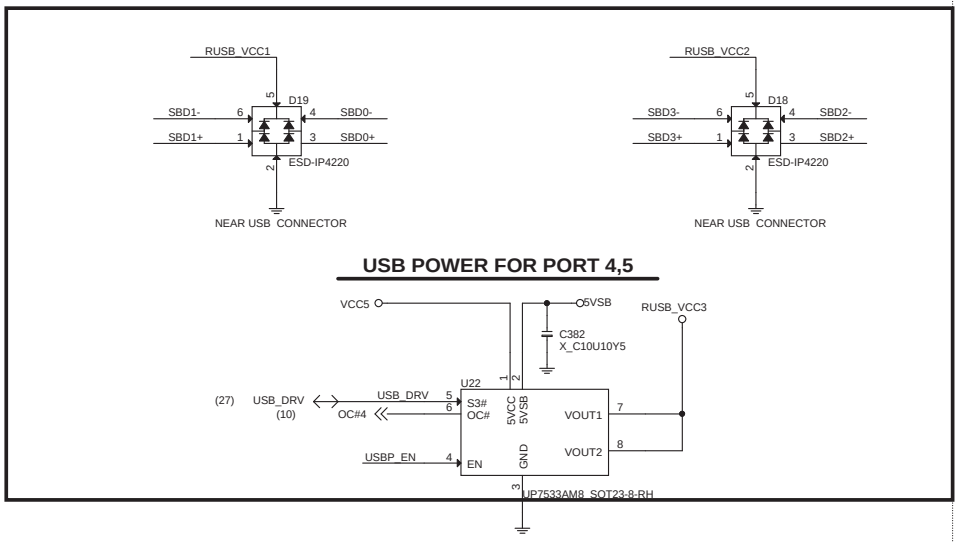
NEAR USB CONNECTOR



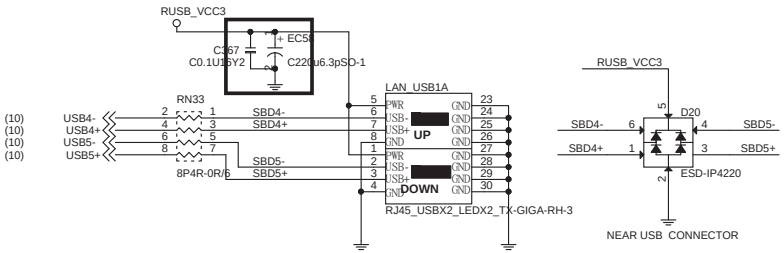
USB POWER FOR PORT 6,7

NEAR CONNECTOR

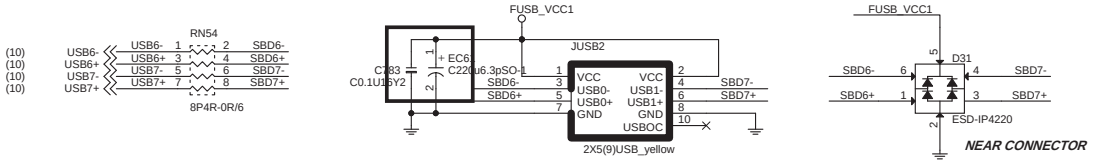




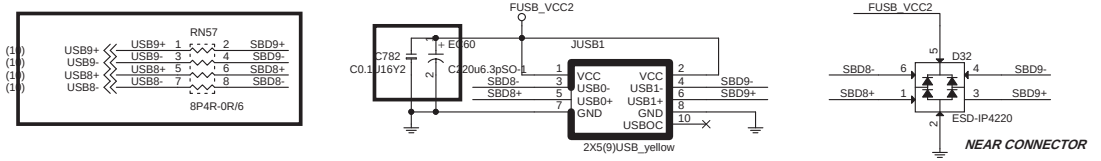
REAR USB PORT 4,5 (With LAN)



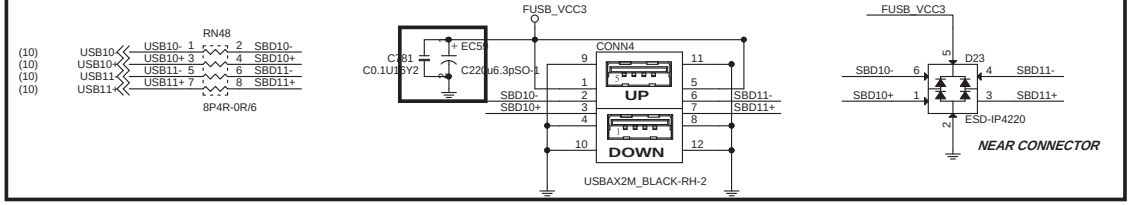
FRONT USB PORT 6,7



FRONT USB PORT 8,9



FRONT USB PORT 10,11



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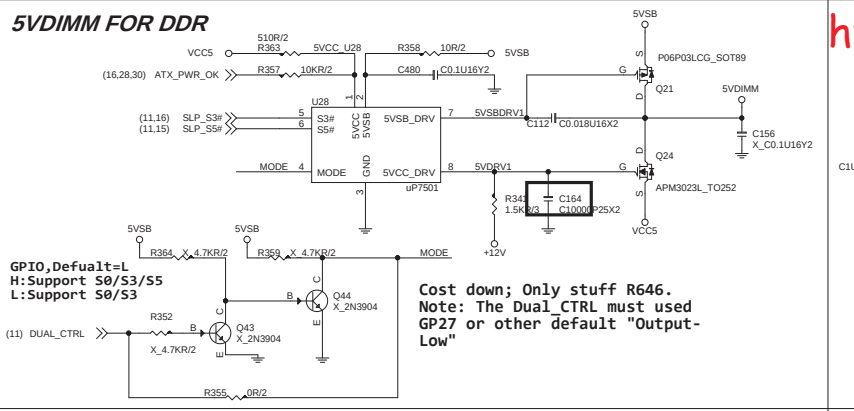
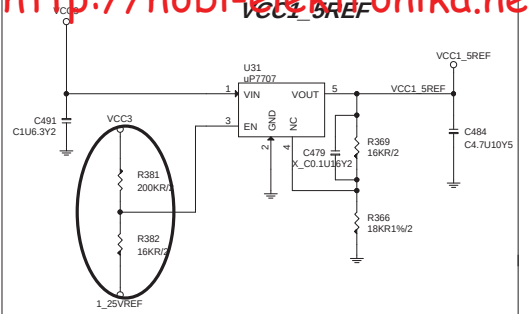
5VDIMM FOR DDR



GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3

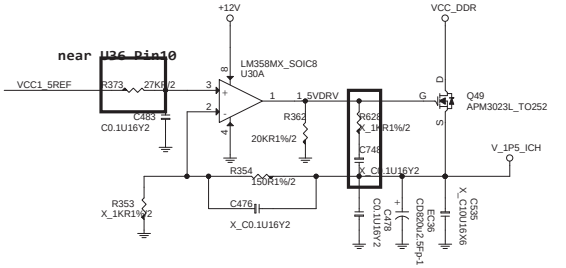
Cost down; Only stuff R646.
Note: The Dual_CTRL must used GP27 or other default "Output-Low"

VCC1_5REF

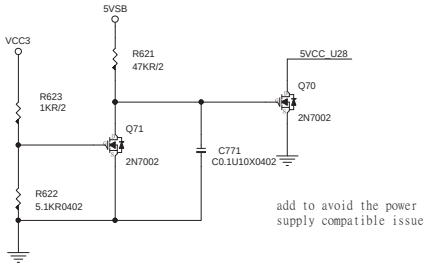


Let 1.25V and 1.5V at the same tine power up or power down

SB 1.5V 2.75A



Change EC44
from 1000uf to 820uf
07.11.26



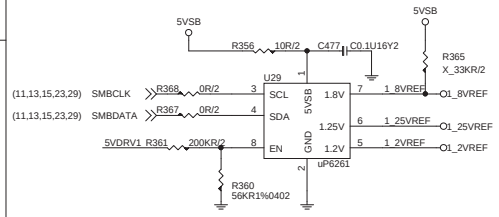
add to avoid the power supply compatible issue

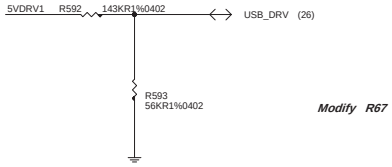
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable

Stuff R361 to prevent the source current not enough issue (5.1-1.8)/33K=100uA

reference Voltage

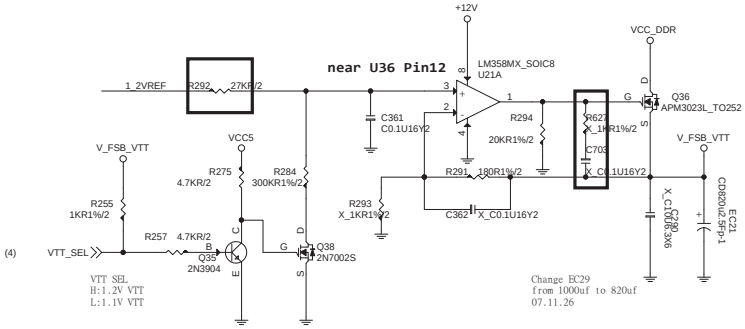
DDR REF
NB 1.25V REF
V_FSB_VTT REF





Modify R67 from 4.7K to 20K 07.3.30 by Robile

1.2V 5.8A

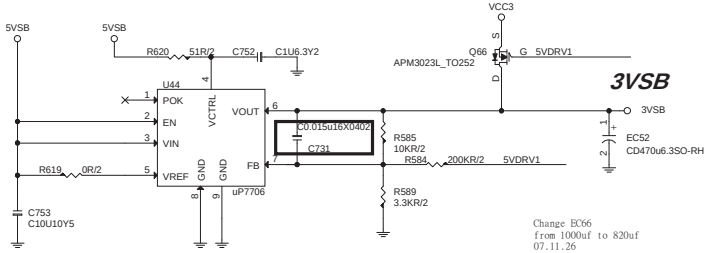


VTT SEL
H:1.2V VTT
L:1.1V VTT

Change EC29
from 1000uf to 820uf
07.11.26

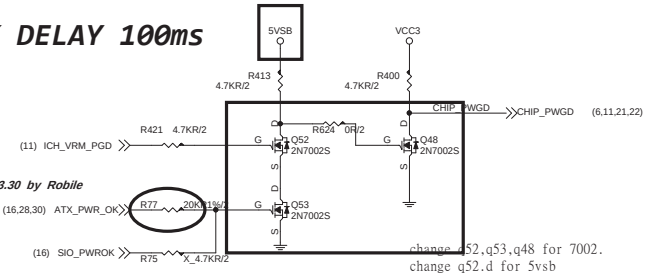
Modify This Page Circuit 07.3.30 by Robile
1. add R607 for Q35 turn on using
2. change C652 from 0.018u to 2200p & stuff
3. change R114 from 10K to 10R
4. change R132 from 0402 1K to 0603 1.5K

3VSB



Change EC66
from 1000uf to 820uf
07.11.26

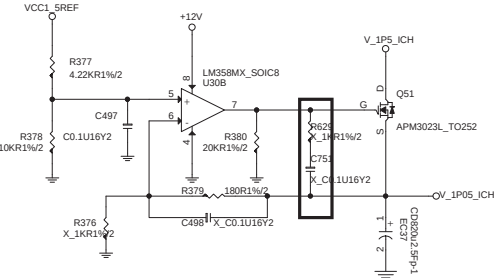
PWROK DELAY 100ms

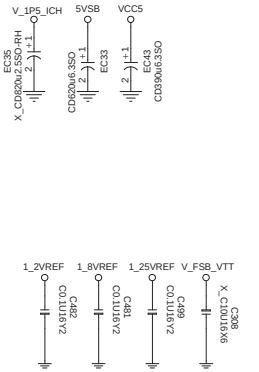


change q52,q53,q48 for 7002.
change q52.d for 5vsb

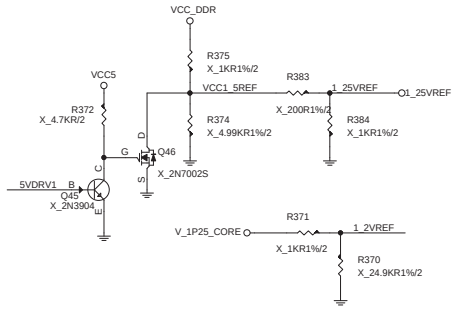
SB 1.05V 2A

Change EC45
from 1000uf to 820uf
07.11.26

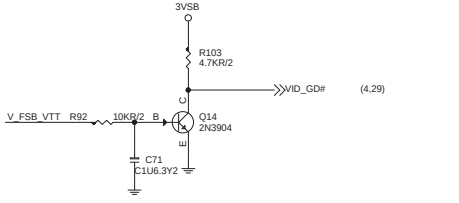




*Reserve for remove uP6261 and uP7707
*1_8REF use uP6103's internal 0.8VREF



VID before PWROK >3ms



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DDR II 1.8V POWER

Iripple=22.25*0.4*0.8/1=10.68A
2.5*3*1.7=5.814A>10.68A
Change EC21,EC20 from 1000uf to 470uf 07.11.26

D8 S-BAT54C_SOT23, +12V, 5VDIMM, R125 X_0R/3, R129 2.2R1%/5C97, C1U25X5

D11 X_S-BAT54ALT1G_SOT23-RH

5VDIMM_IN, C198, C181, C10U10Y5 C0.1U16Y2, EC15 X_CD470u6.3SO-RH, EC18 X_CD470u6.3SO-RH, EC14 CD470u6.3SO-RH, CHOKE1 CH_1.2U18A, C163 X_C10000P25X2

VCC_DDR

1_8VREF, R155 2KR1%/2, C108 C0.1U16Y2, R145 X_1KR1%/2, R143 3.01KR1%/2, C100 C10000P25X2, R140 X_1KR1%/2

U6 uP6103: Vref, VCC, BOOT, PHASE, UG, LG, FB, GND

R142 0R/3C1U25X5, C110

Q27 N-NTD4809NT4G_DPAK3-RH, Q30 N-NTD4806NT4G_DPAK3-RH

CHOKE2 CH-1.1U25A, R234 2.2R1%/5, C262 C3300P50X2, C1U16Y3, C298, EC29 CD820u2.5Fp-1, EC22 CD820u2.5Fp-1, EC23 CD820u2.5Fp-1

5VSB, R138 1KR1%/2, C99 C0.1U16Y2, Q19 2N7002S

Modify circuit 07.3.30 by Robile

(11) SLP_S4#, R134 1KR1%/2, Q17 2N3904, Q16 2N3904, R118 20KR1%/2, ATX_PWR_OK (16,27,30)

To meet Intel power down sequence.

9.4A+4.3A+2.75A+5.8A=22.25A
Irms(MAX) of VCC_DDR=22A

Change EC27,EC28,EC30 from 1000uf to 8200uf 07.11.26

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

DDR VTT Power

U9 W83310DS_SOIC8: VREF2, ENABLE, VCTRL, BOOT_SEL, VIN, GND2, VREF1, VOUT, GND

3VSB, VCC_DDR, VTT_DDR, EC11 移除, C144 C0.1U16Y2, C125 C0.1U16Y2, R174 1KR1%/2, R169 1KR1%/2, X_CD220u2.5SO-RH-3, EC10 CD820u2.5Fp-1, EC9 CD820u2.5Fp-1

EMI suggest to add 4pcs 0.1uf cap between VTT_DDR to VCC_DDR 08.01.09

C115 X_C0.1U16Y2, C291 C0.1U16Y2, C186 C0.1U16Y2, C350 C0.1U16Y2, C274 C0.1U16Y2

C176 C0.1U16Y2, C165 X_C0.1U16Y2, C175 X_C0.1U16Y2, C179 X_C0.1U16Y2

de- VCC_DDR high frequency noise.

C311 C0.1U16Y2, C216 C0.1U16Y2, C197 C0.1U16Y2, C334 C0.1U16Y2

EMI suggest to add 4pcs 0.1uf cap between VCC_DDR to GND 08.01.09

NB 1.25V POWER

Change EC33,EC34 from 1000uf to 470uf 07.11.26

Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A

+12V, X_S-BAT54ALT1G_SOT23-RH D21, VCC5_IN, C386, C417, C10U10Y5 C0.1U16Y2, EC37 CD470u6.3SO-RH, EC27 CD470u6.3SO-RH, CHOKE3 CH-1.2U8A-LF, C732 X_C10000P25X2, VCC5

NB_V1_25 16.3A

Irms(MAX) of VCC1_25=16.3A

1_25VREF, R338 1KR1%/2, R350 2.2R1%/5C473, C1U25X5, U27 uP6103: Vref, VCC, BOOT, PHASE, UG, LG, FB, GND

R333 0R/3C1U25X5, C415, Q42 N-NTD4809NT4G_DPAK3-RH, Q41 N-NTD4806NT4G_DPAK3-RH

CHOKE4 CH_1.2U18A, R331 2.2R1%/5, C418 C3300P50X2, V_1P25_CORE

C421 C0.1U16Y2, R334 X_1KR1%/2, R342 3.01KR1%/2, C428 C10000P25X2, R340 X_1KR1%/2

C423 C1U16Y3, CD820u2.5Fp-1 EC30, CD820u2.5Fp-1 EC28, EC32 X_C470u2.5SO-RH

Change EC35,EC36 from 1000uf to 820uf 07.11.26

AMT POWER

V_1P25_CL_MCH(4.3A)

For vPRO

3VSB, R274, X_24.3KR1%2, R273, X_15KR1%/2, Place CAP to close PIN 3 or PIN5, C348 X_C2.2U6.3Y3

U20A, CL_MCH_DRV, C347, X_C2200P50X2, R277 X_20KR1%/2, Q39 X_N-IPD09N03LA_TO252-LF

5VSB, VCC_DDR, C328 X_C0.1U10X0402, C329 X_C4.7U10Y5, EC24 X_CD470u6.3SO-RH

X_LM358MX_SOIC8, R299 X_0R/2, R278 X_499R1%0402, C360 X_C0.1U10X0402 CTose MOS PIN of V_1P25_AMT, C375, EC25 X_CD470u6.3SO-RH, X_C0.1U10X0402

V_1P25_CL_MCH, V_1P25_CORE, R317 0R/5, R316 0R/5

For ViiV

(11) SLP_M#, SLP_M# R408 X_10KR/2, Q47 X_2N3904, C506 X_C1U16Y3

SLP_M R262 X_10KR/2, Q34 X_2N3904, C336 X_C1U16Y3

R269 X_A_150R/3

CLINK PWROK GENERATION

V_1P25_CL_MCH, R303 X_3.32KR1%/2, R290 X_82.5KR1%2, R289 X_470R1%/2, MCH_CLPWROK, MCH_CLPWROK (11)

C373 X_C1U16Y3, R288 X_1KR1%/2, Q40 X_2N3904

3VSB, R300 X_2.49KR1%/2, U20B X_LM358MX_SOIC8, R301 X_1KR1%/2

SLP_M R267 X_1KR1%/2

For vPRO

V_3P3_CL

(711mA)

3VSB, V_3P3_CL, R534 0R/5, R535 0R/5

For ViiV

For vPRO

C630 X_C1U16Y3, Q59 X_P-IRF5800_TSOP6

(15) SLP_M, SLP_M R520 X_1KR1%/2

(11) WOL_ONLY, WOL_ONLY R538 X_10KR/2, Q58 X_2N3904

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Voltage Regular Module

N-P0903BDG_TO252	mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=5m (@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=7800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG/TO252	mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U2SP	ESR<13m ,Ripple cur.=2.7A,LCC12uAv105C
CD560U4OS-2	CAP,OS-CON,560u/4V,Dip-2/8*9/3.5mm,ESR<7mohm, Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
1800UF/6.3V	ESR<12m , Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs, KZJ series
0.25uH/40A	,IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
CH-1.1U25A-LF	IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CD1000U16EL20-2	CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE

change NIKE to 4809,4806

0.8375~1.6V / 125A

CP25,CP26,CP27,CP28 PLACE ON THE SOLDER SIDE, CLOSE TO INDUCTOR

Place close to inductor

Only reserve for 3 phase operate

FOR WATCH DOG

BOTTOM PAD CONNECT TO GND

Change EC18,EC13,EC3,EC26 from 1000uf to 270uf 07.11.26

680uF EL Capactiors

PANASONIC Cap.

change 680u cap to 820u POScap 07.11.22

MLCC Inside Socket

Samsung Cap.

change to 22uF for power

SP Capacitors

EL Capacitors

OSTOR Cap.

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Size: Custom	Document Description: VRD11-ISL6322 4-phase		Rev: 0A
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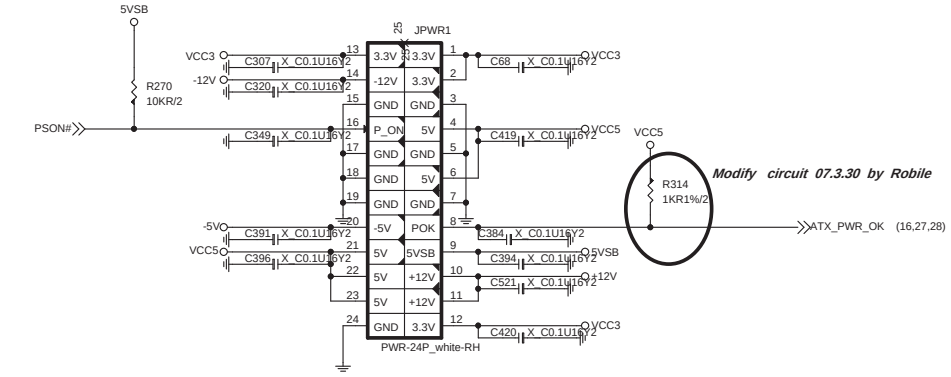
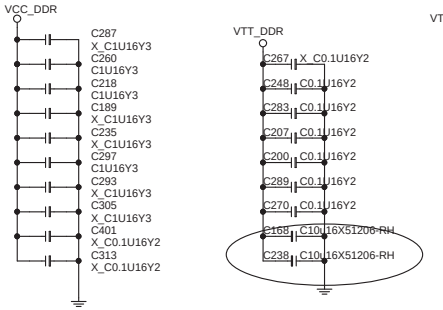
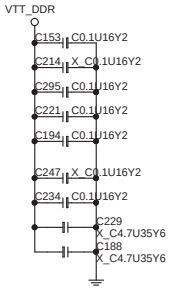
ATX POWER CONNECTOR



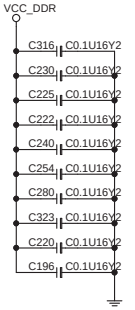
CHANNEL A V_SM_VTT DECOUPLING CAPS



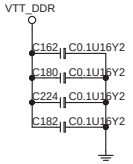
CHANNEL B V_SM_VTT DECOUPLING CAPS



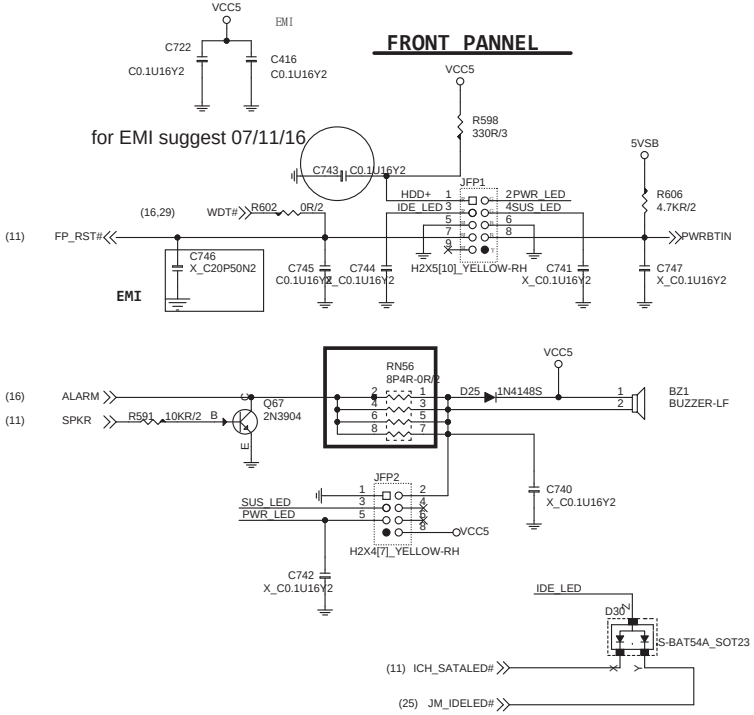
FOR EMI



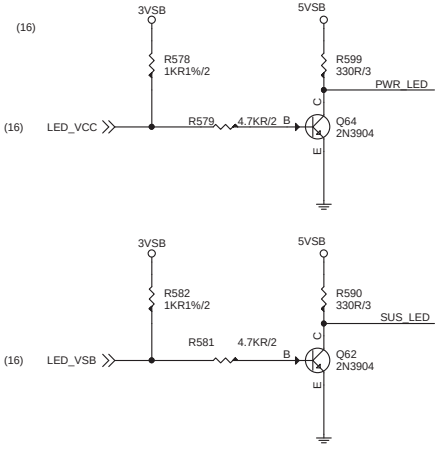
EC41 移除



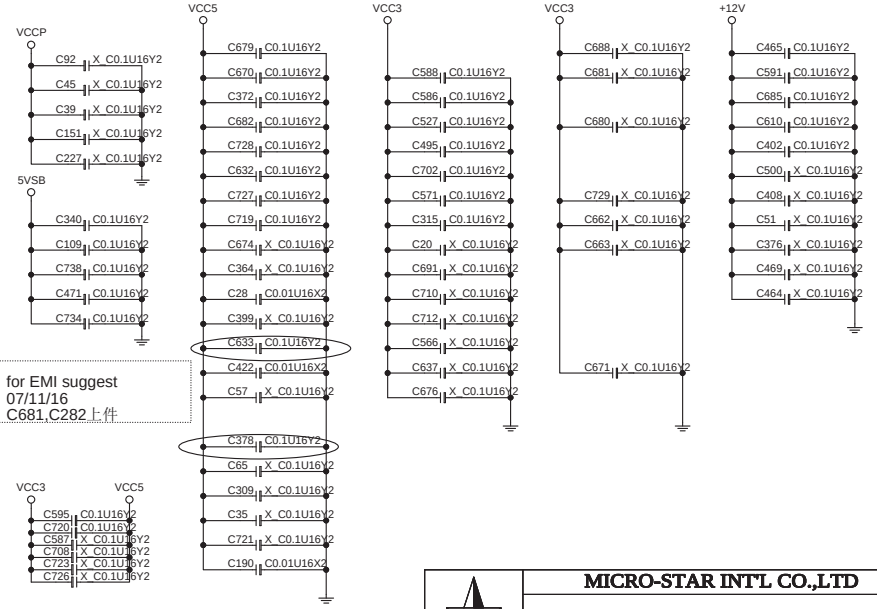
FRONT PANNEL



LED (for Fintek 71882)



Cap. for EMI & Power



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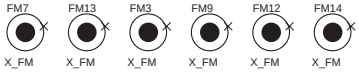
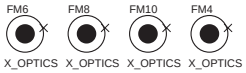
Optical Fiducial Marks-120





PCB1

9849-10

AMI LABLE1

AMI Lable

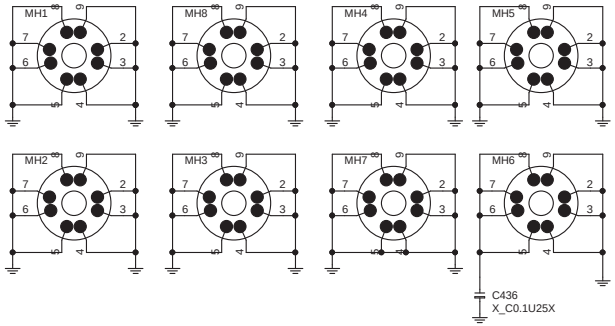
JFP2(4-6)

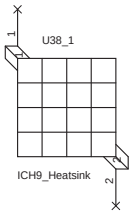
X_JUMPER-1X2A_green

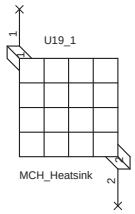
BAT1_X

BATTERY-CR2032

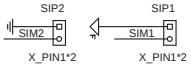
Mounting Holes







Simulation



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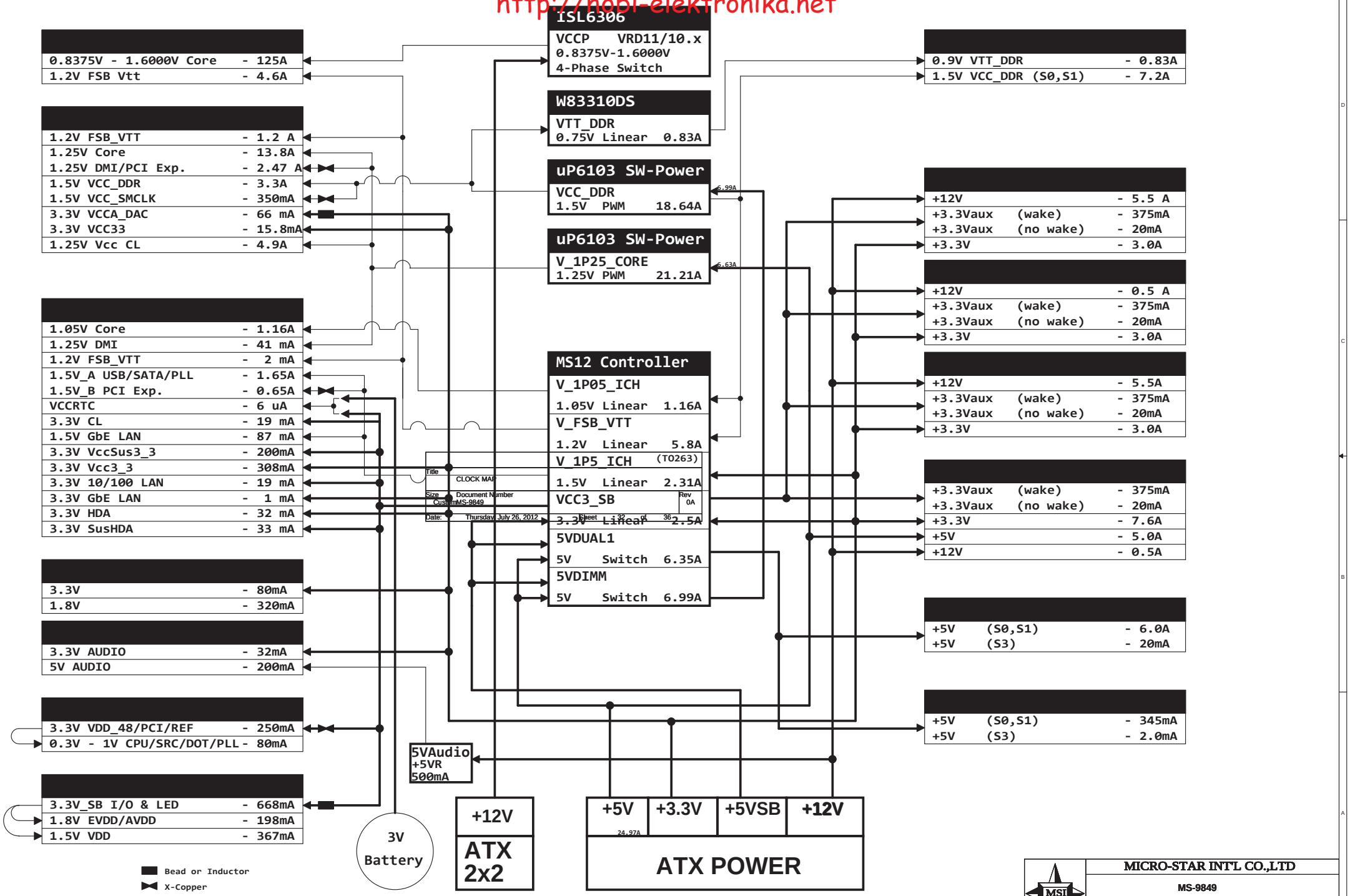

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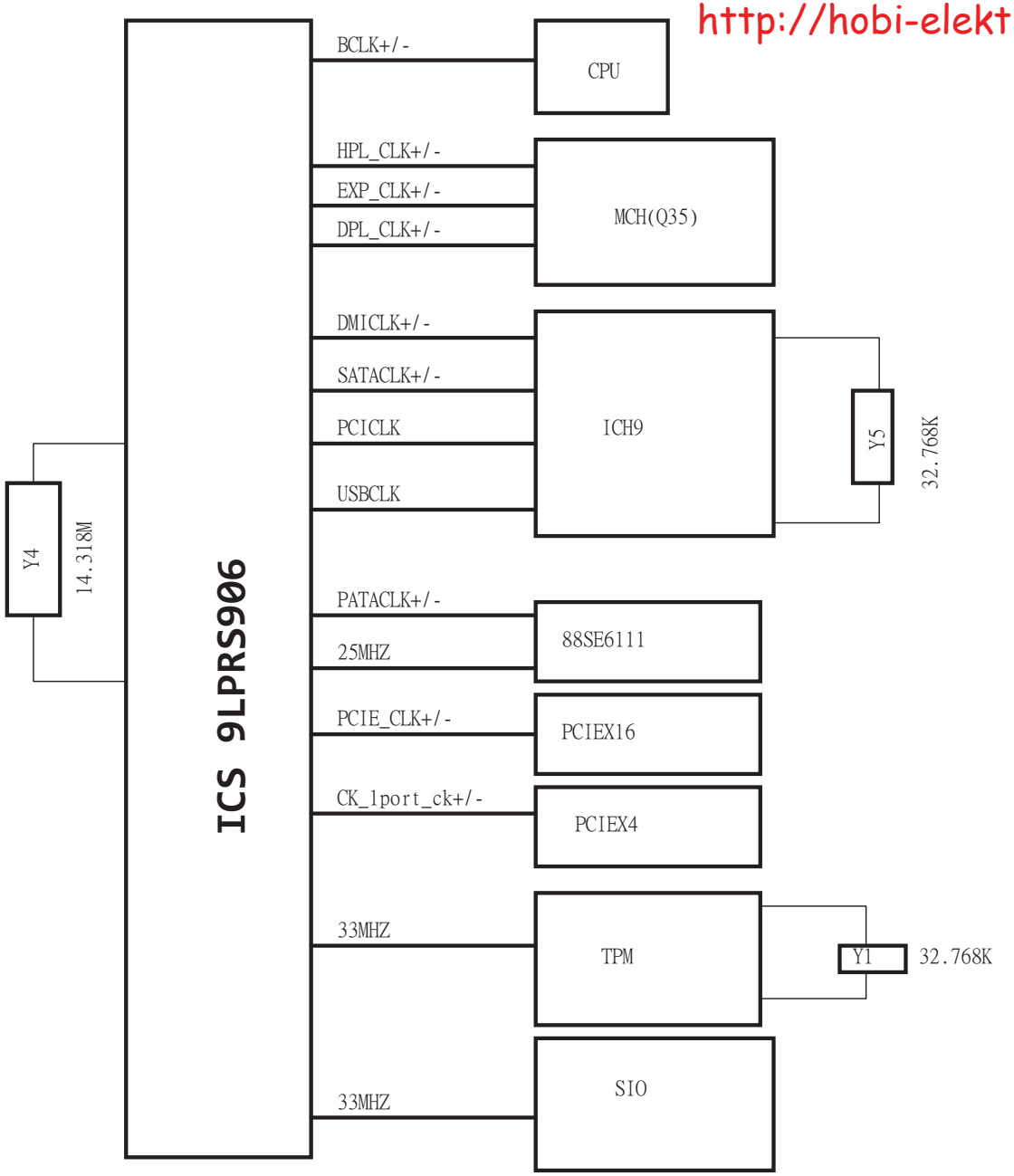

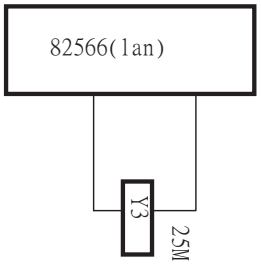

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ICH9

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2_FANTAC/PU
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	WOL_ONLY
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	PHY_DIS#
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	CK_PCI_STOP_N
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	CK_CPU_STOP_N
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	USB_MODE
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	DMI_STRAP
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

SIO(IT8892)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	UNUSED		
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	UNUSED		
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	LED_VSB	OUTPUT/OD	Power LED for VSB
GPIO16	LED_VCC	OUTPUT/OD	Power LED for VCC.
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT/OD	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO25	PME#	OUTPUT/OD	Generated PME event.
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	SIO_PWROK	OUTPUT/OD	PWROK function,delayed 400ms as VCC arrives 2.8V
GPIO33	RSMRST#		Resume Reset# function, delayed 66ms as VSB arrives 2.3V.
GPIO40	SYS2_FANTAC	INPUT	SYSFAN2 tachometer input.
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	Infrared Transmitter Output.
GPIO43	IRRX	INPUT	Infrared Receiver input.
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN[3:5]	UNUSED	INPUT	

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	P/N_DDR0_A	P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A	P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B	P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B	P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1/#3 PGNT#1/#3	AD17 AD19	CK_P_33M_S2 CK_P_33M_S3
1394	PIRQ#C	PREQ#2 PGNT#2	AD18	CK_P_33M_1394

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

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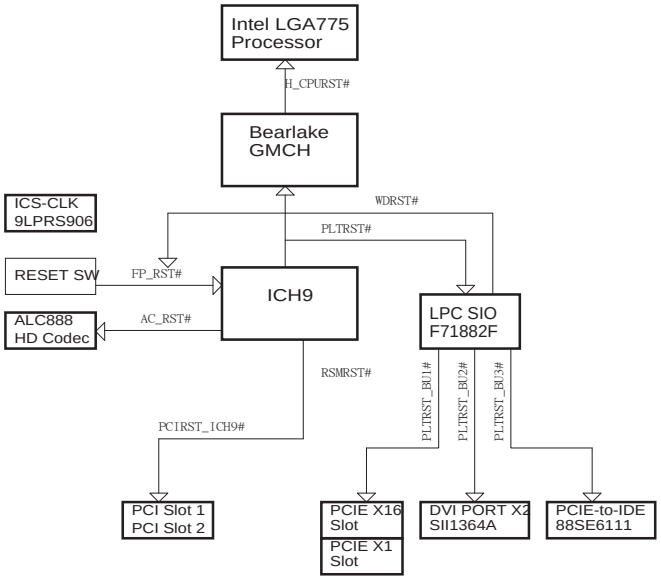
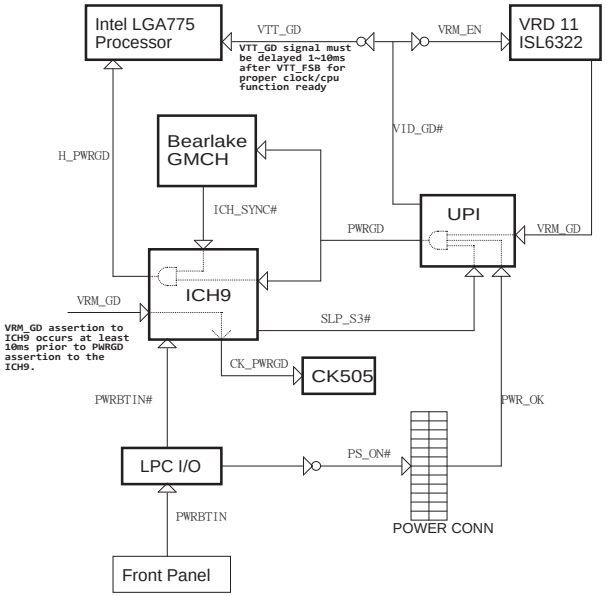
RESET MAP



PWROK MAP



12V

5V

3.3V

1.5VREF

NB 1.25V Core

VDDR

SB 1.5V

V_FSB_VTT

VID_GD

VTT_PWGD

VRM_EN

CPU VCore

VRMGD to SB

CK_PGD

CHIP_GD

PL_RST

PCI_RST

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9849 1.0 change Part:2009.03.02

1: change Q48,Q52,Q53 to 2N7002 (0226)

2: change RN56 to 0ohm (0226)

3: Remove the front-end SII1364 series resistor and change CN3,CN4 to C11-1042542-S02. (0226)

4: USB POWER at end add-Solid Capacitor 220U (0226)

5: Add in U34.2 Pull high resistor R625 (0226)

6: R292, R373 changed to 1% precision resistors (0226)

7: C614 from 22P replaced 33p (0226)

8: R41, R30, R23, R86, R188, R184, R178, R216 from 120R replaced 90.9Ohm (0226)

9: R208,R116 from 270R replaced 360R (0226)

10:C731 from 0.015UF replaced 2200P (0226)

11:Add C164 (0226)

12:CONN3 change p/n to N53-16M0101-F02. for EMI (0226)

13:VRM Modify FOR power team (0226)
(1) R11=680ohm,0402,1% P/N: R11-0681T12-W08
(2) R14=0ohm P/N: R11-0000012-W08
(3) R7=1.4K,0402,1% P/N: R11-0142T12-W08
(4) R22=1000HM,0402,1% P/N:R11-0101T12-W08
(5) C16=470pF P/N: C11-4712012-W08
(6) RT1=10K (R51-0103T13-M05)
(7) C148,C149,C150,C169,C170,C171,C172,C173,C174 Change to 22uF 1206 MLCC P/N: C11-2267317-S02
(8) C116,C118,C119,C120,C121,C123,C145,C146,C147 Change to 22uF 1206 MLCC P/N: C11-2267317-S02

14:Add R629,C751,R627,C703,R628,C748 for POWER TEAM (0226)

15:RGB put side of FB1, FB2, FB3 remove (0226)

16:Remove EC26 for layout (0226)

17:Remove C488,C489,C490,C492,C493,C494,C485,C486 for EMI (0226)

18:Remove R44,R60 for layout (0226)

19:Put the CPU heat sink to remove the four screw hole grounding for layout(0226)

20:Vcore put the H-MOS from the original D03-0903BDB-N03 changed to D03-0480900-O05
L-MOS from the original D03-75N022B-N03 changed to D03-0480600-O05 (0226)

21:Change Q27,Q30,Q41,Q42 to D03-0480600-O05(0226)

22:Change Q27,Q30,Q41,Q42 to D03-0480600-O05(0226)

23:USB OC# increase the pull high resistor (0226)

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