

MS-6778 Ver : 00A

VIA KM400 + VT8237 Chipset

CPU:
AMD Athlon XP / Athlon / Duron Socket 462

System Chipset:
VIA KM400 + VT8237

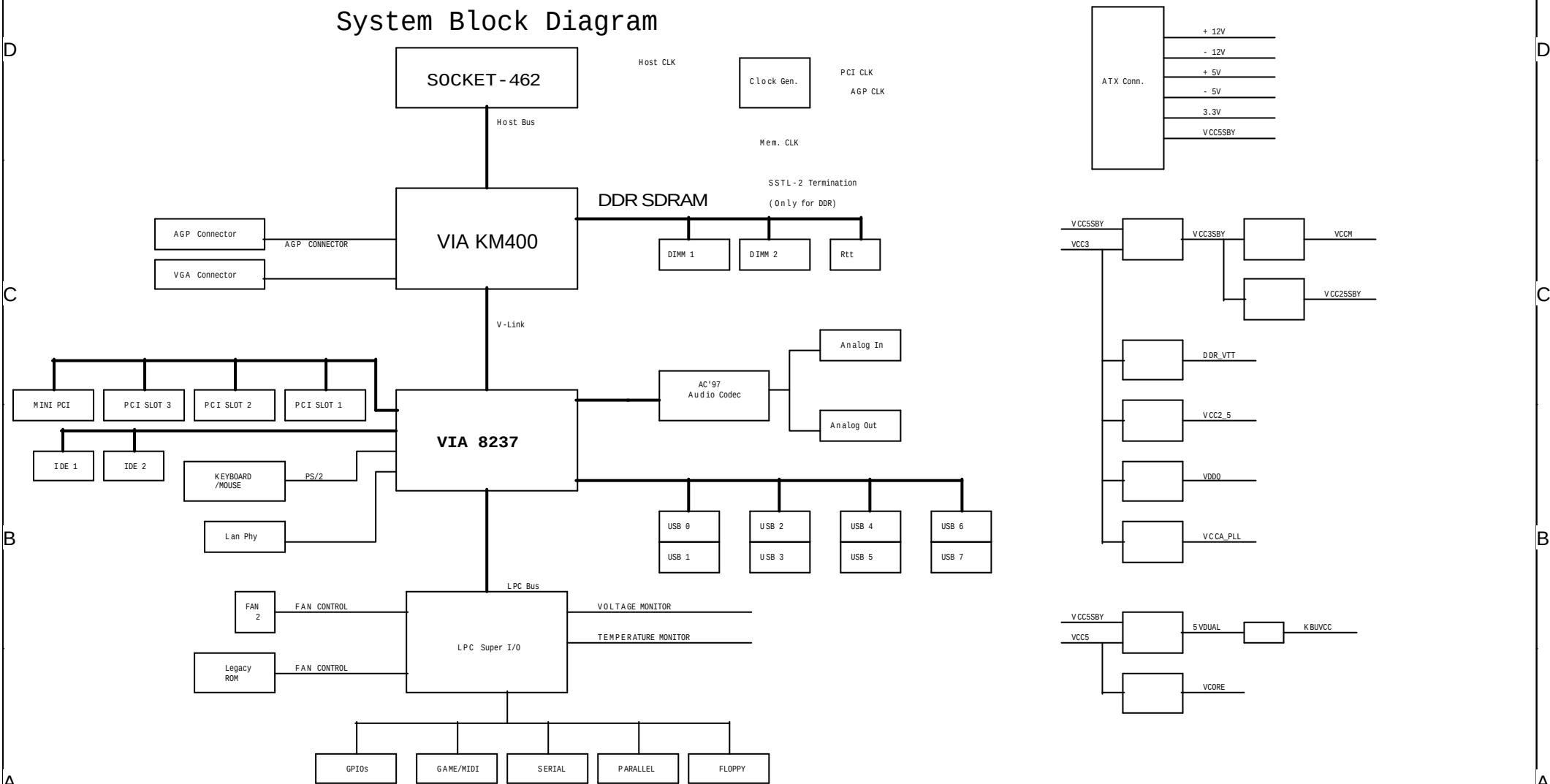
On Board Chipset:
LPC Super I/O -- W83697HF
Lan : Via PHY VT6103

Expansion Slots:
AGP 3.0 Slot * 1
DDR Slot * 2
PCI 2.2 Slot * 3
MINIPCI*1

ON Board LAN(PHY):VT6103

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System Block Diagram

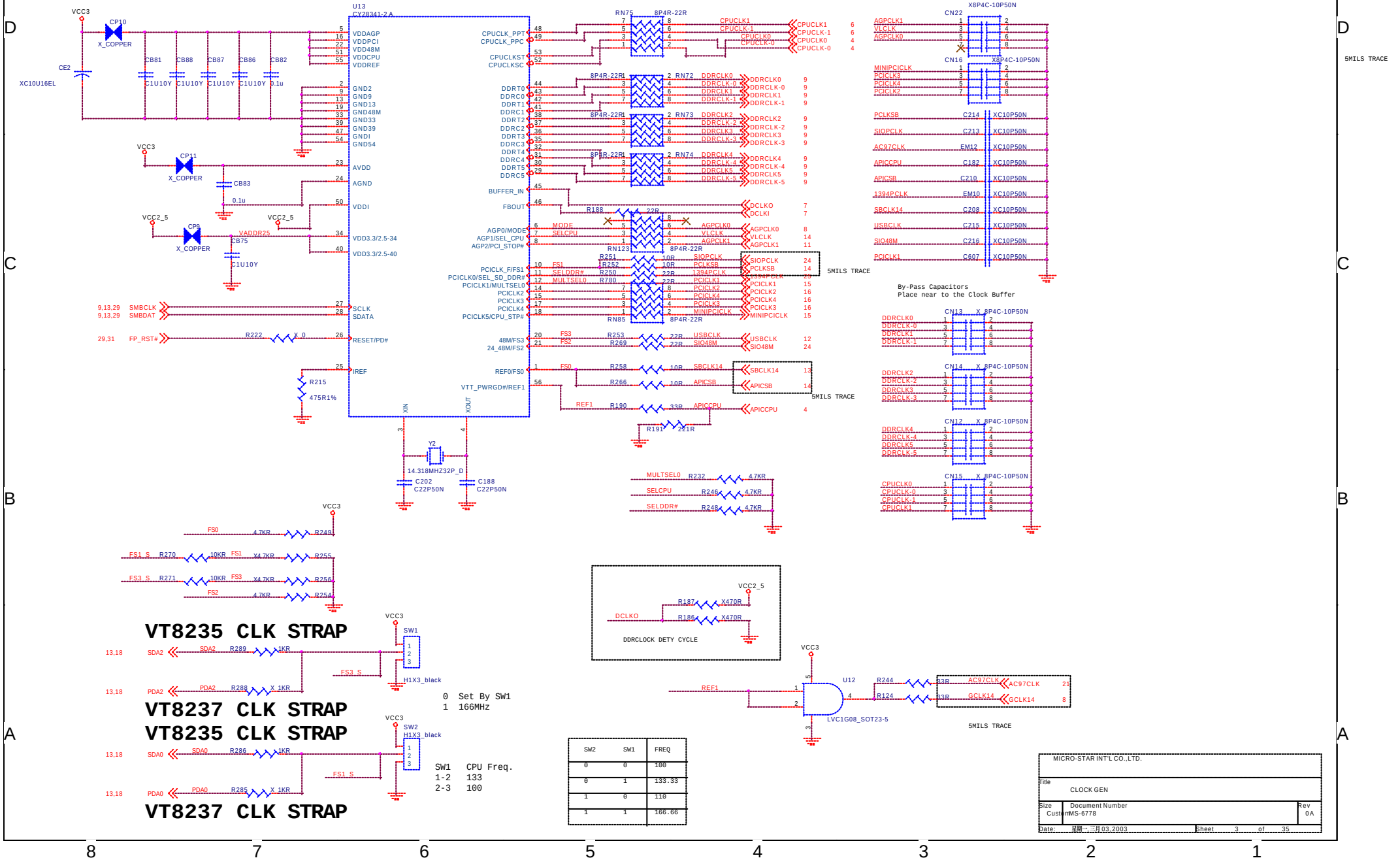


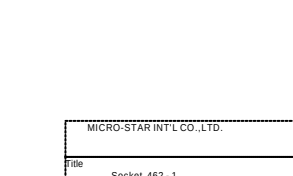
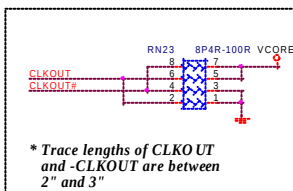
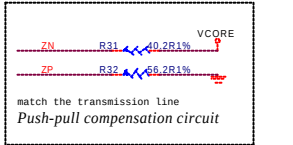
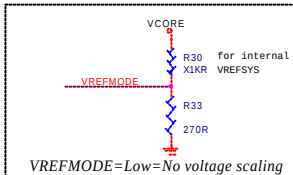
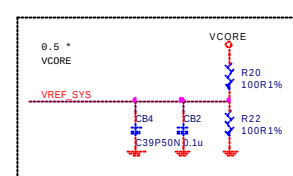
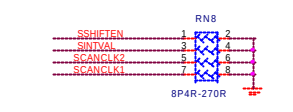
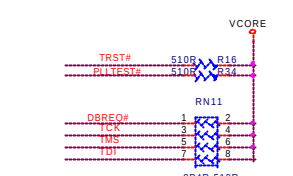
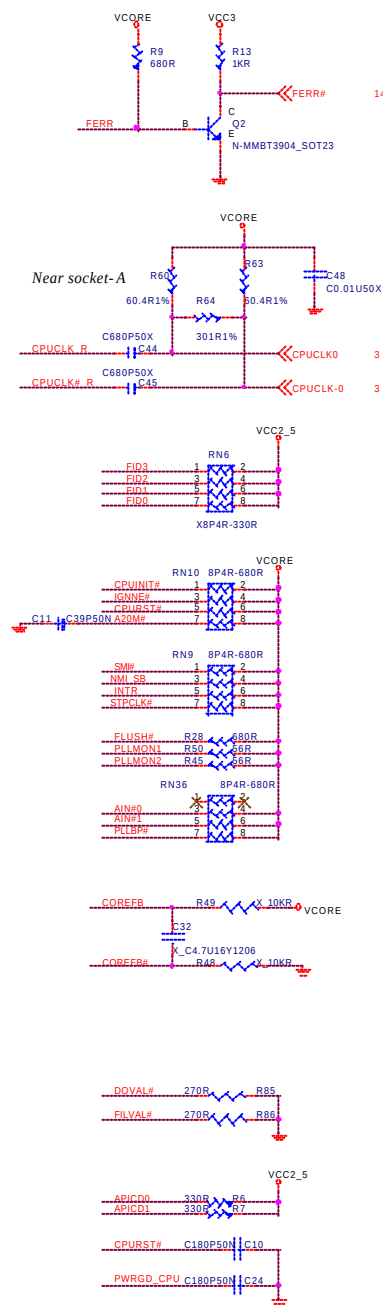
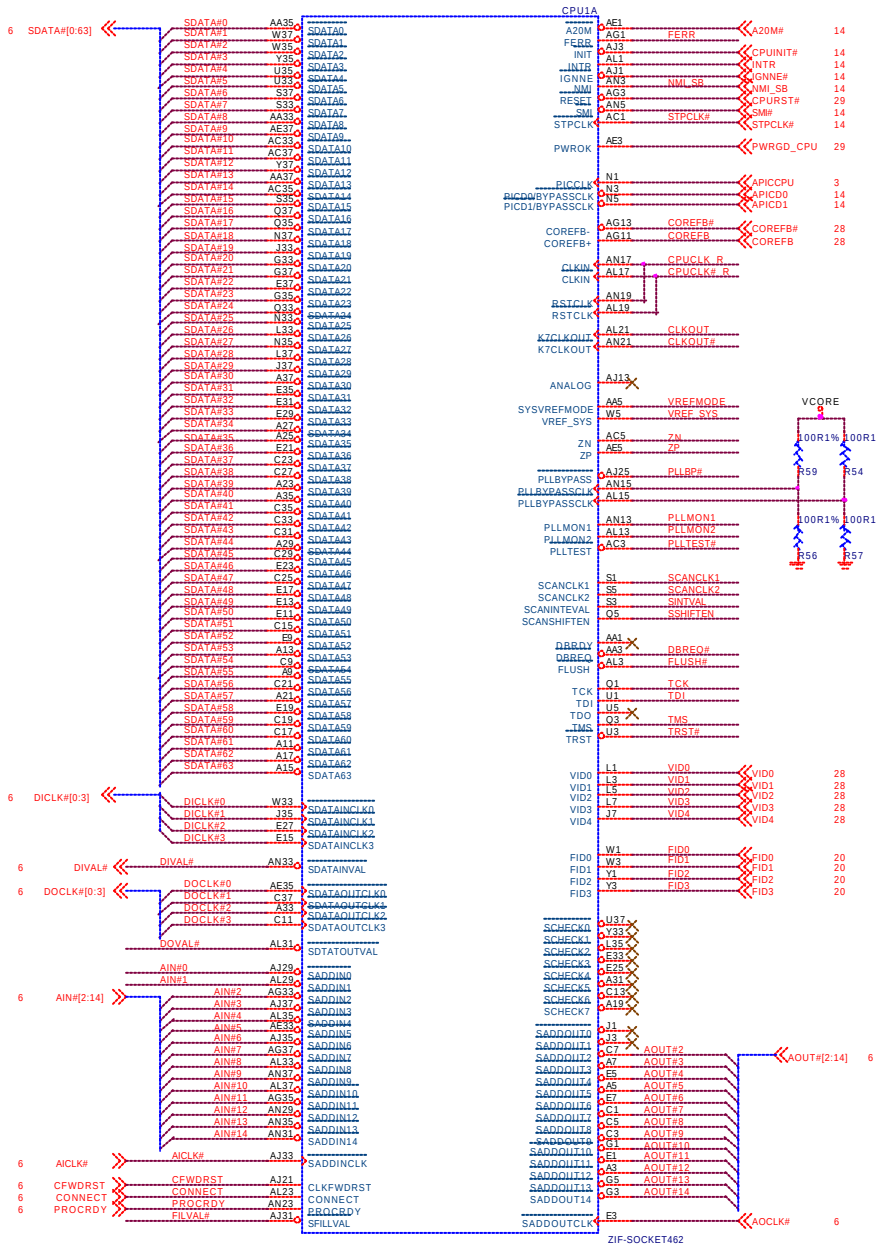
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Title			
System Block Diagram			
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Main Clock Generator

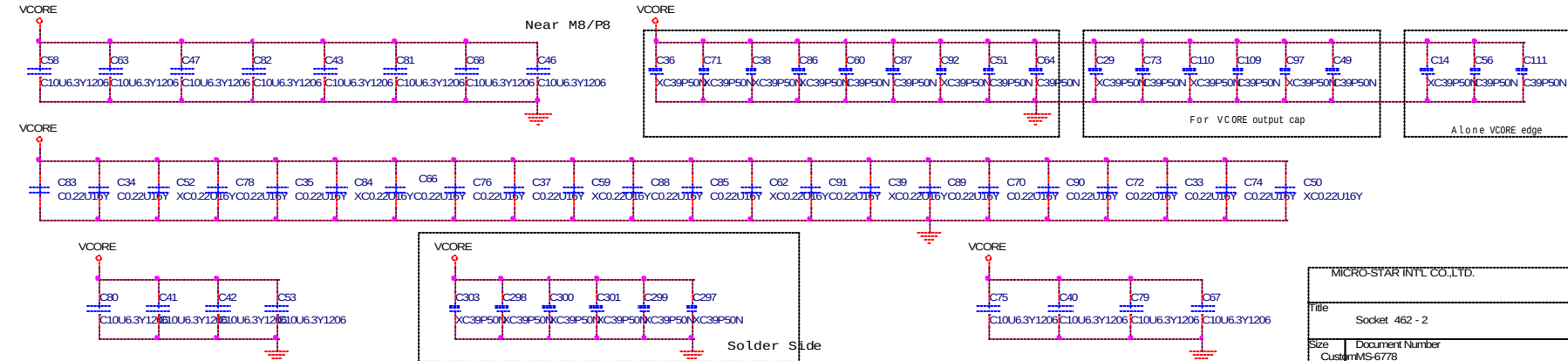
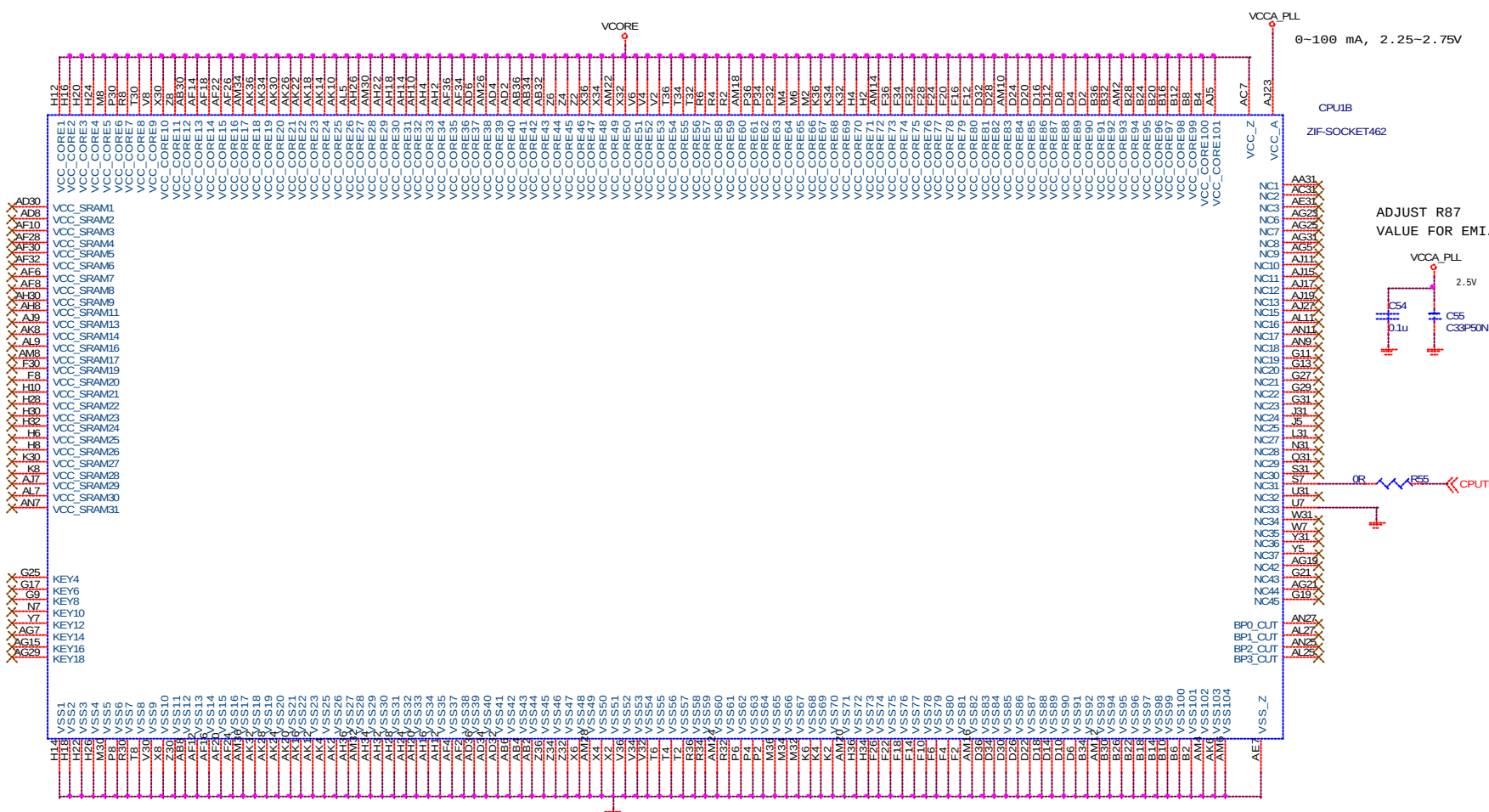
Damping Resistors Place near to the Clock Outputs

By-Pass Capacitors
Place near to the Clock Outputs



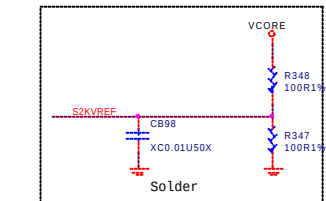
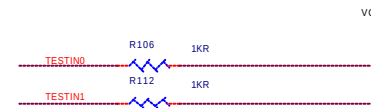
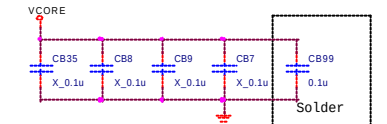
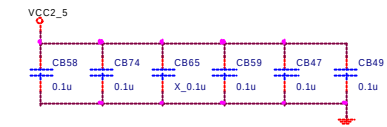
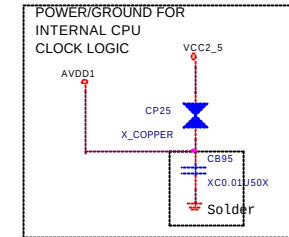
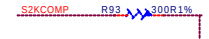


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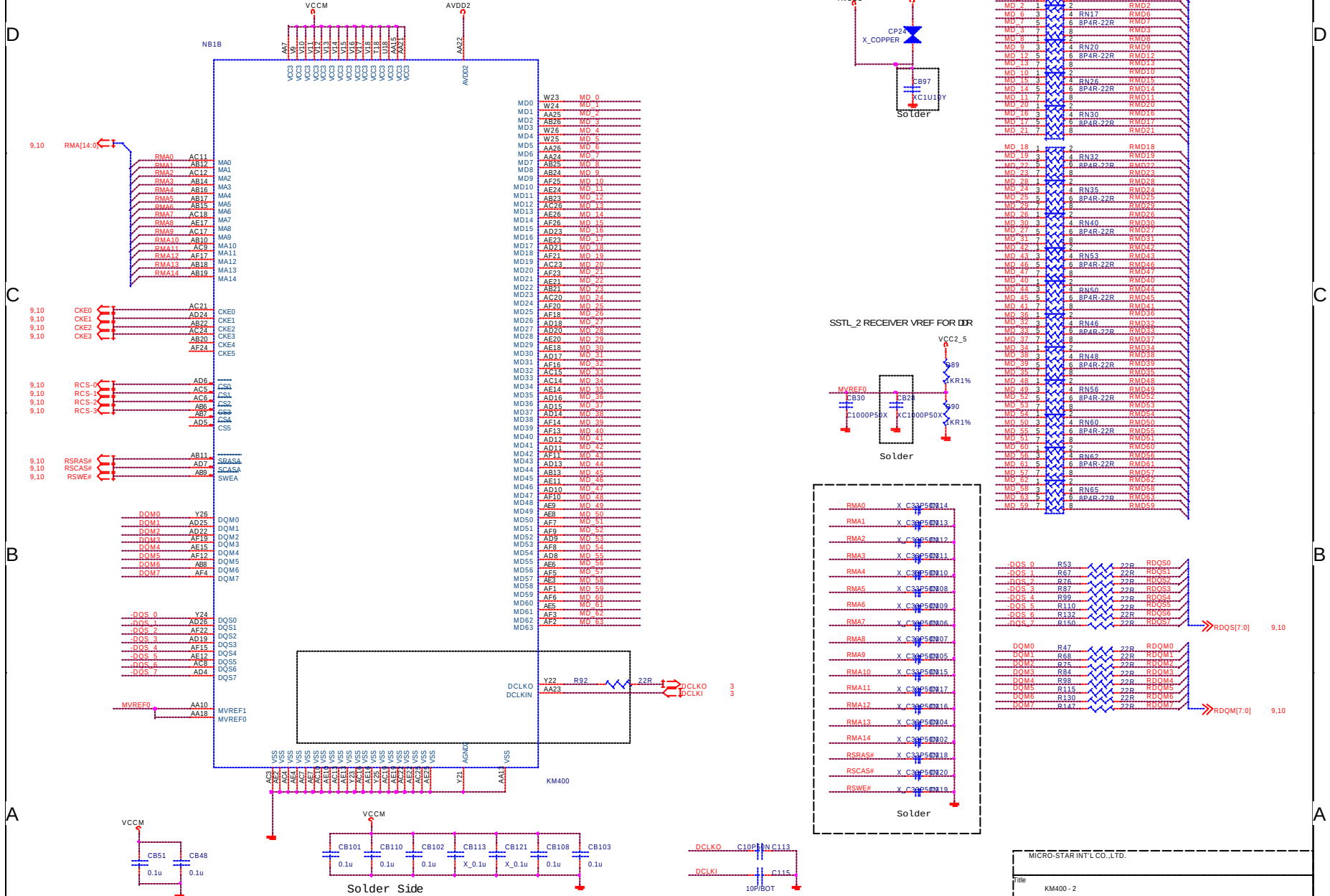


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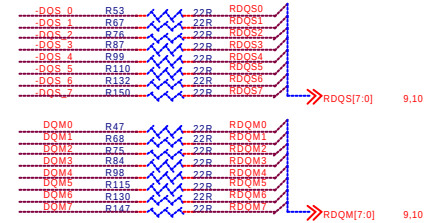
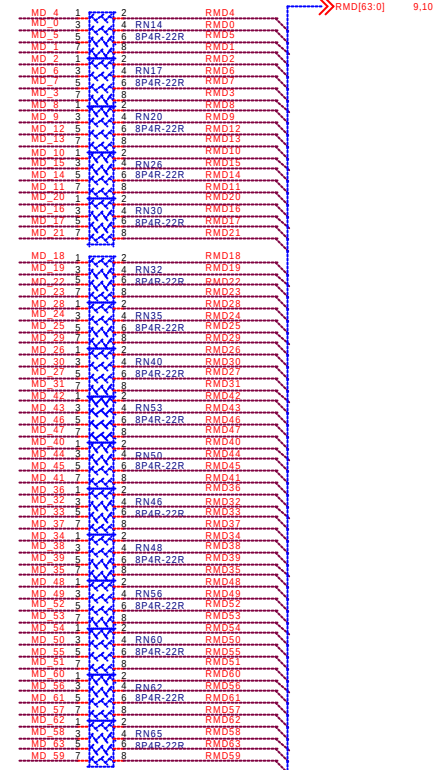
D



NORTH BRIDGE 2 of 3 (MEMORY)



Place these damping resistors close to DIMM1



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KM400-2			
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NORTH BRIDGE 3 of 3 (AGP,VLINK,VGA)

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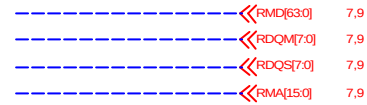
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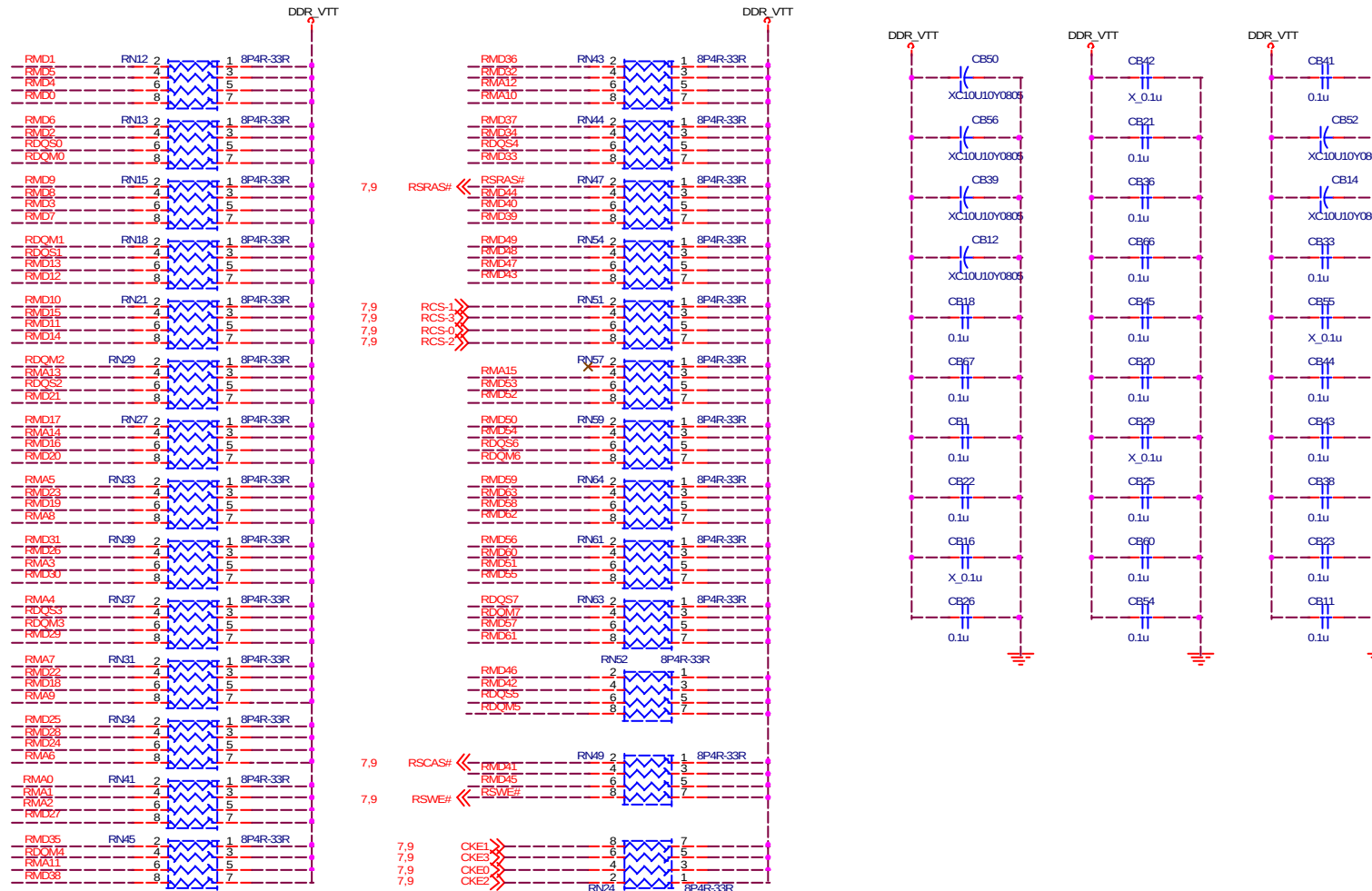
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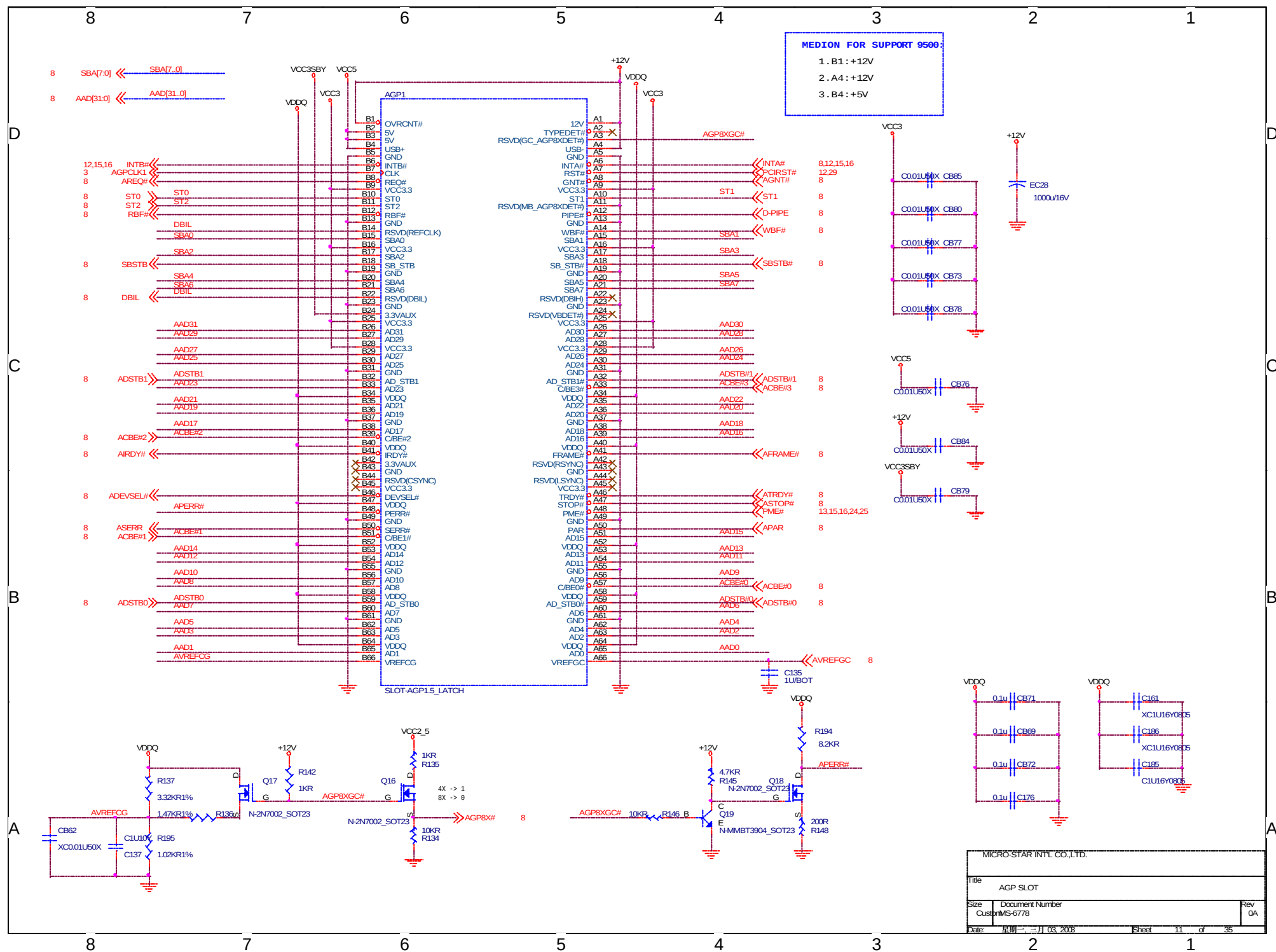
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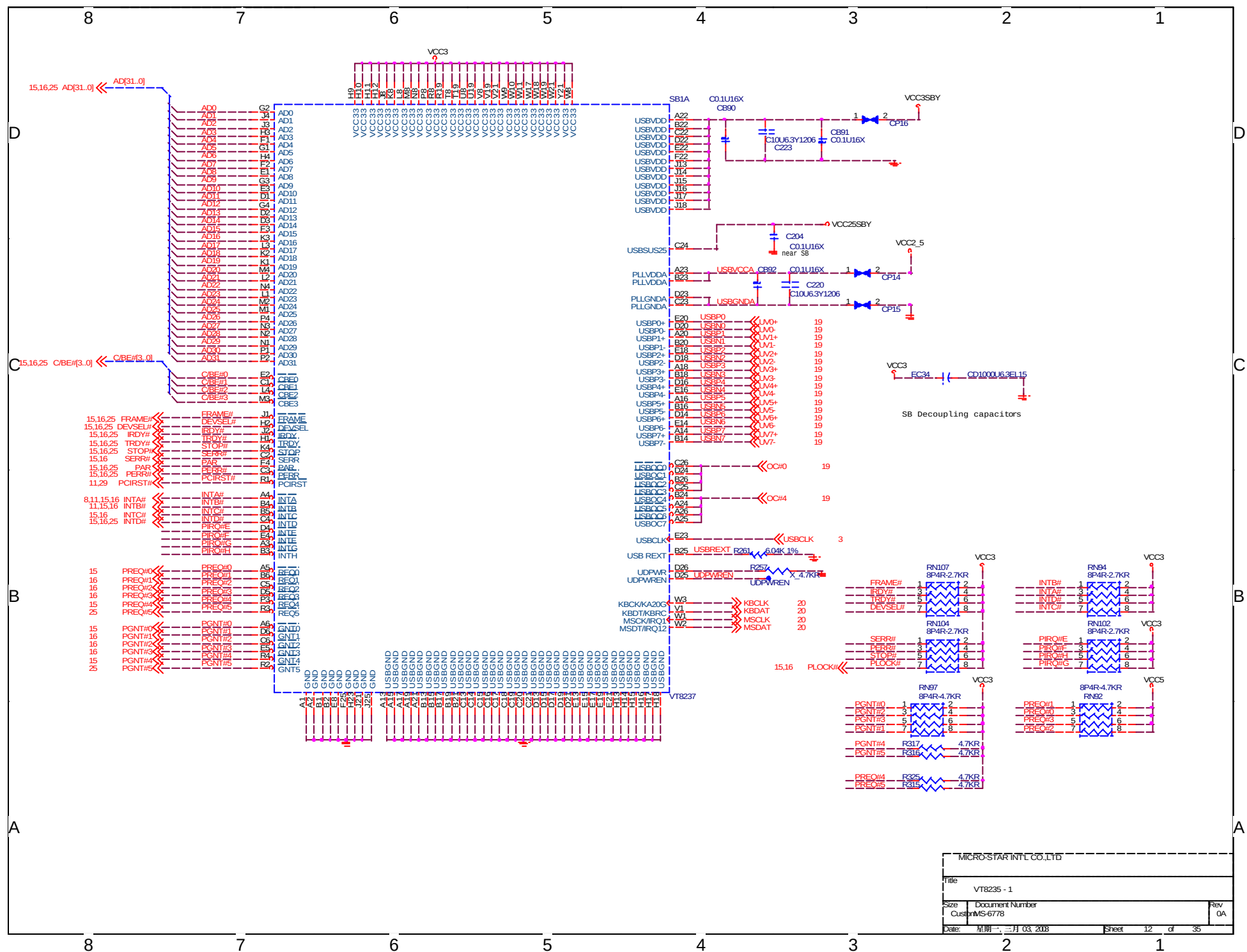
SSTL-2 Termination Resistors

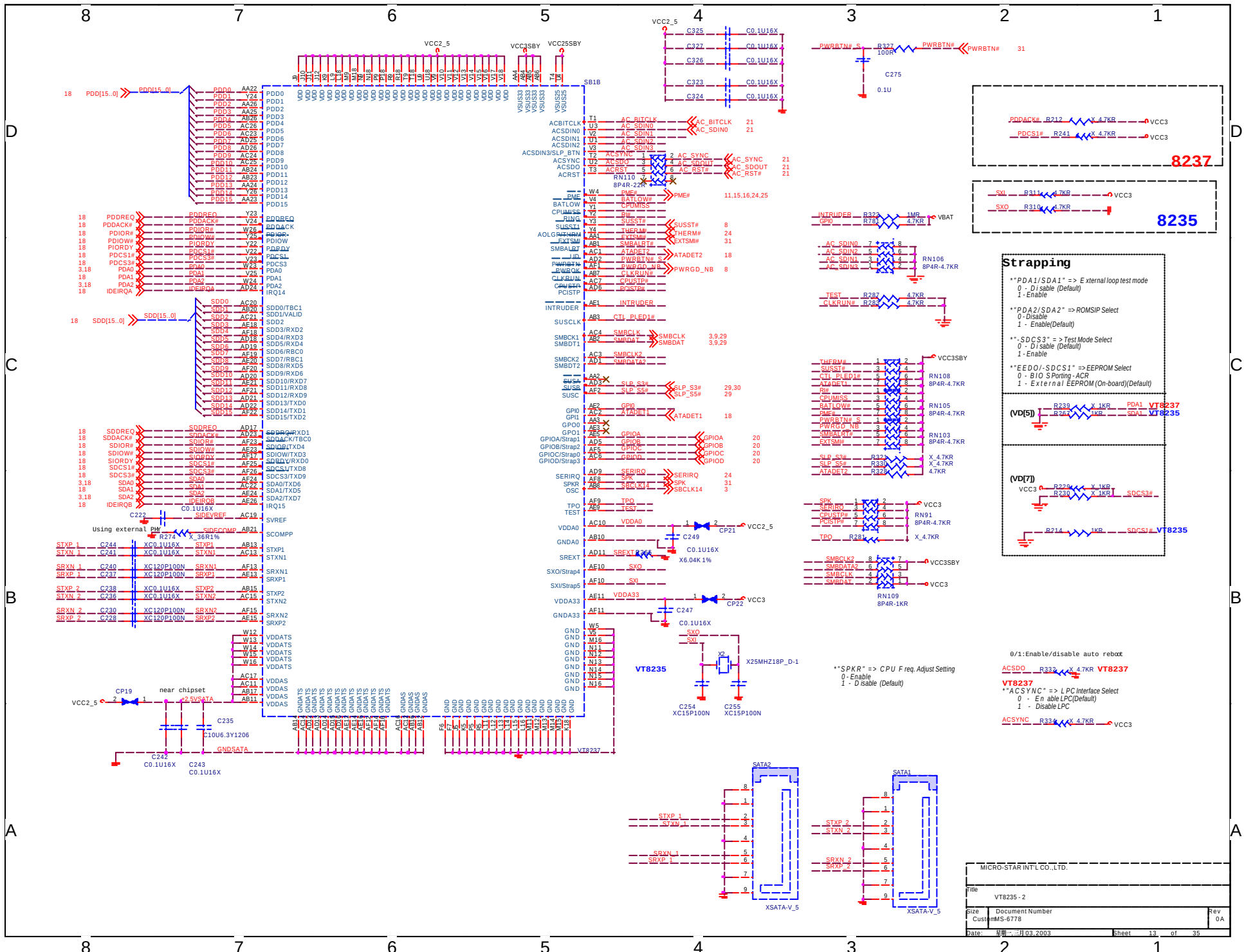


	SDR	RS	DDR	FS	RLT
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	47
MA/Control	LV-CMOS	10	SSTL-2	0	47
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		









Strapping

**PDA1/SDA1* => External loop test mode
0 - Disable (Default)
1 - Enable

**PDA2/SDA2* => ROMSIP Select
0 - Disable
1 - Enable(Default)

**SDCS3* => Test Mode Select
0 - Disable (Default)
1 - Enable

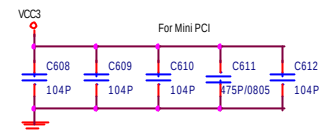
**EEDO/-SDCS1* => EEPROM Select
0 - BIO S Porting-ACR
1 - External EEPROM (On-board)(Default)

(V[5])

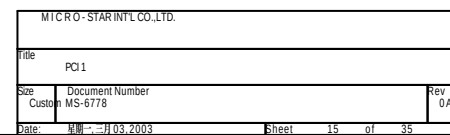
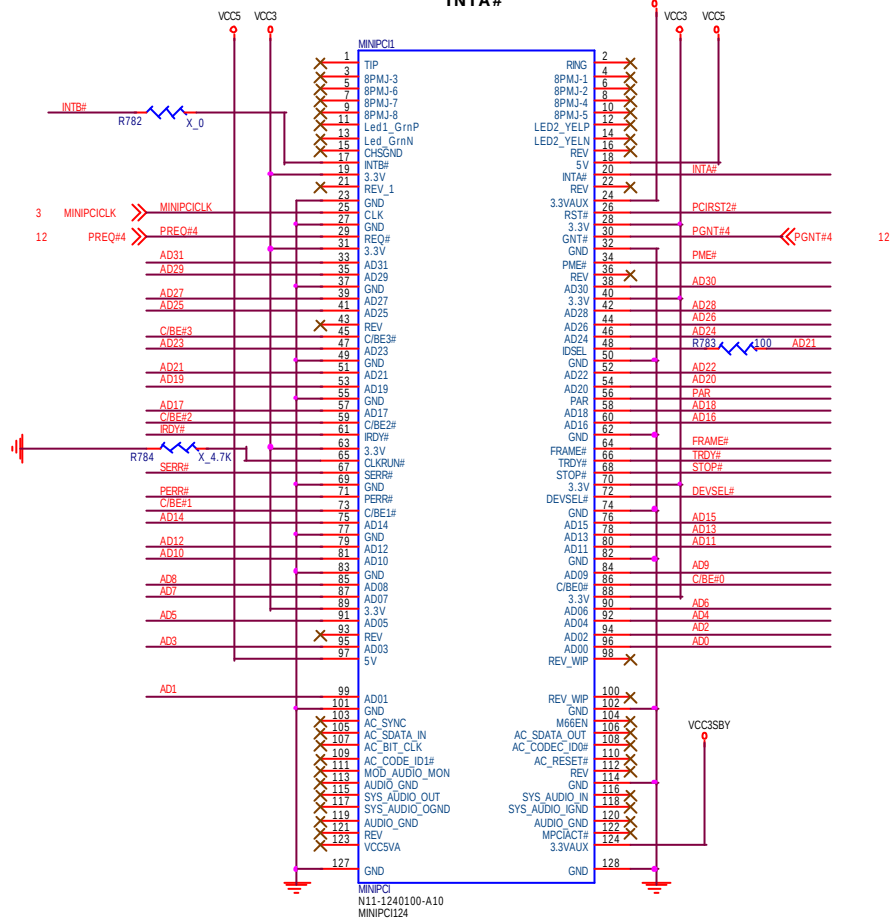
(V[7])

0/1:Enable/disable auto reboot
ACSDO R332 X 4.7K R8237
VT8237
**ACSYNC* => LPC Interface Select
0 - Enable (Default)
1 - Disable LPC
ACSYNC R334 X 4.7K R8235

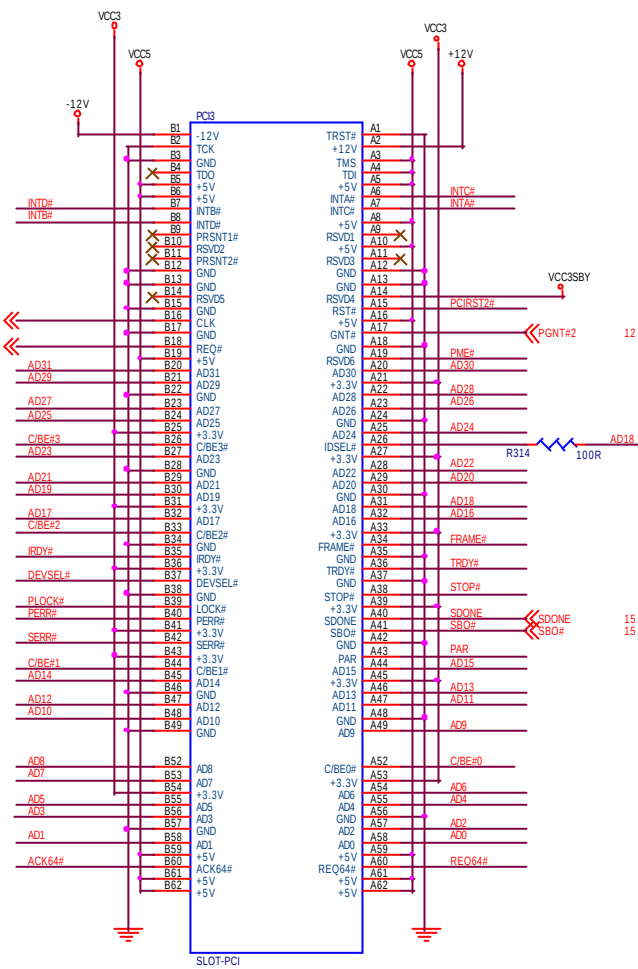
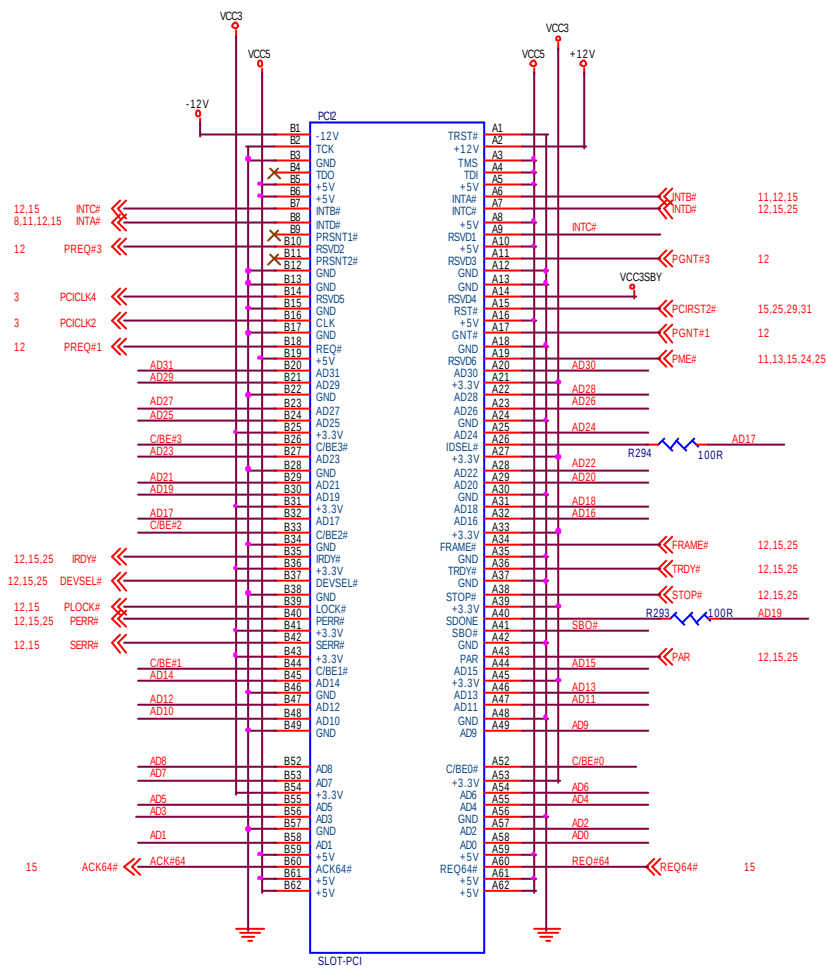
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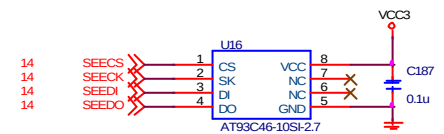
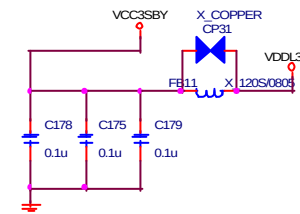
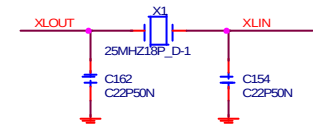
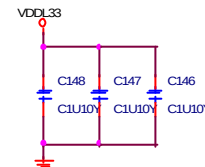
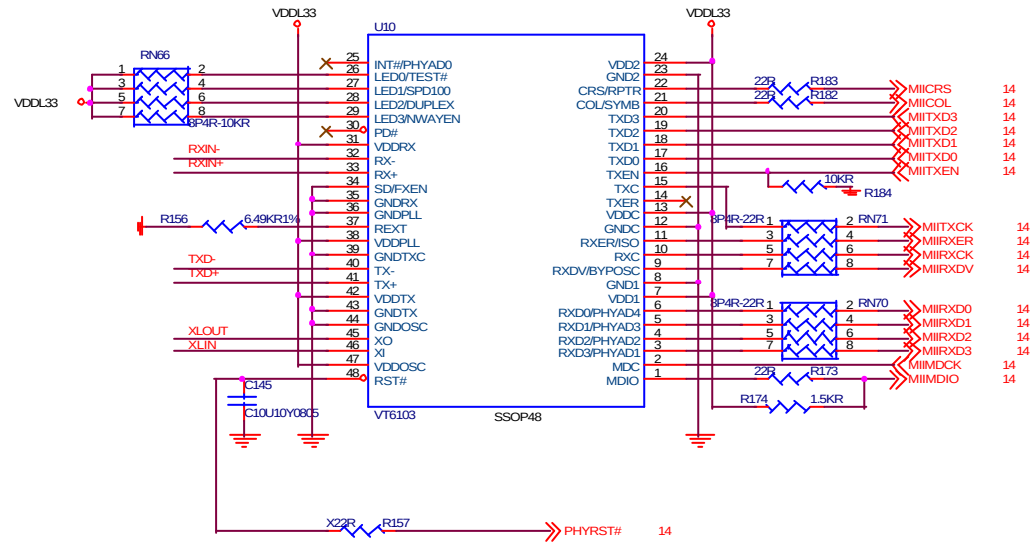
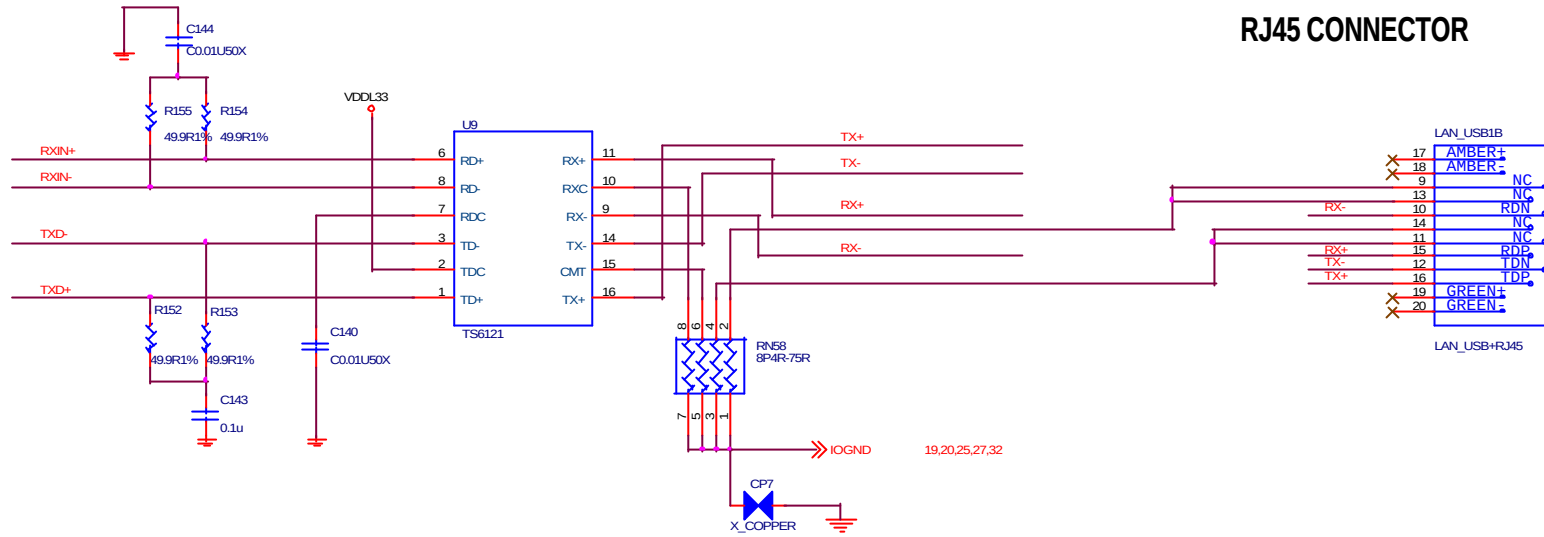
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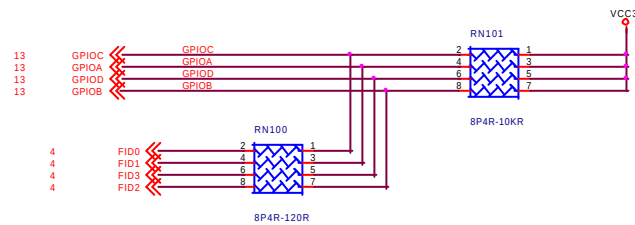
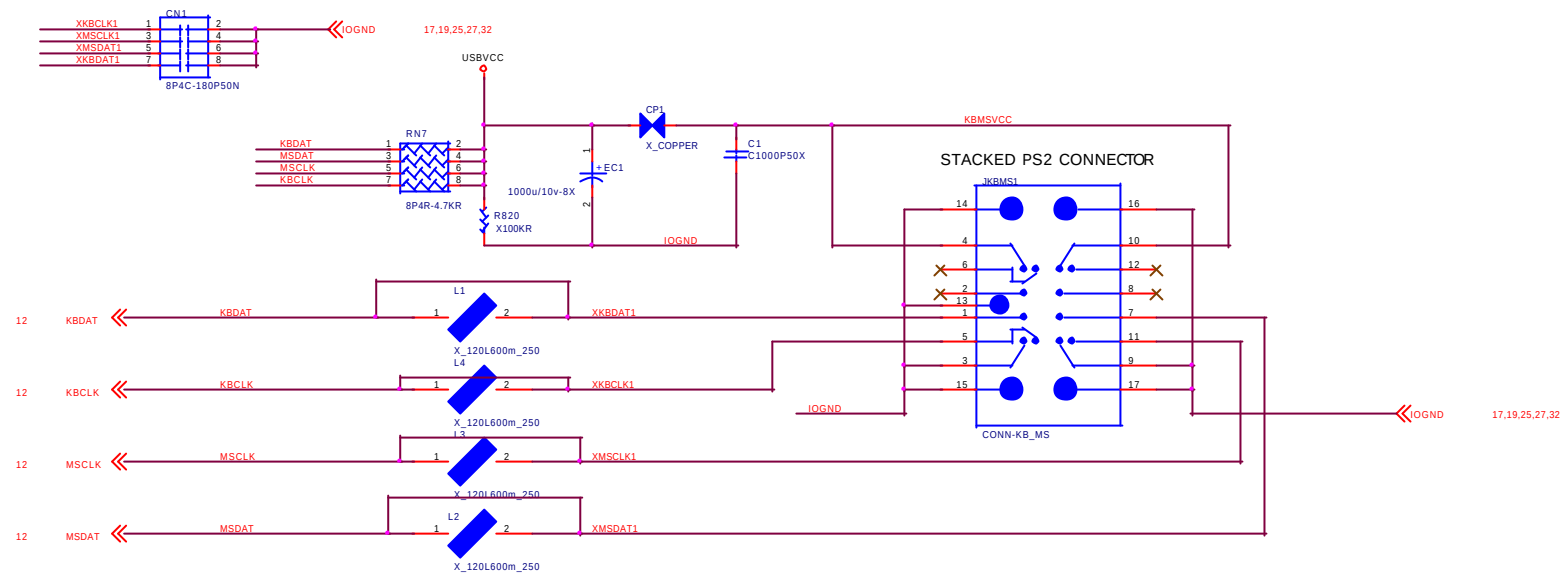


RJ45 CONNECTOR

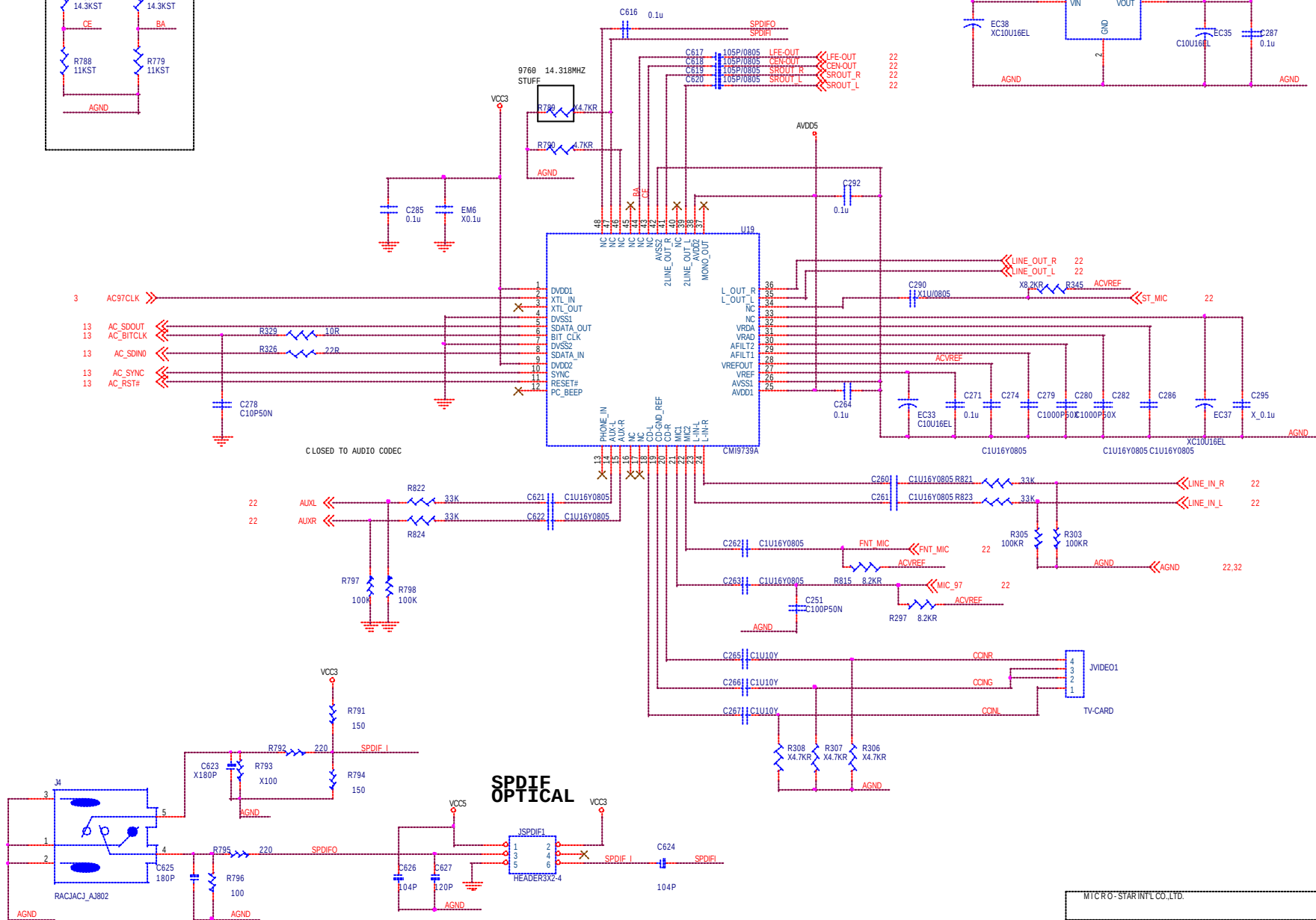
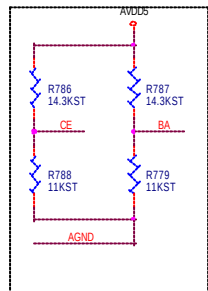


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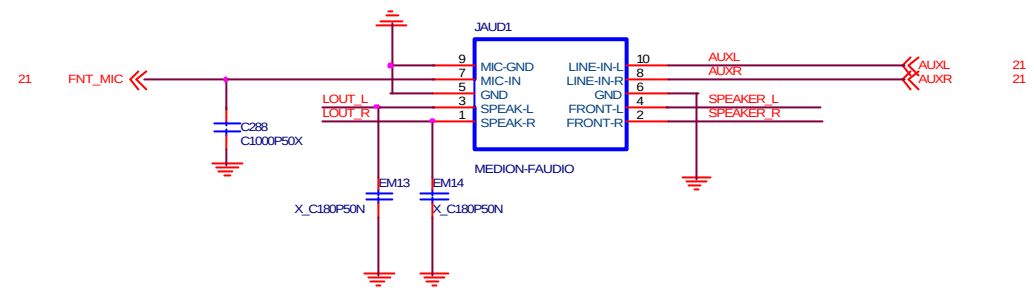
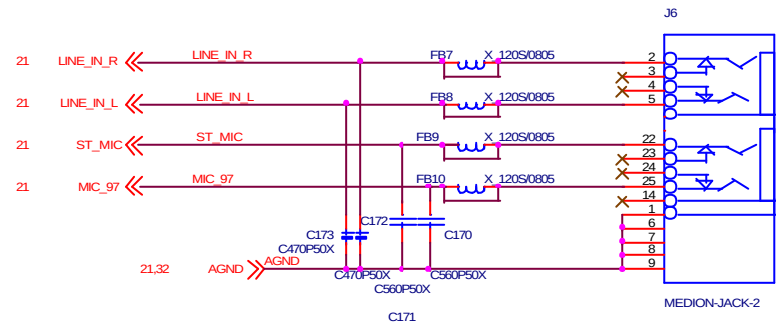
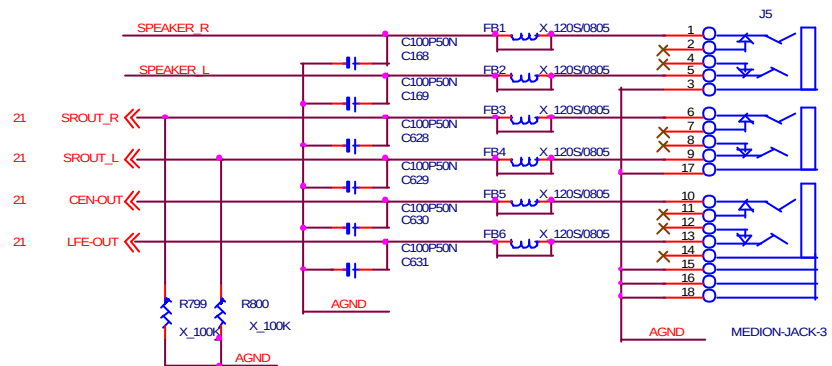
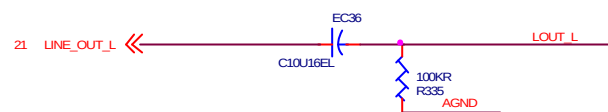
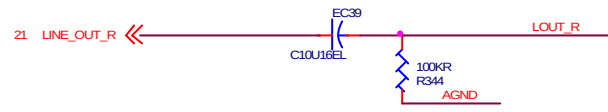
KEYBOARD/MOUSE PORTS



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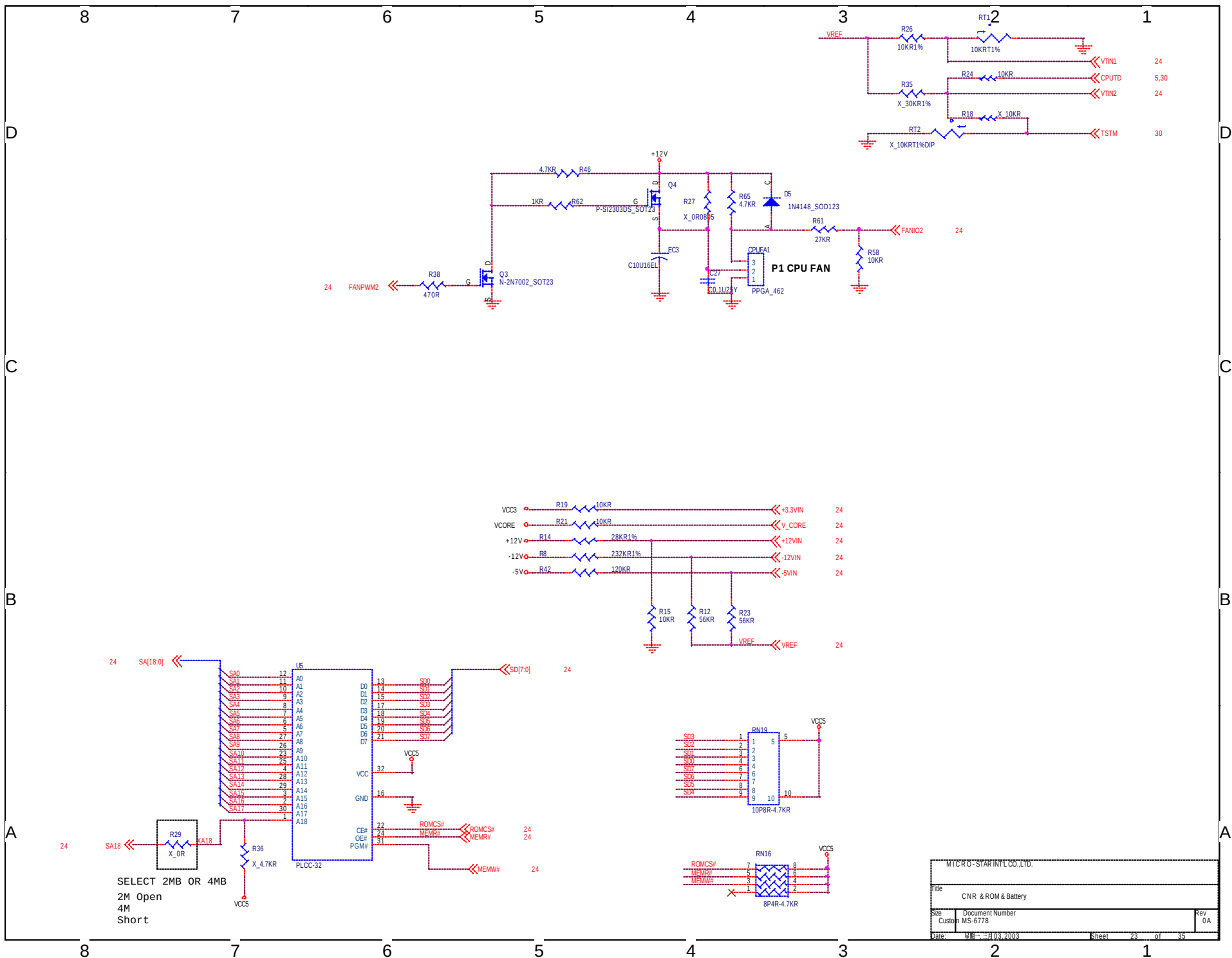


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AC'97 CODEC			
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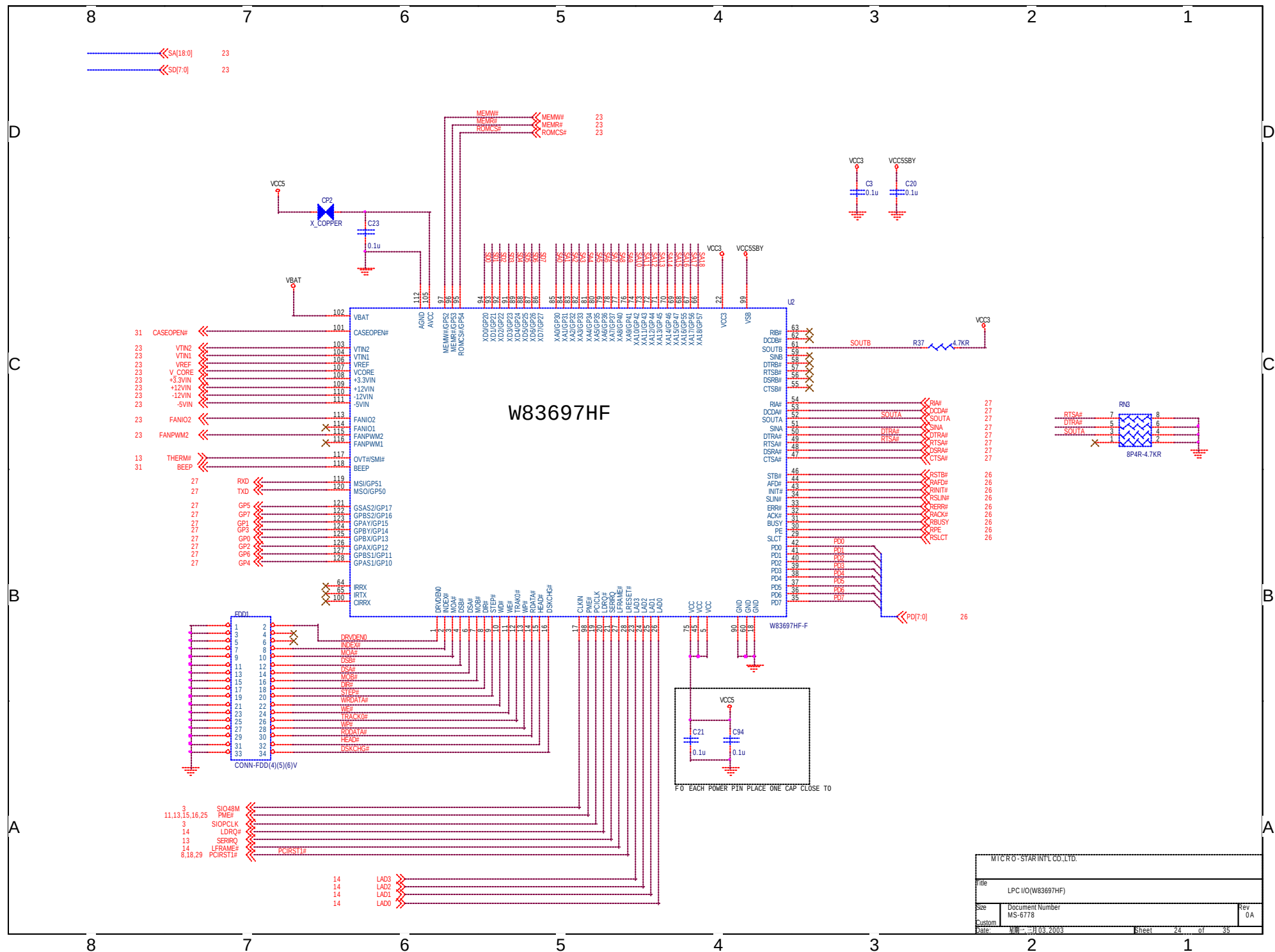


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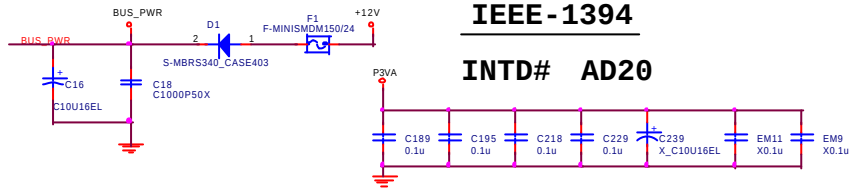
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CNR & ROM & Battery			
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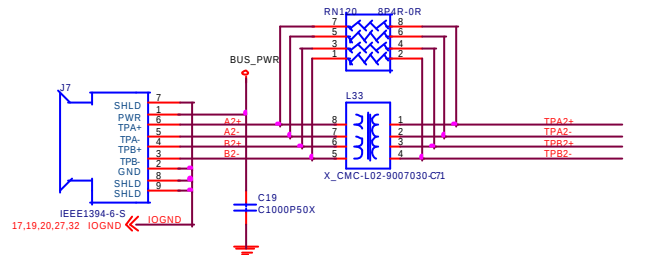
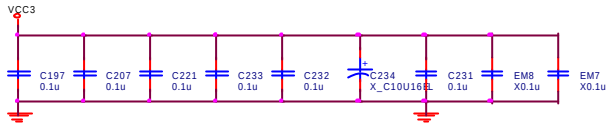
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IEEE-1394

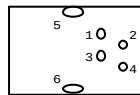
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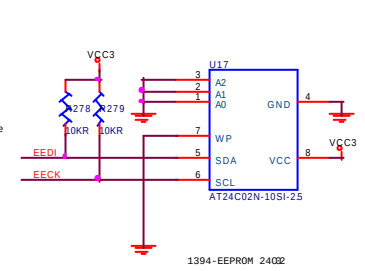
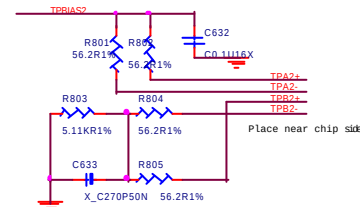
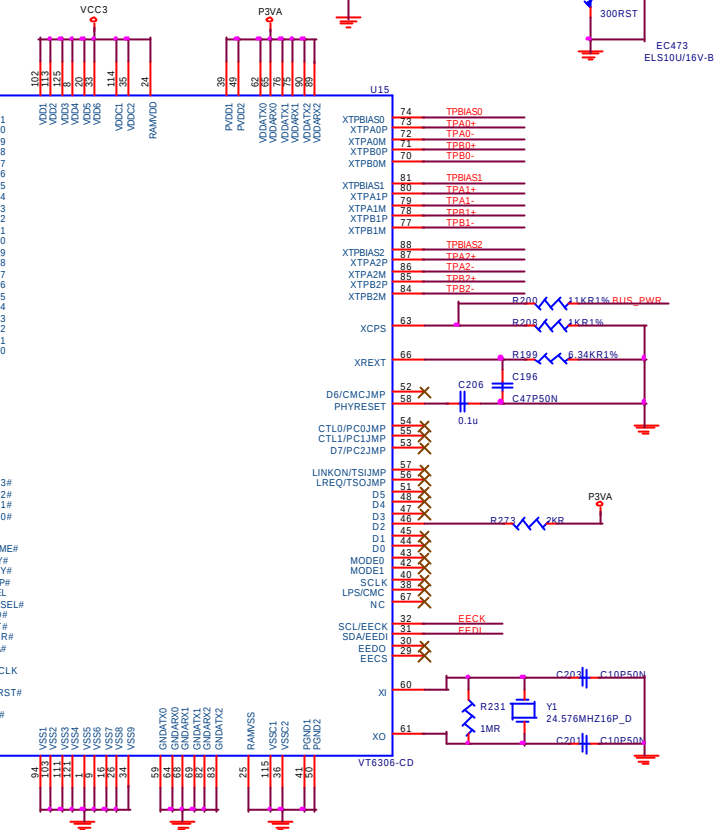
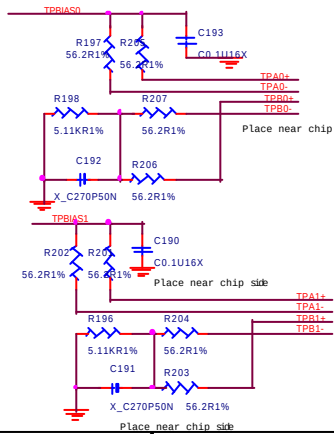
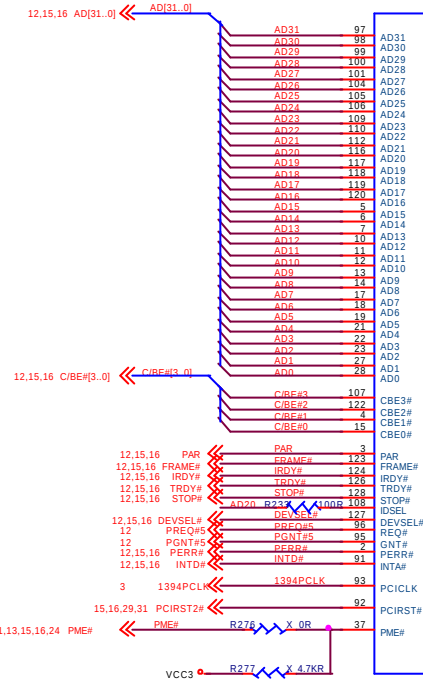
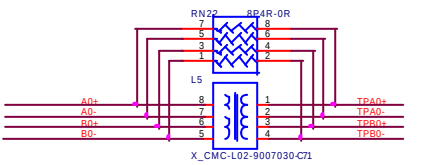
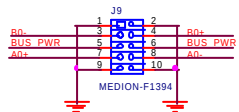
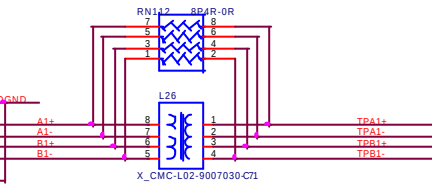
NEAR EACH POWER PIN



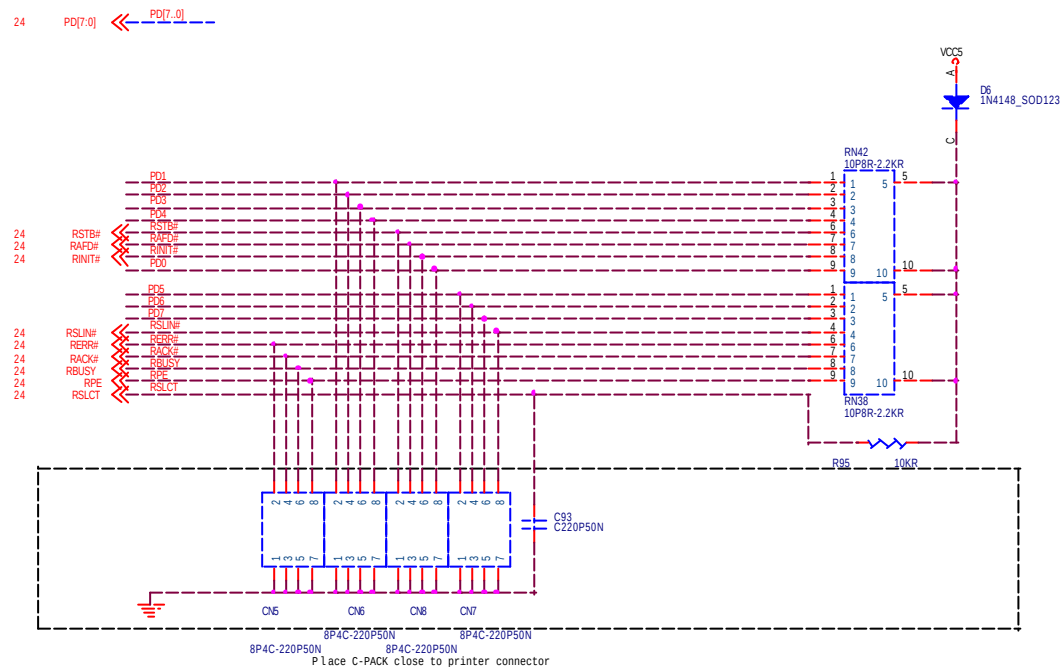
MINI 4PIN



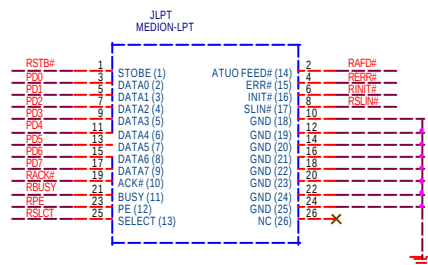
IEEE1394-4



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PARALLAL PORT



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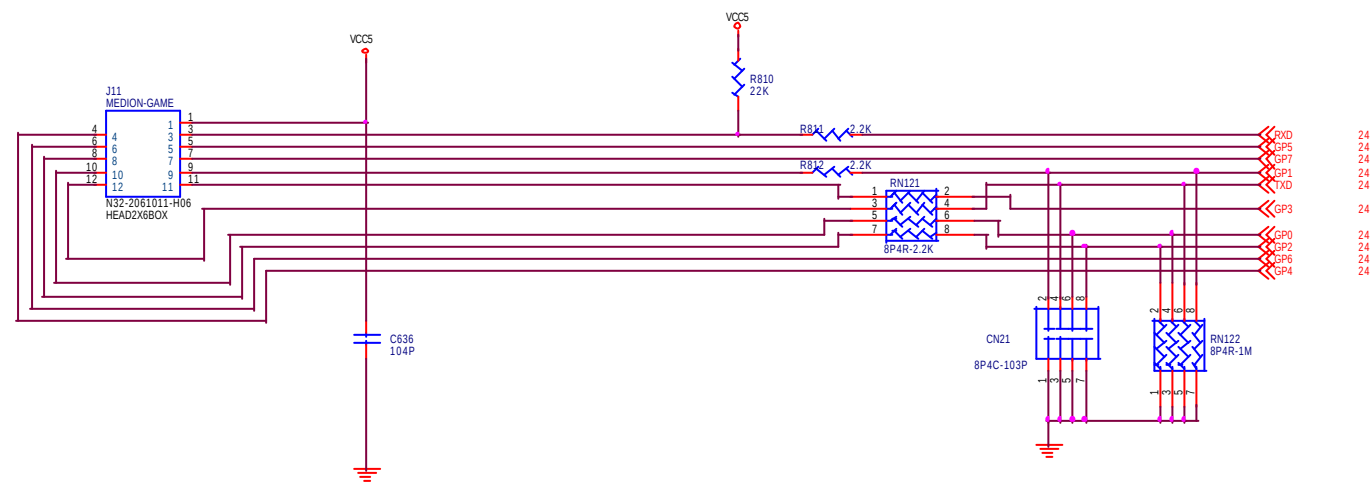
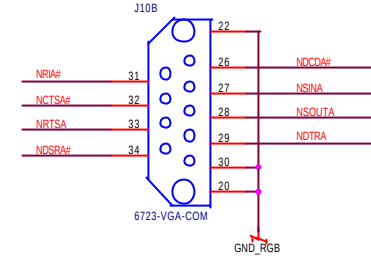
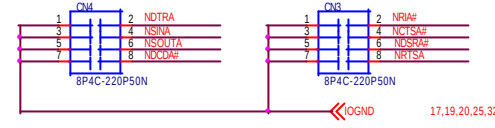
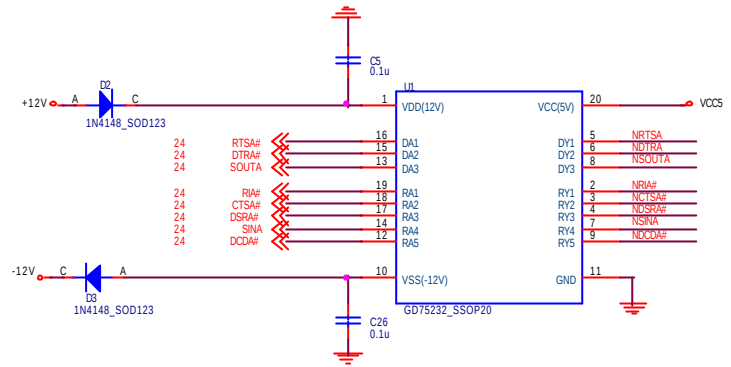
File Parallel Port

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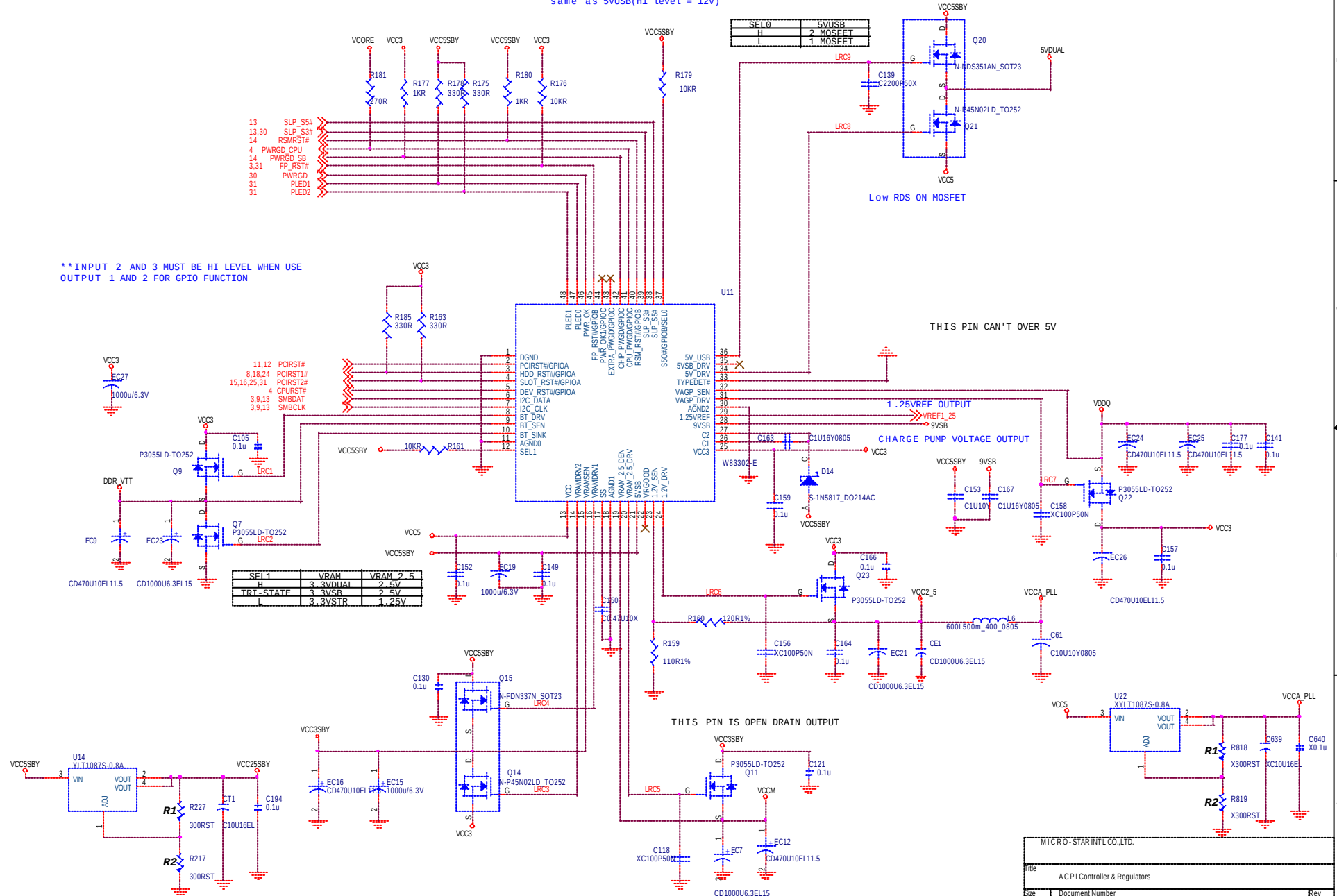
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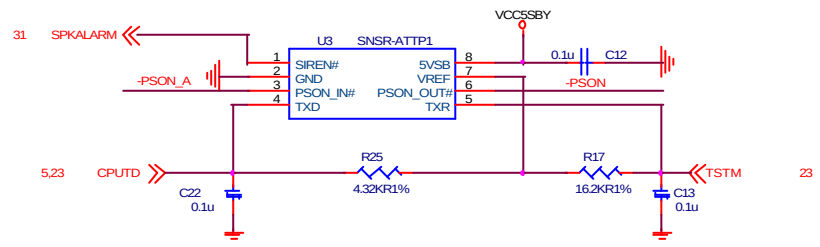
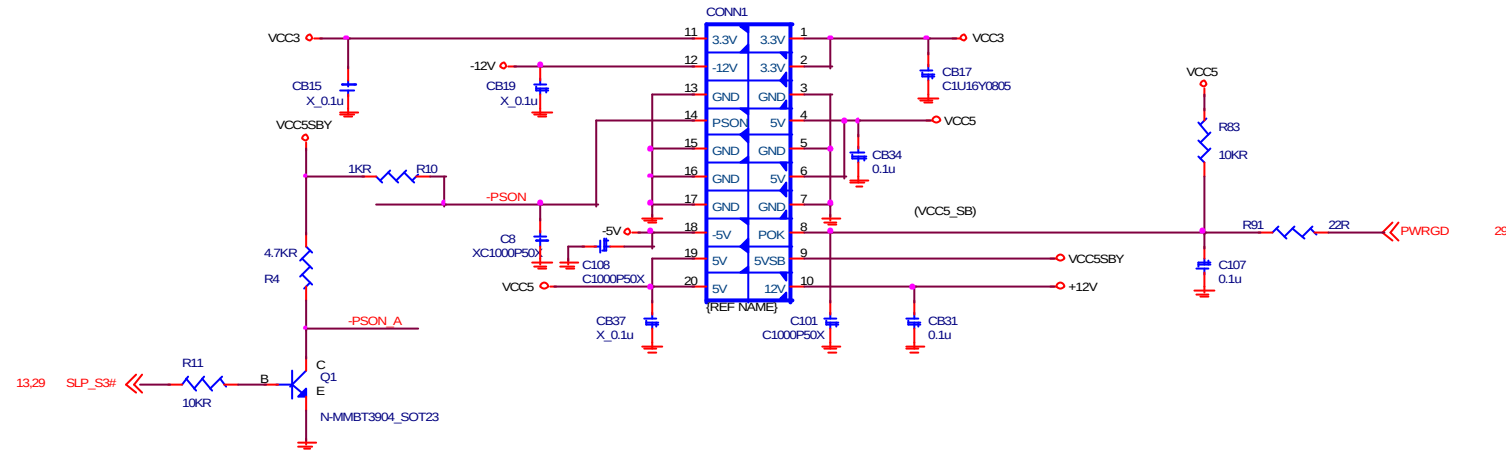


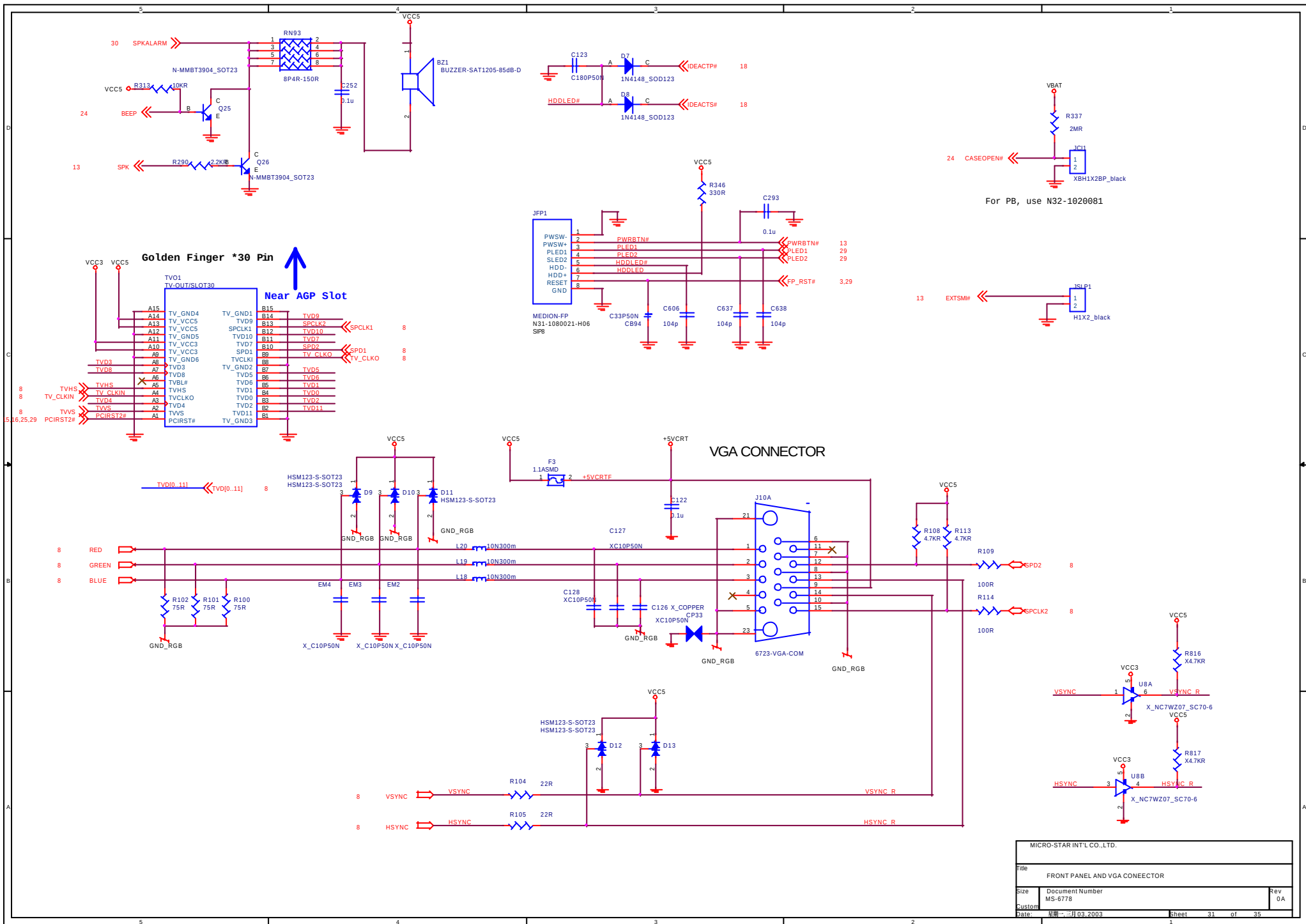
**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

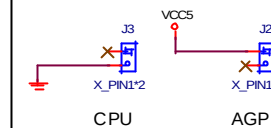
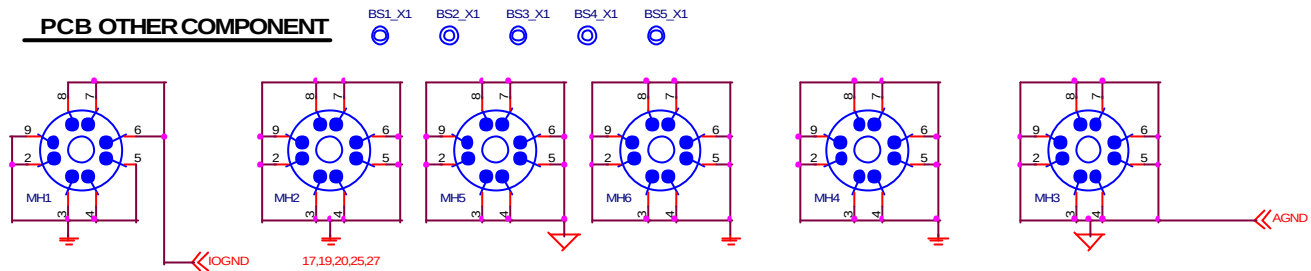


ATX CONNECTOR

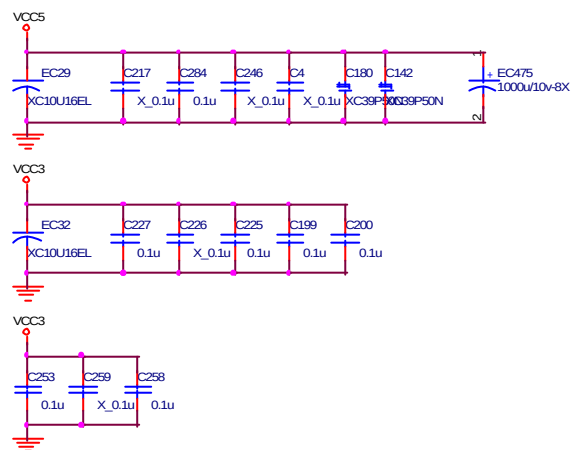
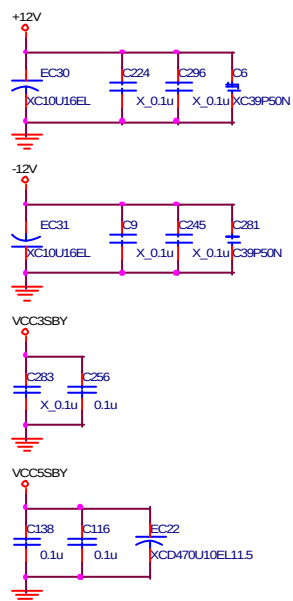




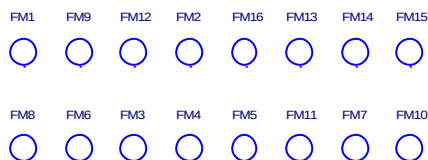
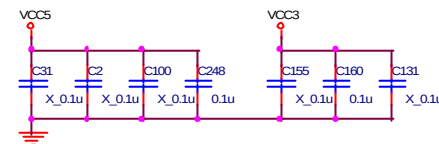
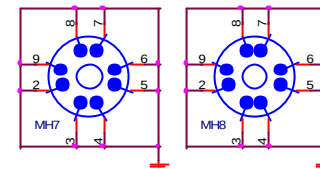
PCB OTHER COMPONENT



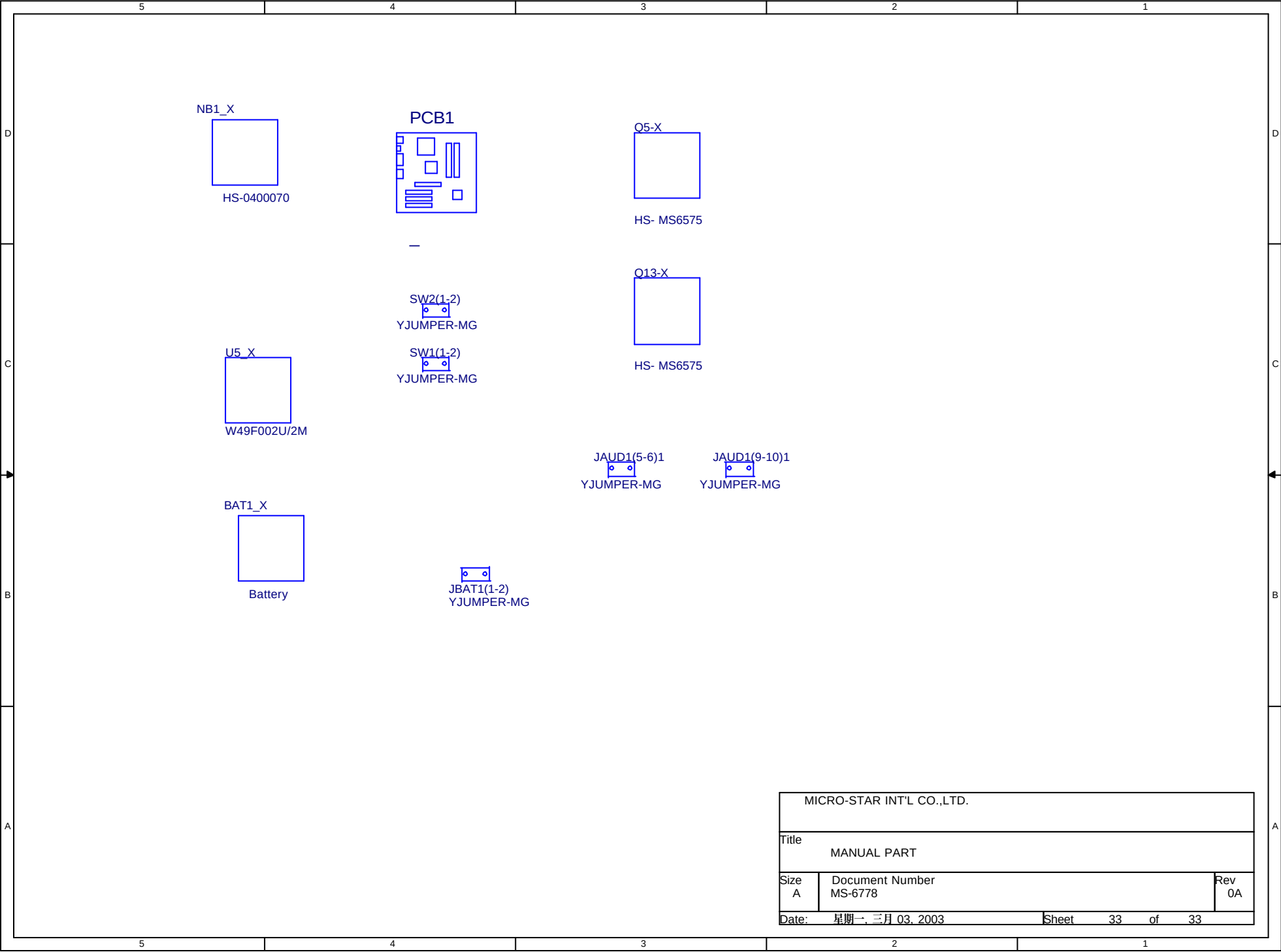
System Decoupling Capacitors



High Freq. return current decoupling



MICRO-STAR INT'L CO.,LTD.			
Title			
DECOUPLING CAPACITOR			
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GPIO FUNCTION

VT8235 GPIO Function Define

PIN NAME	Default Function	Function define	Pull up / down
GP00 (VSUS33)	GP00	SUSLED (Power LED)	Pull up to 3VDUAL
GP01/SUSA#(VSUS33)	SUSA#	NA	
GP02/SUSB#(VSUS33)	SUSB#	SUSB#	
GP03/SUSST1#(VSUS33)	SUSST1#	SUSST#	
GP04/SUSCLK(VSUS33)	SUSCLK	CTL_PLED1# (Power LED)	
GP05/CPUSTP#	CPUSTP#	NA	Pull up to VCC3
GP06/PCISTP#	PCISTP#	NA	Pull up to VCC3
GP07/SLP#	GP07	NA	
GP08/GPI8/IPBIN0	GPI8	JPWD1	Pull up to VCC3
GP09/GPI9/IPBIN1	GPI9	JBAT1	Pull up to VCC3
GP010/GPI10/IPBRDFR	GPI10	HWID1	Pull up to VCC3
GP011/GPI11/IPBRDCK	GPI11	HWID3	Pull up to VCC3
GP012/GPI12/IPBOUT0	GPI12	ROMLOCK	
GP013/GPI13/IPBOUT1	GPI13	NA	
GP014/GPI14/IPBTDFR	GPI14	HWID0	Pull up to VCC3
GP015/GPI15/IPBTDCCK	GPI15	HWID2	Pull up to VCC3
GP016/SA16/STRAP	SA16	LDT Freq Strapping Bit0	
GP017/SA17/STRAP	SA17	LDT Freq Strapping Bit1	
GP018/SA18/STRAP	SA18	LDT Width (Low=8 Bit)	
GP019/SA19/STRAP	SA19	Fast Command (Low=Disable)	
GP020/GPI20/ACSDIN2/PCS0#/EI	GPI20	NA	Pull down to GND
GP021/GPI21/ACSDIN3/PCS1#/SLPBTN#	GPI21	NA	Pull down to GND
GP022/GPI22/IOR#	GPI22	NA	Pull up to VCC3
GP023/GPI23/IOW#	GPI23	NA	Pull up to VCC3
GP024/GPI24/GPIOA	GPI24	NA	Pull up to VCC3
GP025/GPI25/GPIOC	GPI25	NA	Pull up to VCC3
GP026/GPI26/SMBDT2 (VSUS33)	SMBDT2	SMBDATA2/Slave SMBUS	Pull up to 3VDUAL
GP027/GPI27/SMBCK2 (VSUS33)	SMBCK2	SMBCLK2/Slave SMBUS	Pull up to 3VDUAL
GP028/GPI28/APICD0/APICCS#		NA	Pull up to VCC3
GP029/GPI29/APICD1/APICACK#		NA	Pull up to VCC3
GP030/GPI30/GPIOD	GPI30	NA	Pull up to VCC3
GP031/GPI31/GPIOE	GPI31	NA	Pull up to VCC3

PIN NAME	Default Function	Function define	Pull up / down
GPI0 (VBAT)	GPI0	NA	Pull up to VBAT
GPI1 (VSUS33)	GPI1	ATADET0=>Detect IDE1 ATA100/66	Pull up to 3VDUAL
GPI2/EXTSMI# (VSUS33)	EXTSMI#	EXTSMI#	Pull up to 3VDUAL
GPI3/RING# (VSUS33)	RING#	RING#	Pull up to 3VDUAL
GPI4/LID# (VSUS33)	LID#	ATADET1=>Detect IDE2 ATA100/66	Pull up to 3VDUAL
GPI5/BATLOW# (VSUS33)	BATLOW#	NA	Pull up to 3VDUAL
GPI6/PME#		PCI_PME#	Pull up to 3VDUAL
GPI7/SMBALRT#	GPI7	NA	Pull up to 3VDUAL
GPI16/INTRUDER# (VBAT)	INTRUDER#	NA	Pull up to VBAT
GPI17/CPUMISS	CPUMISS	NA	Pull up to 3VDUAL
GPI18/AOLGP1/THRM#	AOLGP1	THRM#	Pull up to 3VDUAL
GPI19/IORDY	IORDY	NA	Pull up to VCC3

PCI Routing

DEVICES	INT#	IDSEL	REQ#/GNT#	CLOCK
PCI SLOT 1	INT#A INT#B INT#C INT#D	AD16	PREQ#1 PGNT#1	PCICLK1
PCI SLOT 2	INT#B INT#C INT#D INT#A	AD17	PREQ#2 PGNT#2	PCICLK2
PCI SLOT 3	INT#C INT#D INT#A INT#B	AD18	PREQ#3 PGNT#3	PCICLK3
PCI SLOT 2 (MEDION 2nd)	INT#A	AD19	PREQ#4 PGNT#4	PCICLK4
1394	INT#D	AD25	PREQ#5 PGNT#5	1394_PCLK
LAN	INT#A	AD26	PREQ#0 PGNT#0	LAN_PCLK

Micro Star Restricted Secret		
Title	GPIO Spec.	Rev
Document Number	MS-6778	0A
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GERBER OUT 03/03/2003

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