VISE (MS-6715)

Version 0C
10/21/2002 Updated

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.0G & Above

System Chipset:

Intel Springdale - GMCH (North Bridge)
Intel ICH5 (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM
AC'97 Codec -- AD1981B
LPC Super I/O -- LPC47B387
LAN -- CSR Interface
CLOCK -- ICS952606 / CY28405
H/W Monitoring -- ADM1027

Main Memory:

DDR2700 * 4 (Max 4GB)

Expansion Slots:

PCI2.3 SLOT * 3
AGP4X/8X SLOT * 1

Intersil PWM:

Controller: HIP6556B
Driver: HIP6602B * 2

Regulators

System : FAN5236

MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

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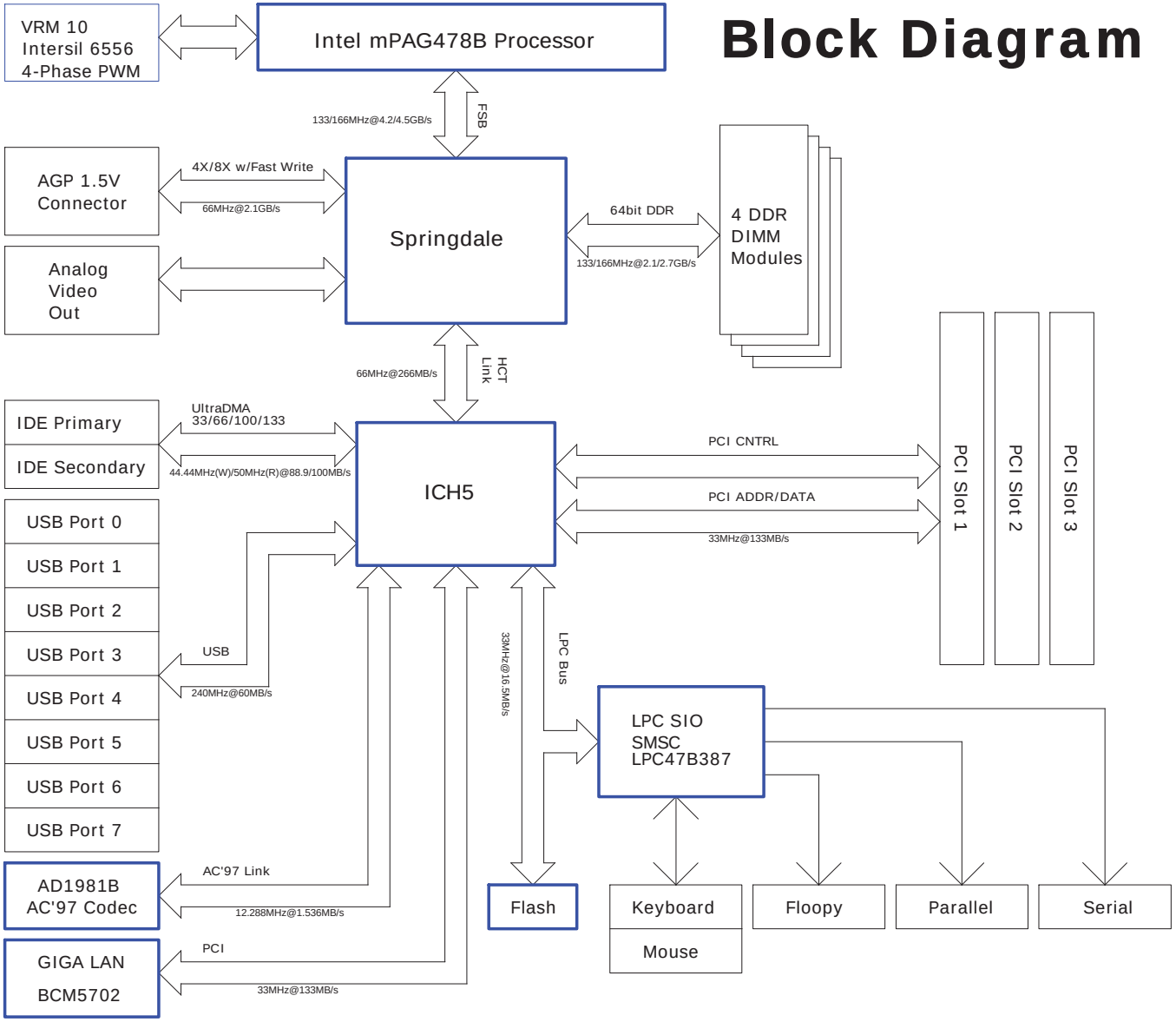
Block Diagram



MICRO-STAR INt'L CO., LTD.		
H/W Project Leader : Andy Chen H/W Project Engineer : Prudence Wang		
Title	BLOCK DIAGRAM	
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Revision Initial ver: 0AE0 on 07/31/2002

Schematic Initial on July 31.

Revision change list from ver: 0AE0 to ver: 0AE1 on 08/01/2002

Sheet 1: Modify some txts.

Sheet 2: Modify some txts.

Sheet 16: Move Lan connector to page 26.

Sheet 25: Modify some block for customer request, detail list on below:

(1) Modify 5v USB power supplier.

(2) Modify 5V main power circuit.

(3) Modify GMCH VTT voltage supplier.

(4) Add GMCH VTT reference voltage circuit.

Sheet 26: Modify some block for customer request, detail list on below:

(1) Modify 3V standby power supplier.

(2) Change VTT_DDR to LP2995.

(3) Add lan magnetic circuit.

(4) Modify Lan connector.

(5) Add 1.5V standby voltage.

Revision change list from ver: 0AE1 to ver: 0AE2 on 08/09/2002

Sheet 8: Change VTT_FSB to capacitors termination on pin A15 and A21.

Sheet 9: Change VCC_DDR to capacitors termination on pin E35,E35,AA35,AR21 and AR15.

Sheet 27: Change some bulk caps from 2200uF to 560uF.

Revision change list from ver: 0AE2 to ver: 0AE3 on 08/13/2002

Sheet 12: Modify some block for customer request, detail list on below:

(1) Delete GP14 and GP15 on pin U21 and pin T20 on ICH5.

(2) Add CHASIS_ID2 on pin V3 on ICH5.

(3) Delete USB6+, USB6-, USB7+, and USB7-.

(4) Change FRONT_USB_DET# from pin C13 to pin D13 on ICH5.

Sheet 13: Modify some block for customer request, detail list on below:

(1) Modify clock generator library.

(2) Change PCI clock label.

(3) Add strapping resistors.

Sheet 17: Delete some caps on VCC_DDR.

Sheet 18: Delete some caps on VCC_DDR.

Sheet 19: Delete some AGP termination resistors.

Sheet 20: Change PCI clock label.

Sheet 22: Modify some block for customer request, detail list on below:

(1) Delete 2 ports USB, and one USB power.

(2) Removed LAN connector to here.

Sheet 24: Modify some block for customer request, detail list on below:

(1) Change from GP14 to NC on pin 10 of F_P1.

(2) Change from NC to CHASIS_ID2 on pin 15 of F_P1.

(3) Change from GP15 to CHASIS_ID0 on pin 17 of F_P1.

(4) Change from GND to CHASIS_ID1 on pin 18 of F_P1.

(5) Pull VCC3_SB to pin C13 on ICH5.

Sheet 27: Modify some block for customer request, detail list on below:

(1) Change R473 from 1Kohm to NC.

(2) Change R475 from 0 ohm to NC.

(3) Change some bulk caps from 2200uF to 560uF.

Sheet 28: Delete R89,R90,R91, and R92.

Revision change list from ver: 0AE3 to ver: 0AE4 on 8/14/2002

Sheet 13: Modify clock generator library.

Sheet 14: Modify some block for customer request, detail list on below:

(1) Change SERIAL PORT 2 connector to 10 pin center-keyed shrouded header.

(2) Add TI GD75232.

(3) Change label PS_ON to PS_ON#.

Sheet 15: Modify some block for customer request, detail list on below:

(1) Delete Q7,Q8,Q10,Q11,Q12,Q34.

(2) Modify this page same as reference schematic.

Sheet 17: Exchange pin 103 and pin 167 on DIMM1 and DIMM2.

Sheet 18: Exchange pin 103 and pin 167 on DIMM3 and DIMM4.

Sheet 21: Modify some block for customer request, detail list on below:

(1) Add 33 ohm series resistors on Data 15:0 on Primary IDE.

(2) Add 33 ohm series resistors on Data 15:0 on Secondary IDE.

(3) Delete U12, NC7WZ08.

Sheet 24: Modify some block for customer request, detail list on below:

(1) Delete Q31, R376, R377,and R378.

(2) Change label PS_ON to PS_ON#.

(3) Delete U12, NC7WZ08.

Sheet 25: Change Q25 from 2N3904 to 2N7002.

Revision change list from ver: 0AE4 to ver: 0AE5 on 08/16/2002

Sheet 6: Modify some block for customer request, detail list on below:

(1) All TESTHI pull up resistors change from 51ohm to 62ohm.

(2) Delete OPTIMZ label.

Sheet 7: Modify some block for customer request, detail list on below:

(1) Delete EC1 and EC2.

(2) Change L1 and L2 from 4.7uH to 10uH.

Sheet 8: Modify some block for customer request, detail list on below:

(1) Separate from VCCA_FSB and add 0.1uF cap to GND on pin A31.

(2) Change C225 from 0.22uF to 0.47uF.

Sheet 10: Modify some block for customer request, detail list on below:

(1) Add 2pins header to pin T20.

(2) Change pin D14 and C14 to OC#2 signal.

(3) Change label OC#2 to OC#3.

(4) Change label OC#3 to OC#7.

(5) Add label CI_VREF and CI_SWING to pin AF4 and AF2.

(6) Delete R65 on pin AG10.

Sheet 11: Modify some block for customer request, detail list on below:

(1) Add 0.1uF cap to pin F19.

(2) Add 0.1uF cap to pin Y5, AA4 and AB4.

(3) Add 0.1uF cap to pin F7 and F8.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Change R102 from 0ohm to 10Kohm.

Sheet 13: Modify some block for customer request, detail list on below:

(1) Change R154 and R152 from 300ohm to 330ohm.

(1) Change R151 from 2Kohm to 2.2Kohm.

Sheet 15: Modify some block for customer request, detail list on below:

(1) Add 47ohm resistor to AC_SDIN0.

(2) Change R199 from 10ohm to 47ohm and add 47pF cap.

(3) Change R219 and R209 from 4.7Kohm to 100ohm.

(4) Change R202, R203, R207, R208 from 6.8Kohm to 4.7Kohm.

(5) Add divide 1Kohm pull down resistor to OUT_R and OUT_L signals.

(6) Delete C71.

Revision change list from ver: 0AE4 to ver: 0AE5 on 08/16/2002

Sheet 17: Modify some block for customer request, detail list on below:

(1) Add two 75 ohm divide resistors in DDR_VREF.

(2) Change 110ohm to 56ohm on Rterm array resistors.

(3) Add two divide 75ohm resistors pin 1.

Sheet 18: Modify some block for customer request, detail list on below:

(1) Add two 75 ohm divide resistors in DDR_VREF.

(2) Change 110ohm to 56ohm on Rterm array resistors.

(3) Add two divide 75ohm resistors pin 1.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Add 2pins header for support Prochot latch.

Sheet 21: Modify some block for customer request, detail list on below:

(1) Change R299 and R295 from 4.7Kohm to 8.2Kohm.

Sheet 22: Modify some block for customer request, detail list on below:

(1) Add one usb power circuit to seperate port 0,1 and 2,3.

(2) Change R315 and R313 from 21Kohm to 470Kohm.

(3) Change R320 and R319 from 51Kohm to 560Kohm.

(4) Change C134 from 470pF to 1000pF.

Sheet 24: Modify some block for customer request, detail list on below:

(1) Change R380 from 330ohm to 68ohm.

Sheet 27: Modify some block for customer request, detail list on below:

(1) Change CT41-CT44 from 2200uF to 560uF.

Sheet 28: Modify some block for customer request, detail list on below:

(1) Change label OC#3 to OC#7.

(2) Add some divide resistors to CI_VREF and CI_SWING signals.

(3) Change R1 from 100ohm to 200ohm and add a 200ohm resistor pull to VTT voltage.

(4) Delete R14. and ITP_VCC direct connect to Vccp.

(5) Change BPM# from 51ohm to 62ohm.

(6) Change R30 from 220ohm to 200ohm.

(7) Add two 0ohm resistors to support ITP or USB_ITP port.

(6) Change R17 from 27ohm to 47ohm.

Revision change list from ver: 0AE5 to ver: 0AE6 on 08/19/2002

Sheet 25: Modify some block for customer request, detail list on below:

(1) Add 300 ohm resistor from BOOT to VCC_VID and change R423 to 10Kohms.

(2) Change R411 and R415 to 3V_SW_CTRL# signal.

Sheet 27: Modify some block for customer request, detail list on below:

(1) Add Northwood FB network and Prescott FB network to VRM controlled by BOOT.

(2) Change 110ohm to 56ohm on Rterm array resistors.

(3) Change R460,R464,R467,and R470 from 2.83Kohm to 3.3Kohm.

Sheet 28: Add teo 10Kohm pull down resistors to RSMRST# and ICH_GD signals.

Revision change list from ver: 0AE6 to ver: 0AE7 on 08/20/2002

Sheet 13: Modify some block for customer request, detail list on below:

(1) Change R495 from ICHPCLK to LANPCLK signal.

(2) Change R496 from FWHPCLK to PCICLK0 signal.

(3) Change R497 from LANPCLK to PCICLK1 signal.

Sheet 16: Delete CB89,CB90,CB88,CB114, CB117, and CB118.

Sheet 17: Change all component from 0603 to 0402.

Sheet 18: Change all component from 0603 to 0402.

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title: REVISION HISTORY - 1

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Revision change list from ver: 0AE7 to ver: 0AE8 on 08/21/2002

Sheet 7: Change some caps of north side to not install.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Add LPC_DRQ#1 label on pin R2 on ICH5.

(2) Change pin Y12 from INTRUDER# to HOOD_SENSE#.

Sheet 13: Modify some block for customer request, detail list on below:

(1) Remove R143 and R142. Connect FWH RST# signal directly to PCIRST#.

(2) Delete R154,Q5,Q3, and R151.

(3) Change R152 from 330 ohm to 8.2K ohm.

(4) Add one resistor to SEC_PCLK signal and share with SIO_PCLK.

(5) Delete INIT# BLOCK.

Sheet 14: Modify some block for customer request, detail list on below:

(1) Change pin 44 to BRD_V1.

(2) Change pin 45 to MB_ADPT_DET#.

(3) Change pin 47 to SEC_TPM_PRES.

(4) Change pin 49 to MB_ADPT_DET#.

(5) Change pin 54 to FDD_2M.

(6) Add pin 104 to 5V_IN.

Sheet 18: Change all component from 0603 to 0402.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Change TAP resistors from 4.7Kohm to 2.2Kohm.

(2) Add a 2.2Kohm pull down resistor to PCIRST#1.

Sheet 24: Add Security header.

Sheet 25: Change VCC5 & VCC3 Discharge Residual Voltage same as reference schematic.

Revision change list from ver: 0AE8 to ver: 0AE9 on 08/23/2002

Sheet 16: Support BCM4401.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Delete CT17.

(2) Change CT16 from intall to not install.

Sheet 23: Delete CB284 and R324.

Sheet 27: Change R456,R466,R479, and R489 from 1 ohm/1206 to 4.7ohm/0805.

Revision change list from ver: 0AE9 to ver: 0AEA on 08/26/2002

Sheet 11: Change Label from VCC3_SB to 3VSB.

Sheet 13: Modify some block for customer request, detail list on below:

(1) Change Label from PCIRST# to PCIRST_ICH5#.

(2) Change all pull high resistors of clock generator from VCC3V to VCC3.

Sheet 14: Modify some block for customer request, detail list on below:

(1) Change Label from VCC3_SB to 3VSB.

(2) Change pin 45 to GP25 and add a 4.7Kohm resistor to VCC3 on GP25.

(3) Add a label SYSMAG_INT on pin 61.

(4) Change pin 44 to MB_ADPT_DET#.

(5) Change pin 49 to SEC_TPM_PRES.

Sheet 15: Modify some block for customer request, detail list on below:

(1) Delete R514, R515, C81, C86, C88, C89.

(2) Change R211 & R216 to 0 ohm.

(3) Change C82 & C84 to 4.7uF.

(4) Change R209 & R219 to 4.7K.

(5) Add 0.22uF and 4.12K in series to pin1 of Front Audio Header.

(6) Add label bias circuit to pin 3 of Front Audio Header.

(7) Add X_330 ohm from OUT_L to junction of C218 & R504.

Sheet 16: Change Label from VCC3_SB to 3VSB.

Sheet 21: Change Label from VCC3_SB to 3VSB.

Sheet 22: Change Label from VCC3_SB to 3VSB.

Revision change list from ver: 0AE9 to ver: 0AEA on 08/26/2002

Sheet 23: Modify some block for customer request, detail list on below:

(1) Change H/W monitoring circuit.

(2) Change Fan circuit.

Sheet 24: Change Label from VCC3_SB to 3VSB.

Sheet 25: Change Label from VCC3_SB to 3VSB.

Sheet 26: Change Label from VCC3_SB to 3VSB.

Sheet 27: Change Label from VCC3_SB to 3VSB.

Sheet 28: Change Label from VCC3_SB to 3VSB.

Revision change list from ver: 0AEA to ver: 0AEB on 09/03/2002

Sheet 6: Change CPU Symbol - pin F6=GTLREF3, pin F20=GTLREF2, pin AA6=GTLREF1, pin AA21=GTLREF0.

Sheet 9: Modify some block for customer request, detail list on below:

(1) Disconnect U28 pin E34 (GMCH) directly to VREF.

(2) Add a 2.2uF cap to this pin E34.

Sheet 13: Modify some block for customer request, detail list on below:

(1) Change R135 & R139 from 1K to 10K.

(2) Add pullup resistor from BSEL0 to VCC3.

(3) Add pullup resistor from BSEL1 to VCC3.

Sheet 21: Change FB16, FB18 & FB20 to be the same as FB17, FB19 & FB21.

Sheet 25: Modify some block for customer request, detail list on below:

(1) Change Q40 & Q41 to Depletion Mode JFETs.

(2) Connect R400 to -12V.

(3) Change R399 to a 39 ohm RNET and connect in parallel to VCC5.

(4) Change R405 to a 39 ohm RNET and connect in parallel to VCC3.

(5) Move R417 from Drain of Q51 to Source.

(6) Change R417 from 150 to 866 ohms.

(7) Change R425 from 150 to 634ohms.

(8) Change R426 from 150 to 499 ohms.

Sheet 28: Change R46 & R50 to 150 ohms 1%.

Revision change list from ver: 0AEB to ver: 0AEC on 09/09/2002

Sheet 7: Delete 0.1uF caps on CPU side.

Sheet 8: Change R41 from 24.9ohm to 20ohm.

Sheet 9: Modify some block for customer request, detail list on below:

(1) Disconnect U2 pin AR31 (GMCH).

(2) Disconnect U2 pin AL35 (GMCH) and add single cap to it.

Sheet 17: Delete decoupling caps between VCC_DDR and VTT_DDR.

Sheet 18: Delete decoupling caps between VCC_DDR and VTT_DDR.

Sheet 21: Change all arrary resistors from 0603 to 0402 on all IDE.

Sheet 22: Add secondary transformer to support 10M and 100M NIC.

Revision change list from ver: 0AEC to ver: 0AED on 09/12/2002

Sheet 6: Modify some block for customer request, detail list on below:

(1) Disconnect CPU1 pin AC3, IERR# signal.

(2) Add a pull down resistor to CPU1 pin AE26, OPTIMIZ signal, and not install.

Sheet 7: Change R36 from 1Kohm to 2.43Kohm.

Sheet 11: Add RN91 to support VCCSUS1_5A,B,C voltage for ICH5.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Change net GPI12 to PS_DETECT.

(2) Add net FAN_CMD to pin U20.

(3) Change net GPI7 to PROC_HOT#.

(4) Change R102 to 390Kohm, not install ,and a resistor to GND.

(5) Delete net RTC_XI.

Sheet 14: Modify some block for customer request, detail list on below:

(1) Change net TRMTRIP# to SIO_TRMTRIP#.

(2) Delete R551, and change net 5V_IN to COMM_B_DET#.

Revision change list from ver: 0AEC to ver: 0AED on 09/12/2002

Sheet 14: Modify some block for customer request, detail list on below:

(1) Swap net BRD_V1 and FAN_CLAMP.

(2) Delete R551, and change net 5V_IN to COMM_B_DET#.

Sheet 15: Modify some block for customer request, detail list on below:

(1) Change R196 to 3.3Kohm.

(2) Add a 270pF cap to GND and AGND, not install.

(3) Add a 1uF caps to MONO_L and MONO_L_R.

(4) Add a 1uF caps to MONO_R and MONO_R_R.

(5) Change R501 and R555 to 130ohm.

(6) Change C218 from 4700pF to 0.01uF.

Sheet 17: Change net DDR_VREF to DDR_VREF1.

Sheet 18: Change net DDR_VREF to DDR_VREF2, and add two resistors.

Sheet 23: Modify some block for customer request, detail list on below:

(1) Modify H/W monitoring and FAN controller.

(2) Change U13 pin 22 from VCC_DDR to No Connect.

Sheet 24: Add PROCHOT# LED.

Sheet 25: Modify some block for customer request, detail list on below:

(1) Delete R394 and R401.

(2) Change C166 to 0.01uF.

(3) Change Q38 pin 5 and pin 6 to VCC5_STR.

(4) Change Q39 pin 5 and pin 6 to VCC3.

(5) Change Q38 pin 3 to PHASE_2V5.

(6) Change Q39 pin 3 to PHASE_1V5.

(7) Change DZ5 to VCC5.

(8) Change U15 pin 15 and 16 to VCC5_STR.

Sheet 26: Modify some block for customer request, detail list on below:

(1) Add VR THERMAL BLOCK.

(2) Add ICH5 VCCSUS1_5A, B, and C voltage regulatot to support this version fail chipset.

Sheet 28: Modify some block for customer request, detail list on below:

(1) Delete R35, IERR#.

(2) Change net GPI12 to PS_DETECT.

(3) Change net GPI7 to PROC_HOT#.

(4) Add Thermtrip Translation Block.

(5) Change RN3 pin 2 to No Connect.

(6) Delete C36, C37, and R100.

(7) Delete net RTC_XI.

Revision change list from ver: 0AED to ver: 0AEE on 09/18/2002

Sheet 11: Change U3 pin A5 from PREQ#A to BRD_ID1. Delete R72.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Change U3 pin G23 from BRD_ID1 to SATALED#.

(2) Change U3 pin U22 from RISER#2 to No Connect.

(3) Change U3 pin T1 from BRD_ID0 to NIC_ENABLE#.

(4) Change U3 pin V2 from SIO_PME# to PCI_PME#.

(5) Change U3 pin F21 from CH_FAN_OVRD to BRD_ID0.

Sheet 13: Change R625 and R626 to 1Kohm.

Sheet 14: Modify some block for customer request, detail list on below:

(1) Change U6 pin 29 from COMM_B_DET# to DDRC and add pull up to VCC3.

(2) Change R191 from 3VSB to VCC3.

MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title: REVISION HISTORY - 2

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Revision change list from ver: 0AED to ver: 0AEE on 09/18/2002

Sheet 14: Modify some block for customer request, detail list on below:
- (3) Change U6 pin 8 from PLED to SUSLED.
- (4) Change U6 pin 13 from SUSLED to PLED.
- (5) Change U6 pin 14 from SIO_PME# to RI#.
- (6) Change U5 & U22 from 75232 to TI75185.

Sheet 19: Change U11 pin 55 from RISER#2 to No Connect. Delete R148.

Sheet 21: Modify some block for customer request, detail list on below:
- (1) Add 1K pull up from IDEA_RST# to VCC5.
- (2) Add 1K pull up from IDEB_RST# to VCC5.

Sheet 22: Delete U32.

Sheet 23: Change CT53 and CT54 to 25V part.

Sheet 25: Change Q51 and Q53 to FDV301N.

Sheet 26: Add U35 for support sata led on front panel.

Sheet 28: Modify some block for customer request, detail list on below:
- (1) Add R36 62 ohms from TRMTRIP# to VCCP.
- (2) Change R80 from TRMTRIP# to ICH_TRMTRIP#.

Revision change list from ver: 0AEE to ver: 0AEF on 09/22/2002

Sheet 14: Modify some block for customer request, detail list on below:
- (1) Change KBGND to GND on COM2.
- (2) Delete FB3.
- (3) Change U6 pin 14 from SIO_PME# to RI#.
- (4) Change U5 & U22 from 75232 to TI75185.

Sheet 19: Change U11 pin 55 from RISER#2 to No Connect. Delete R148.

Revision change list from ver: 0AEF to ver: 0AE10 on 09/27/2002

Sheet 7: Modify some block for customer request, detail list on below:
- (1) Change EC32,46,5,30,15,23,49,45,25,and EC37 to not install.
- (2) Change EC 8,42,21,43,38,28,29,36,17,16,39, and EC35 to not install.

Sheet 16: Modify some block for customer request, detail list on below:
- (1) Change U9 pin H2 from PIRQ#H to PIRQ#E.
- (2) Change U9 pin C3 from PGNT#5 to PGNT#0.
- (3) Change U9 pin J3 from PREQ#5 to PREQ#0.

Sheet 19: Modify some block for customer request, detail list on below:
- (1) Change AGP1 pin A6 from PIRQ#A to PIRQ#C.
- (2) Change AGP1 pin B6 from PIRQ#B to PIRQ#D.
- (3) Change U11 pin 5 from PIRQ#A to PIRQ#F.
- (4) Change U11 pin 66 from PIRQ#B to PIRQ#G.
- (5) Change U11 pin 6 from PIRQ#C to PIRQ#A.
- (6) Change U11 pin 67 from PIRQ#D to PIRQ#C.

Sheet 20: Modify some block for customer request, detail list on below:
- (1) Change PCI1 pin A17 from PGNT#0 to PGNT#5.
- (2) Change PCI1 pin B18 from PREQ#0 to PREQ#5.

Sheet 22: Change NIC_IDESEL to NIC_IDSEL.

Sheet 27: Change CT35 to not install.

Revision change list from ver: 0AE10 to ver: 0AE11 on 09/30/2002

Sheet 16: Modify some block for customer request, detail list on below:
- (1) U9 pin P9 should connect to U31 pin 4.
- (2) U9 pin N9 should connect to U31 pin 3.
- (3) U31 pin 1 should connect to U9 pin P10 (EE_DATA).
- (4) U31 pin 2 should connect to U9 pin M10 (EE_CLK).

Sheet 28: Add SMBBUS isolation block.

Revision change list from ver: 0AE11 to ver: 0AE12 on 10/01/2002

Sheet 13: Modify some block for customer request, detail list on below:
- (1) Change SMBCLK to SMB_CLK.
- (2) Change SMBDATA to SMB_DATA.

Sheet 17: Modify some block for customer request, detail list on below:
- (1) Change SMBCLK to SMB_CLK.
- (2) Change SMBDATA to SMB_DATA.

Sheet 18: Modify some block for customer request, detail list on below:
- (1) Change SMBCLK to SMB_CLK.
- (2) Change SMBDATA to SMB_DATA.

Sheet 19: Add some caps between VCC3 and VCC5.

Sheet 20: Add some caps on VCC3 and VCC5.

Sheet 23: Modify some block for customer request, detail list on below:
- (1) Change SMBCLK to SMB_CLK.
- (2) Change SMBDATA to SMB_DATA.

Revision change list from ver: 0AE12 to ver: 0BE0 on 10/16/2002

Sheet 8: Change U28 to install and R526 to not install.

Sheet 10: Add pin D10 to GND.

Sheet 11: Change RN91 to not install.

Sheet 12: Modify some block for customer request, detail list on below:
- (1) Add RSMRST# pull high resistor.
- (2) Add PWRBTN# pull high resistor.
- (3) Change R628 to R102 to install.

Sheet 13: Add ICH66 pull down resistor.

Sheet 14: Modify some block for customer request, detail list on below:
- (1) Change RSLCT to SLCT.
- (2) Change RPE to PE.

Sheet 16: Modify some block for customer request, detail list on below:
- (1) Add two resistors to VDD_PCI voltage.
- (2) Delete DZ3.

Sheet 17: Add some caps on VCC_DDR voltage.

Sheet 18: Add some caps on VTT_DDR voltage.

Sheet 22: Change LAN connector to popular 8pins.

Sheet 25: Modify some block for customer request, detail list on below:
- (1) Change FAN5236 circuit.
- (2) Change VCC5_STR circuit.
- (3) Change Q50 to TO-252.
- (4) Change VTT circuit some components to not install.

Sheet 26: Move 1_5VSB voltage.

Sheet 28: Change Q95 to 2N3906.

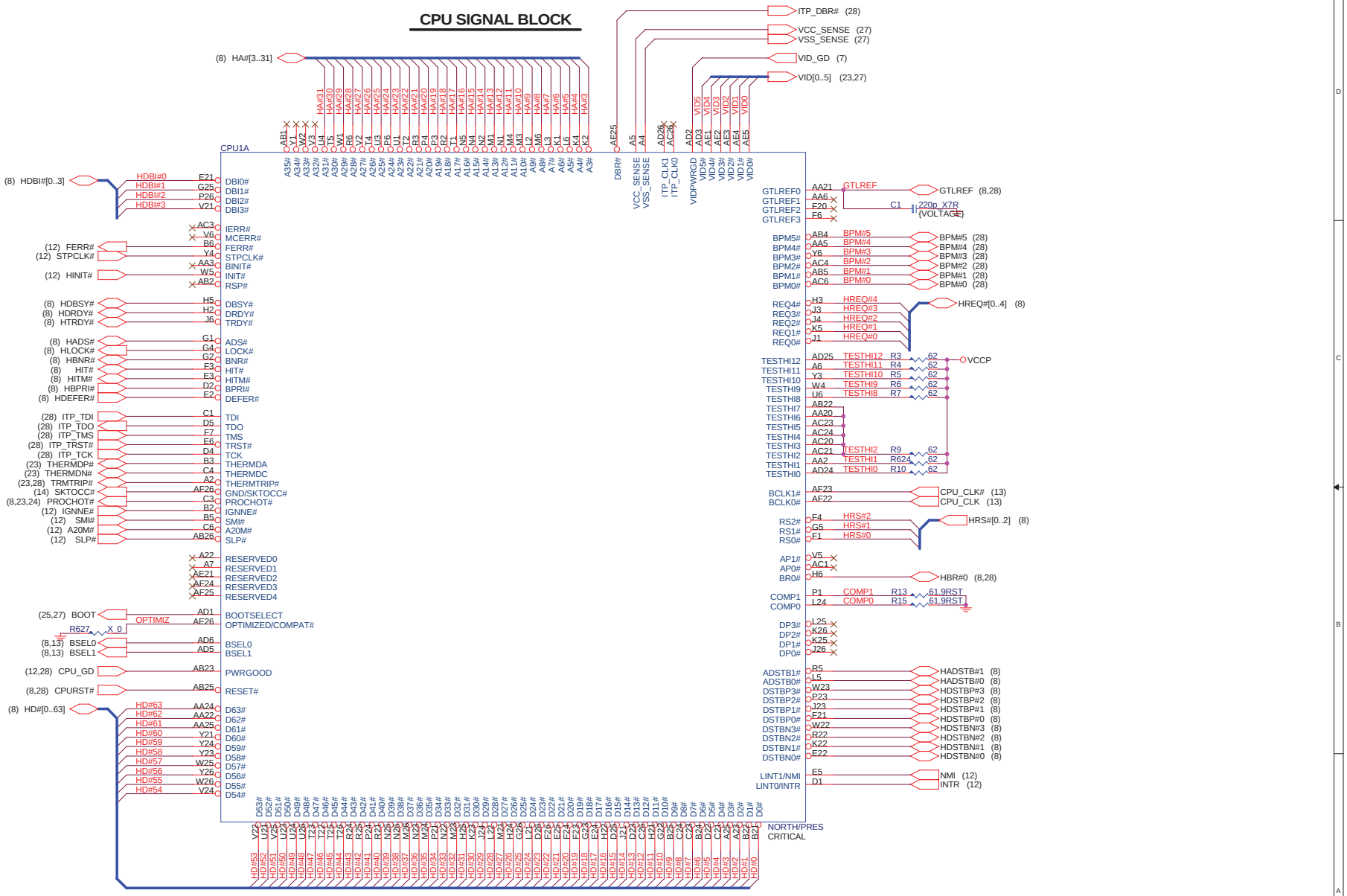
Revision change list from ver: 0BE0 to ver: 0BE1 on 10/18/2002

Sheet 13: Change pull high strapping to pull down.

Sheet 15: Change some component to fix audio solution.

Sheet 27: Change some components to fix VRM solution.

Sheet 30: Add two mini jumpers to support front panel.


CPU SIGNAL BLOCK
CPU1A
(8) HA#[3..31]
ITP_DBR# (28)
VCC_SENSE (27)
VSS_SENSE (27)
VID_GD (7)
VID[0..5] (23,27)
(8) HDBI#[0..3]
HDBI#0
HDBI#1
HDBI#2
HDBI#3
DBI0#
DBI1#
DBI2#
DBI3#
(12) FERR#
(12) STPCLK#
(12) HINIT#
IERR#
MCERR#
FERR#
STPCLK#
BINIT#
INIT#
RSP#
(8) HDBSY#
(8) HDRDY#
(8) HTRDY#
DBSY#
DRDY#
TRDY#
(8) HADS#
(8) HLOCK#
(8) HBNR#
(8) HIT#
(8) HITM#
(8) HBPRI#
(8) HDEFER#
ADS#
LOCK#
BNR#
HIT#
HITM#
BPRI#
DEFER#
(28) ITP_TDI
(28) ITP_TDO
(28) ITP_TMS
(28) ITP_TRST#
(28) ITP_TCK
(23) THERMDP#
(23) THERMDN#
(23,28) TRMTRIP#
(14) SKTOCC#
(8,23,24) PROCHOT#
(12) IGNNE#
(12) SMI#
(12) A20M#
(12) SLP#
TDI
TDO
TMS
TRST#
TCK
THERMDA
THERMDC
THERMTRIP#
GND/SKTOCC#
PROCHOT#
IGNNE#
SMI#
A20M#
SLP#
RESERVED0
RESERVED1
RESERVED2
RESERVED3
RESERVED4
(25,27) BOOT
OPTIMIZ
R627
X_0
BOOTSELECT
OPTIMIZED/COMPAT#
(8,13) BSEL0
(8,13) BSEL1
BSEL0
BSEL1
(12,28) CPU_GD
PWRGOOD
(8,28) CPURST#
RESET#
(8) HD#[0..63]
D63#
D62#
D61#
D60#
D59#
D58#
D57#
D56#
D55#
D54#
NORTH/PRES
CRITICAL
GTLREF0
GTLREF1
GTLREF2
GTLREF3
GTLREF
GTLREF (8,28)
C1
220p_X7R
{VOLTAGE}
BPM5#
BPM4#
BPM3#
BPM2#
BPM1#
BPM0#
BPM#5 (28)
BPM#4 (28)
BPM#3 (28)
BPM#2 (28)
BPM#1 (28)
BPM#0 (28)
REQ4#
REQ3#
REQ2#
REQ1#
REQ0#
HREQ#[0..4] (8)
TESTHI12
TESTHI11
TESTHI10
TESTHI9
TESTHI8
TESTHI7
TESTHI6
TESTHI5
TESTHI4
TESTHI3
TESTHI2
TESTHI1
TESTHI0
VCCP
62
BCLK1#
BCLK0#
CPU_CLK# (13)
CPU_CLK (13)
RS2#
RS1#
RS0#
HRS#[0..2] (8)
AP1#
AP0#
BR0#
HBR#0 (8,28)
COMP1
COMP0
61.9RST
DP3#
DP2#
DP1#
DP0#
ADSTB1#
ADSTB0#
DSTBP3#
DSTBP2#
DSTBP1#
DSTBP0#
DSTBN3#
DSTBN2#
DSTBN1#
DSTBN0#
HADSTB#1 (8)
HADSTB#0 (8)
HDSTBP#3 (8)
HDSTBP#2 (8)
HDSTBP#1 (8)
HDSTBP#0 (8)
HDSTBN#3 (8)
HDSTBN#2 (8)
HDSTBN#1 (8)
HDSTBN#0 (8)
LINT1/NMI
LINT0/INTR
NMI (12)
INTR (12)
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
Title
Intel mPGA478B - Signals
Size
Document Number
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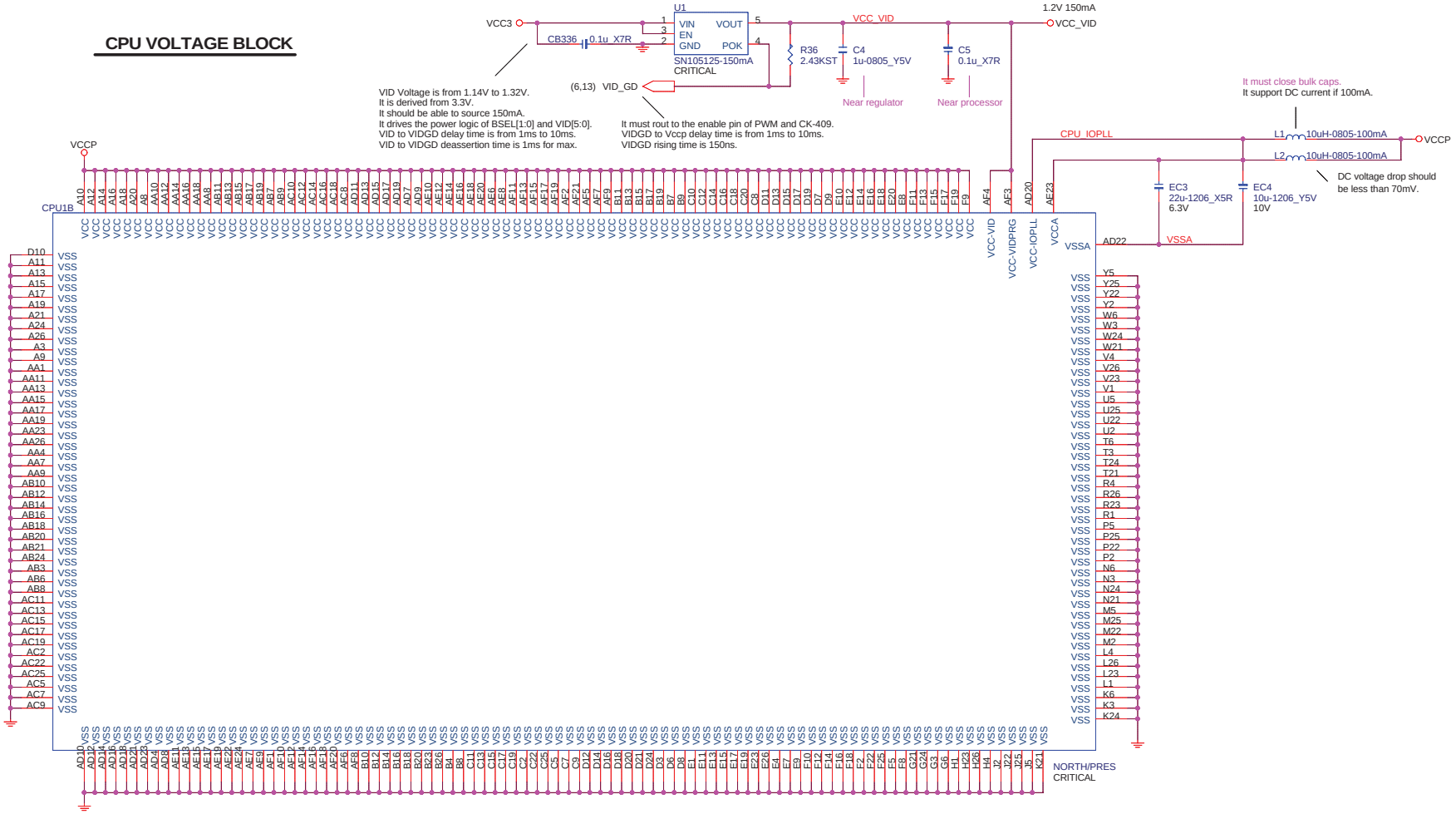
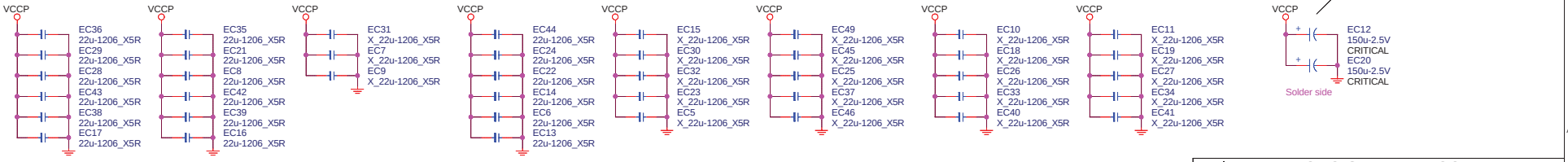
CPU VOLTAGE BLOCK



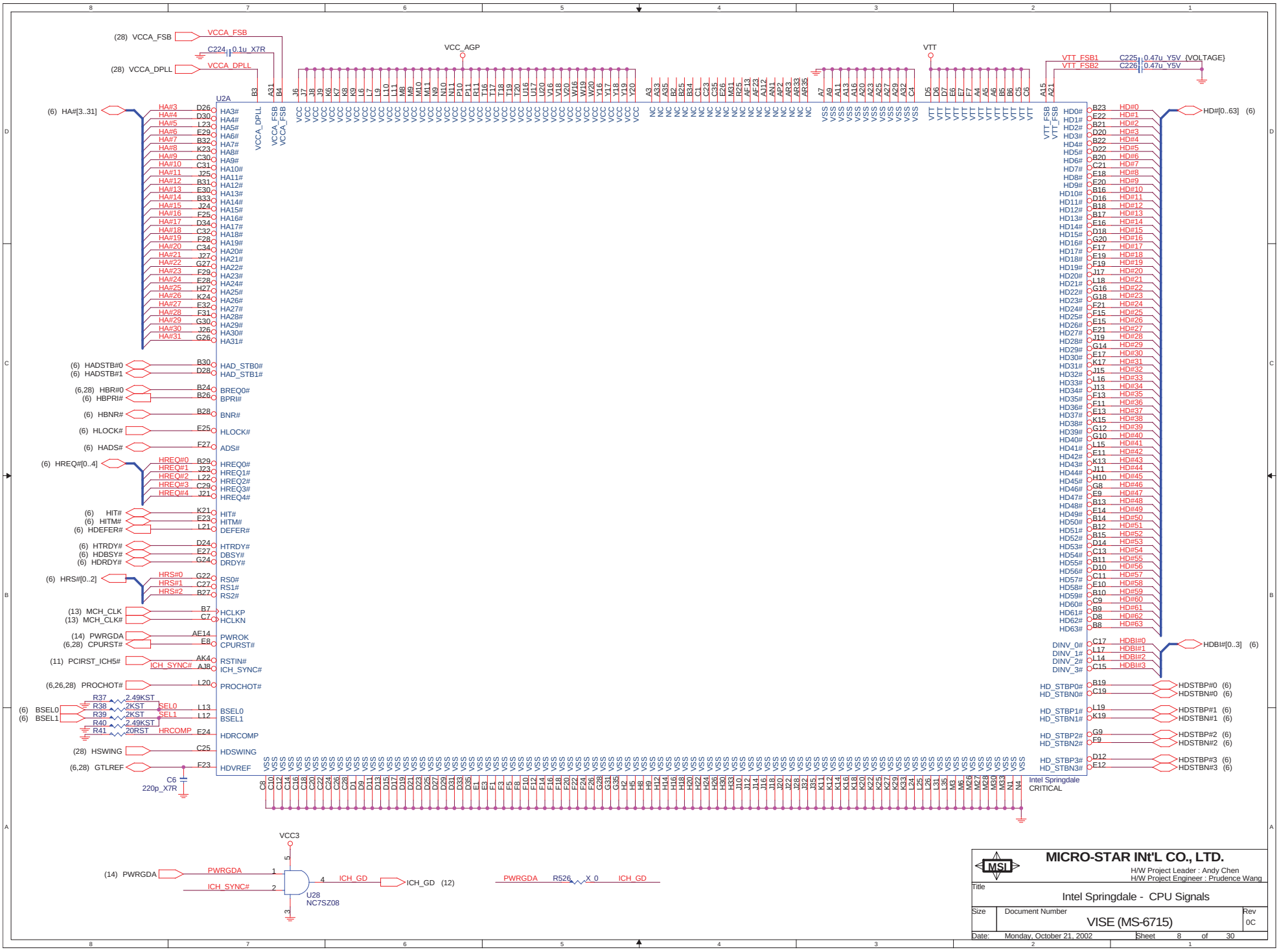
CPU DECOUPLING CAPACITORS



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	Intel mPGA478B - Power	
Size	Document Number: VISE (MS-6715)	Rev: 0C
Date: Monday, October 21, 2002	Sheet 7 of 30	



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: Intel Springdale - CPU Signals

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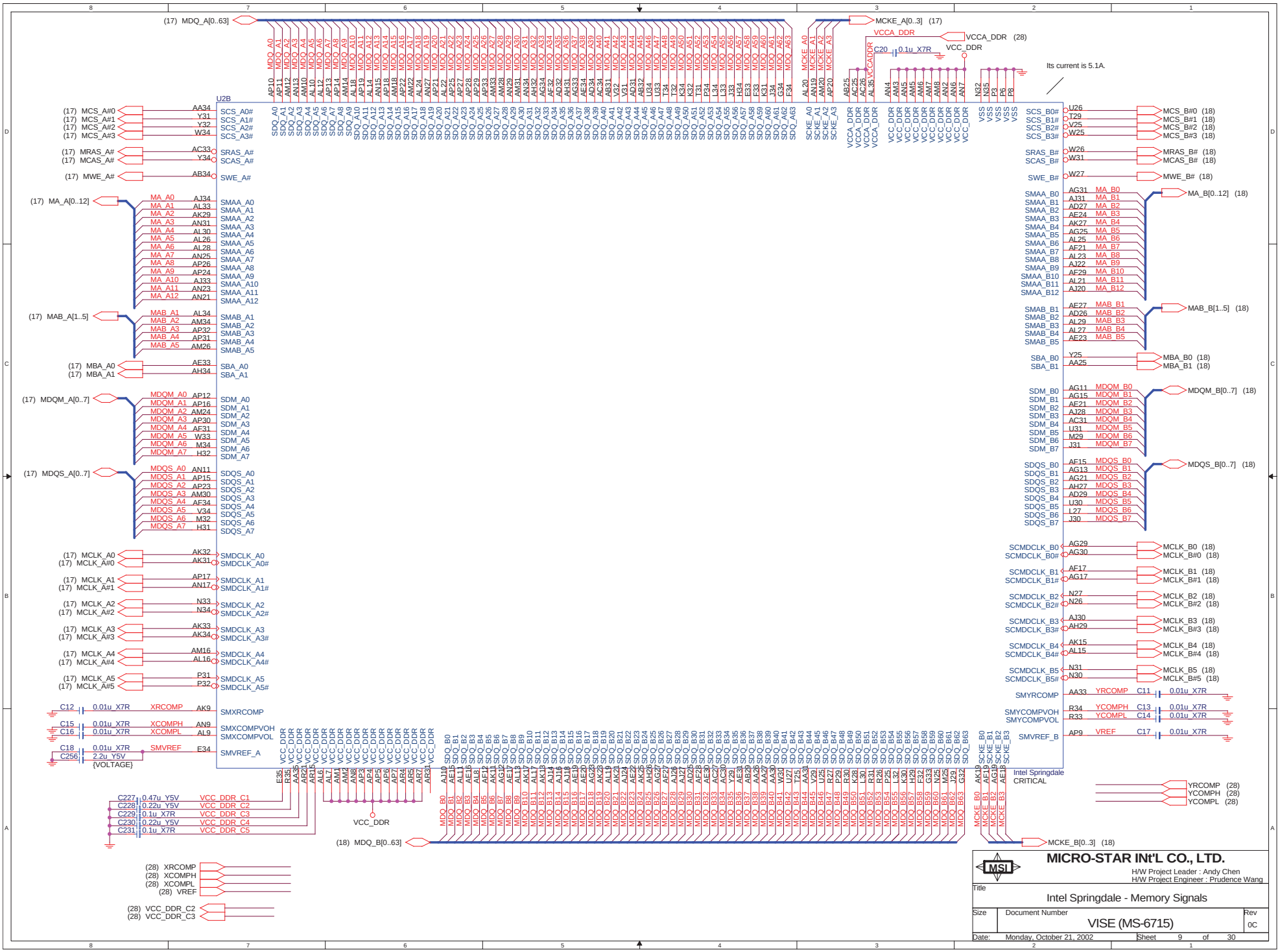

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: Intel Springdale - Memory Signals

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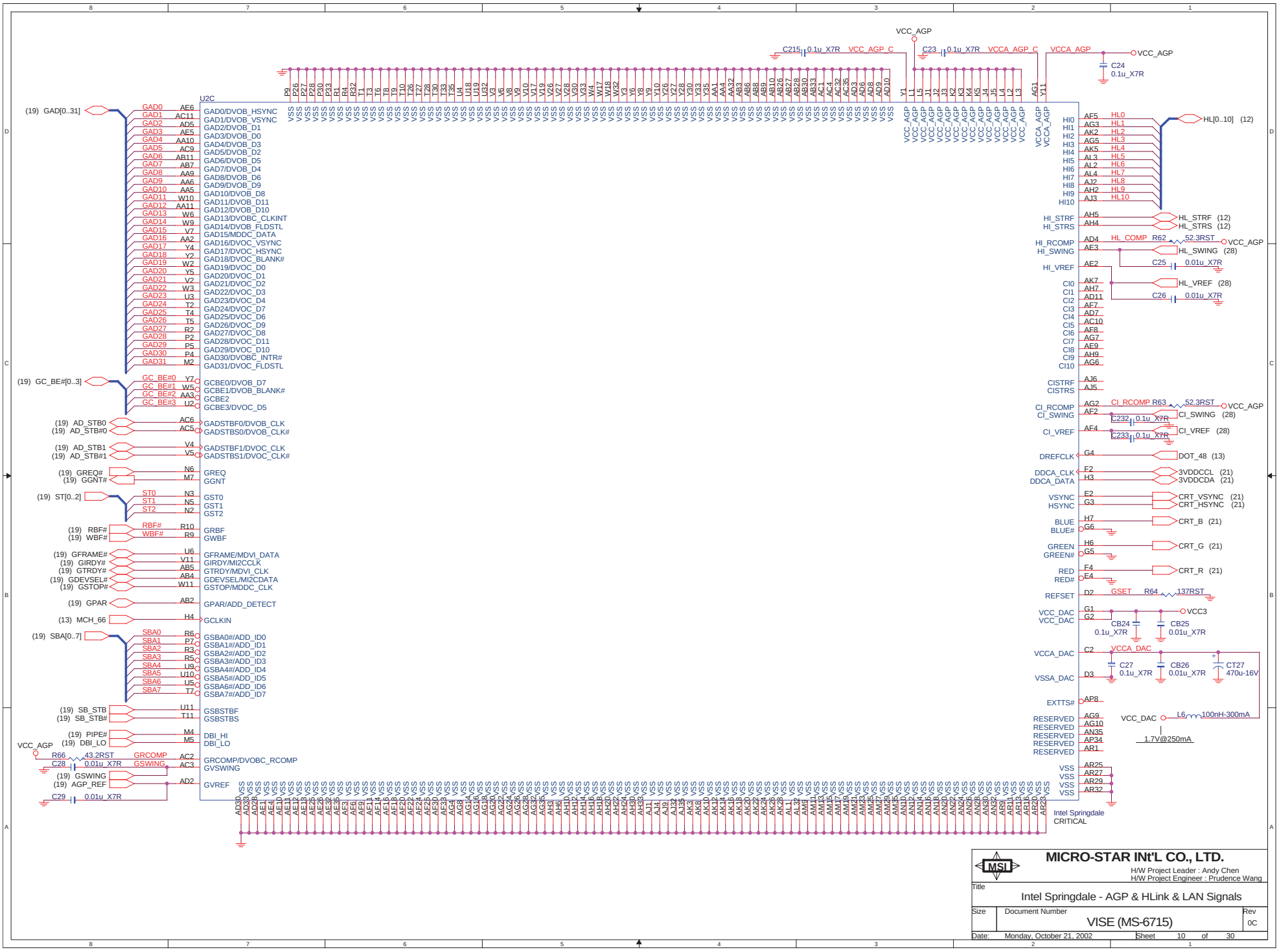
U2C
(19) GAD[0..31]
GAD0 AE6 GAD0/DVOB_HSYNC
GAD1 AC11 GAD1/DVOB_VSYNC
GAD2 AD5 GAD2/DVOB_D1
GAD3 AE5 GAD3/DVOB_D0
GAD4 AA10 GAD4/DVOB_D3
GAD5 AC9 GAD5/DVOB_D2
GAD6 AB11 GAD6/DVOB_D5
GAD7 AB7 GAD7/DVOB_D4
GAD8 AA9 GAD8/DVOB_D6
GAD9 AA6 GAD9/DVOB_D9
GAD10 AA5 GAD10/DVOB_D8
GAD11 W10 GAD11/DVOB_D11
GAD12 AA11 GAD12/DVOB_D10
GAD13 W6 GAD13/DVOBC_CLKINT
GAD14 W9 GAD14/DVOB_FLDSTL
GAD15 V7 GAD15/MDDC_DATA
GAD16 AA2 GAD16/DVOC_VSYNC
GAD17 Y4 GAD17/DVOC_HSYNC
GAD18 Y2 GAD18/DVOC_BLANK#
GAD19 W2 GAD19/DVOC_D0
GAD20 Y5 GAD20/DVOC_D1
GAD21 V2 GAD21/DVOC_D2
GAD22 W3 GAD22/DVOC_D3
GAD23 U3 GAD23/DVOC_D4
GAD24 T2 GAD24/DVOC_D7
GAD25 T4 GAD25/DVOC_D6
GAD26 T5 GAD26/DVOC_D9
GAD27 R2 GAD27/DVOC_D8
GAD28 P2 GAD28/DVOC_D11
GAD29 P5 GAD29/DVOC_D10
GAD30 P4 GAD30/DVOBC_INTR#
GAD31 M2 GAD31/DVOC_FLDSTL
(19) GC_BE#[0..3]
GC_BE#0 Y7 GCBE0/DVOB_D7
GC_BE#1 W5 GCBE1/DVOB_BLANK#
GC_BE#2 AA3 GCBE2
GC_BE#3 U2 GCBE3/DVOC_D5
(19) AD_STB0 AC6 GADSTBF0/DVOB_CLK
(19) AD_STB#0 AC5 GADSTBS0/DVOB_CLK#
(19) AD_STB1 V4 GADSTBF1/DVOC_CLK
(19) AD_STB#1 V5 GADSTBS1/DVOC_CLK#
(19) GREQ# N6 GREQ
(19) GGNT# M7 GGNT
(19) ST[0..2]
ST0 N3 GST0
ST1 N5 GST1
ST2 N2 GST2
(19) RBF# RBF# R10 GRBF
(19) WBF# WBF# R9 GWBF
(19) GFRAME# U6 GFRAME/MDVI_DATA
(19) GIRDY# V11 GIRDY/MI2CCLK
(19) GTRDY# AB5 GTRDY/MDVI_CLK
(19) GDEVSEL# AB4 GDEVSEL/MI2CDATA
(19) GSTOP# W11 GSTOP/MDDC_CLK
(19) GPAR AB2 GPAR/ADD_DETECT
(13) MCH_66 H4 GCLKIN
(19) SBA[0..7]
SBA0 R6 GSBA0#/ADD_ID0
SBA1 P7 GSBA1#/ADD_ID1
SBA2 R3 GSBA2#/ADD_ID2
SBA3 R5 GSBA3#/ADD_ID3
SBA4 U9 GSBA4#/ADD_ID4
SBA5 U10 GSBA5#/ADD_ID5
SBA6 U5 GSBA6#/ADD_ID6
SBA7 T7 GSBA7#/ADD_ID7
(19) SB_STB U11 GSBSTBF
(19) SB_STB# T11 GSBSTBS
(19) PIPE# M4 DBI_HI
(19) DBI_LO M5 DBI_LO
VCC_AGP
R66 43.2RST GRCOMP AC2 GRCOMP/DVOBC_RCOMP
C28 0.01u_X7R GSWING AC3 GVSWING
(19) GSWING
(19) AGP_REF AD2 GVREF
C29 0.01u_X7R
VCC_AGP
C215 0.1u_X7R VCC_AGP_C
C23 0.1u_X7R VCCA_AGP_C
VCCA_AGP
VCC_AGP
C24 0.1u_X7R
HI0 AF5 HL0
HI1 AG3 HL1
HI2 AK2 HL2
HI3 AG5 HL3
HI4 AK5 HL4
HI5 AL3 HL5
HI6 AL2 HL6
HI7 AL4 HL7
HI8 AJ2 HL8
HI9 AH2 HL9
HI10 AJ3 HL10
HL[0..10] (12)
HI_STRF AH5 HL_STRF (12)
HI_STRS AH4 HL_STRS (12)
HI_RCOMP AD4 HL_COMP R62 52.3RST VCC_AGP
HI_SWING AF3 HL_SWING (28)
HI_VREF AE2 C25 0.01u_X7R
AK7 HL_VREF (28)
AH7
AD11 C26 0.01u_X7R
CI0 AF7
CI1 AD7
CI2 AC10
CI3 AF8
CI4 AG7
CI5 AE9
CI6 AH9
CI7 AG6
CI8
CI9
CI10
CISTRF AJ6
CISTRS AJ5
CI_RCOMP AG2 CI_RCOMP R63 52.3RST VCC_AGP
CI_SWING AF2 C232 0.1u_X7R CI_SWING (28)
CI_VREF AF4 C233 0.1u_X7R CI_VREF (28)
DREFCLK G4 DOT_48 (13)
DDCA_CLK F2 3VDDCCL (21)
DDCA_DATA H3 3VDDCDA (21)
VSYNC E2 CRT_VSYNC (21)
HSYNC G3 CRT_HSYNC (21)
BLUE H7 CRT_B (21)
BLUE# G6
GREEN H6 CRT_G (21)
GREEN# G5
RED F4 CRT_R (21)
RED# E4
REFSET D2 GSET R64 137RST
VCC_DAC G1 VCC3
VCC_DAC G2 CB24 0.1u_X7R CB25 0.01u_X7R
VCCA_DAC C2 VCCA_DAC C27 0.1u_X7R CB26 0.01u_X7R CT27 470u-16V
VSSA_DAC D3
EXTTS# AP8
RESERVED AG9
RESERVED AG10
RESERVED AN35
RESERVED AP34
RESERVED AR1
VCC_DAC L6 100nH-300mA
1.7V@250mA
VSS AR25
VSS AR27
VSS AR29
VSS AR32
Intel Springdale
CRITICAL
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
Title
Intel Springdale - AGP & HLink & LAN Signals
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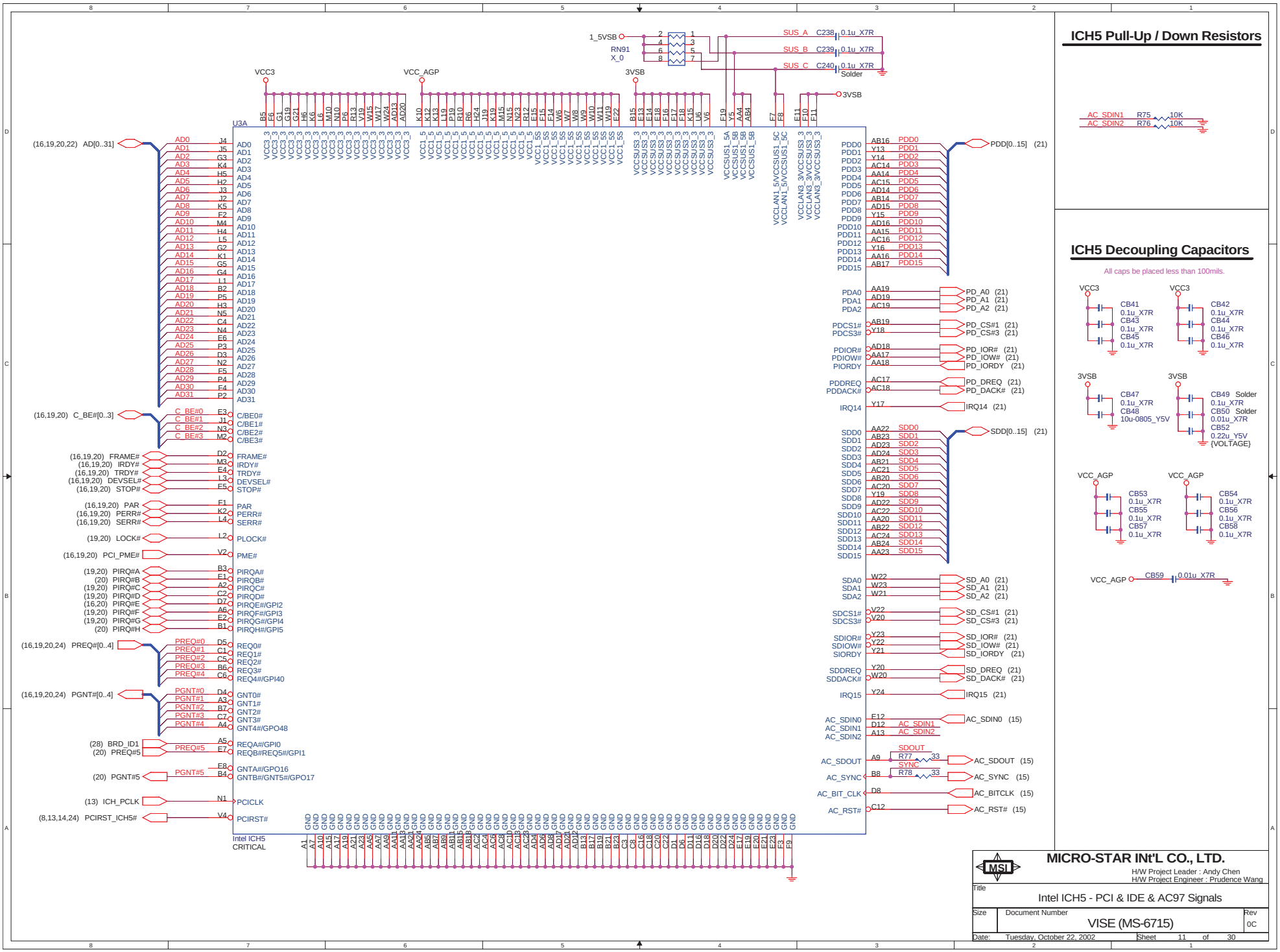

ICH5 Pull-Up / Down Resistors

AC_SDIN1 R75 10K
AC_SDIN2 R76 10K

ICH5 Decoupling Capacitors

All caps be placed less than 100mils.

VCC3: CB41 0.1u_X7R, CB43 0.1u_X7R, CB45 0.1u_X7R
VCC3: CB42 0.1u_X7R, CB44 0.1u_X7R, CB46 0.1u_X7R
3VSB: CB47 0.1u_X7R, CB48 10u-0805_Y5V
3VSB: CB49 Solder 0.1u_X7R, CB50 Solder 0.01u_X7R, CB52 0.22u_Y5V {VOLTAGE}
VCC_AGP: CB53 0.1u_X7R, CB55 0.1u_X7R, CB57 0.1u_X7R
VCC_AGP: CB54 0.1u_X7R, CB56 0.1u_X7R, CB58 0.1u_X7R
VCC_AGP CB59 0.01u_X7R

MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: Intel ICH5 - PCI & IDE & AC97 Signals
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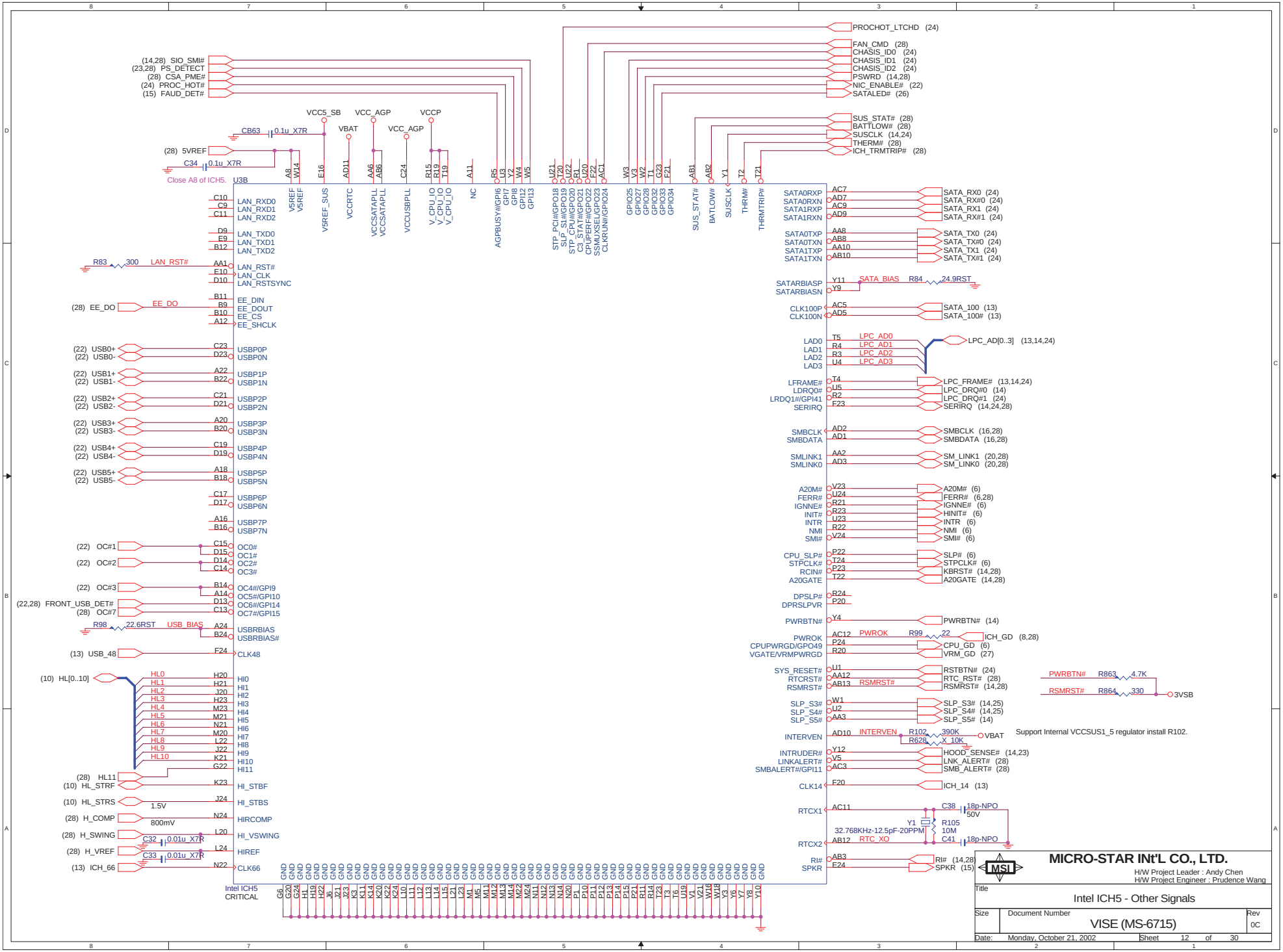
PROCHOT_LTCHD (24)
FAN_CMD (28)
CHASIS_ID0 (24)
CHASIS_ID1 (24)
CHASIS_ID2 (24)
PSWRD (14,28)
NIC_ENABLE# (22)
SATALED# (26)
(14,28) SIO_SMI#
(23,28) PS_DETECT
(28) CSA_PME#
(24) PROC_HOT#
(15) FAUD_DET#
SUS_STAT# (28)
BATTLOW# (28)
SUSCLK (14,24)
THERM# (28)
ICH_TRMTRIP# (28)
VCC5_SB
VCC_AGP
VCCP
VBAT
CB63 0.1u_X7R
(28) 5VREF
C34 0.1u_X7R
Close A8 of ICH5.
U3B
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
R83 300 LAN_RST#
LAN_RST#
LAN_CLK
LAN_RSTSYNC
EE_DIN
EE_DOUT
EE_CS
EE_SHCLK
(28) EE_DO
EE_DO
(22) USB0+
(22) USB0-
USBP0P
USBP0N
(22) USB1+
(22) USB1-
USBP1P
USBP1N
(22) USB2+
(22) USB2-
USBP2P
USBP2N
(22) USB3+
(22) USB3-
USBP3P
USBP3N
(22) USB4+
(22) USB4-
USBP4P
USBP4N
(22) USB5+
(22) USB5-
USBP5P
USBP5N
USBP6P
USBP6N
USBP7P
USBP7N
(22) OC#1
(22) OC#2
(22) OC#3
(22,28) FRONT_USB_DET#
(28) OC#7
OC0#
OC1#
OC2#
OC3#
OC4#/GPI9
OC5#/GPI10
OC6#/GPI14
OC7#/GPI15
R98 22.6RST USB_BIAS
USBRBIAS
USBRBIAS#
(13) USB_48
CLK48
(10) HL[0..10]
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
HL8
HL9
HL10
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
HI11
(28) HL11
(10) HL_STRF
HI_STBF
(10) HL_STRS
1.5V
HI_STBS
(28) H_COMP
800mV
HIRCOMP
(28) H_SWING
C32 0.01u_X7R
HI_VSWING
(28) H_VREF
C33 0.01u_X7R
HIREF
(13) ICH_66
CLK66
Intel ICH5
CRITICAL
SATA0RXP
SATA0RXN
SATA1RXP
SATA1RXN
SATA_RX0 (24)
SATA_RX#0 (24)
SATA_RX1 (24)
SATA_RX#1 (24)
SATA0TXP
SATA0TXN
SATA1TXP
SATA1TXN
SATA_TX0 (24)
SATA_TX#0 (24)
SATA_TX1 (24)
SATA_TX#1 (24)
SATARBIASP
SATARBIASN
SATA_BIAS R84 24.9RST
CLK100P
CLK100N
SATA_100 (13)
SATA_100# (13)
LAD0
LAD1
LAD2
LAD3
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_AD[0..3] (13,14,24)
LFRAME#
LDRQ0#
LDRQ1#/GPI41
SERIRQ
LPC_FRAME# (13,14,24)
LPC_DRQ#0 (14)
LPC_DRQ#1 (24)
SERIRQ (14,24,28)
SMBCLK
SMBDATA
SMBCLK (16,28)
SMBDATA (16,28)
SMLINK1
SMLINK0
SM_LINK1 (20,28)
SM_LINK0 (20,28)
A20M# (6)
FERR# (6,28)
IGNNE# (6)
HINIT# (6)
INTR (6)
NMI (6)
SMI# (6)
CPU_SLP#
STPCLK#
RCIN#
A20GATE
SLP# (6)
STPCLK# (6)
KBRST# (14,28)
A20GATE (14,28)
DPSLP#
DPRSLPVR
PWRBTN#
PWRBTN# (14)
PWROK
CPUPWRGD/GPO49
VGATE/VRMPWRGD
R99 22
ICH_GD (8,28)
CPU_GD (6)
VRM_GD (27)
SYS_RESET#
RTCRST#
RSMRST#
RSTBTN# (24)
RTC_RST# (28)
RSMRST# (14,28)
PWRBTN# R863 4.7K
RSMRST# R864 330
3VSB
SLP_S3#
SLP_S4#
SLP_S5#
SLP_S3# (14,25)
SLP_S4# (14,25)
SLP_S5# (14)
INTERVEN
R102 390K
R628 X_10K
VBAT
Support Internal VCCSUS1_5 regulator install R102.
INTRUDER#
LINKALERT#
SMBALERT#/GPI11
HOOD_SENSE# (14,23)
LNK_ALERT# (28)
SMB_ALERT# (28)
CLK14
ICH_14 (13)
RTCX1
RTCX2
C38 18p-NPO 50V
Y1 32.768KHz-12.5pF-20PPM
R105 10M
C41 18p-NPO
RTC_XO
RI#
SPKR
RI# (14,28)
SPKR (15)
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
Title
Intel ICH5 - Other Signals
Size
Document Number
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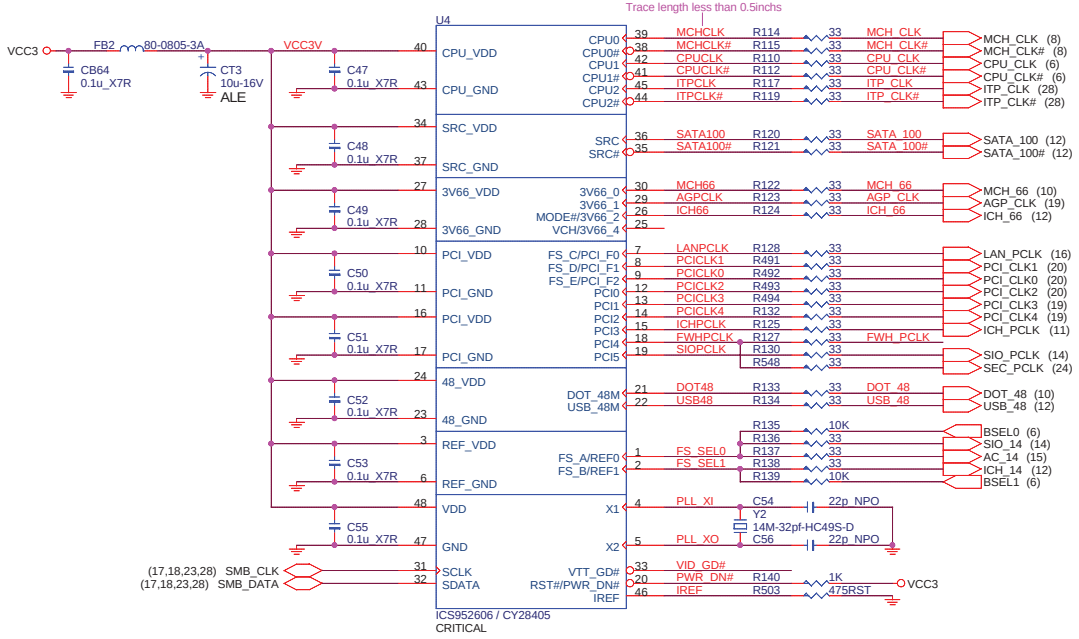
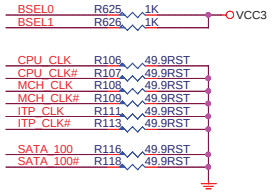
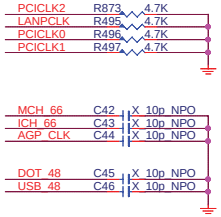
Clock Generator - CY28405

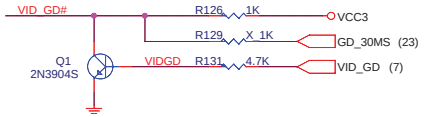




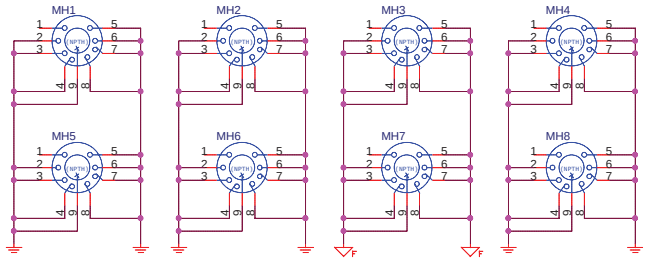


EMC HF filter capacitors, located close to PLL

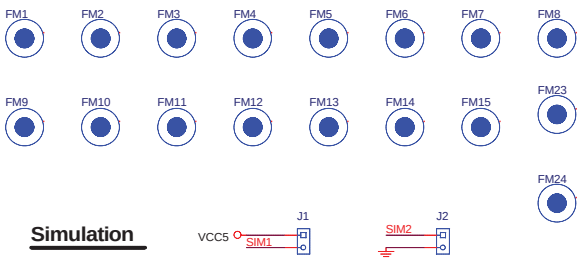
Clock Generator VTT Power Down Block



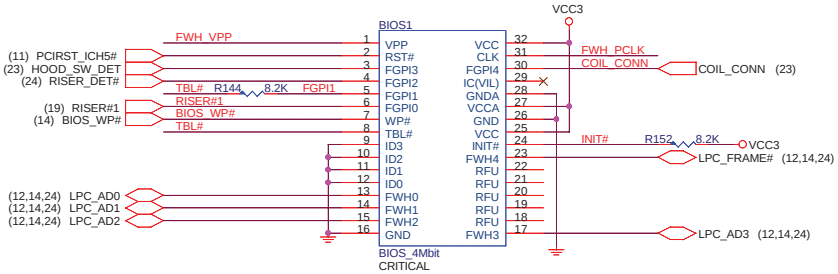
Mounting Holes



Optics Orientation Holes



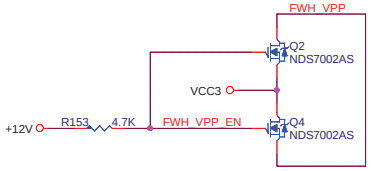
Firware Hub (FWH)



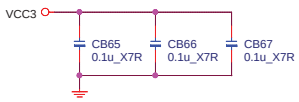
BIOS PROTECT BLOCK

BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default

Simulation

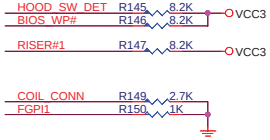


FWH Decoupling Capacitors



Place Cap. as Close to every pin of FWH< 250 mil.

FWH Strapping Resistors

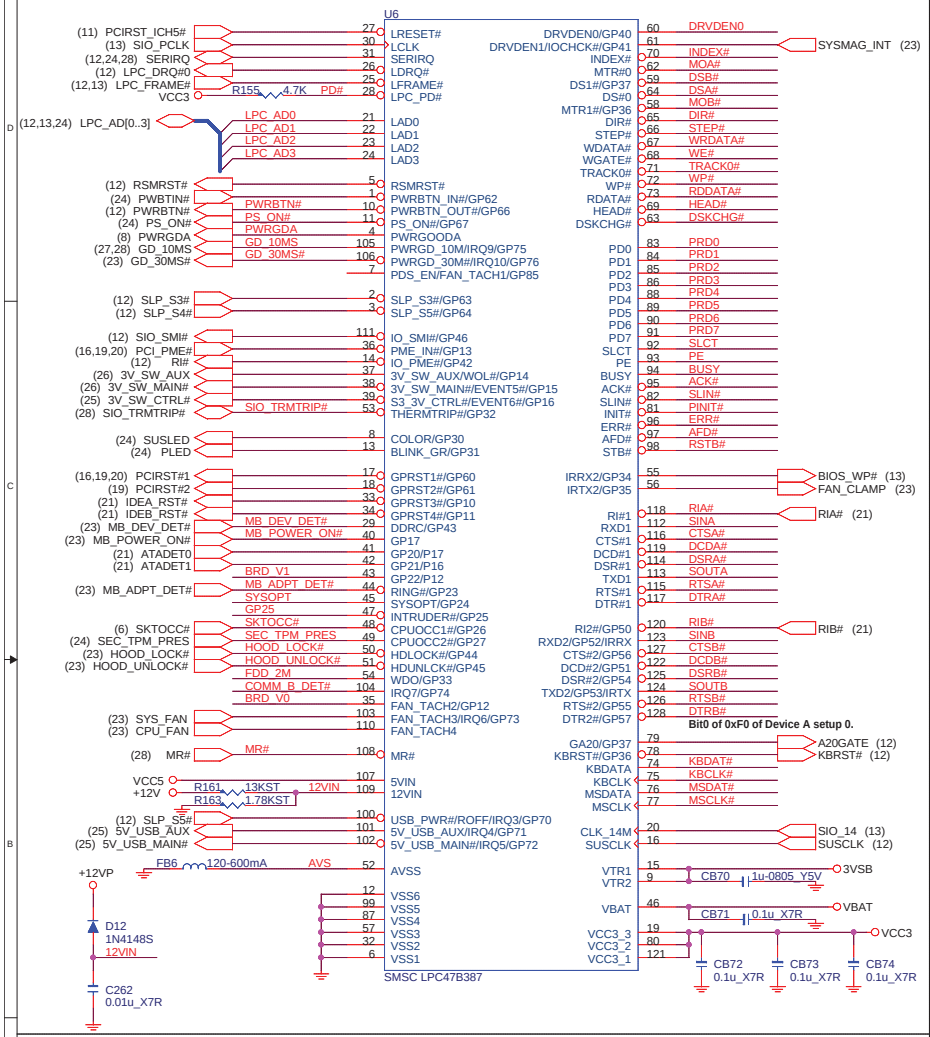


MICRO-STAR INt'L CO., LTD.

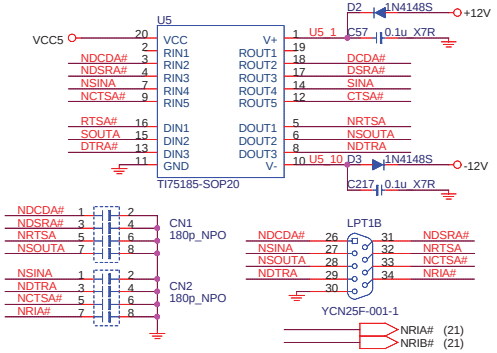
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	CY28405 & FWH	
Size	Document Number: VISE (MS-6715)	Rev: 0C
Date: Monday, October 21, 2002	Sheet 13 of 30	

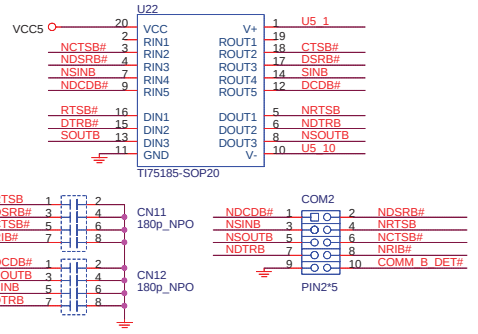
LPC SUPER I/O LPC47B387



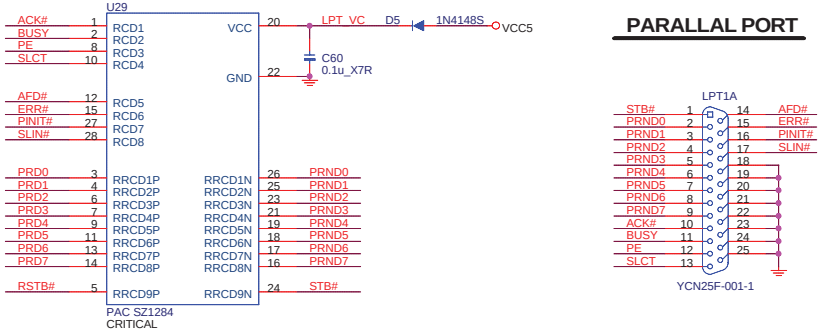
SERIAL PORT 1



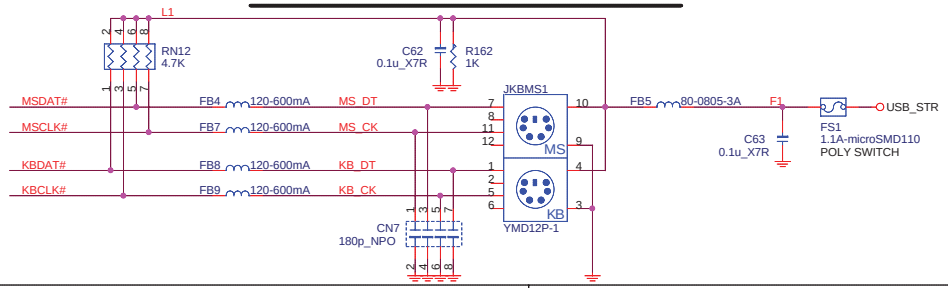
SERIAL PORT 2



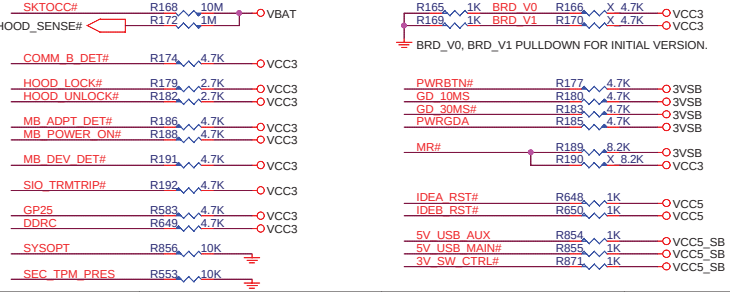
PARALLAL PORT



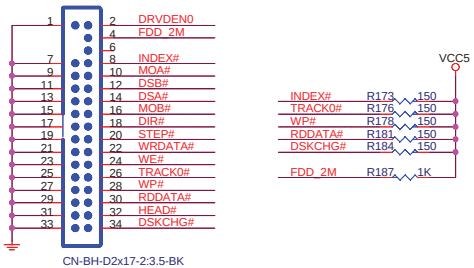
PS2 KEYBOARD & MOUSE CONNECTOR



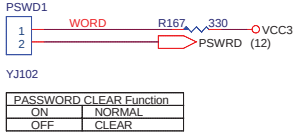
LPC I/O STRAPPING RESISTOR



FLOPPY CONNECTOR



PASSWORD CLEAR



PASSWORD CLEAR Function	
ON	NORMAL
OFF	CLEAR

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: LPC SUPER I/O & CONNECTORS

Size | Document Number: VISE (MS-6715) | Rev: 0C

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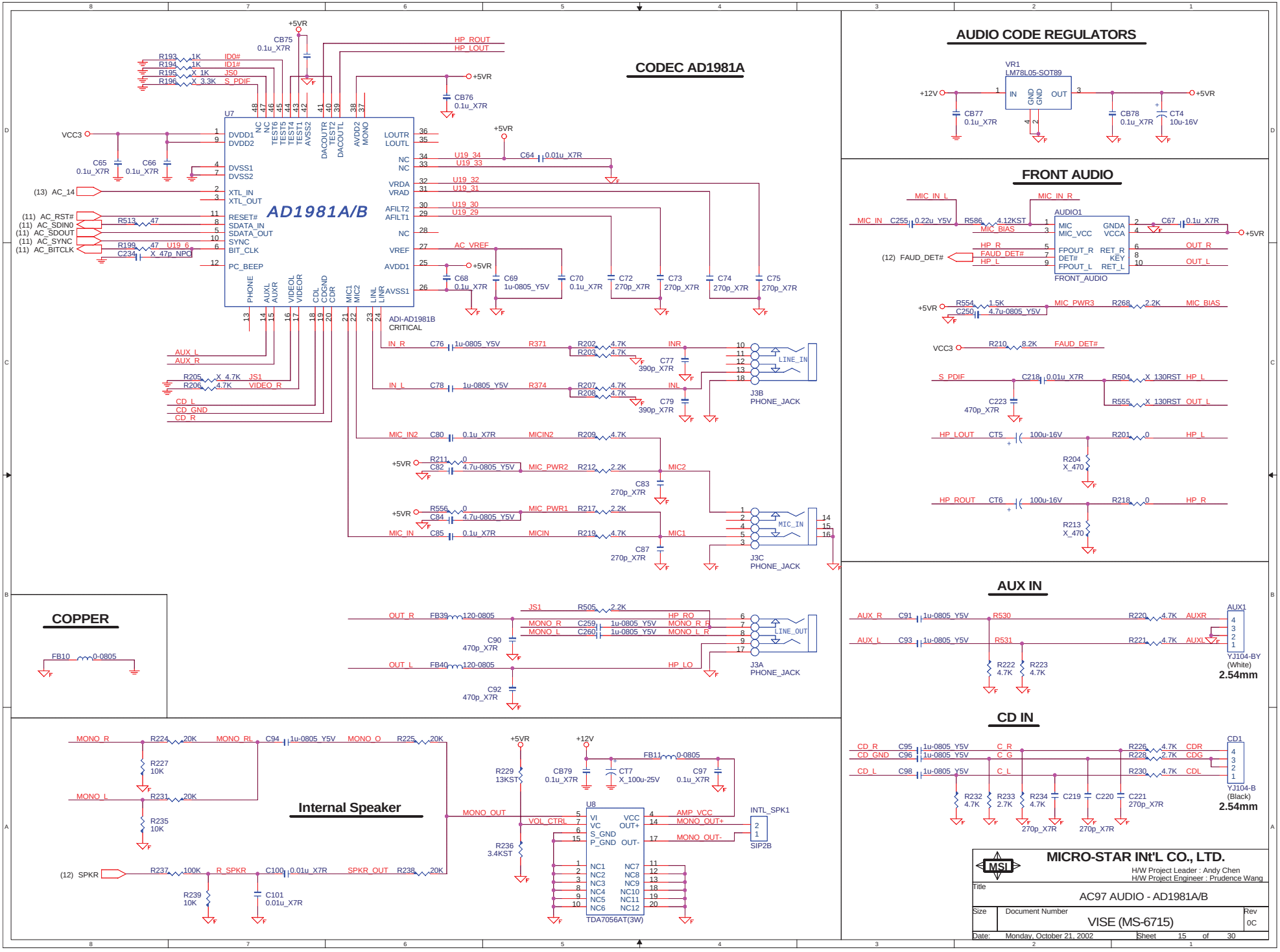
CODEC AD1981A
AD1981A/B
ADI-AD1981B
CRITICAL
AUDIO CODE REGULATORS
VR1
LM78L05-SOT89
FRONT AUDIO
AUDIO1
FRONT_AUDIO
AUX IN
AUX1
YJ104-BY
(White)
2.54mm
CD IN
CD1
YJ104-B
(Black)
2.54mm
COPPER
Internal Speaker
TDA7056AT(3W)
SIP2B
J3B
PHONE_JACK
J3C
PHONE_JACK
J3A
PHONE_JACK
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
AC97 AUDIO - AD1981A/B
VISE (MS-6715)
Monday, October 21, 2002
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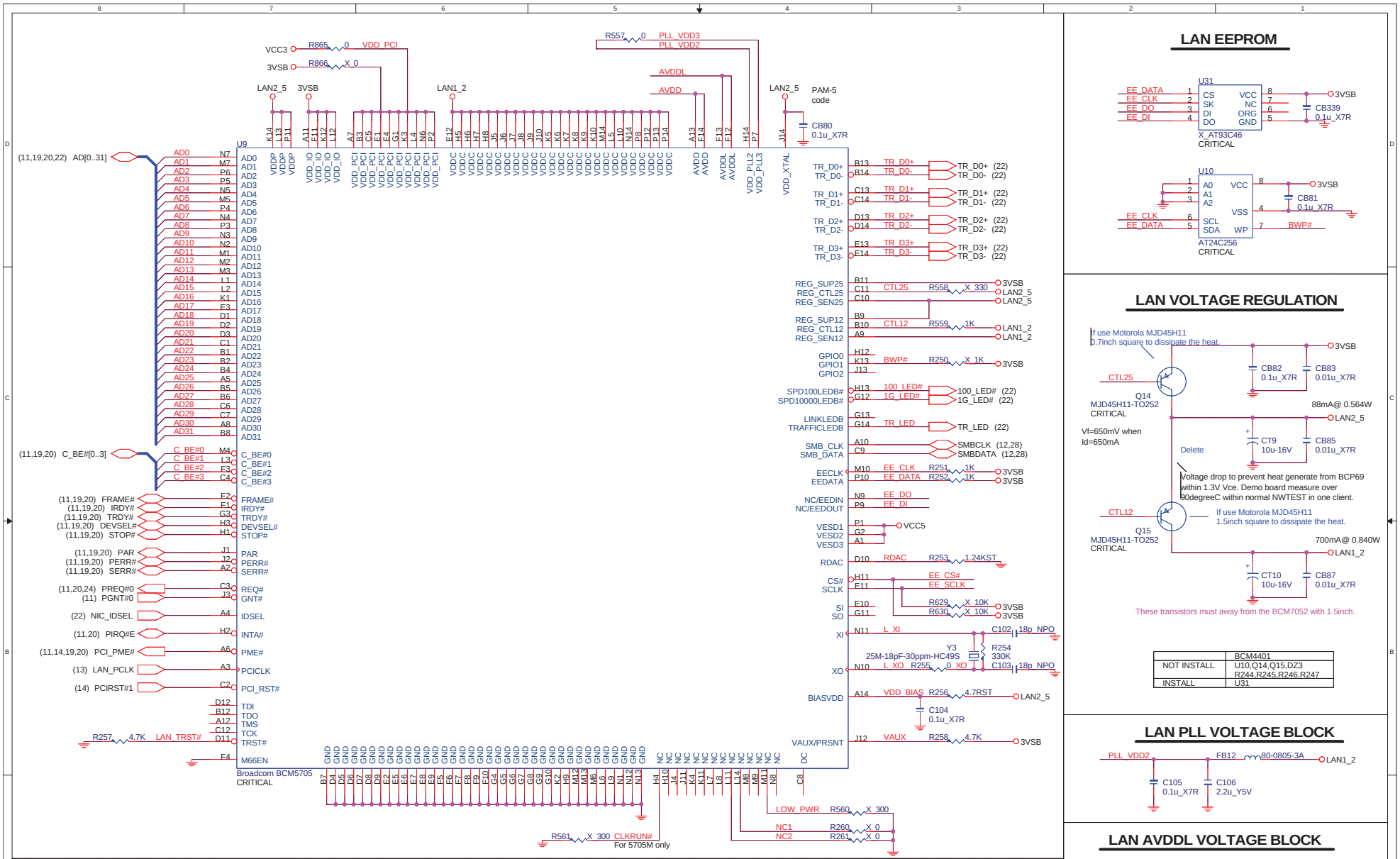


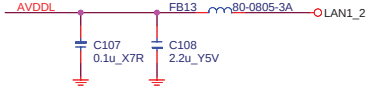
LAN EEPROM

LAN VOLTAGE REGULATION

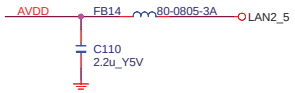
	BCM4401
NOT INSTALL	U10,Q14,Q15,DZ3 R244,R245,R246,R247
INSTALL	U31

LAN PLL VOLTAGE BLOCK

LAN AVDDL VOLTAGE BLOCK

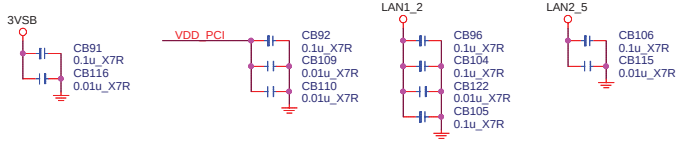


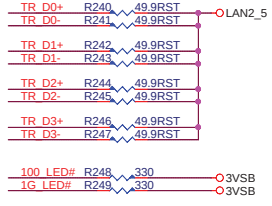
LAN AVDD VOLTAGE BLOCK



LAN Decoupling Capacitors

Close chipset, and trace length is less than 20mils.



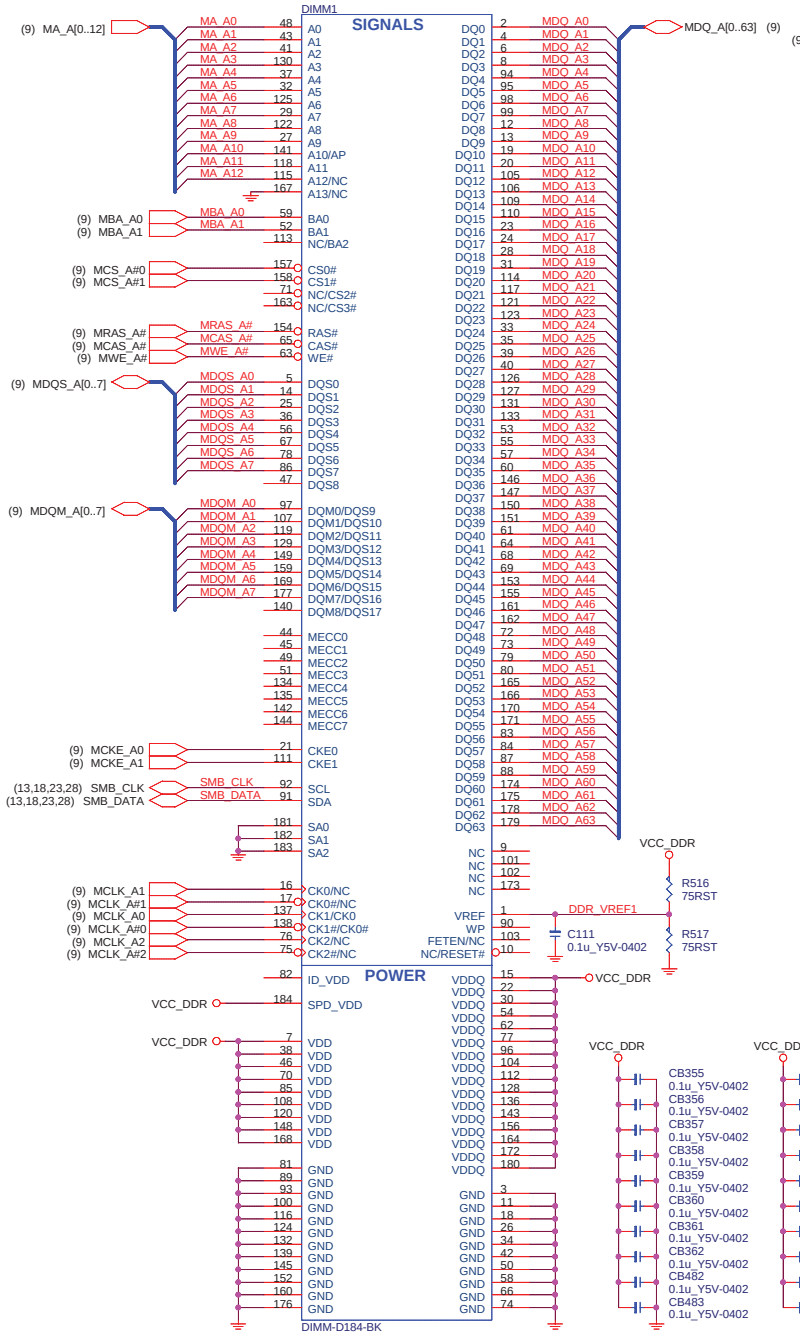


MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

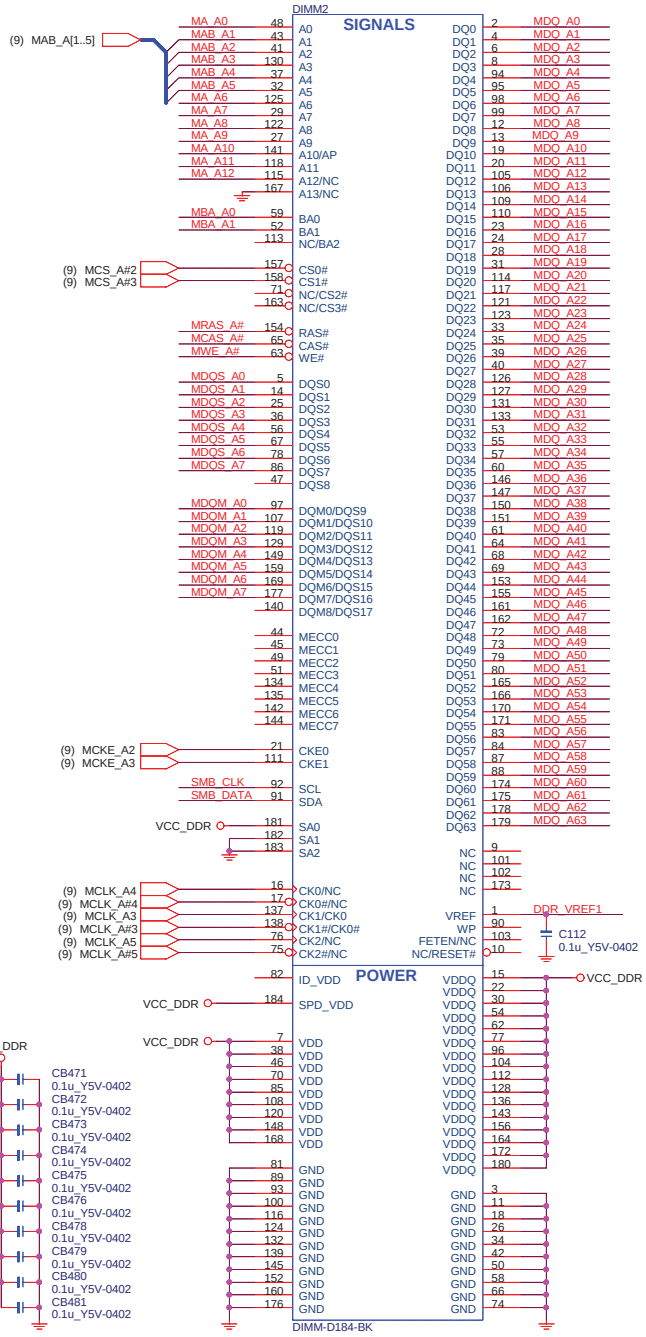
Title	Broadcom BCM5702	
Size	Document Number: VISE (MS-6715)	Rev 0C
Date: Monday, October 21, 2002	Sheet 16 of 30	

DDR DIMM1



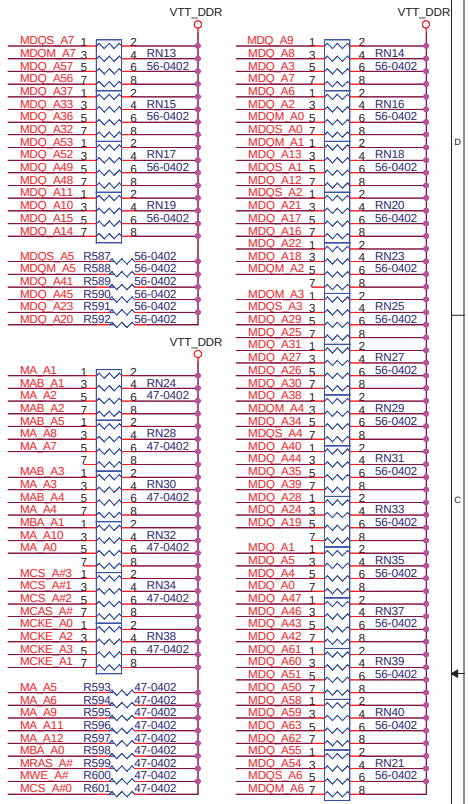
ADDR.=1010000B

DDR DIMM2

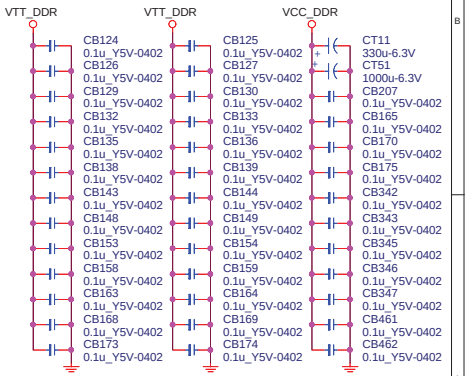


ADDR.=1010001B

DDR Terminational Resisitors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	DDR DIMM 1 & 2	
Size	Document Number: VISE (MS-6715)	Rev: 0C
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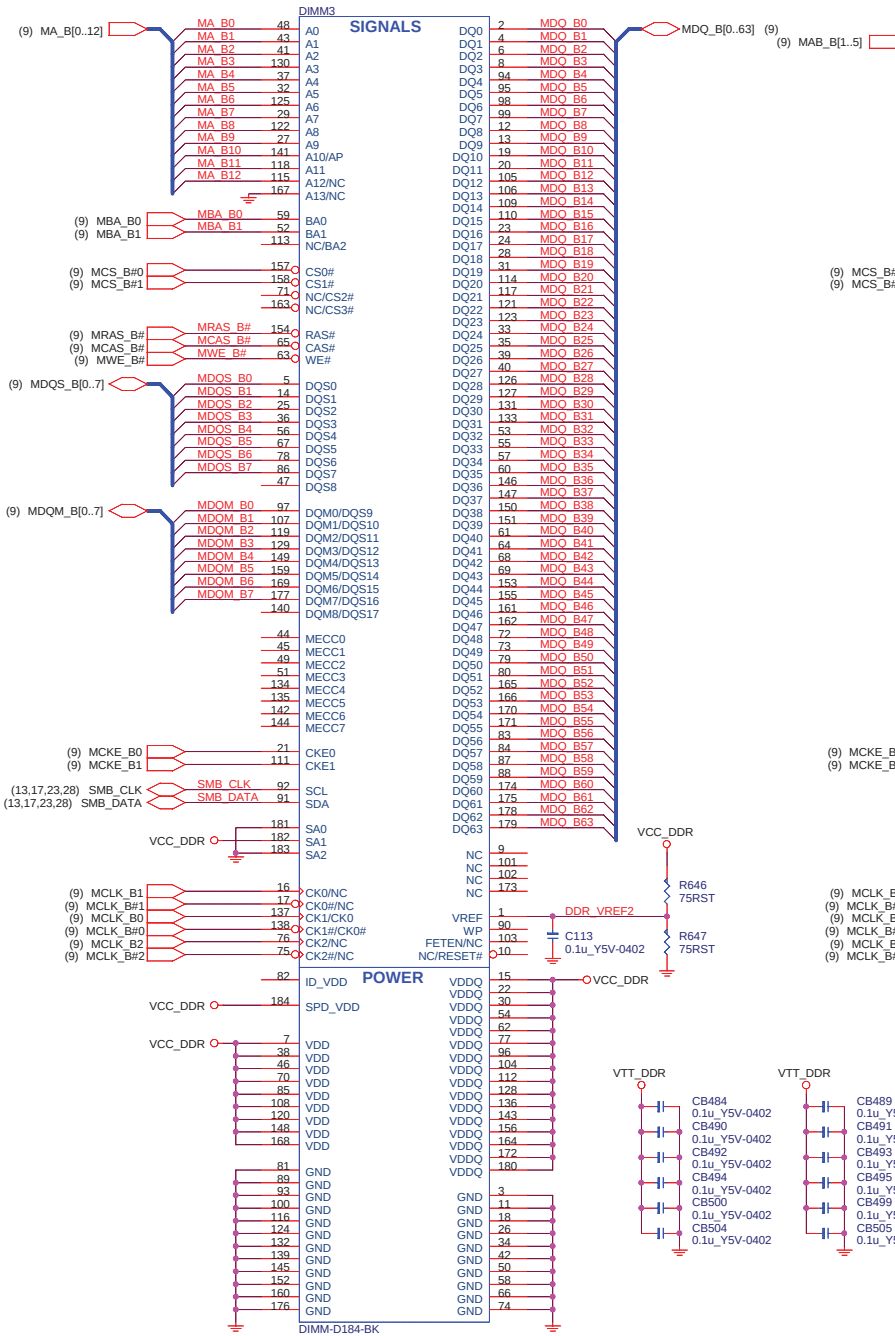
DDR DIMM3



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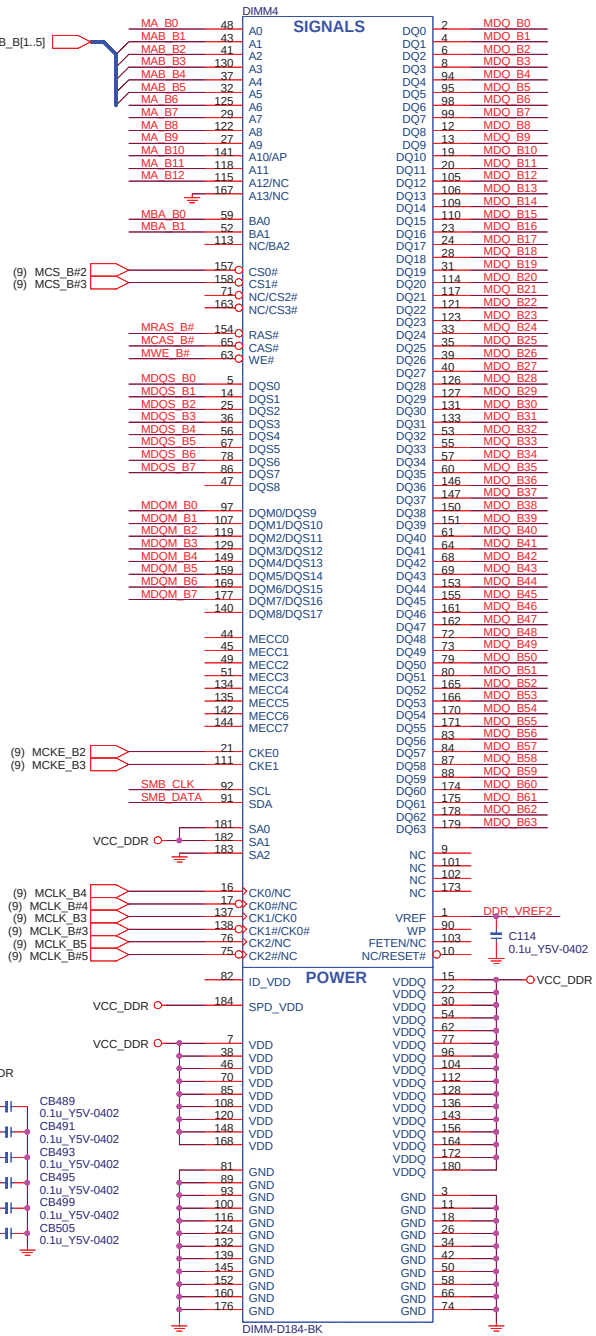
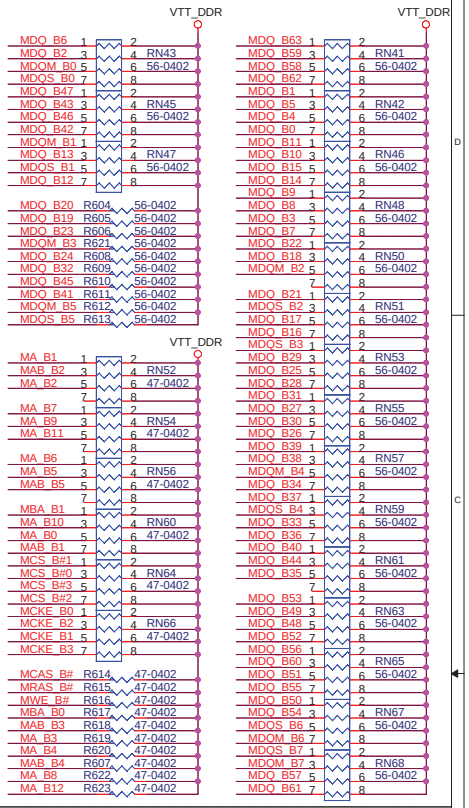
DDR DIMM4

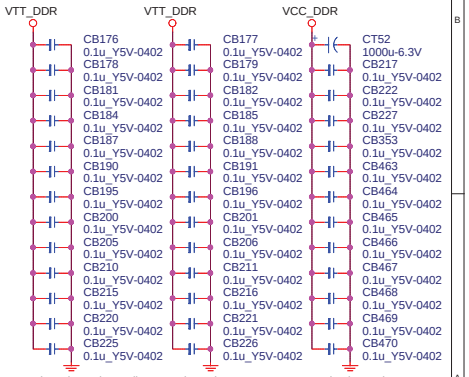


ADDR.=1010011B

DDR Terminational Resisitors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	DDR DIMM 3 & 4	
Size	Document Number: VISE (MS-6715)	Rev: 0C
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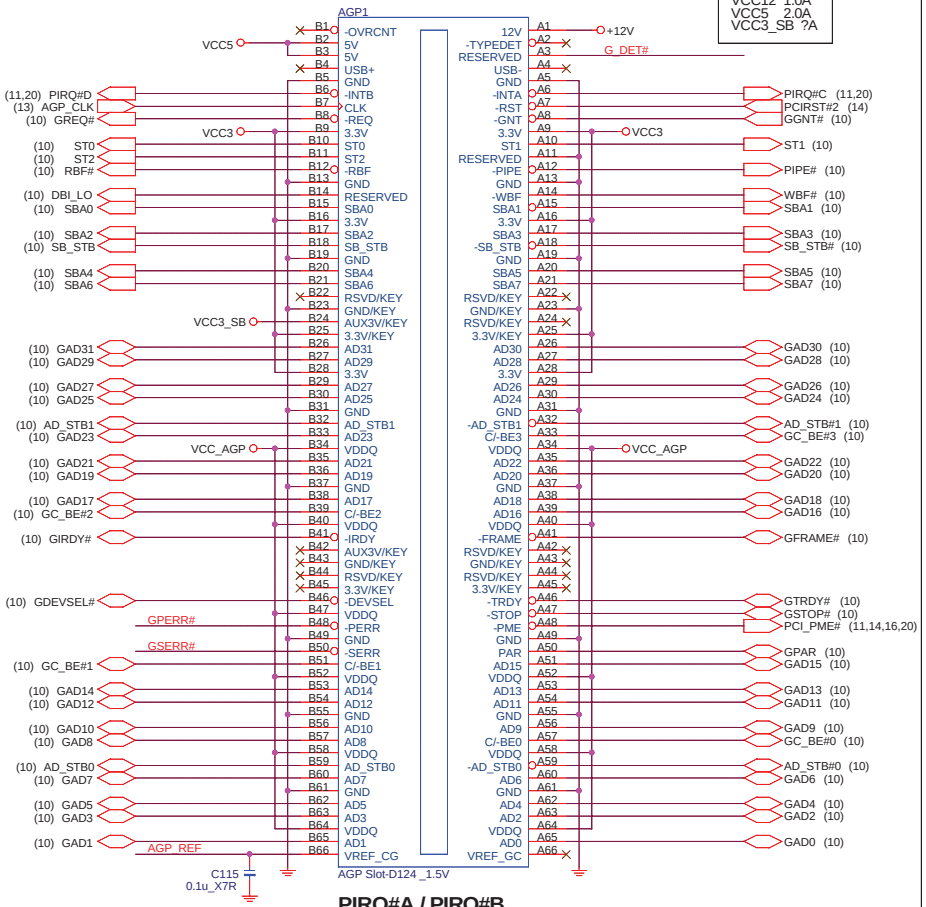
AGP 1.5V 1X/2X/4X/8X SLOT(AGP VER:3.0)

VCC5 = 60mils trace / 15 mils space

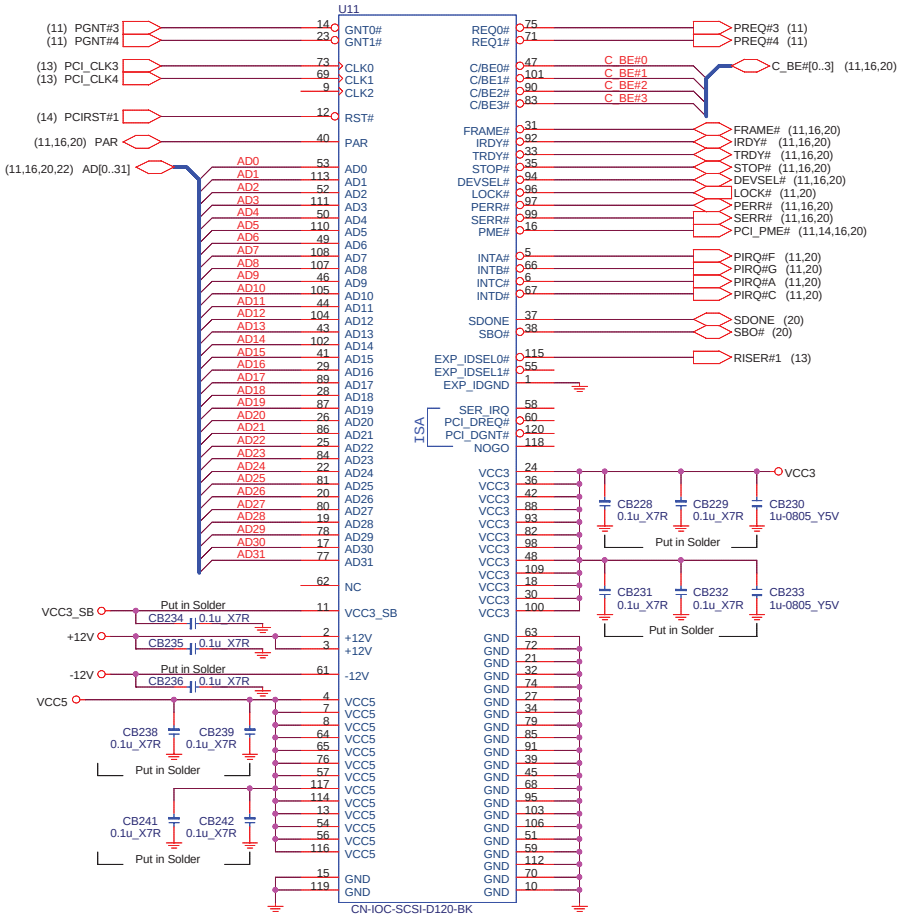
AGP Slot Imax

VCCq	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	?A

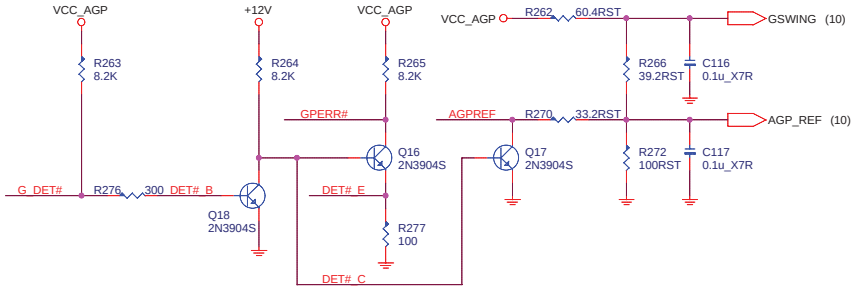


PIRQ#A / PIRQ#B

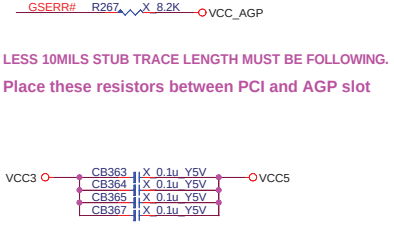
PCI EXPANSION RISER (PCI VER:2.2 COMPLY)



Springdale Reference & Swing Voltage Circuit



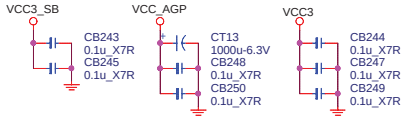
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	AGP 1.5V SLOT & PCI RISER	
Size	Document Number: VISE (MS-6715)	Rev: 0C
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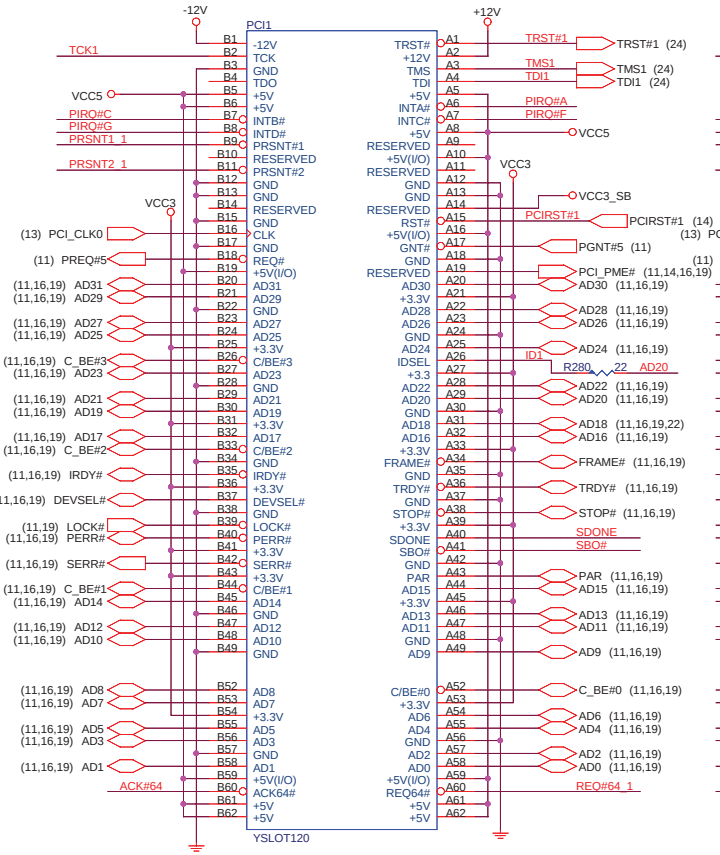
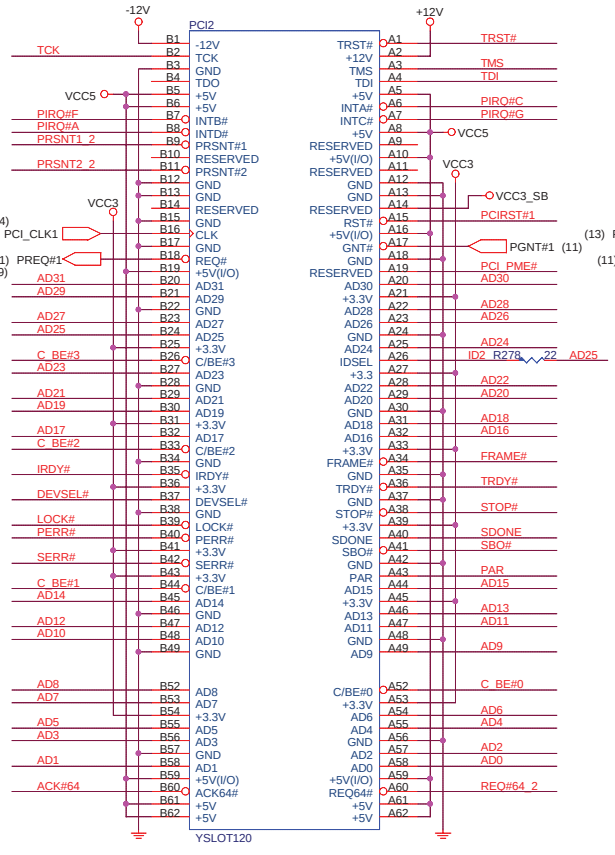
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



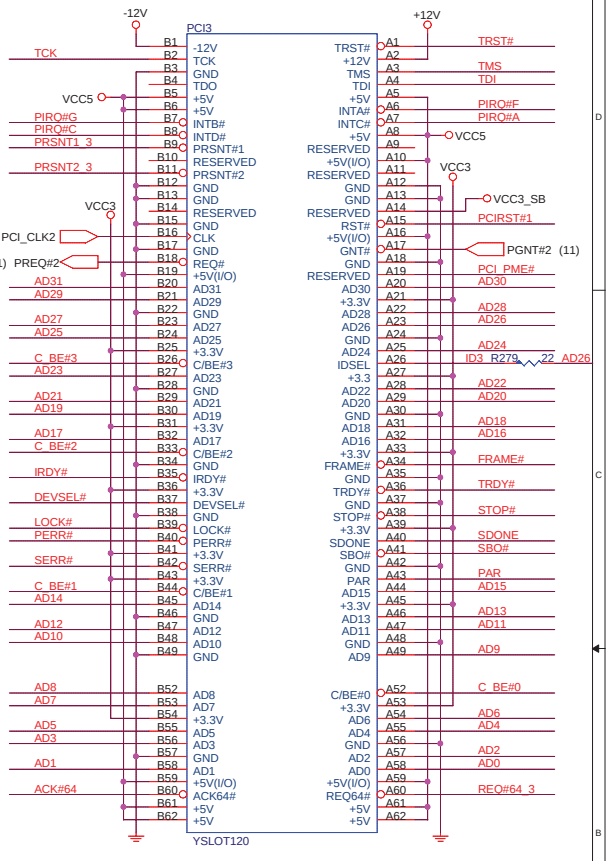
IDSEL = AD20
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



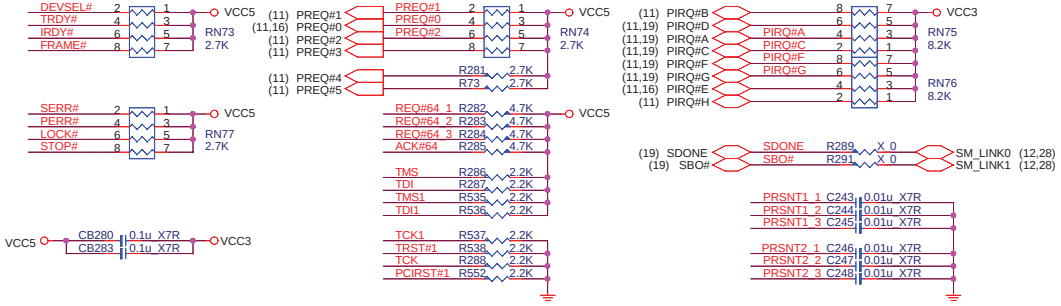
IDSEL = AD25
MASTER = PREQ#1
PIRQ#C

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

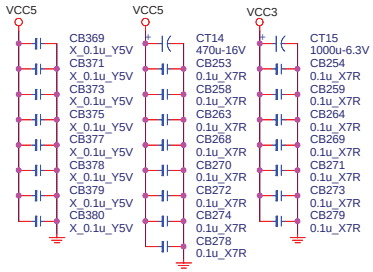


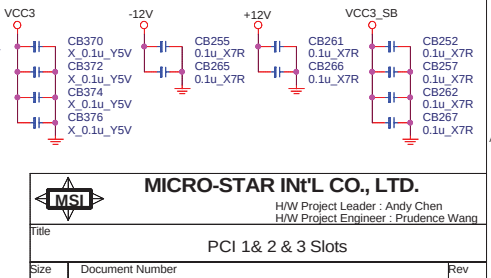
IDSEL = AD26
MASTER = PREQ#2
PIRQ#F

PCI PULL-UP / DOWN RESISTORS



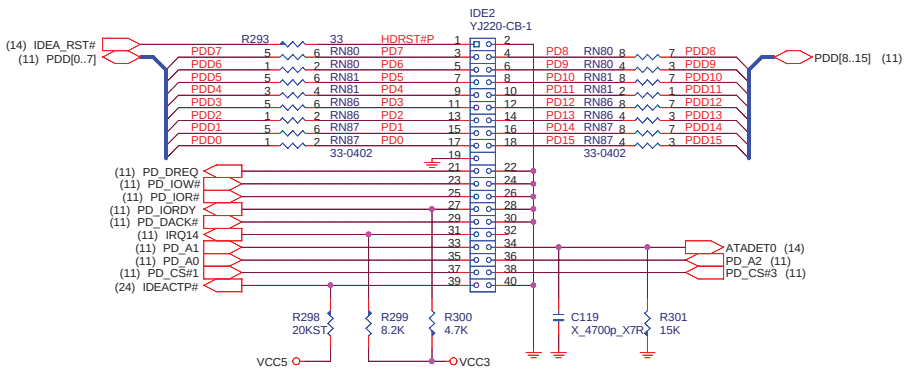
PCI SLOT DECOUPLING CAPACITORS

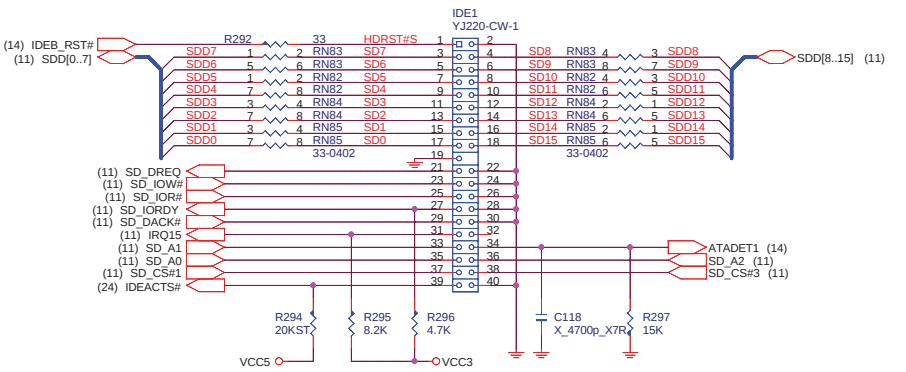




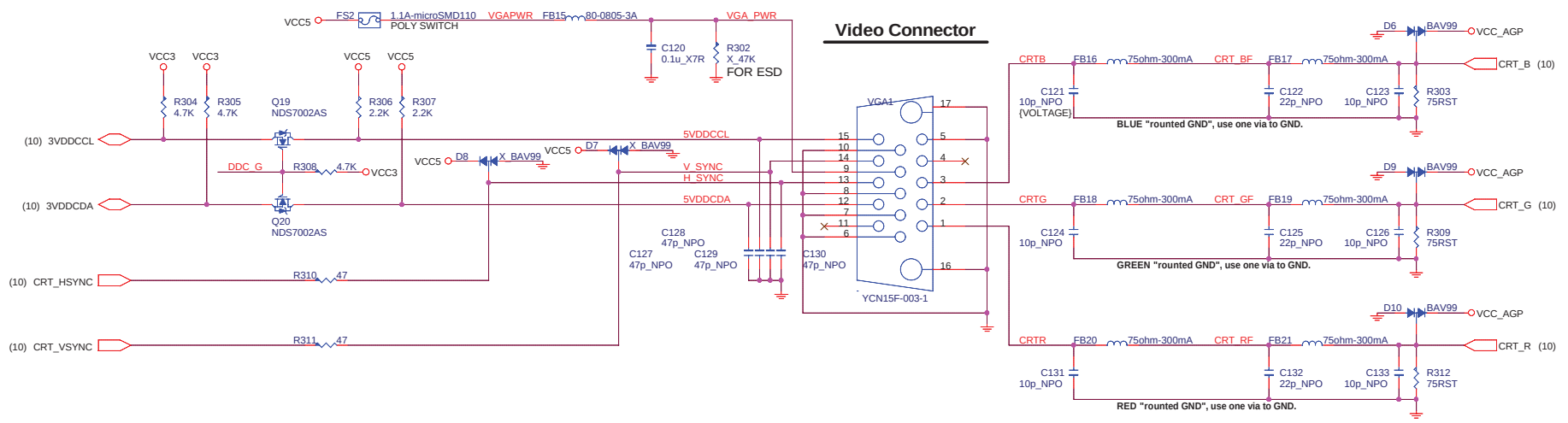
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

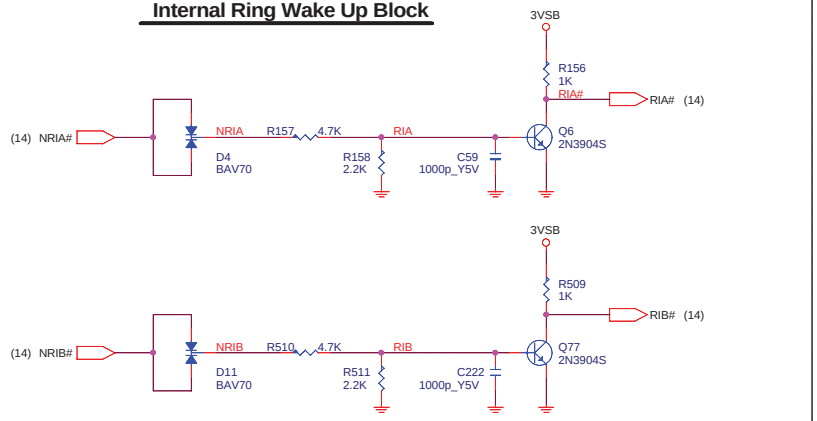
Title	PCI 1& 2 & 3 Slots	
Size	Document Number: VISE (MS-6715)	Rev: 0C
Date: Monday, October 21, 2002	Sheet 20 of 30	

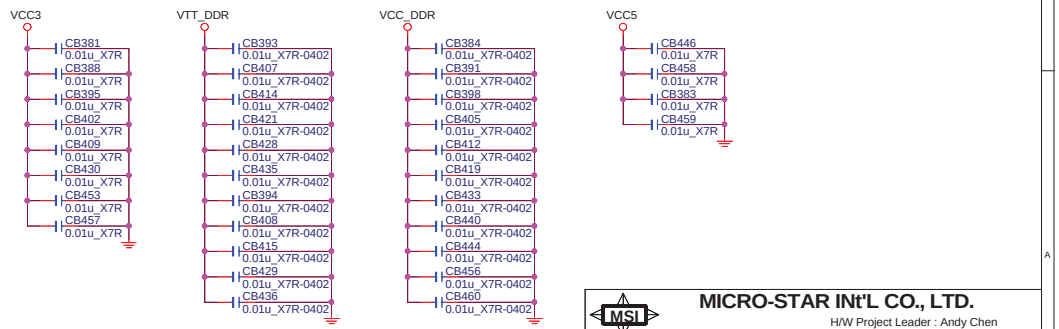




ATA 33/66/100 IDE Connectors







MICRO-STAR INt'L CO., LTD.

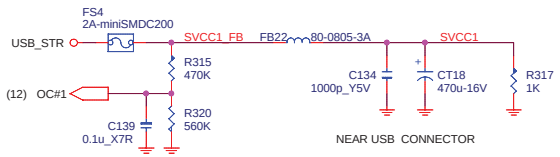
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: ATA33/66/100 IDE & VIDEO Connectors

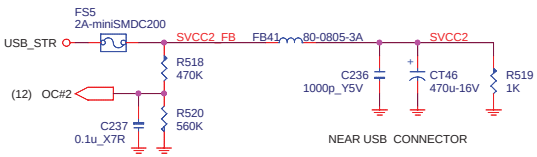
Size | Document Number: VISE (MS-6715) | Rev: 0C

Date: Monday, October 21, 2002 | Sheet 21 of 30

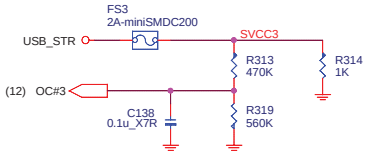
POWER CIRCUIT FOR USB PORT 0,1



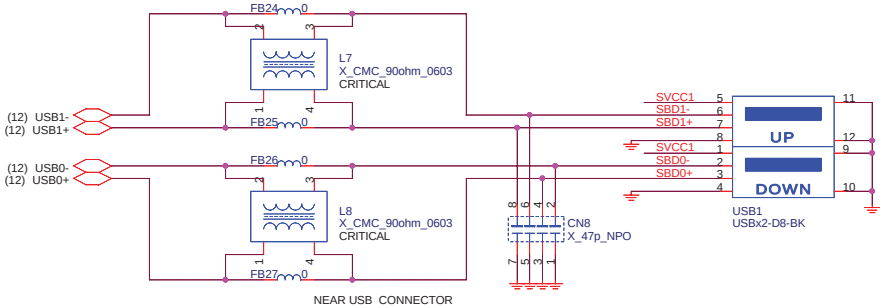
POWER CIRCUIT FOR USB PORT 2,3



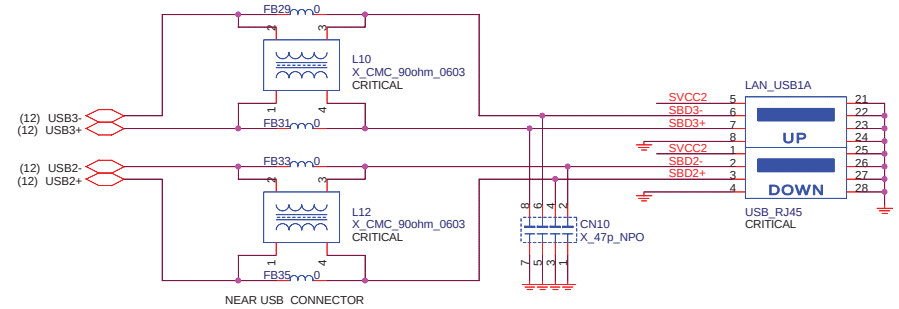
POWER CIRCUIT FOR USB PORT 4,5



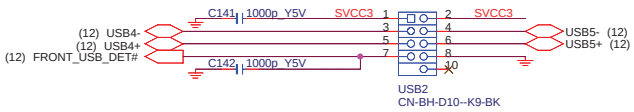
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



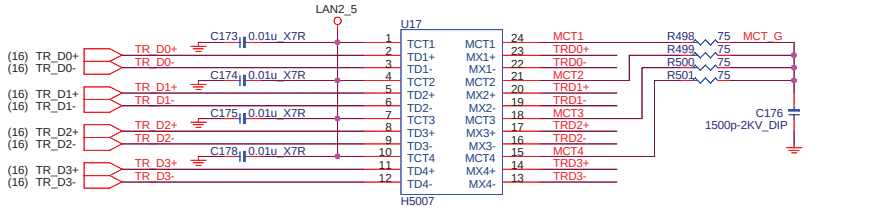
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



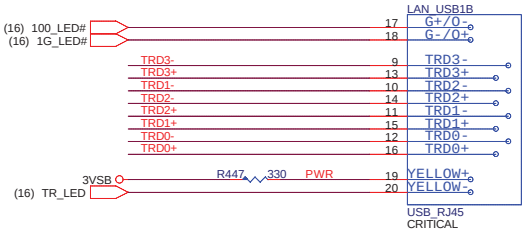
LAN MAGNETICS

	BCM4401
NOT INSTALL	C175,C178 R500,R501
Transformer	H1267

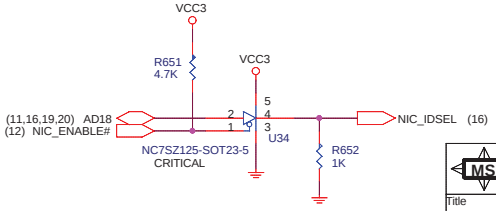
L05-0100050-P21



LAN CONNECTOR



LAN IDSEL BLOCK



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: USB & LAN Connectors

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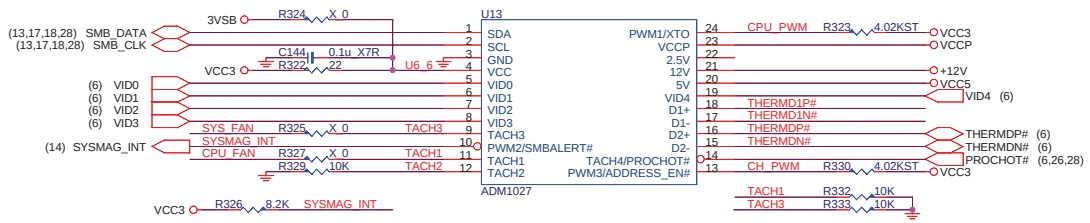
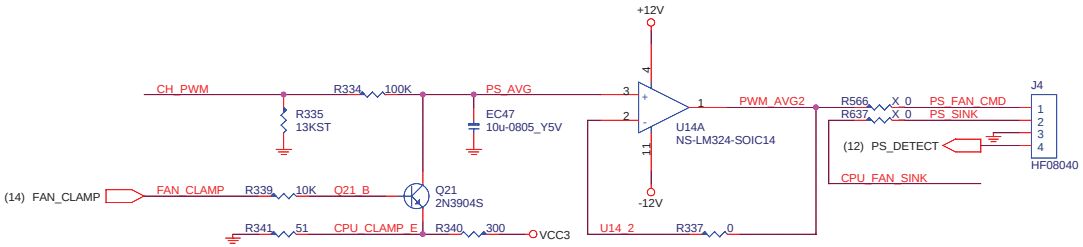
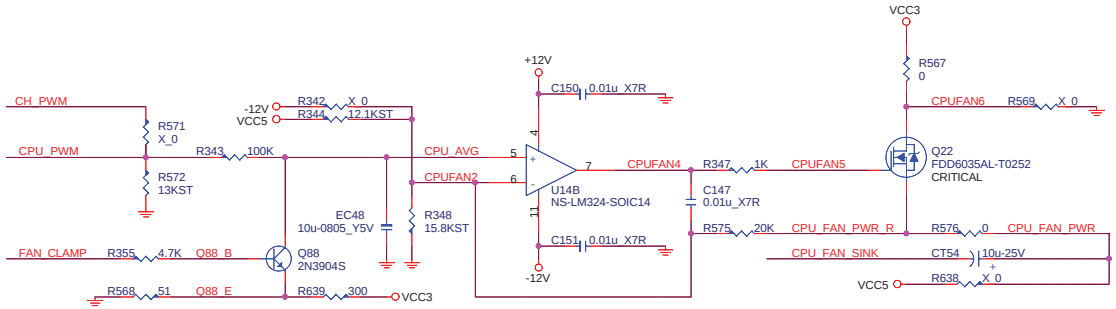
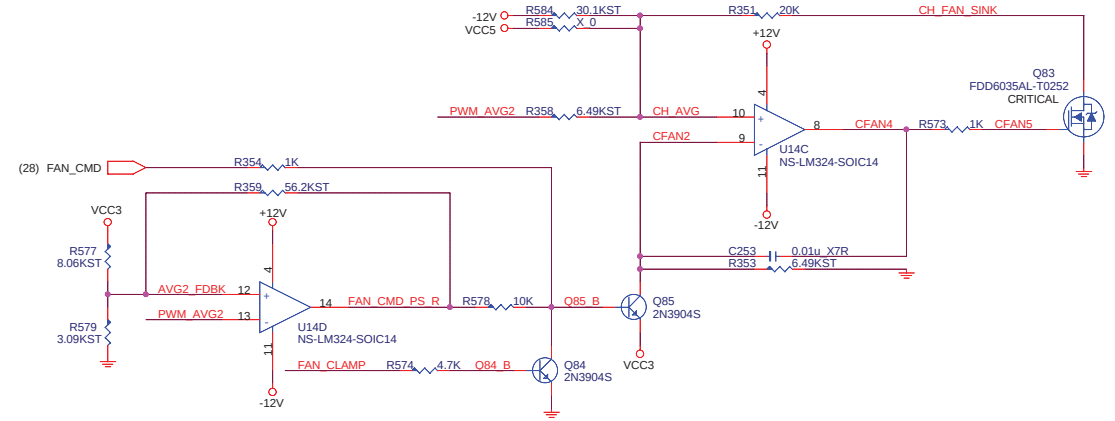
H/W MONITOR - ADM1027

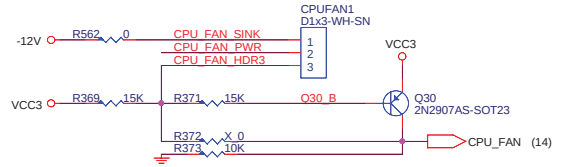




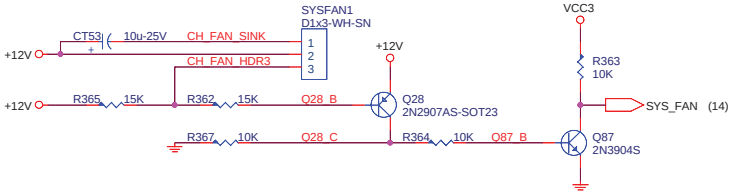




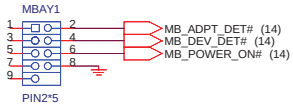
CPU FAN



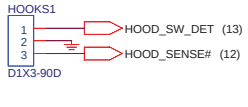
SYSTEM FAN



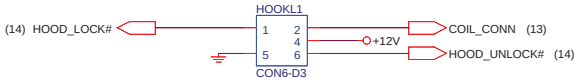
Multi Bay Circuit



Hood Sense Circuit

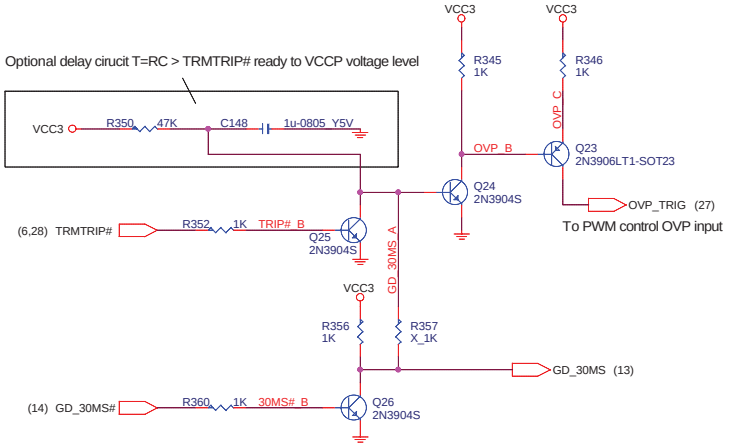


Hood Lock Circuit



PWM OVER VOLTAGE PROTECT CIRCUIT

Block function to force VCC_CORE volatge drop to zero within 0.5s after Thermaltrip active.



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	H/W MONITORING & FAN & THERMAL TRIP	
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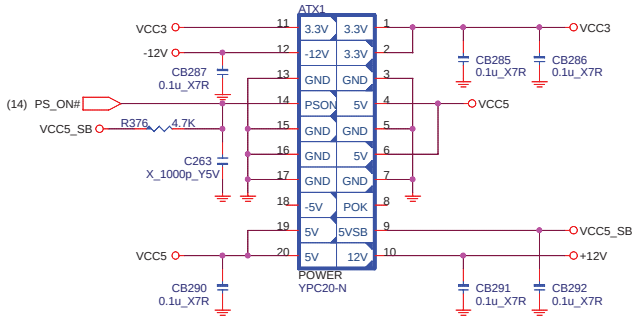
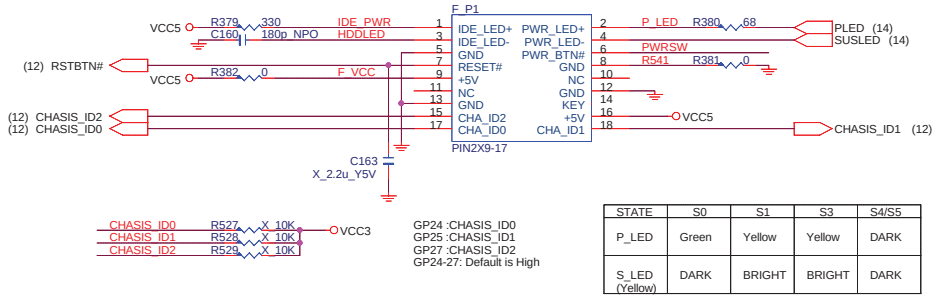
ATX Connector



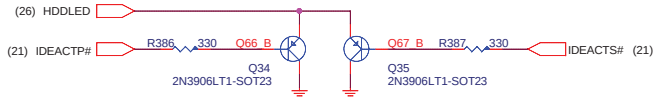
Front Panel



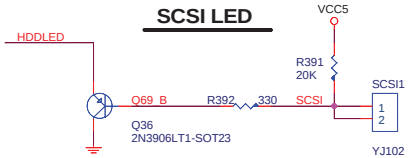
GP24 :CHASIS_ID0
GP25 :CHASIS_ID1
GP27 :CHASIS_ID2
GP24-27: Default is High

STATE	S0	S1	S3	S4/S5
P_LED	Green	Yellow	Yellow	DARK
S_LED (Yellow)	DARK	BRIGHT	BRIGHT	DARK

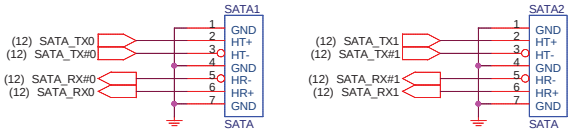
IDE LED



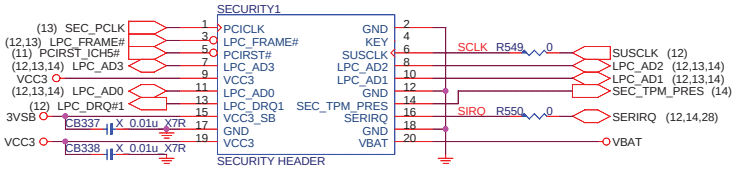
SCSI LED



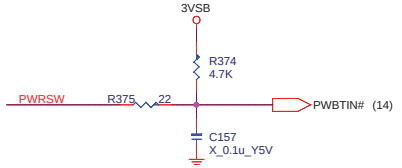
SERIAL ATA CONNECTOR BLOCK



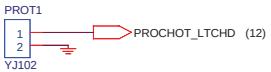
SECURITY HEADER BLOCK



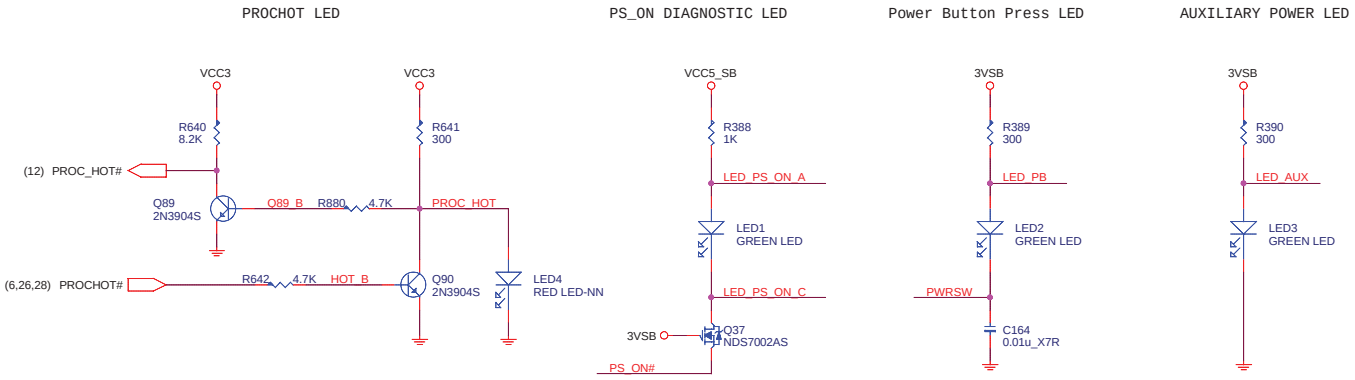
Power Button Block



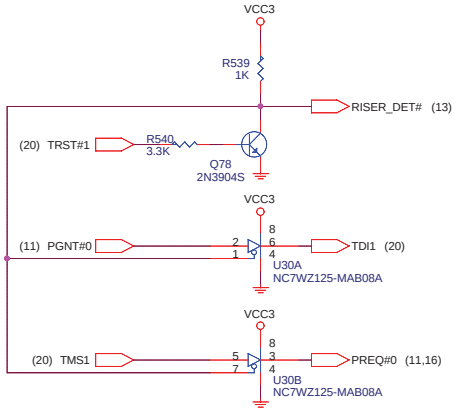
Prochot Latch Button



PCA LEDs Block



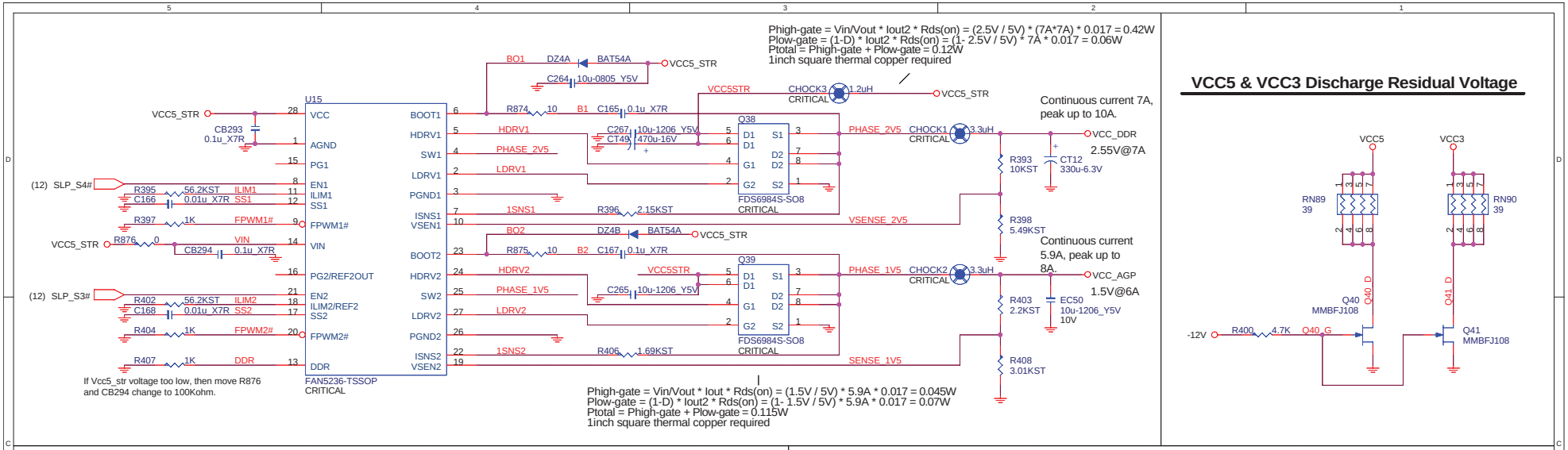
Riser Detect Block



MICRO-STAR INt'L CO., LTD.

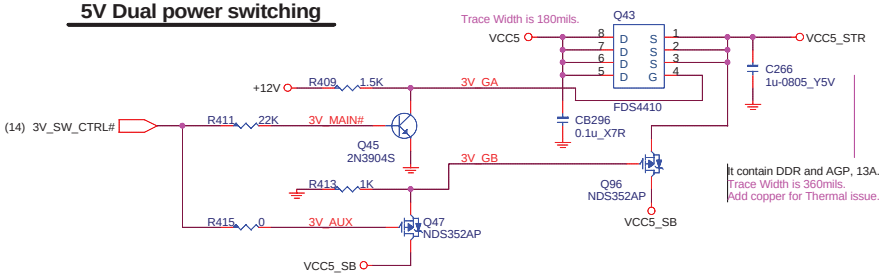
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	ATX Connector & Front Panel	
Size	Document Number: VISE (MS-6715)	Rev: 0C
Date: Tuesday, October 22, 2002	Sheet 24 of 30	

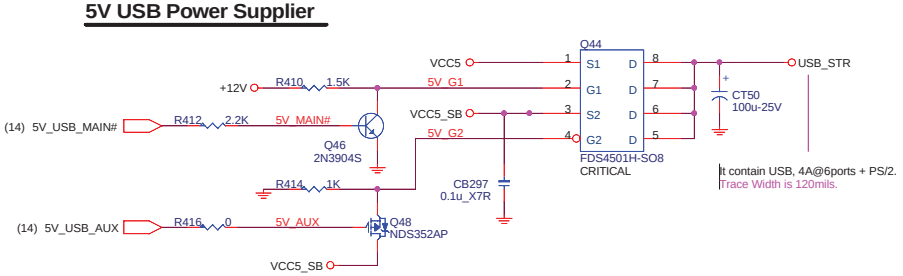


VCC5 & VCC3 Discharge Residual Voltage

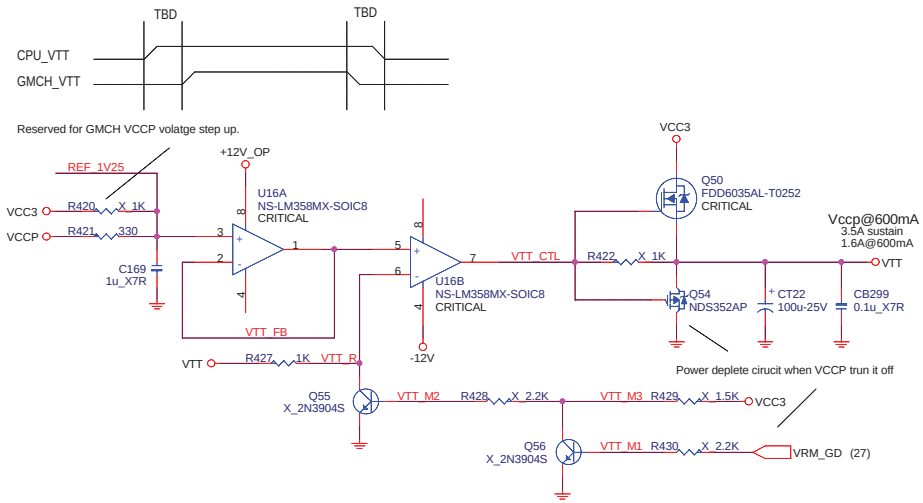
5V Dual power switching



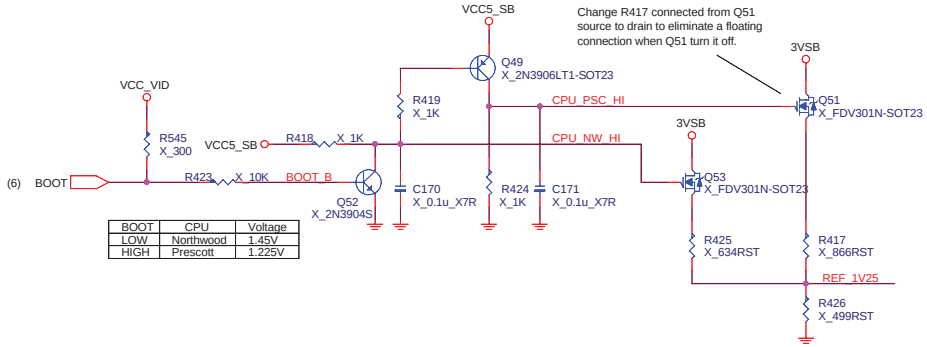
5V USB Power Supplier



GMCH VTT Generator



Intel reference GMCH VTT power cirucit



Bootstrip pin are input rather then output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side ciruit. And the bootstrip pin power by core voltage so the outside ciruit need to adjust the turn off voltage.

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: AGP & MEMORY & USB Regulator Controller

Size | Document Number: VISE (MS-6715) | Rev: 0BE1

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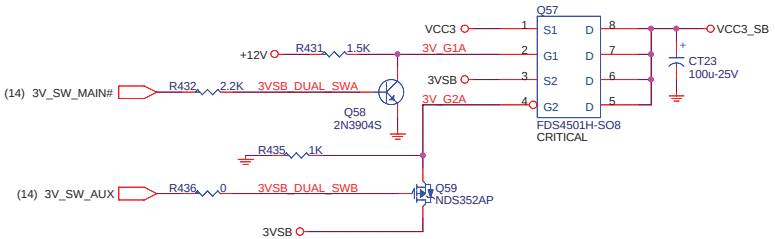
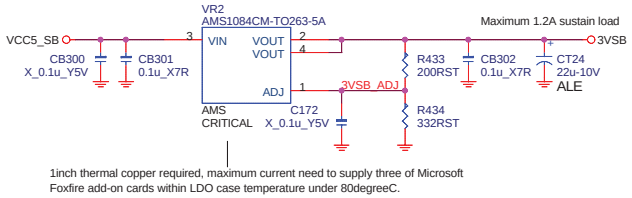
3.3V Dual Power Supplier

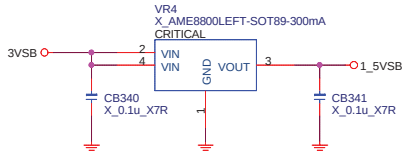


3.3V Standby Power Supplier

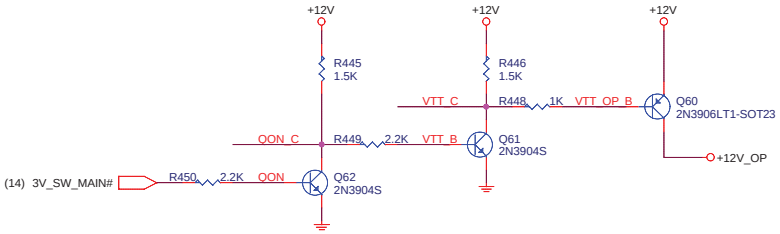


1inch thermal copper required, maximum current need to supply three of Microsoft Foxfire add-on cards within LDO case temperature under 80degreeC.

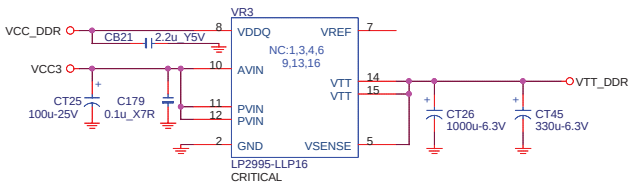
ICH5 VCCSUS1_5 VOLTAGE



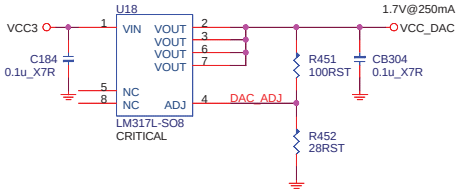
GMCH_VTT ON/OFF CIRCUIT



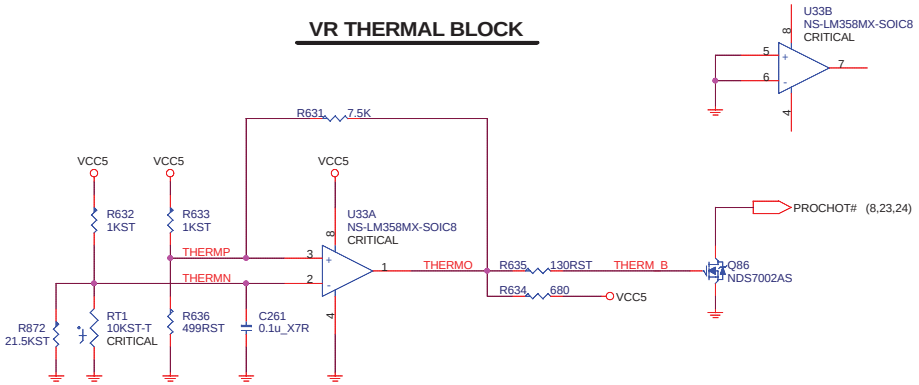
VTT_DDR VOLTAGE SUPPLIER



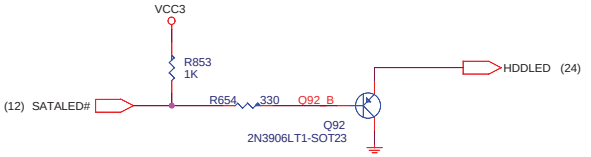
GMCH VCC_DAC Voltage Supplier



VR THERMAL BLOCK



SATA LED BLOCK



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	VCC3_SB & VCC_DAC & VTT Regulator Controller	
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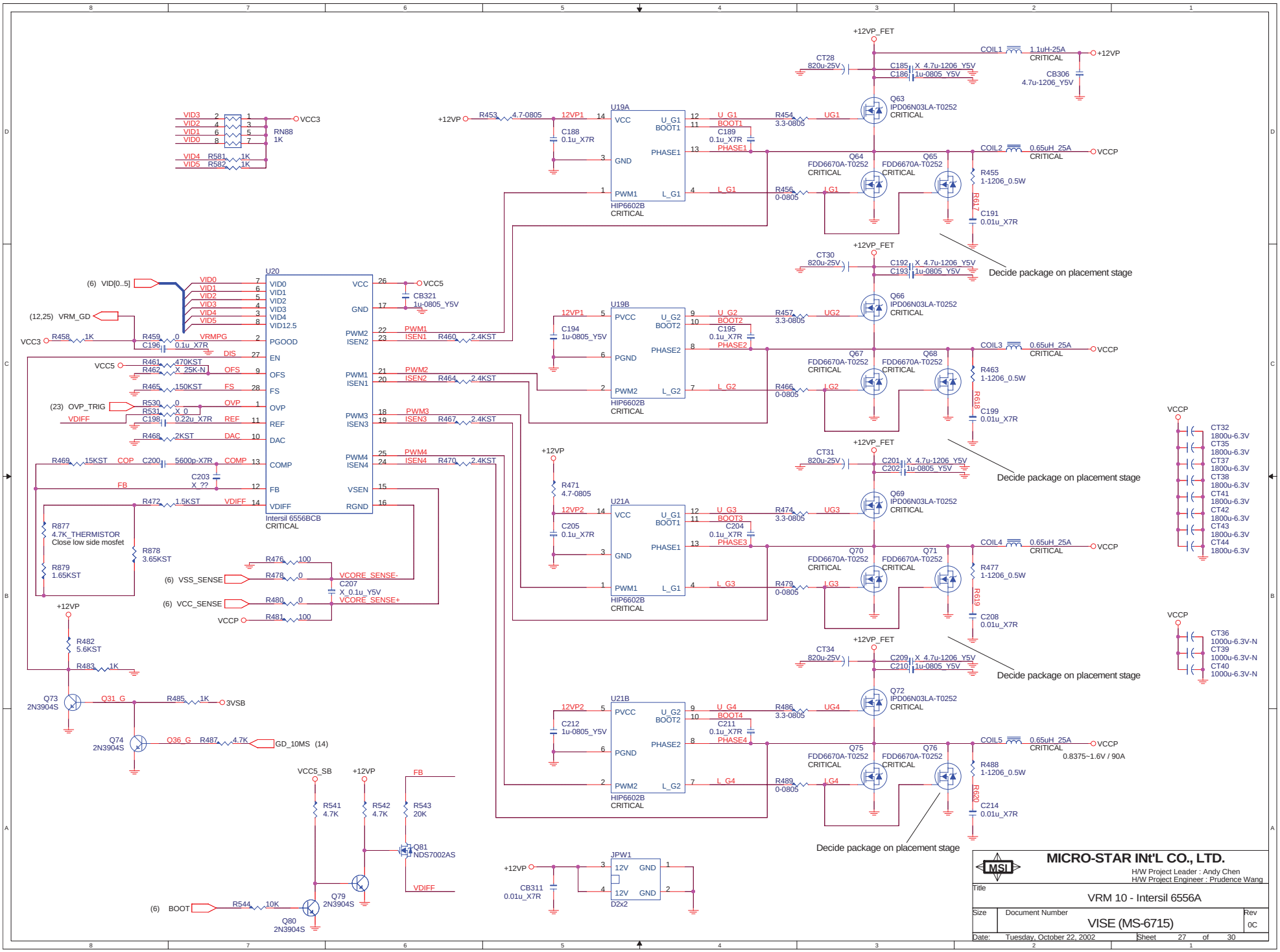
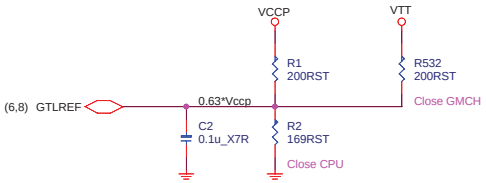
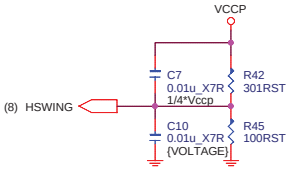

U20
Intersil 6556BCB
CRITICAL
U19A
U19B
U21A
U21B
HIP6602B
CRITICAL
Q63
Q64
Q65
Q66
Q67
Q68
Q69
Q70
Q71
Q72
Q75
Q76
IPD06N03LA-T0252
FDD6670A-T0252
CRITICAL
Decide package on placement stage
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
VRM 10 - Intersil 6556A
VISE (MS-6715)
Tuesday, October 22, 2002

CPU GTL REFERNCE VOLTAGE BLOCK

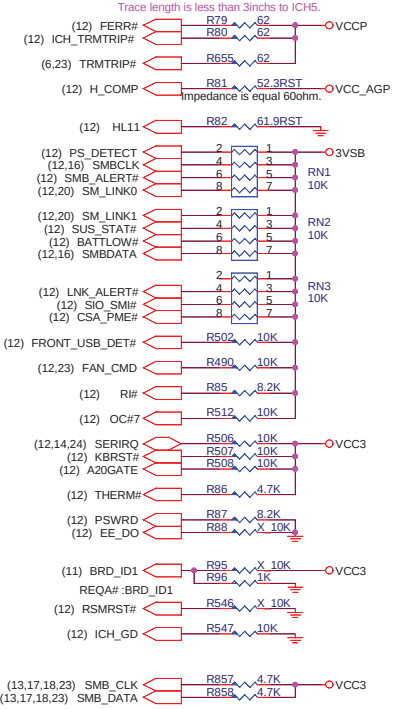




ICH5 STRAPPING RESISTORS

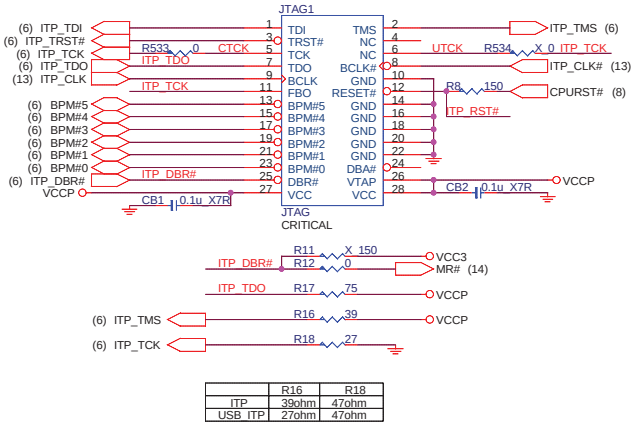
ALL COMPONENTS CLOSE TO ICH5

Trace length is less than 3inchs to ICH5.

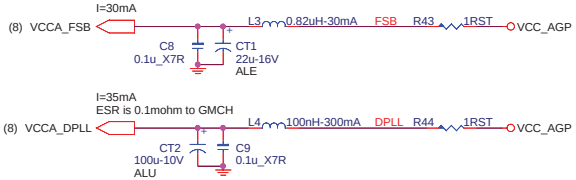


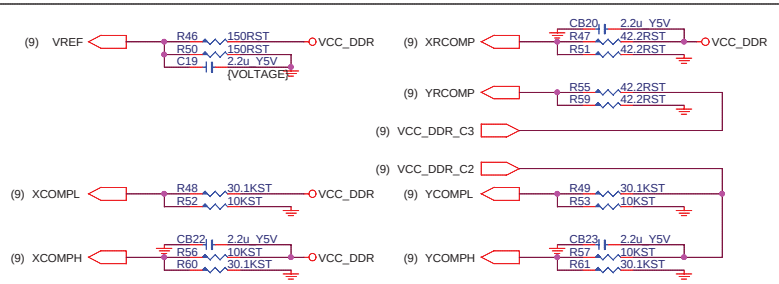
CPU ITP BLOCK

ALL COMPONENTS CLOSE TO ITP



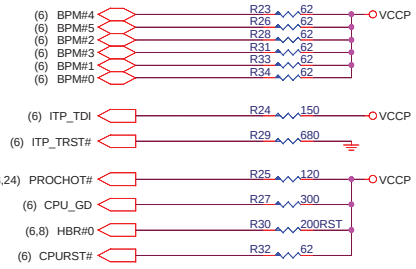
	R16	R18
ITP	39ohm	47ohm
USB_ITP	27ohm	47ohm

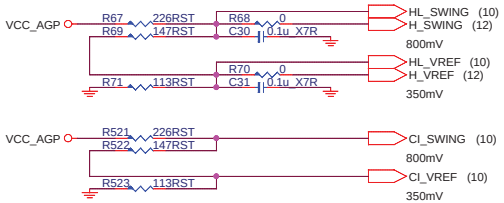




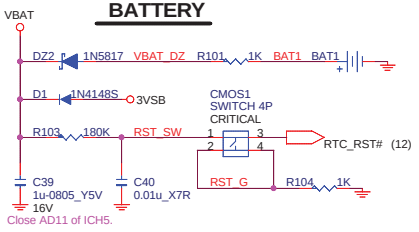
CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU

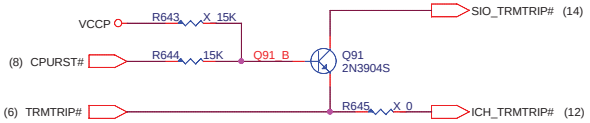


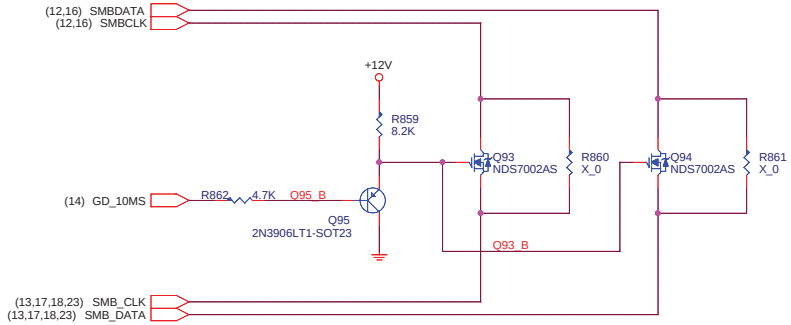


BATTERY



THERMTRIP TRANSLATION





5VREF Sequencing Circuit

MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: CPU & GMCH & ICH5 PULL UP / DOWN RESISTORS

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ICH5

GPIO Pin	Type	Function
GPIO 0	I	PCI_REQ#4 (multifunction pin)
GPIO 1	O	PCI_GNT#4 (multifunction pin)
GPIO 2	I/O	PCI_PERR# (multifunction pin)
GPIO 3	I	PCI_IRQ#E (multifunction pin)
GPIO 4	O	PWM_GPIO4 (multifunction pin)
GPIO 5	O	Unused (multifunction pin)
GPIO 6	I	USB_OC2# (multifunction pin)
GPIO 7	I	USB_OC2# (multifunction pin)
GPIO 8	I	USB_OC2# (multifunction pin)
GPIO 9	I	USB_OC3# (multifunction pin)
GPIO 10	I	USB_OC3# (multifunction pin)
GPIO 11	I	AC_SDIN1 (multifuntion pin)
GPIO 12	I	A20GATE (multifuntion pin)
GPIO 13	I	Unused (multifunction pin)
GPIO 14	I	AUD_DET# (multifunction pin)
GPIO 15	O	Unused (multifunction pin)
GPIO 16	O	Unused (multifunction pin)
GPIO 18	O	Unused (multifunction pin)
GPIO 19	I	SIO_PME# (multifunction pin)
GPIO 20	O	Unused (multifunction pin)
GPIO 21	I	SIO_SMI# (multifunction pin)
GPIO 22	I	THERM# (multifuntion pin)
GPIO 24	I	RI# (multifuntion pin)
GPIO 25	I	KBRST# (multifuntion pin)
GPIO 26	O	SUSCLK (multifunction pin)
GPIO 27	I	AGP_PME# (multifunction pin)
GPIO 28	O	Unused (multifunction pin)
GPIO 29	O	Unused (multifunction pin)
GPIO 30	O	Unused (multifunction pin)
GPIO 31	O	Unused (multifunction pin)
GPIO 32	O	EE_SEL (multifunction pin)
GPIO 33	O	EE_CLK (multifunction pin)
GPIO 34	O	EE_DO (multifuntion pin)
GPIO 35	I	EE_DI (multifuntion pin)
GPIO 36	I	SOS# (multifuntion pin)
GPIO 37	I	SOS# (multifuntion pin)
GPIO 38	I	SOS# (multifuntion pin)
GPIO 39	O	Unused (multifunction pin)
GPIO 40	I/O	SMBCLK (multifuntion pin)
GPIO 41	I/O	SMBDATA (multifuntion pin)
GPIO 42	I/O	SMBCLK1 (multifuntion pin)
GPIO 43	I/O	SMBDATA1 (multifuntion pin)
GPIO 44	I/O	DDC_CLK (multifuntion pin)
GPIO 45	I/O	DDC_DATA (multifuntion pin)
GPIO 46	O	Unused (multifunction pin)
GPIO 47	O	CH_FAN_OVRD (multifunction pin)
GPIO 48	O	LPC_CS# (multifunction pin)
GPIO 49	O	FAN_CLAMP (multifunction pin)

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD22	PCICLK0	MCP/AB20 (PCI_CLK0)
PCI Slot 2	INTD# INTA# INTB# INTC#	PCI_REQ#1 PCI_GNT#1	AD23	PCICLK1	MCP/AB18 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD24	PCICLK2	MCP/AB12 (PCI_CLK2)

LPC Super I/O

GPIO Pin	Type	Function
GPIO 10	I	VERSION_ID0
GPIO 11	I	VERSION_ID1
GPIO 12	I	CPU_FAN
GPIO 13	I	PCI_PME#
GPIO 14	I	CHASSIS_ID0
GPIO 15	I	CHASSIS_ID1
GPIO 16	I/O	Unused
GPIO 17	I/O	Unused
GPIO 20	I/O	ATADET0
GPIO 21	I/O	ATADET1
GPIO 22	I/O	Unused
GPIO 23	I	BOARD_ID0
GPIO 24	I/O	SIO_ADDR
GPIO 25	I/O	Unused
GPIO 26	I	CPUOCC#
GPIO 27	I	BOARD_ID1
GPIO 30	O	PLED
GPIO 31	O	SUSLED
GPIO 32	I/O	TRMTRIP#
GPIO 33	I/O	FDD_DET
GPIO 34	O	BIOS Protect
GPIO 35	I/O	Unused
GPIO 36	O	MOB#
GPIO 37	O	DSB#
GPIO 40	O	DRVDEN0
GPIO 41	I/O	Unused
GPIO 42	O	SIO_PME#
GPIO 43	I	HM_INIT#

GPIO Pin	Type	Function
GPIO 44	I/O	Unused
GPIO 45	I/O	Unused
GPIO 46	O	SIO_SMI#
GPIO 50	I/O	Unused
GPIO 51	I/O	Unused
GPIO 52	I/O	Unused
GPIO 53	I/O	Unused
GPIO 54	I/O	Unused
GPIO 55	I/O	Unused
GPIO 56	I/O	Unused
GPIO 57	I/O	Unused
GPIO 60	I/O	Unused
GPIO 61	I/O	Unused
GPIO 62	I	PWBTIN#
GPIO 63	I	DLY_S3#
GPIO 64	I	SLP_S5#
GPIO 65	I	USB_SENS
GPIO 66	O	PWRBTN#
GPIO 67	O	PS_ON
GPIO 70	I/O	Unused
GPIO 71	I	RISER#1
GPIO 72	I	RISER#2
GPIO 73	I	PHY_DIS
GPIO 74	I/O	PHY Disable
GPIO 75	O	GD_10MS
GPIO 76	O	GD_30MS
GPIO 85	I/O	Unused
GPIO 86	I/O	Unused

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2	1010010B	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 1	1010001B	MCLK_B0/MCLK_B0# MCLK_B1/MCLK_B1# MCLK_B2/MCLK_B2#

PCI RESET DEVICE

Signals	Target
PCIRST#1	Northbridge
PCIRST#0	FWH, Super I/O,AGP slot
PCIRST#2	PCI slot 1-3, PCI Riser
HDDRST#	Primary, Scondary IDE

BIOS Protect Config.	
BIOS Un_Protected	1
BIOS Protected	0

Flash ROM

GPIO Pin	Type	Function
GPI 0	I	Pull down through 1K ohms (unused)
GPI 1	I	Pull down through 1K ohms (unused)
GPI 2	I	Pull down through 1K ohms (unused)
GPI 3	I	Pull down through 1K ohms (unused)
GPI 4	I	Pull down through 1K ohms (unused)

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Title: General Purpose Spec
Size | Document Number: VISE (MS-6715) | Rev: 0C
Date: Monday, October 21, 2002 | Sheet 29 of 30