MS-6714

Version 300

INTEL (R) Brookdale-G/GL/GE/GV Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU: Willamette/Northwood mPGA-478B Processor

System Brookdale-G / GE / PE Chipset:

INTEL GMCH + ICH4

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF-AW

Clock Generator -- CY28349

AC'97 Codec -- RealTek AC650

Onboard Lan Chipset-- RealTek RTL8101L

Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 3

Platform: Micro ATX

MODEL Config.	ORCAD Config.	Function	Option	ERP Number
MS6714GE STD	cfg6714GE-STD	GE STD	STD	601-6714-010
MS6714GE Option:L	cfg6714GE-LAN	GE STD+LAN	L	601-6714-020
MS6714GV STD	cfg6714GV-STD	GV STD	GV	601-6714-030
MS6714GV Option:L	cfg6714GV-LAN	GV STD+LAN	GVL	601-6714-040
MS6714G STD	cfg6714G-STD	G STD	GB	601-6714-07S
MS6714G Option:L	cfg6714G-LAN	G STD+LAN	GBL	601-6714-08S
MS6714GL STD	cfg6714GL-STD	GL STD	GL	601-6714-05S
MS6714GL Option:L	cfg6714GL-LAN	GL STD+LAN	GLL	601-6714-06S

MICRO-STAR

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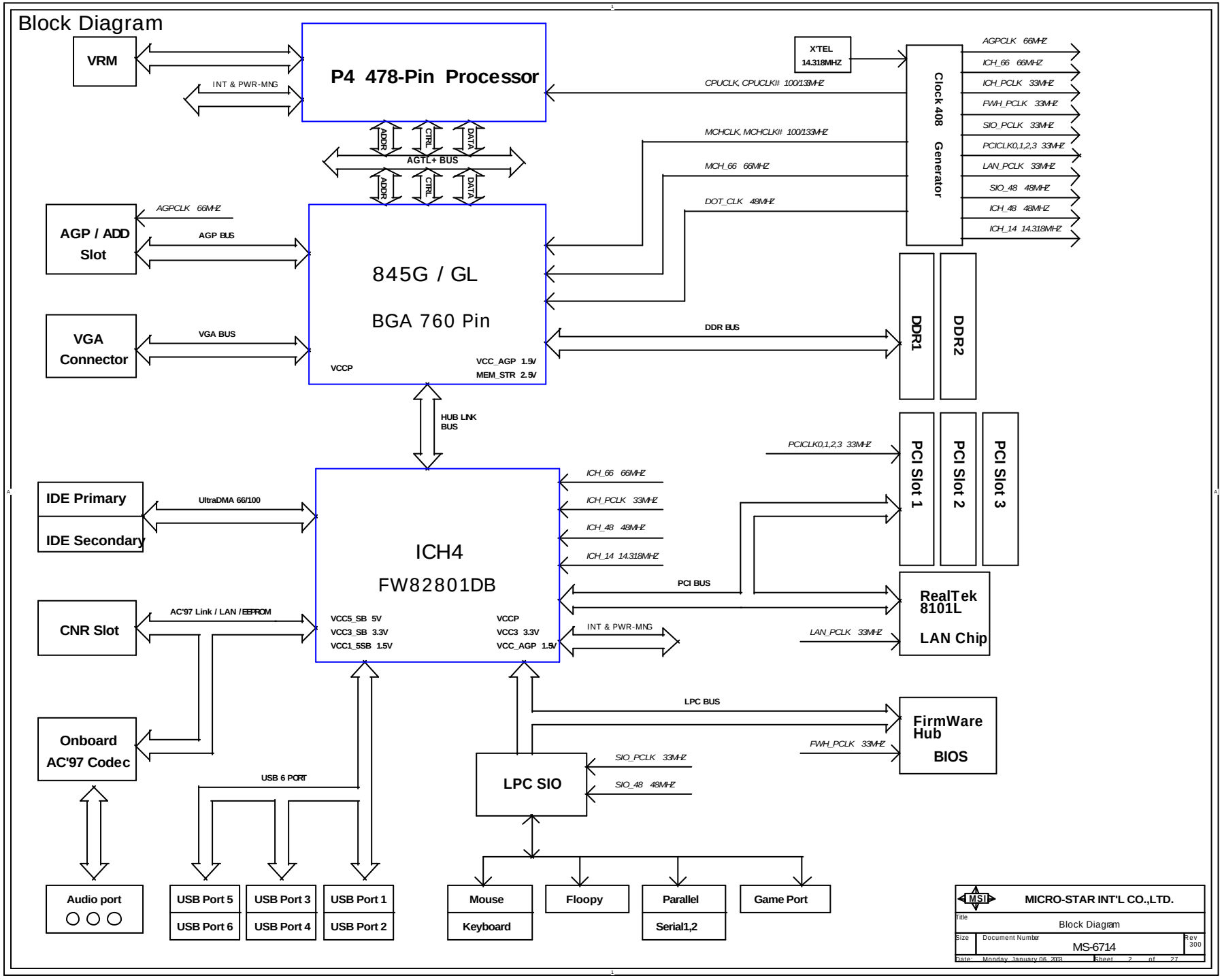
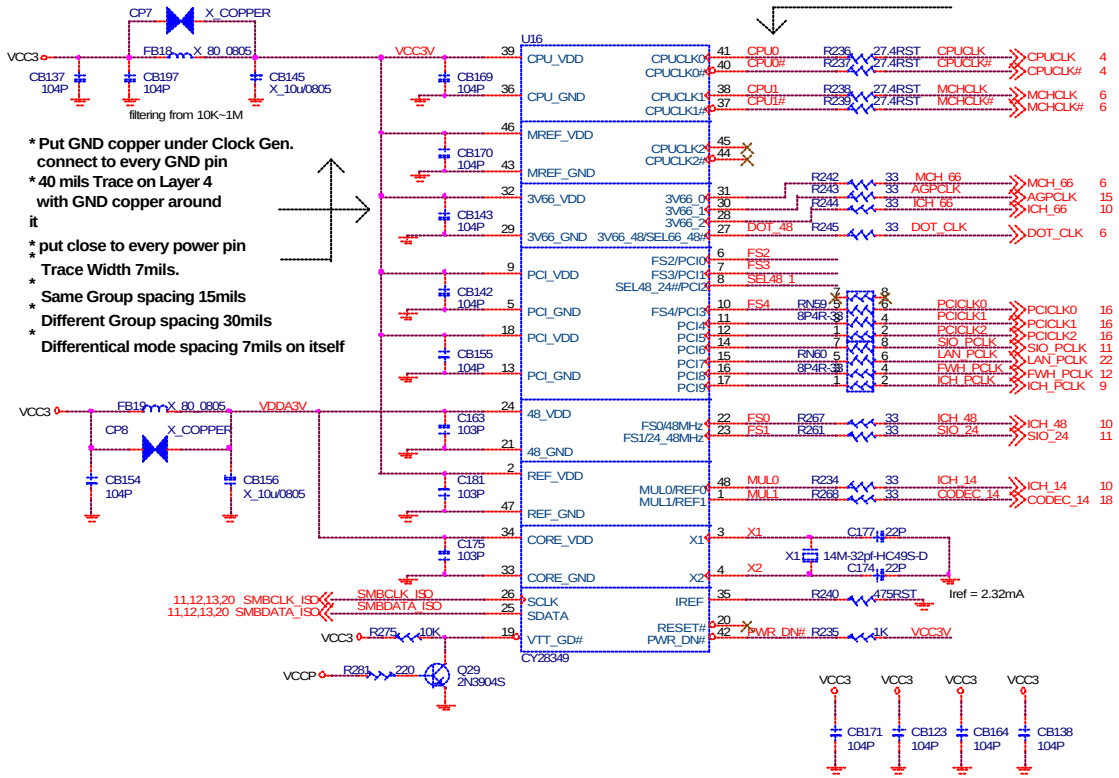
Block Diagram



CLOCK GENERATOR BLOCK

*Trace < 0.5"



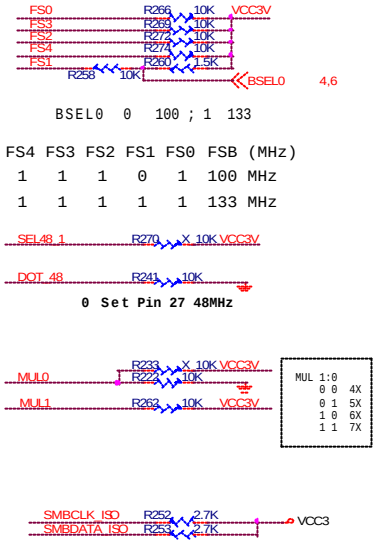
* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differentical mode spacing 7mils on itself

Shut Source Termination Resistors

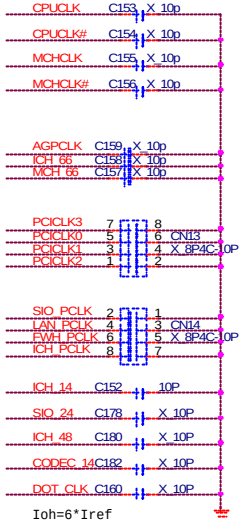
Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



Pull-Down Capacitors

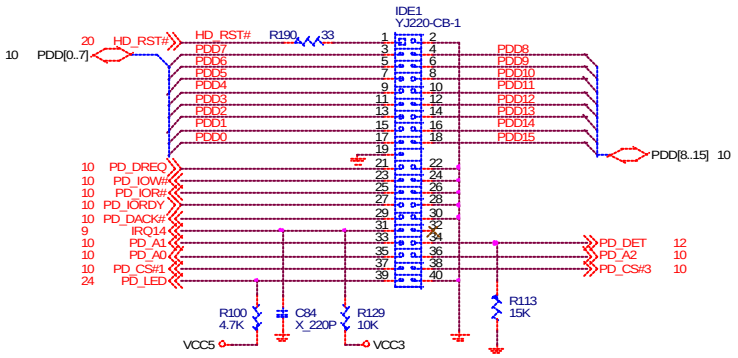


Ioh=6*Iref
Voh=0.71V

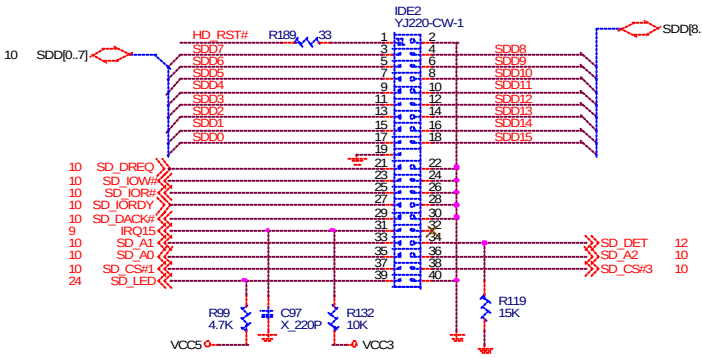
used only for EMI issue

Trace less 0.2"

PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



ATA100 IDE CONNECTORS

* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than5"

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Title	CLOCK GEN & ATA100 IDE	
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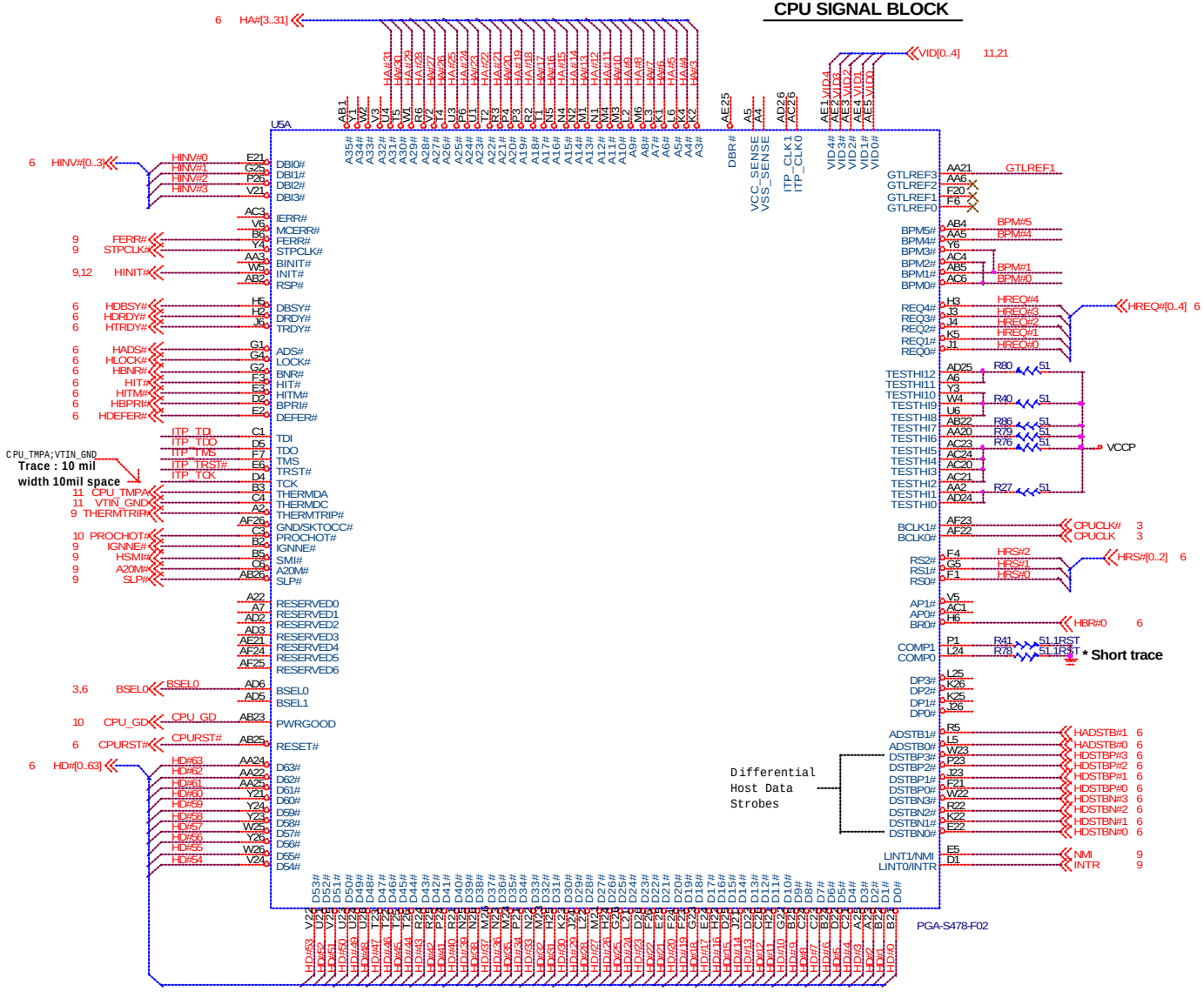
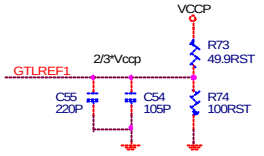
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK

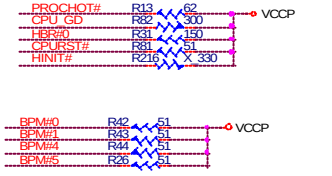


Every pin put one 220pF cap near it.
Trace Width 10mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK

ALL COMPONENTS CLOSE TO CPU

CPU STRAPPING RESISTORS



MSI	MICRO-STAR	
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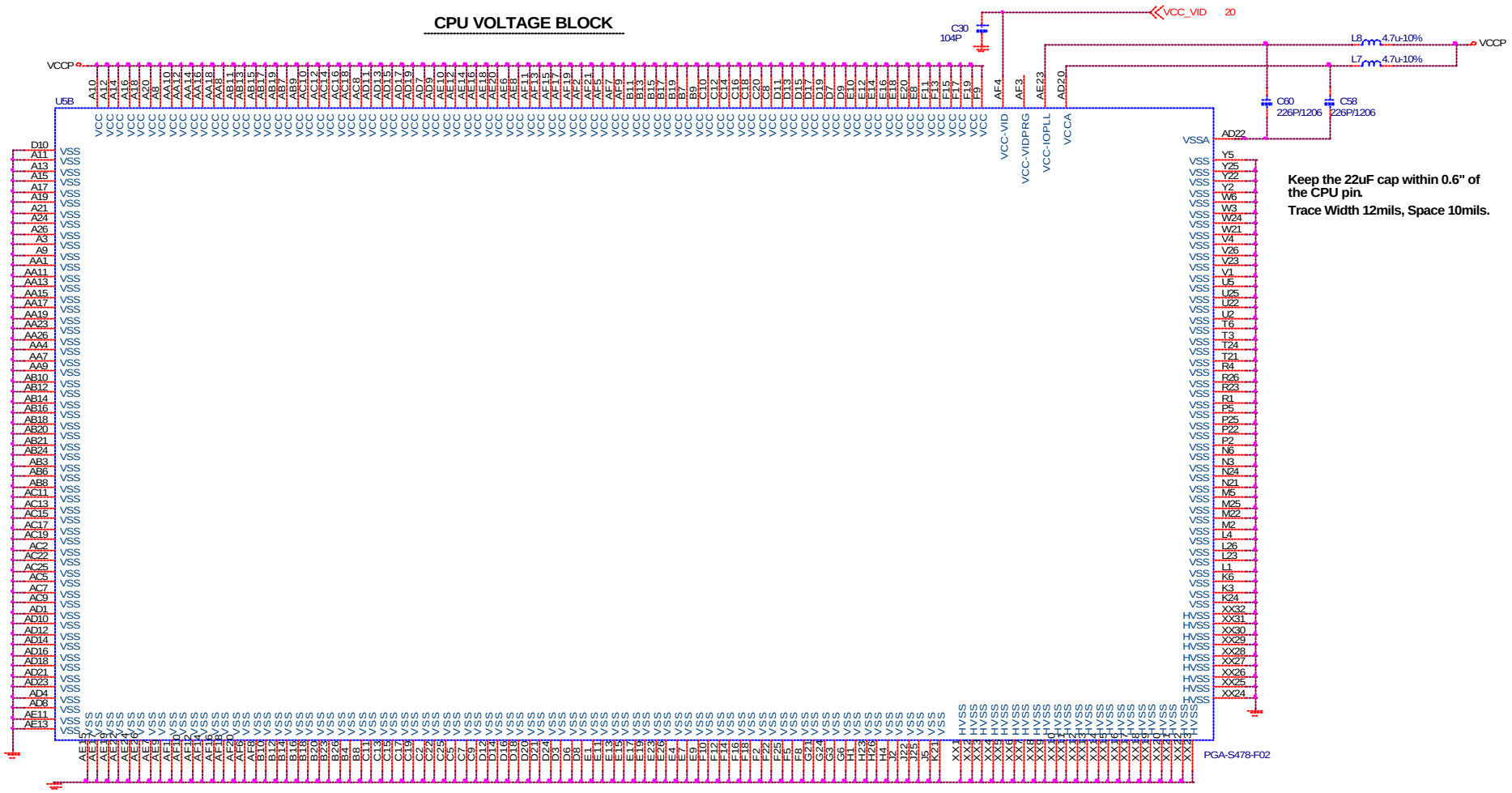
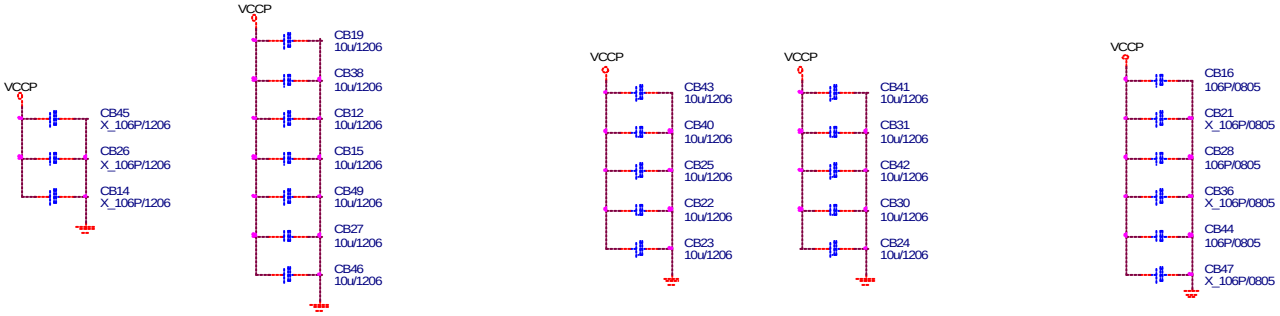
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



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Title: INTEL mPGA478-B CPU2

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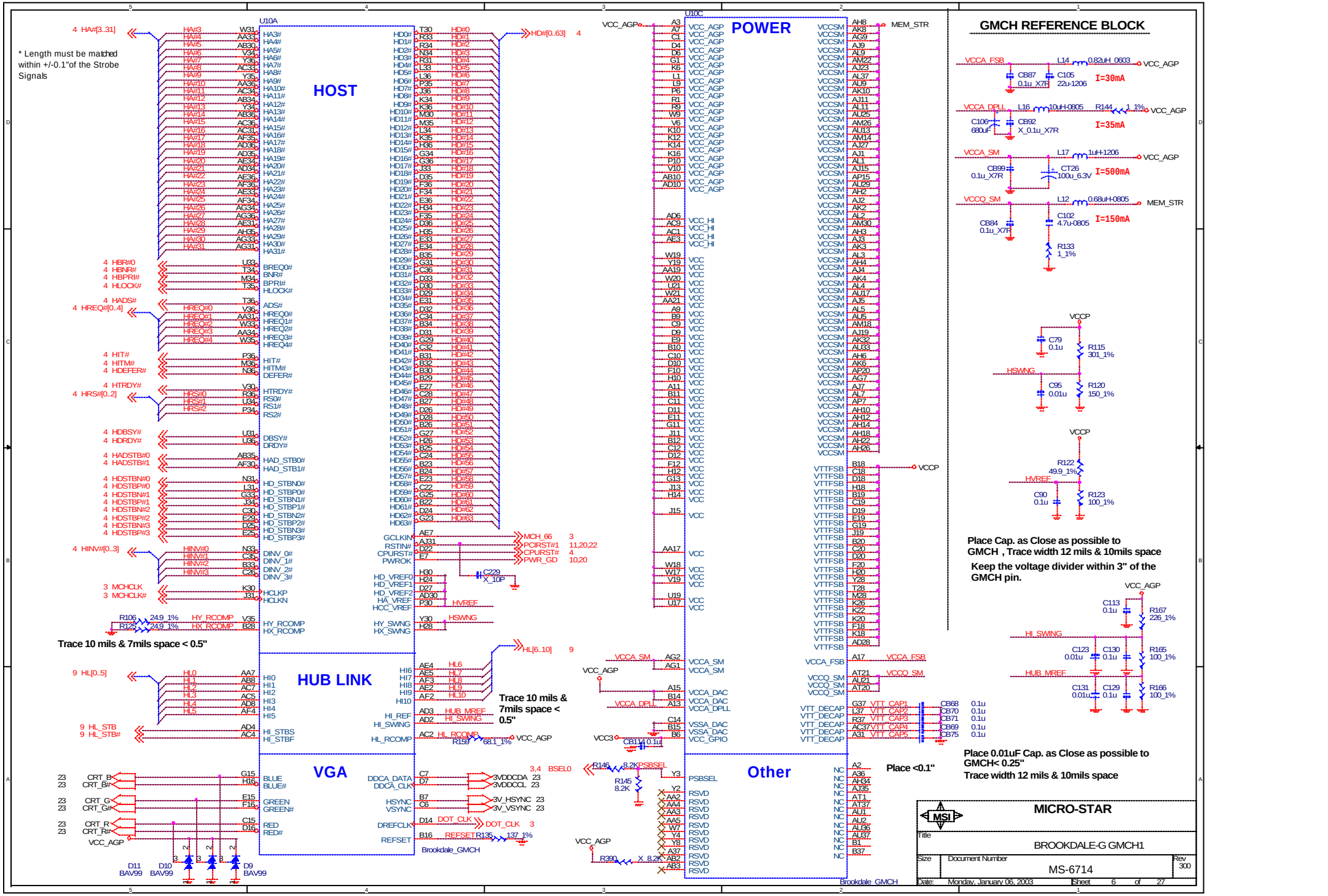
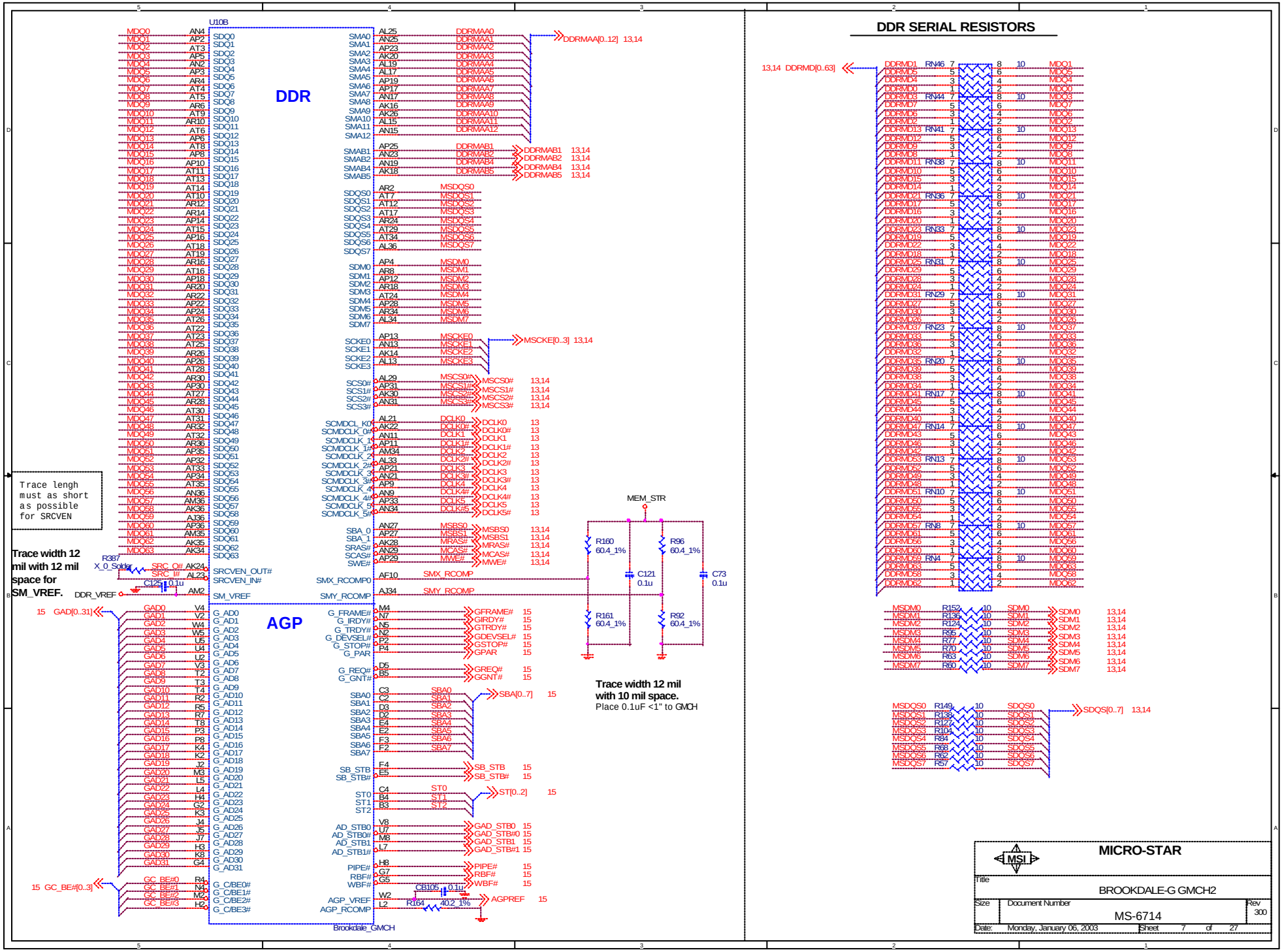

HOST
POWER
HUB LINK
VGA
Other
GMCH REFERENCE BLOCK
* Length must be matched within +/-0.1"of the Strobe Signals
Trace 10 mils & 7mils space < 0.5"
Trace 10 mils & 7mils space < 0.5"
Place Cap. as Close as possible to GMCH , Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the GMCH pin.
Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space
Place <0.1"
MICRO-STAR
BROOKDALE-G GMCH1
MS-6714
Brookdale_GMCH
Monday, January 06, 2003


DDR
AGP
U10B
Brookdale_GMCH
Trace lengh must as short as possible for SRCVEN
Trace width 12 mil with 12 mil space for SM_VREF.
Trace width 12 mil with 10 mil space.
Place 0.1uF <1" to GMCH
MEM_STR
DDR SERIAL RESISTORS
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MSI
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BROOKDALE-G GMCH2
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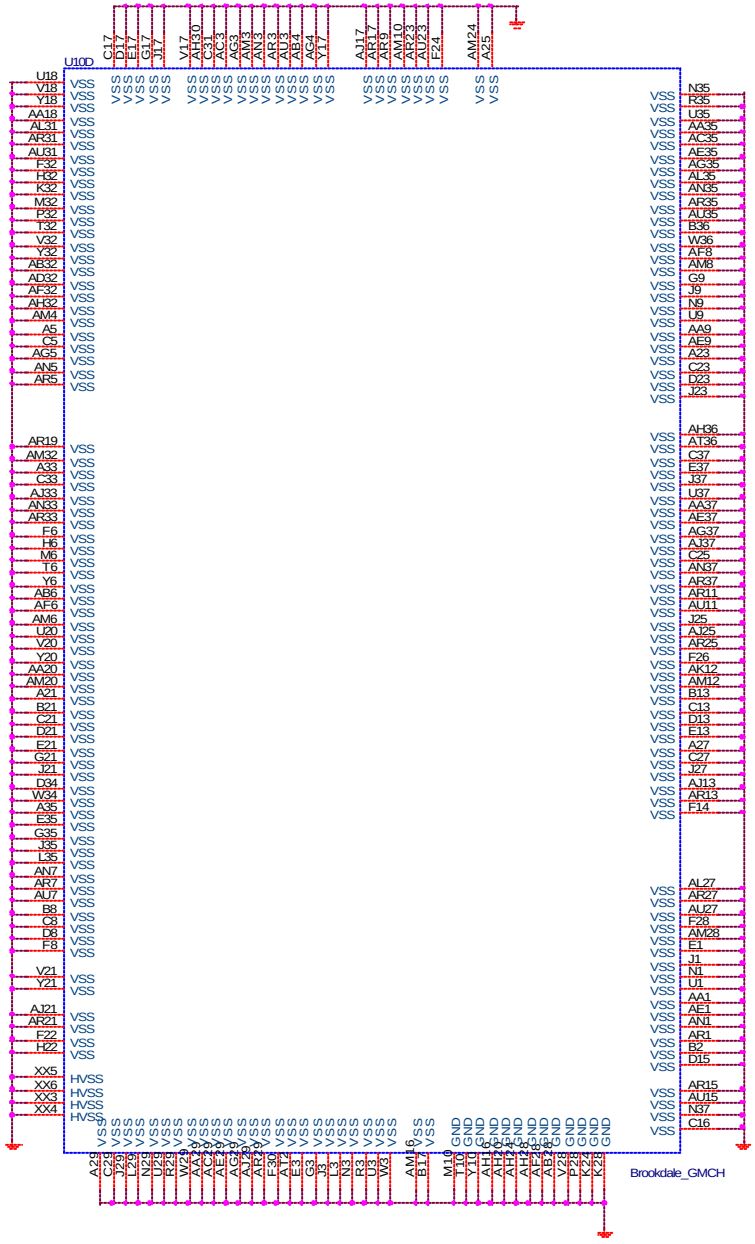
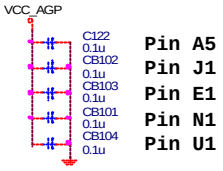
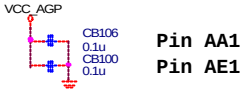


GMCH DECOUPLING CAPACITOR



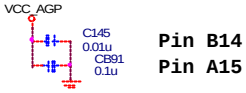
Pin A5
Pin J1
Pin E1
Pin N1
Pin U1

Place decoupling cap close to GMCH AGP Interface < 0.1"



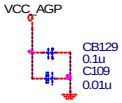
Pin AA1
Pin AE1

Place decoupling cap close to GMCH Hub-Link Interface< 0.1"

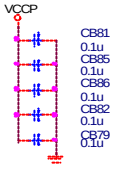


Pin B14
Pin A15

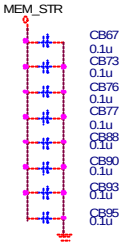
Place decoupling cap close to GMCH DAC Interface< 0.1"



Place decoupling cap close to GMCH Core Logic Interface < 0.1"

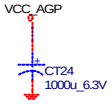


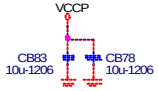
Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor



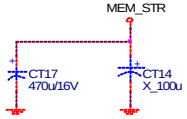
Pin AL37
Pin AU33
Pin AU29
Pin AU25
Pin AU17
Pin AU13
Pin AU9
Pin AU5

Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width





Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot

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Title: Broodale-G GMCH3

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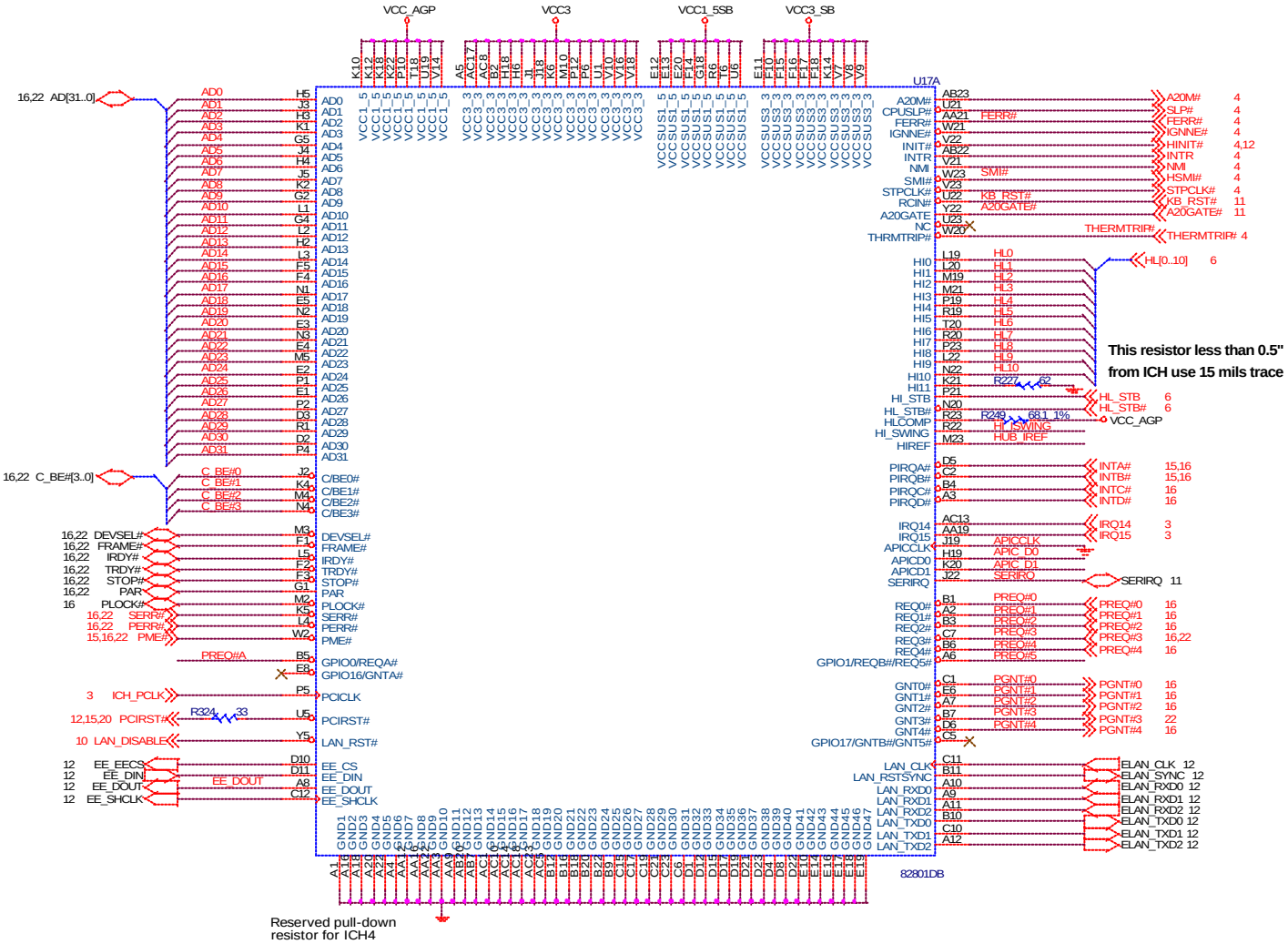
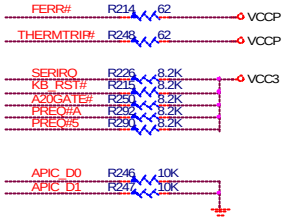
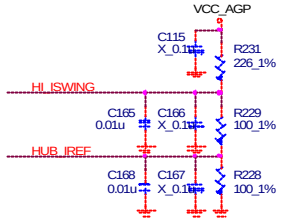
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



ICH4 PULL-UP/DOWN RESISTORS



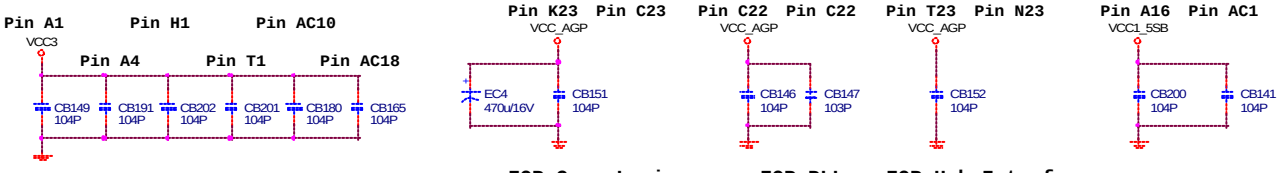
ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



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Title: ICH4 PCI/HI/LAN

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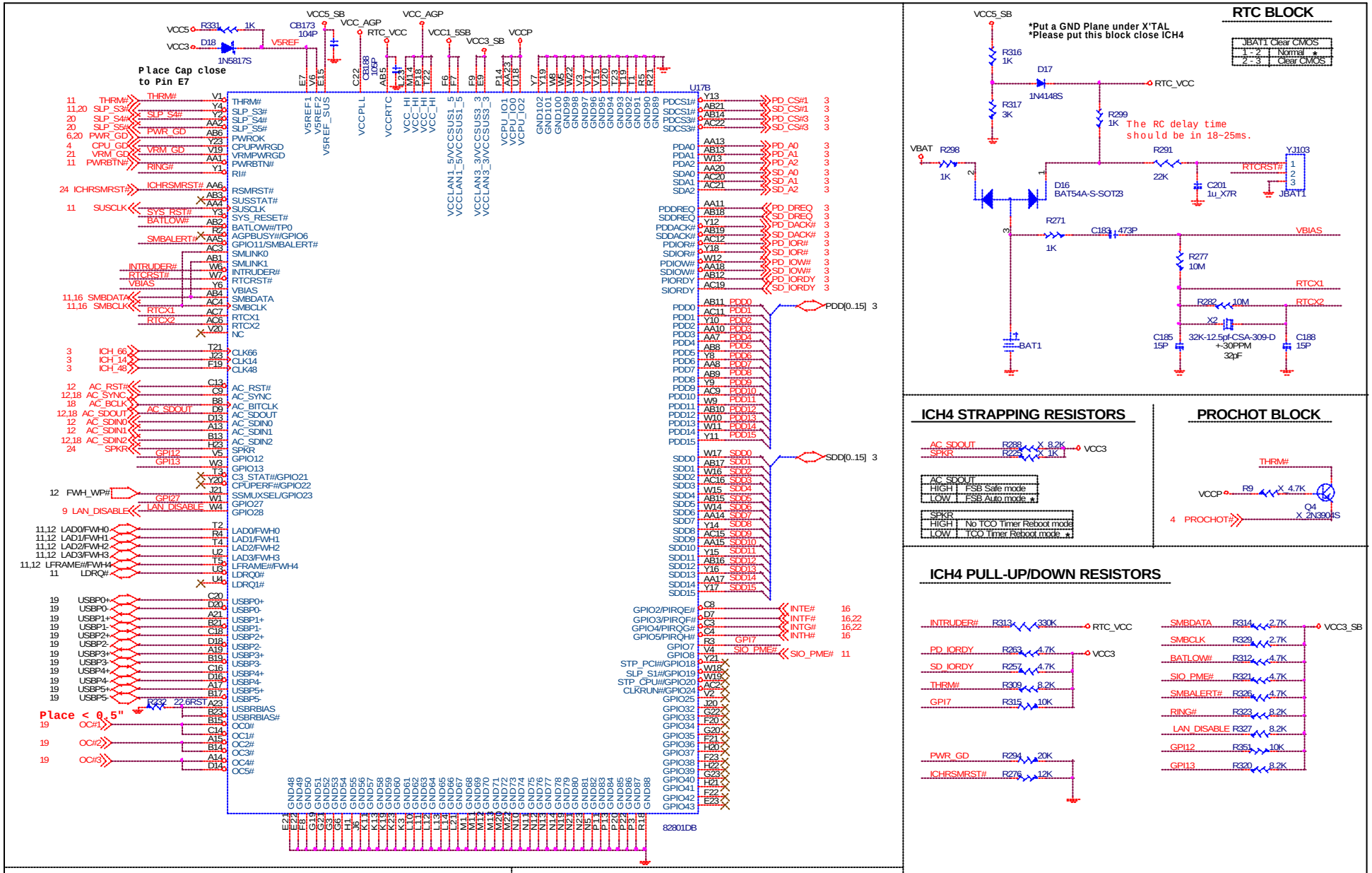


RTC BLOCK

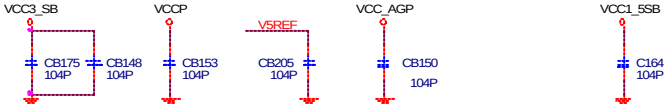
ICH4 STRAPPING RESISTORS

PROCHOT BLOCK

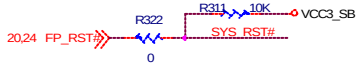
ICH4 PULL-UP/DOWN RESISTORS

ICH4 DECOUPLING CAPACITOR

Place one 0.1u close to ICH4 <100 mil



SYSTEM RESET



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Title: ICH4 OTHER

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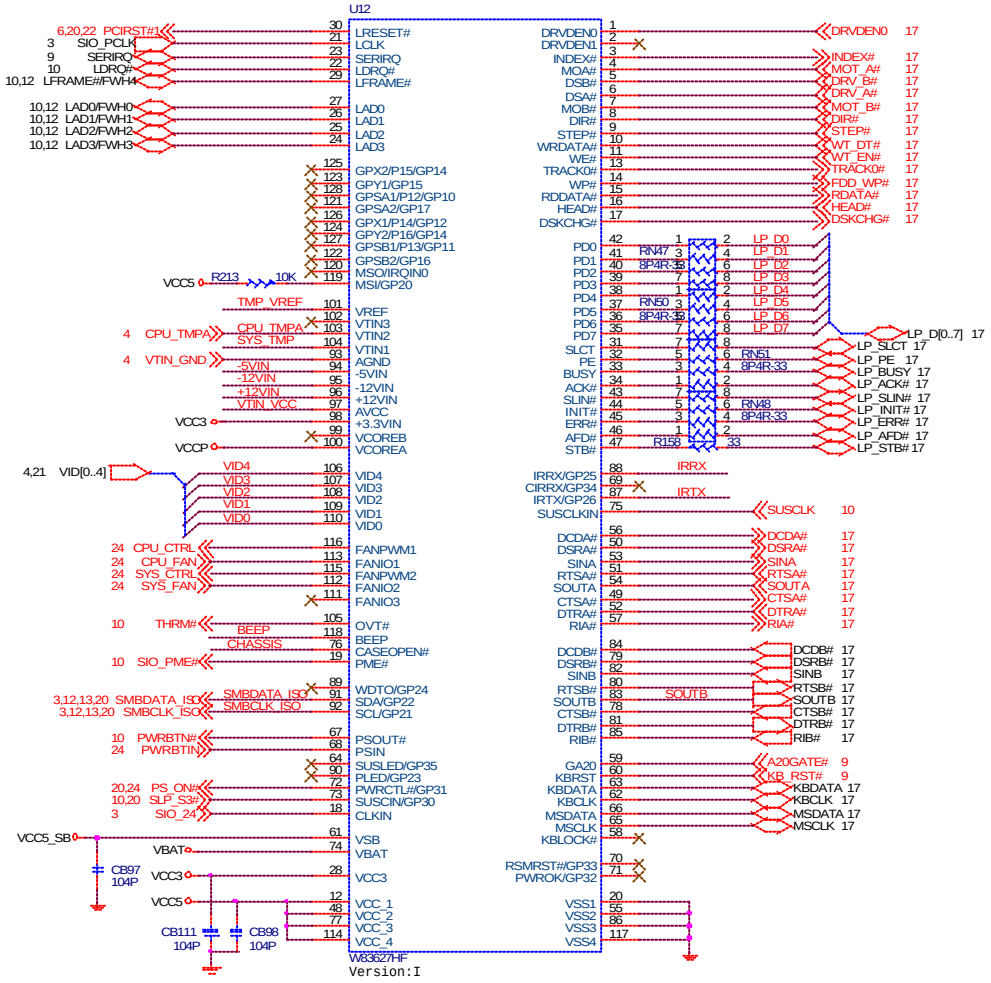
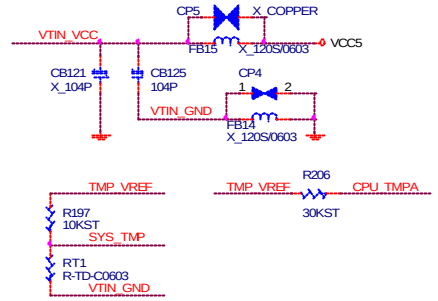
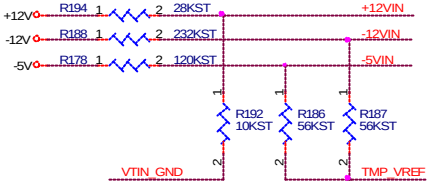
LPC SUPER I/O W83627HF



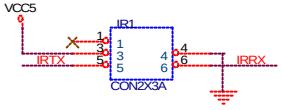
THERMAL RESISTOR BLOCK



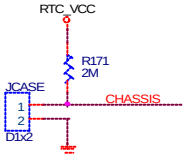
NOTE: LOCATE CLOSE STATUS PANEL



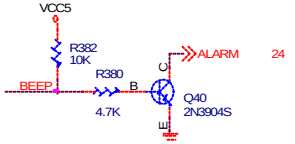
Intel Front IR Header



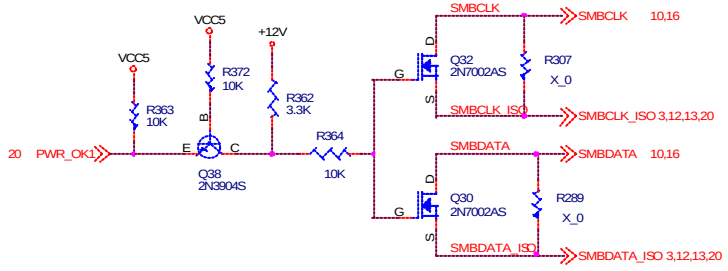
Chasiss Intrusion Header



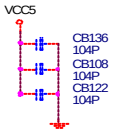
SPEAKER BLOCK



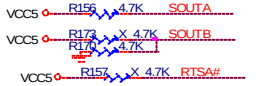
SMBus Isolation



LPC I/O DECOUPLING CAPACITORS



SUPER I/O STRAPPING RESISTOR



SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

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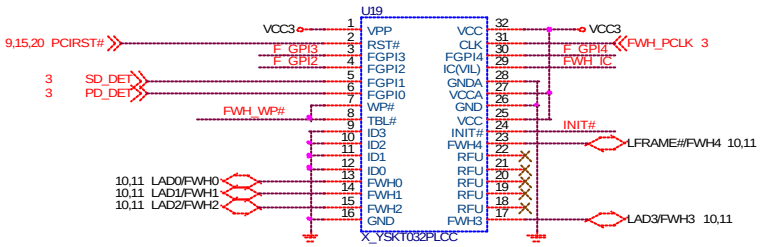
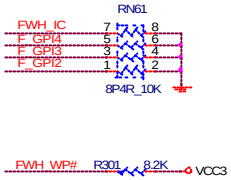
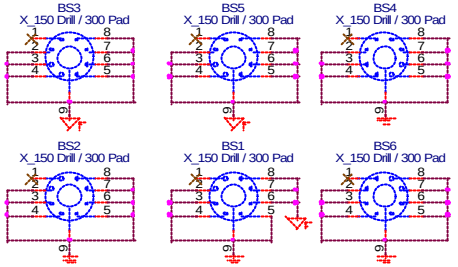
Firware Hub (FWH)



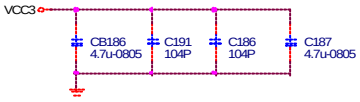
FWH RESISTORS



PCB Mounting Holes

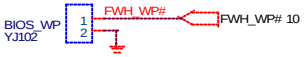


FWH DECOUPLING CAPACITORS



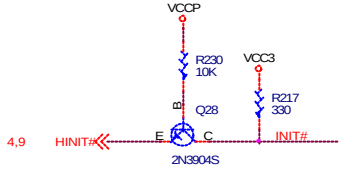
Place Cap. as Close to FWH< 350 mil

FWH write protect

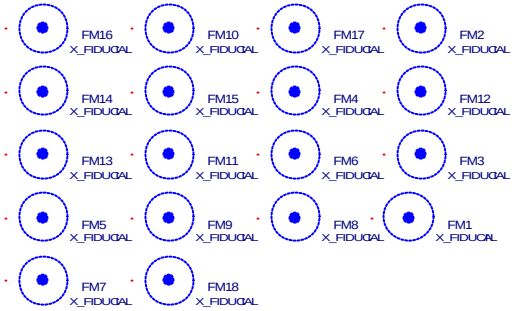


BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block

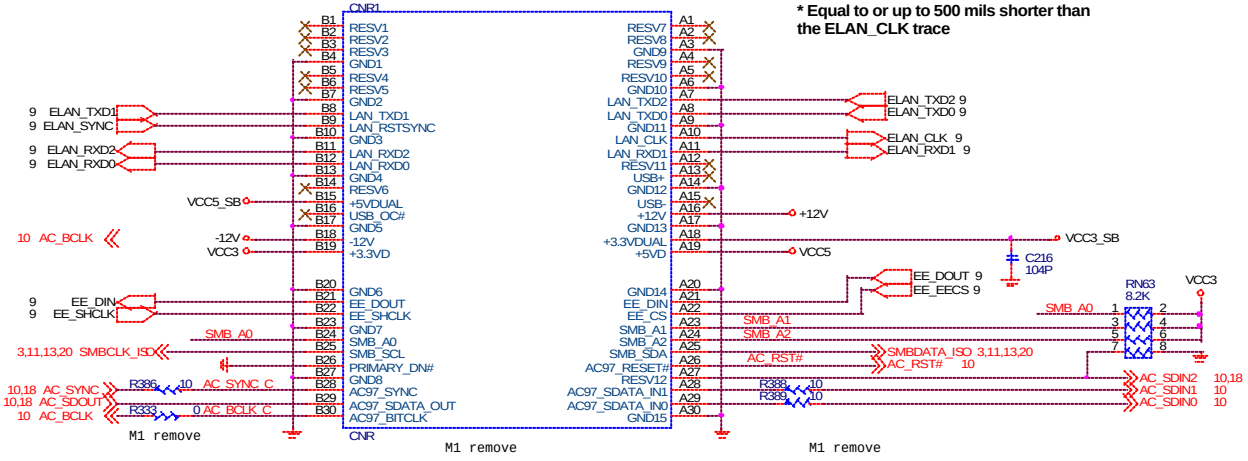


PCB Fiducials



SIMULATION TRACE

CNR RISER



*** LAN Trace width : 5 mils**

*** AC'97 Trace Spacing : 10 mils**

*** Maxium trace length < 9.5"**

*** Equal to or up to 500 mils shorter than the ELAN_CLK trace**

MSI **MICRO-STAR**

Title: FWH

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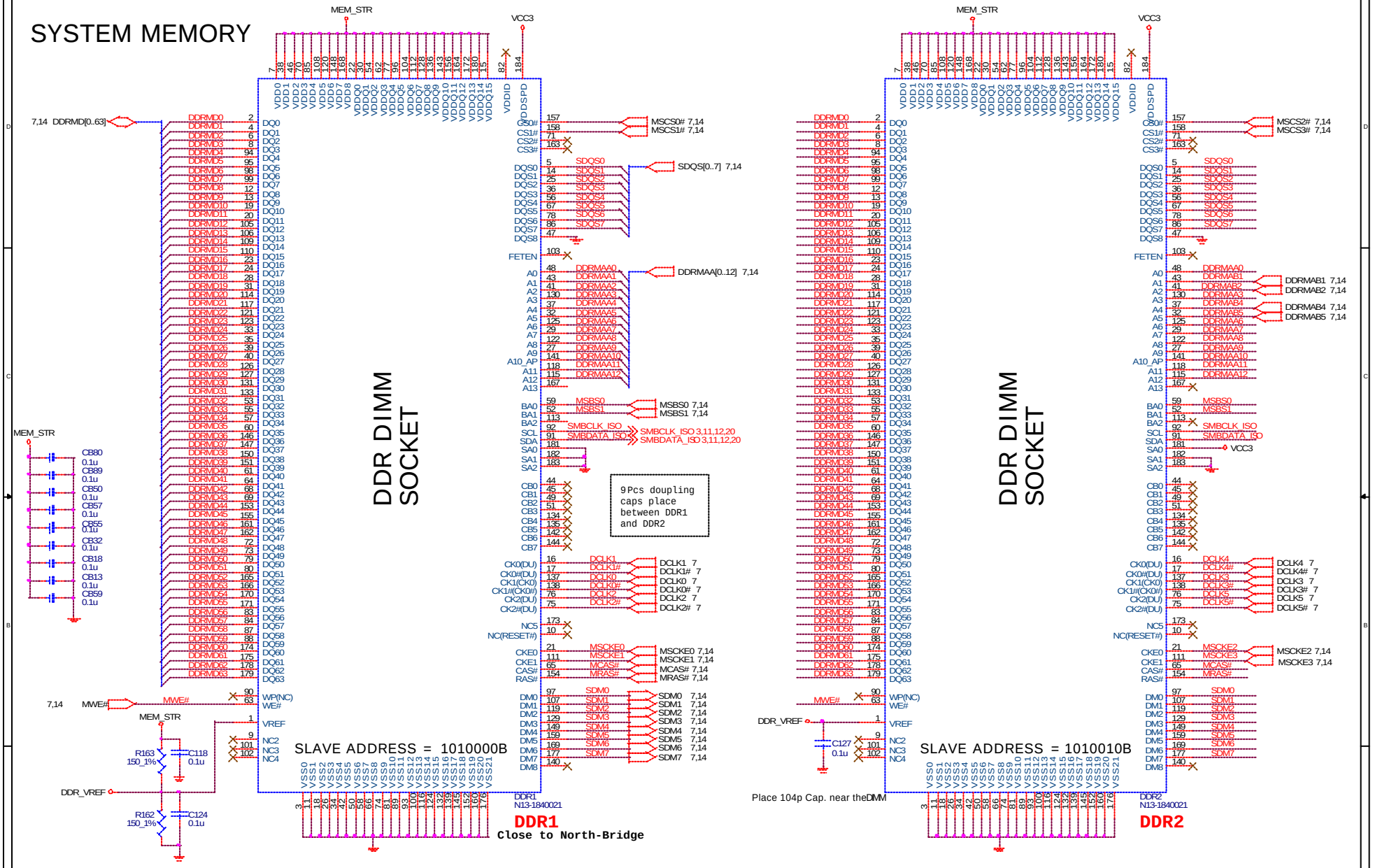
SYSTEM MEMORY



Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near theDIMM

MICRO-STAR

Title	DDR DIMM1 & 2	
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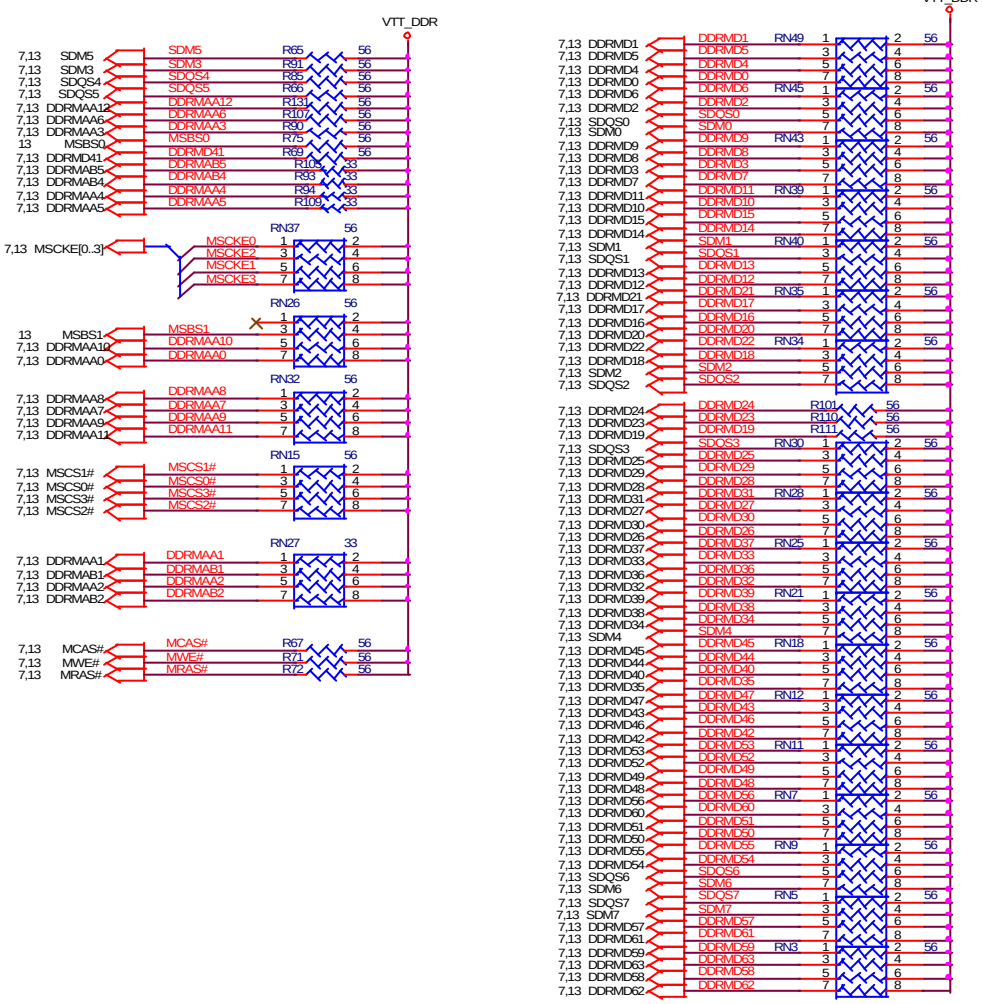
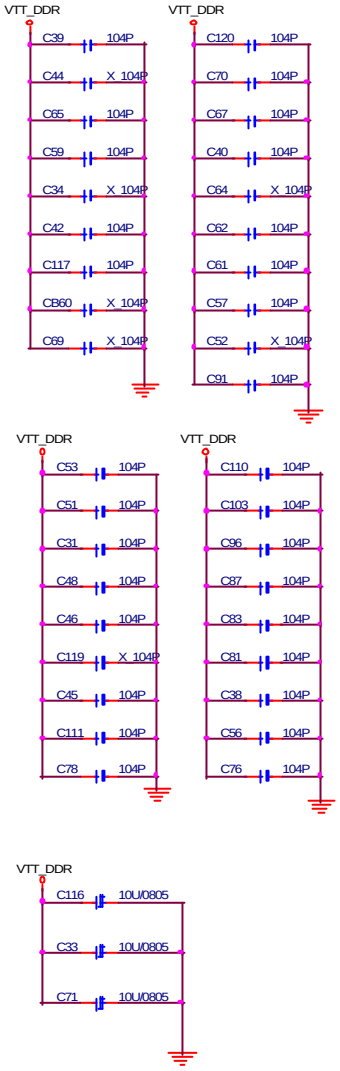
DDR TERMINATORS



TERMINATION DECOUPLING



MICRO-STAR

Title: DDR DAMPING

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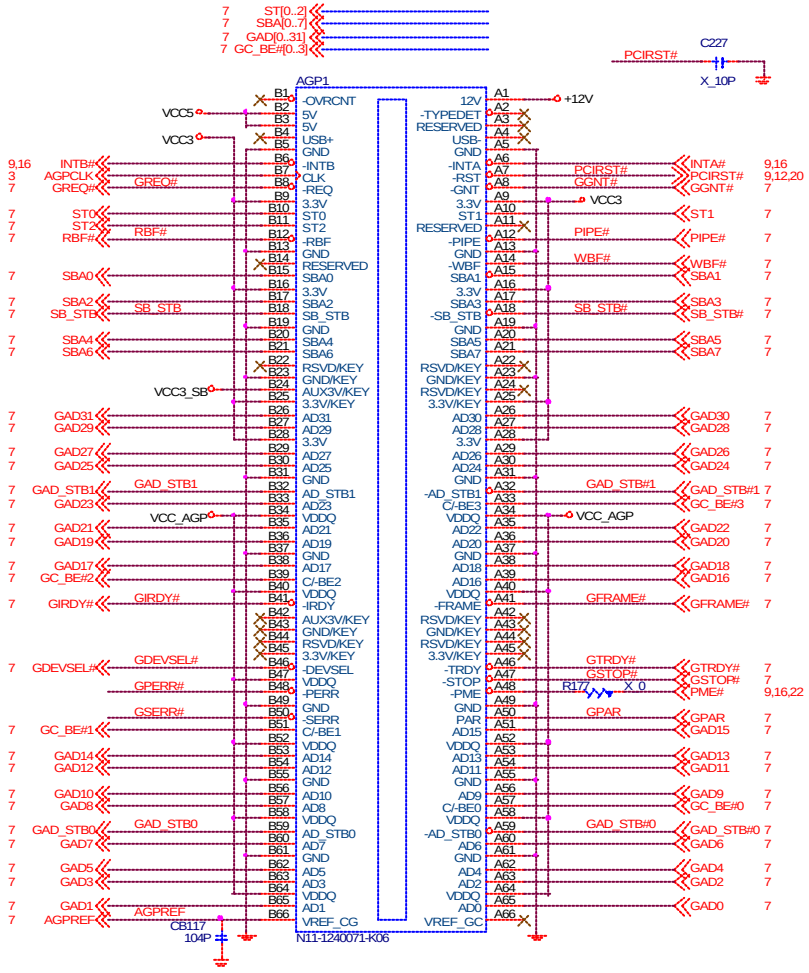
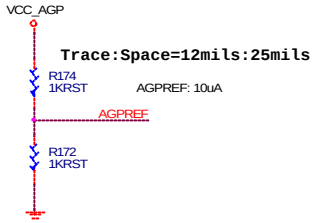
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



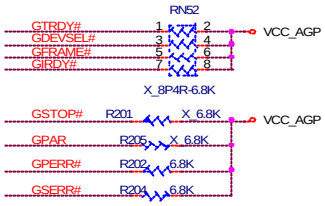
INTA#
INTB#

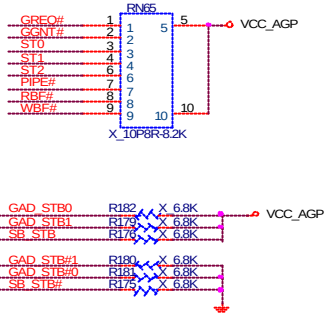
AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

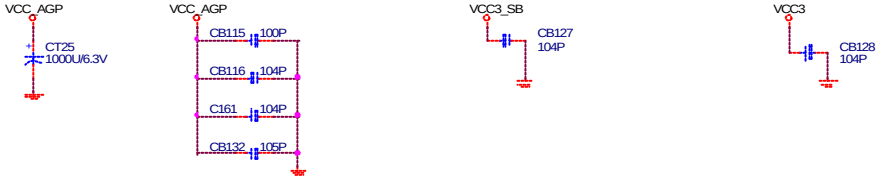
AGP TERMINATION RESISTORS





LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

AGP SLOT DECOUPLING CAPACITORS



MICRO-STAR

Title	AGP SLOT	
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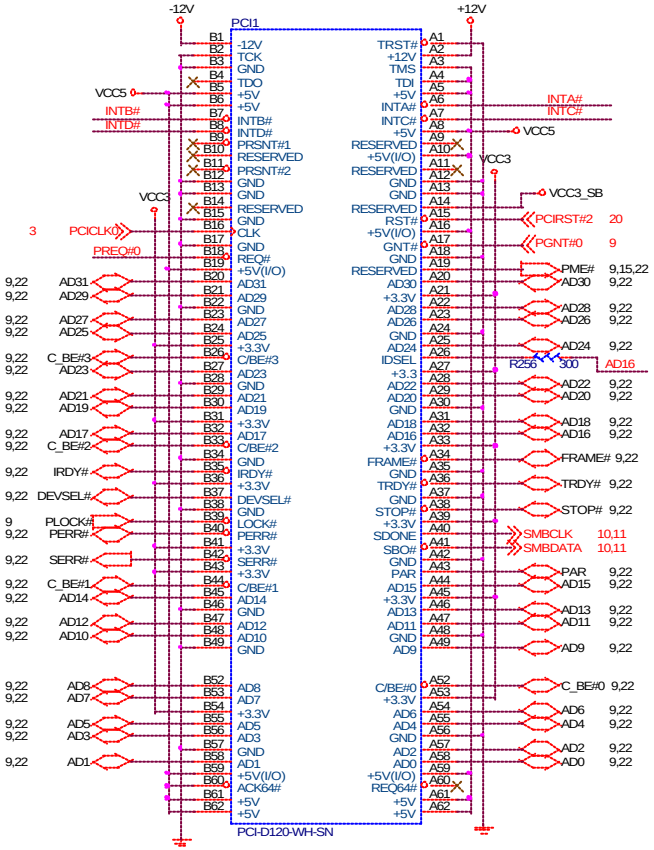
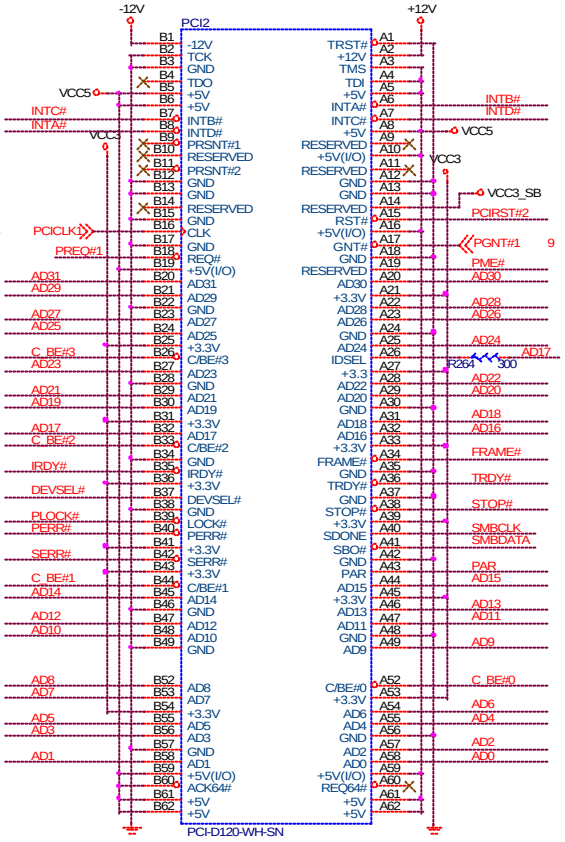
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



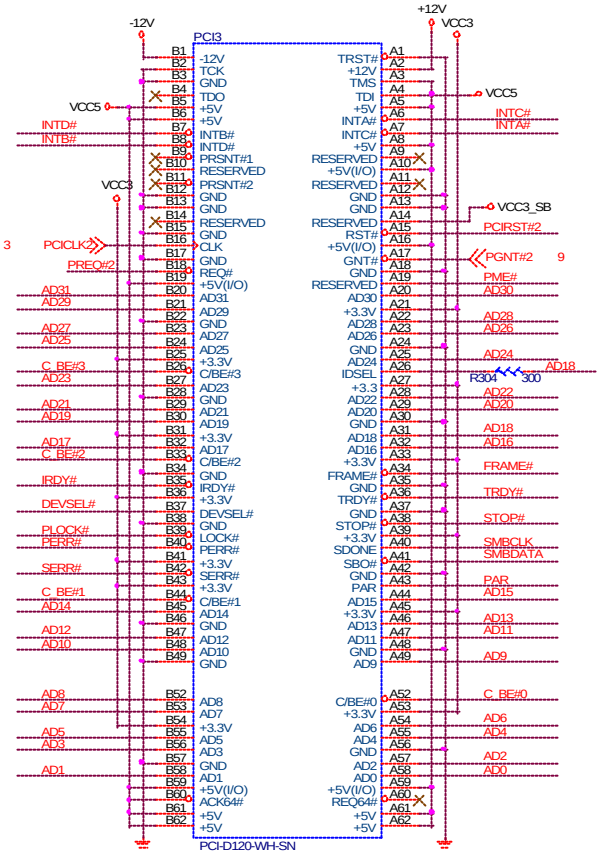
IDSEL = AD25
MASTER = PREQ0
INTF#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD26
MASTER = PREQ1
INTG#

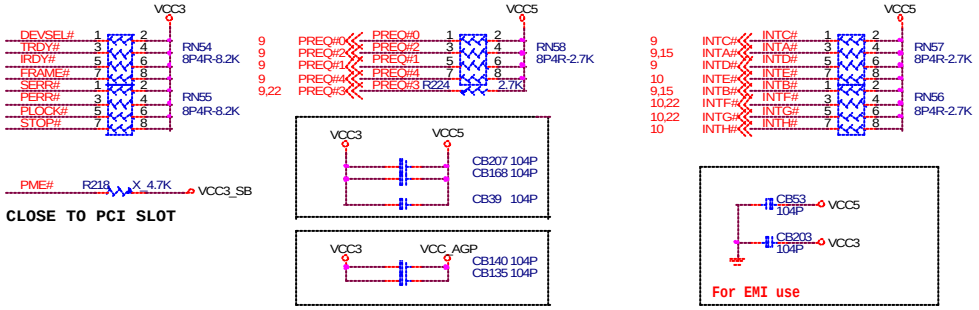
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



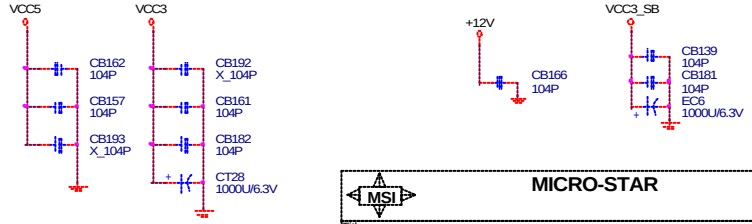
IDSEL = AD27
MASTER = PREQ2
INTD#

IDSEL = AD29
SLAVE = PREQ4
INTB#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MSI **MICRO-STAR**

Title: PCI SLOT 1,2,3

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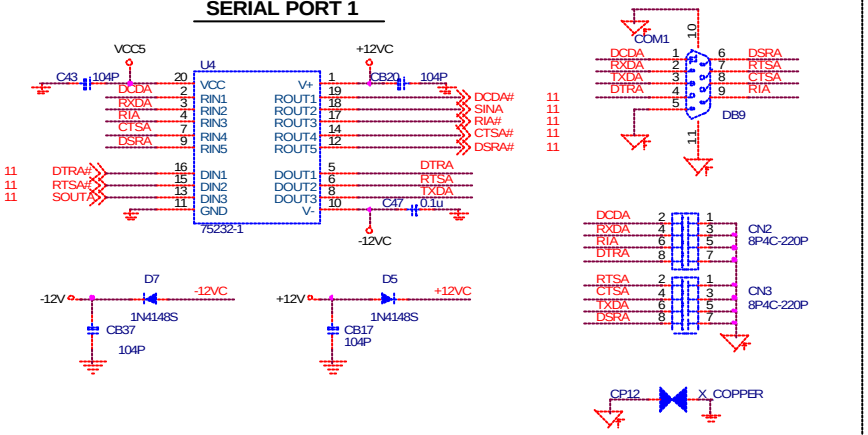
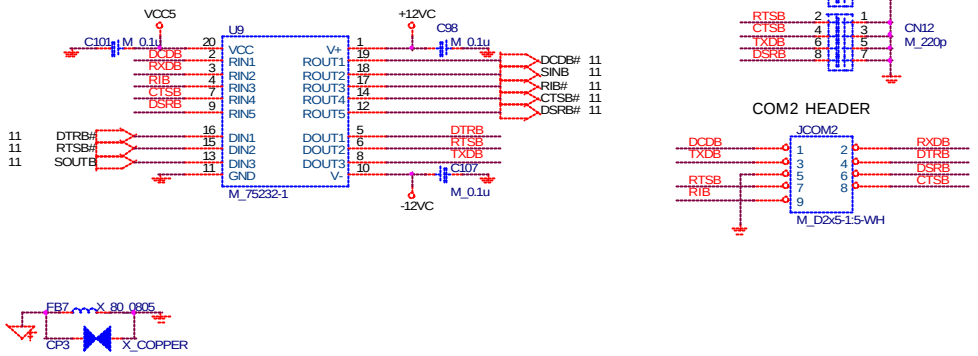
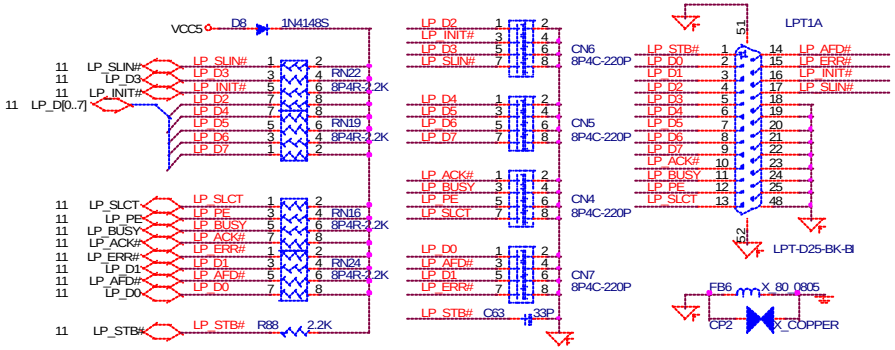
SERIAL PORT 1



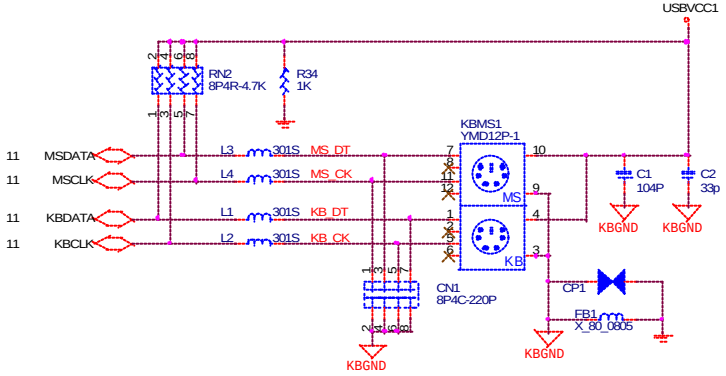
SERIAL PORT 2



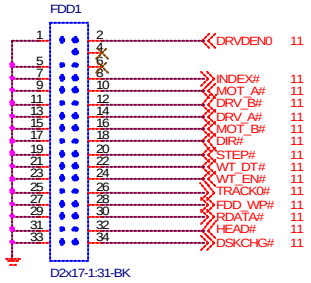
PARALLAL PORT

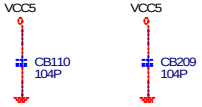


PS2 KEYBOARD & MOUSE CONNECTOR



FLOPPY CONNECTOR





MSI **MICRO-STAR**

Title: I/O CONNECTORS

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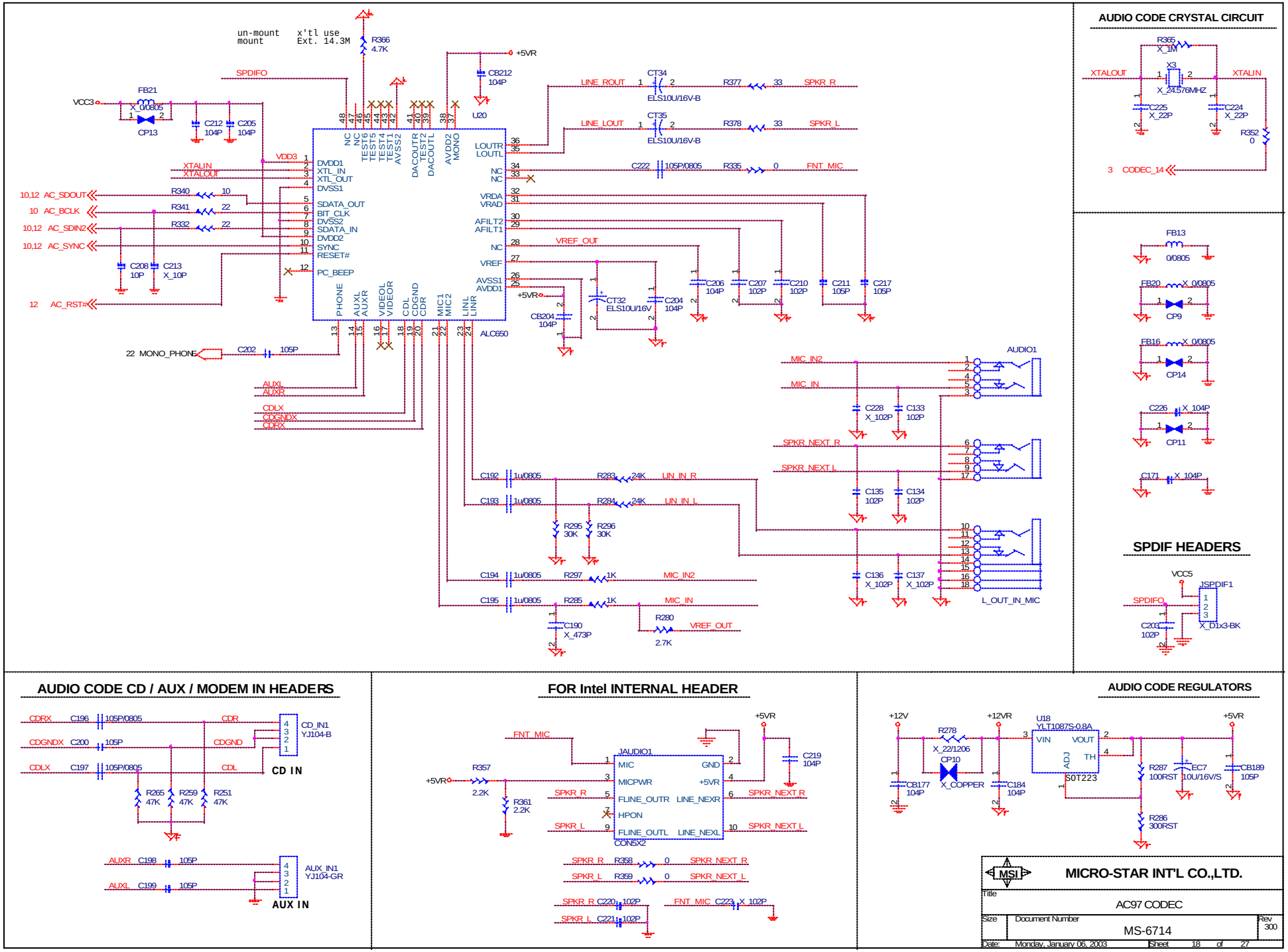

AUDIO CODE CRYSTAL CIRCUIT

SPDIF HEADERS

AUDIO CODE CD / AUX / MODEM IN HEADERS

FOR Intel INTERNAL HEADER

AUDIO CODE REGULATORS

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	AC97 CODEC	
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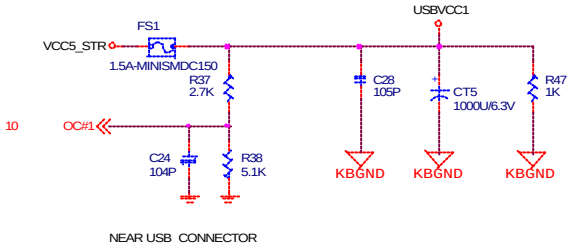
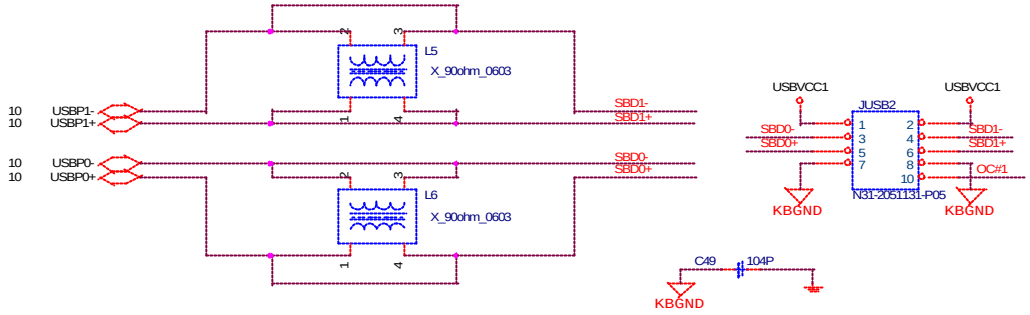
POWER CIRCUIT FOR USB PORT 0,1



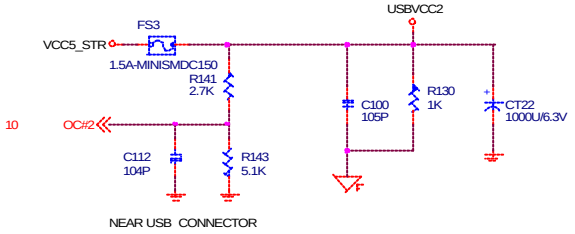
NEAR USB CONNECTOR

REAR PANEL USB CONNECTOR FOR USB PORT 0,1



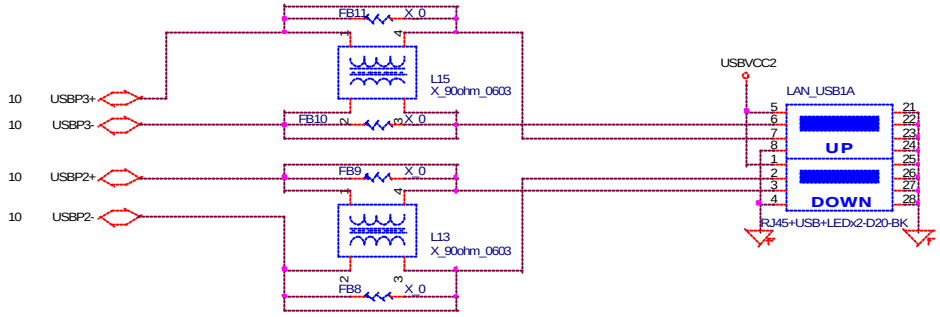
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 2,3



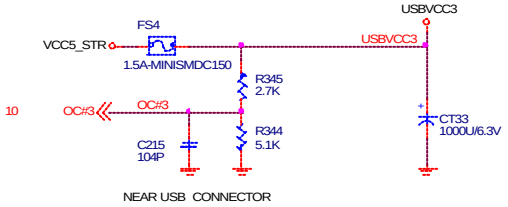
NEAR USB CONNECTOR

REAR PANEL USB CONNECTOR FOR USB PORT 2,3



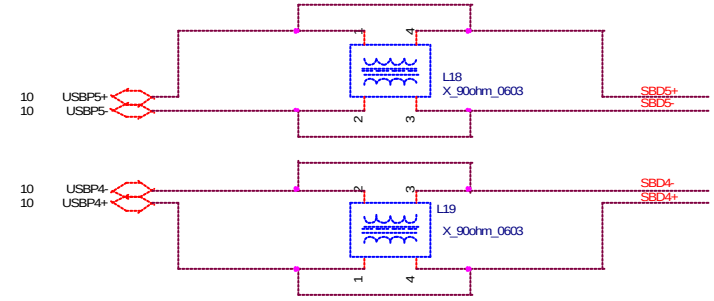
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 4,5



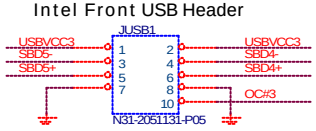
NEAR USB CONNECTOR

FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



NEAR USB CONNECTOR

Intel Front USB Header



*** USB Trace width : 7.5 mils** *** Differential USB Signlas Trace, Spacing : 7.5 mils**

*** USB Trace Spacing : 20 mils** *** USB Power Trace must be 50mils width**

MSI **MICRO-STAR**

Title: USB CONNECTORS

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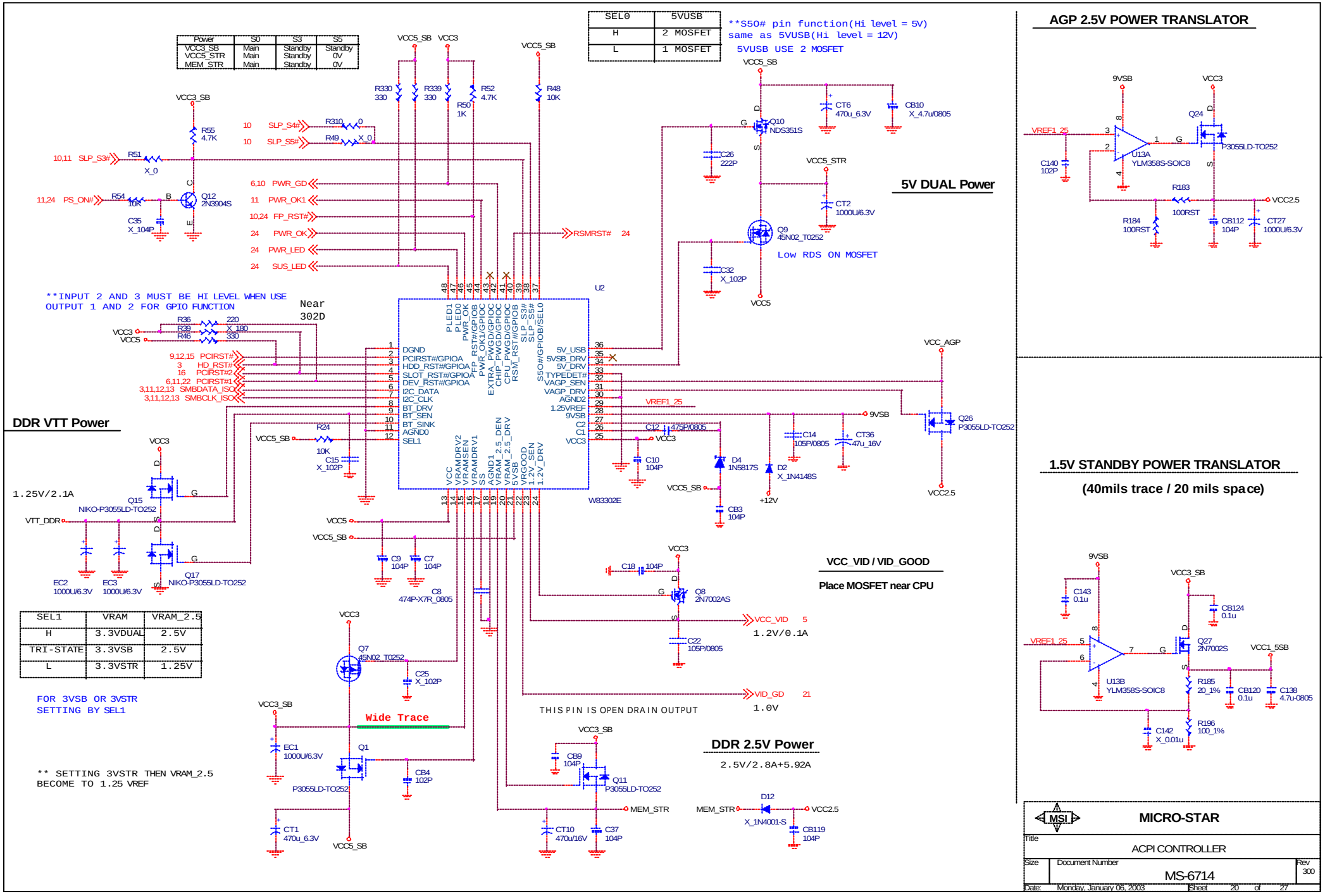
Power | S0 | S3 | S5
VCC3_SB | Main | Standby | Standby
VCC5_STR | Main | Standby | 0V
MEM_STR | Main | Standby | 0V
SEL0 | 5VUSB
H | 2 MOSFET
L | 1 MOSFET
**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET
5V DUAL Power
Low RDS ON MOSFET
**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION
Near 302D
W83302E
DDR VTT Power
1.25V/2.1A
VTT_DDR
NIKO-P3055LD-TO252
VCC_VID / VID_GOOD
Place MOSFET near CPU
1.2V/0.1A
VID_GD
1.0V
THIS PIN IS OPEN DRAIN OUTPUT
SEL1 | VRAM | VRAM_2.5
H | 3.3VDUAL | 2.5V
TRI-STATE | 3.3VSB | 2.5V
L | 3.3VSTR | 1.25V
FOR 3VSB OR 3VSTR
SETTING BY SEL1
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF
Wide Trace
DDR 2.5V Power
2.5V/2.8A+5.92A
AGP 2.5V POWER TRANSLATOR
1.5V STANDBY POWER TRANSLATOR
(40mils trace / 20 mils space)
MSI
MICRO-STAR
Title
ACPI CONTROLLER
Size
Document Number
MS-6714
Rev
300
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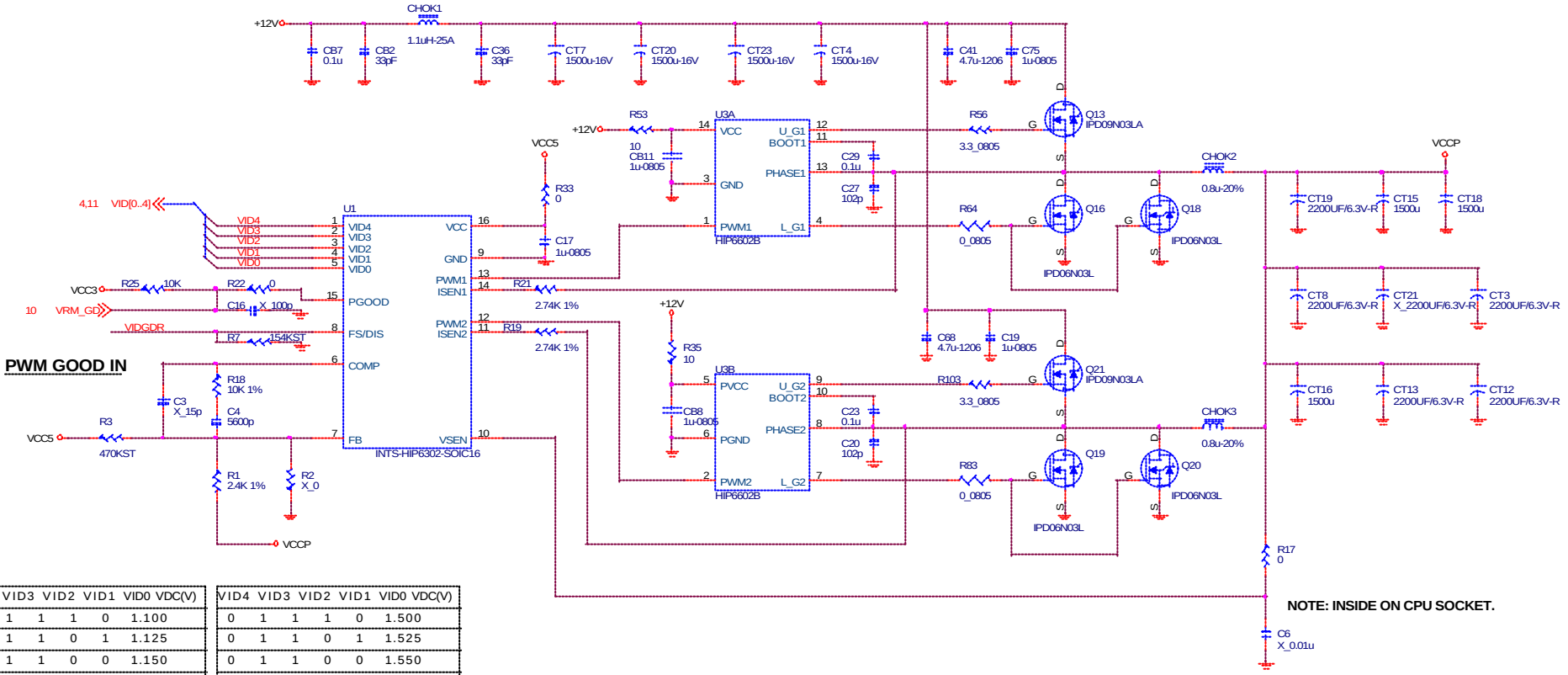
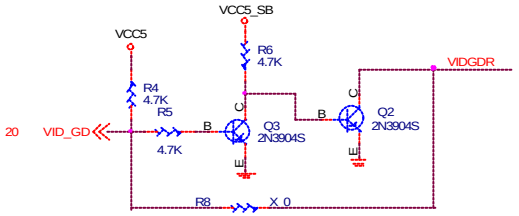
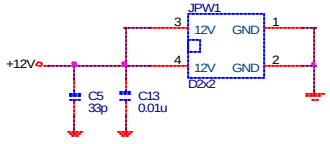


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

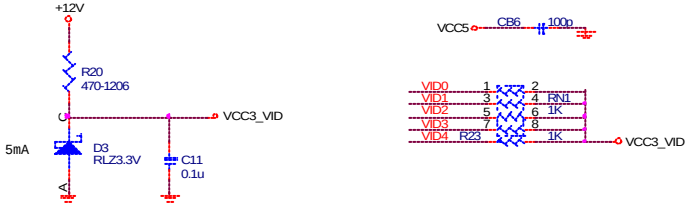
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF



ATX12V POWER CONNECTOR



VID PULL-UP RESISTORS



MSI MICRO-STAR INT'L CO.,LTD.

Title: VRM 9.0

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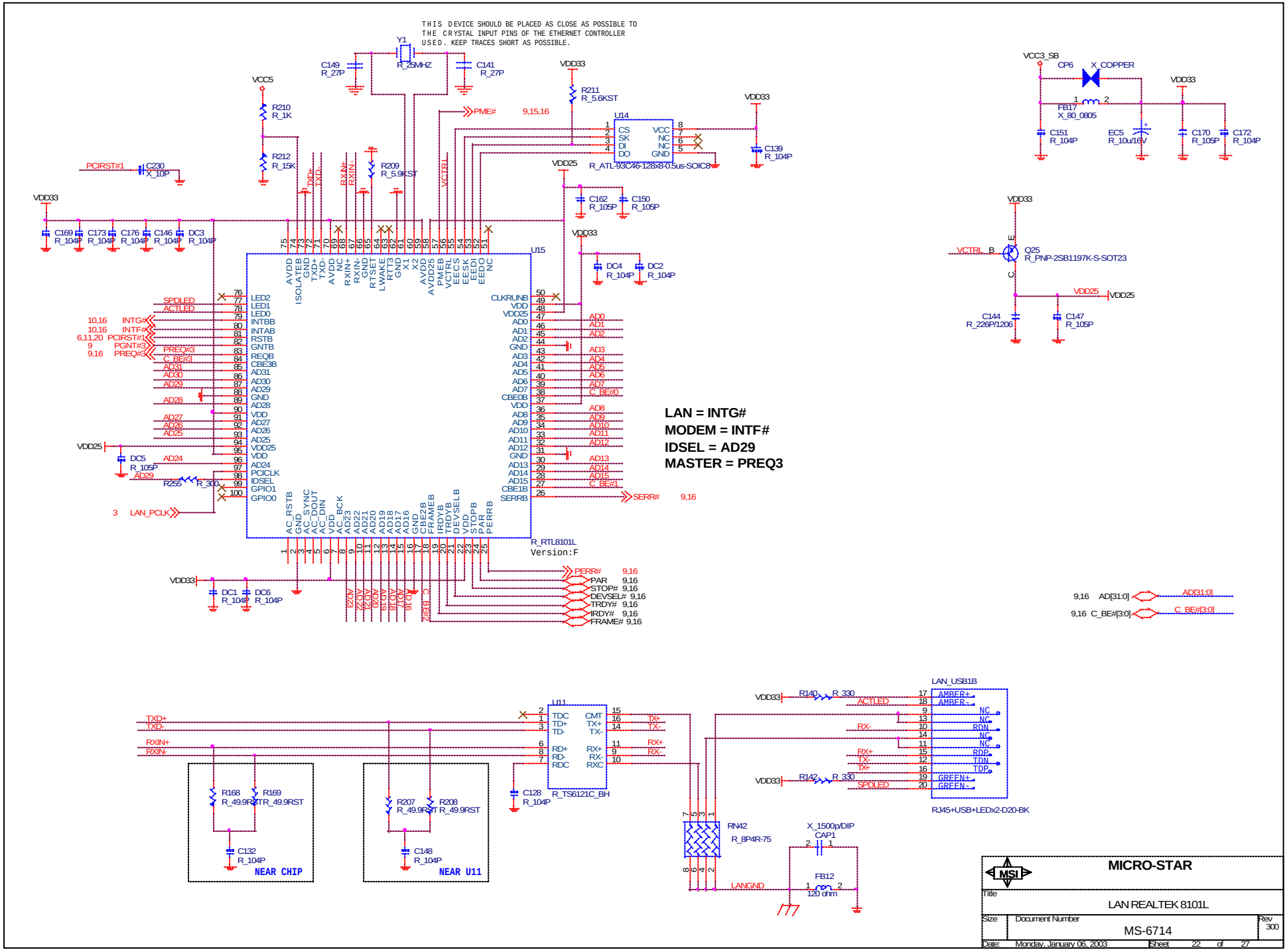
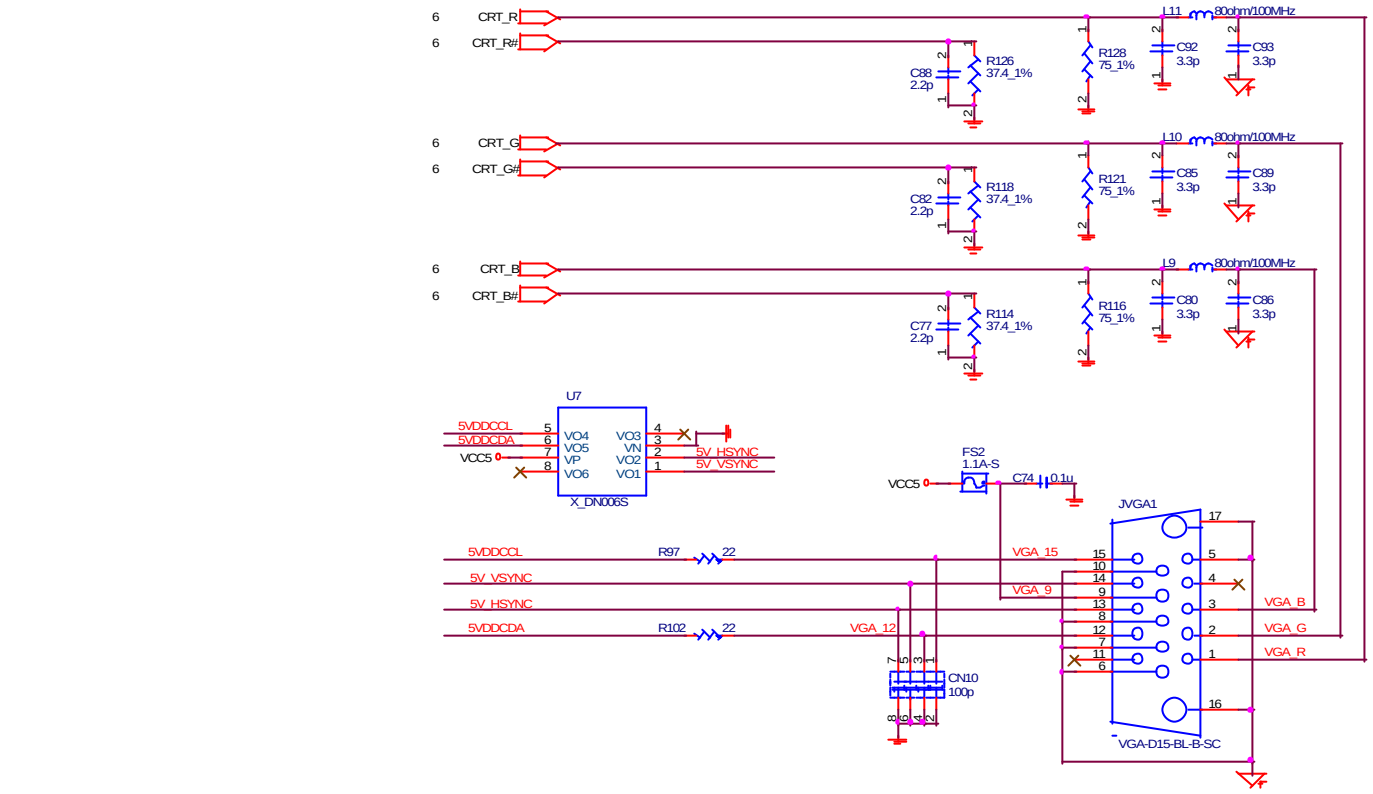
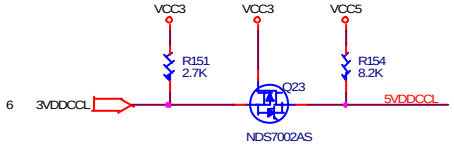
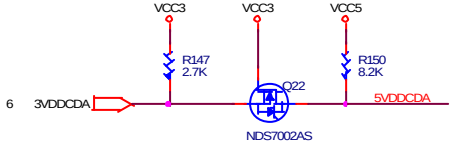
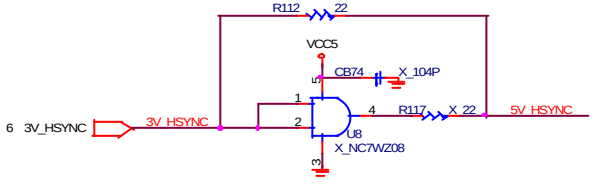

THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.
LAN = INTG#
MODEM = INTF#
IDSEL = AD29
MASTER = PREQ3
NEAR CHIP
NEAR U11
MICRO-STAR
LAN REALTEK 8101L
MS-6714
Monday, January 06, 2003

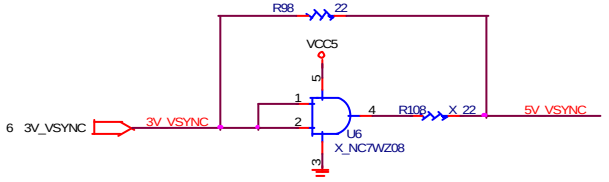
Video Connector











MSI	MICRO-STAR	
Title	VGA CONNECTOR	
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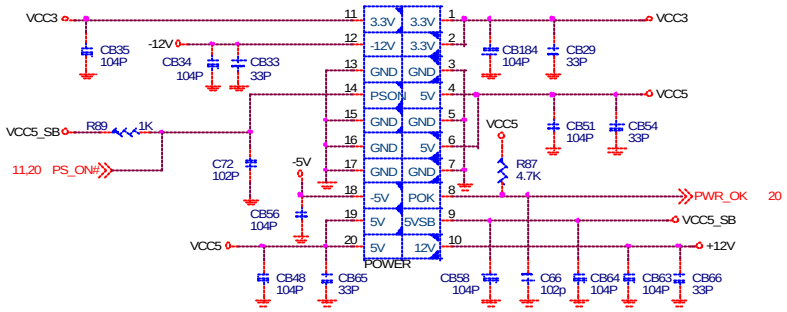
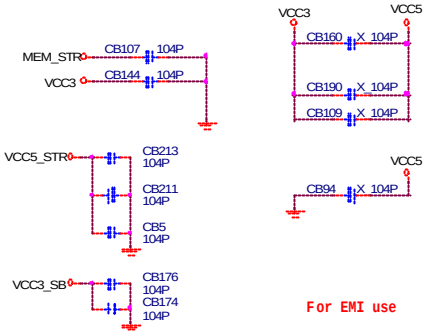
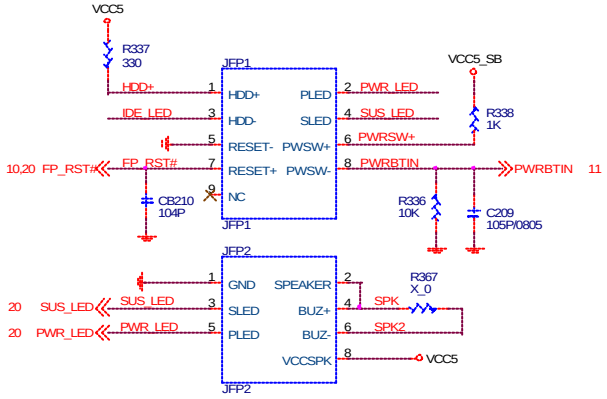
ATX CONNECTOR



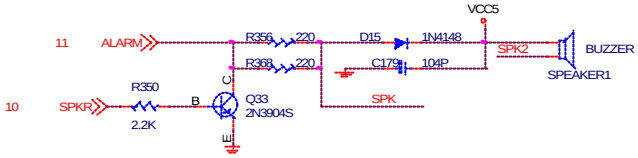
REGULATORS OUTPUT DECOUPLING CAPACITORS



Intel Front Panel

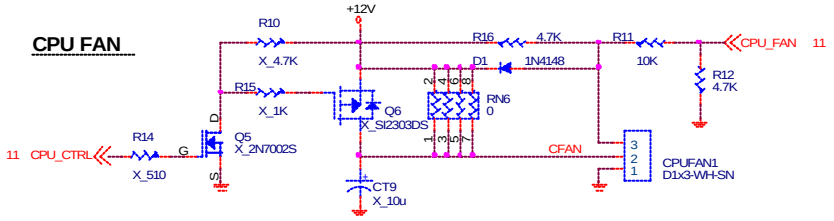


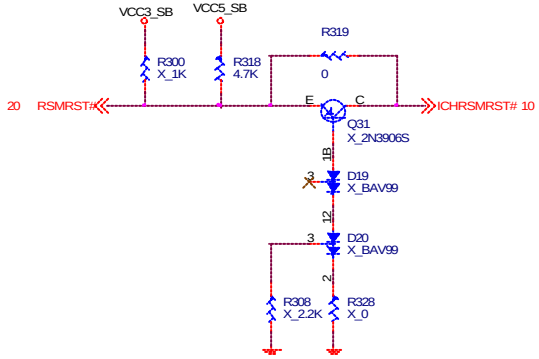
BUZZER



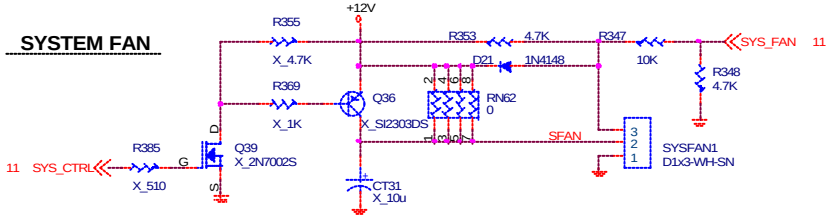
IDE LED

CPU FAN





SYSTEM FAN



MSI **MICRO-STAR**

Title: Front Panel & ATX Connector & FAN

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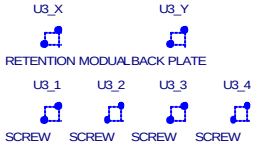
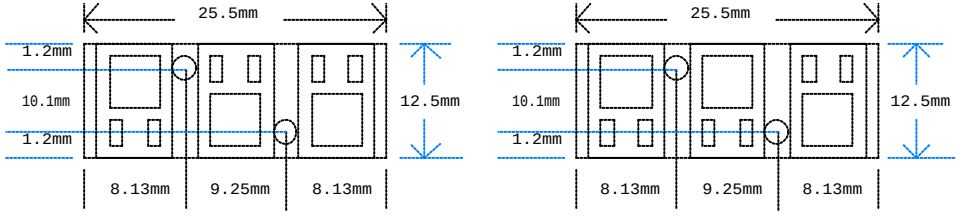
Jumper Setting & Connector Setting

STD	U10_A B01-845GE15-I06 **845GE B1**	U17_A B01-801DB55-I06 **ICH4 B0**	LAN_USB1_A USB X 2 - 8pin	Q16_A, Q18_A, Q19_A, Q20_A IPD06N03L	U10_A1 E31-0400741-K08	U19_A1 FLASH 4M	R1_A 2.4K 1% R3_A 470KST R19_A 2.74K 1% R21_A 2.74K 1%	LABEL1_A G51-LA00830 **845GE**
LAN			LAN_USB1_B USB X2 +RJ45					
GV	U10_B B01-845GV05-I06 **845GV A1**	U17_B B01-801DB15-I06 **ICH4 A1**				U19_B1 FLASH 2M		LABEL1_B G51-LA00828 **845GV**
G	U10_C B01-0845GC65-I06 **845G B1**	U17_C B01-801DB55-I06 **ICH4 B0**						LABEL1_C G51-LA00829 **845G(B)**
GL	U10_D B01-845GL15-I06 **845GL B1**	U17_D B01-801DB55-I06 **ICH4 B0**		Q16_B, Q18_B, Q19_B, Q20_B IPD09N03LA	U10_B1 E31-0400440-A02		R1_B 2.61K 1% R3_B 422KST R19_B 4.75K 1% R21_B 4.75K 1%	LABEL1_D G51-LA00831 **845GL**





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Title: JUMPER SETTING & MANUAL PARTS

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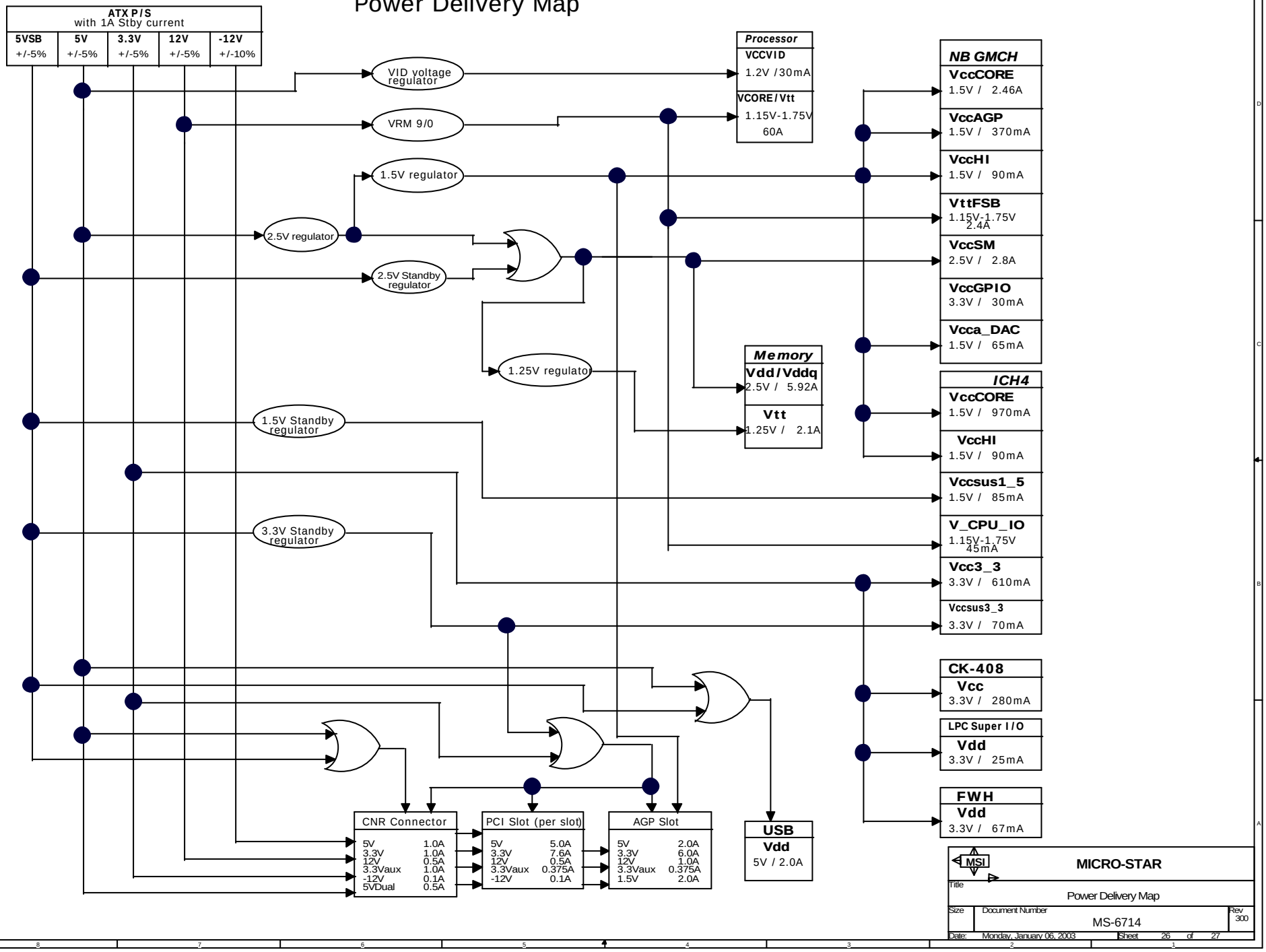
Power Delivery Map



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Title: Power Delivery Map

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General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntion pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifuntion pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

** GPIO18 will toggle at 1Hz frequency.*

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2	12 (PCI5)
PCI LAN	INTG# INTF#	AD29	LAN_PCLK	17 (PCI9)

**ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.*

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

MSI MICRO-STAR

Title: General SPEC

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