MS-6710

Version 10B
07/10/2003 Update

INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-GE Chipset:

INTEL MCH (North Bridge) +
INTEL ICH4 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generator -- CY283490C

PCI SOUND -- C-MEDIA CMI8738MX

PCI 1394 -- VIA 6386

PCI LAN -- RealTek 8100BL

Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 1

ERP BOM	Function Description	
501/601-6710-030	Opt :IL	W/1394, W/LAN
501/601-6710-060	Opt :I	W/1394, Wo/LAN
501/601-6710-040	Opt :L	Wo/1394, W/LAN
501/601-6710-050	Opt :LV	GV/Wo/1394, W/LAN

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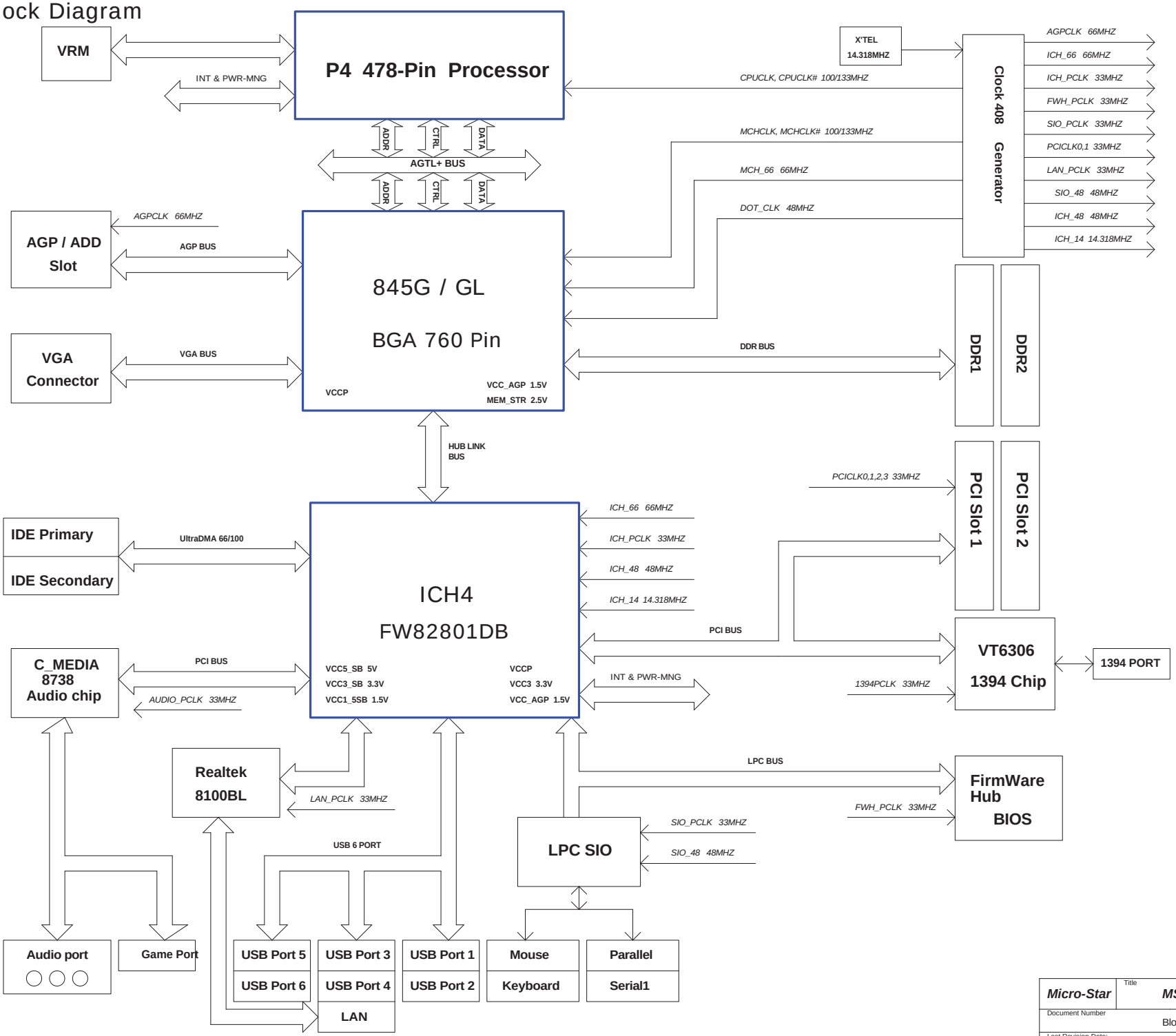
Block Diagram



Micro-Star	Title: MS-6710	Rev: 10B
Document Number: Block Diagram		
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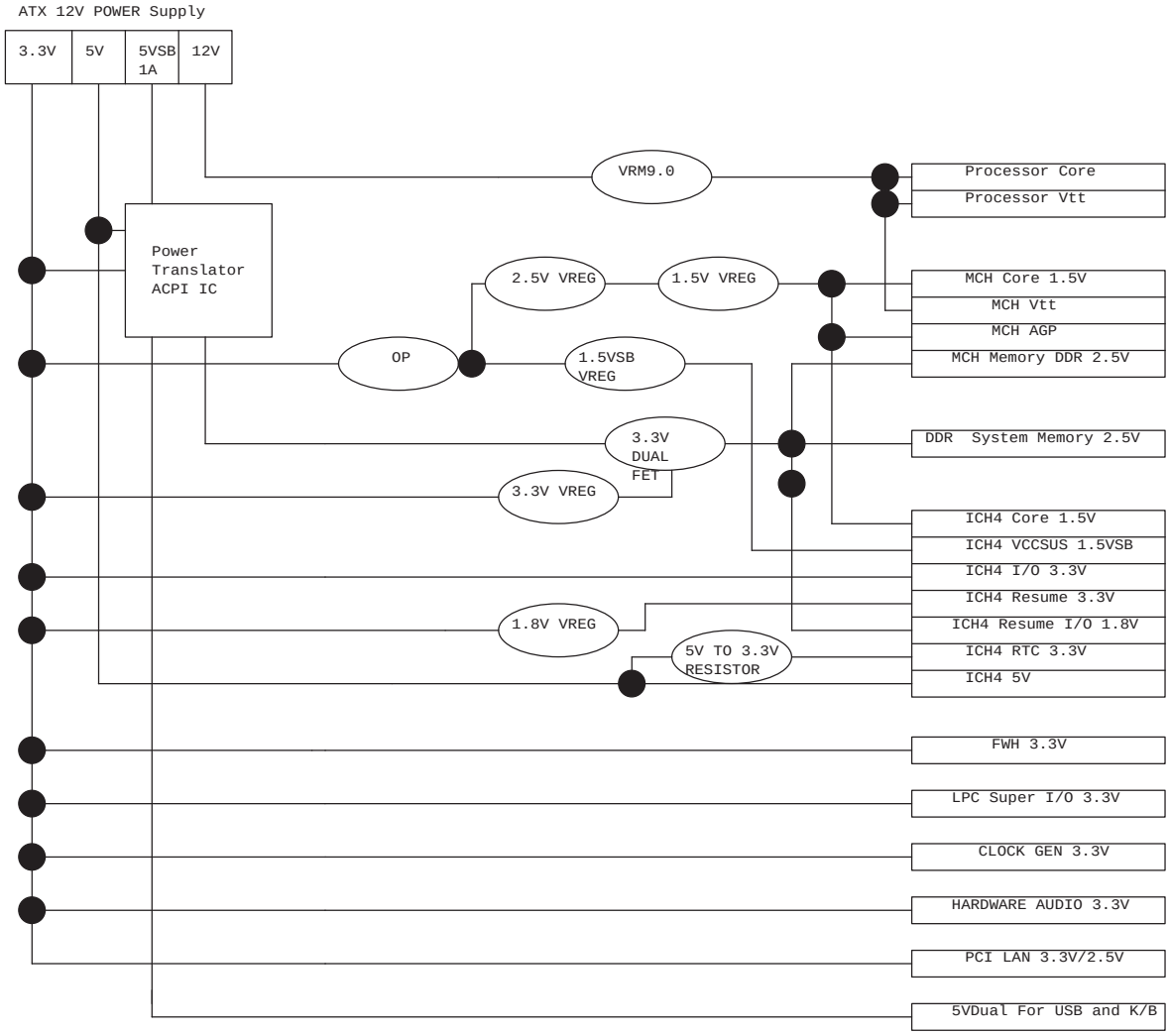
Power Delivery Map



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH4	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY283490C	0	0	0	0	0	0	0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0		0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 2 = 4.0A ---> V_DIMM
S1/S3 STATE --- 200mA * 2 = 400mA ---> V_DIMM
V_DIMM -->400mA*2.5V/3.3V=303mA --> VCC3_SB

NOTE3 --- ICH4

Power	S0	S1	S3/S4/S5
1.8V	132mA	99mA	N/A
VCC_AGP	550mA	266mA	N/A
VCC1_5SB	82mA	52mA	25mA
VCC3(I/O)	528mA	0.76mA	N/A
VCC3_SB	167mA	1mA	0.8mA / N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

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General Purpose I/O Spec.

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A
GPIO 1	I	REQ#5
GPIO 2	I	IRQE#
GPIO 3	I	IRQF#
GPIO 4	I	IRQG#
GPIO 5	I	IRQH#
GPIO 6~7	I	Not Implemented
GPIO 8	I	SIO_PME#
GPIO 9~10	I	Not Implemented
GPIO 11	I	External SMI
GPIO 12~13	I	Not Implemented
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	GNT#5
GPIO 18~21	O	Non Connect
GPIO 22	O/D	Non Connect
GPIO 23	O	BIOS Protect
GPIO 24~27	I/O	Non Connect
GPIO 28	I/O	LAN DISABLED(ICH4)
GPIO 29~47	I/O	Non Connect

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL	CLOCK
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1
PCI LAN	INTC#	AD26	LANPCLK
PCI AUDIO	INTF#	AD25	AUDPCLK
PCI 1394	INTH#	AD23	1394PCLK

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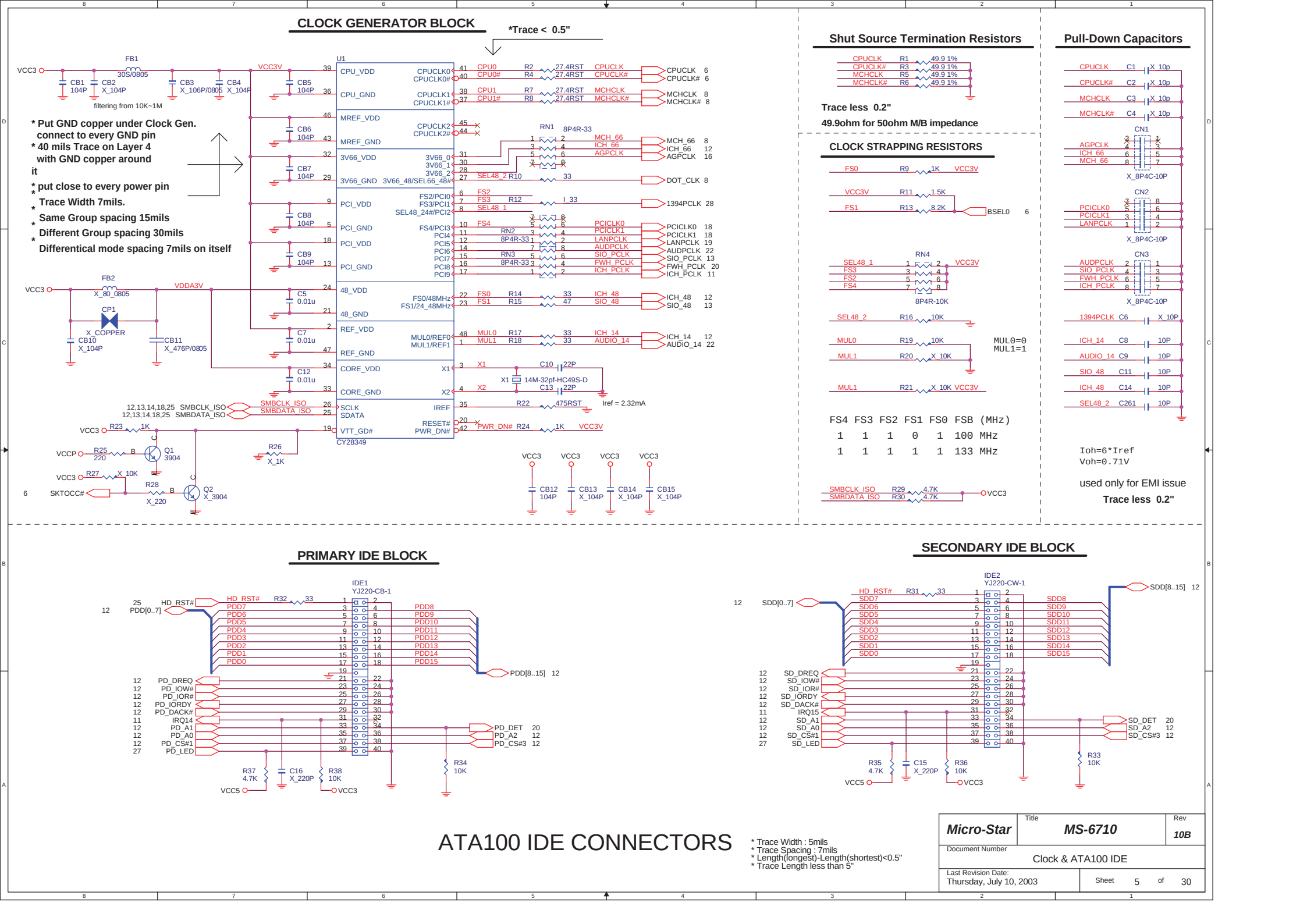
CLOCK GENERATOR BLOCK
*Trace < 0.5"
U1
CY28349
* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differentical mode spacing 7mils on itself
Shut Source Termination Resistors
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
FS4 FS3 FS2 FS1 FS0 FSB (MHz)
1 1 1 0 1 100 MHz
1 1 1 1 1 133 MHz
MUL0=0
MUL1=1
Pull-Down Capacitors
Ioh=6*Iref
Voh=0.71V
used only for EMI issue
Trace less 0.2"
PRIMARY IDE BLOCK
IDE1
YJ220-CB-1
SECONDARY IDE BLOCK
IDE2
YJ220-CW-1
ATA100 IDE CONNECTORS
* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than 5"
Micro-Star
Title
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Document Number
Clock & ATA100 IDE
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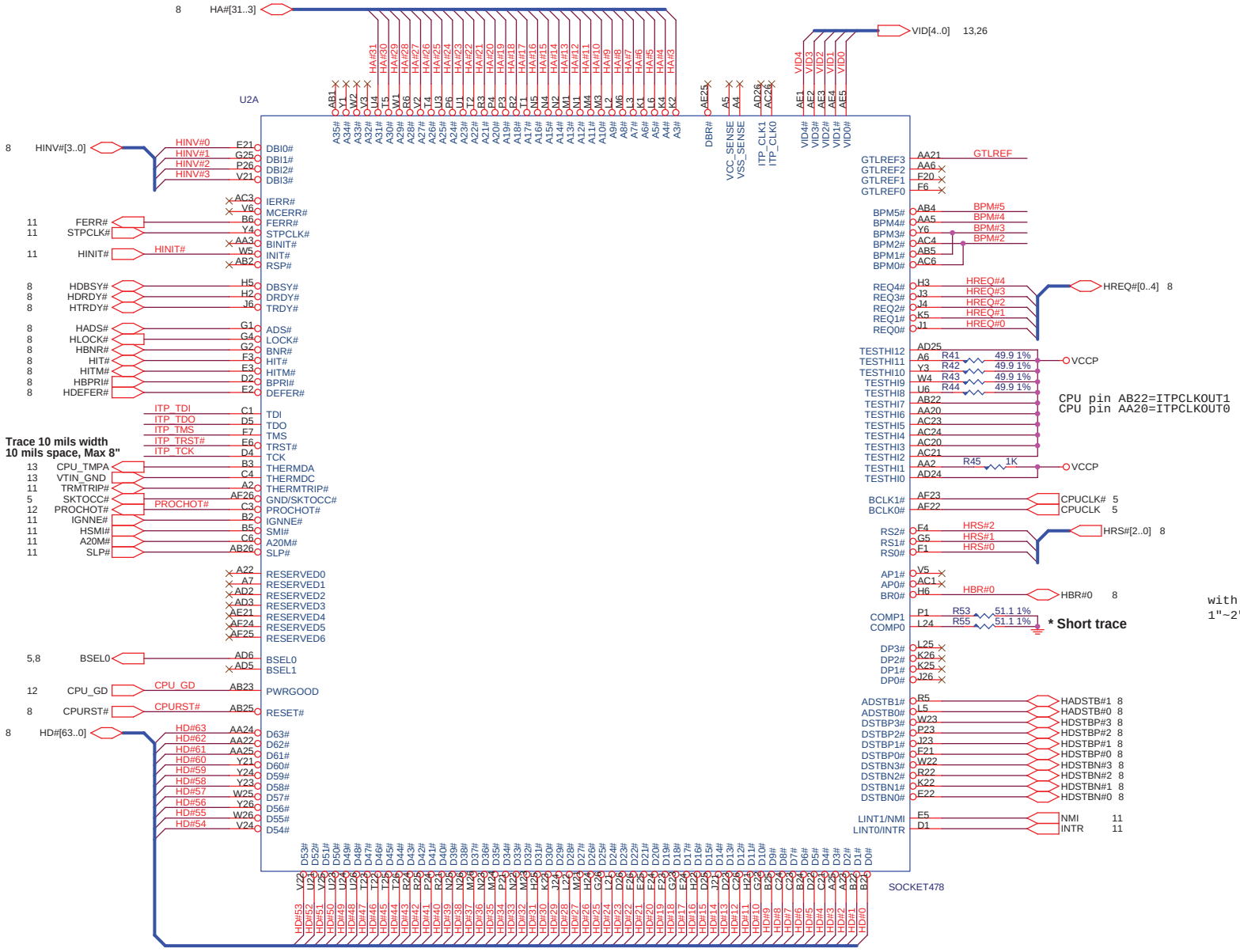
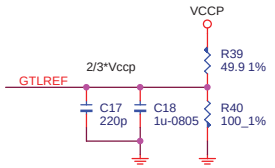
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK

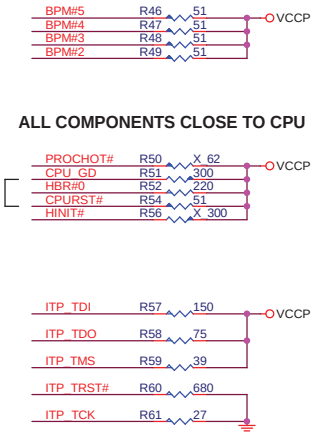


Every pin put one 220pF cap near it.

Trace Width 7mils, Space 10mils.

Keep the voltage divider within 1.5" of the GETREF pin.

CPU STRAPPING RESISTORS



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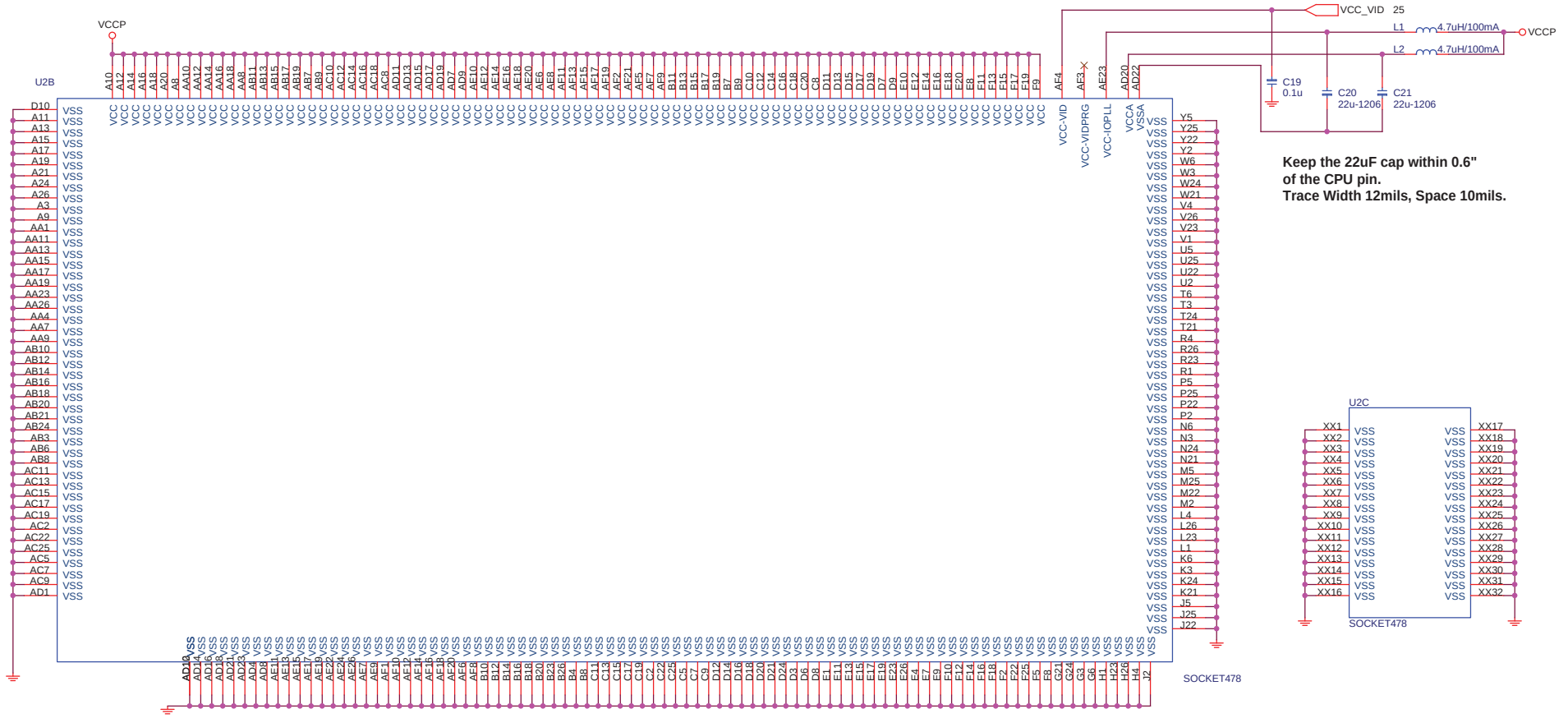
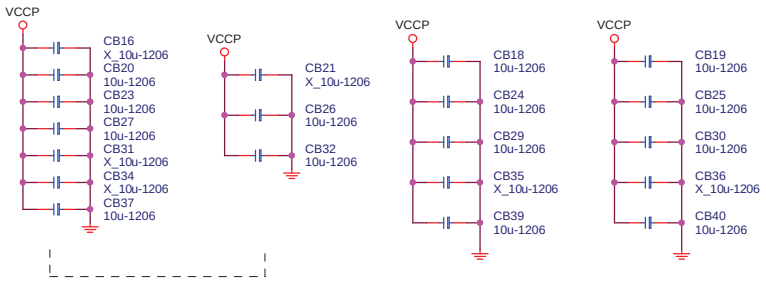
CPU VOLTAGE BLOCK



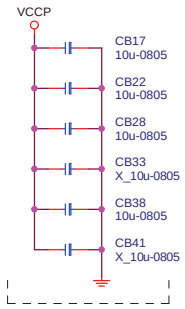
Keep the 22uF cap within 0.6" of the CPU pin.
Trace Width 12mils, Space 10mils.

CPU DECOUPLING CAPACITORS



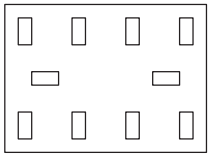
Place 14 pcs 1206 size cap north side of processor

PLACE CAPS WITHIN CPU CAVITY



Place these caps on south side of processor

Within CPU Cavity Solder Side



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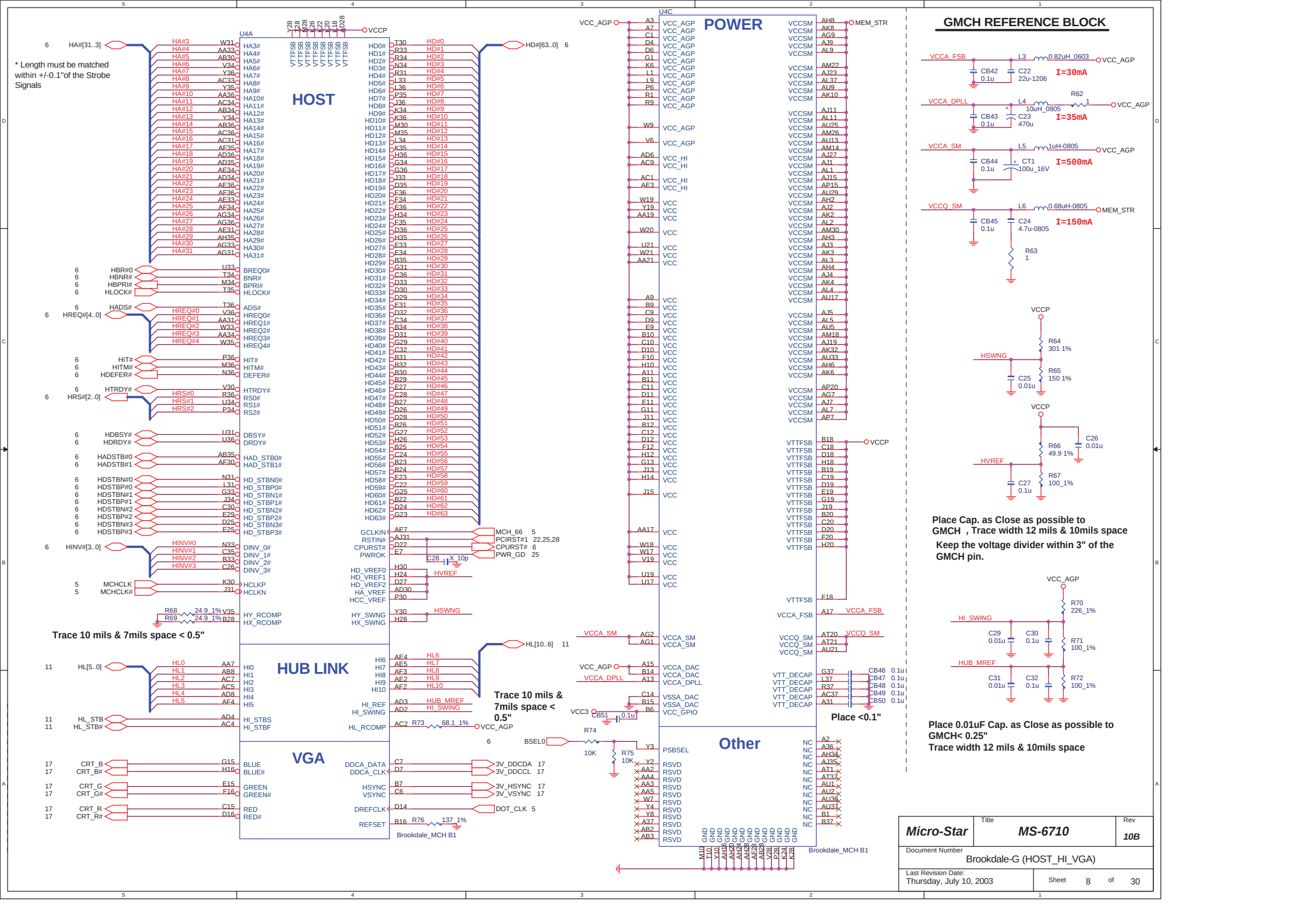
HOST
HUB LINK
VGA
POWER
Other
U4A
U4C
* Length must be matched within +/-0.1"of the Strobe Signals
Trace 10 mils & 7mils space < 0.5"
Trace 10 mils & 7mils space < 0.5"
Place <0.1"
Brookdale_MCH B1
GMCH REFERENCE BLOCK
VCCA_FSB
L3 0.82uH_0603
VCC_AGP
I=30mA
VCCA_DPLL
L4 10uH_0805
R62 1
I=35mA
VCCA_SM
L5 1uH-0805
I=500mA
VCCQ_SM
L6 0.68uH-0805
MEM_STR
I=150mA
R63 1
VCCP
R64 301 1%
HSWNG
R65 150 1%
C25 0.01u
R66 49.9 1%
HVREF
R67 100_1%
C27 0.1u
Place Cap. as Close as possible to GMCH , Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the GMCH pin.
R70 226_1%
HI_SWING
R71 100_1%
HUB_MREF
R72 100_1%
Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space
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Brookdale-G (HOST_HI_VGA)
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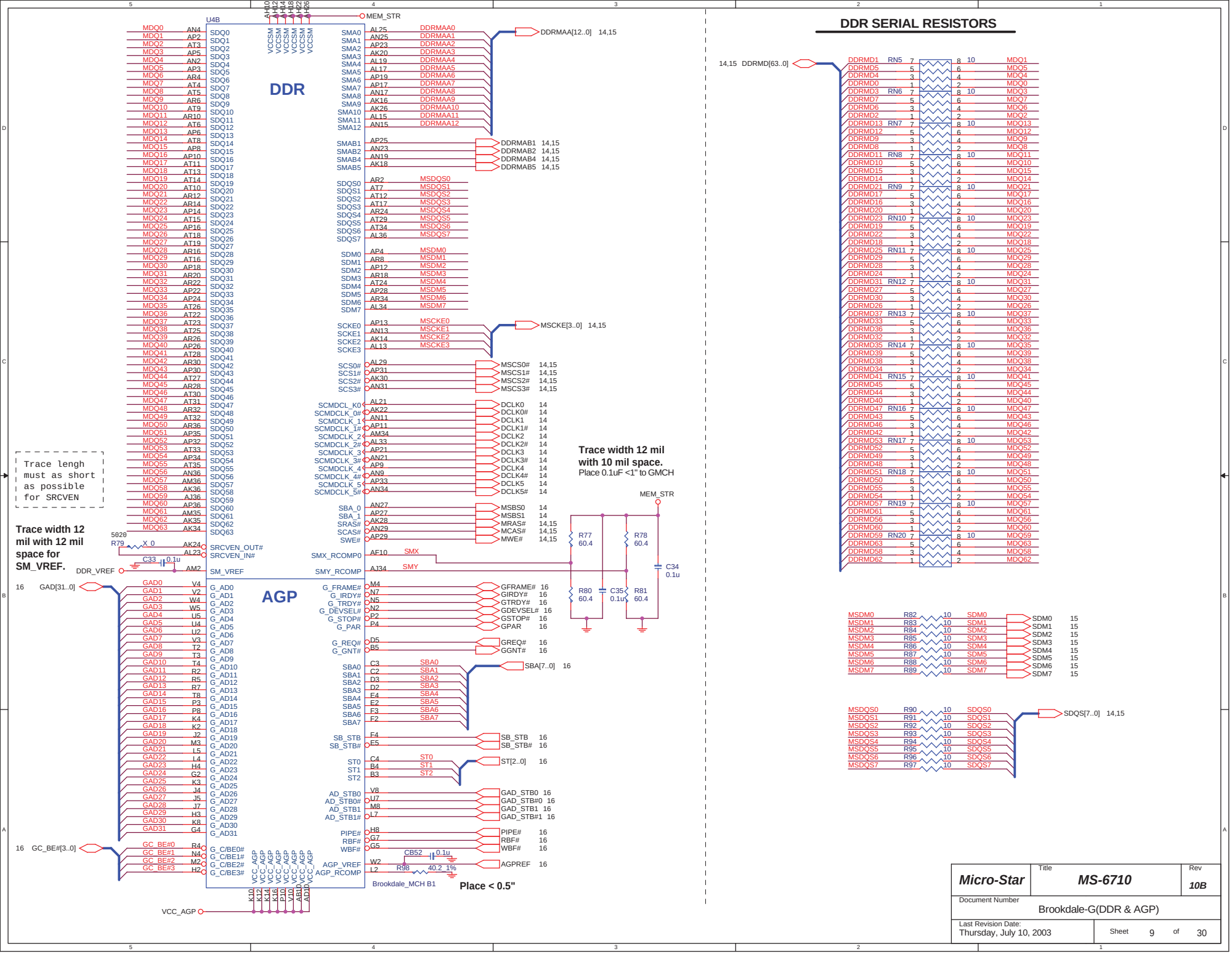
DDR
AGP
U4B
MEM_STR
DDR SERIAL RESISTORS
Trace lengh must as short as possible for SRCVEN
Trace width 12 mil with 12 mil space for SM_VREF.
Trace width 12 mil with 10 mil space.
Place 0.1uF <1" to GMCH
Place < 0.5"
Brookdale_MCH B1
DDRMAA[12..0] 14,15
DDRMAB1 14,15
DDRMAB2 14,15
DDRMAB4 14,15
DDRMAB5 14,15
MSCKE[3..0] 14,15
MSCS0# 14,15
MSCS1# 14,15
MSCS2# 14,15
MSCS3# 14,15
SBA[7..0] 16
ST[2..0] 16
SDQS[7..0] 14,15
GAD[31..0] 16
GC_BE#[3..0] 16
DDR_VREF
SM_VREF
VCC_AGP
SRCVEN_OUT#
SRCVEN_IN#
SMX_RCOMP0
SMY_RCOMP
AGP_VREF
AGP_RCOMP
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Brookdale-G(DDR & AGP)
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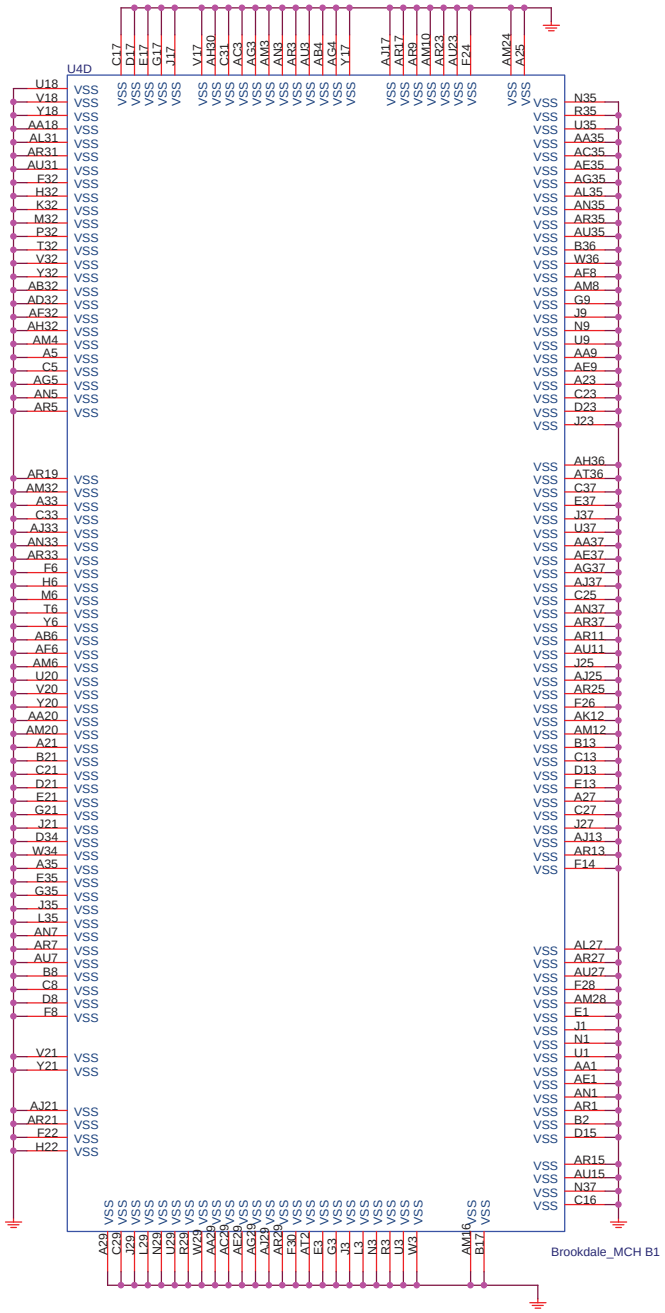
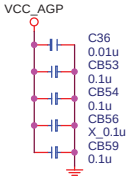
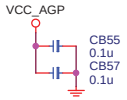


GMCH DECOUPLING CAPACITOR



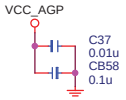
Pin A5
Pin E1
Pin J1
Pin N1
Pin U1

Place decoupling cap close to GMCH AGP Interface < 0.1"



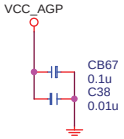
Pin AA1
Pin AE1

Place decoupling cap close to GMCH Hub-Link Interface< 0.1"

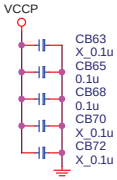


Pin B14
Pin A15

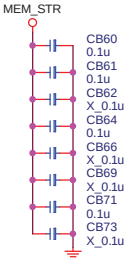
Place decoupling cap close to GMCH DAC Interface< 0.1"



Place decoupling cap close to GMCH Core Logic Interface < 0.1"

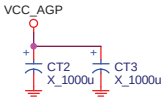


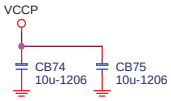
Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor



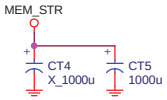
Pin AL37
Pin AU5
Pin AU9
Pin AU13
Pin AU17
Pin AU25
Pin AU29
Pin AU33

Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width





Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot

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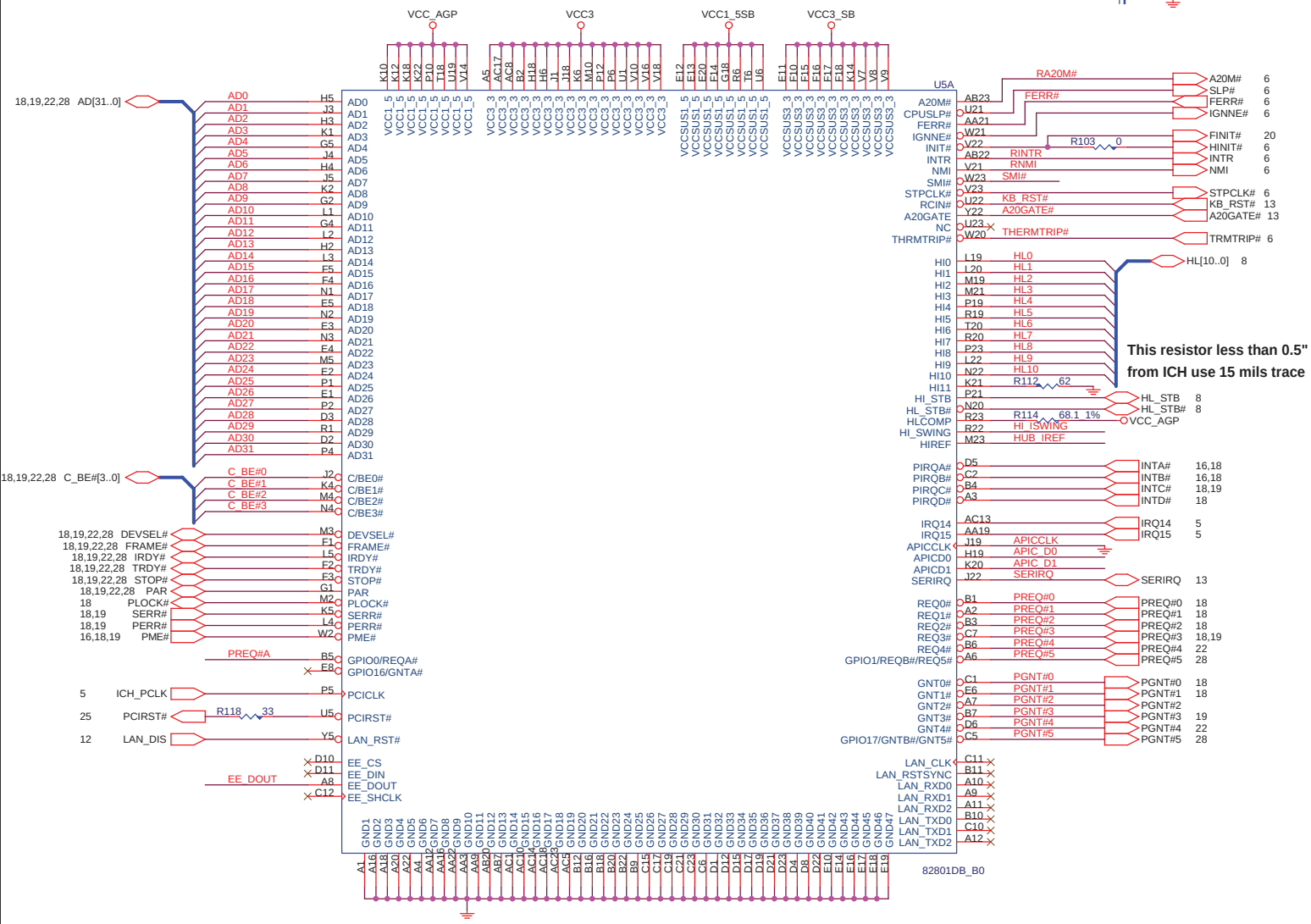
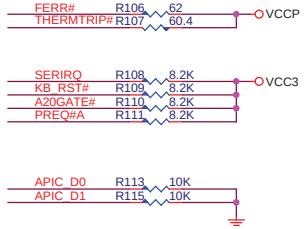
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



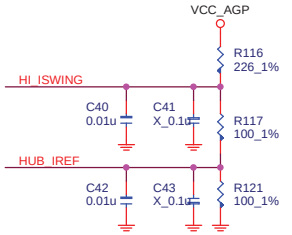
ICH4 STRAPPING RESISTORS

Reserved pull-down resistor for ICH4 reserved function straps.

ICH4 PULL-UP/DOWN RESISTORS



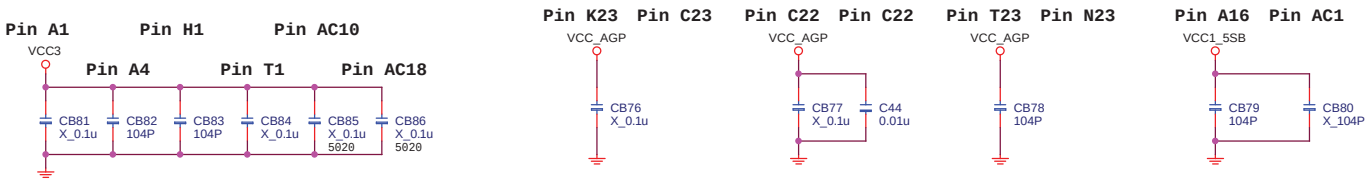
ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



FOR Core Logic FOR PLL FOR Hub Interface

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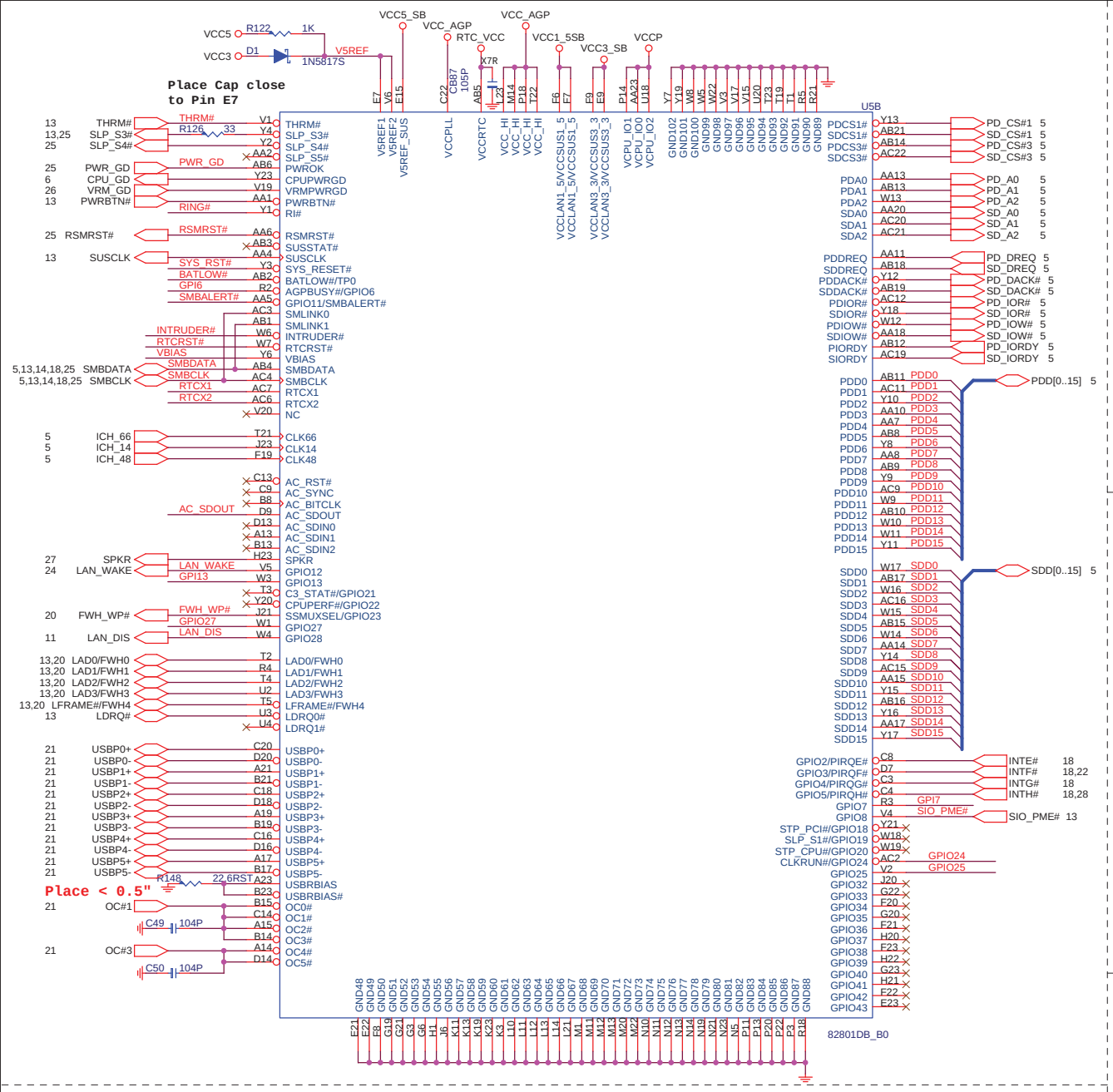
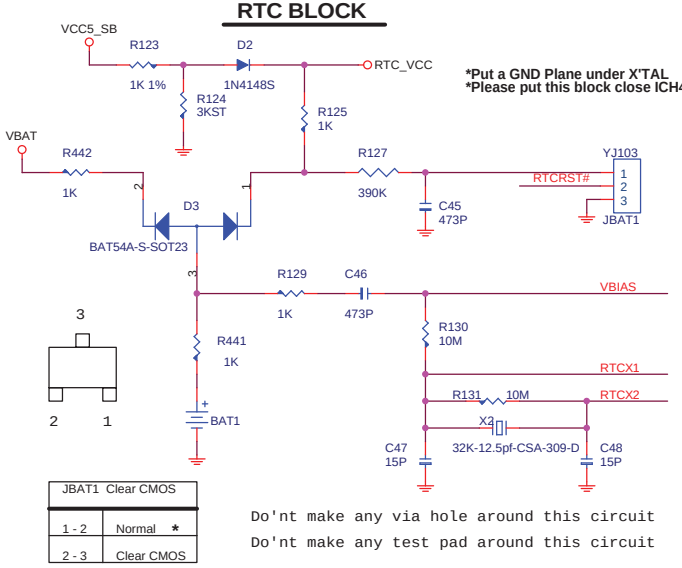


RTC BLOCK



JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

Do'nt make any via hole around this circuit

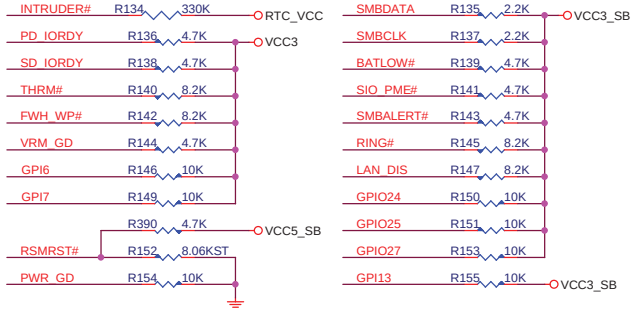
Do'nt make any test pad around this circuit

ICH4 STRAPPING RESISTORS

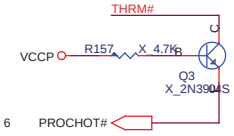
AC_SDOUT	
HIGH	FSB Safe mode
LOW	FSB Auto mode *

SPKR	
HIGH	No Reboot mode
LOW	Reboot mode *

ICH4 PULL-UP/DOWN RESISTORS



PROCHOT BLOCK



SYSTEM RESET

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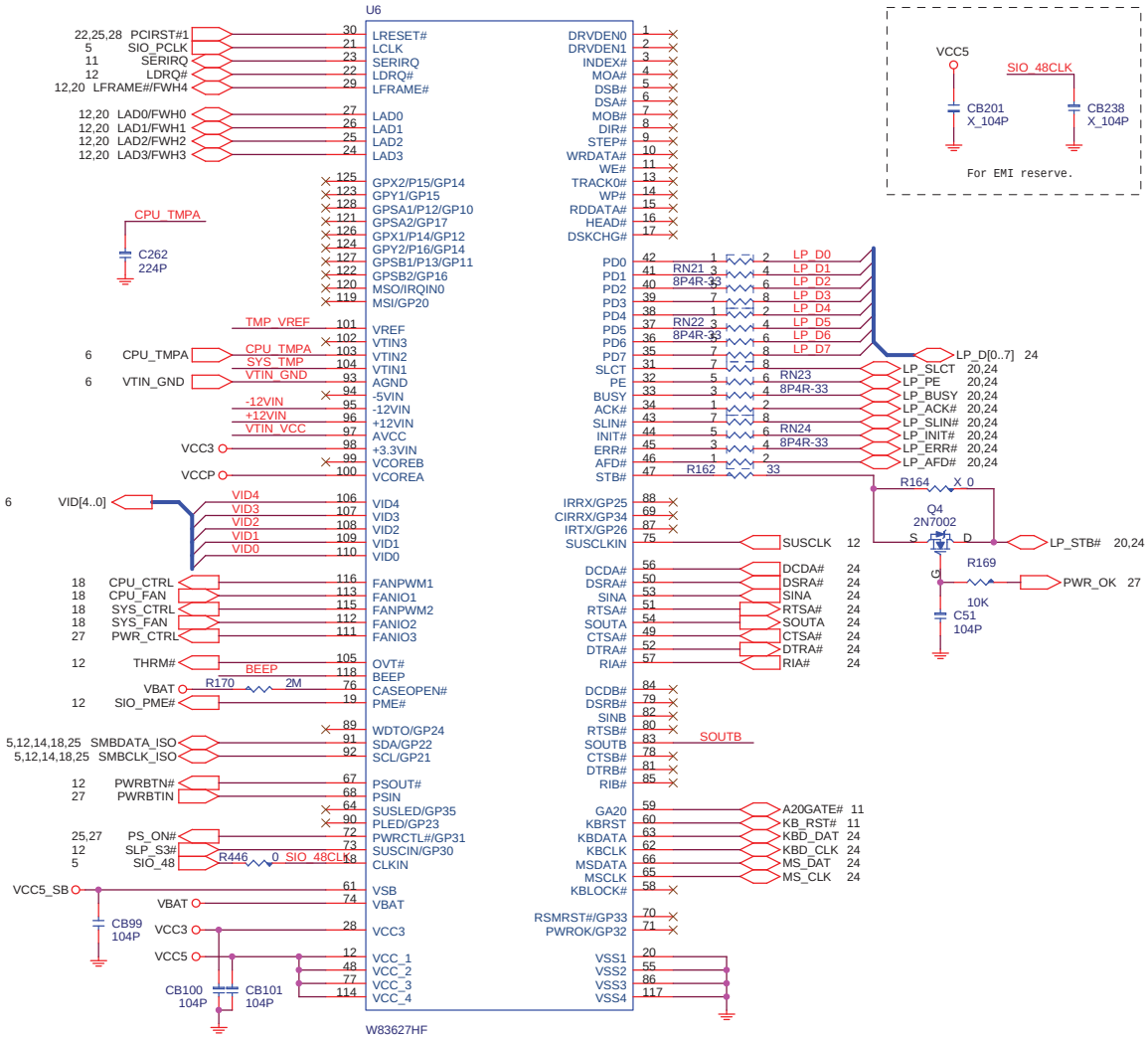
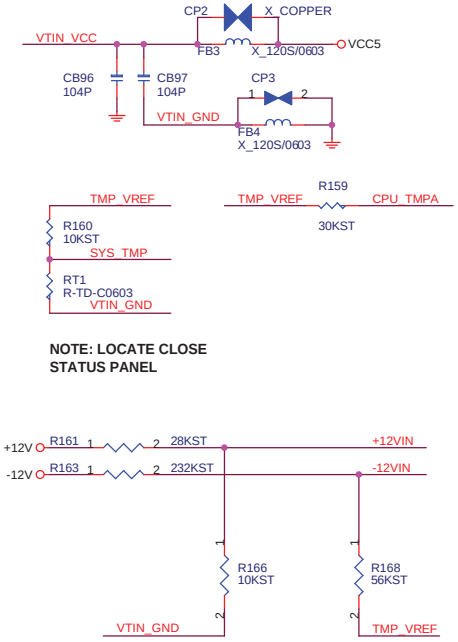
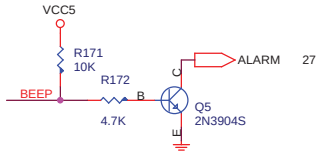
LPC SUPER I/O W83627HF



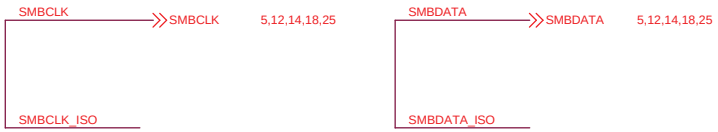
THERMAL RESISTOR BLOCK



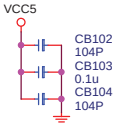
SPEAKER BLOCK



SMBus Isolation



LPC I/O DECOUPLING CAPACITORS

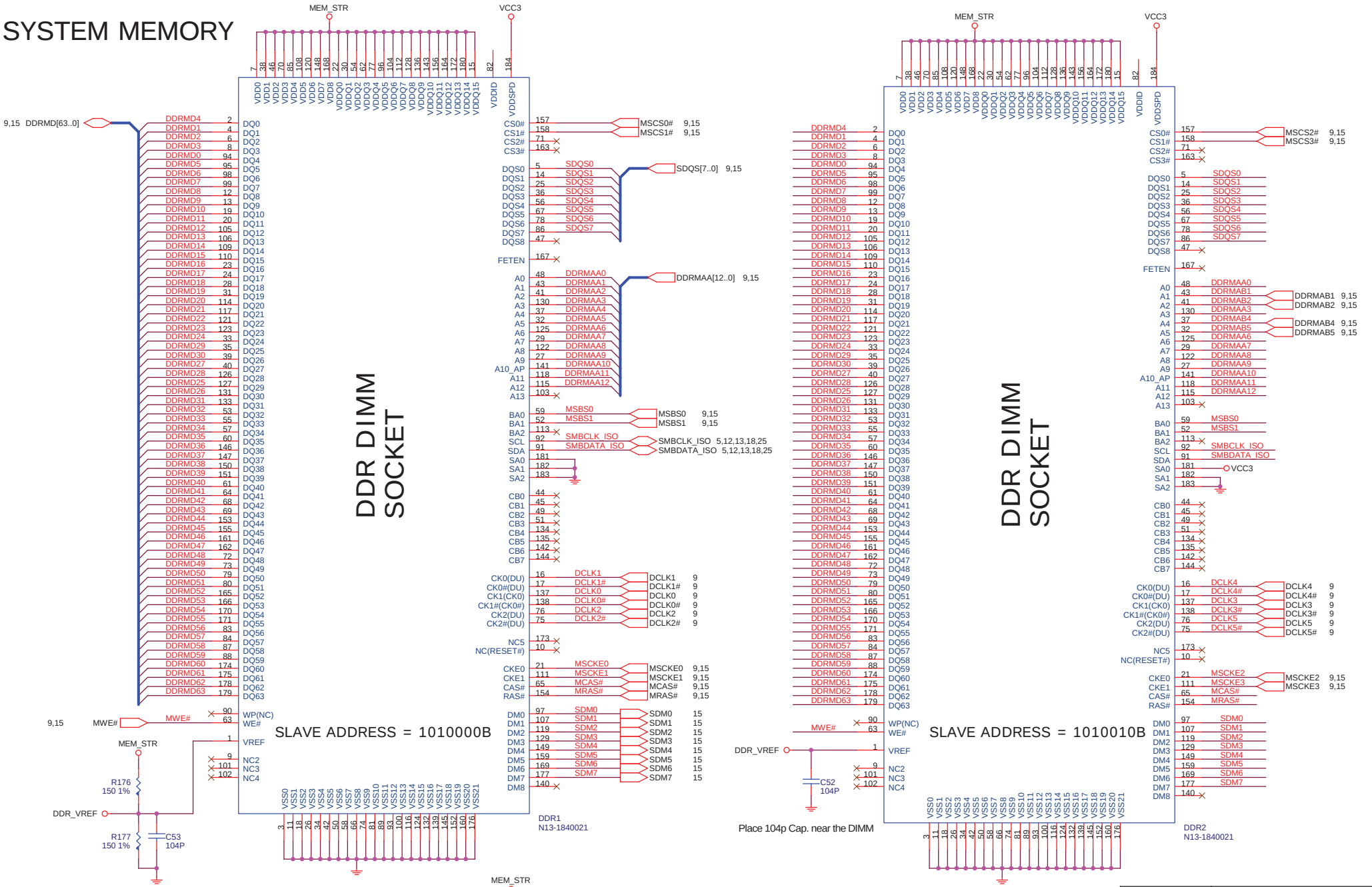


SUPER I/O STRAPPING RESISTOR

SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

Micro-Star	Title: MS-6710	Rev: 10B
Document Number: LPC I/O W83627HF		
Last Revision Date: Thursday, July 10, 2003	Sheet 13 of 30	

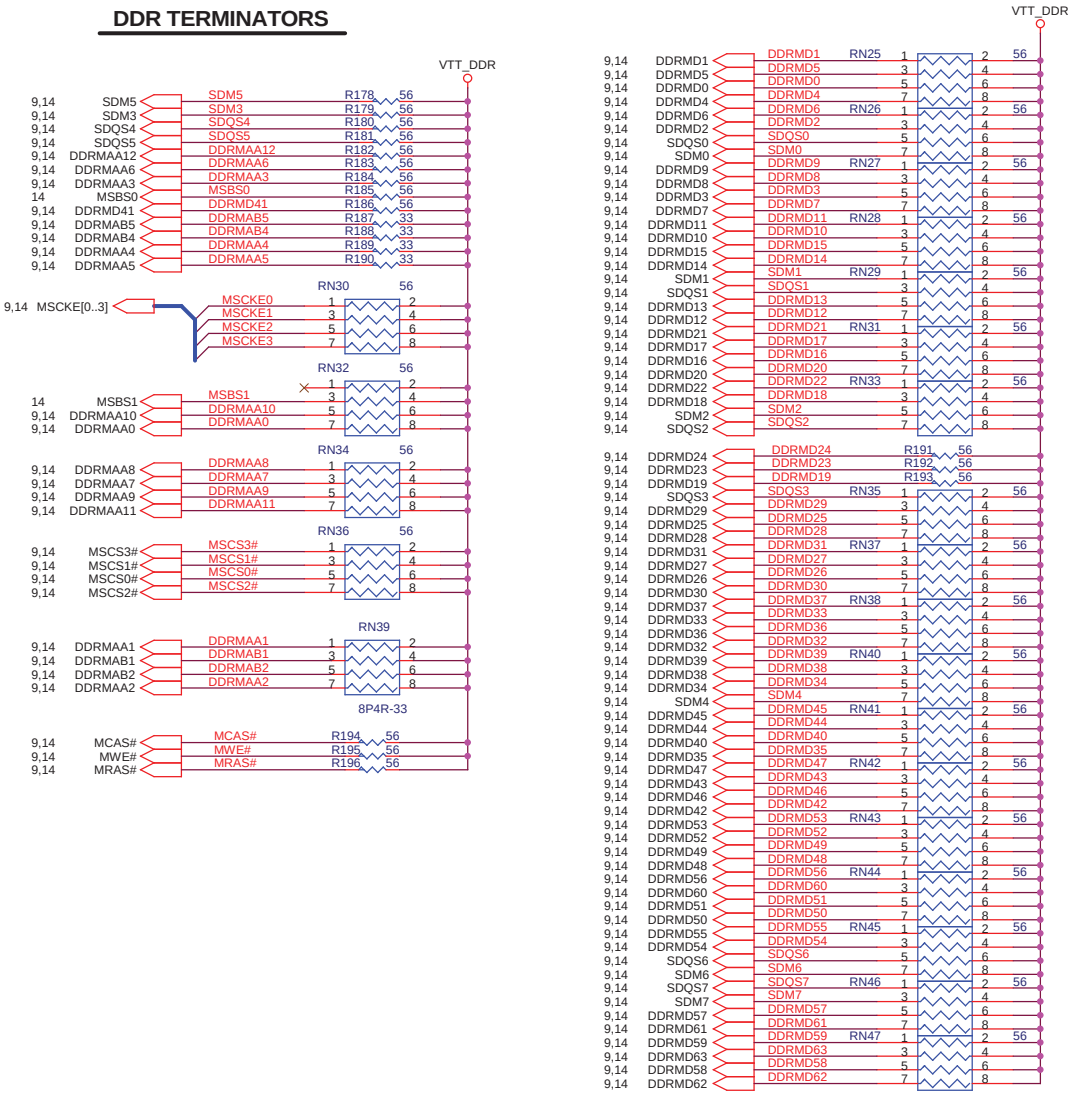
SYSTEM MEMORY



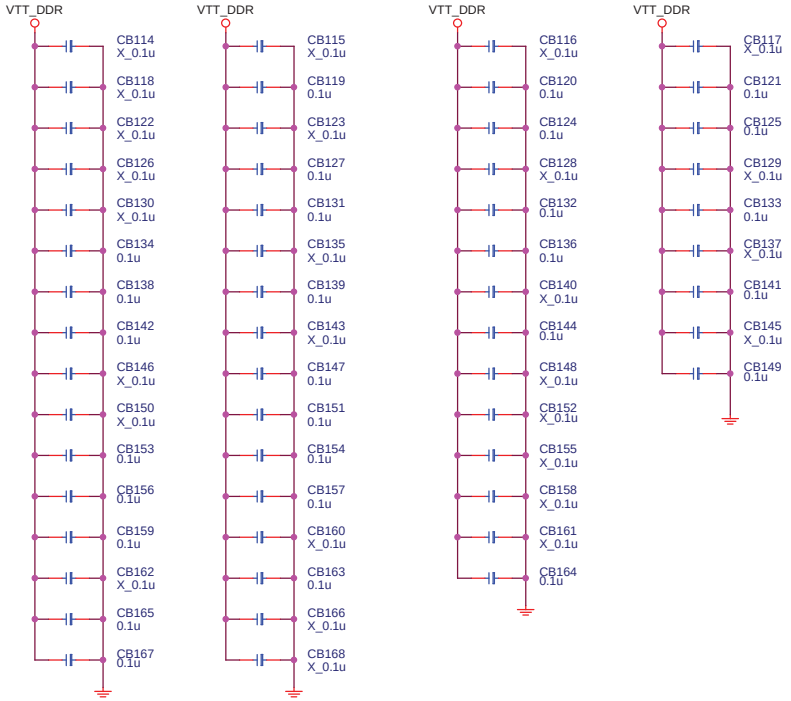
Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DIMM

Micro-Star	Title: MS-6710	Rev: 10B
Document Number: DDR DIMM1 & 2		
Last Revision Date: Thursday, July 10, 2003	Sheet 14 of 30	

DDR TERMINATORS

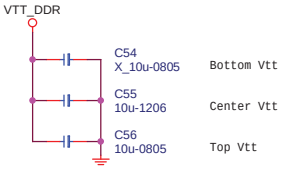


DDR Decouping Caps



Total 110 signal, need 55 pcs decoupling.

Place for VTT_DDR island



Place at the end of the VTT_DDR island

Micro-Star	Title: MS-6710	Rev: 10B
Document Number: DDR Terminator Resistor		
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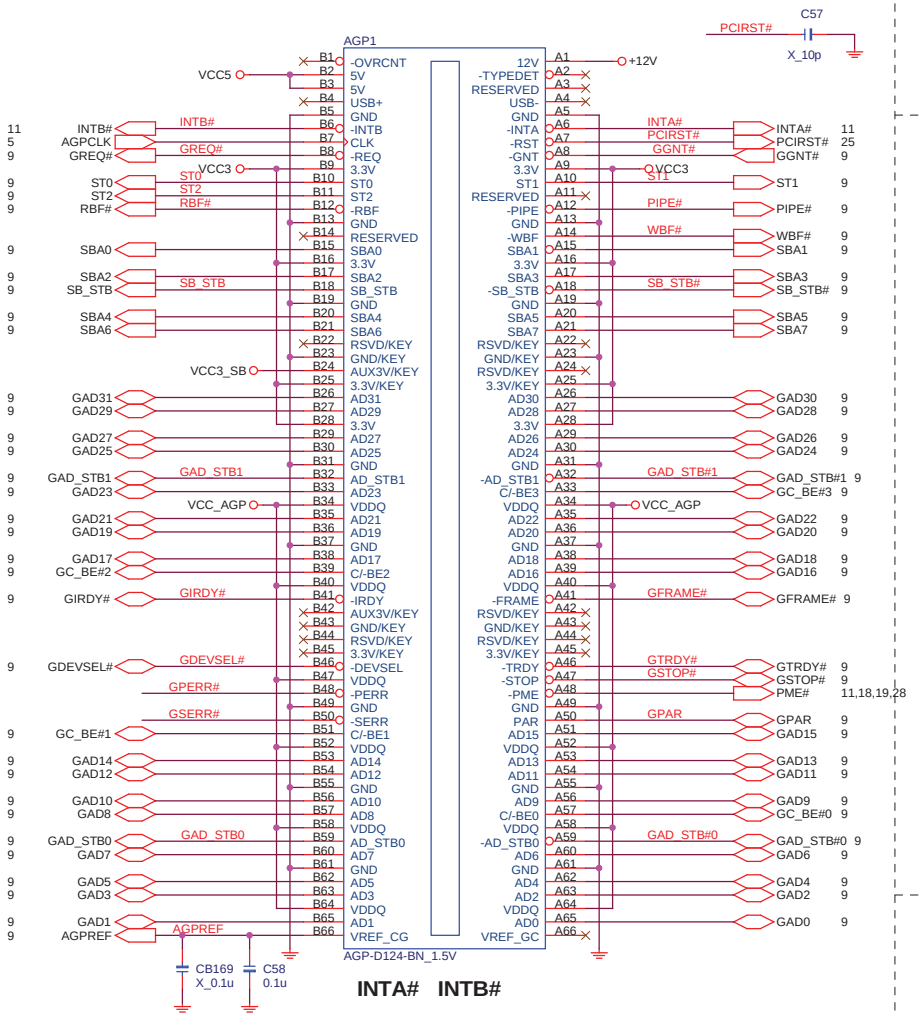
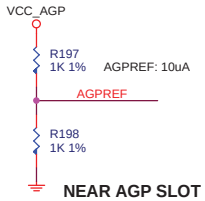
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



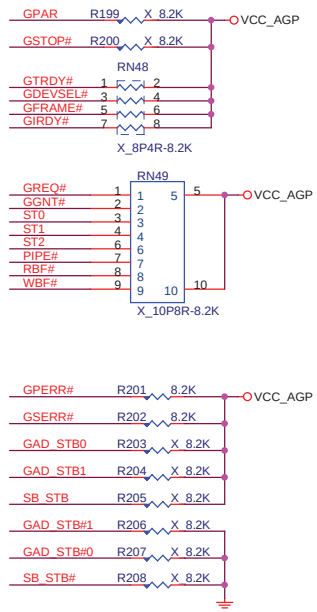
INTA# INTB#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

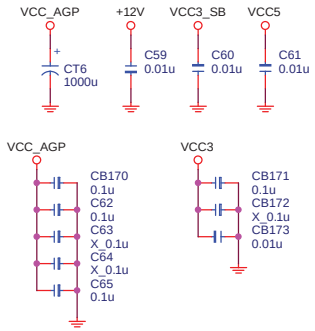
AGP TERMINATION RESISTORS



LESS 100MILS STUB TRACE LENGTH FOR 2/4X
LESS 500MIL FOR 1X MUST BE FOLLOWING.

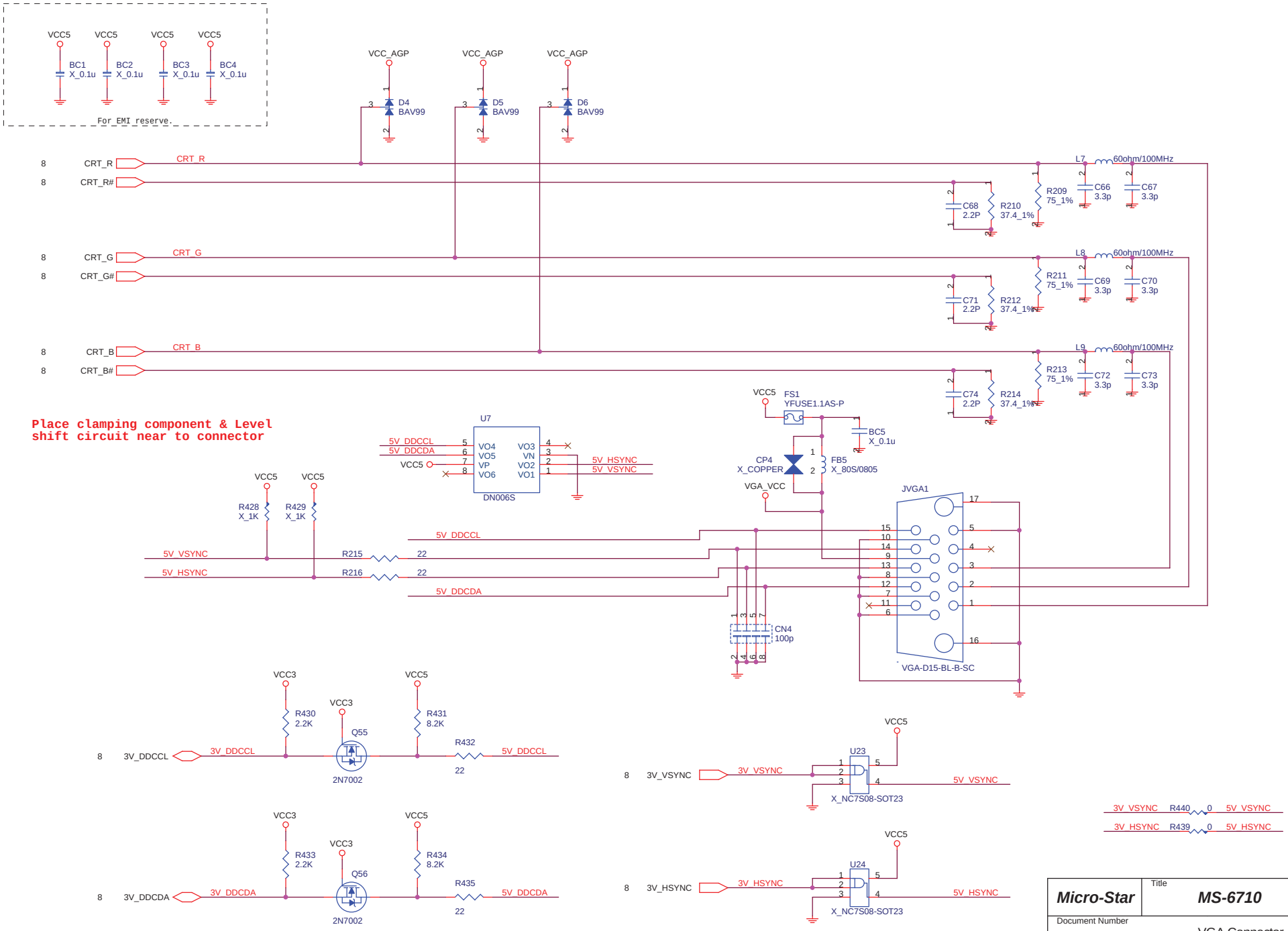
Place these resistors between AGP slot & GMCH

AGP SLOT DECOUPLING CAPACITORS



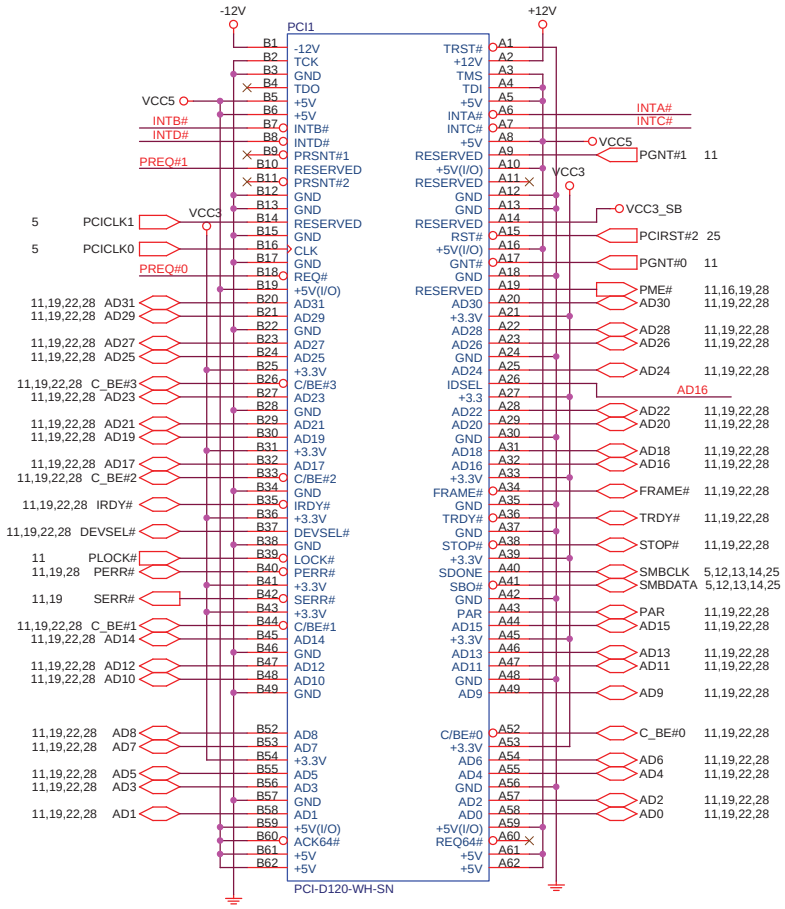
Micro-Star	Title: **MS-6710**	Rev: **10B**
Document Number: AGP Slot		
Last Revision Date: Thursday, July 10, 2003	Sheet 16 of 30	

Video Connector



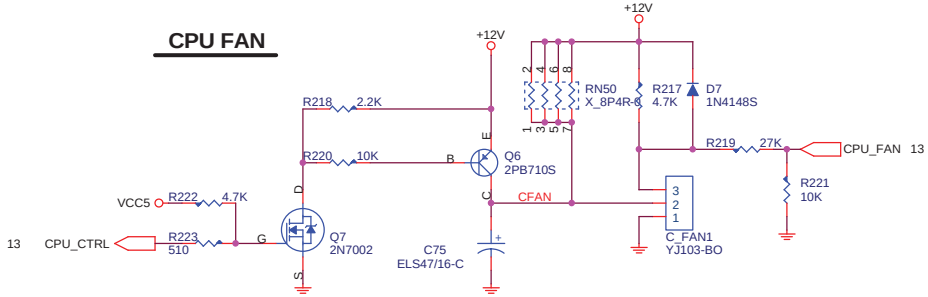
Micro-Star	Title: MS-6710		Rev: 10B
Document Number: VGA Connector			
Last Revision Date: Thursday, July 10, 2003		Sheet 17 of 30	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

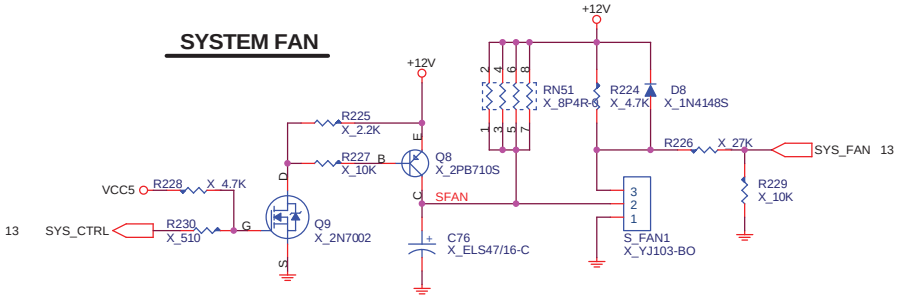


IDSEL = AD16
MASTER = PREQ0
INTA#

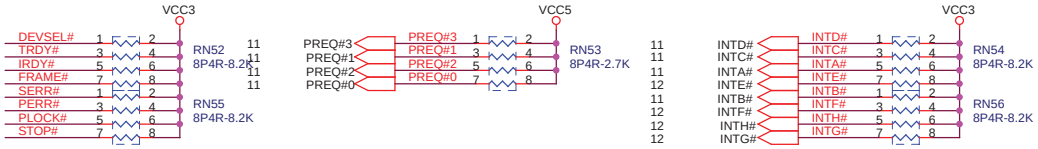
CPU FAN



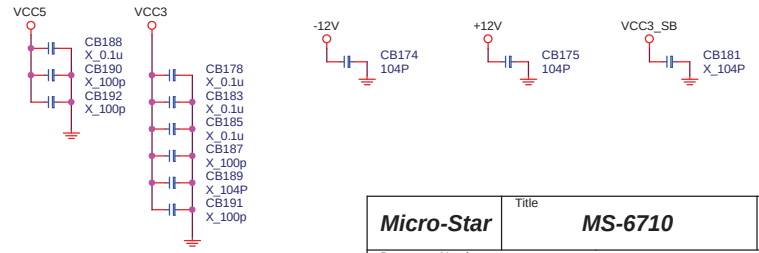
SYSTEM FAN



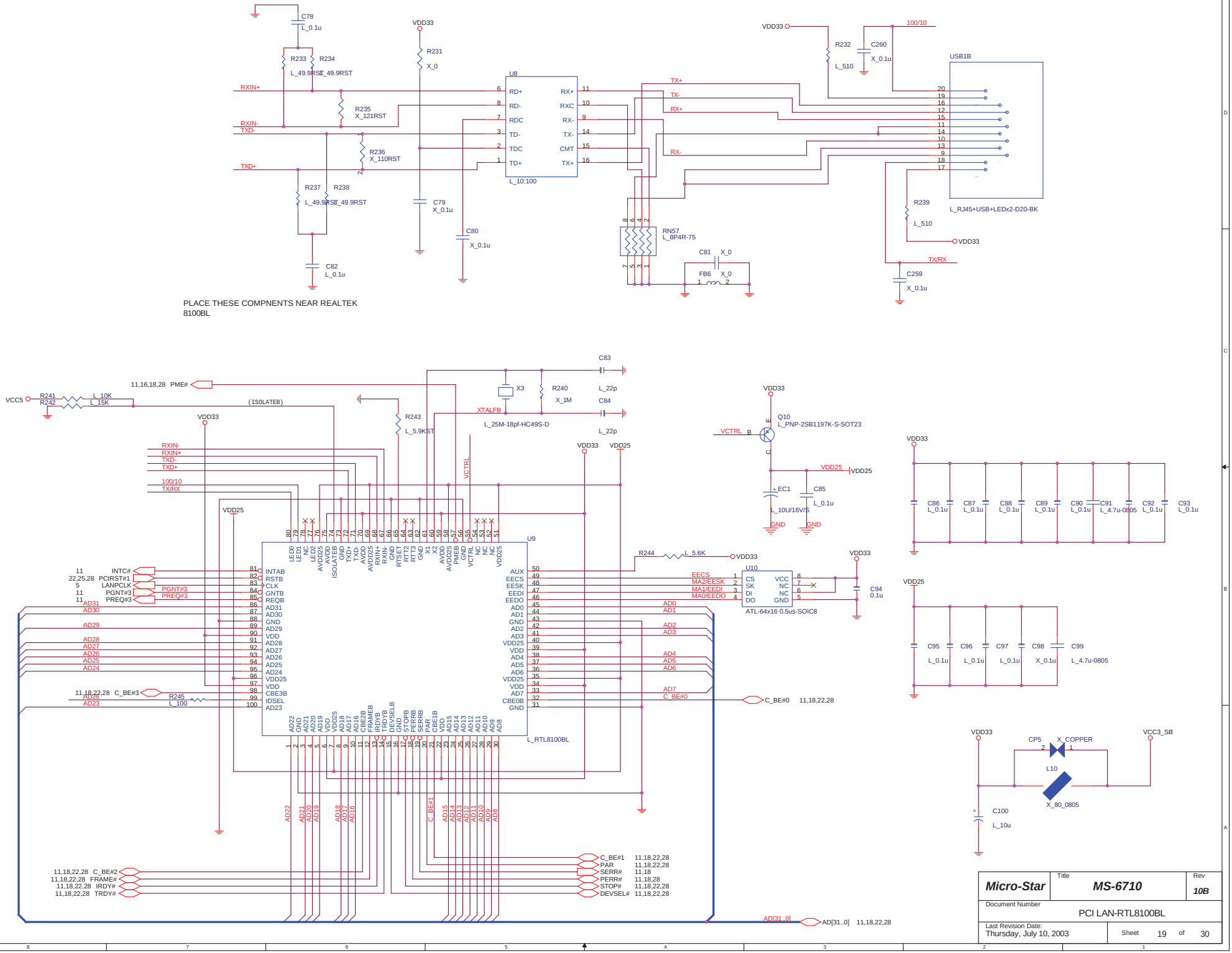
PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6710	Rev: 10B
Document Number: PCI Slot 1 & FAN		
Last Revision Date: Thursday, July 10, 2003	Sheet 18 of 30	


C78
L_0.1u
VDD33
R231
X_0
R233
R234
L_49.9RST
L_49.9RST
RXIN+
RXIN-
TXD-
TXD+
R235
X_121RST
R236
X_110RST
R237
R238
L_49.9RST
L_49.9RST
C79
X_0.1u
C80
X_0.1u
C82
L_0.1u
U8
RD+
RD-
RDC
TD-
TDC
TD+
RX+
RXC
RX-
TX-
CMT
TX+
L_10:100
TX+
TX-
RX+
RX-
VDD33
R232
L_510
C260
X_0.1u
100/10
USB1B
L_RJ45+USB+LEDx2-D20-BK
R239
L_510
VDD33
TX/RX
C259
X_0.1u
RN57
L_8P4R-75
C81
X_0
FB6
X_0
PLACE THESE COMPNENTS NEAR REALTEK
8100BL
C83
X3
R240
X_1M
L_22p
C84
L_22p
XTALFB
L_25M-18pf-HC49S-D
R243
L_5.9KST
11,16,18,28 PME#
VCC5
R241
L_10K
R242
L_15K
(ISOLATEB)
VDD33
VDD25
RXIN-
RXIN+
TXD-
TXD+
100/10
TX/RX
VCTRL
U9
L_RTL8100BL
INTAB
RSTB
CLK
GNTB
REQB
AD31
AD30
GND
AD29
VDD
AD28
AD27
AD26
AD25
AD24
VDD25
VDD
CBE3B
IDSEL
AD23
AUX
EECS
EESK
EEDI
EEDO
AD0
AD1
GND
AD2
AD3
VDD25
VDD
AD4
AD5
AD6
VDD25
VDD
AD7
CBE0B
GND
11 INTC#
22,25,28 PCIRST#1
5 LANPCLK
11 PGNT#3
11 PREQ#3
R245
L_100
11,18,22,28 C_BE#3
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
C_BE#2 11,18,22,28
FRAME# 11,18,22,28
IRDY# 11,18,22,28
TRDY# 11,18,22,28
C_BE#1 11,18,22,28
PAR 11,18,22,28
SERR# 11,18
PERR# 11,18,28
STOP# 11,18,22,28
DEVSEL# 11,18,22,28
C_BE#0 11,18,22,28
AD[31..0] 11,18,22,28
R244
L_5.6K
VDD33
U10
CS
SK
DI
DO
VCC
NC
NC
GND
EECS
MA2/EESK
MA1/EEDI
MA0/EEDO
ATL-64x16 0.5us-SOIC8
C94
0.1u
VDD33
Q10
L_PNP-2SB1197K-S-SOT23
VCTRL
VDD25
VDD25
+EC1
L_10U/16V/S
C85
L_0.1u
GND
GND
VDD33
C86 L_0.1u
C87 L_0.1u
C88 L_0.1u
C89 L_0.1u
C90 L_0.1u
C91 L_4.7u-0805
C92 L_0.1u
C93 L_0.1u
VDD25
C95 L_0.1u
C96 L_0.1u
C97 L_0.1u
C98 X_0.1u
C99 L_4.7u-0805
VDD33
CP5
X_COPPER
VCC3_SB
L10
X_80_0805
C100
L_10u
Micro-Star
Title
MS-6710
Rev
10B
Document Number
PCI LAN-RTL8100BL
Last Revision Date:
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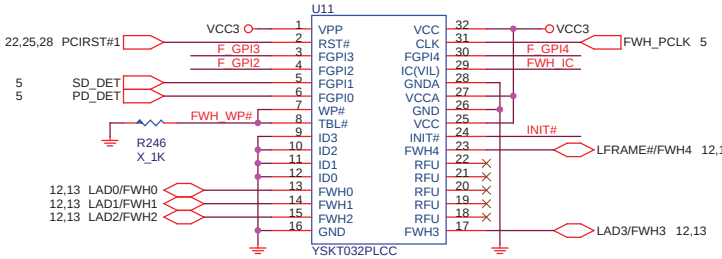
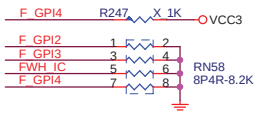
Sheet 19 of 30

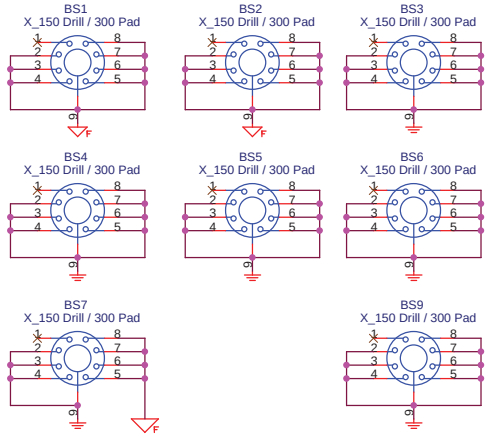
Firware Hub (FWH)



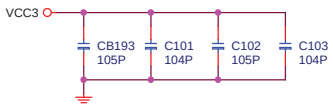
FWH RESISTORS



PCB Mounting Holes

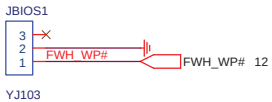


FWH DECOUPLING CAPACITORS



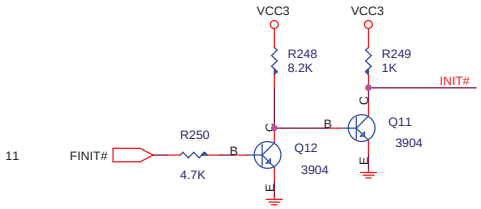
Place Cap. as Close to FWH< 350 mil

FWH write protect



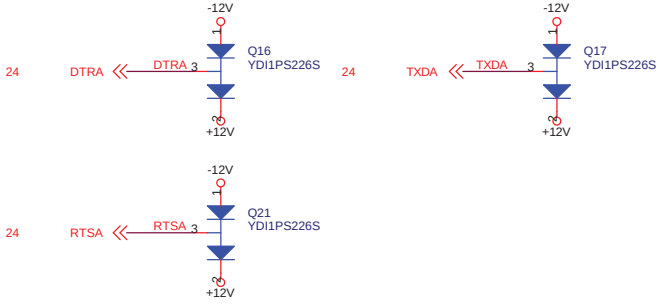
JBIOS BIOS Update	
1-2	Locked
2-3	Unlocked *

FWH INIT Signal Voltage Translation Block

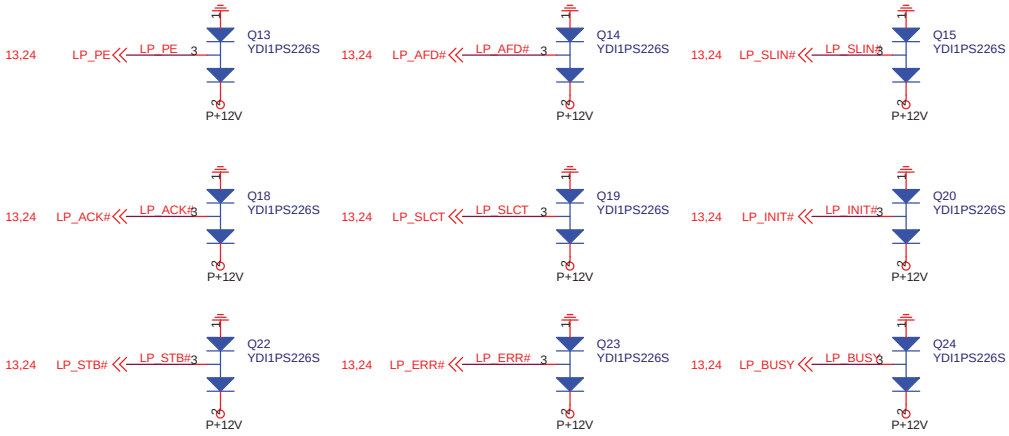


SIMULATION TRACE

Serial port protection diode

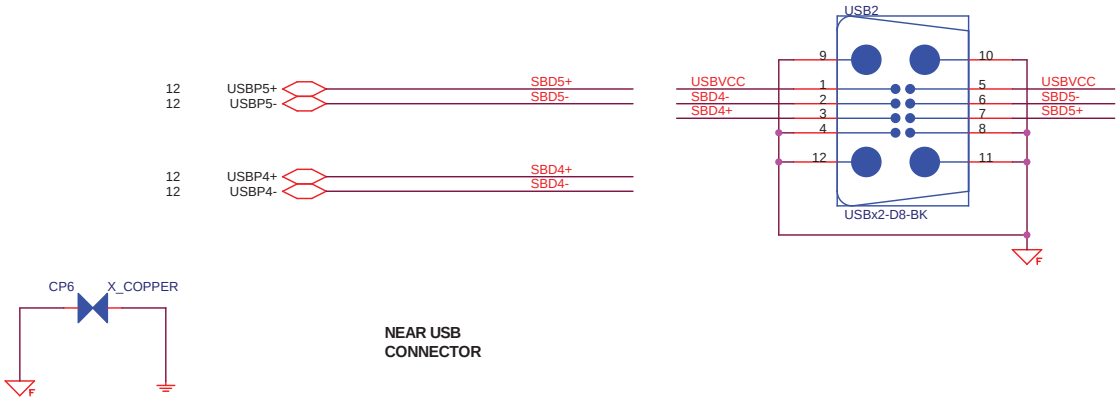


Perallal port protection diode

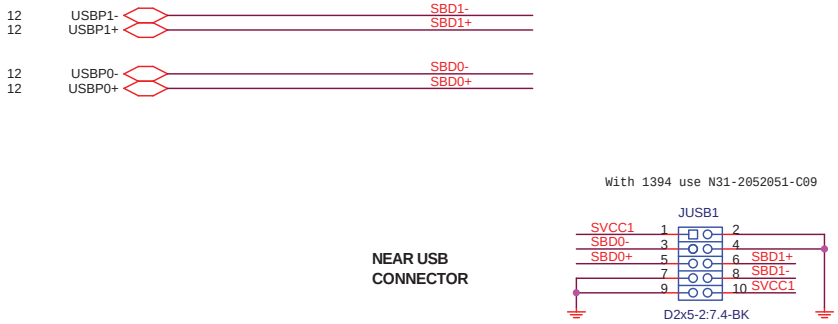


Micro-Star	Title: MS-6710	Rev: 10B
Document Number: FWH & protection diode		
Last Revision Date: Thursday, July 10, 2003	Sheet 20 of 30	

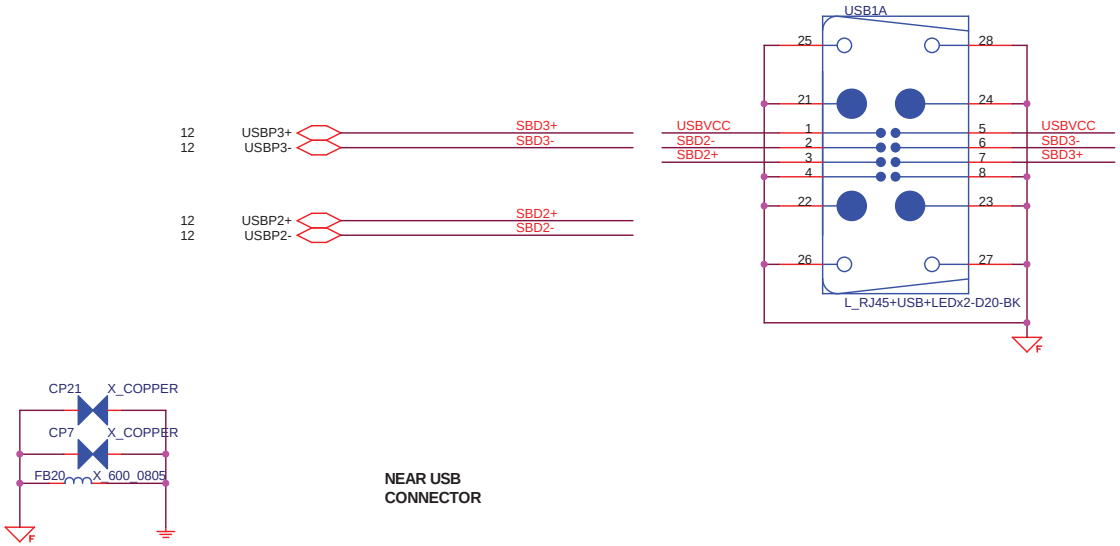
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



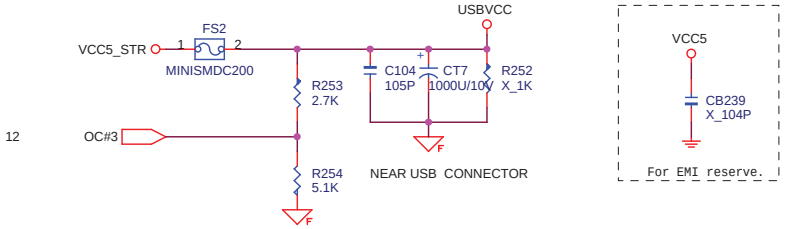
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



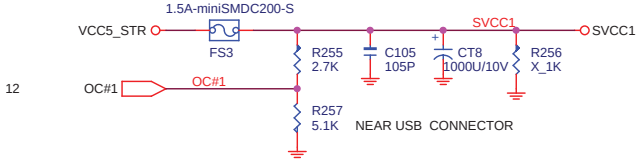
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 2,3,4,5



POWER CIRCUIT FOR USB PORT 0,1



*** USB Trace width : 7.5 mils**
*** USB Trace Spacing : 20 mils**
*** Differential USB Signlas Trace, Spacing : 18 mils**
*** USB Power Trace must be 40mils width**

Micro-Star	Title: MS-6710	Rev: 10B
Document Number: USB Connectors		
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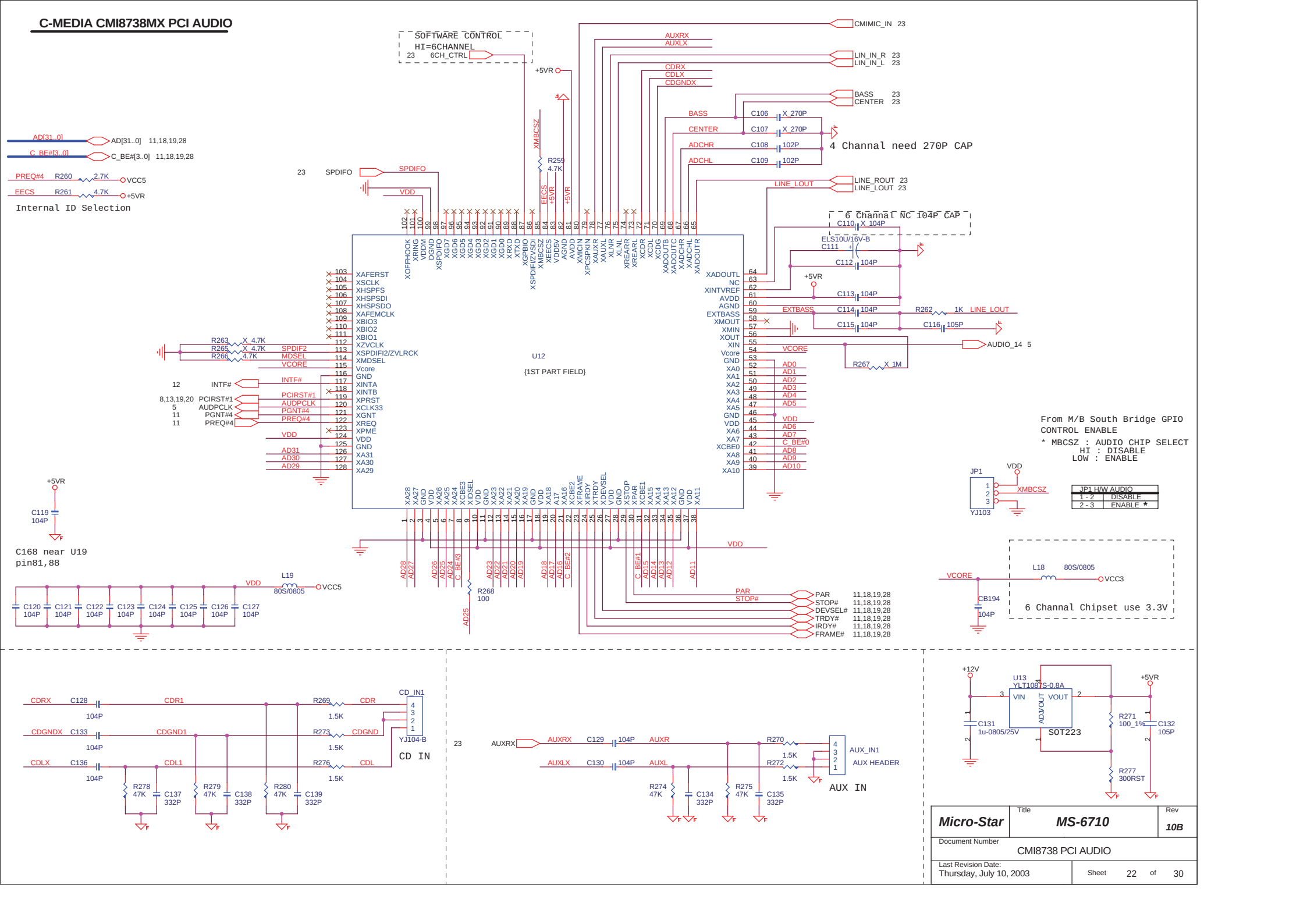
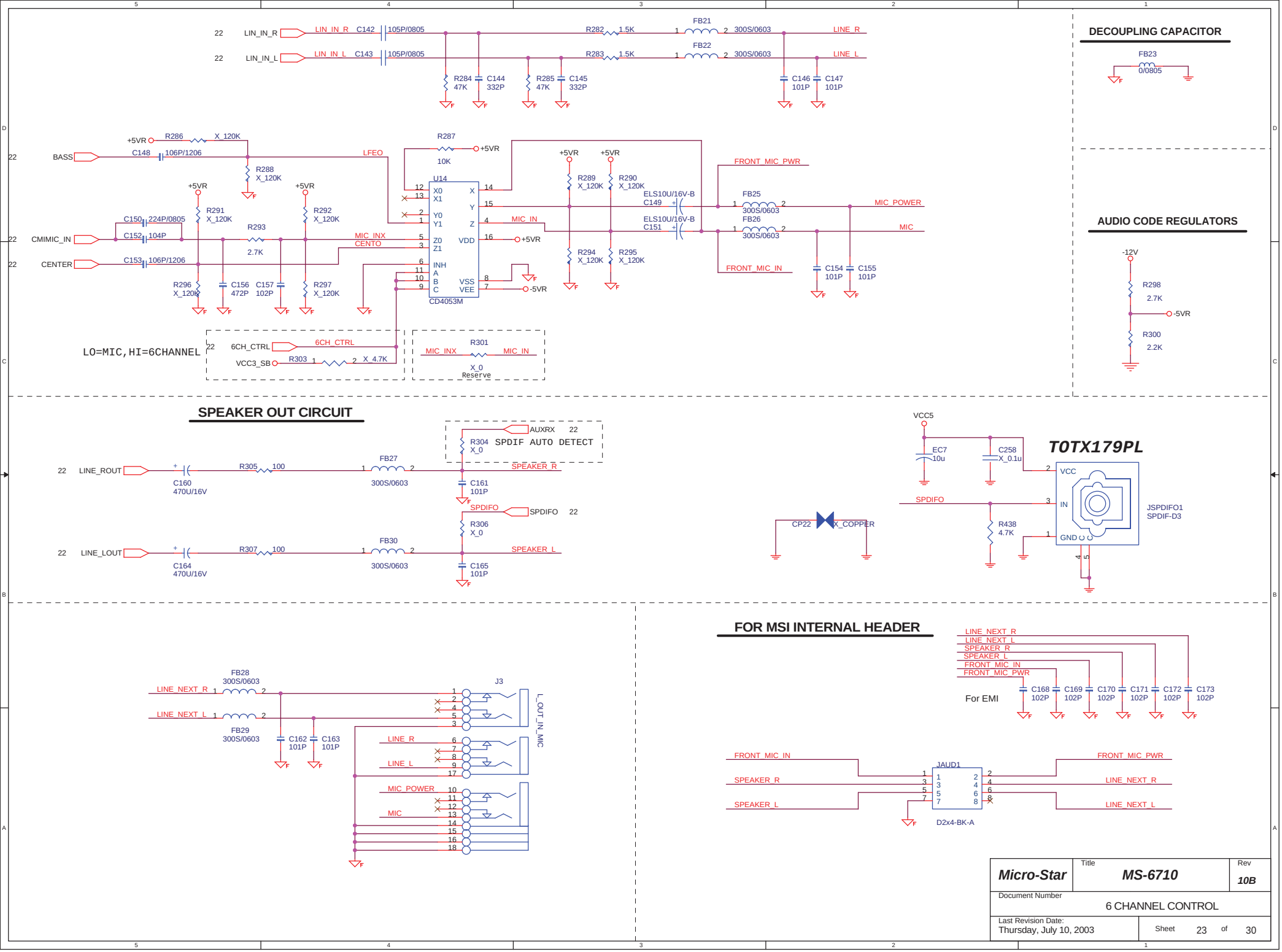
C-MEDIA CMI8738MX PCI AUDIO

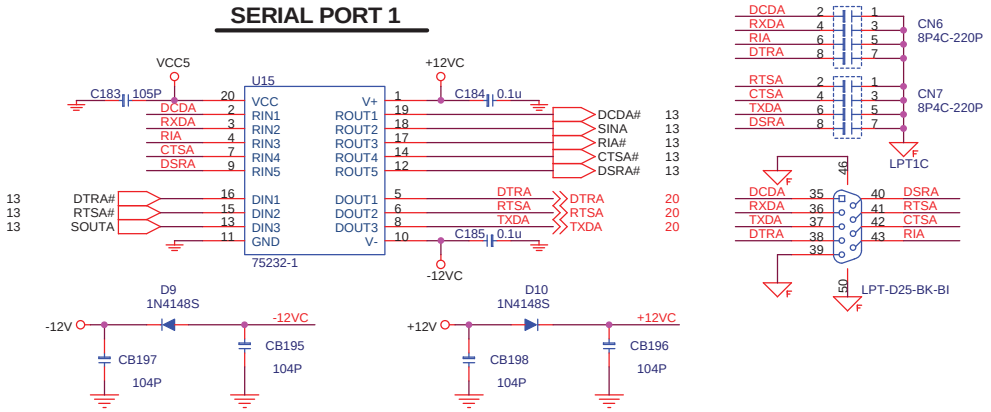


Micro-Star	Title: MS-6710	Rev: 10B
Document Number: CMI8738 PCI AUDIO		
Last Revision Date: Thursday, July 10, 2003	Sheet 22 of 30	

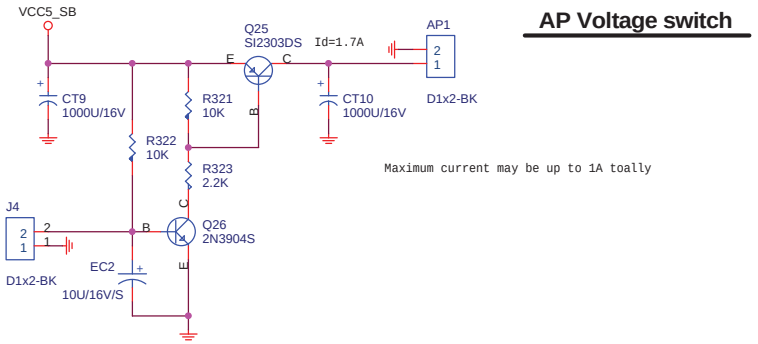


Micro-Star	Title: MS-6710	Rev: 10B
Document Number: 6 CHANNEL CONTROL		
Last Revision Date: Thursday, July 10, 2003	Sheet 23 of 30	

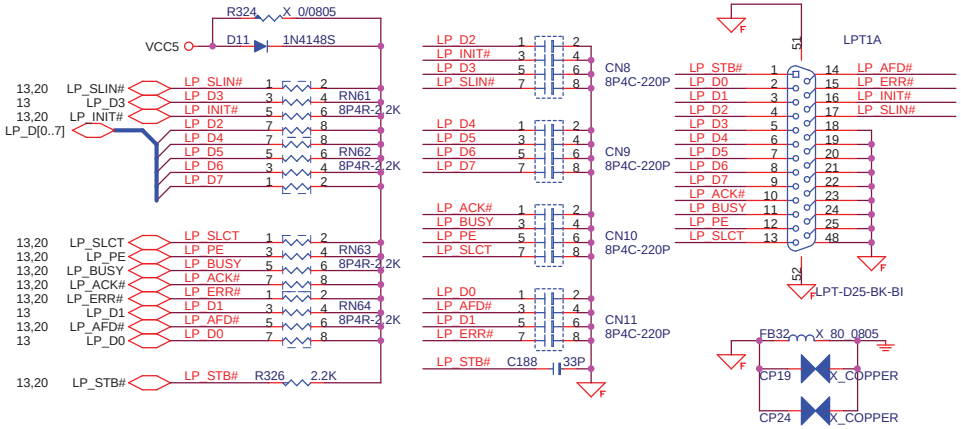
SERIAL PORT 1



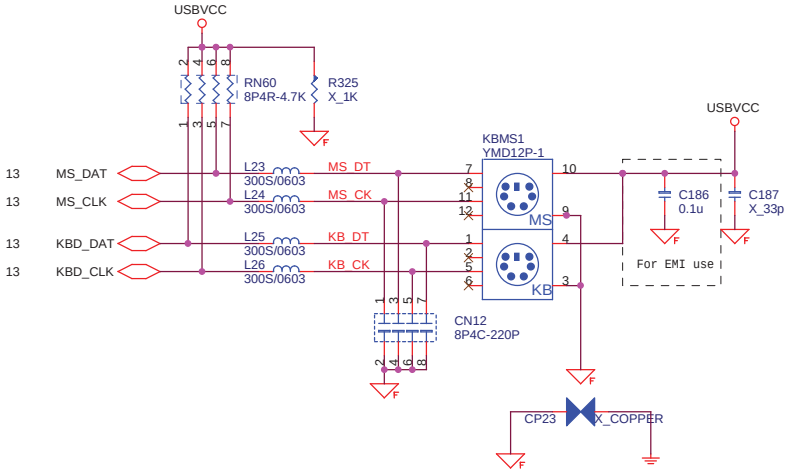
AP Voltage switch

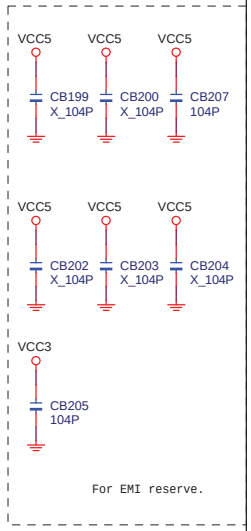


PARALLAL PORT

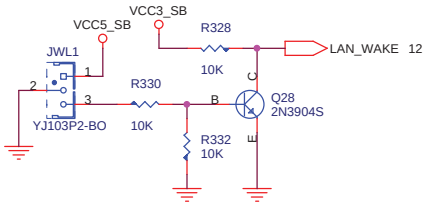


PS2 KEYBOARD & MOUSE CONNECTOR

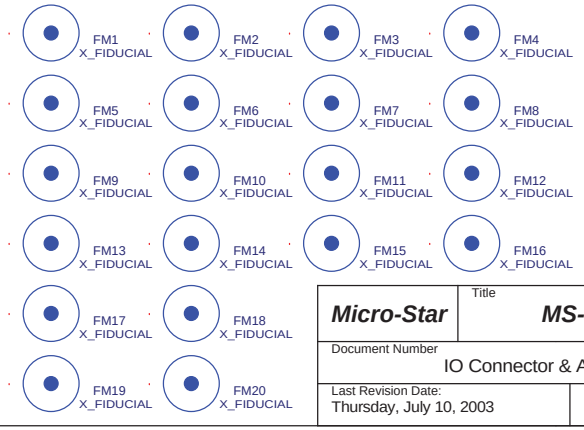




Wake On LAN Header



PCB Fiducials



Micro-Star	Title: MS-6710	Rev: 10B
Document Number: IO Connector & AP Voltage switch		
Last Revision Date: Thursday, July 10, 2003	Sheet 24 of 30	

AGP4X & GMCH 1.8V POWER TRANSLATOR

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

VCC3 VCC5_SB VCC3_SB PS_ON# 13

R337 1K R338 4.7K R334 10K R340 4.7K R339 10K C190 X_104P

12 SLP_S4#
12 SLP_S3# R341 X_0
8,12 PWR_GD
27 PWR_OK

Q31 2N3904S

RSMRST# 12

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

Near 302D

U17

R346 330 R347 X_200 R348 330

11,16 PCIRST#
5 HD_RST#
18 PCIRST#2
8,13,19,20 PCIRST#1
5,12,13,14,18 SMBDATA_ISO
5,12,13,14,18 SMBCLK_ISO

1 DGND
2 PCIRST#/GPIOA
3 HDD_RST#/GPIOA
4 SLOT_RST#/GPIOA
5 DEV_RST#/GPIOA
6 I2C_DATA
7 I2C_CLK
8 BT_DRV
9 BT_SEN
10 BT_SINK
11 AGND0
12 SEL1

48 PLED1 47 PLED0 46 PWR_OK 45 FP_RST#/GPIOB 44 PWR_OK1/GPIOC 43 EXTRA_PWGD/GPIOC 42 CHIP_PWGD/GPIOC 41 CPU_PWGD/GPIOC 40 RSM_RST#/GPIOB 39 SLP_S3# 38 SLP_S5# 37 S5O#/GPIOB/SEL0

36 5V_USB
35 5VSB_DRV
34 5V_DRV
33 TYPEDET#
32 VAGP_SEN
31 VAGP_DRV
30 AGND2
29 1.25VREF
28 9VSB
27 C2
26 C1
25 VCC3

13 VCC 14 VRAMDRV2 15 VRAMSEN 16 VRAMDRV1 17 SS 18 AGND1 19 VRAM_2.5_DEN 20 VRAM_2.5_DRV 21 5VSB 22 VRGOOD 23 1.2V_SEN 24 1.2V_DRV

W83302GCRB

5V DUAL Power

Q30 NDS351S C191 222P CB208 475P/0805/10V VCC5_STR
Q33 P45N02LD C192 X_102P VCC5
Low RDS ON MOSFET

C193 102P VCC_AGP
VREF1_25
C194 105P C195 105P/0805/16V 9VSB
Q34 P3055LSB C196 X_102P +2.5V
D14 1N5817S D15 X_1N4148S EC8 X_47u/16V +12V
CB210 104P VCC5_SB

DDR VTT Power

1.25V/2.1A

VCC3 Q35 P3055LD VTT_DDR Q36 P3055LD
EC3 1000U/6.3V EC4 1000U/6.3V C200 X_102P

VCC5_SB R349 10K
VCC5 VCC5_SB
C198 104P C199 104P C202 474P-X7R

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

FOR 3VDUAL
SETTING BY
SEL1

VCC3 CT14 1000u Q39 P45N02LD

VCC_VID / VID_GOOD

Q37 2N7002 Place MOSFET near CPU
VCC_VID 7
1.2V/0.1A
C204 X_102P C205 106P/1206
R350 X_4.7K VCC5
VID_GD 26
1.0V
THIS PIN IS OPEN DRAIN OUTPUT

VCC3_SB
Wide Trace
EC5 X_1000U/6.3V EC6 1000U/6.3V Q41 NDS351S
CB211 102P VCC5_SB

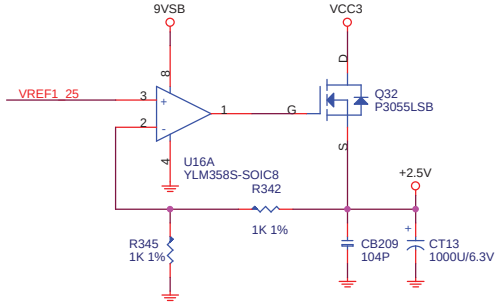
DDR 2.5V Power

2.5V/2.8A+5.92A

VCC3_SB Q40 P3055LD MEM_STR D16 +2.5V
CT15 X_1000U/6.3V C210 X_104P X_1N5817S CB212 104P

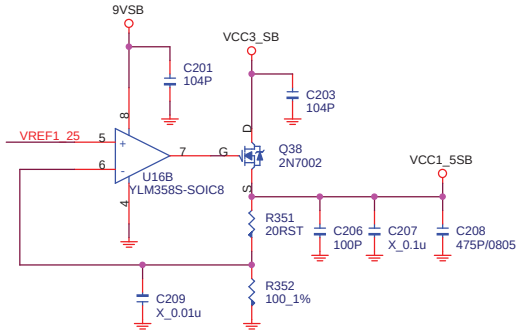
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

AGP 4X 2.5V POWER TRANSLATOR



1.5V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



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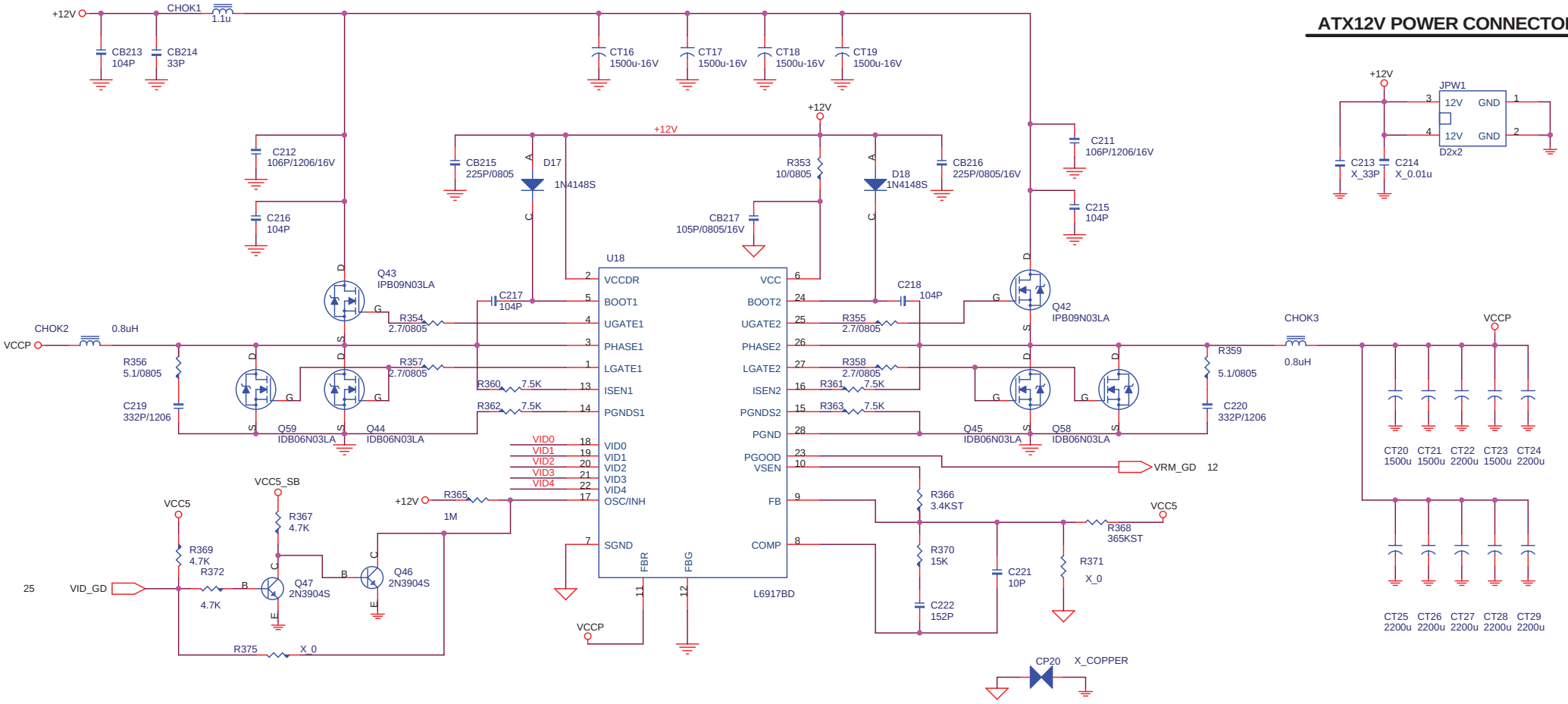
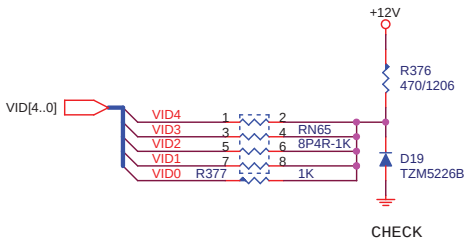
ATX12V POWER CONNECTOR





VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

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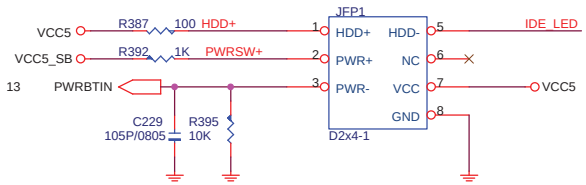
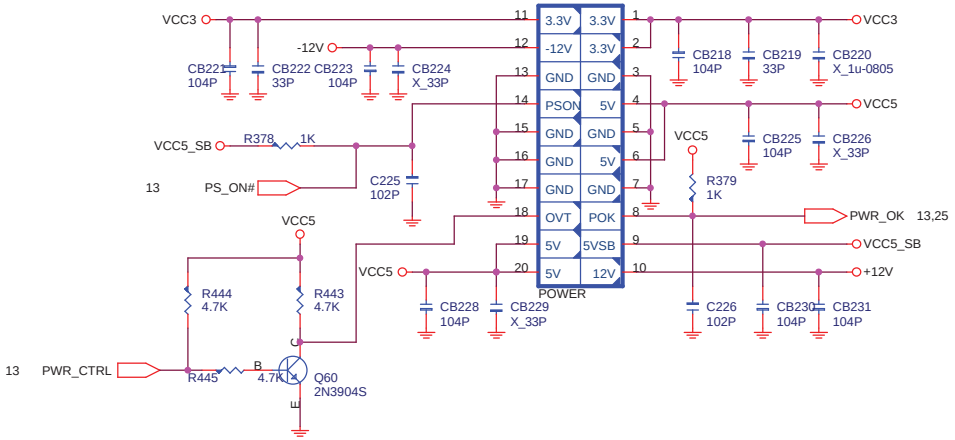
FRONT PANEL

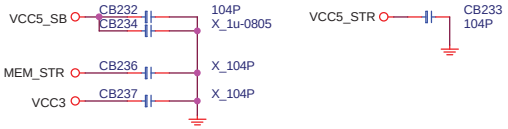


ATX CONNECTOR

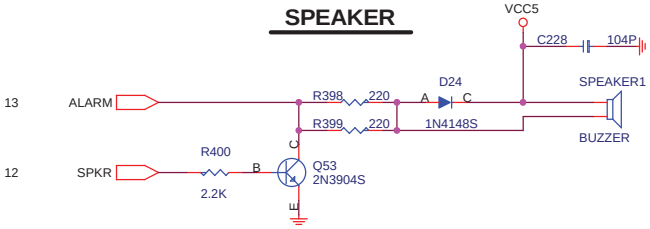


HDD LED

REGULATORS OUTPUT DECOUPLING CAPACITORS



SPEAKER



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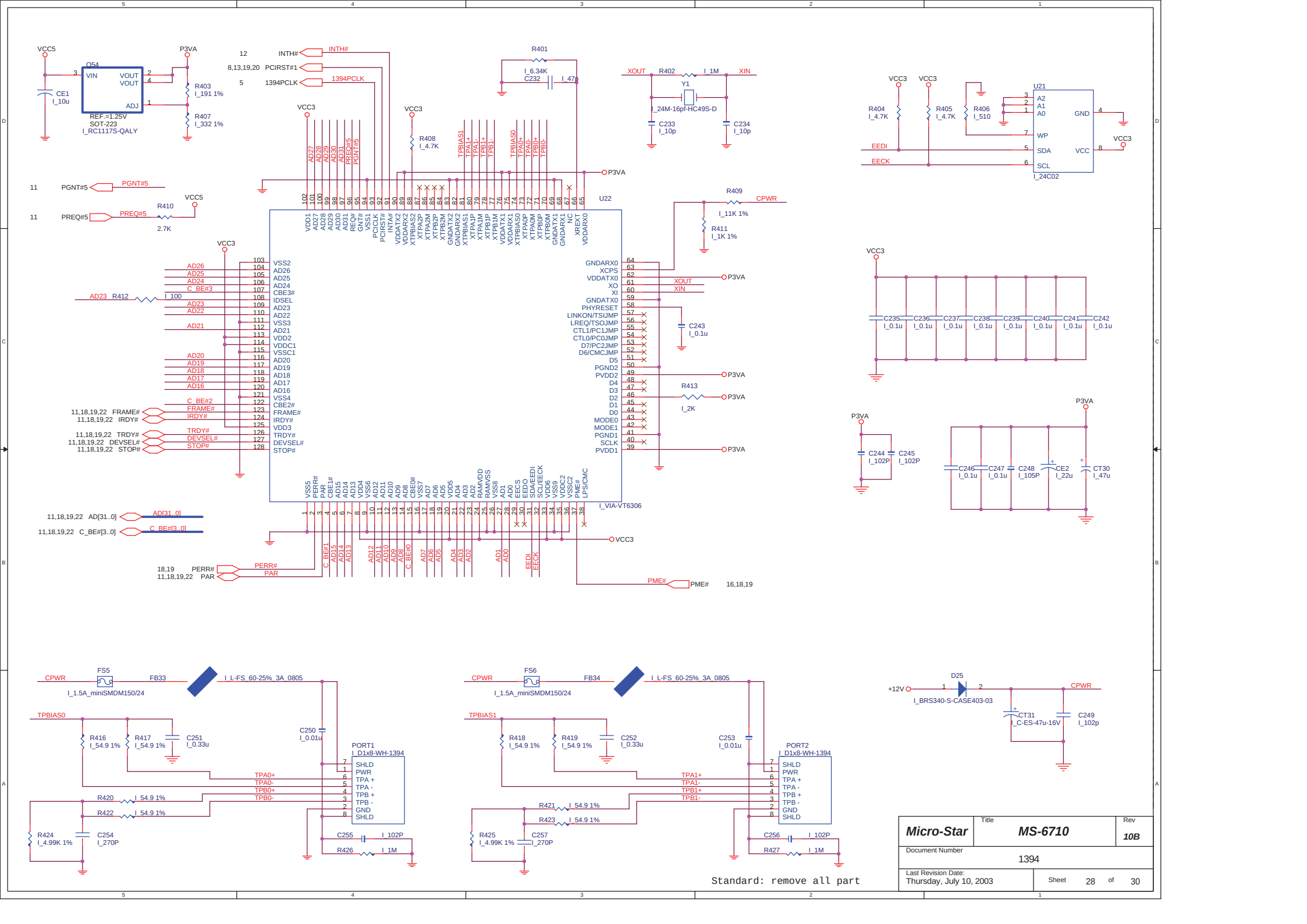
VCC5
P3VA
Q54
VIN
VOUT
VOUT
ADJ
REF.=1.25V
SOT-223
I_RC1117S-QALY
CE1
I_10u
R403
I_191 1%
R407
I_332 1%
INTH#
PCIRST#1
1394PCLK
R401
I_6.34K
C232
I_47p
XOUT
R402
I_1M
XIN
Y1
I_24M-16pf-HC49S-D
C233
I_10p
C234
I_10p
R408
I_4.7K
PGNT#5
PREQ#5
R410
2.7K
U22
R409
I_11K 1%
CPWR
R411
I_1K 1%
I_VIA-VT6306
C243
I_0.1u
R413
I_2K
AD23
R412
I_100
C_BE#3
C_BE#2
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
AD[31..0]
C_BE#[3..0]
PERR#
PAR
PME#
U21
R404
I_4.7K
R405
I_4.7K
R406
I_510
EEDI
EECK
I_24C02
C235
C236
C237
C238
C239
C240
C241
C242
I_0.1u
C244
I_102P
C245
I_102P
C246
I_0.1u
C247
I_0.1u
C248
I_105P
CE2
I_22u
CT30
I_47u
FS5
FB33
I_L-FS_60-25%_3A_0805
I_1.5A_miniSMDM150/24
TPBIAS0
R416
I_54.9 1%
R417
I_54.9 1%
C251
I_0.33u
C250
I_0.01u
PORT1
I_D1x8-WH-1394
SHLD
PWR
TPA +
TPA -
TPB +
TPB -
GND
SHLD
TPA0+
TPA0-
TPB0+
TPB0-
R420
I_54.9 1%
R422
I_54.9 1%
R424
I_4.99K 1%
C254
I_270P
C255
I_102P
R426
I_1M
FS6
FB34
TPBIAS1
R418
I_54.9 1%
R419
I_54.9 1%
C252
I_0.33u
C253
I_0.01u
PORT2
TPA1+
TPA1-
TPB1+
TPB1-
R421
I_54.9 1%
R423
I_54.9 1%
R425
I_4.99K 1%
C257
I_270P
C256
I_102P
R427
I_1M
D25
+12V
I_BRS340-S-CASE403-03
CT31
I_C-ES-47u-16V
C249
I_102p
Standard: remove all part
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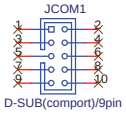
Jumper Setting & Connector Setting

JBAT1	Clear CMOS
1 - 2	Normal *
2 - 3	Clear CMOS



Connector	Description
U2	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIMM1	DDRAM DIMM1
DIMM2	DDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
COM1	Serial Port
LPT1	Parallel Port
JWR1	MODEM RING HEADER
KBMS1	PS/2 Keyboard and mouse
C_FAN1	CPU FAN HEADER
S_FAN1	System FAN HEADER
USB	USB REAR CONNECTOR
JUSB1	USB INTERNAL HEADER
CONN1	ATX Power
JFP1	Front Panel
JPW1	ATX12V Power

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Revision History (Changes from Rev 0A)

Sheet	Desciption
11	Remove R101,R102,R104,R105,R119,R120 and direct short.
12	Add R441,R442 for VBAT leakage reserve.
	Remove R128 and direct connect CPU_GD signal.
	Remove R158 for LG request.
	Change R152 value from 20K to 12K.
13	Remove IR1,CB98,JCI1,R165,R167 for LG request.
17	Add U23,U24,R400,R401 for HSYNC, VSYNC lecel shifters.
21	Change USB1A pin 5 from Gnd to USBVCC.
22	Remove R264 and direct short.
	Remove X4,C117,C118,L20,L17 reserve location.
24	Change AP1 from 3 pin to 2 pin for LG request.
	Remove wake on ring logic Q27,Q29,D12,C189,R327,R329,R331,JWR1 for LG request.
25	Remove R440,R335,R336,R334,CT12 reserve location and change Q32,Q34 package from to252 to to263.
	Remove R439 and direct short and add EC8 for reserve.
26	Remove R373,R374,R364 and direct short and change CB211,CB212 size form 1210 to 1206.
27	Remove U19,U20,Q48,Q57,D20,C223,C224,R380,R381,R382,R383,R436,R437,SEL1,SEL2,J6 for LG request.
	Change JFP1 form 2*9 to 2*4 and remove KBLOCK#,SUS_LED,PWR_LED,FP_RST# signal for LG request.
	Change R387 from 330 ohm to 100 ohm for LG request.
	Remove R384,R388,C227,Q50,R385,Q49,R386,R391,R393,R396,Q52,R394,Q51 for ICHRSMRST# signal.
	Change R390 value from 1K to 4.7K and change pull up from 3VSB to 5VSB.
	Add Q60,R444,R443,R445 and remove CB227 for Fan speed logic.
28	Remove RN66,RN67 and direct short.

Revision History (Changes from Rev 0B)

Sheet	Desciption
5	Remove CN2,CN3 for EMI use.
13	SI/O pin 111 direct connect R445 for LG request.
14	Change dimm1 & dimm2 and pin 181.
26	Change R366 from 1.78K to 3.4K and R368 from 174K to 365K for support FMB2.

Revision History (Changes from Rev 0C)

Sheet	Desciption
5	Add C261 near R16 for SEL48_2 signal for LG EMI request.
24	Stuff C186 for LG EMI request.
27	Direct connect USB signal.

Revision History (Changes from Rev 100)

Sheet	Desciption
23	Change SPDIF for LG request.

Revision History (Changes from Rev 10A)

Sheet	Desciption
13	Add C262 224p cap can reduce CPU_TEMP signal noise

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Document Number: History		
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