MS-6705

Version 200
1/06/2003 Update

INTEL (R) Brookdale-GE Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-GE Chipset:

INTEL MCH (North Bridge) +
INTEL ICH4 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generator -- CY283490C

PCI SOUND -- C-MEDIA CMI8738MX

PCI 1394 -- VIA 6306

Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 4

ERP BOM	Function Description	
601-6705-010	MS-6705 100 845G Standard	LG SPEC. Without 1394.
601-6705-020	MS-6705 100 845G Opt : A	LG SPEC. With 1394.
601-6705-03S	MS-6705 10A 845GE Standard	LG SPEC. Without 1394.
601-6705-04S	MS-6705 10A 845GE Opt : A	LG SPEC. With 1394.

Micro-Star	Title: *MS-6705*	Rev: *200*
Document Number: Cover Sheet		
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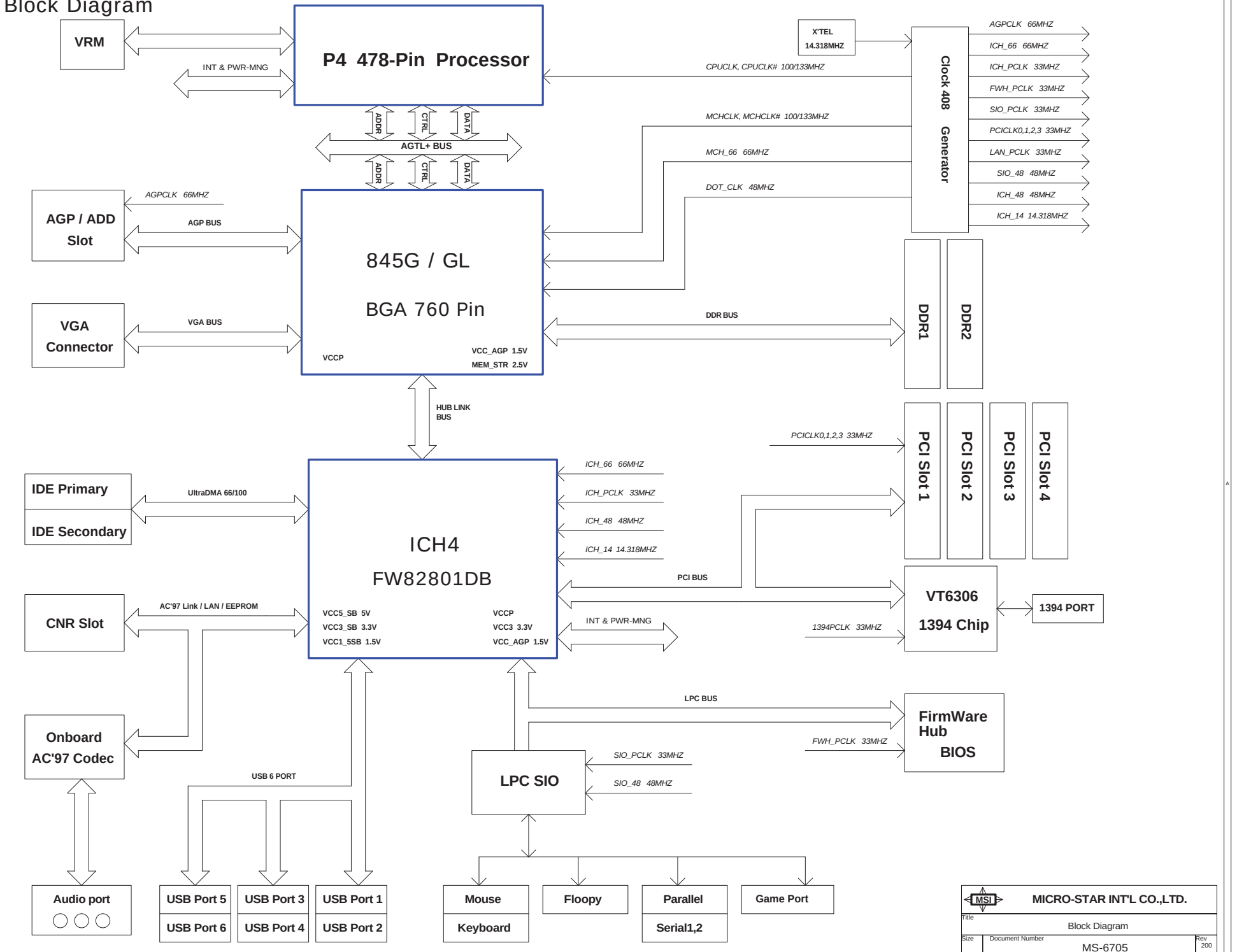
Block Diagram



MSI MICRO-STAR INT'L CO.,LTD.

Title	Block Diagram	
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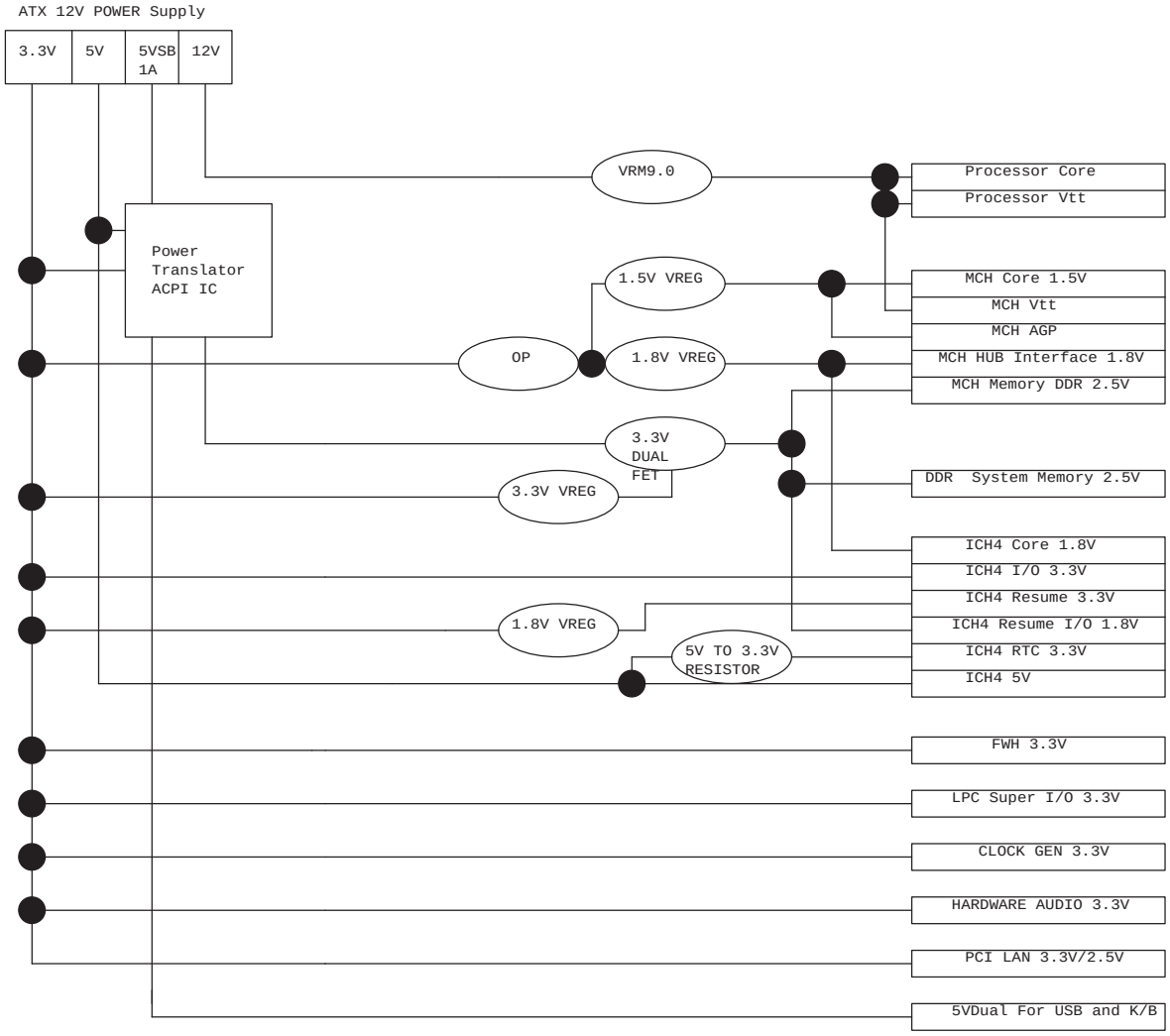
Power Delivery Map



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH4	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY283490C	0	0	0	0	0	0	0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0		0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 2 = 4.0A ---> V_DIMM
S1/S3 STATE --- 200mA * 2 = 400mA ---> V_DIMM
V_DIMM -->400mA*2.5V/3.3V=303mA --> VCC3_SB

NOTE3 --- ICH4

Power	S0	S1	S3/S4/S5
1.8V	132mA	99mA	N/A
VCC_AGP	550mA	266mA	N/A
VCC1_5SB	82mA	52mA	25mA
VCC3(I/O)	528mA	0.76mA	N/A
VCC3_SB	167mA	1mA	0.8mA / N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

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General Purpose I/O Spec.

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A
GPIO 1	I	REQ#5
GPIO 2	I	IRQE#
GPIO 3	I	IRQF#
GPIO 4	I	IRQG#
GPIO 5	I	IRQH#
GPIO 6~7	I	Not Implemented
GPIO 8	I	SIO_PME#
GPIO 9~10	I	Not Implemented
GPIO 11	I	External SMI
GPIO 12~13	I	Not Implemented
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	GNT#5
GPIO 18~21	O	Non Connect
GPIO 22	O/D	Non Connect
GPIO 23	O	BIOS Protect
GPIO 24~27	I/O	Non Connect
GPIO 28	I/O	LAN DISABLED(ICH4)
GPIO 29~47	I/O	Non Connect

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL	CLOCK
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19	PCICLK3
PCI AUDIO	INTF#	AD25	AUDPCLK
PCI 1394	INTH#	AD23	1394PCLK

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Document Number: GPIO Spec.		
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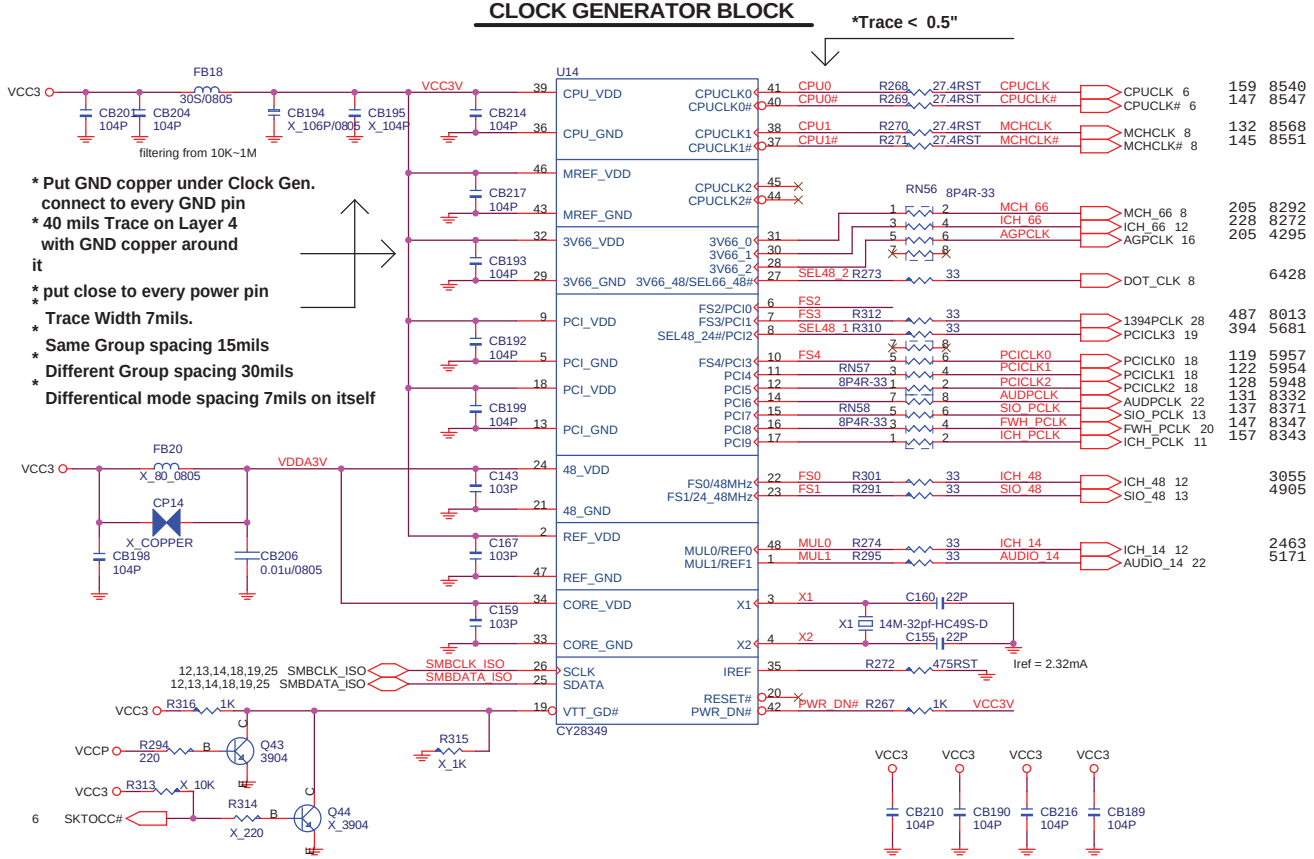
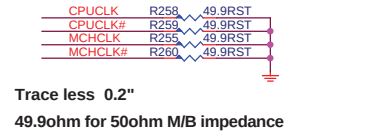
CLOCK GENERATOR BLOCK



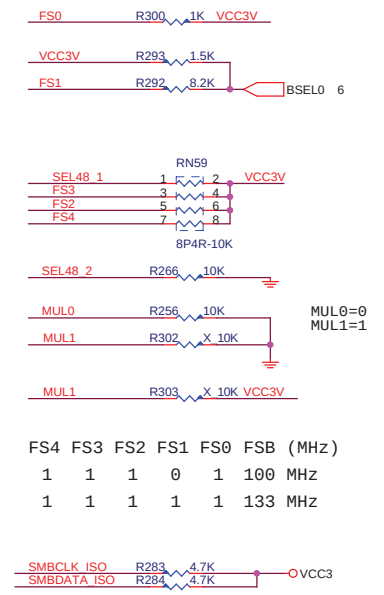
Shut Source Termination Resistors



Trace less 0.2"

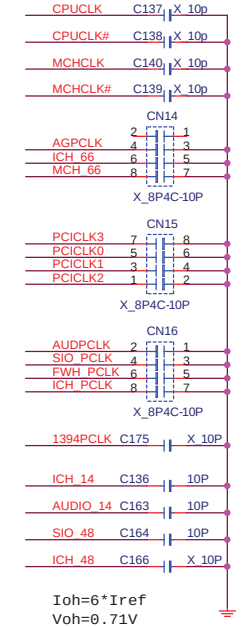
49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



FS4	FS3	FS2	FS1	FS0	FSB (MHz)
1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz

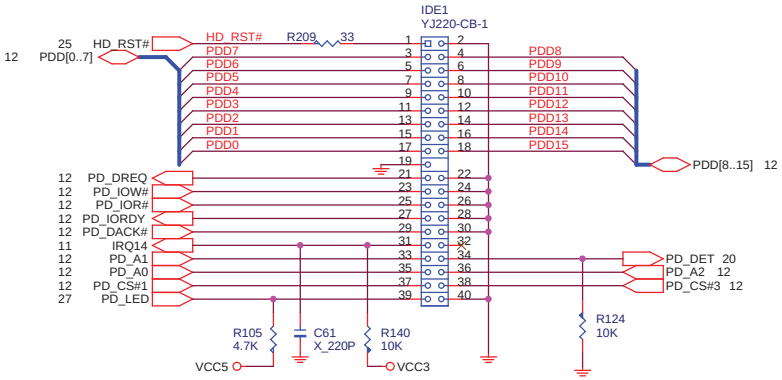
Pull-Down Capacitors



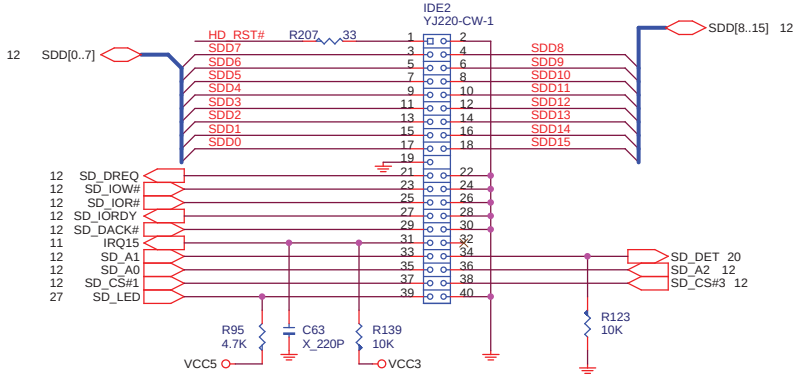
used only for EMI issue

Trace less 0.2"

PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



ATA100 IDE CONNECTORS

* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than 5"

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Document Number: Clock & ATA100 IDE		
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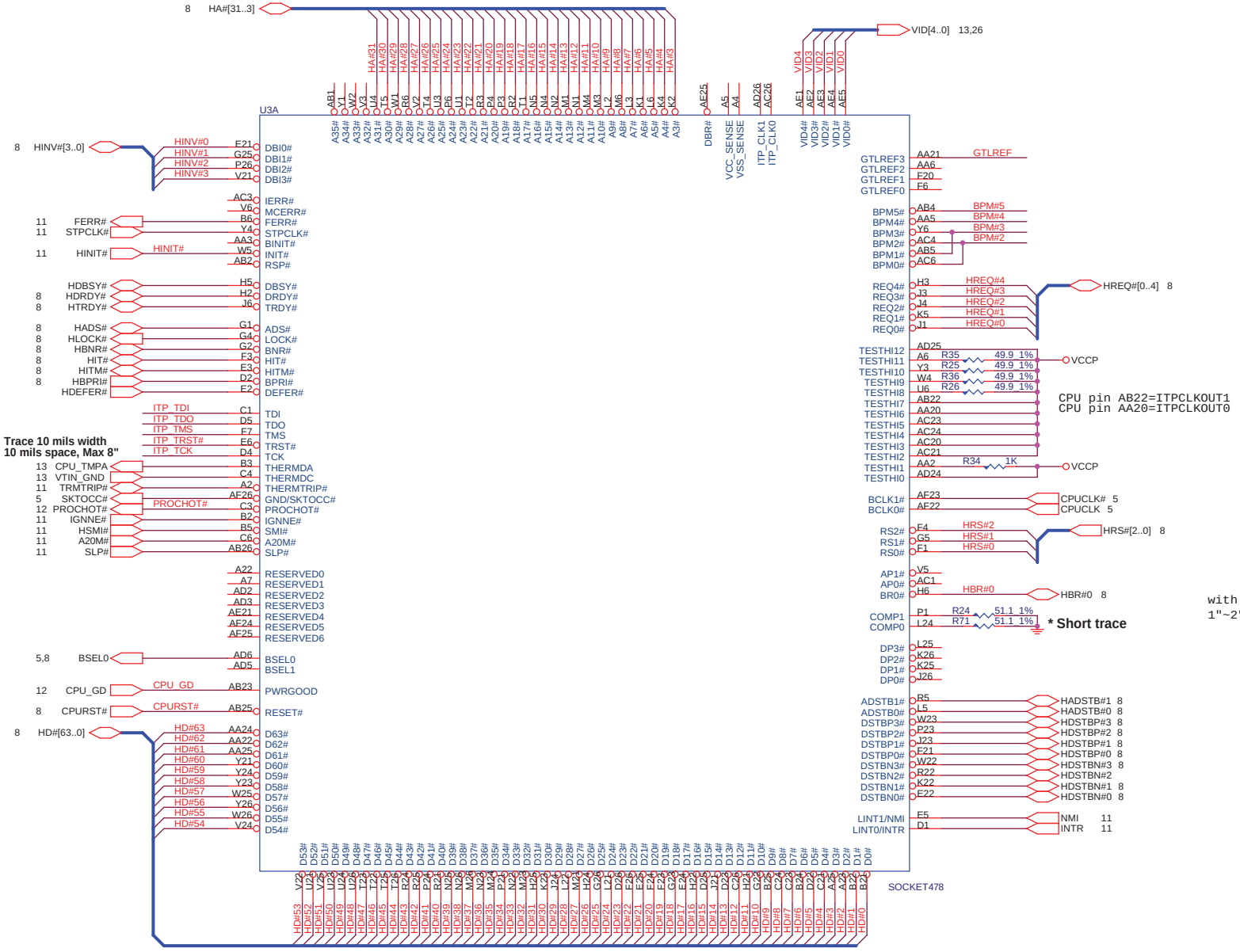
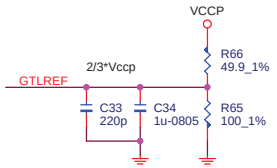
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK

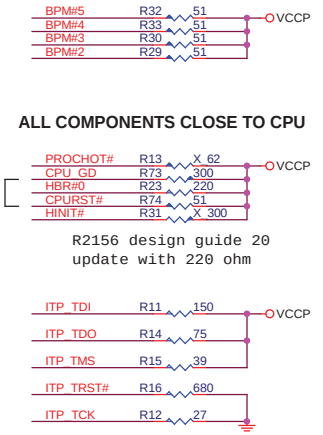


Every pin put one 220pF cap near it.

Trace Width 7mils, Space 10mils.

Keep the voltage divider within 1.5" of the GETREF pin.

CPU STRAPPING RESISTORS



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Title	mPGA478-B INTEL CPU SOCKET Part1		
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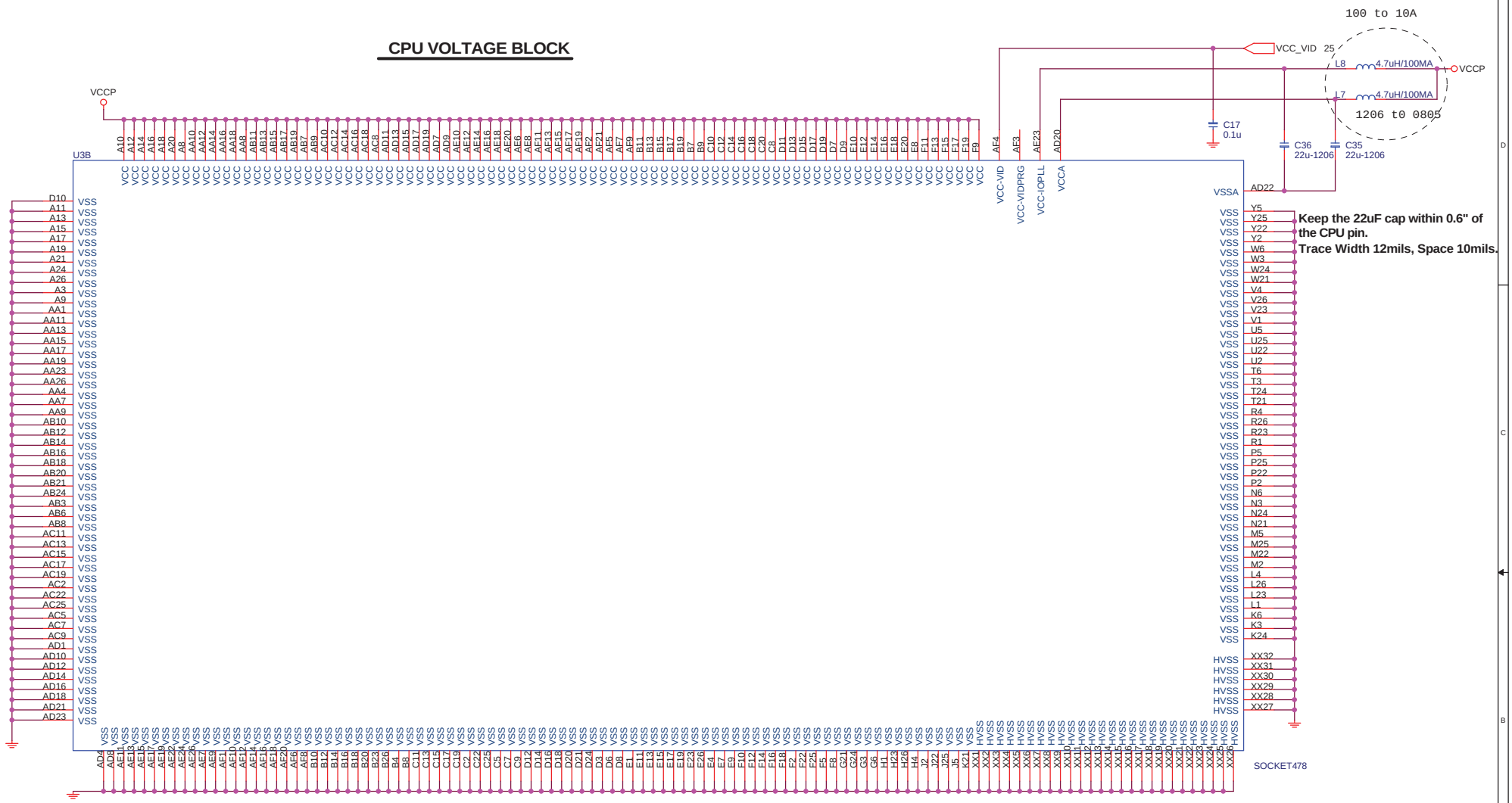
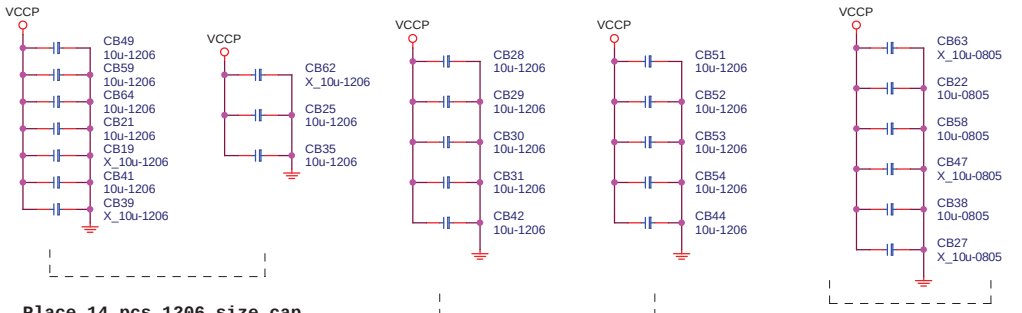
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS

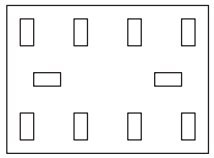


Place 14 pcs 1206 size cap north side of processor

PLACE CAPS WITHIN CPU CAVITY

Place these caps on south side of processor

Within CPU Cavity Solder Side



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	mPGA478-B INTEL CPU Part2	
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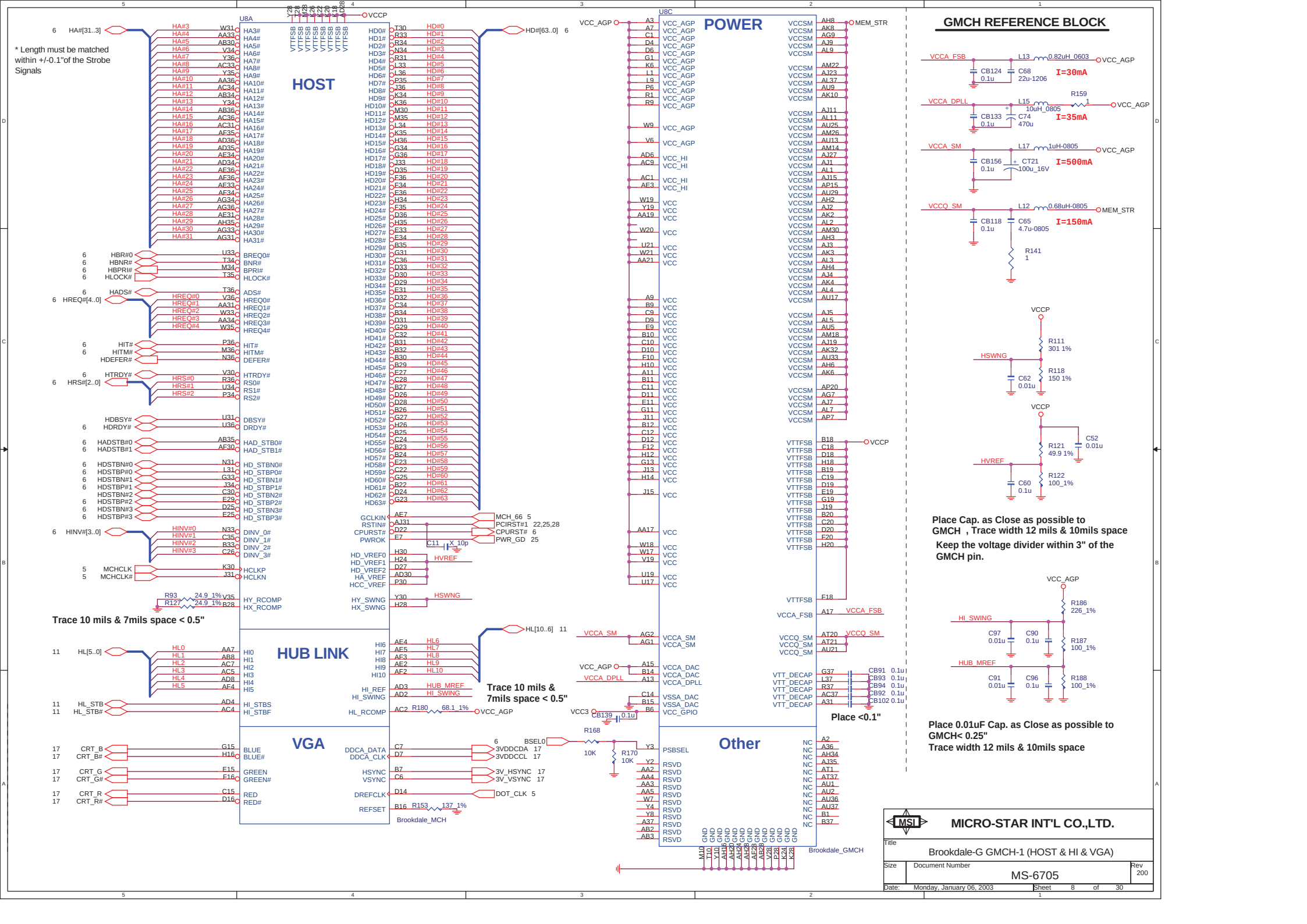
HOST
HUB LINK
VGA
POWER
Other
U8A
U8C
* Length must be matched within +/-0.1"of the Strobe Signals
Trace 10 mils & 7mils space < 0.5"
Trace 10 mils & 7mils space < 0.5"
Place <0.1"
Brookdale_MCH
Brookdale_GMCH
GMCH REFERENCE BLOCK
I=30mA
I=35mA
I=500mA
I=150mA
Place Cap. as Close as possible to GMCH , Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the GMCH pin.
Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space
MICRO-STAR INT'L CO.,LTD.
Brookdale-G GMCH-1 (HOST & HI & VGA)
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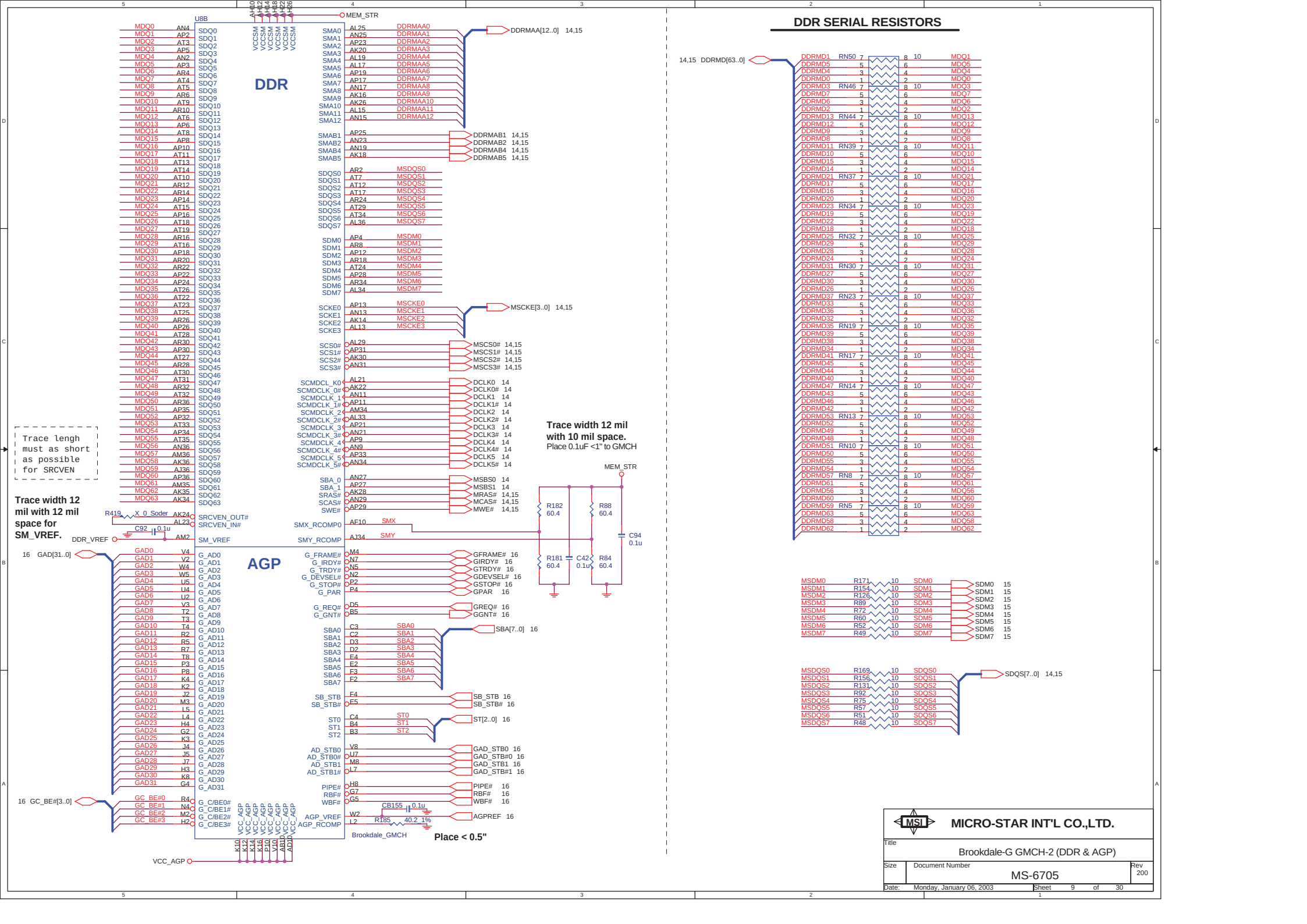
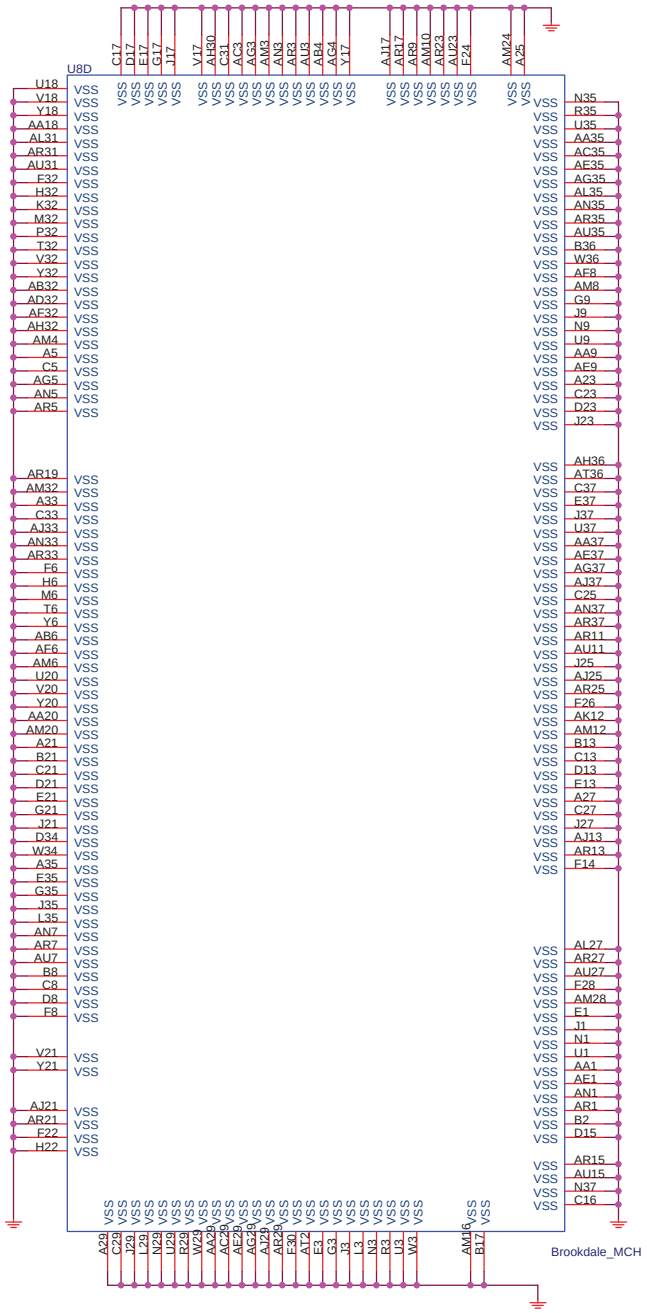
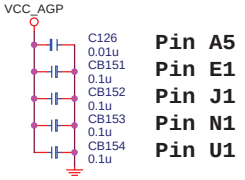

DDR SERIAL RESISTORS
DDR
AGP
U8B
MEM_STR
Trace lengh must as short as possible for SRCVEN
Trace width 12 mil with 12 mil space for SM_VREF.
Trace width 12 mil with 10 mil space.
Place 0.1uF <1" to GMCH
Place < 0.5"
Brookdale_GMCH
MICRO-STAR INT'L CO.,LTD.
Brookdale-G GMCH-2 (DDR & AGP)
MS-6705
Monday, January 06, 2003



GMCH DECOUPLING CAPACITOR

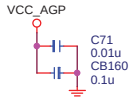


Pin A5
Pin E1
Pin J1
Pin N1
Pin U1

Place decoupling cap close to GMCH AGP Interface < 0.1"

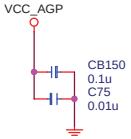
Pin AA1
Pin AE1

Place decoupling cap close to GMCH Hub-Link Interface< 0.1"

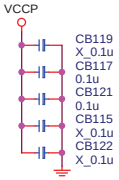


Pin B14
Pin A15

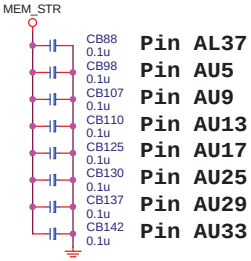
Place decoupling cap close to GMCH DAC Interface< 0.1"



Place decoupling cap close to GMCH Core Logic Interface < 0.1"

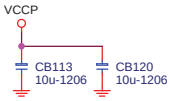


Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor

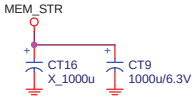


Pin AL37
Pin AU5
Pin AU9
Pin AU13
Pin AU17
Pin AU25
Pin AU29
Pin AU33

Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width



Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot

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Title	Broodale GMCH(VSS)	
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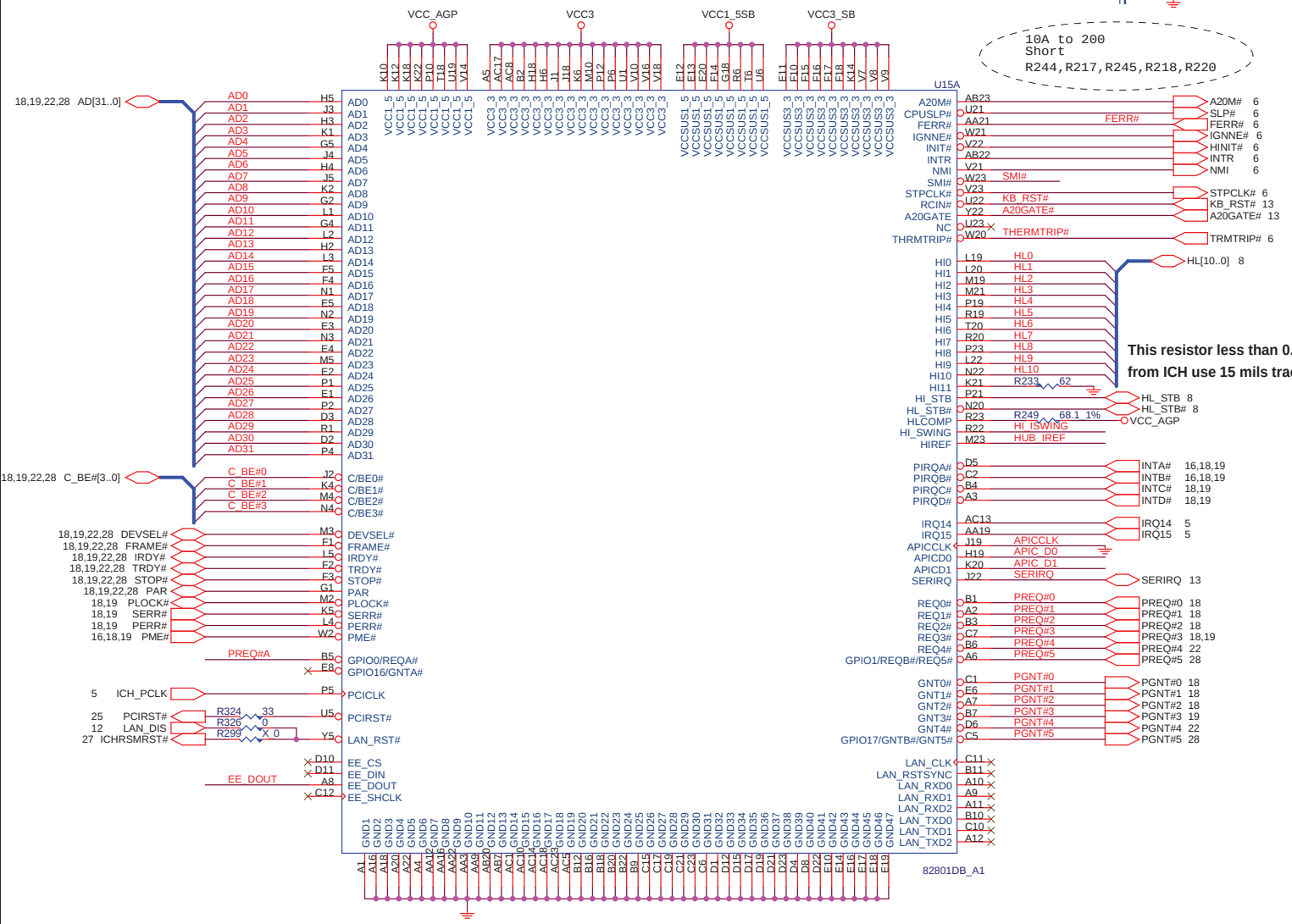
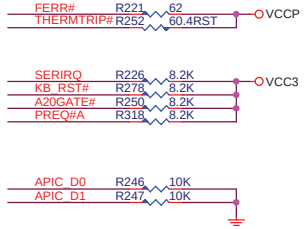
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



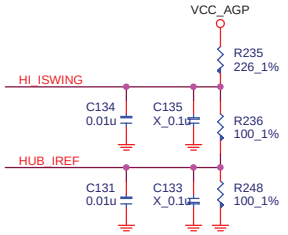
ICH4 STRAPPING RESISTORS

Reserved pull-down resistor for ICH4 reserved function straps.

ICH4 PULL-UP/DOWN RESISTORS



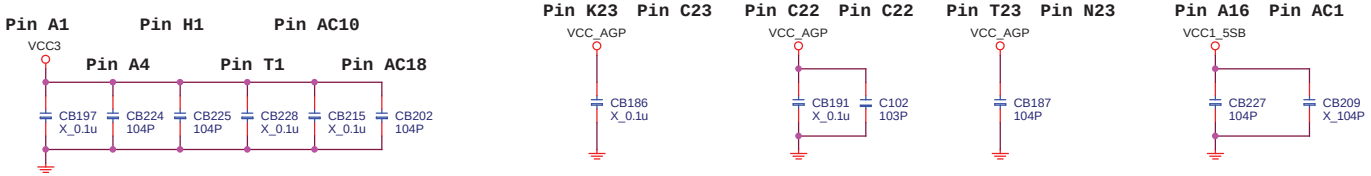
ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



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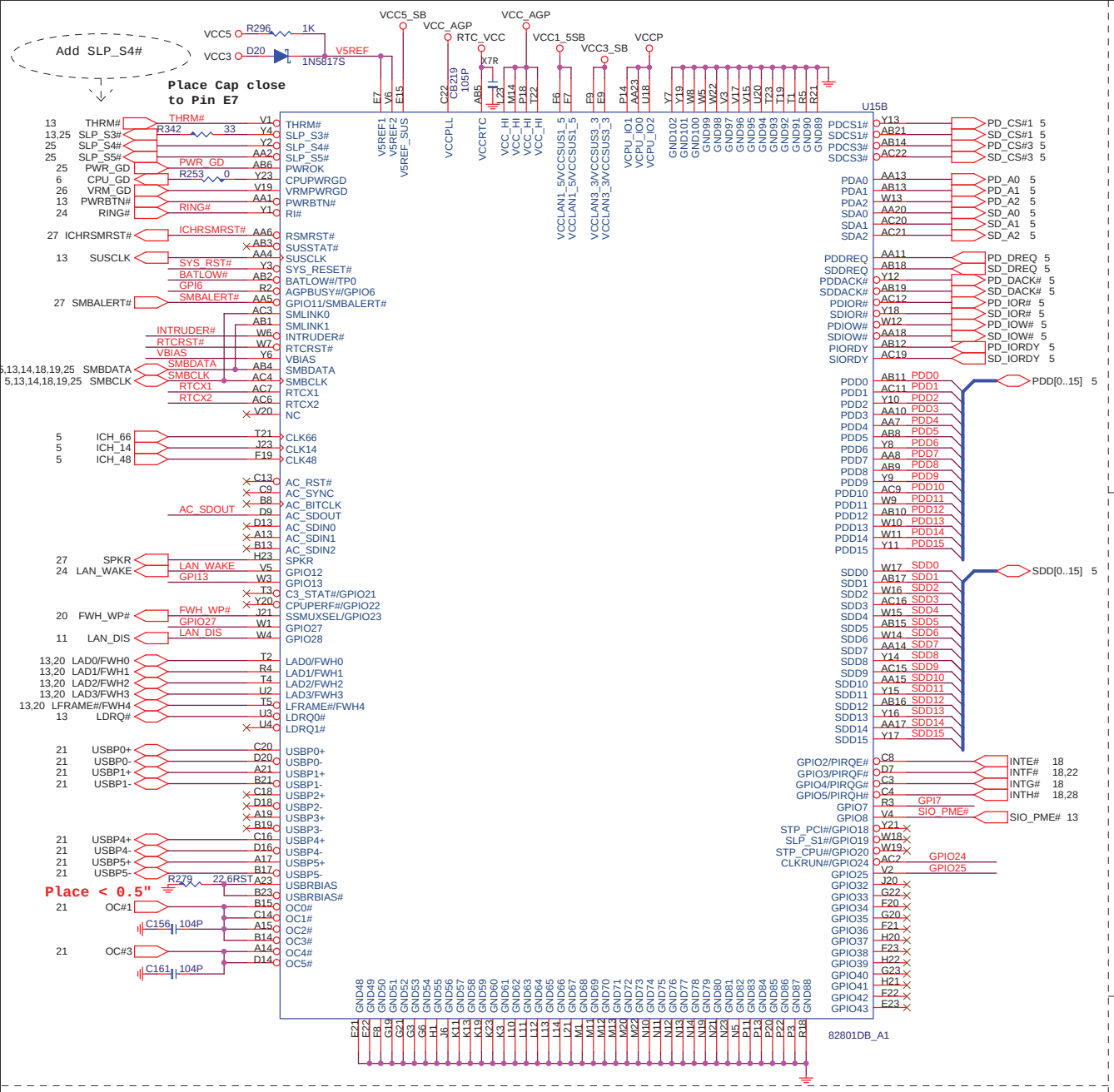
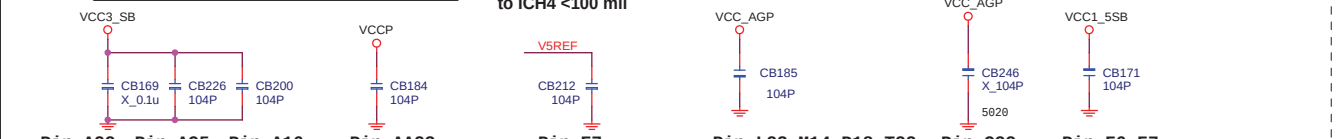
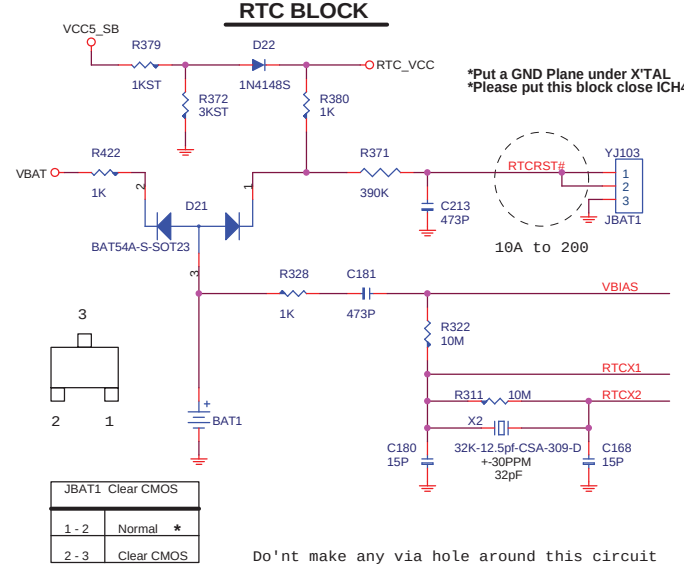


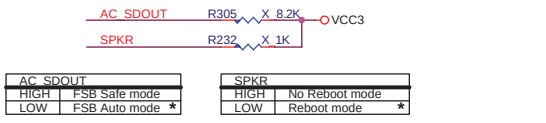
ICH4 DECOUPLING CAPACITOR



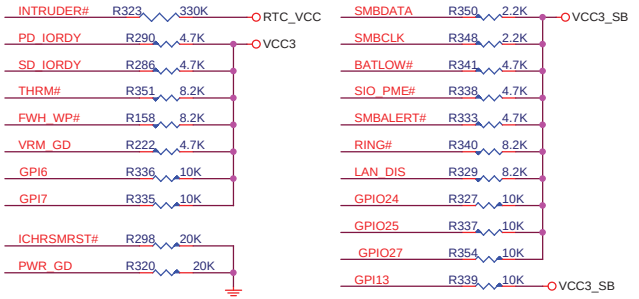
RTC BLOCK



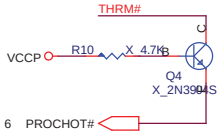
ICH4 STRAPPING RESISTORS



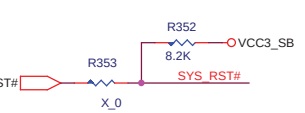
ICH4 PULL-UP/DOWN RESISTORS



PROCHOT BLOCK



SYSTEM RESET



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Document Number: ICH4 ASIC/RTC/AC'97/GPIO/LPC/USB/IDE			
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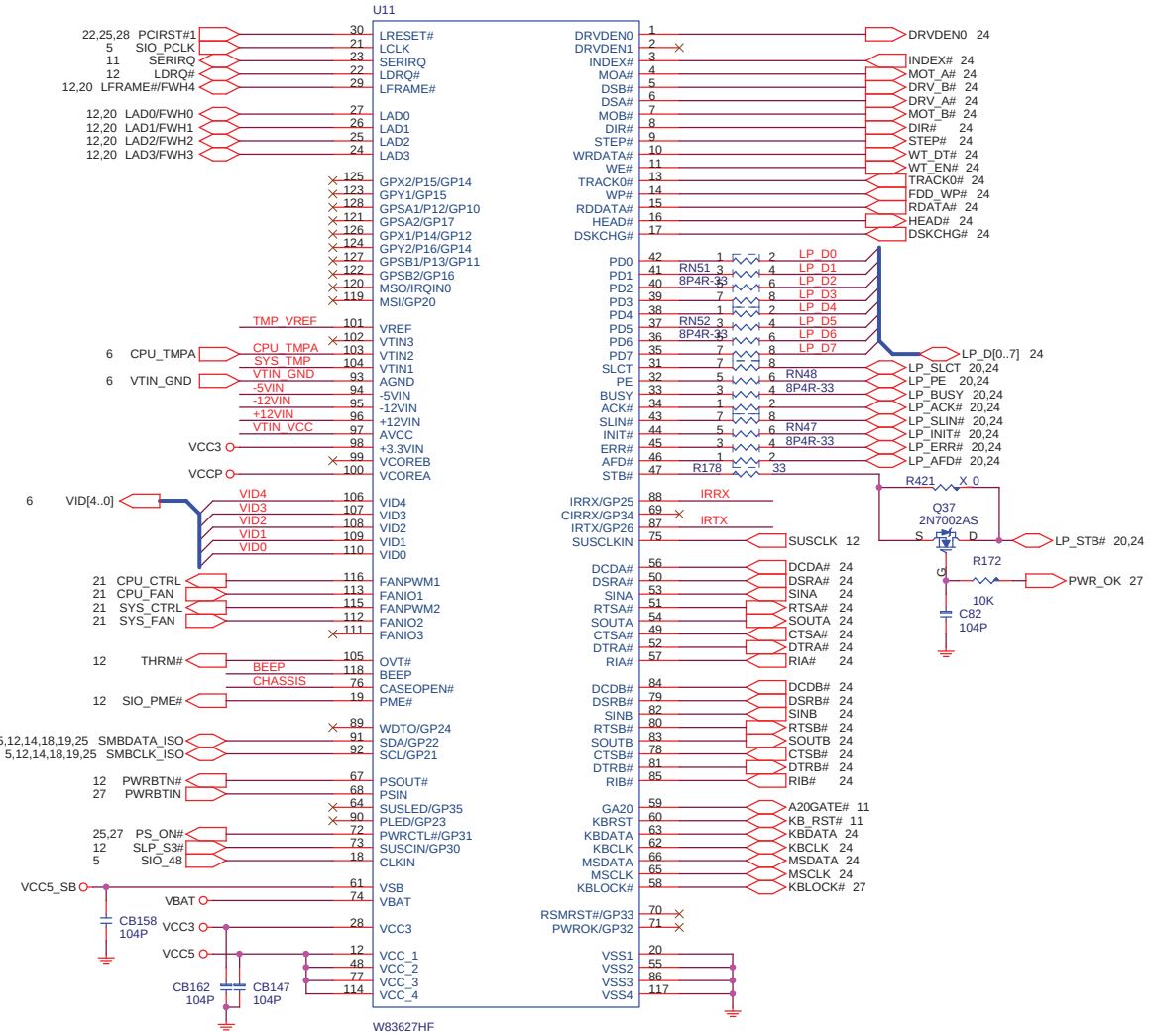
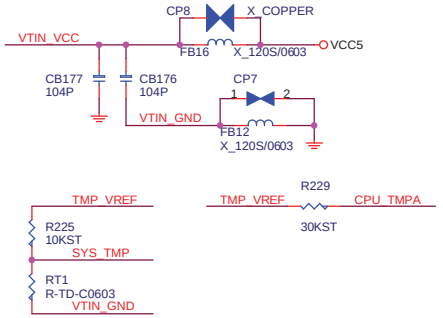
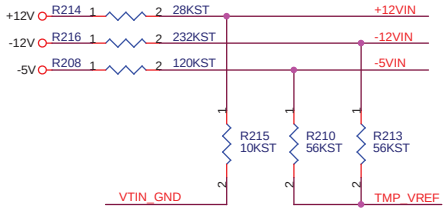
LPC SUPER I/O W83627HF



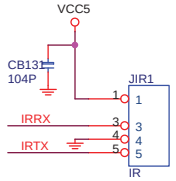
THERMAL RESISTOR BLOCK



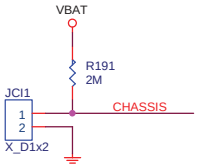
NOTE: LOCATE CLOSE STATUS PANEL



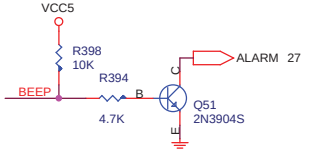
IR HEADER



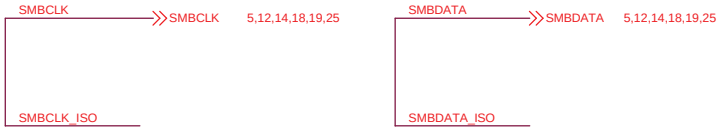
Chasis Intrusion Header



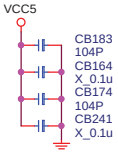
SPEAKER BLOCK



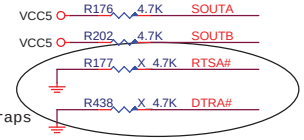
SMBus Isolation



LPC I/O DECOUPLING CAPACITORS



SUPER I/O STRAPPING RESISTOR

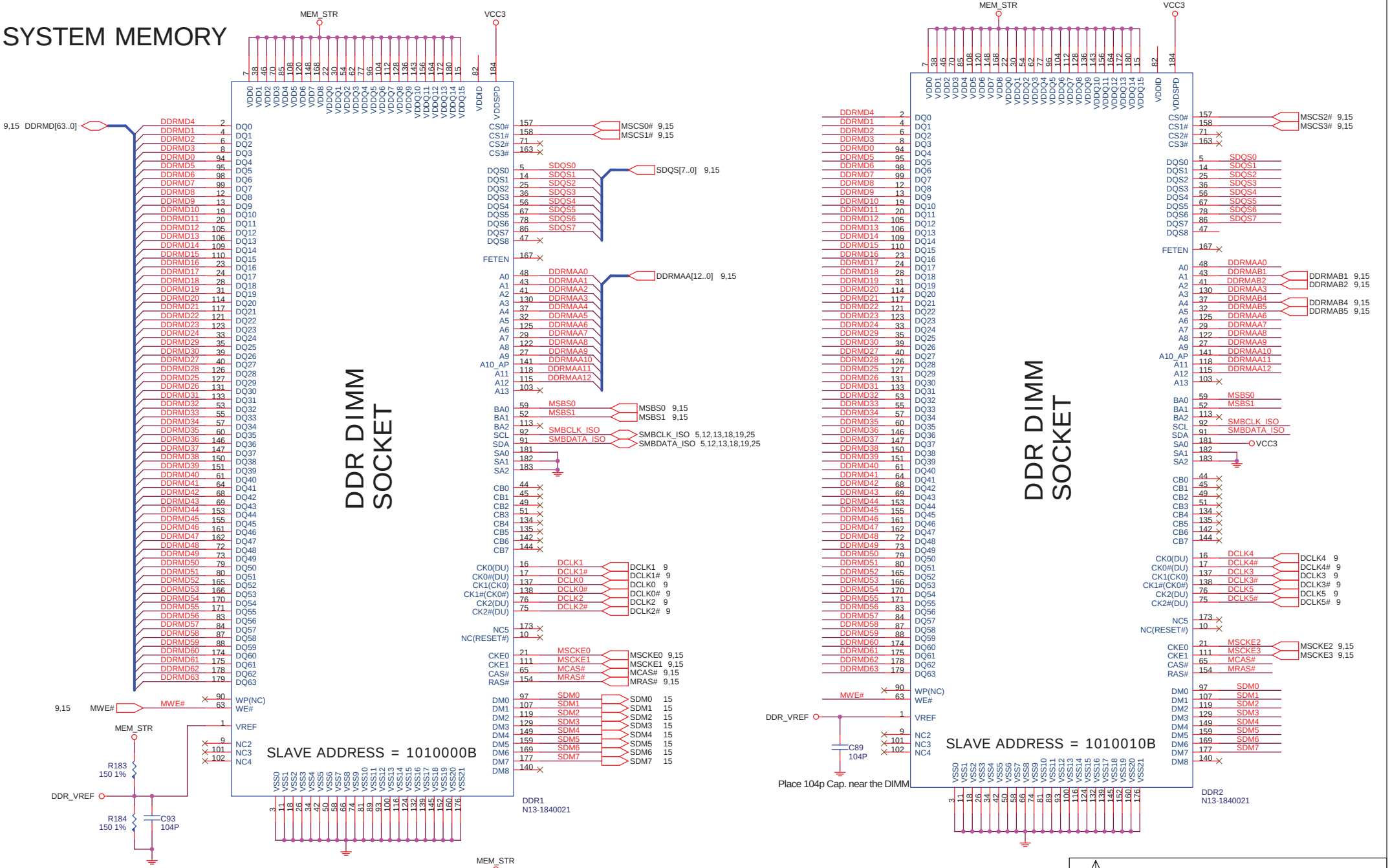


100 to 10A
reserved for SIO straps

SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

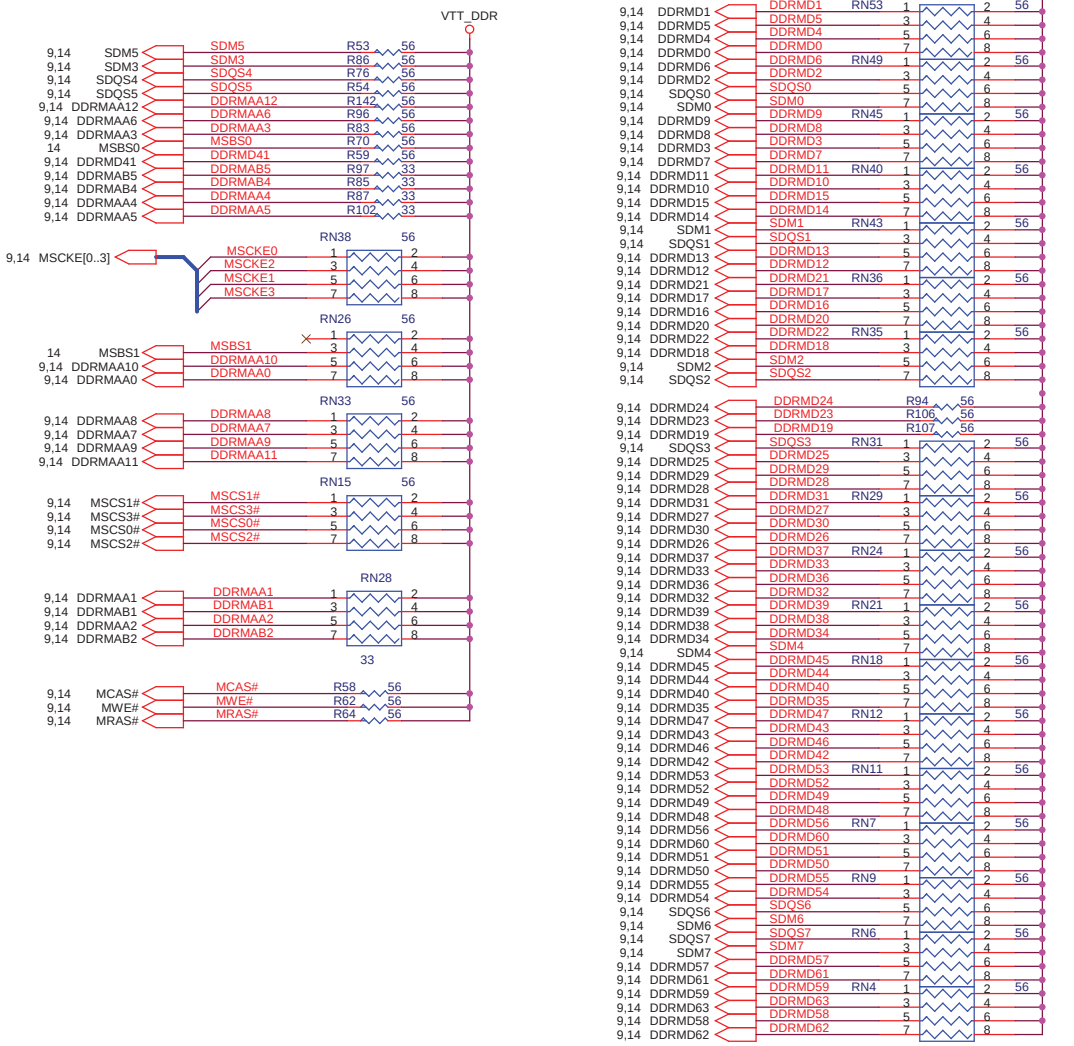
Micro-Star	Title: MS-6705	Rev: 200
Document Number: LPC I/O W83627HF		
Last Revision Date: Monday, January 06, 2003	Sheet 13 of 30	

SYSTEM MEMORY

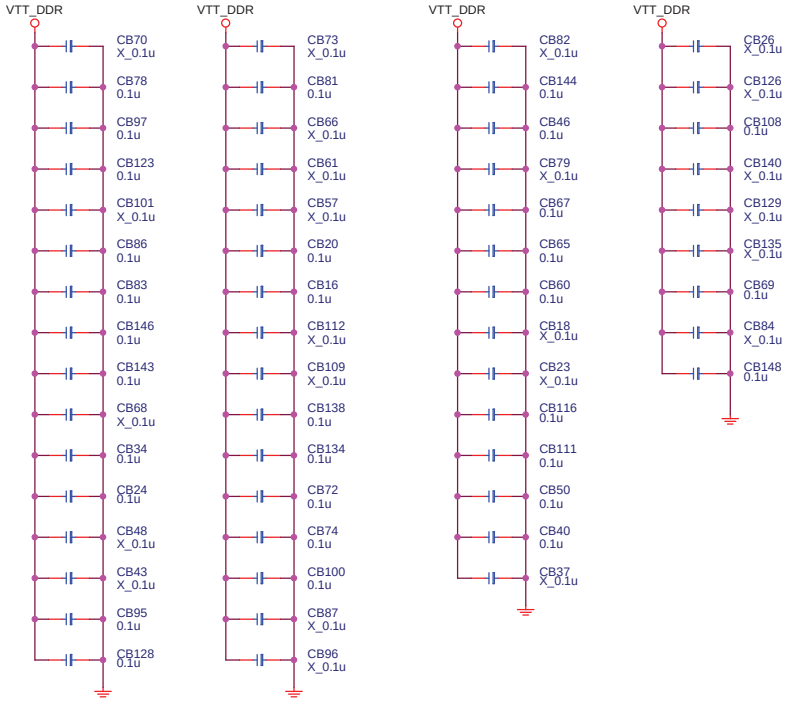


MSI	MICRO-STAR INT'L CO.,LTD.
Title	DDR DIMM1&2
Size	Document Number: MS-6705
Rev	200
Date:	Monday, January 06, 2003
Sheet	14 of 30

DDR TERMINATORS

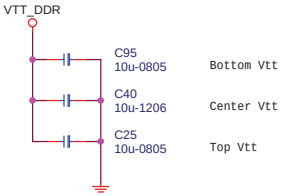


DDR Decouping Caps



Total 110 signal, need 55 pcs decoupling.

Place for VTT_DDR island



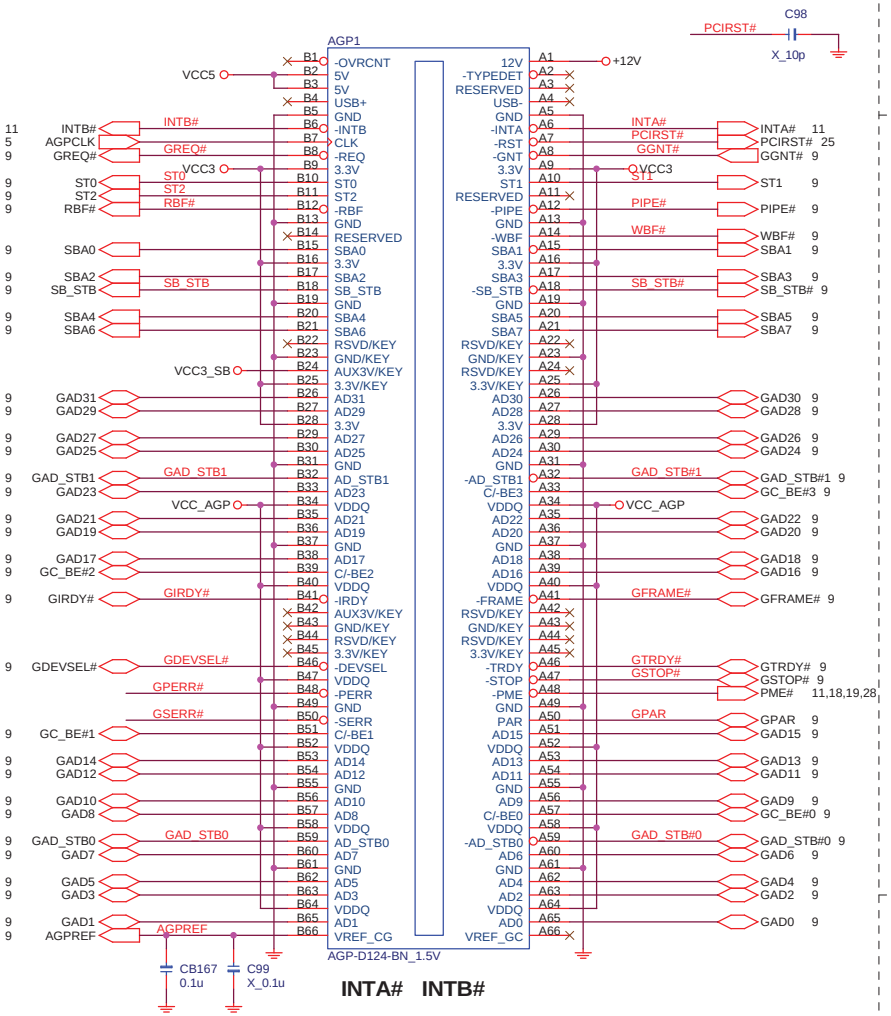
Place at the end of the VTT_DDR island

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	DDR Terminator Resistor	
Size	Document Number MS-6705	Rev 200
Date: Monday, January 06, 2003	Sheet 15 of 30	

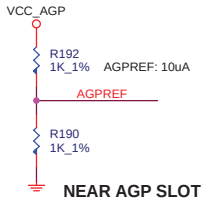
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



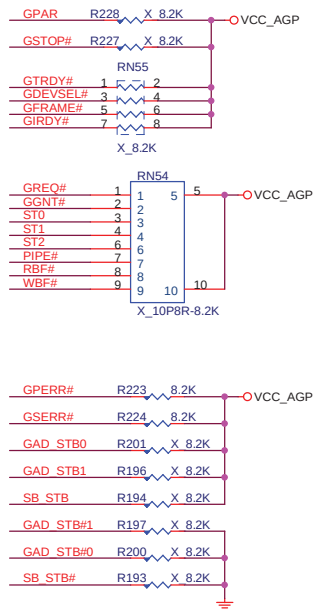
INTA# INTB#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

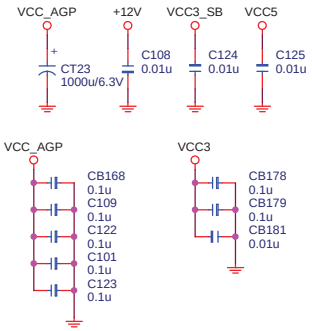
AGP TERMINATION RESISTORS



LESS 100MILS STUB TRACE LENGTH FOR 2/4X
LESS 500MIL FOR 1X MUST BE FOLLOWING.

Place these resistors between AGP slot & GMCH

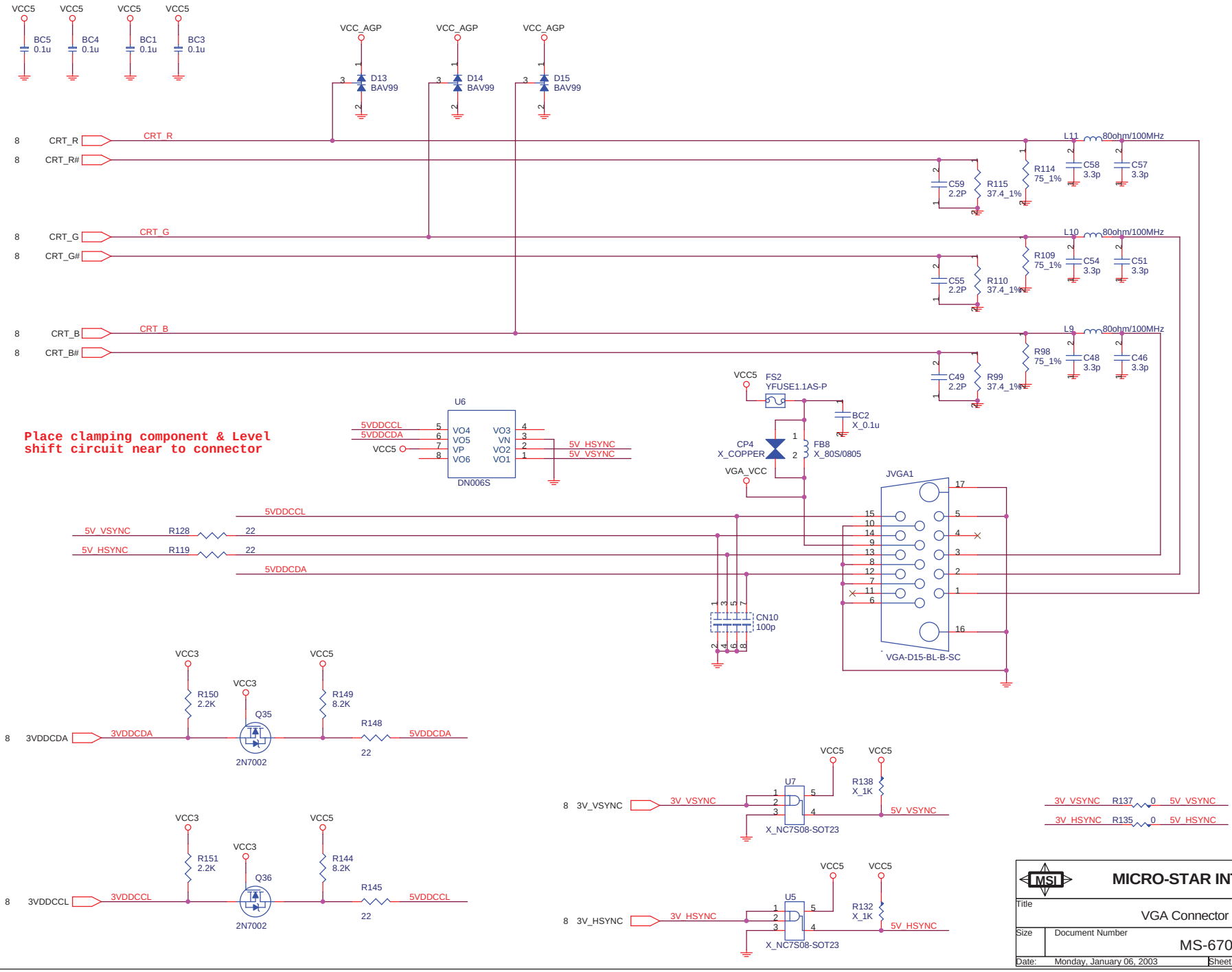
AGP SLOT DECOUPLING CAPACITORS



MSI **MICRO-STAR INT'L CO.,LTD.**

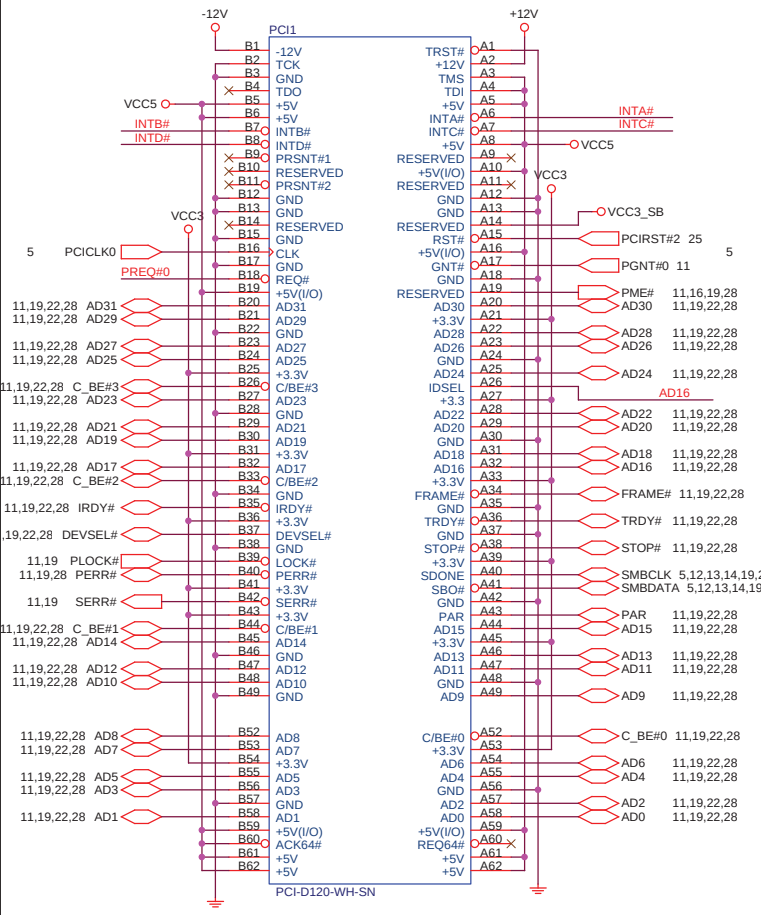
Title	AGP SLOT	
Size	Document Number: MS-6705	Rev: 200
Date: Monday, January 06, 2003	Sheet 16 of 30	

Video Connector



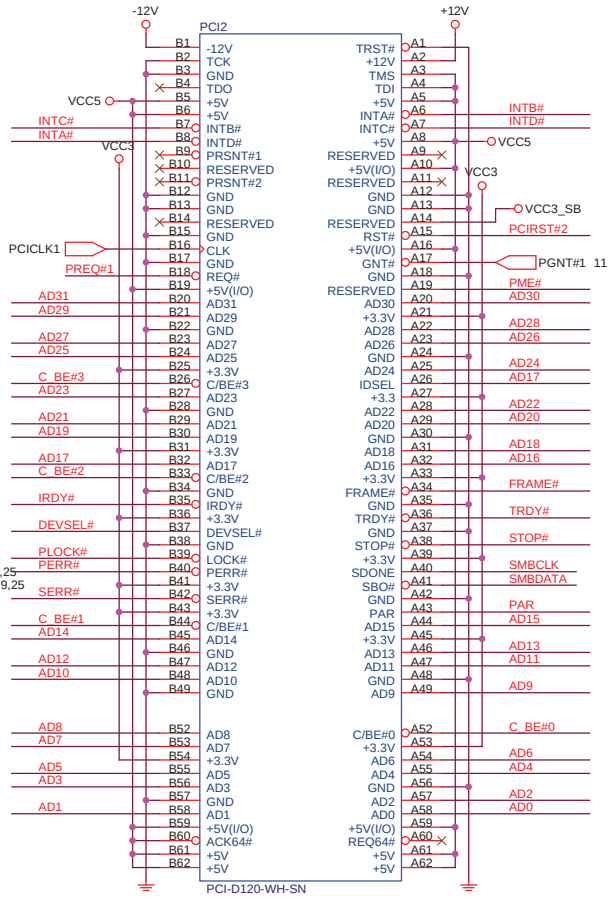
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	VGA Connector	
Size	Document Number MS-6705	Rev 200
Date: Monday, January 06, 2003	Sheet 17 of 30	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



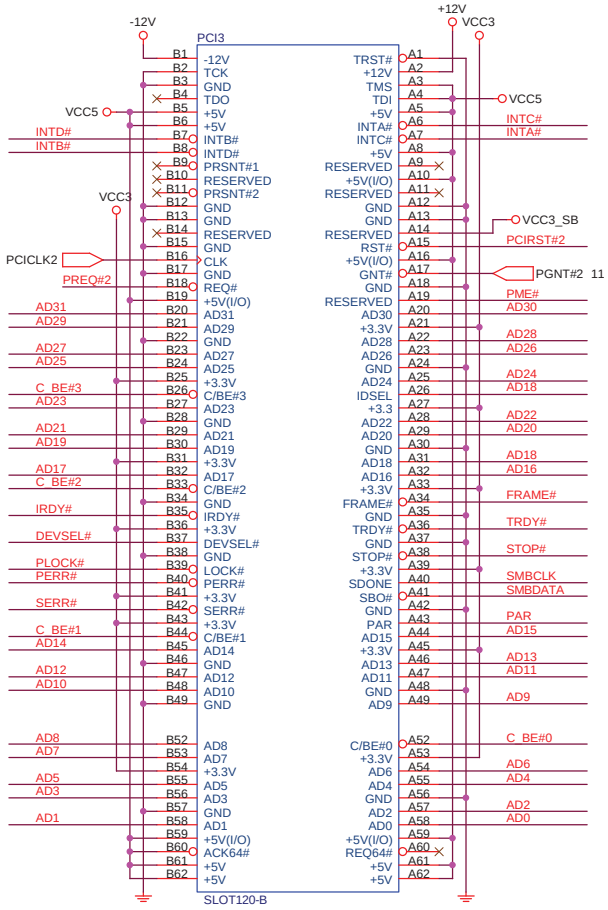
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



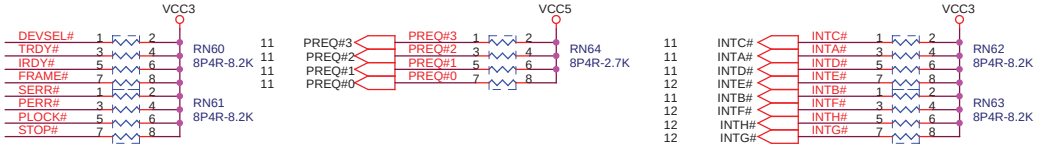
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

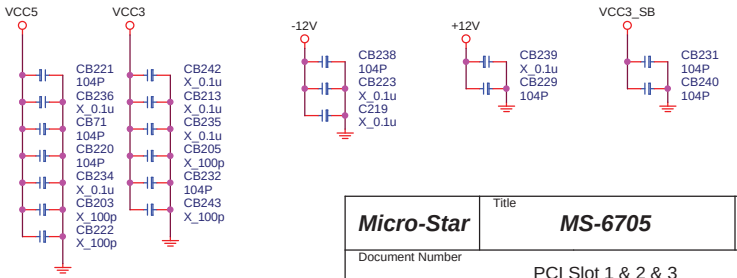


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS

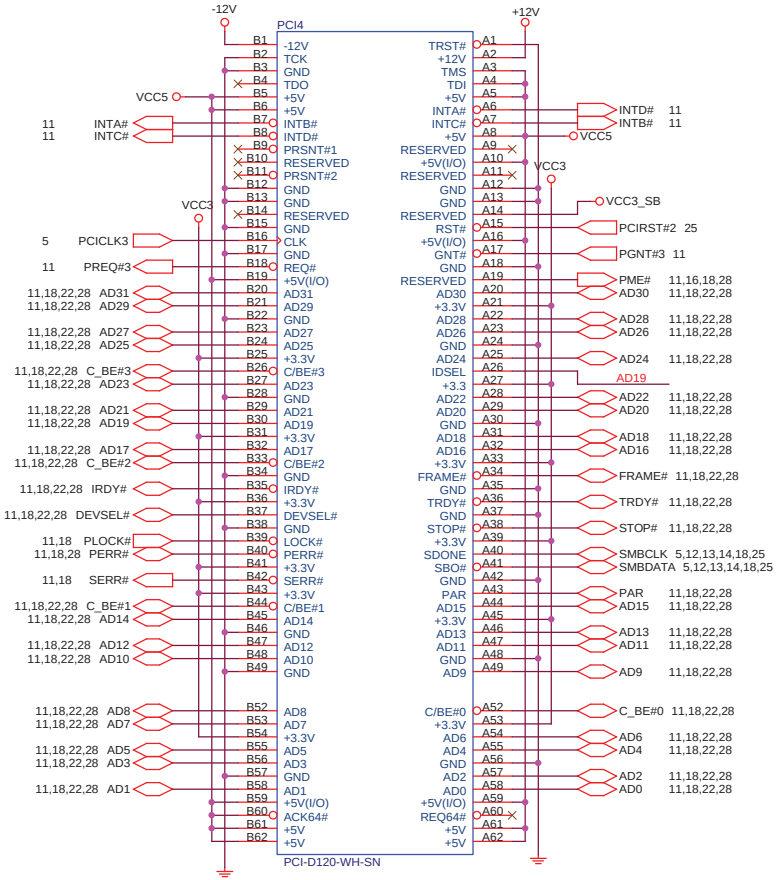


PCI SLOT DECOUPLING CAPACITORS



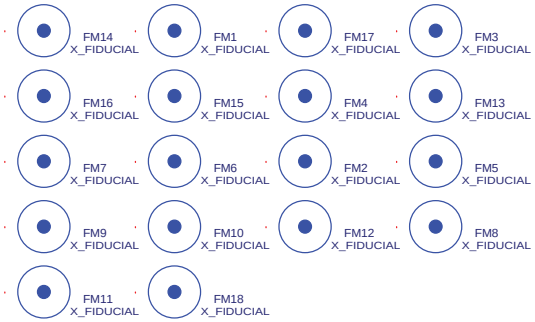
Micro-Star	Title: MS-6705	Rev: 200
Document Number: PCI Slot 1 & 2 & 3		
Last Revision Date: Monday, January 06, 2003	Sheet 18 of 30	

PCI SLOT 4 (PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER = PREQ3
INTD#

PCB Fiducials



Micro-Star	Title: MS-6705	Rev: 200
Document Number: AGP Slot & PCI SLOT4		
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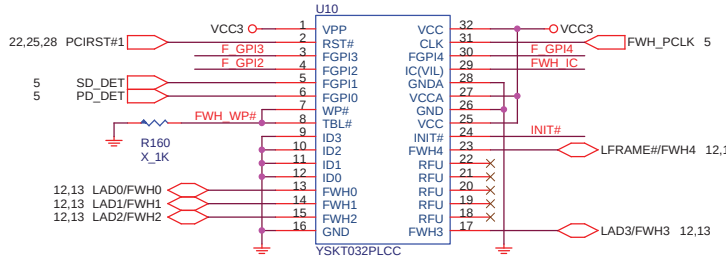
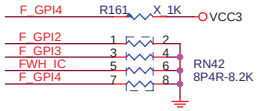
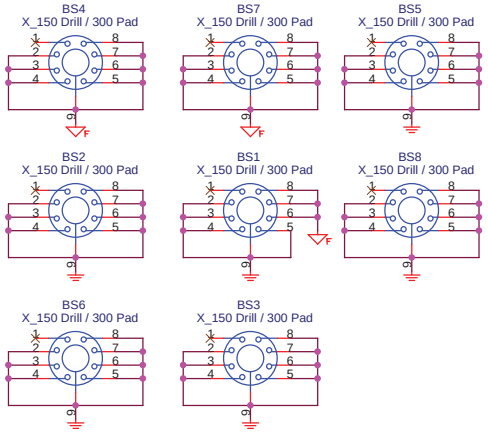
Firware Hub (FWH)



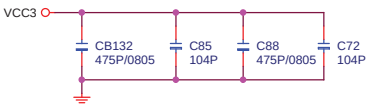
FWH RESISTORS



PCB Mounting Holes

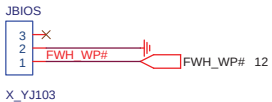


FWH DECOUPLING CAPACITORS



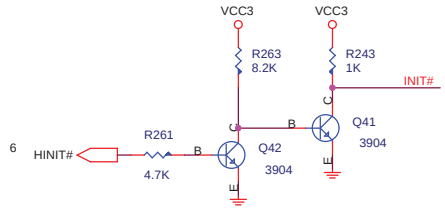
Place Cap. as Close to FWH< 350 mil

FWH write protect



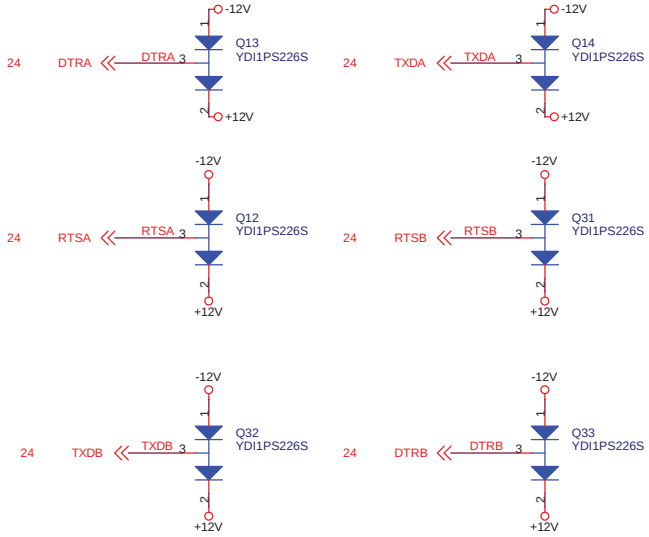
JBIOS BIOS Update	
1-2	Locked
2-3	Unlocked *

FWH INIT Signal Voltage Translation Block

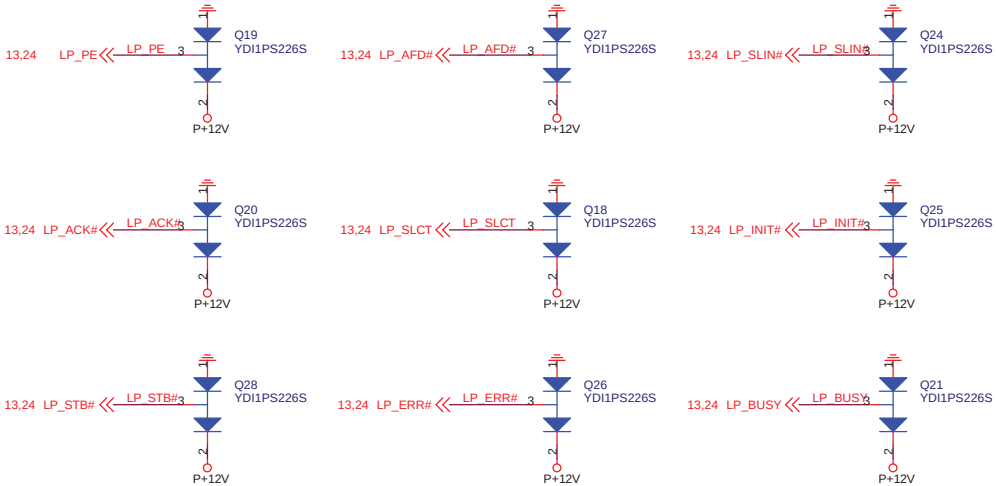


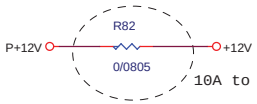
SIMULATION TRACE

Serial port protection diode



Perallal port protection diode





Micro-Star	Title: MS-6705	Rev: 200
Document Number: FWH & protection diode		
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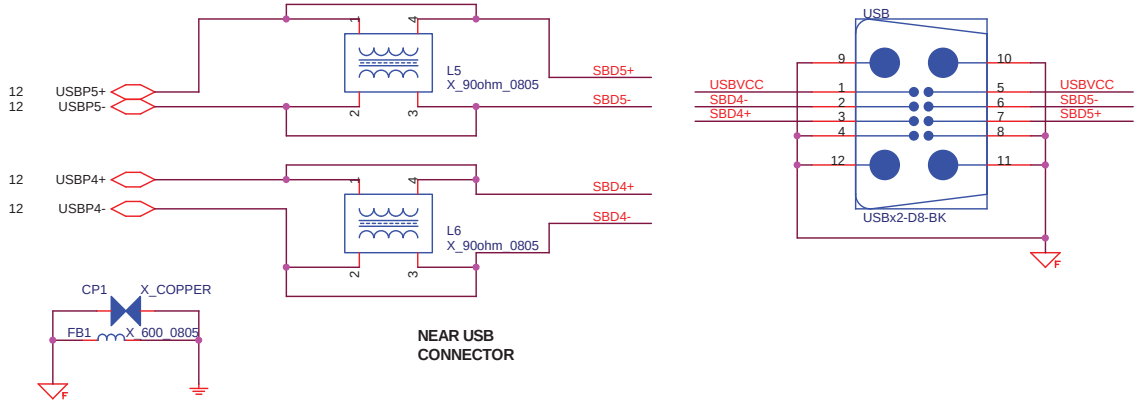
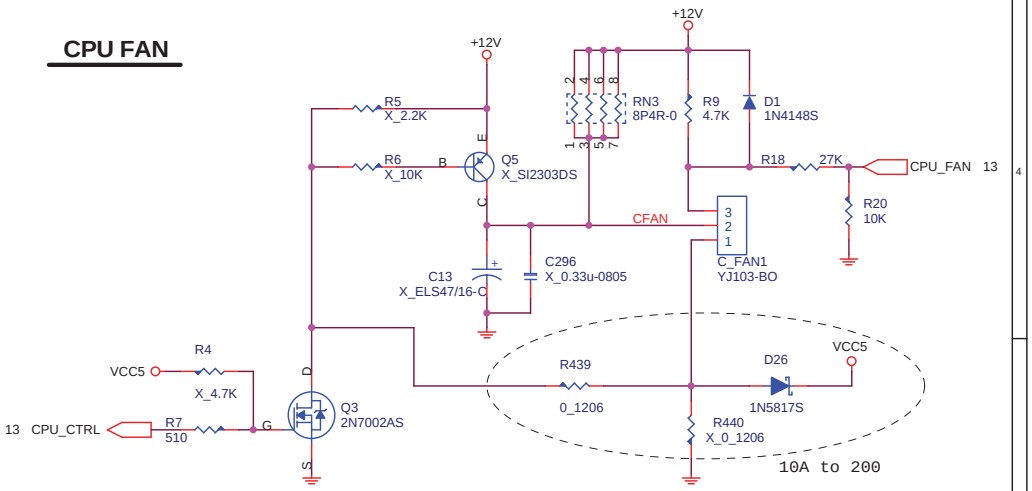
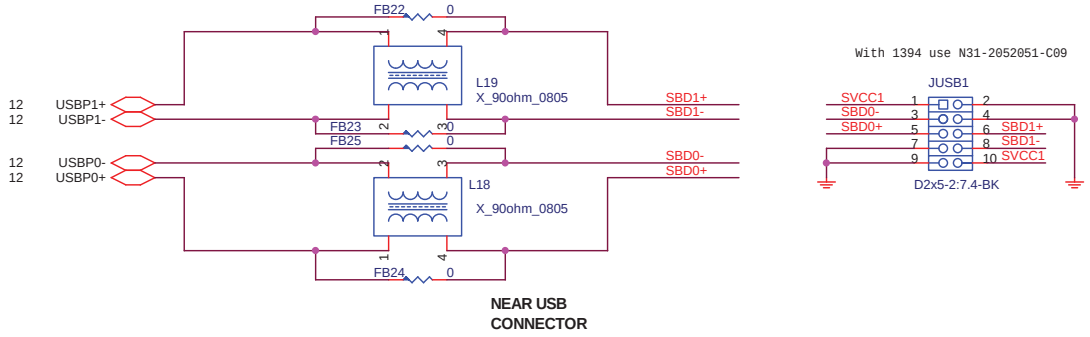
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



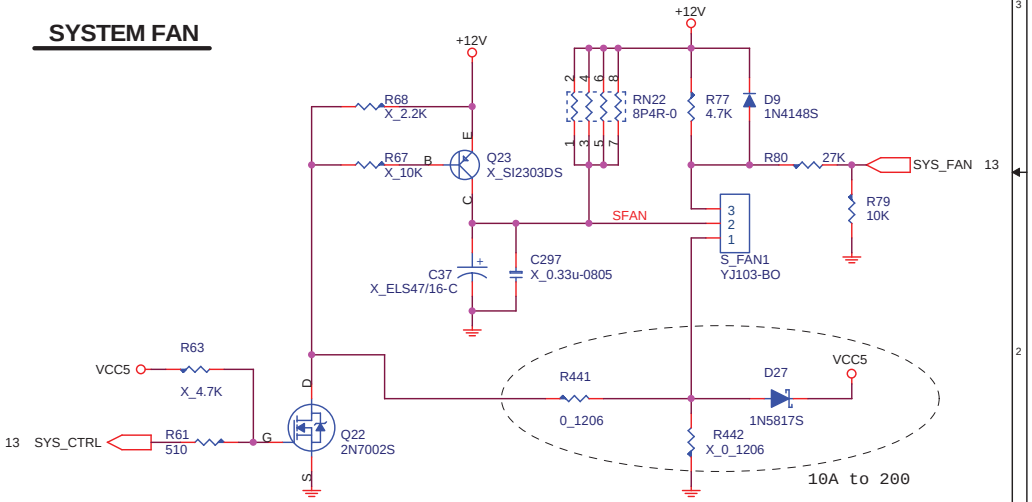
CPU FAN



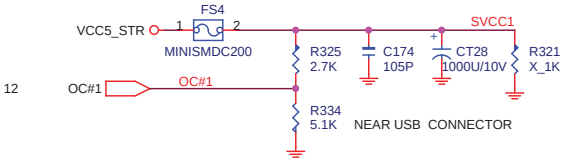
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



SYSTEM FAN

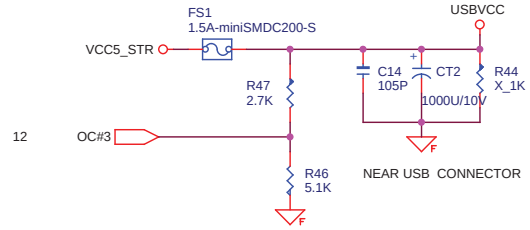


POWER CIRCUIT FOR USB PORT 0,1



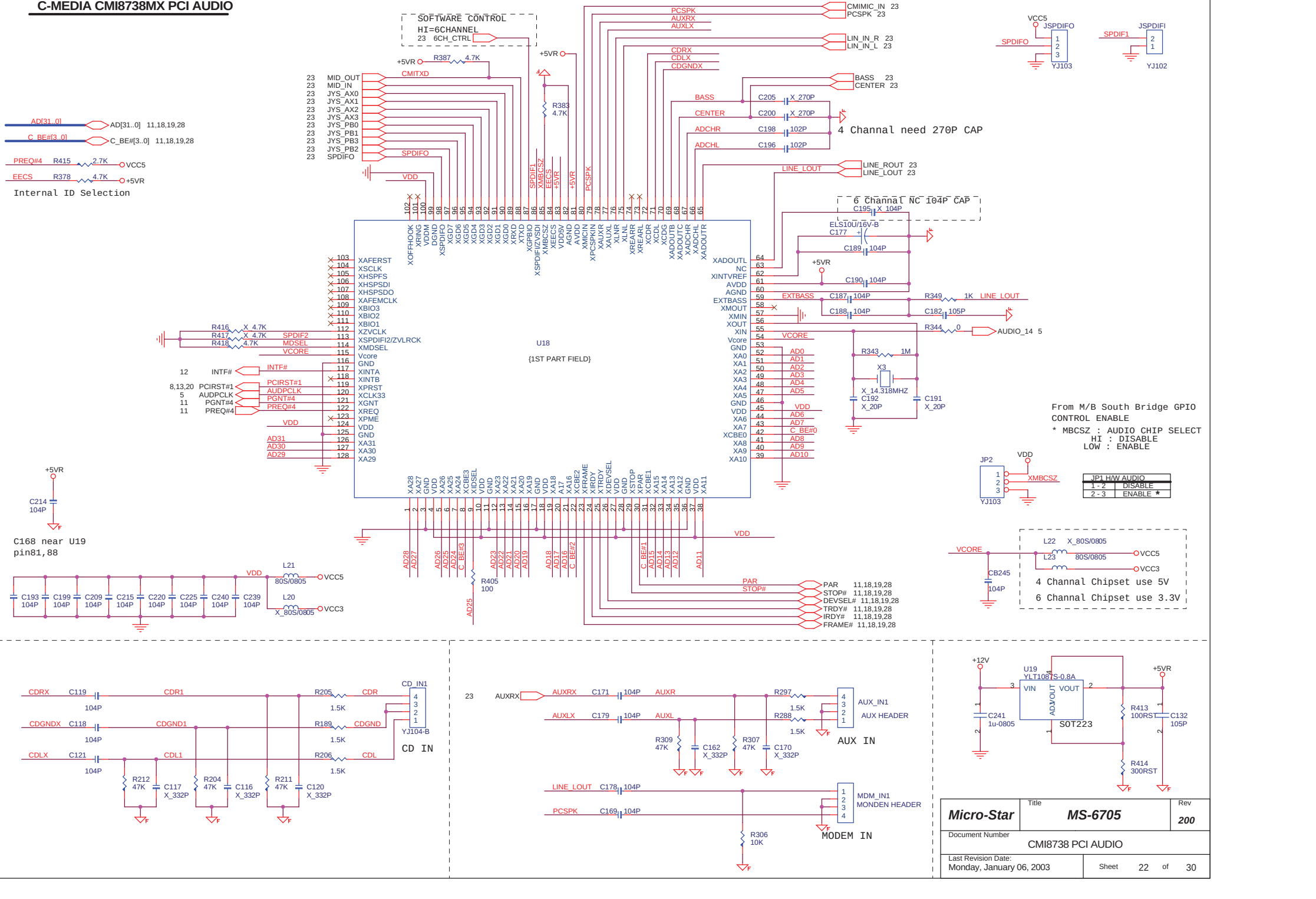
* USB Trace width : 7.5 mils
* USB Trace Spacing : 20 mils
* Differential USB Signlas Trace, Spacing : 18 mils
* USB Power Trace must be 40mils width

POWER CIRCUIT FOR USB PORT 4,5

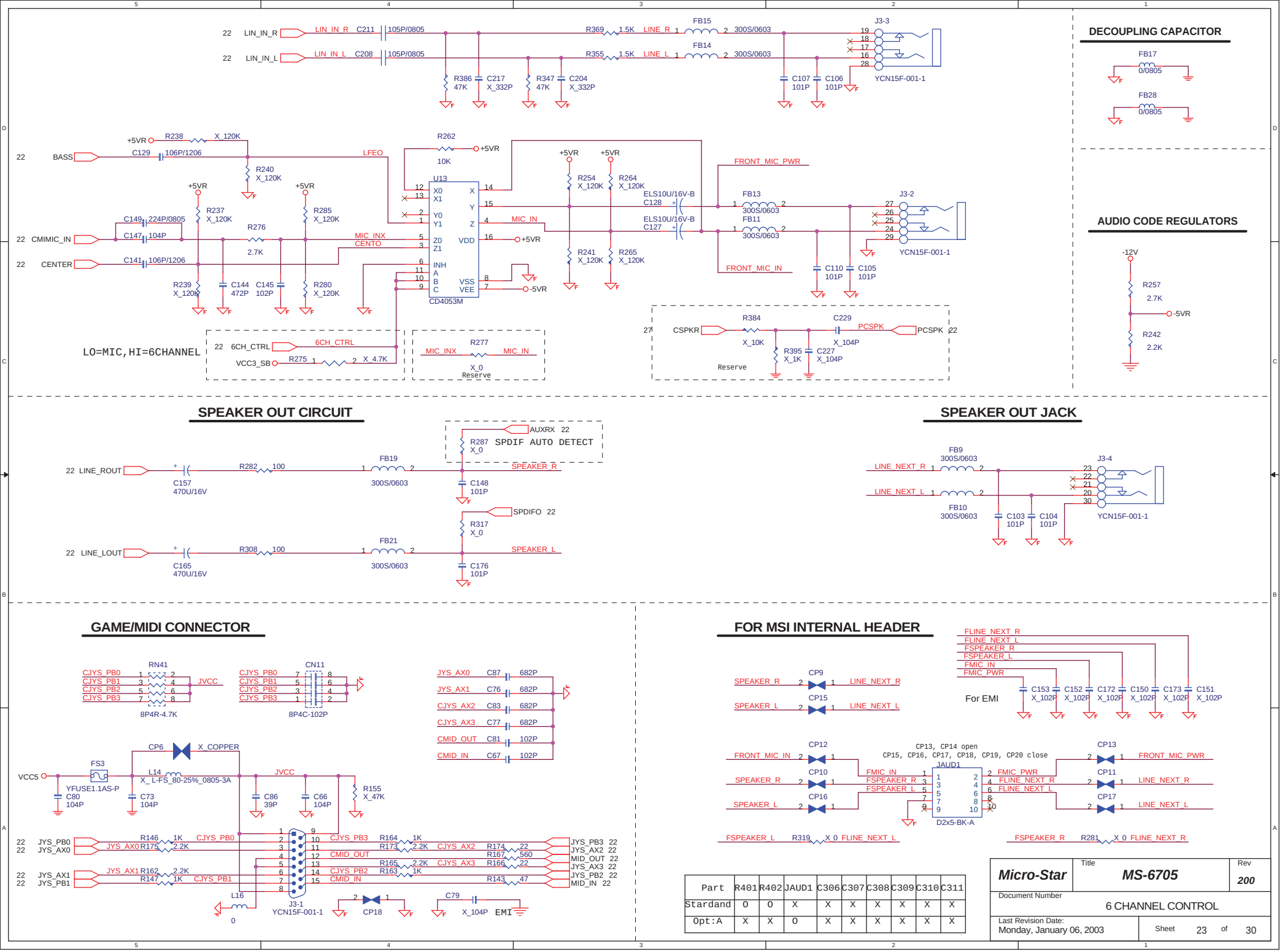


Micro-Star	Title: MS-6705	Rev: 200
Document Number: USB & FAN Connectors		
Last Revision Date: Monday, January 06, 2003	Sheet 21 of 30	

C-MEDIA CMI8738MX PCI AUDIO



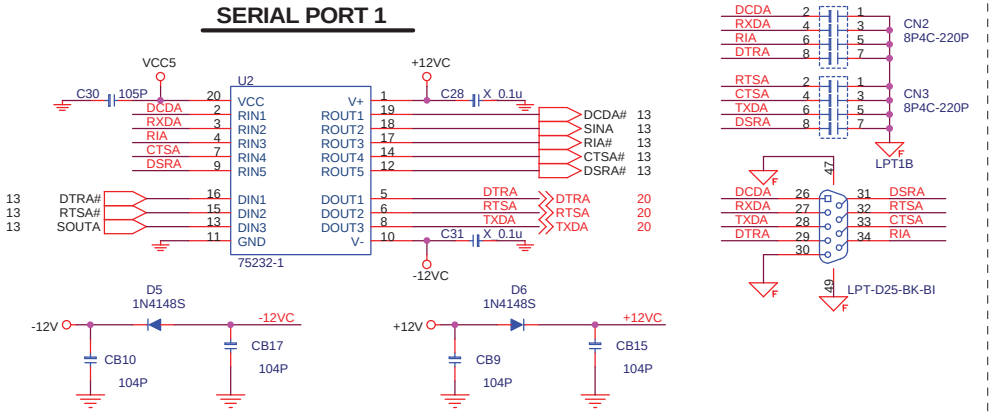
Micro-Star	Title: MS-6705		Rev: 200
Document Number: CMI8738 PCI AUDIO			
Last Revision Date: Monday, January 06, 2003		Sheet 22 of 30	



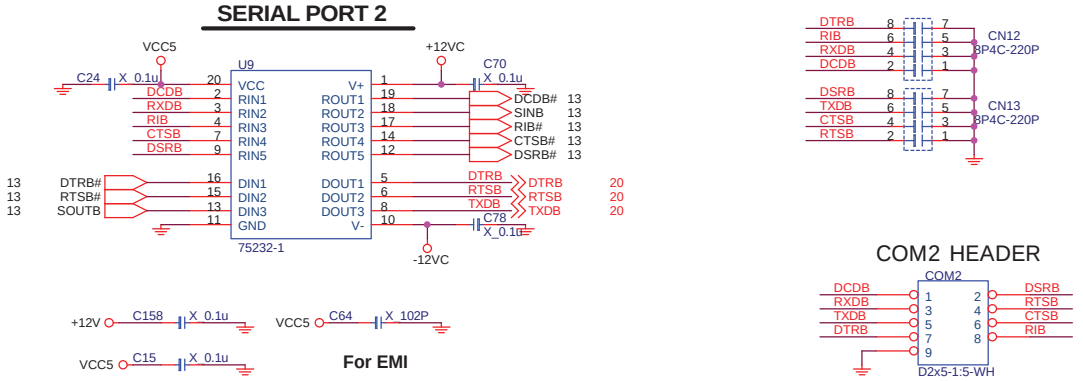
Part	R401	R402	JAUD1	C306	C307	C308	C309	C310	C311
Stardand	0	0	X	X	X	X	X	X	X
Opt:A	X	X	0	X	X	X	X	X	X

Micro-Star	Title: MS-6705	Rev: 200
Document Number: 6 CHANNEL CONTROL		
Last Revision Date: Monday, January 06, 2003	Sheet 23 of 30	

SERIAL PORT 1

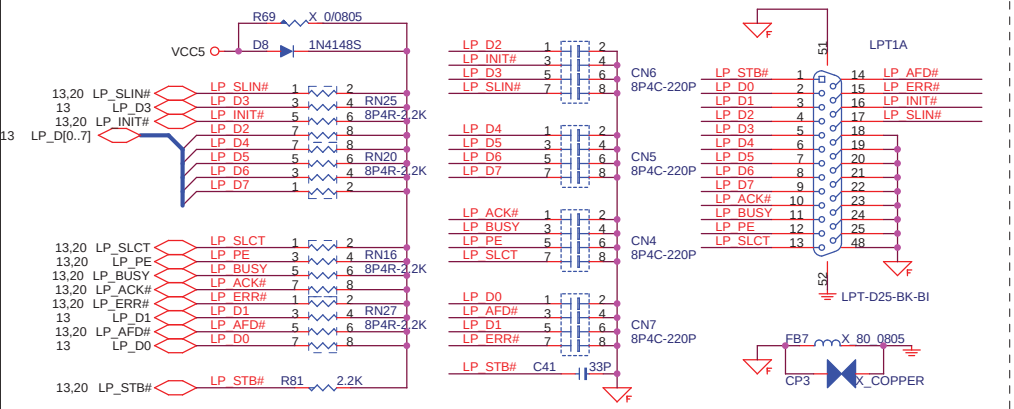


SERIAL PORT 2

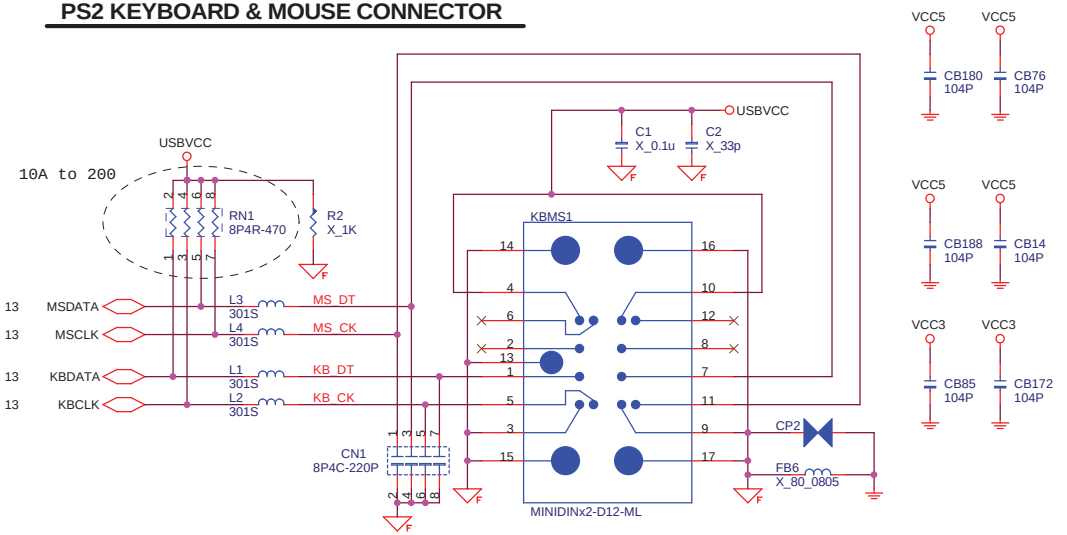


COM2 HEADER

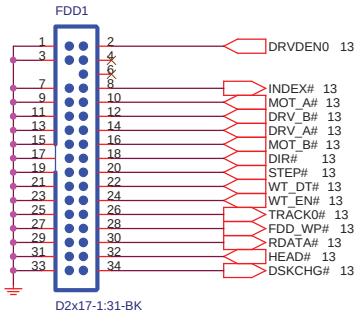
PARALLAL PORT



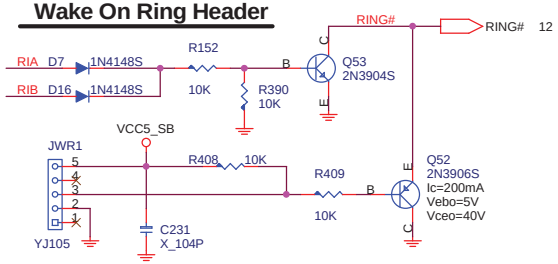
PS2 KEYBOARD & MOUSE CONNECTOR



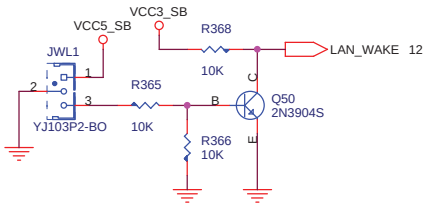
FLOPPY CONNECTOR

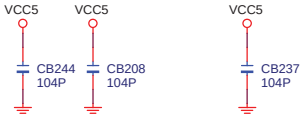


Wake On Ring Header

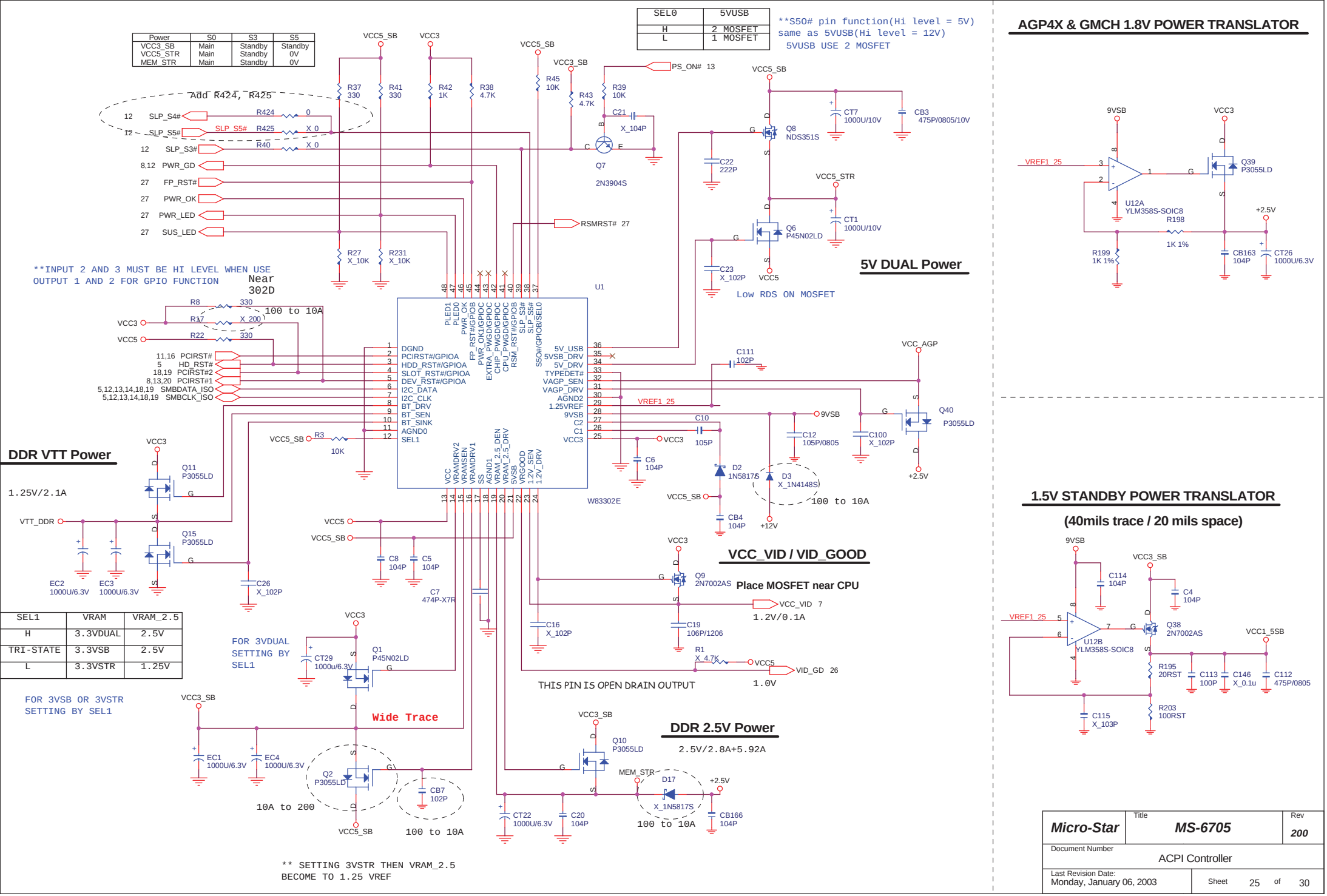


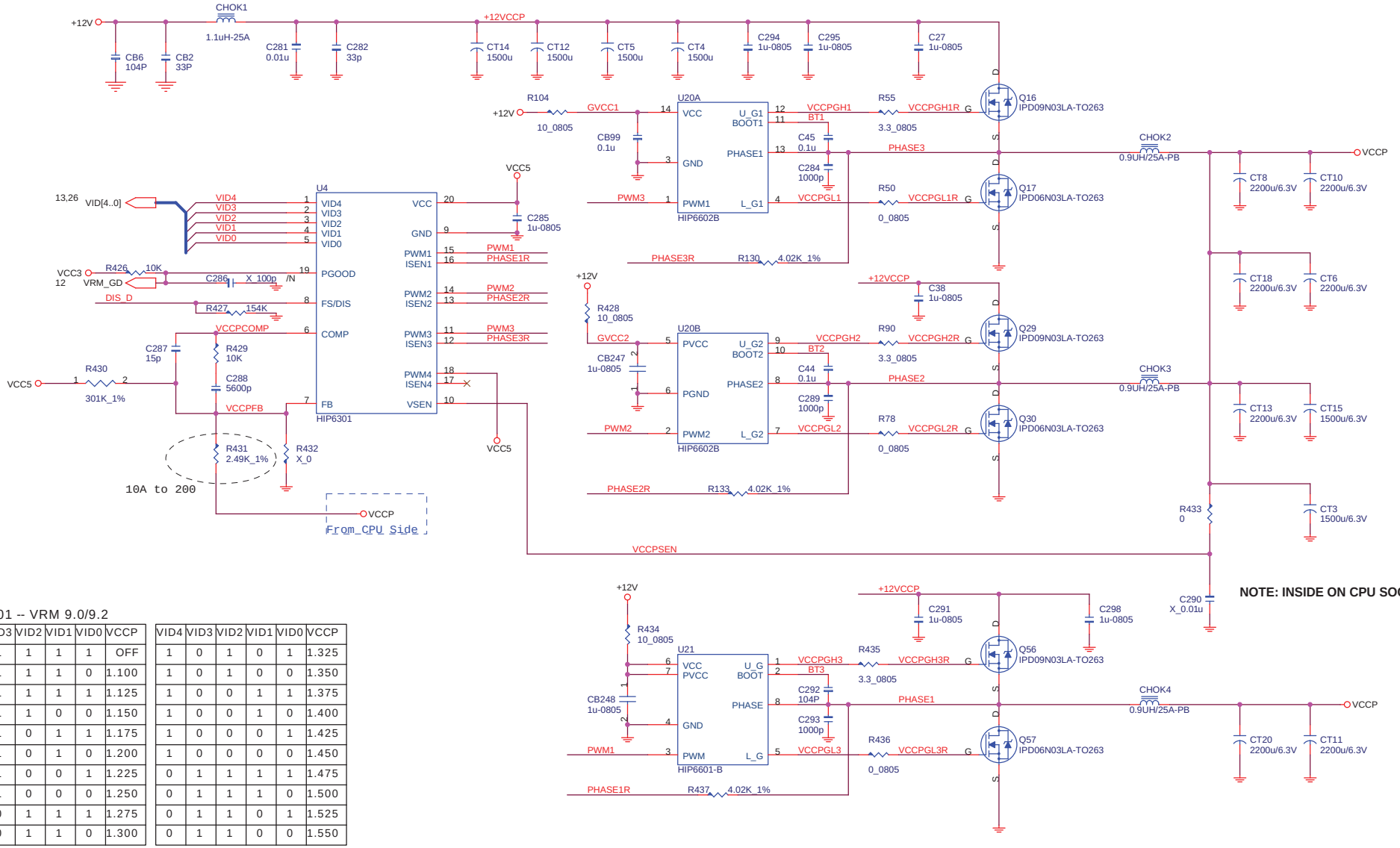
Wake On LAN Header





Micro-Star	Title: MS-6705	Rev: 200
Document Number: IO Connector		
Last Revision Date: Monday, January 06, 2003	Sheet 24 of 30	


Power | S0 | S3 | S5
VCC3_SB | Main | Standby | Standby
VCC5_STR | Main | Standby | 0V
MEM_STR | Main | Standby | 0V
SEL0 | 5VUSB
H | 2 MOSFET
L | 1 MOSFET
**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET
Add R424, R425
SLP_S4#
SLP_S5#
SLP_S3#
PWR_GD
FP_RST#
PWR_OK
PWR_LED
SUS_LED
PS_ON# 13
RSMRST# 27
5V DUAL Power
Low RDS ON MOSFET
**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION
Near 302D
100 to 10A
U1
W83302E
DDR VTT Power
1.25V/2.1A
VTT_DDR
SEL1 | VRAM | VRAM_2.5
H | 3.3VDUAL | 2.5V
TRI-STATE | 3.3VSB | 2.5V
L | 3.3VSTR | 1.25V
FOR 3VDUAL SETTING BY SEL1
FOR 3VSB OR 3VSTR SETTING BY SEL1
VCC_VID / VID_GOOD
Place MOSFET near CPU
VCC_VID 7
1.2V/0.1A
VID_GD 26
1.0V
THIS PIN IS OPEN DRAIN OUTPUT
Wide Trace
DDR 2.5V Power
2.5V/2.8A+5.92A
10A to 200
100 to 10A
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF
AGP4X & GMCH 1.8V POWER TRANSLATOR
1.5V STANDBY POWER TRANSLATOR
(40mils trace / 20 mils space)
Micro-Star
MS-6705
200
ACPI Controller
Monday, January 06, 2003
Sheet 25 of 30



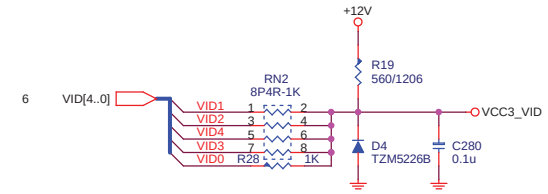
HIP6301 -- VRM 9.0/9.2

VID4	VID3	VID2	VID1	VID0	VCCP
1	1	1	1	1	OFF
1	1	1	1	0	1.100
1	1	1	1	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300

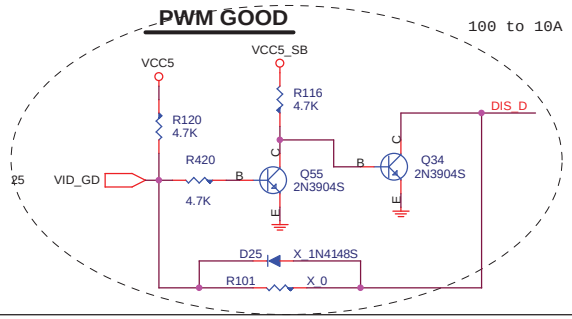
VID4	VID3	VID2	VID1	VID0	VCCP
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550

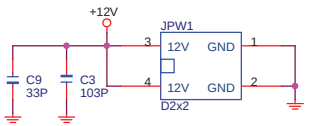
VID4	VID3	VID2	VID1	VID0	VCCP
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800

VID PULL-UP RESISTORS



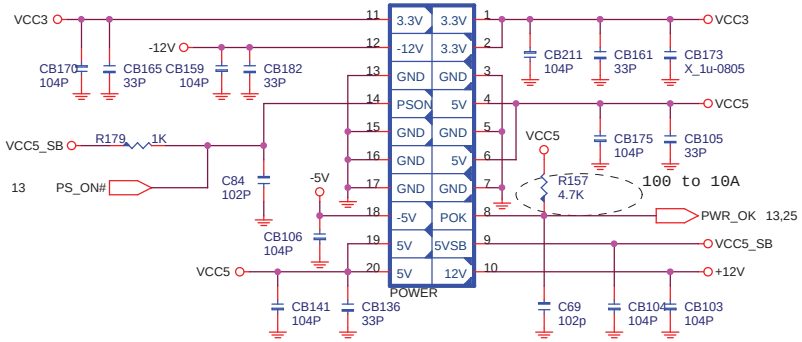
PWM GOOD



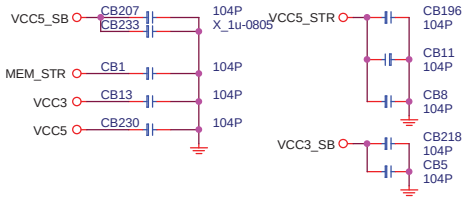


Micro-Star	Title: MS-6705	Rev: 200
Document Number: VRM 9.0		
Last Revision Date: Monday, January 06, 2003	Sheet 26 of 30	

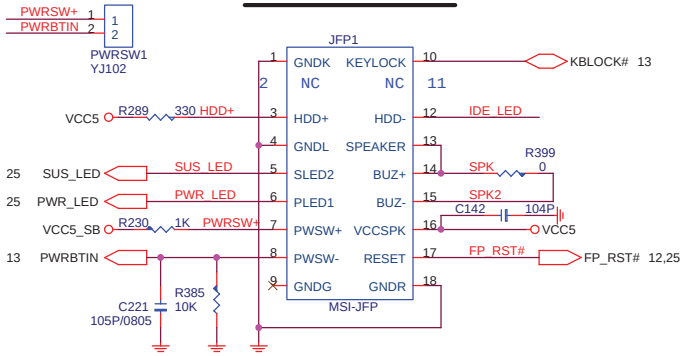
ATX CONNECTOR

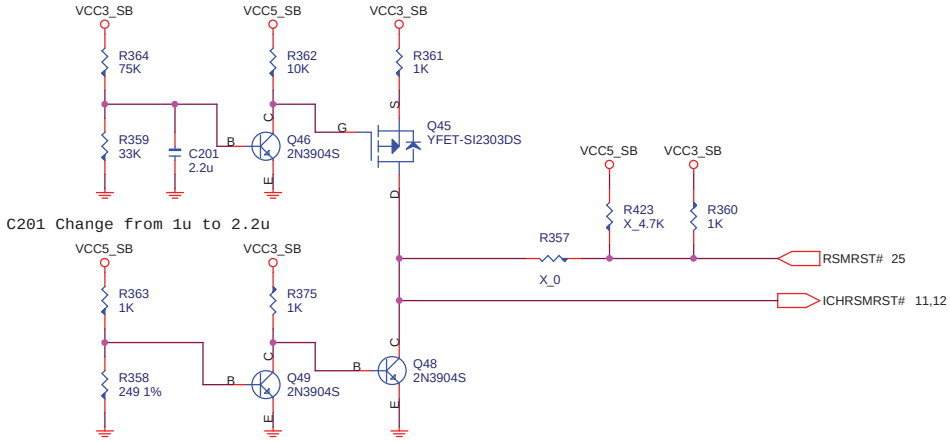


REGULATORS OUTPUT DECOUPLING CAPACITORS

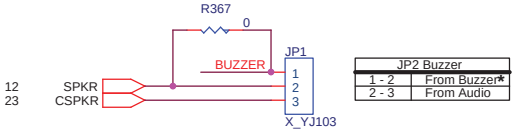


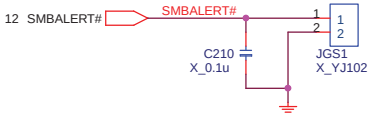
FRONT PANEL



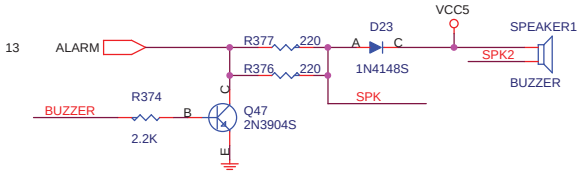


HDD LED





SPEAKER



Micro-Star	Title: MS-6705		Rev: 200
Document Number: MSI	Front Panel & Connector		
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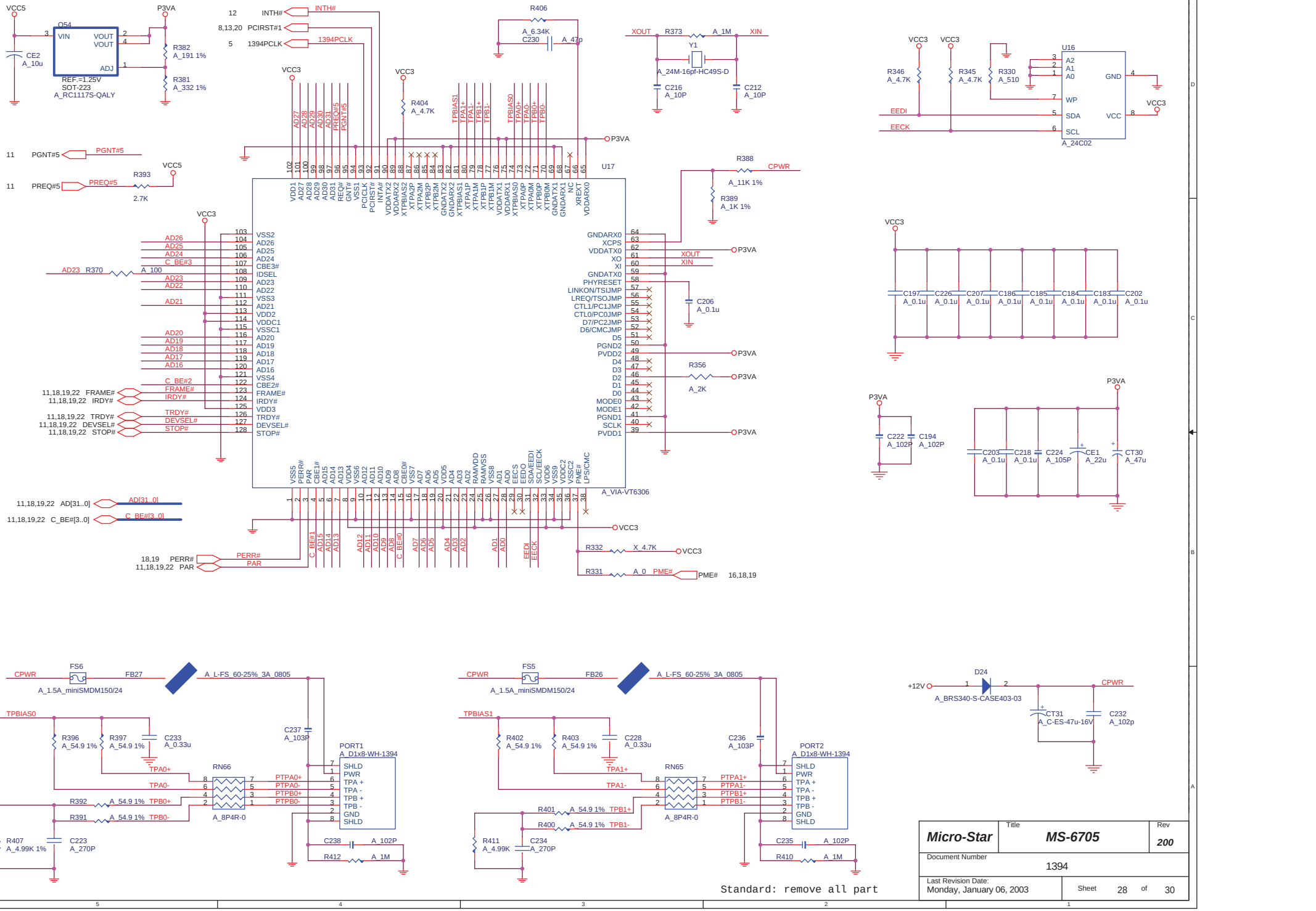
VCC5
P3VA
Q54
VIN
VOUT
VOUT
ADJ
REF.=1.25V
SOT-223
A_RC1117S-QALY
CE2
A_10u
R382
A_191 1%
R381
A_332 1%
INTH#
PCIRST#1
1394PCLK
R406
A_6.34K
C230
A_47p
XOUT
R373
A_1M
XIN
Y1
A_24M-16pf-HC49S-D
C216
A_10P
C212
A_10P
R404
A_4.7K
PGNT#5
PREQ#5
R393
2.7K
U17
VSS2
AD26
AD25
AD24
C_BE#3
IDSEL
AD23
AD22
VSS3
AD21
VDD2
VDDC1
VSSC1
AD20
AD19
AD18
AD17
AD16
VSS4
CBE2#
FRAME#
IRDY#
VDD3
TRDY#
DEVSEL#
STOP#
GNDARX0
XCPS
VDDATX0
XO
XI
GNDATX0
PHYRESET
LINKON/TSIJMP
LREQ/TSOJMP
CTL1/PC1JMP
CTL0/PC0JMP
D7/PC2JMP
D6/CMCJMP
D5
PGND2
PVDD2
D4
D3
D2
D1
D0
MODE0
MODE1
PGND1
SCLK
PVDD1
R388
A_11K 1%
CPWR
R389
A_1K 1%
C206
A_0.1u
R356
A_2K
A_VIA-VT6306
AD23 R370
A_100
11,18,19,22 FRAME#
11,18,19,22 IRDY#
11,18,19,22 TRDY#
11,18,19,22 DEVSEL#
11,18,19,22 STOP#
11,18,19,22 AD[31..0]
11,18,19,22 C_BE#[3..0]
18,19 PERR#
11,18,19,22 PAR
R332
X_4.7K
R331
A_0
PME#
16,18,19
U16
A0
A1
A2
WP
SDA
SCL
GND
VCC
EEDI
EECK
A_24C02
R346
A_4.7K
R345
A_4.7K
R330
A_510
C197
C226
C207
C186
C185
C184
C183
C202
A_0.1u
C222
A_102P
C194
A_102P
C203
C218
A_0.1u
C224
A_105P
CE1
A_22u
CT30
A_47u
FS6
A_1.5A_miniSMDM150/24
FB27
A_L-FS_60-25%_3A_0805
TPBIAS0
R396
A_54.9 1%
R397
A_54.9 1%
C233
A_0.33u
C237
A_103P
PORT1
A_D1x8-WH-1394
SHLD
PWR
TPA +
TPA -
TPB +
TPB -
GND
SHLD
RN66
A_8P4R-0
TPA0+
TPA0-
TPB0+
TPB0-
R392
R391
C223
A_270P
R407
A_4.99K 1%
C238
A_102P
R412
A_1M
FS5
A_1.5A_miniSMDM150/24
FB26
TPBIAS1
R402
R403
C228
A_0.33u
C236
A_103P
PORT2
RN65
TPA1+
TPA1-
TPB1+
TPB1-
R401
R400
C234
A_270P
R411
A_4.99K
C235
A_102P
R410
A_1M
D24
A_BRS340-S-CASE403-03
+12V
CT31
A_C-ES-47u-16V
C232
A_102p
Standard: remove all part
Micro-Star
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MS-6705
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200
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1394
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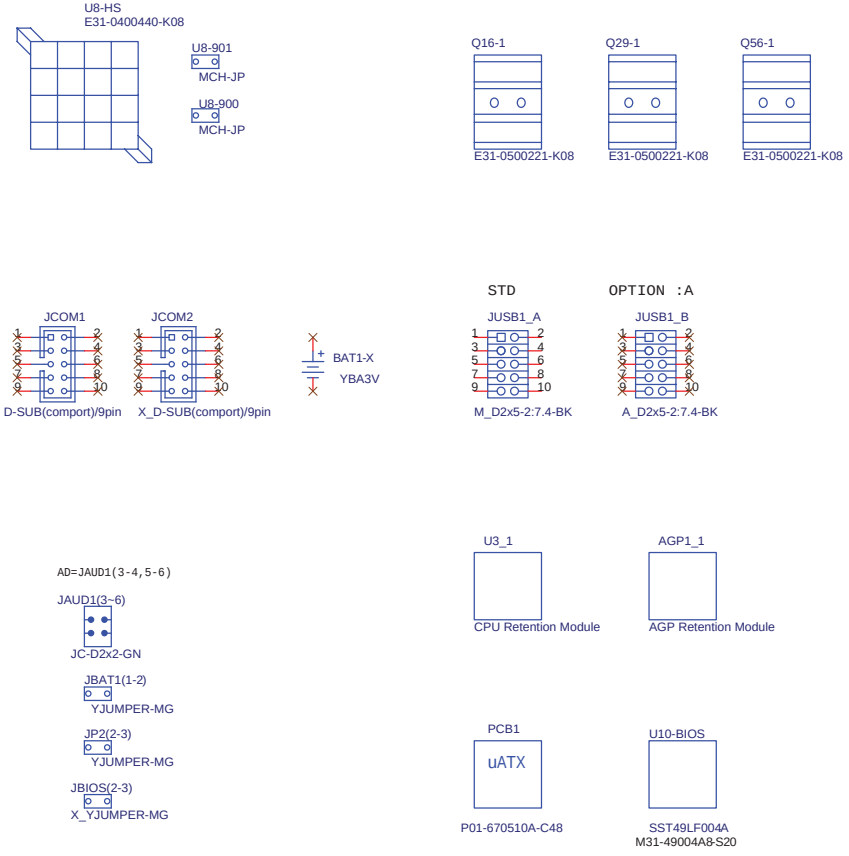
Jumper Setting & Connector Setting

JBAT1	Clear CMOS
1 - 2	Normal *
2 - 3	Clear CMOS



Connector	Description
U7	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIMM1	DDRAM DIMM1
DIMM2	DDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
PCI4	PCI Slot4
COM1	Serial Port
COM2	Serial Port
LPT1	Parallel Port
FDD1	Floopy
JWR1	MODEM RING HEADER
KBMS1	PS/2 Keyboard and mouse
C_FAN1	CPU FAN HEADER
S_FAN1	System FAN HEADER
USB	USB REAR CONNECTOR
JUSB1	USB INTERNAL HEADER
CONN1	ATX Power
JFP1	Front Panel
JPW1	ATX12V Power

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Document Number: JUMPER SETTING		
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History : 100 to 10A

Page	Description	Date
7	L7,L8 size change from 1206 to 0805	
8,9,10	NB Change from 845G to 845GE rev:B1	
11,12	SB Change from ICH4 rev:A1to ICH4 rev:B0	
13	R177 connect change to GND & add R438 for SIO power on strapping reserve	
21	Add C296,C297 & mount FAN speed control request parts but unmount RN3,RN22,C13,C37 ,R4,R63	
24	Remove CN8,CN9 , COM2 I/O connector	
25	U1 change Version from ver:E to ver:GCRB. For this version change unmount R17,D3,D17 & change CB7 from 104PF to 102PF	
26	VRM 9.0 change from two phase to three phase. For PWM good circuit unmount R101 & add D25 reserved and mount R116,R120,R420,Q34,Q55	
27	R157 change from 1K to 4.7K for U1 change version from ver:E to ver:GCRB.	
29	U10-BIOS change from 2M to 4M flash ROM	

History : 10A to 200

Page	Description	Date
11	Short R244,R217,R245,R218,R220 0ohm Resistor	
12	Short JBAT1 pin1,2	
20	R82 change from 47K to 0 ohm	
21	Add R439~R442,D26,D27 for FAN Speed control ; un-mount R5,R6,Q5,C293,R68,R67,Q23,C297	
24	Change RN1 from 4.7K to 470	
25	Change Q2 size from SOT23 to TO252	
26	Change R431 from 1.78K to 2.49K for meet VRM 9.0 load line test	
20	Change C88,CB132 from 0.1uF 0603 to 4.7uF 0805 for improve BIOS program yield rate	

Micro-Star	Title: MS-6705	Rev: 200
Document Number: History		
Last Revision Date: Wednesday, January 08, 2003	Sheet 30 of 30	