MS-6702 VER:0E ATX

AMD PGA 754 K8-Processor (DDR 400)
VIA K8T400M / VT8237 Chipset (AGP 8X / VLink 8X)
Winbond 83697HF-VF LPC I/O
VT6306 1394a OHCI Link Layer Controller
PDC20378 Serial ATA Controller
RTL 8110S Giga/ 8100C100/10 Bit LAN Support
USB 2.0 support (integrated into VT8237)
Vcore Jumpless support
ALC650/ALC655 6 channel S/W Audio

DDR DIMM * 3
AGP SLOT * 1 (8X)
PCI SLOT * 5

Layout Gerber-Out 0822-91

1. Modify Circuit 6702-0A_0822-91.DSN 08/22/91-> Layout Finished (Gerber-Out Version).

Release ES-BOM

1. Modify Circuit 6702-0A_0827A-91.DSN 08/27/91-> Release NEW BOM of ES-BOM for Standard (6702-A20).
2. Modify Circuit 6702-0A_1001-91.DSN 10/01/91-> After Pilot-Run (Didn't release ECR) .

Modify MS6702/VER:0B 10/04/2002

1. Modify Circuit 6702-0B_1108-91.DSN 11/08/91=> VER:0A -> OB : Modify H/W issue & K8-CPU & NB-K8T400M & Change H/W Audio to S/W Audio (Gerber-Out Version) .
2. Creat new BOM for MS6702/VER:0B , 6702-0B_1108A-91.dsn 11/08/91 .
3. Modify BOM for MS6702/VER:0B , 6702-0B_1118-91.dsn 11/18/91 .

Modify MS6702/VER:0C 1/03/2003

1. Modify Circuit 6702-0C FROM 67020B.
2. GERBER OUT 1/29/2003.

MS6702-0E

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Title	*Cover Sheet*	Rev 0E
Document Number	*MS-6702*	

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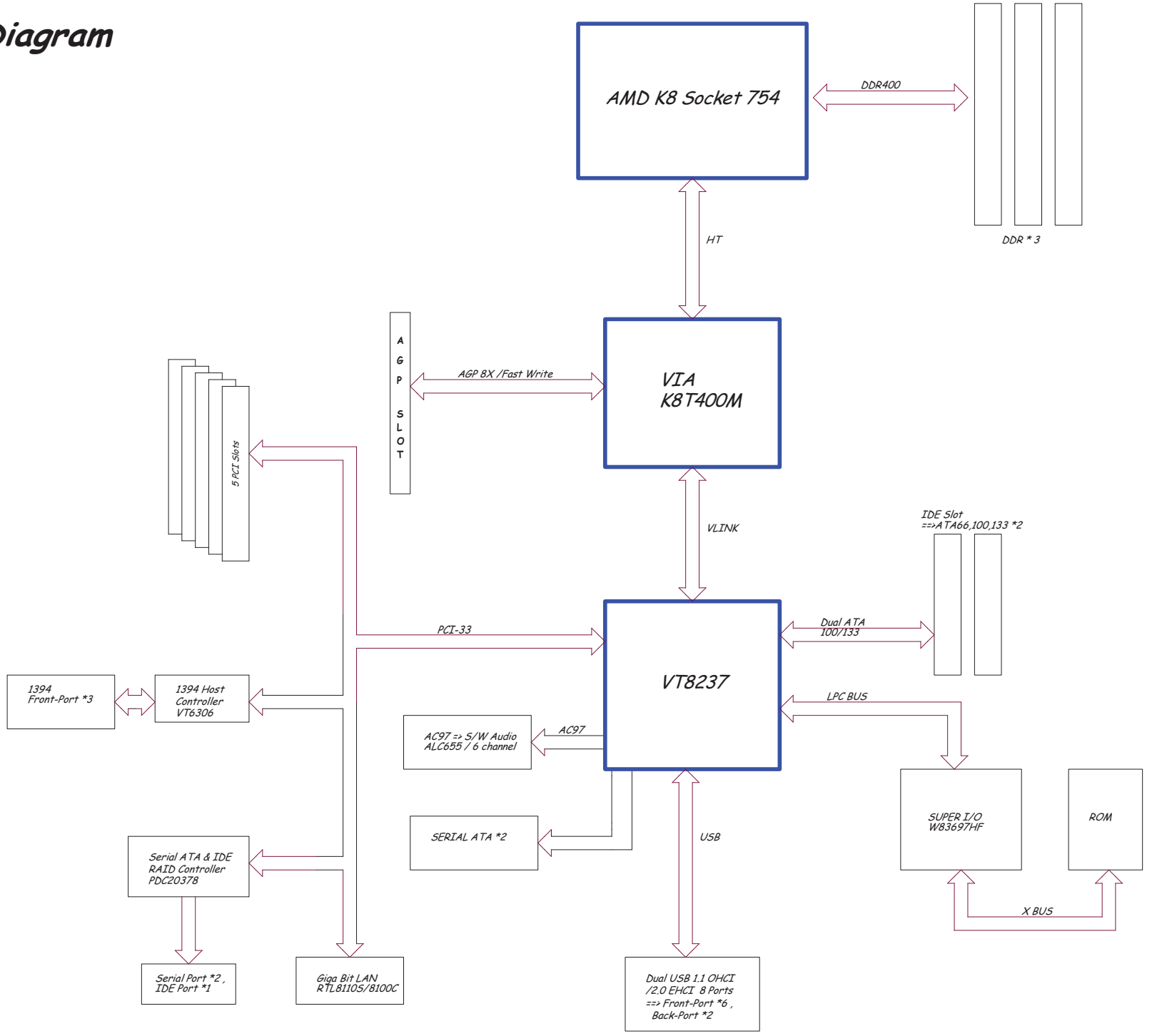
Block Diagram



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GPIO FUNCTION

VT8237 GPIO Function Define

PIN NAME	Function define
GPO0 (VSUS33)	VCORE_ADJ
GPO1/SUSA#(VSUS33)	NA
GPO2/SUSB#(VSUS33)	SUSB#
GPO3/SUSST1#(VSUS33)	SUSST#
GPO4/SUSCLK(VSUS33)	NA (Exteranl Pull up to 3VDUAL)
GPO5/CPUSTP#	NA (Exteranl Pull up to VCC3)
GPO6/PCISTP#	NA (Exteranl Pull up to VCC3)
GPO7/SLP#	LDTSTOP#
GPO8/GPI8/IPBIN0	NA
GPO9/GPI9/IPBIN1	NA
GPO10/GPI10/IPBRDFR	NA
GPO11/GPI11/IPBRDCK	NA
GPO12/GPI12/INTE#	S_VID0
GPO13/GPI13/INTF#	S_VID1
GPO14/GPI14/INTG#	S_VID2
GPO15/GPI15/INTH#	NA
GPO16/SA16/STRAP	LDT Freq Strapping Bit0
GPO17/SA17/STRAP	LDT Freq Strapping Bit1
GPO18/SA18/STRAP	LDT Width (Low=8 Bit)
GPO19/SA19/STRAP	Fast Command (Low=Disable)
GPO20/GPI20 /ACSDIN2/PCS0#/EI	POWERF1
GPO21/GPI21/ACSDIN3 /PCS1#/SLPBTN#	POWERF2
GPO22/GPI22/IOR#	NA
GPO23/GPI23/DPSLP	ROMLOCK
GPO24/GPI24/GPIOA	NA
GPO25/GPI25/GPIOC	NA
GPO26/GPI26/SMBDT2 (VSUS33)	SMBDATA2/Slave SMBUS
GPO27/GPI27/SMBCK2 (VSUS33)	SMBCLK2/Slave SMBUS
GPO28/GPI28/ VIDSEL	NA
GPO29/GPI29/ VRDSLP	NA
GPO30/GPI30/GPIOD	NA
GPO31/GPI31/GPIOE	NA

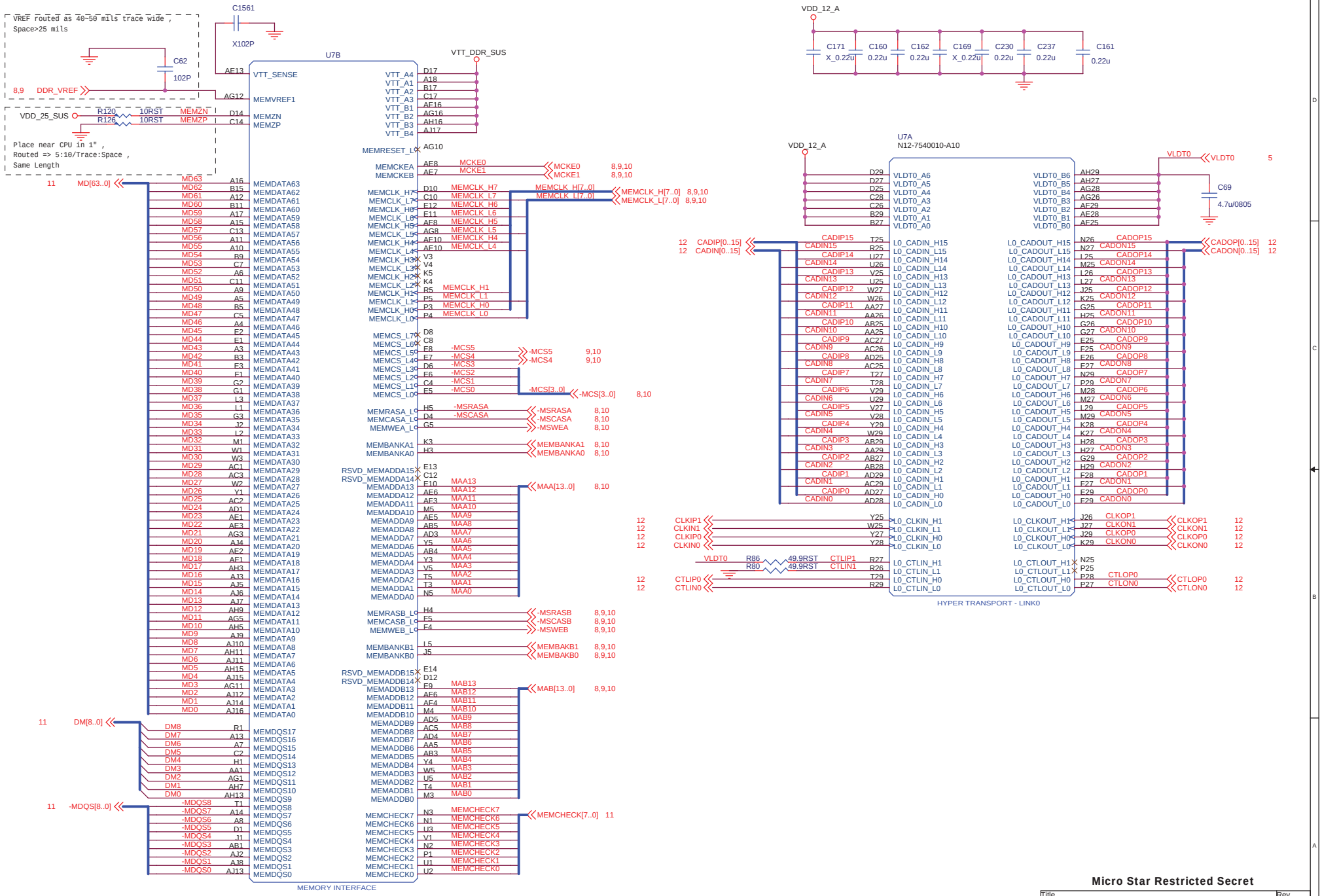
PIN NAME	Function define
GPI0	NA (Exteranl Pull up to VBAT)
GPI1	ATADET0=>Detect IDE1 ATA100/66
GPI2/EXTSMI#	EXTSMI#
GPI3/RING#	RING#
GPI4/LID#	ATADET1=>Detect IDE2 ATA100/66
GPI5/BATLOW#	NA (Exteranl Pull up to 3VDUAL)
GPI6/AGPBZ#	POWERF3
GPI7/REQ#5	NA (Exteranl Pull up to 3VDUAL)
GPI16/INTRUDER#	NA (Exteranl Pull up to VBAT)
GPI17/CPUMISS	NA (Exteranl Pull up to 3VDUAL)
GPI18/AOLGP1/THRM#	THRM#
GPI19/IORDY	NA (Exteranl Pull up to VCC3)

S/IO GPIO Function Define

PIN NAME	Function define
GPBX/GP13	LED#4
GPAY/GP15	LED#2
GPAS1/GP10	LED1
GPAS2/GP17	LED4
GPAX/GP12	LED#3
GPBY/GP14	LED#1
GPBS1/GP11	LED2
GPBS2/GP16	LED3

PCI Routing

DEVICES	INT#	IDSEL	REQ#/GNT#	CLOCK
PCI SLOT 1	INT#A INT#B INT#C INT#D	AD16	PREQ#6 PGNT#6	PCICLK1
PCI SLOT 2	INT#B INT#C INT#D INT#A	AD17	PREQ#3 PGNT#3	PCICLK2
PCI SLOT 3	INT#C INT#D INT#A INT#B	AD18	PREQ#4 PGNT#4	PCICLK3
PCI SLOT 4	INT#D INT#A INT#B INT#C	AD19	PREQ#7 PGNT#7	PCICLK4
PCI SLOT 5	INT#B INT#C INT#D INT#A	AD21	PREQ#8 PGNT#8	PCICLK5
Giga-Bit LAN	INT#A	AD22	PREQ#1 PGNT#1	GLAN_PCLK
MS1 #1			PREQ#0 PGNT#0	MS1_PCLK
SERIAL ATA	INT#B	AD24	(PREQ#2) (PGNT#2)	SATAPCLK
1394	INT#D	AD25	(PREQ#5) (PGNT#5)	1394_PCLK



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VCCA_PLL trace length from the VR1 to the PGA must be 0.75".

Place al filters close to the PGA.

Keep all power and signal trce away from the VR1.

Place a cut in the GND plane around the VCCA_PLL regulator circuit.

VDDIO_SENSE
C1562 X_102P

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

VDDA_25 FB1 180nH/1210 CPU_VDDA_25
C74 4.7u/0805 C72 0.22u C73 3300p

FB1505 THERMDC_CPU
X_120S/0603

U7C

C46 X_102P

36 CPU_GD
38 -CPURST CPU_GD
12,19 -LDTSTOP

VLDT0 R87 44.2RST
VLDT0 R83 44.2RST
C76 102P C77 102P
Place near CPU in 1" , Routed => 5:10/Trace:Space , Same Length

L0_REF1
L0_REF0

15 COREFB_H
15 COREFB_L
Differential , "10:10:5:10:10" .

VCC2_5 R91 1K -LDTSTOP
38 PS_ON#A PS_ON#A Q18 2N7002S

VDDIO_SENSE
7 CPUCLK0_H C75 3900P/X7R CLKIN_H
Near CPU in 0.5" .
R85 169RST
7 CPUCLK0_L C78 3900P/X7R CLKIN_L
VDD_25_SUS
R74 820 NC_AJ23
R64 820 NC_AH23

VTT_DDR_SUS

DBRDY

TMS TCK TRST_L TDI

VCC2_5
R133 1K NC_C18
R124 1K NC_A19

NC_AE23 NC_AF23 NC_AF22 NC_AF21
RN129 8P4R-1K

AH25	VDDA1
AJ25	VDDA2
AE20	RESET_L
AF18	PWROK
AJ27	LDTSTOP_L
AE27	L0_REF1
AE26	L0_REF0
A23	COREFB_H
A24	COREFB_L
B23	CORE_SENSE
AE12	VDDIOFB_H
AF12	VDDIOFB_L
AE11	VDDIO_SENSE
AJ21	CLKIN_H
AH21	CLKIN_L
AJ23	NC_AJ23
AH23	NC_AH23
AE24	NC_AE24
AF24	NC_AF24
C16	VTT_A5
AG15	VTT_B5
AH17	DBRDY
C15	NC_C15
E20	TMS
E17	TCK
B21	TRST_L
A21	TDI
C18	NC_C18
A19	NC_A19
A28	KEY1
AJ28	KEY0
AE23	NC_AE23
AF23	NC_AF23
AF22	NC_AF22
AF21	NC_AF21
C1	FREE29
J3	FREE31
R3	FREE33
AA2	FREE35
D3	FREE1
AG2	FREE37
B18	FREE4
AH1	FREE38
AE21	FREE41
C20	FREE7
AG4	FREE11
C6	FREE12
AG6	FREE13
AE9	FREE14
AG9	FREE40

THERMTRIP_L	A20 THRM#
THERMDA	A26 THERMDA_CPU
THERMDC	A27 THERMDC_CPU
VID4	AG13 VID4
VID3	AE14 VID3
VID2	AG14 VID2
VID1	AF15 VID1
VID0	AE15 VID0
NC_AG18	AG18 NC_AG18
NC_AH18	AH18 NC_AH18
NC_AG17	AG17 NC_AG17
NC_AJ18	AJ18 NC_AJ18
G_FBCLKOUT_H	AH19
G_FBCLKOUT_L	AJ19
DBREQ_L0	AE19 DBREQ_L
NC_D20	D20 NC_D20
NC_C21	C21 NC_C21
NC_D18	D18 NC_D18
NC_C19	C19 NC_C19
NC_B19	B19 NC_B19
TDO	A22 TDO
NC_AF18	AF18
RSVD_SCL	D22
RSVD_SDA	C22
FREE26	B13
FREE28	B7
FREE30	C3
FREE32	K1
FREE34	R2
FREE36	AA3
FREE10	F3
FREE18	C23
FREE19	AG7
FREE42	AE22
FREE24	C24
FREE25	A25
FREE27	C9

THERM# 36
THERMDA_CPU 30,31
THERMDC_CPU 30
VID[4..0] 15,32

LAYOUT: Route FBCLKOUT_H/L differentially with 20/8/5/8/20 spacing and trace width. (In CPU breakout => routed 5:5:5)
FBCLKOUT_H R88 80.6RST FBCLKOUT_L
_Zdiff = 80 ohm

VDD_25_SUS R138 1K

VCC2_5 RN7 8P4R-4.7K
VID2 VID3 VID1 VID0
VID4 R31 4.7K

HDT Test Port Signal .

DBREQ_L DBRDY TMS TCK TRST_L TDI
R71 1K R61 1K
RN128 8P4R-1K
VCC2_5
C1541 4.7u/0805

NC_AH18 NC_AJ18 NC_AG18 NC_AG17 NC_C19 NC_D18 NC_D20 NC_B19 NC_C21
RN130 8P4R-1K
RN131 8P4R-1K
R137 1K

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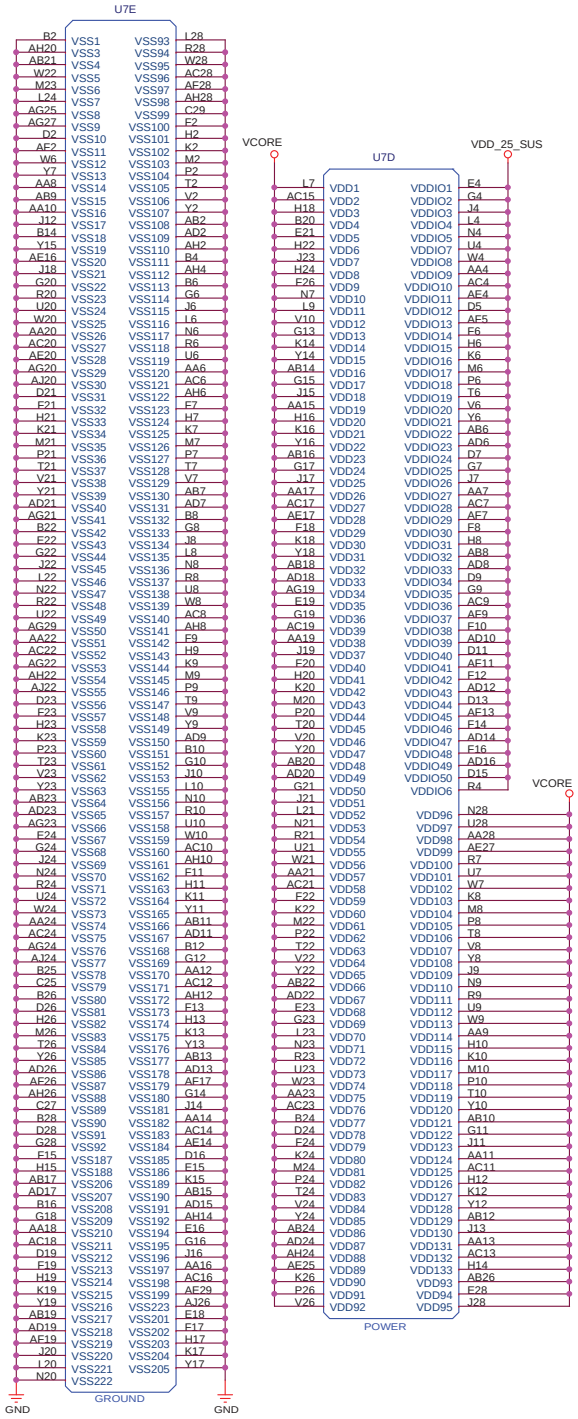

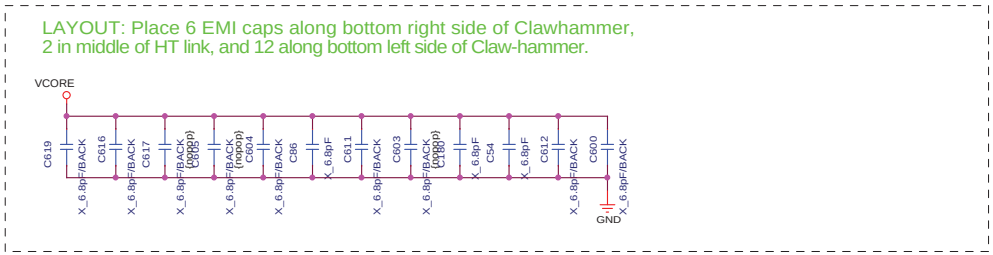

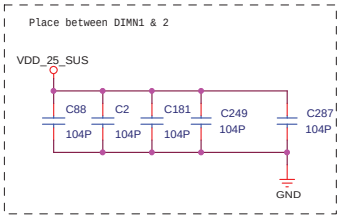

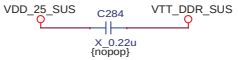

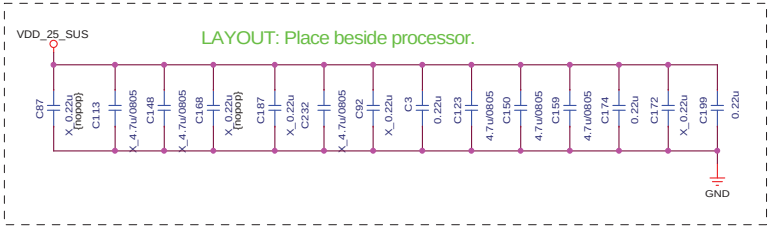

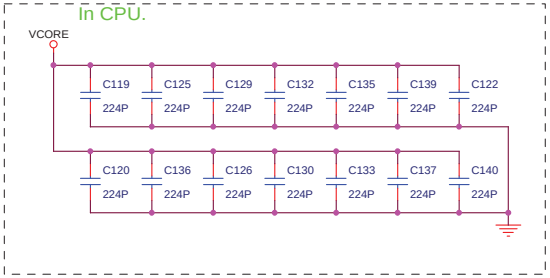

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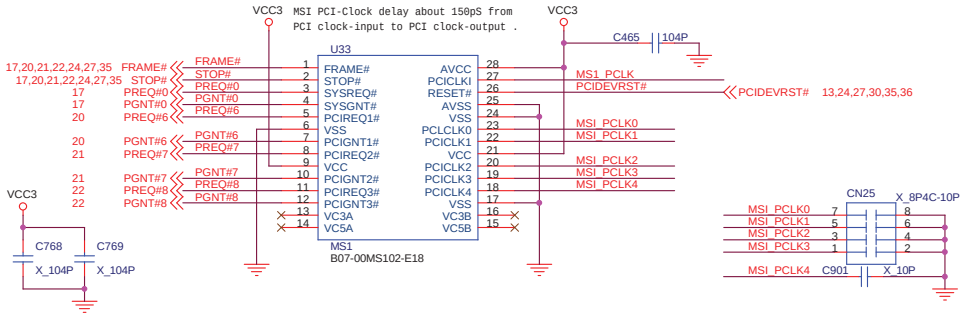
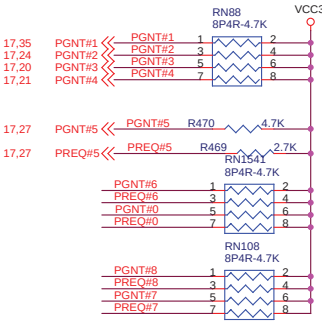
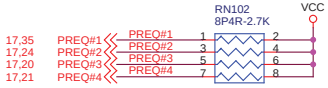
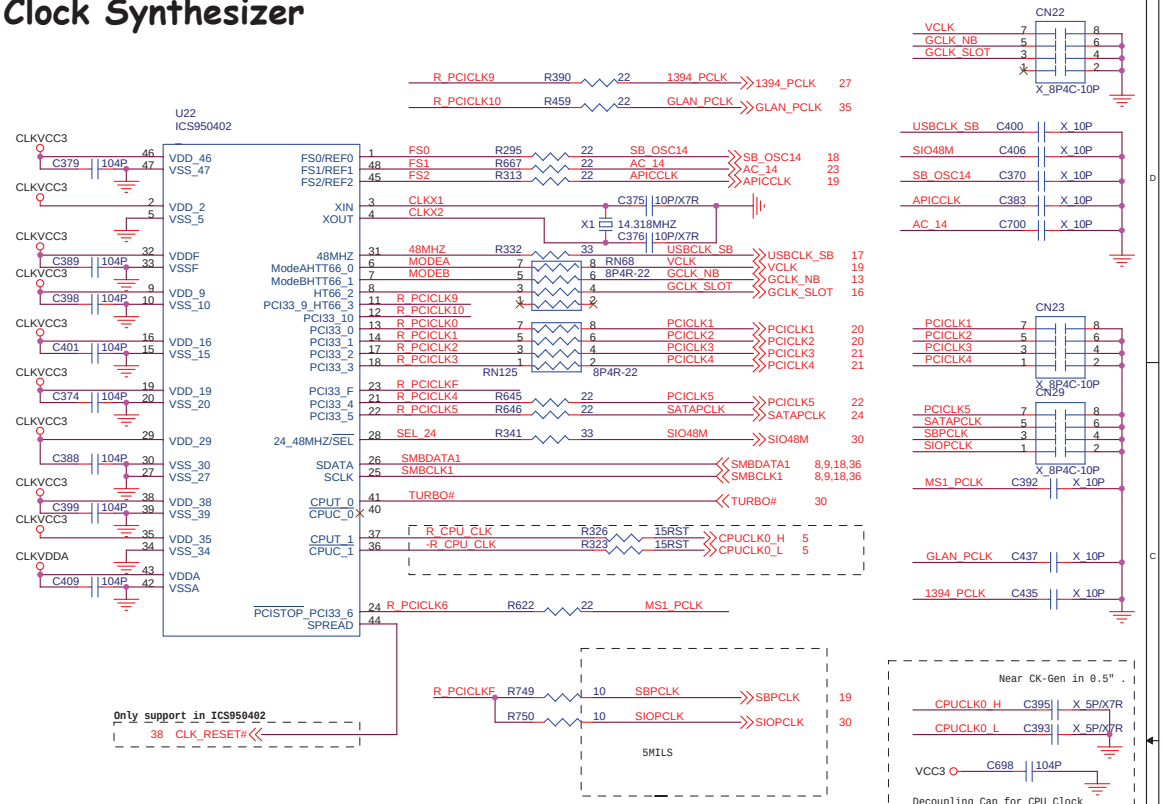
Clock Synthesizer









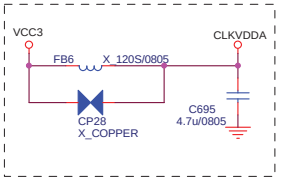
ICS950402						
Strapping				CPU	HTT	PCI
FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	0	0	0	100.90	67.27	33.63
0	0	0	1	133.90	66.95	33.48
0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	66.68	33.34
*** 0	1	1	1	200.40	66.80	33.40
1	0	0	0	150.00	60.00	33.00
1	0	0	1	180.00	60.00	33.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	30.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	33.33
1	1	1	1	300.00	75.00	37.50

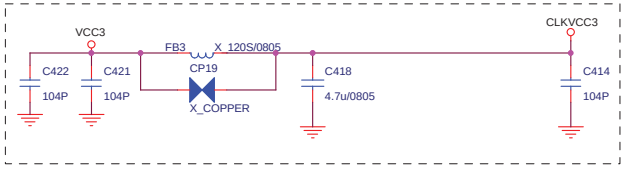
ModeA	ModeB	Pin6	Pin7	Pin8	Pin11
*** 0	0	HTTCLK0	HTTCLK1	HTTCLK2	PCICLK10
0	1	ModeA In	HTTCLK1	HTTCLK2	HTTCLK3
1	0	PCICLK7	PCICLK8	PCICLK9	PCICLK10
1	1	ModeA In	PCICLK8	PCICLK9	PCICLK10

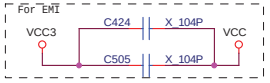
ICS950403 didn't support ModeC

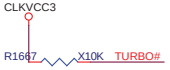
*** => Default Setting

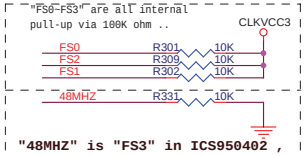
ModeC	Pin24
*** 0	PCICLK6
1	PCI_STOP#

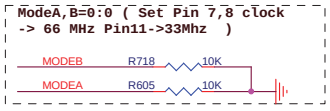


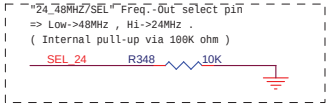












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Title	Clock Synthesizer	Rev 0D
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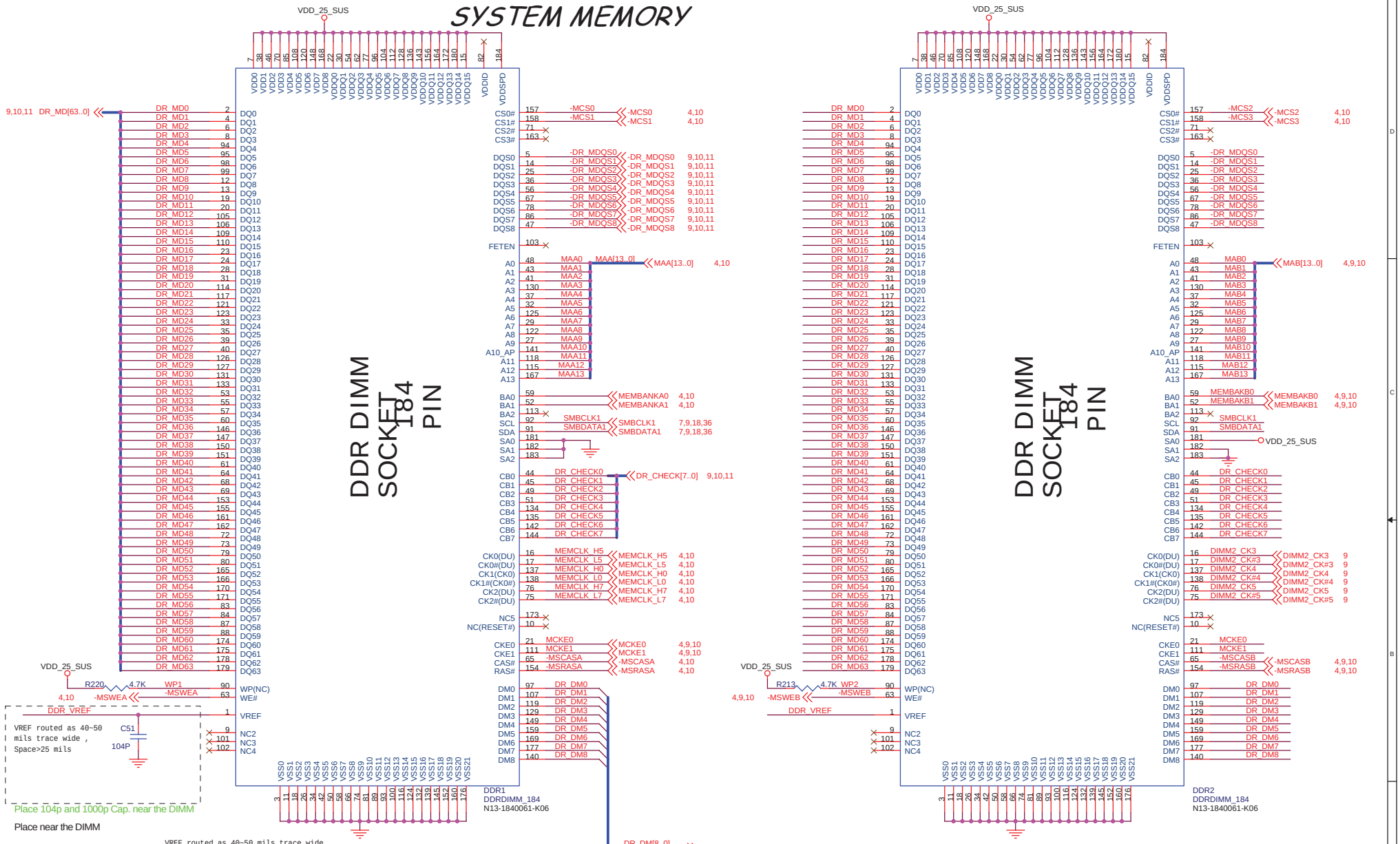
SYSTEM MEMORY



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Title	System Memory : DDR DIMM 1	Rev 0E
Document Number	MS-6702	
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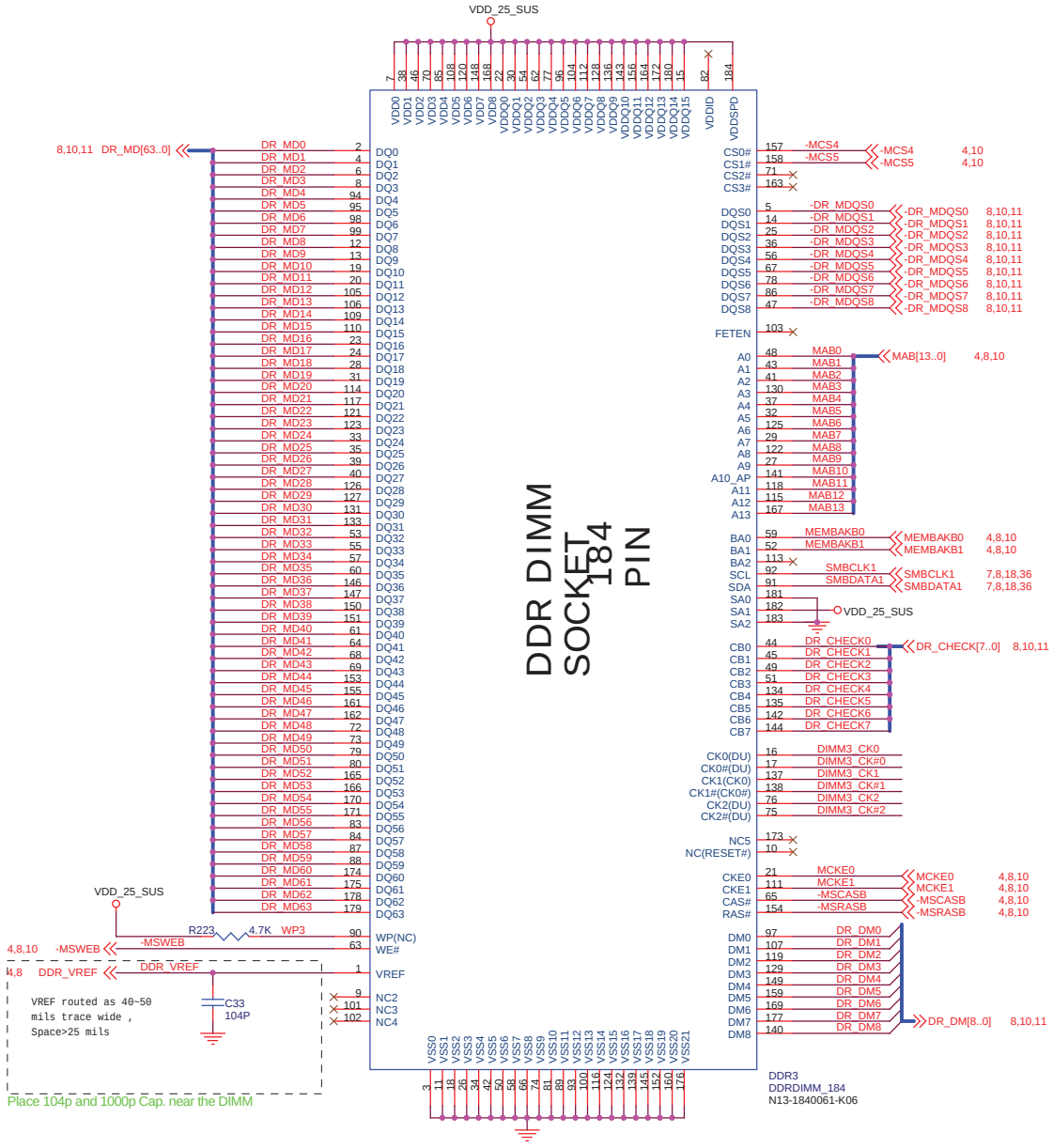
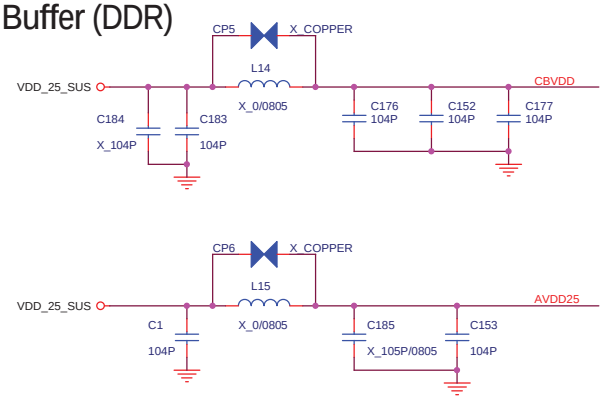
SYSTEM MEMORY



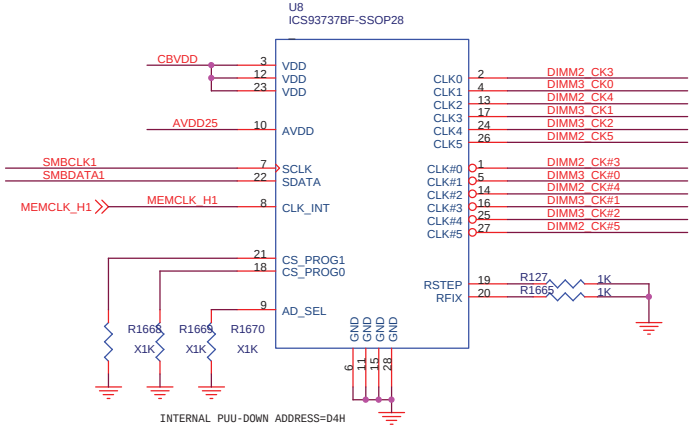
DIMM3 SLAVE ADDRESS = (1010010X)B = A4

Clock Buffer (DDR)



Near U8

8	DIMM2_CK3	DIMM2_CK3	R624	X120RST	DIMM2_CK#3	DIMM2_CK#3 8
		DIMM3_CK0	R625	X120RST	DIMM3_CK#0	
8	DIMM2_CK4	DIMM2_CK4	R626	X120RST	DIMM2_CK#4	DIMM2_CK#4 8
		DIMM3_CK1	R627	X120RST	DIMM3_CK#1	
		DIMM3_CK2	R628	X120RST	DIMM3_CK#2	
8	DIMM2_CK5	DIMM2_CK5	R629	X120RST	DIMM2_CK#5	DIMM2_CK#5 8



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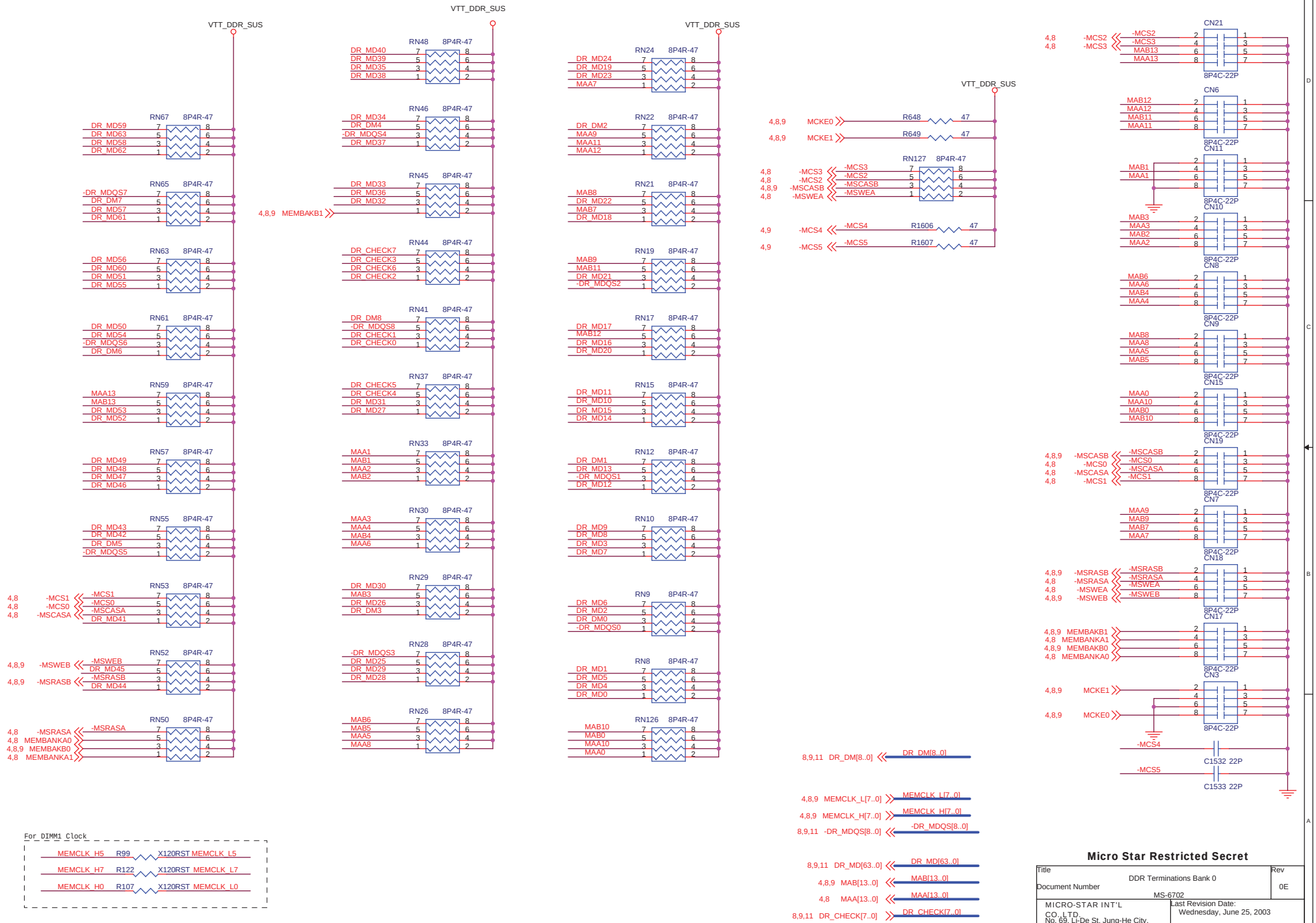
DDR Terminations



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Title	DDR Terminations Bank 0	Rev 0E
Document Number	MS-6702	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003	Sheet 10 of 42

DDR Terminations

-MDQS0 R657 0 -DR_MDQS0

RN11 8P4R-0
MD0 1 2 DR_MD0
MD4 3 4 DR_MD4
MD5 5 6 DR_MD5
MD1 7 8 DR_MD1

RN13 8P4R-0
DM0 1 2 DR_DM0
MD2 3 4 DR_MD2
MD6 5 6 DR_MD6
MD7 7 8 DR_MD7

RN16 8P4R-0
MD3 1 2 DR_MD3
MD8 3 4 DR_MD8
MD9 5 6 DR_MD9
MD12 7 8 DR_MD12

MD15 R658 0 DR_MD15

RN18 8P4R-0
-MDQS1 1 2 -DR_MDQS1
MD13 3 4 DR_MD13
DM1 5 6 DR_DM1
MD14 7 8 DR_MD14

RN23 8P4R-0
-MDQS2 1 2 -DR_MDQS2
MD17 3 4 DR_MD17
MD21 5 6 DR_MD21
DM2 7 8 DR_DM2

MD18 R659 0 DR_MD18

RN20 8P4R-0
MD10 1 2 DR_MD10
MD11 3 4 DR_MD11
MD20 5 6 DR_MD20
MD16 7 8 DR_MD16

RN25 8P4R-0
MD22 1 2 DR_MD22
MD23 3 4 DR_MD23
MD19 5 6 DR_MD19
MD24 7 8 DR_MD24

RN27 8P4R-0
MD28 1 2 DR_MD28
MD29 3 4 DR_MD29
MD25 5 6 DR_MD25
-MDQS3 7 8 -DR_MDQS3

RN32 8P4R-0
MD26 1 2 DR_MD26
MD30 3 4 DR_MD30
MD27 5 6 DR_MD27
MD31 7 8 DR_MD31

MD38 R661 0 DR_MD38

RN42 8P4R-0
MEMCHECK7 1 2 DR_CHECK7
MD32 3 4 DR_MD32
MD36 5 6 DR_MD36
MD33 7 8 DR_MD33

RN47 8P4R-0
MD37 1 2 DR_MD37
-MDQS4 3 4 -DR_MDQS4
DM4 5 6 DR_DM4
MD34 7 8 DR_MD34

MD42 R662 0 DR_MD42

RN49 8P4R-0
MD35 1 2 DR_MD35
MD39 3 4 DR_MD39
MD40 5 6 DR_MD40
MD44 7 8 DR_MD44

RN51 8P4R-0
MD45 1 2 DR_MD45
MD41 3 4 DR_MD41
-MDQS5 5 6 -DR_MDQS5
DM5 7 8 DR_DM5

RN54 8P4R-0
MD43 1 2 DR_MD43
MD46 3 4 DR_MD46
MD47 5 6 DR_MD47
MD48 7 8 DR_MD48

RN58 8P4R-0
MD49 1 2 DR_MD49
MD52 3 4 DR_MD52
MD53 5 6 DR_MD53
DM6 7 8 DR_DM6

MD51 R663 0 DR_MD51

RN60 8P4R-0
-MDQS6 1 2 -DR_MDQS6
MD54 3 4 DR_MD54
MD50 5 6 DR_MD50
MD55 7 8 DR_MD55

RN62 8P4R-0
MD60 1 2 DR_MD60
MD56 3 4 DR_MD56
MD61 5 6 DR_MD61
MD57 7 8 DR_MD57

RN64 8P4R-0
DM7 1 2 DR_DM7
-MDQS7 3 4 -DR_MDQS7
MD62 5 6 DR_MD62
MD58 7 8 DR_MD58

MD59 R707 0 DR_MD59

MD63 R664 0 DR_MD63

RN34 8P4R-0
MEMCHECK5 1 2 DR_CHECK5
MEMCHECK0 3 4 DR_CHECK0
MEMCHECK1 5 6 DR_CHECK1
-MDQS8 7 8 -DR_MDQS8

RN38 8P4R-0
DM8 1 2 DR_DM8
MEMCHECK2 3 4 DR_CHECK2
MEMCHECK6 5 6 DR_CHECK6
MEMCHECK3 7 8 DR_CHECK3

MEMCHECK4 R665 0 DR_CHECK4

DM3 R660 0 DR_DM3

4 -MDQS[8..0] -MDQS[8..0]
8,9,10 -DR_MDQS[8..0] -DR_MDQS[8..0]
8,9,10 DR_MD[63..0] DR_MD[63..0]
4 MD[63..0] MD[63..0]
4 MEMCHECK[7..0] MEMCHECK[7..0]
8,9,10 DR_CHECK[7..0] DR_CHECK[7..0]
8,9,10 DR_DM[8..0] DR_DM[8..0]
4 DM[8..0] DM[8..0]

LAYOUT: Place on backside, evenly spaced around VTT fill.

VDD_25_SUS VTT_DDR_SUS
C28 X_0.22u {nopop}
C285 X_0.22u {nopop}
C11 X_0.22u {nopop}
X_0.22u {nopop} C288

LAYOUT: Locate close to Clawhammer socket.

VTT_DDR_SUS
EC61 1000U/6.3V
EC62 1000U/6.3V
GND

VDD_25_SUS VTT_DDR_SUS
C37 104P
C53 104P
C68 104P
C81 104P
C85 104P
C91 104P
C97 104P

VDD_25_SUS VTT_DDR_SUS
C104 104P
C111 104P
C118 104P
C128 104P
C138 104P
C145 104P
C149 104P

VDD_25_SUS VTT_DDR_SUS
C154 104P
C156 104P
C163 104P
C170 104P
C178 104P
C186 104P
C192 104P

VDD_25_SUS VTT_DDR_SUS
C200 104P
C208 104P
C212 104P
C215 104P
C223 104P
C231 104P
C238 104P

VDD_25_SUS VTT_DDR_SUS
C248 104P
C259 104P
C265 104P
C268 104P
C272 104P
C281 104P

VTT_DDR_SUS

LAYOUT: Place alternating caps to GND and VDD_2.5_SUS in a single line along VTT island.

C49 104P C59 104P C71 104P C83 104P C90 104P C93 104P C100 104P C107 104P C114 104P C121 104P C131 104P C141 104P C146 104P C151 104P C155 104P C157 104P C167 104P
GND

VTT_DDR_SUS
C173 104P C182 104P C189 104P C197 104P C206 104P C209 104P C213 104P C220 104P C226 104P C233 104P C242 104P C252 104P C263 104P C266 104P C270 104P C274 104P C282 104P
GND

VTT_DDR_SUS
C79 0.22u C67 4.7u/0805 C61X 0.22u C66 4.7u/0805 C16 X_4.7u/0805 C14X 0.22u C123 100P
GND

VTT_DDR_SUS
C289X 102P C295X 100P C292 X_4.7u/0805 C239 X_4.7u/0805 C229X 0.22u C217 4.7u/0805 C190 102P C165 0.22u C164 4.7u/0805
GND

LAYOUT: Locate close to Clawhammer socket.

Micro Star Restricted Secret

Title	DDR Terminations Bank 1	Rev 0E
Document Number	MS-6702	
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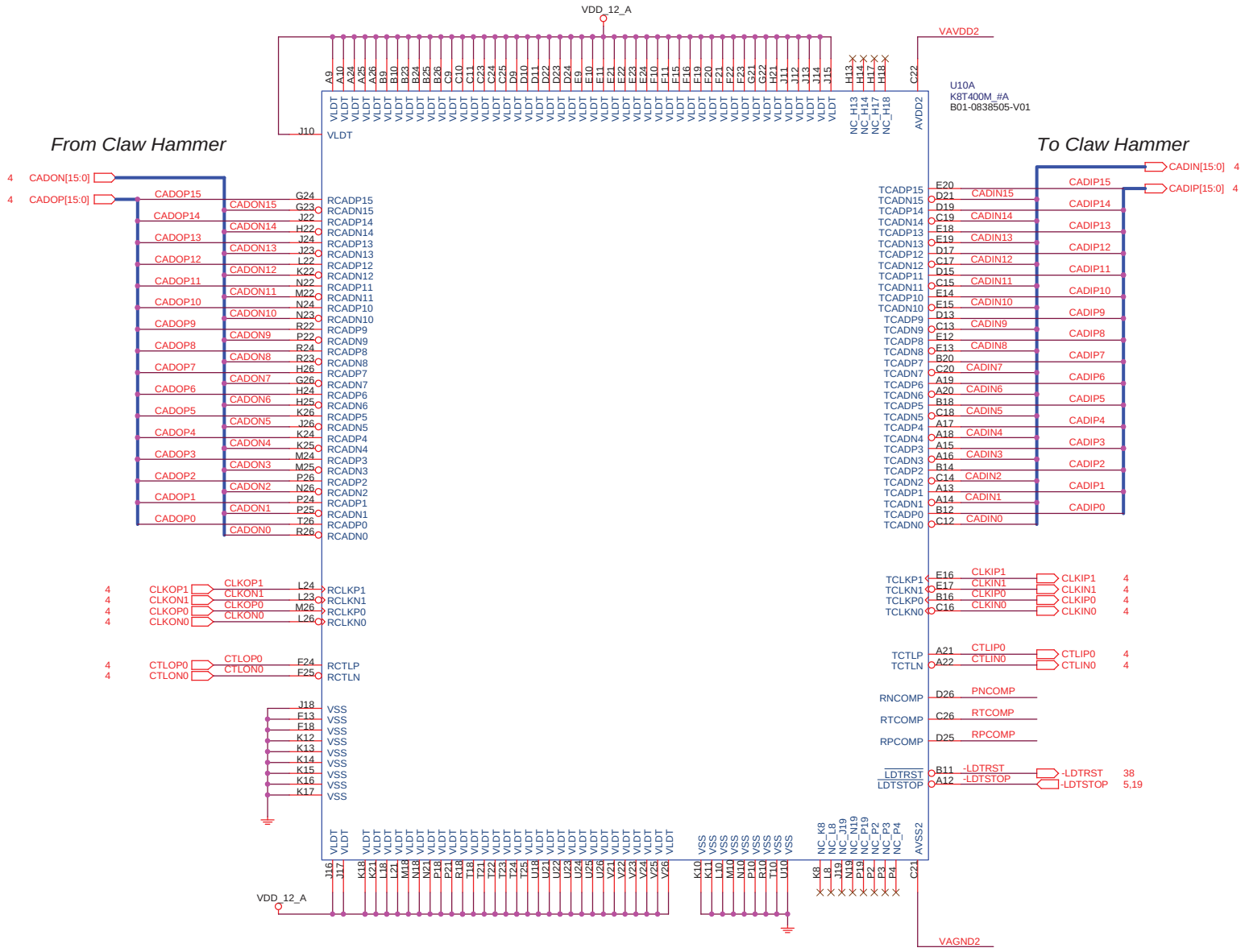
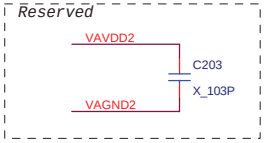
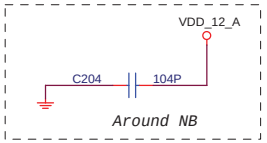
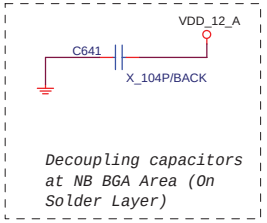
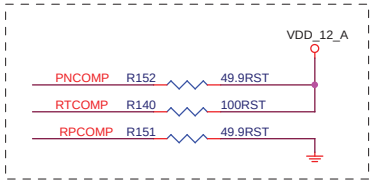
K8T400M HT Interface





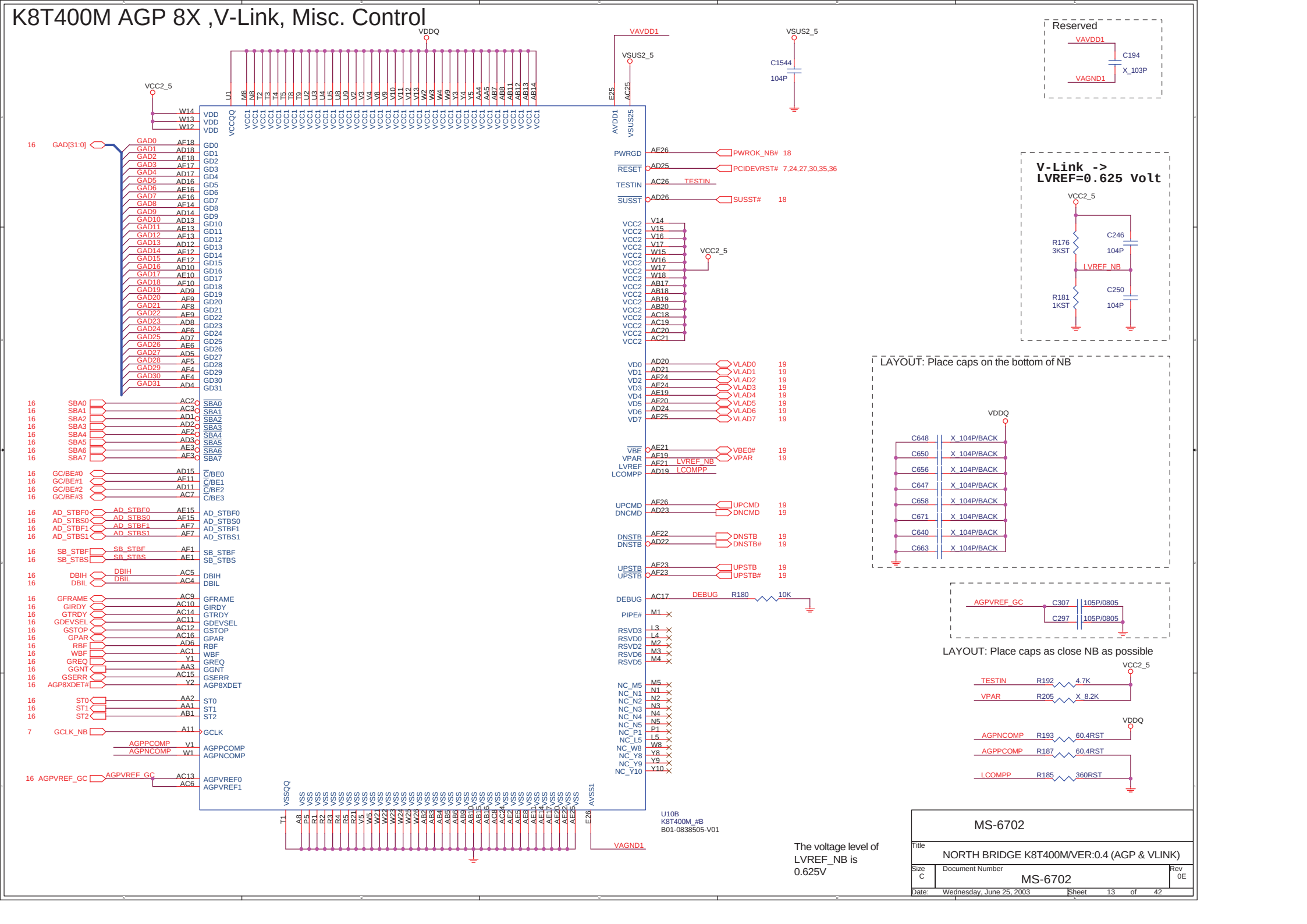






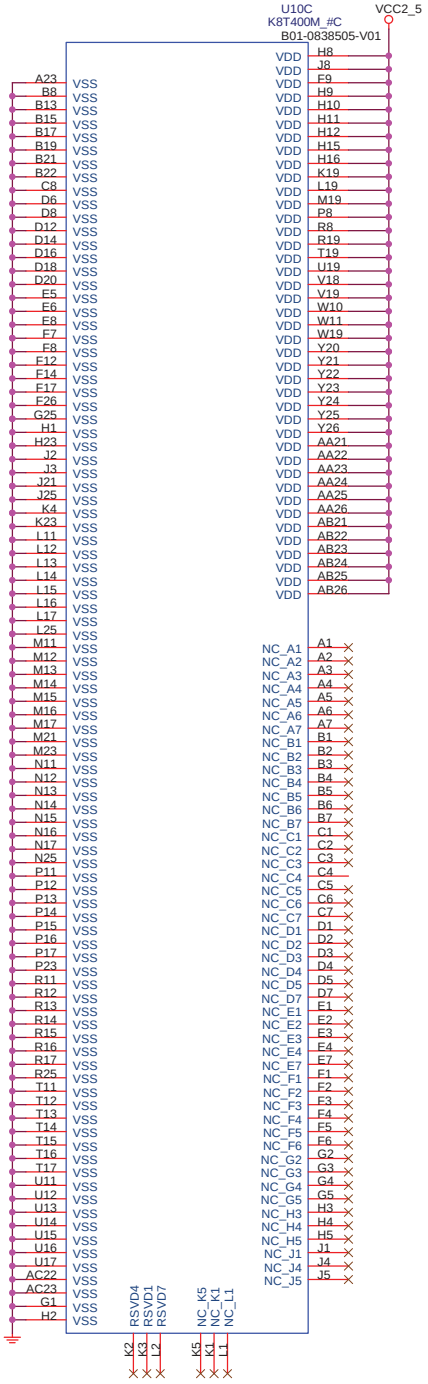
	MS-6702
Title	NORTH BRIDGE K8T400M/VER:0.4 (HT)
Size: C	Document Number: MS-6702
Rev: 0E	
Date: Wednesday, June 25, 2003	Sheet 12 of 42

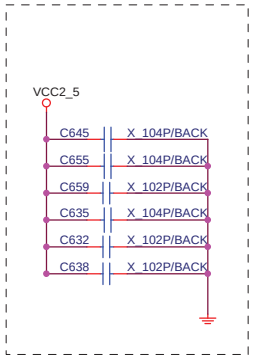
K8T400M AGP 8X ,V-Link, Misc. Control



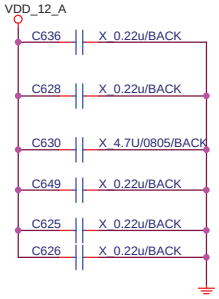
MS-6702	
Title	NORTH BRIDGE K8T400M/VER:0.4 (AGP & VLINK)
Size C	Document Number MS-6702 Rev 0E
Date: Wednesday, June 25, 2003	Sheet 13 of 42

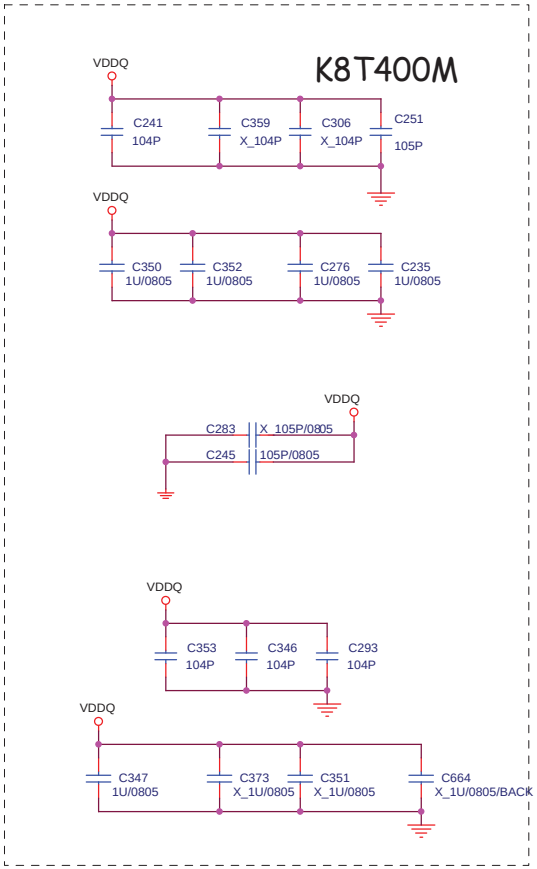
K8T400M Power and Ground Connections





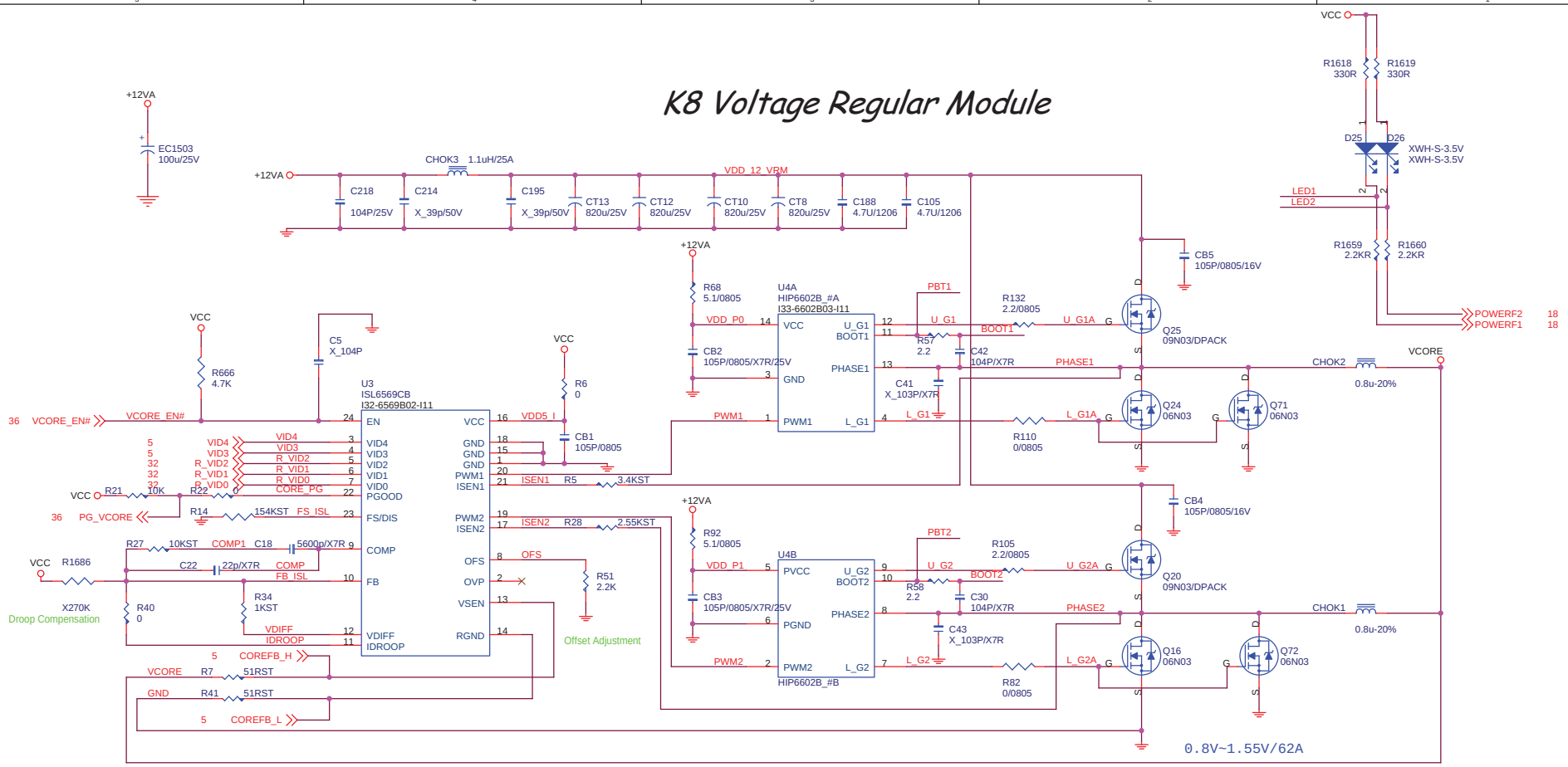
LAYOUT : Popualte caps on the bottom side of NB.





MS-6702			
Title: NORTH BRIDGE K8T400M/VER:0.4 (POWER/GOUND)			
Size: Custom	Document Number: MS-6702		Rev: 0E
Date: Wednesday, June 25, 2003	Sheet 14 of 42		

K8 Voltage Regular Module

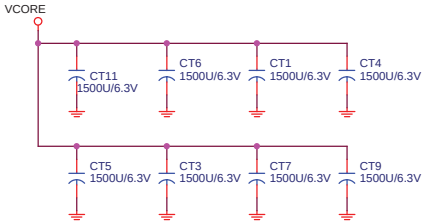


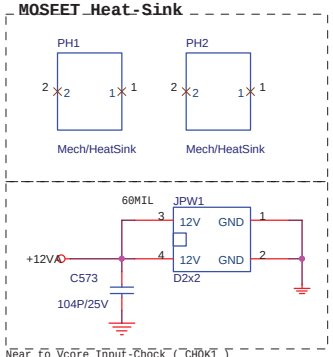
R14 ORIGNAL 154KST R11-1543T13-Y01

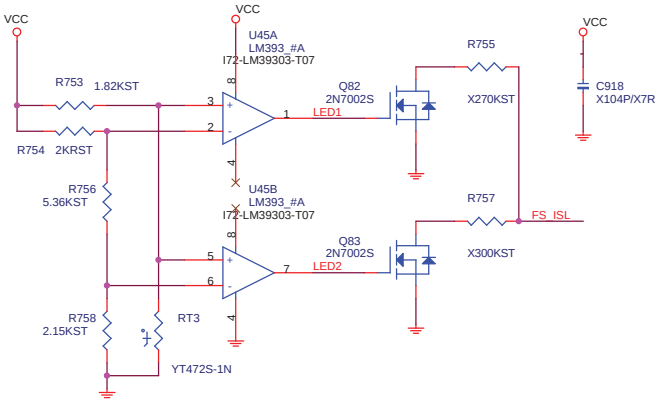
POWER FREQENCY ADIUSTING
300KRST R11-0304T13-Y01

VID4	VID3	VID2	VID1	VID0	Vout
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175

VID4	VID3	VID2	VID1	VID0	Vout
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550
1	1	1	1	1	Shutdown



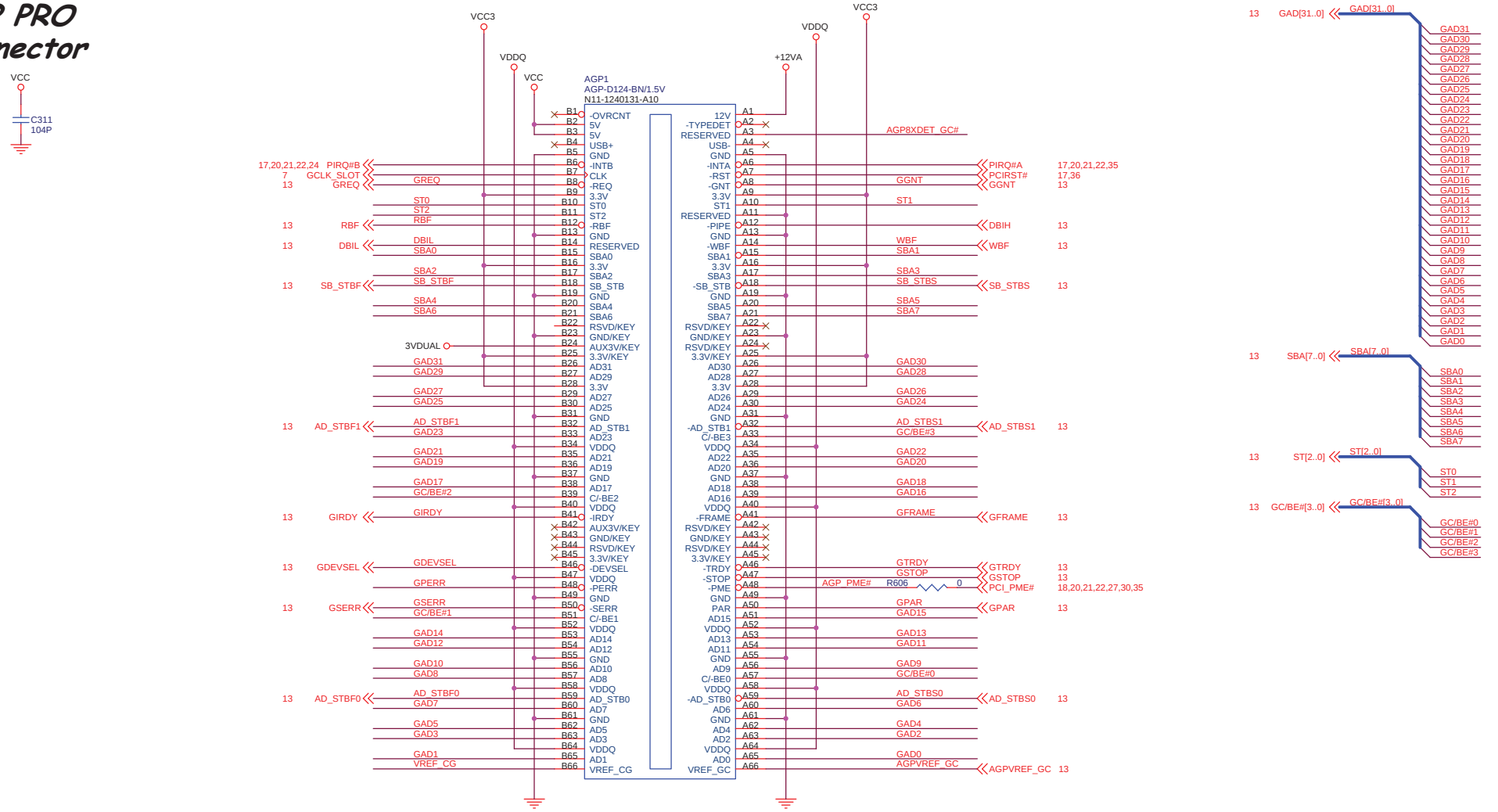


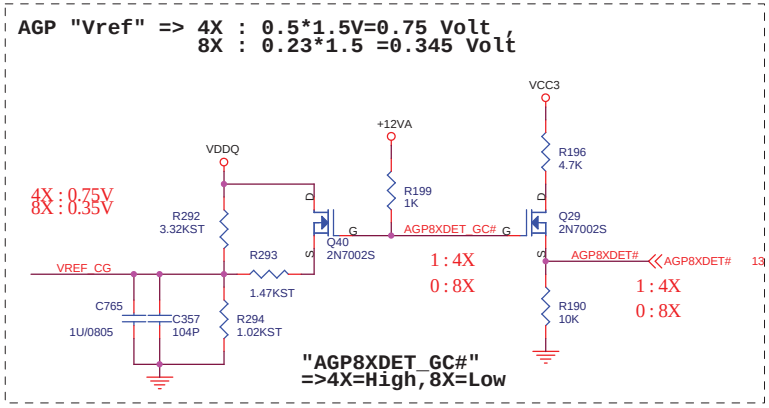


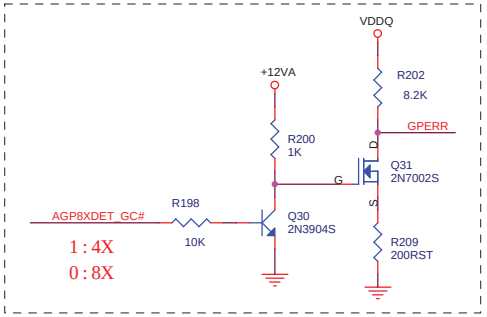
Micro Star Restricted Secret

Title	K8 CORE POWER	Rev 0E
Document Number	MS-6702	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003	Sheet 15 of 42

AGP PRO Connector







Add-in Card Power

	Imax	V_Min	V_Max	Units
VDDQ	2.0A	1.425	1.575	V
VCC3	6.0A	3.15	3.45	V
3VDUAL	0.75A	3.15	3.45	V
VCC5	2.0A	4.75	5.25	V
VCC12	1.0A	11.4	12.6	V

Micro Star Restricted Secret

Title	AGP PRO Slot
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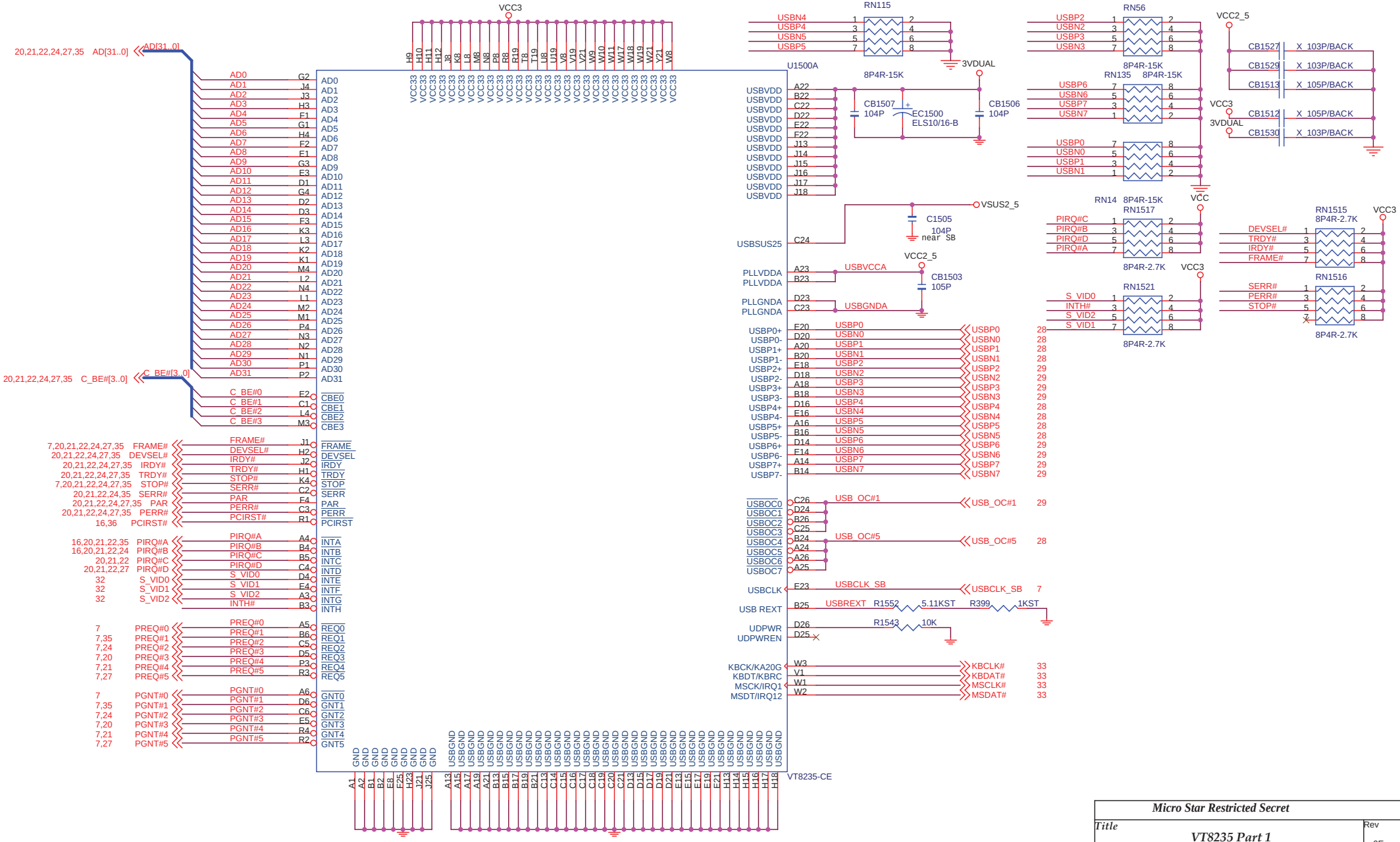
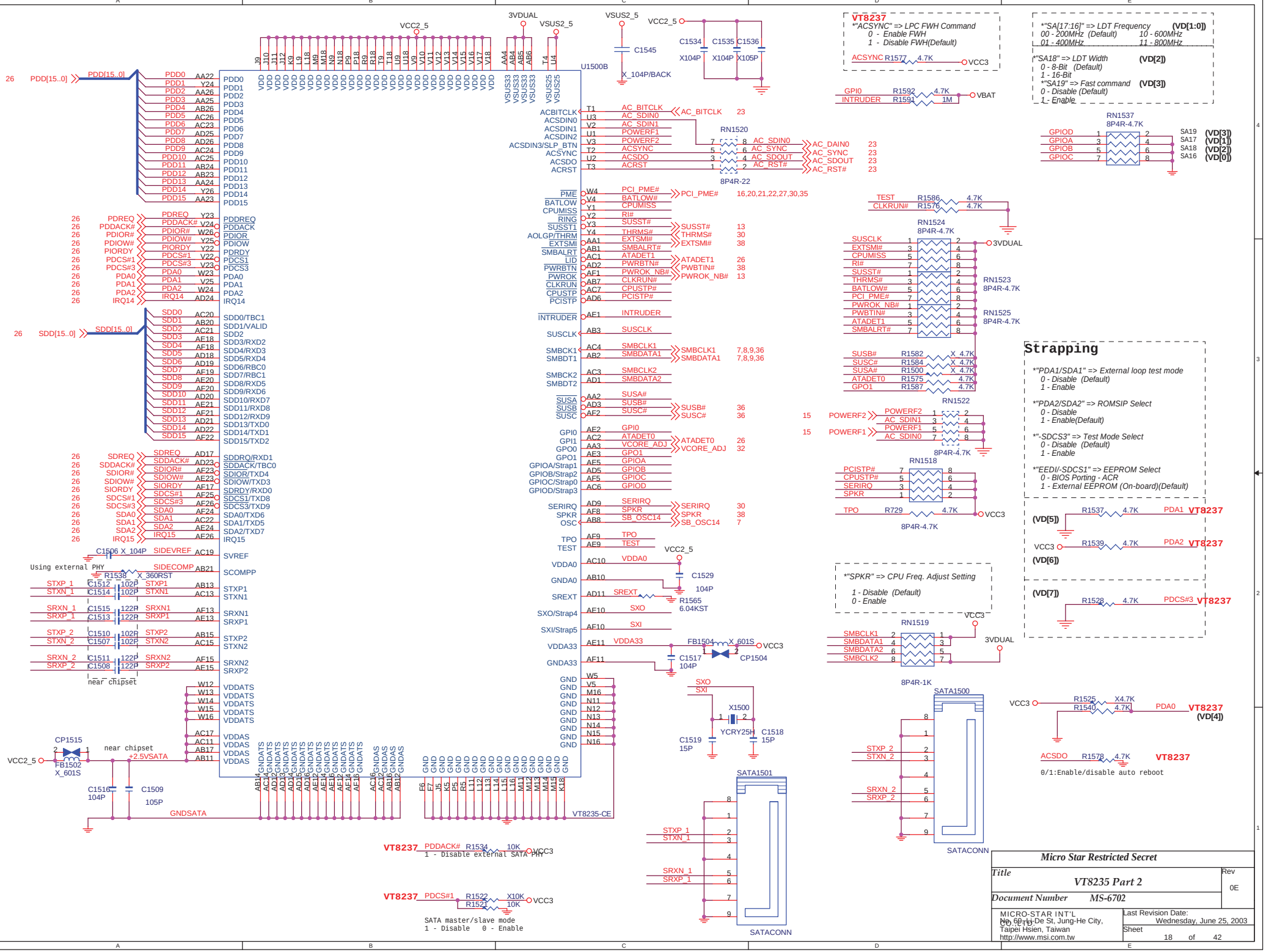


Micro Star Restricted Secret

Title	*VT8235 Part 1*
Rev	0E
Document Number	*MS-6702*
Last Revision Date:	Wednesday, June 25, 2003
Sheet	17 of 42

MICRO-STAR INT'L CO.,LTD
No.69,Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw


U1500B
VT8235-CE
VT8237
*"ACSYNC" => LPC FWH Command
0 - Enable FWH
1 - Disable FWH(Default)
*"SA[17:16]" => LDT Frequency (VD[1:0])
00 - 200MHz (Default) 10 - 600MHz
01 - 400MHz 11 - 800MHz
*"SA18" => LDT Width (VD[2])
0 - 8-Bit (Default)
1 - 16-Bit
*"SA19" => Fast command (VD[3])
0 - Disable (Default)
1 - Enable
Strapping
*"PDA1/SDA1" => External loop test mode
0 - Disable (Default)
1 - Enable
*"PDA2/SDA2" => ROMSIP Select
0 - Disable
1 - Enable(Default)
*"-SDCS3" => Test Mode Select
0 - Disable (Default)
1 - Enable
*"EEDI/-SDCS1" => EEPROM Select
0 - BIOS Porting - ACR
1 - External EEPROM (On-board)(Default)
*"SPKR" => CPU Freq. Adjust Setting
1 - Disable (Default)
0 - Enable
SATA master/slave mode
1 - Disable 0 - Enable
0/1:Enable/disable auto reboot
1 - Disable external SATA PHY
Using external PHY
near chipset
SATACONN
SATA1500
SATA1501
8P4R-22
8P4R-4.7K
8P4R-1K
Micro Star Restricted Secret
Title
VT8235 Part 2
Rev
0E
Document Number
MS-6702
MICRO-STAR INT'L
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
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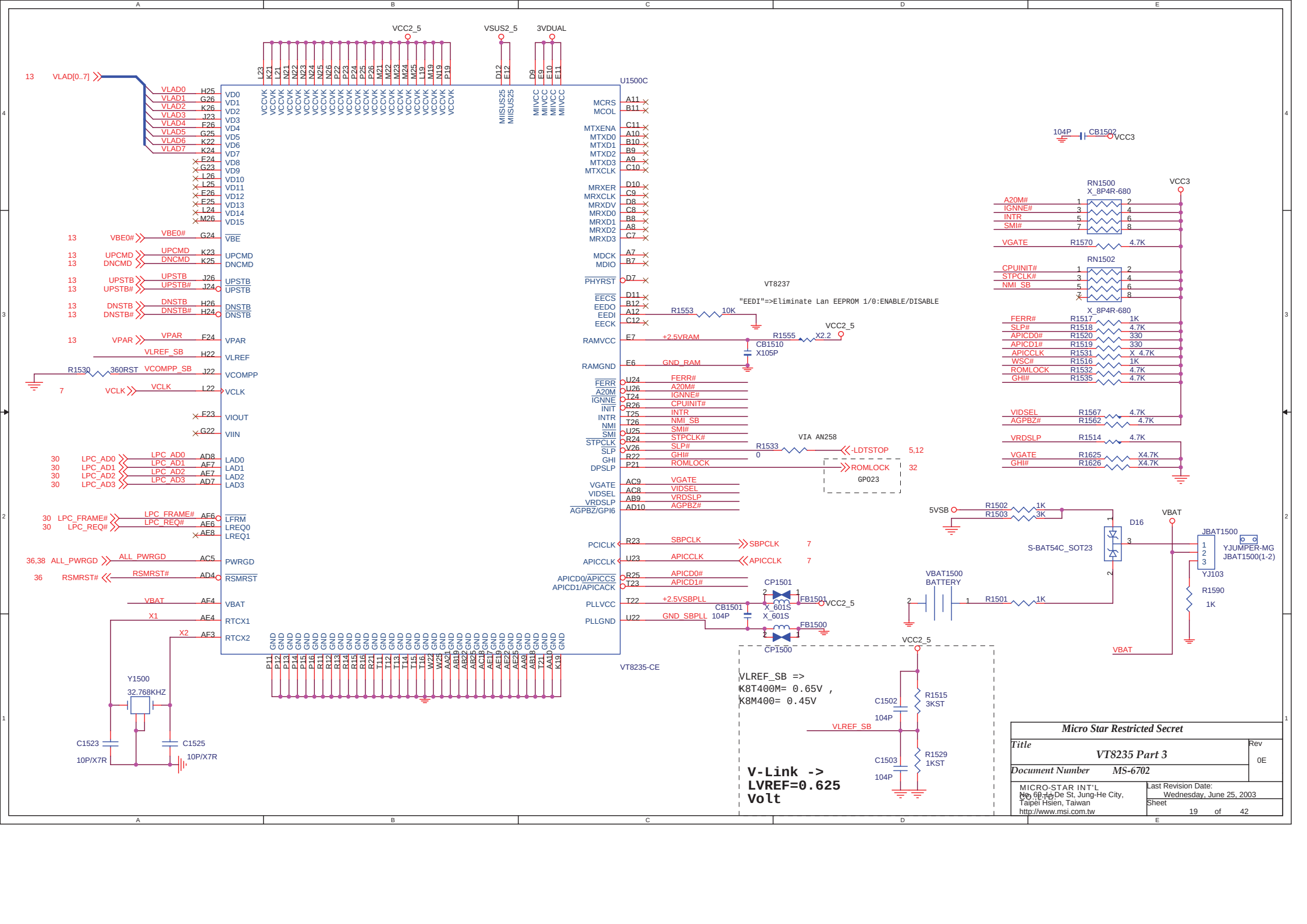
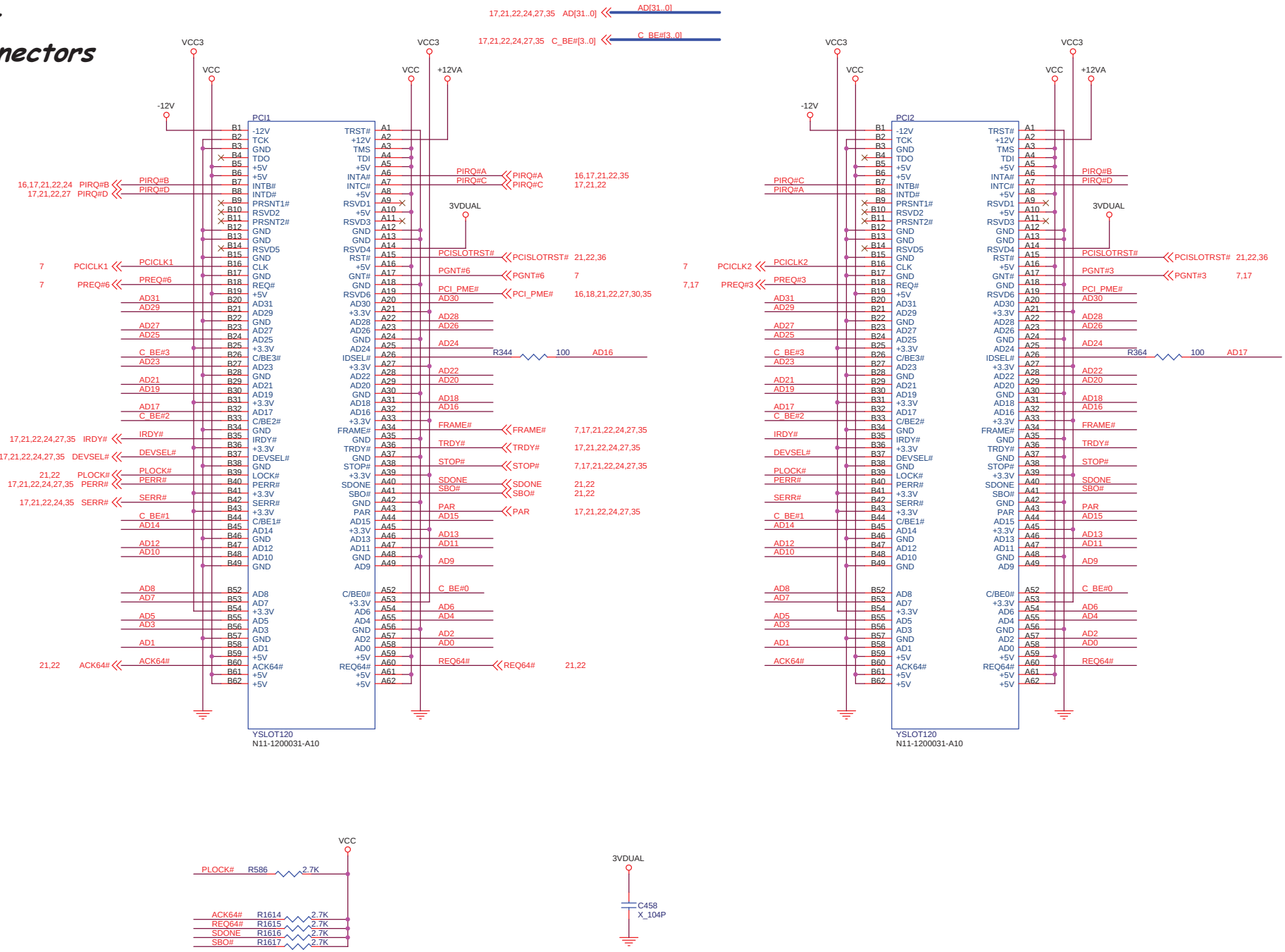


Micro Star Restricted Secret	
Title: VT8235 Part 3	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L CO.,LTD No.69,Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 19 of 42

PCI Connectors



Micro Star Restricted Secret	
Title: PCI Connector 1 & 2	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L CO., LTD. No 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003
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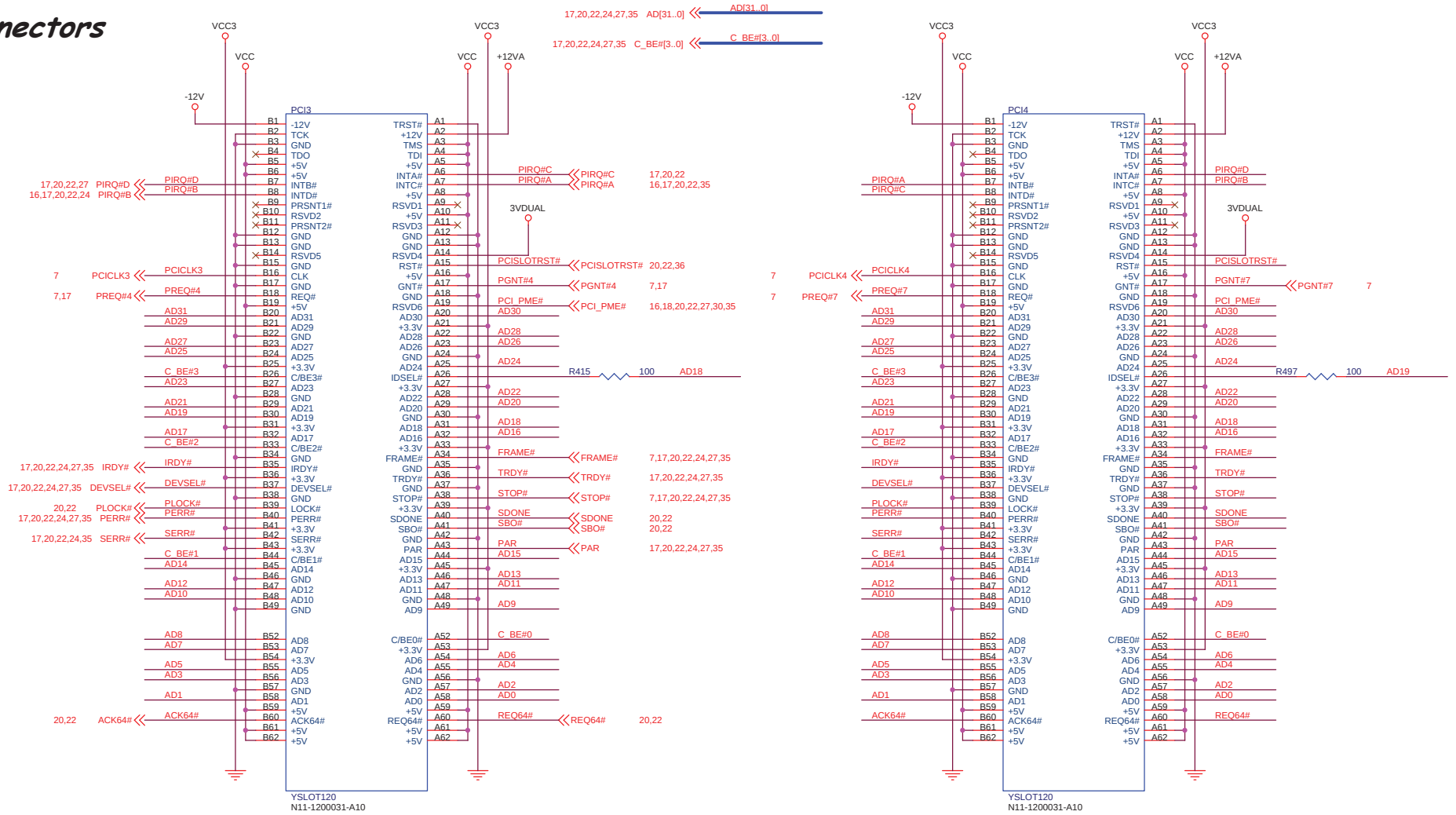
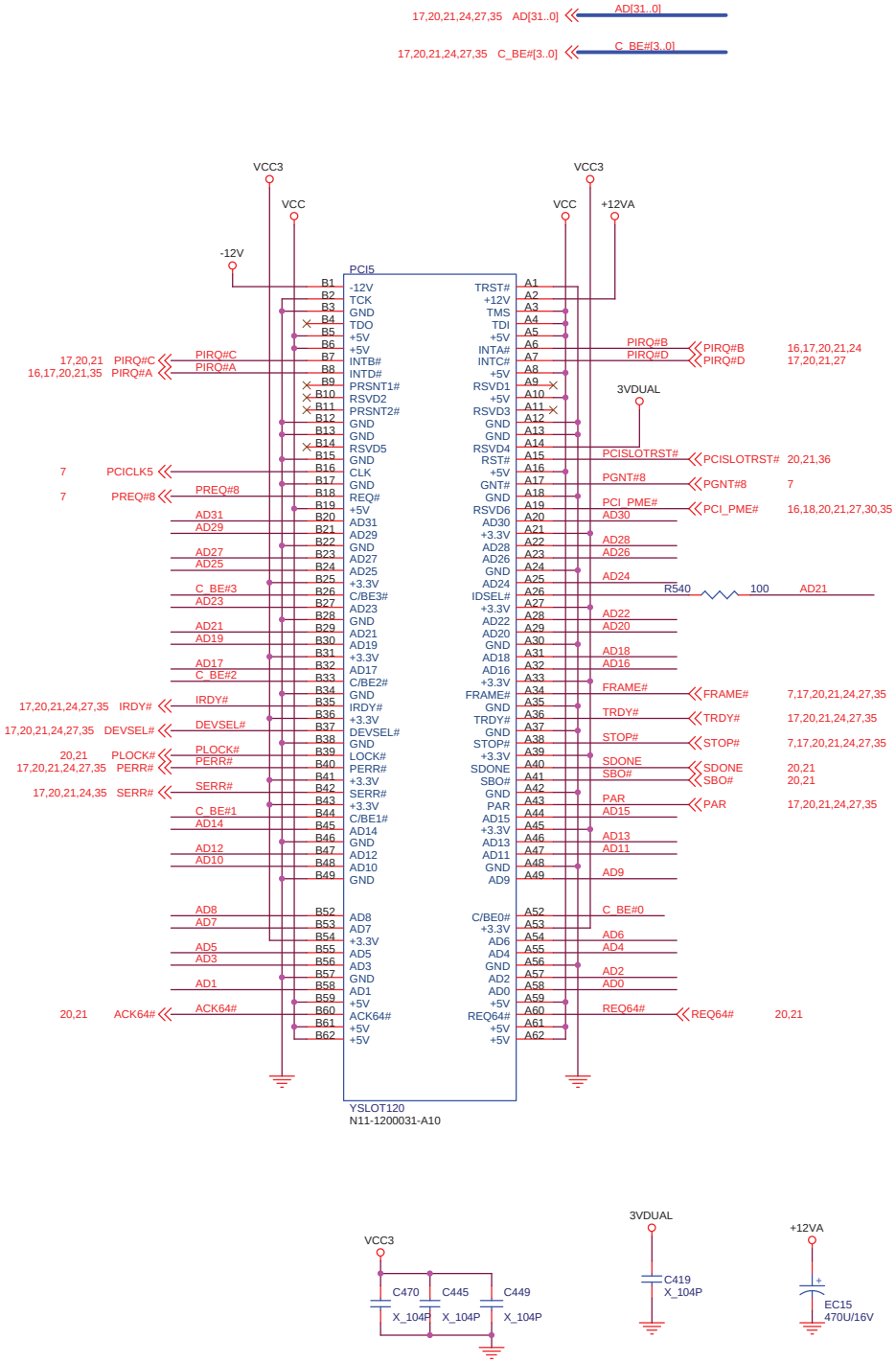
PCI Connectors



Micro Star Restricted Secret	
Title: PCI Connector 3 & 4	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L No 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 21 of 42

PCI Connectors



Micro Star Restricted Secret		
Title: PCI Connector 5		Rev: 0E
Document Number: MS-6702		
MICRO-STAR INT'L NO.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003	Sheet 22 of 42

AUDIO CODEC

CODEC VCC3_3 NEED CAP
AS CLOSE AS POSSIBLE.

For 6 channel codec

C710 105P SROUT_R
C711 105P SROUT_L
C712 105P LFE-OUT
C715 105P CEN-OUT

SPDIFO

C716 104P VCC3

+5VR C718 104P

U40 ALC650/ALC655

DVDD1 XTL_IN XTL_OUT DVSS1 SDATA_OUT BIT_CLK DVSS2 SDATA_IN DVDD2 SYNC RESET# PC_BEEP

NC NC TEST6 TEST5 TEST4 TEST1 AVSS2 AVSS1 TEST2 NC AVDD2 MONO

LOUTR LOUTL NC NC VRDA VRAD AFILT2 AFILT1 NC VREF AVSS1 AVDD1

PHONE AUXL AUXR VIDEOL VIDEOR CDL CDR MIC1 MIC2 LINL LINR

C725 X_10P

7 AC_14

18 AC_SDOUT
18 AC_BITCLK
R676 33
18 AC_DAIN0
18 AC_SYNC
18 AC_RST#

EC55 10U/16V/S LINE_OUT_R
EC56 10U/16V/S LINE_OUT_L
FR_MICIN
C726 1U

VREFOUT

C729 104P
EC57 10U/16V/S
C731 105P
C732 105P
C733 102P
C734 102P
C735 105P
C736 X105P

C738 1U/0805 LINE_IN_R
C739 1U/0805 LINE_IN_L

C744 1U/0805 MICIN2
C741 1U/0805 MICIN1
C748 1U/0805
C750 1U/0805
C751 1U/0805

J8 YJ104-B

JCD

J2B
LINE_NEXT_R
LINE_NEXT_L
C713 102P
C714 102P
LINE_OUT
AUDIO_6CH

J2C
LINE_IN_R
LINE_IN_L
C719 102P
C720 102P
LINE_IN
AUDIO_6CH

VREFOUT R670 4.7K
MICIN2
MICIN1
VREFOUT R677 4.7K
J2A
C727 102P
C728 102P
MIC_IN
AUDIO_6CH

J2D
SROUT_R
SROUT_L
C757 X_102P
C758 X_102P
SR_OUT
AUDIO_6CH

J2E
LFE-OUT
CEN-OUT
C754 X_102P
C755 X_102P
C/W_OUT
AUDIO_6CH

J2F
VCC
SPDIFO
C756 X_102P
SPDIF_OUT
GND
AUDIO_6CH

+12VA
U41 YLT1087S-0.8A
VIN VOUT ADJ
C745 X_104P/12V
R687 100RST
R688 300RST
EC59 100u/16V
+5VR
C746 104P

CP150 X_COPPER
CP36 X_COPPER
CP37 X_COPPER

SPDIFO R1688 100R C1564 103P
R1689 200R
C753 X_102P
USB1B
SPDIF OUT
RCA_USB

JAUDIO

FR_MICIN R1690 X0_S
C1538 X_102P
VREFOUT R697 8.2K_S
LINE_OUT_R
LINE_OUT_L
C760 X_102P
C761 X_102P

JAUD1
MIC MIC_BIAS AUD_FPOUT_R HP_ON AUD_FPOUT_L
AUD_GND AUD_VCC AUD_RET_R CUT AUD_RET_L

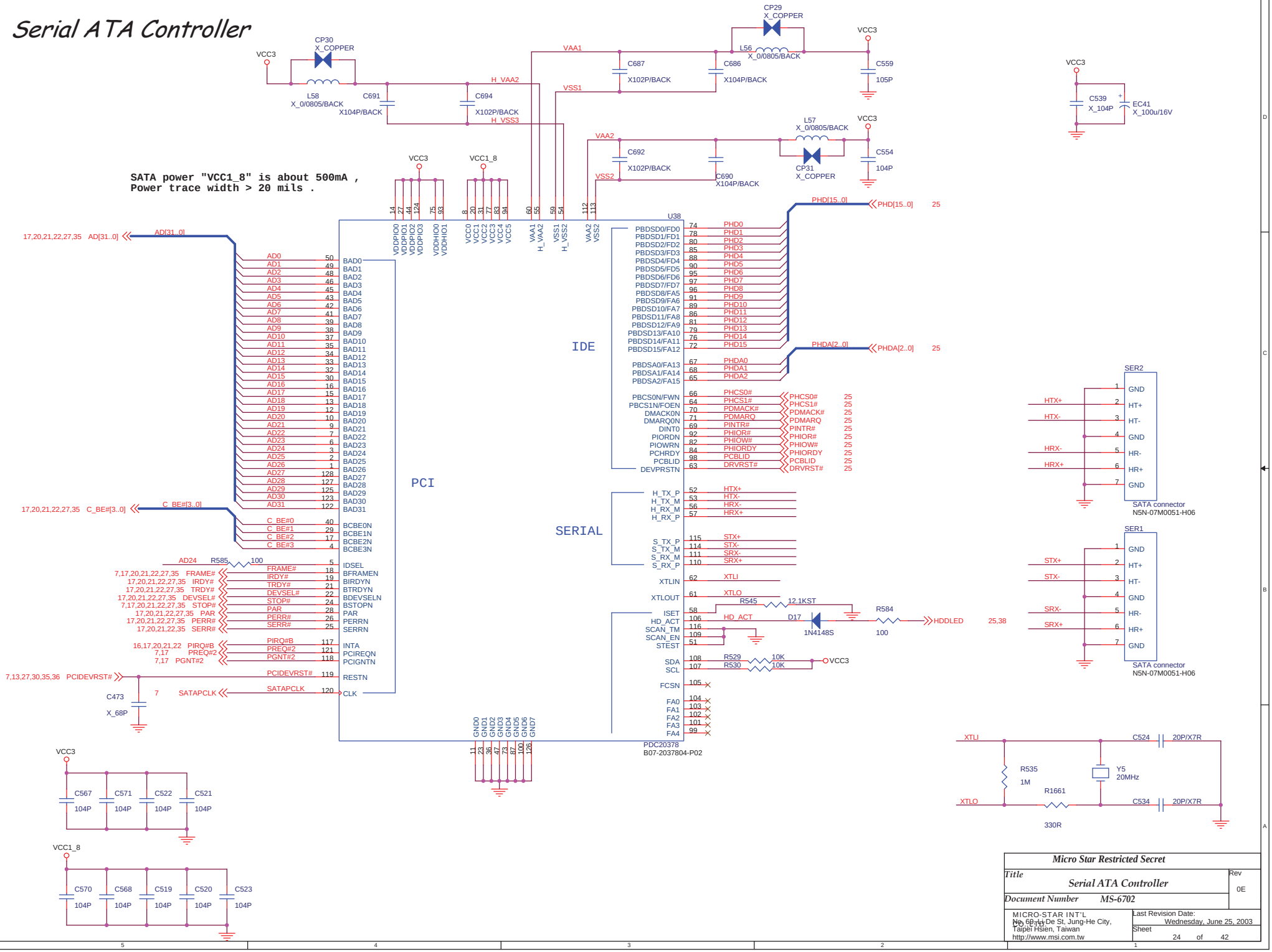
C752 X_102P
+5VR
LINE_NEXT_R
LINE_NEXT_L
C1539 X_102P
C1540 X_102P

JAUD1(5-6) YJUMPER-MG
JAUD1(9-10) YJUMPER-MG

Micro Star Restricted Secret	
Title: C-MEDIA 9739A CODEC	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L No 69-1 De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 23 of 42

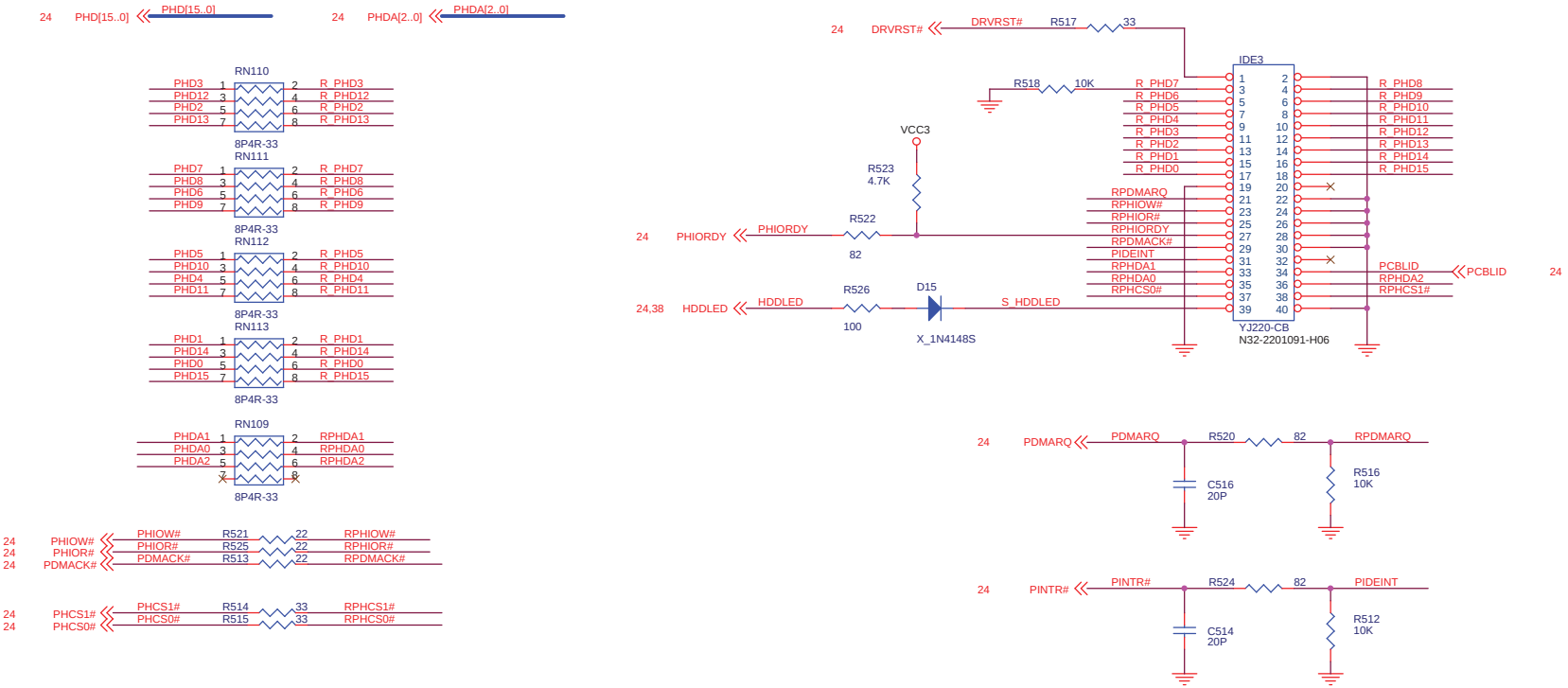
Serial ATA Controller

SATA power "VCC1_8" is about 500mA ,
Power trace width > 20 mils .



Micro Star Restricted Secret	
Title: Serial ATA Controller	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L No.69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 24 of 42

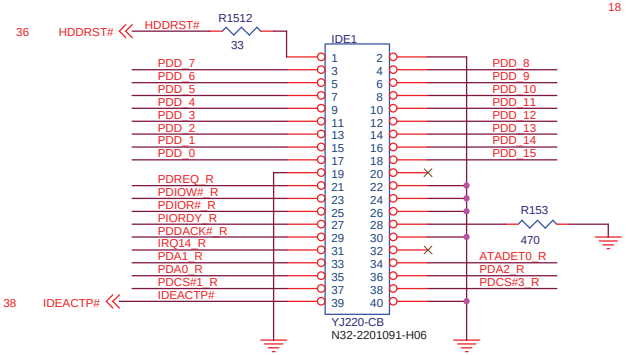
Serial ATA Connector



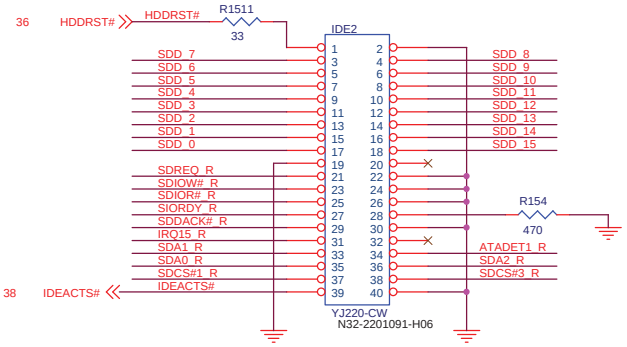
Micro Star Restricted Secret			
Title: Serial ATA Connector			Rev: 0E
Document Number: MS-6702			
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, June 25, 2003 Sheet 25 of 42	

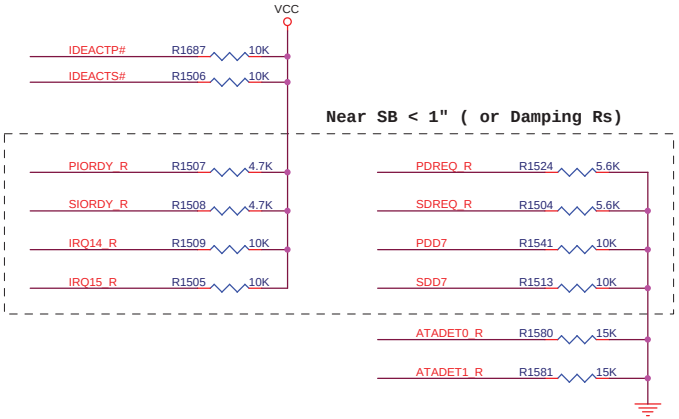
ATA 33/66/100 Connector

PRIMARY IDE CONN.

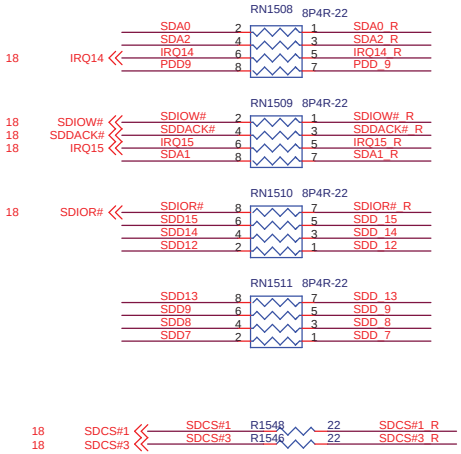


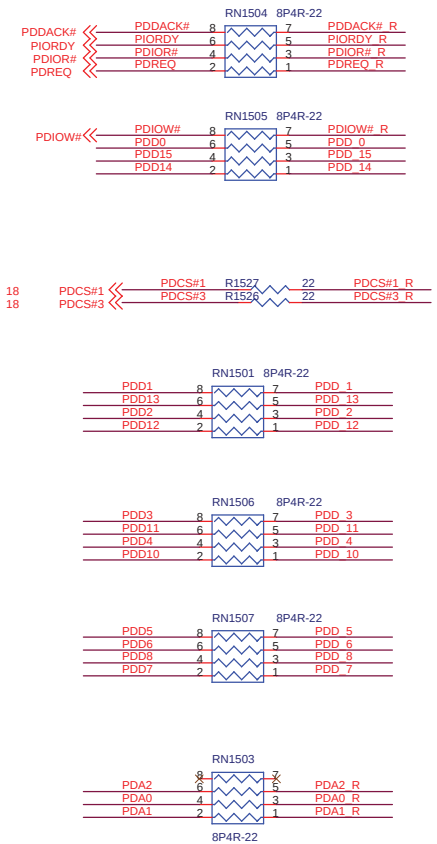
SECONDARY IDE CONN.





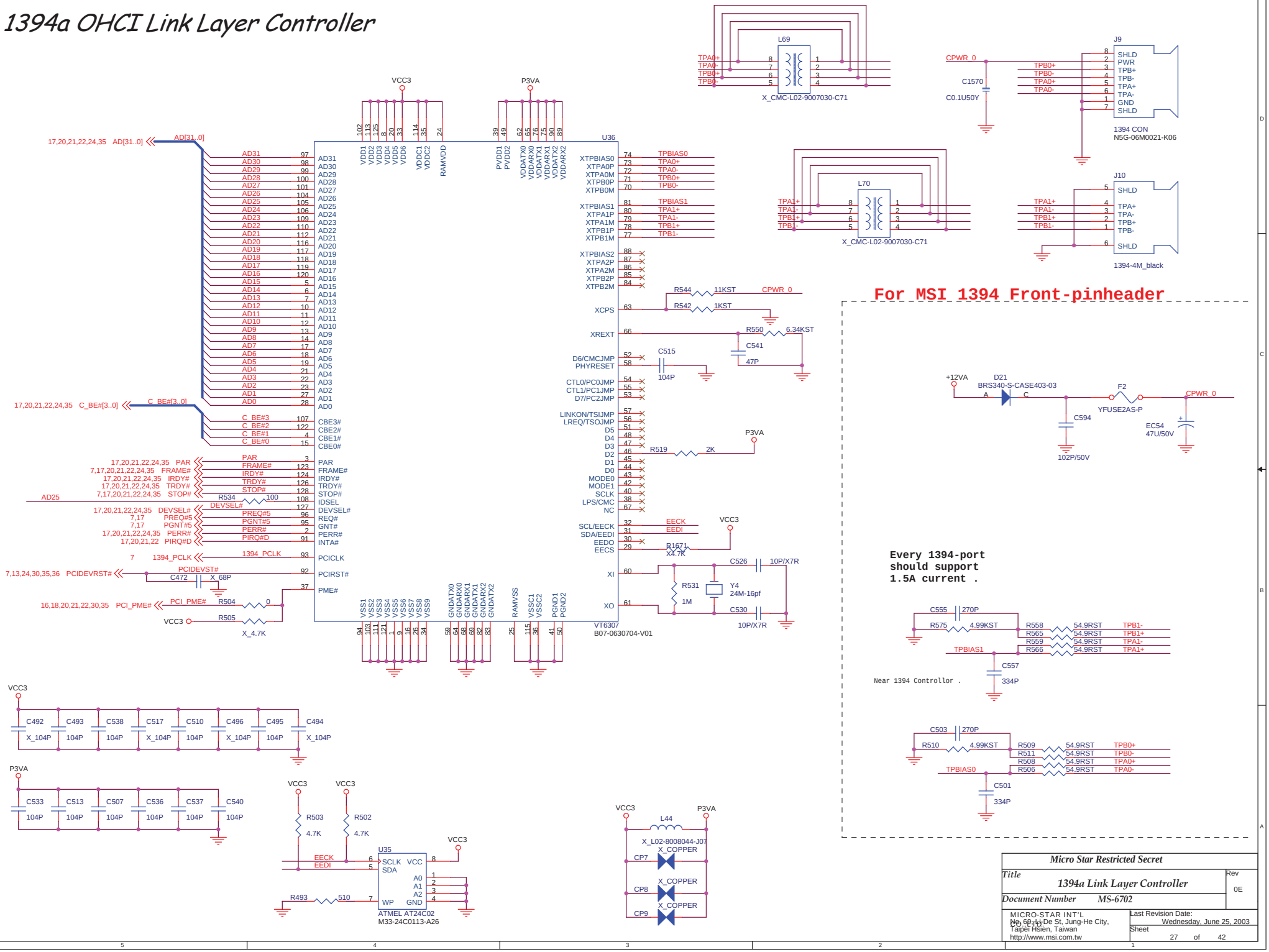
18 PDD[15..0] PDD[15..0]
18 PDA[2..0] PDA[2..0]
18 SDA[2..0] SDA[2..0]
18 SDD[15..0] SDD[15..0]



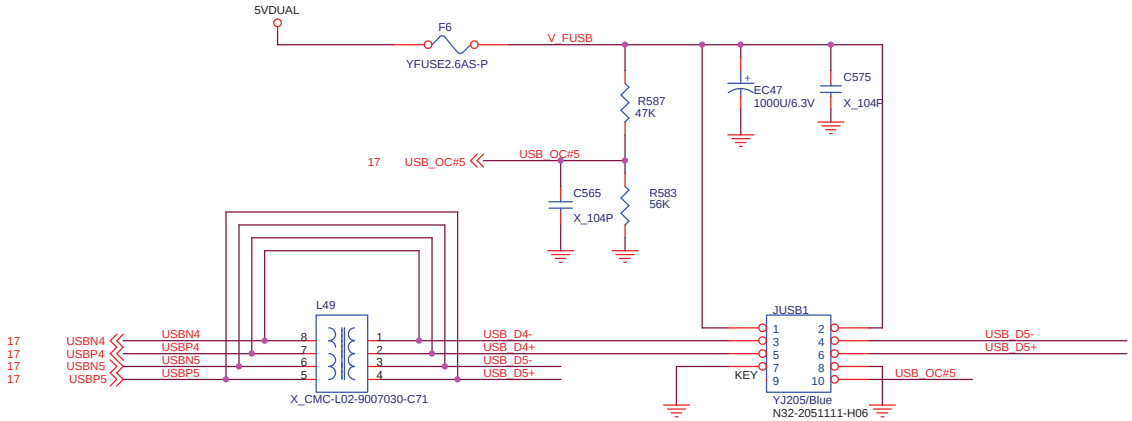


Micro Star Restricted Secret		
Title: ATA 33/66/100 Connector		Rev: 0E
Document Number: MS-6702		
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 26 of 42	

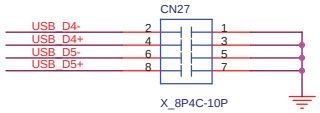
1394a OHCI Link Layer Controller

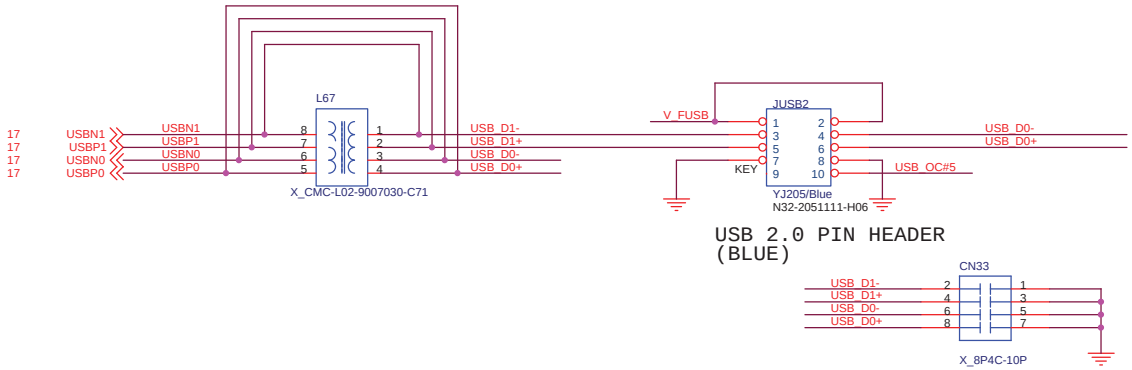


FRONT USB PORT



USB 2.0 PIN HEADER
(BLUE)



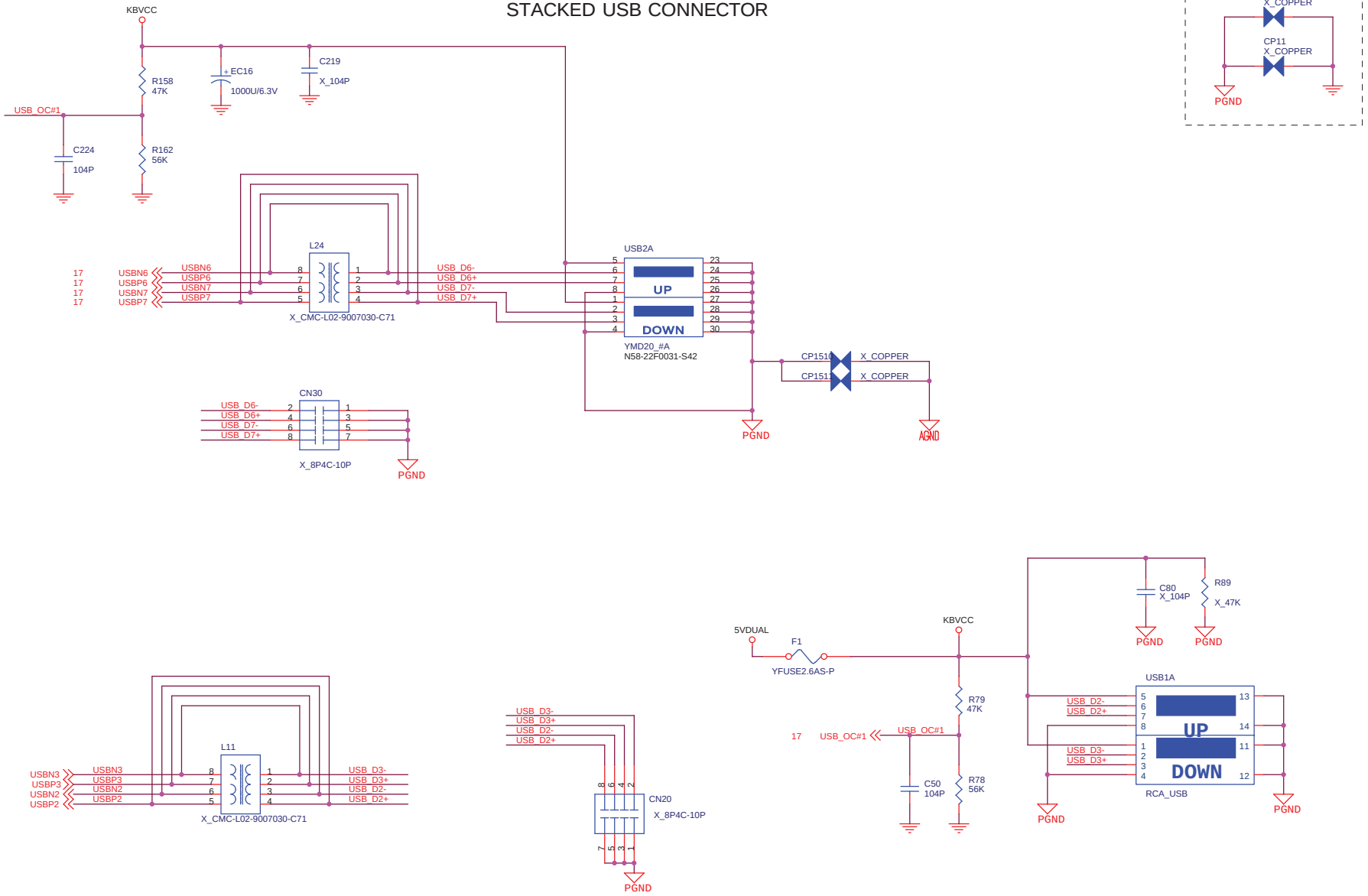


USB 2.0 PIN HEADER
(BLUE)

Micro Star Restricted Secret		
Title	*Front USB Port*	Rev 0E
Document Number	*MS-6702*	
MICRO-STAR INT'L No.69-1, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, June 25, 2003 Sheet 28 of 42

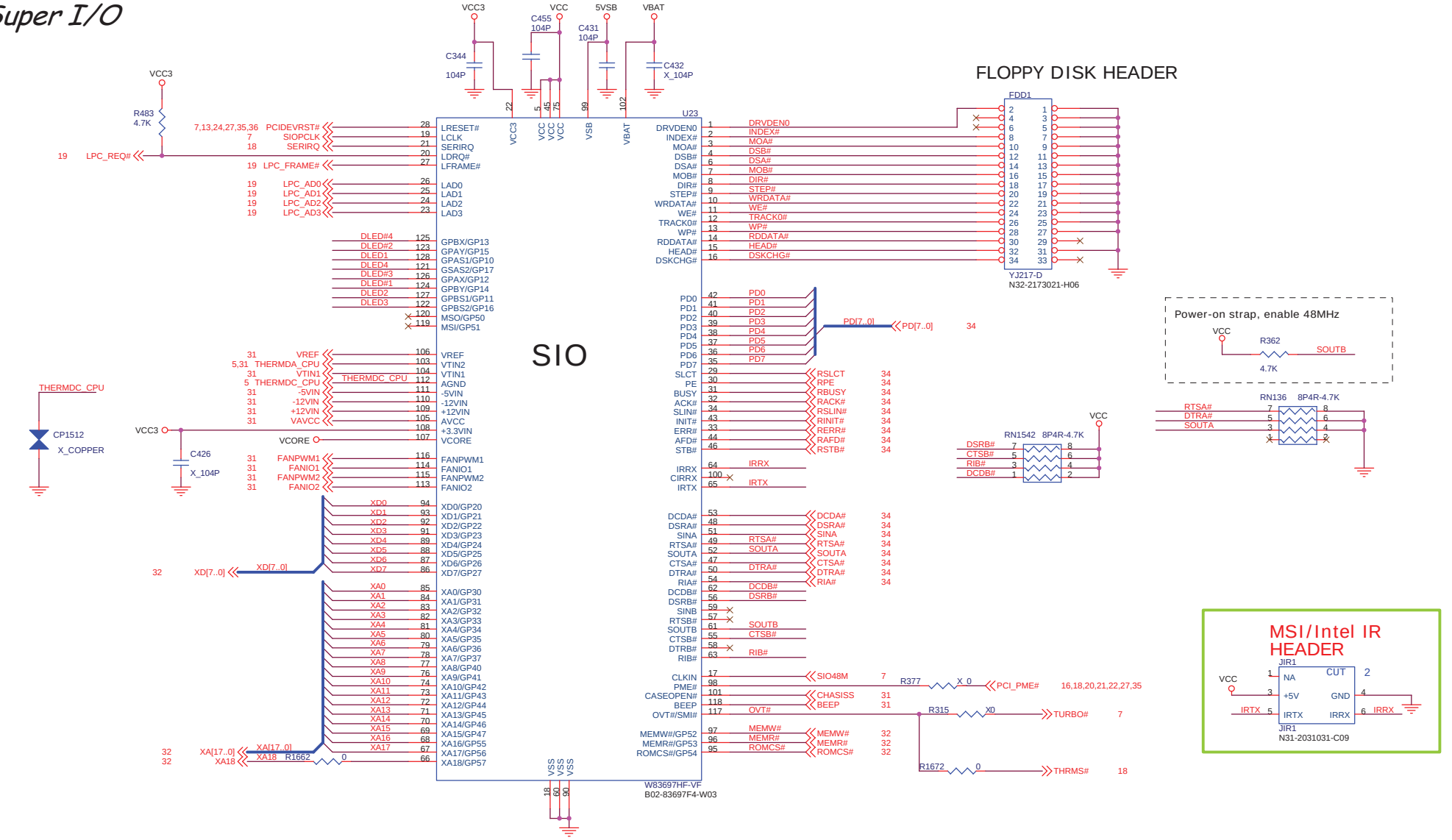
REAR USB PORT

STACKED USB CONNECTOR



Micro Star Restricted Secret	
Title: Rear USB Port	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L No.69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 29 of 42

Super I/O


VCC3
VCC
5VSB
VBAT
C344 104P
C455 104P
C431 104P
C432 X_104P
R483 4.7K
U23
SIO
W83697HF-VF
B02-83697F4-W03
LRESET#
LCLK
SERIRQ
LDRQ#
LFRAME#
LAD0
LAD1
LAD2
LAD3
GPBX/GP13
GPAY/GP15
GPAS1/GP10
GSAS2/GP17
GPAX/GP12
GPBY/GP14
GPBS1/GP11
GPBS2/GP16
MSO/GP50
MSI/GP51
VREF
VTIN2
VTIN1
AGND
-5VIN
-12VIN
+12VIN
AVCC
+3.3VIN
VCORE
FANPWM1
FANIO1
FANPWM2
FANIO2
XD0/GP20
XD1/GP21
XD2/GP22
XD3/GP23
XD4/GP24
XD5/GP25
XD6/GP26
XD7/GP27
XA0/GP30
XA1/GP31
XA2/GP32
XA3/GP33
XA4/GP34
XA5/GP35
XA6/GP36
XA7/GP37
XA8/GP40
XA9/GP41
XA10/GP42
XA11/GP43
XA12/GP44
XA13/GP45
XA14/GP46
XA15/GP47
XA16/GP55
XA17/GP56
XA18/GP57
DRVDEN0
INDEX#
MOA#
DSB#
DSA#
MOB#
DIR#
STEP#
WRDATA#
WE#
TRACK0#
WP#
RDDATA#
HEAD#
DSKCHG#
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
SLCT
PE
BUSY
ACK#
SLIN#
INIT#
ERR#
AFD#
STB#
IRRX
CIRRX
IRTX
DCDA#
DSRA#
SINA
RTSA#
SOUTA
CTSA#
DTRA#
RIA#
DCDB#
DSRB#
SINB
RTSB#
SOUTB
CTSB#
DTRB#
RIB#
CLKIN
PME#
CASEOPEN#
BEEP
OVT#/SMI#
MEMW#/GP52
MEMR#/GP53
ROMCS#/GP54
RSLCT
RPE
RBUSY
RACK#
RSLIN#
RINIT#
RERR#
RAFD#
RSTB#
SIO48M
CHASISS
OVT#
MEMW#
MEMR#
ROMCS#
PCI_PME#
TURBO#
THRMS#
R377 X_0
R315 X0
R1672 0
R1662 0
FLOPPY DISK HEADER
FDD1
YJ217-D
N32-2173021-H06
Power-on strap, enable 48MHz
R362 4.7K
SOUTB
RN136 8P4R-4.7K
RN1542 8P4R-4.7K
MSI/Intel IR HEADER
JIR1
NA
CUT
+5V
GND
IRTX
IRRX
N31-2031031-C09
THERMDC_CPU
CP1512
X_COPPER
C426 X_104P
DELD
Distribute near the VCC power pin of the LPC
C427 X_104P
C405 X_104P
C547 X_104P
JLED
YJ205
N31-2051051-P05
RN118
RN119
8P4R-680
Micro Star Restricted Secret
Winbond W697HF
0E
MS-6702
MICRO-STAR INT'L
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Wednesday, June 25, 2003
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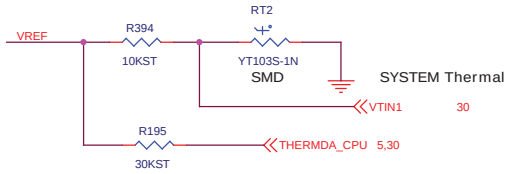
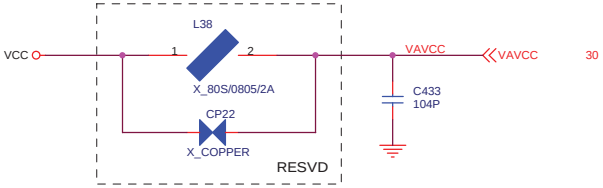
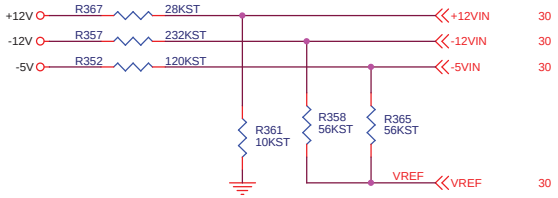
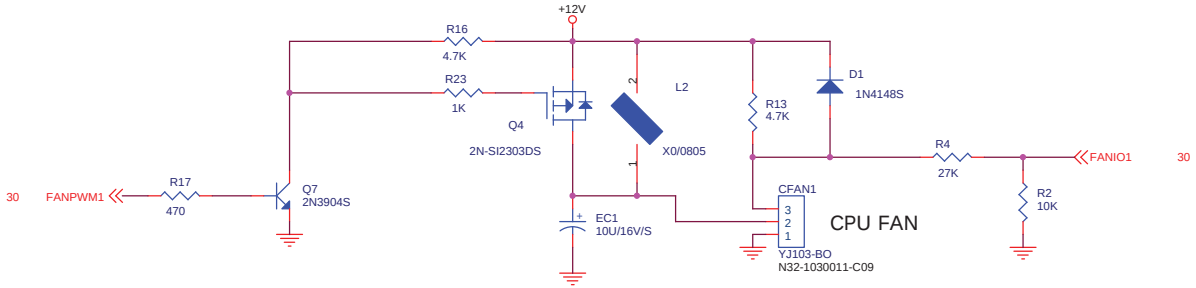
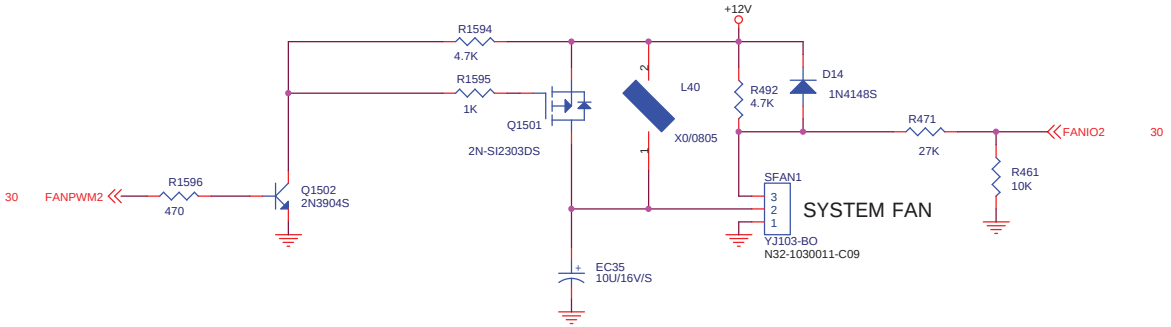
Hardware Monitor



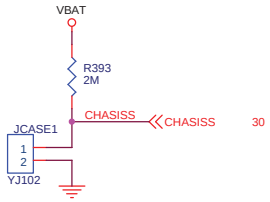


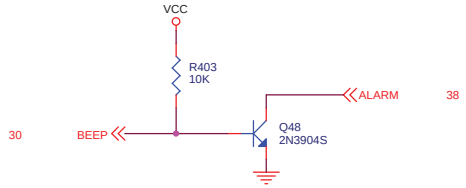


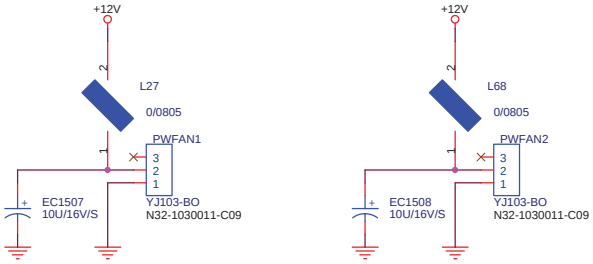




Chasiss Intrusion Header

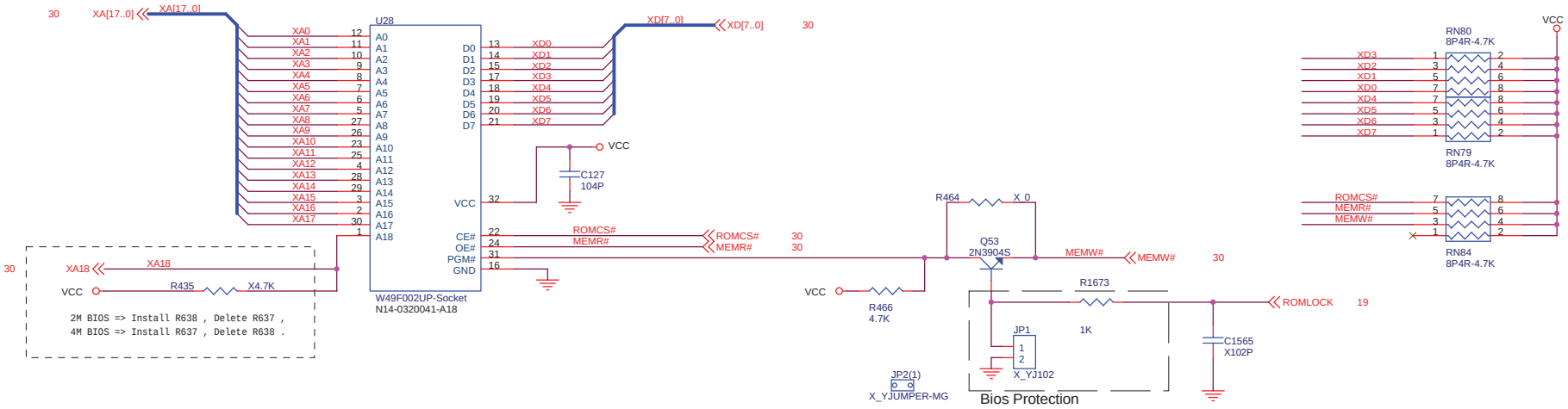


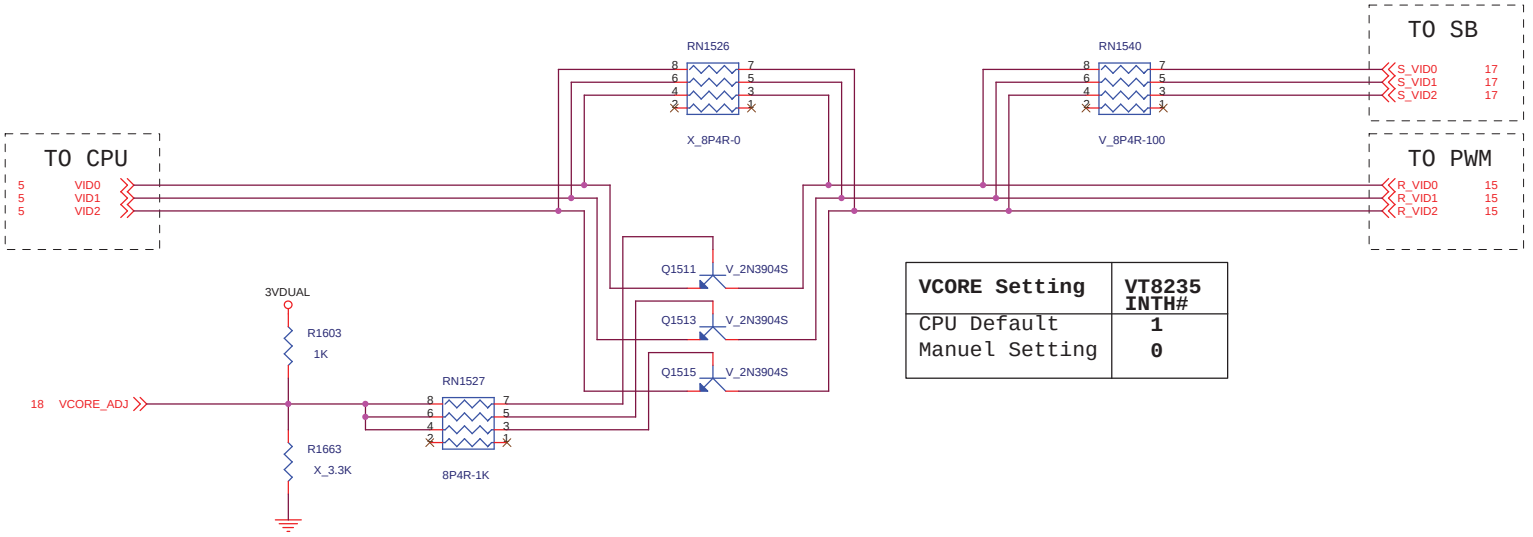




Micro Star Restricted Secret		
Title: Hardware Monitor		Rev: 0E
Document Number: MS-6702		
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 31 of 42	

SYSTEM ROM



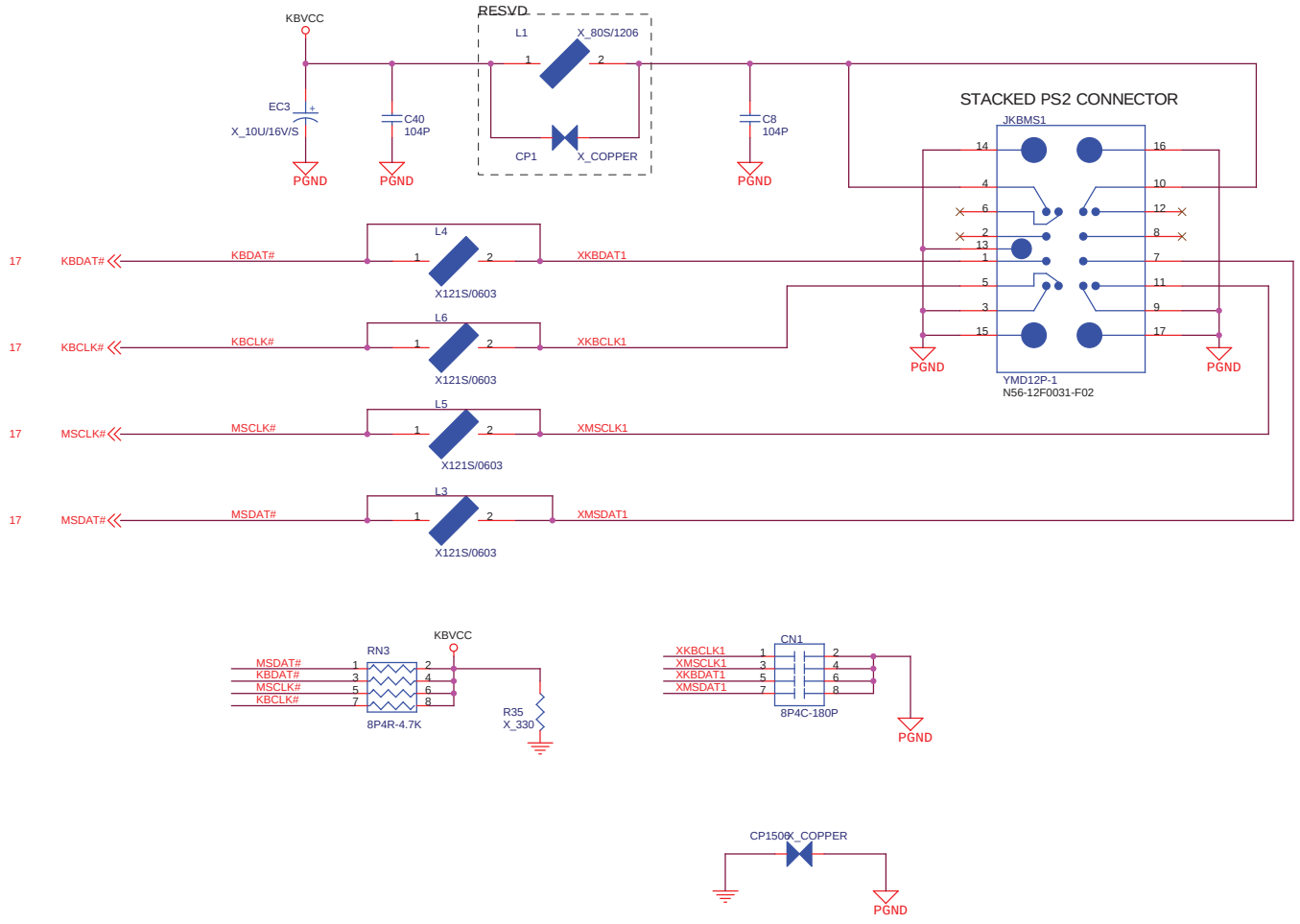


VCORE Setting	VT8235 INTH#
CPU Default	1
Manuel Setting	0

Micro Star Restricted Secret

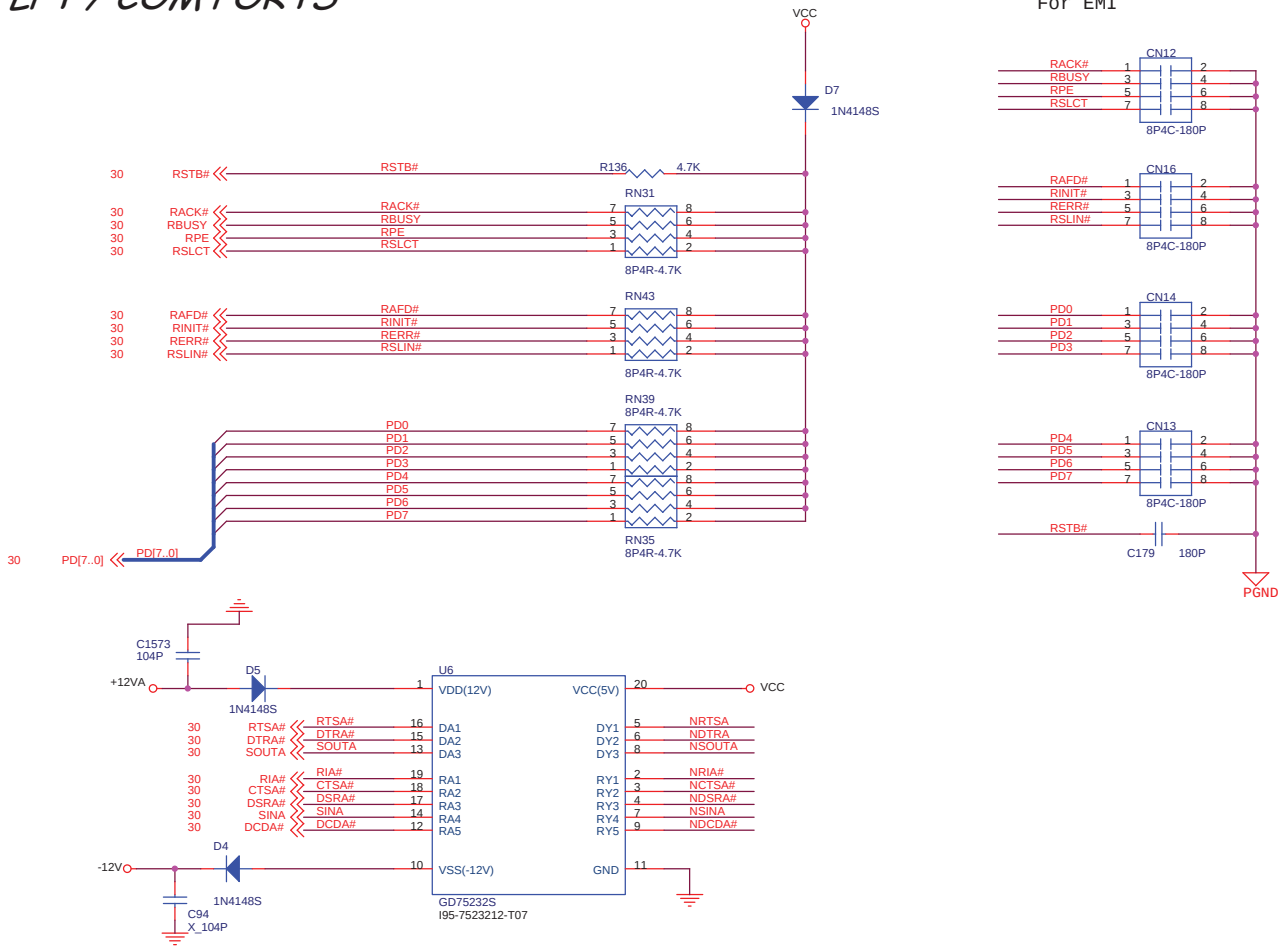
Title: SYSTEM ROM & VCORE ADJUSTING	Rev: 0E
Document Number: MS-6702	
MICRO-STAR INT'L CO.,LTD. No.69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003
	Sheet 32 of 42

Keyboard/Mouse Ports



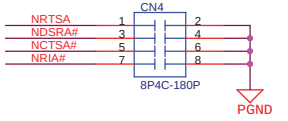
Micro Star Restricted Secret		
Title: KeyBoard/Mouse Port		Rev: 0E
Document Number: MS-6702		
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 33 of 42	

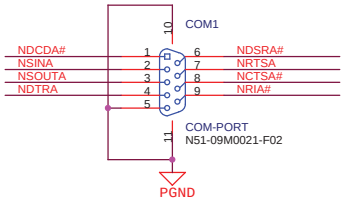
LPT / COM PORTS

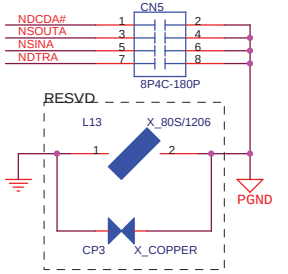


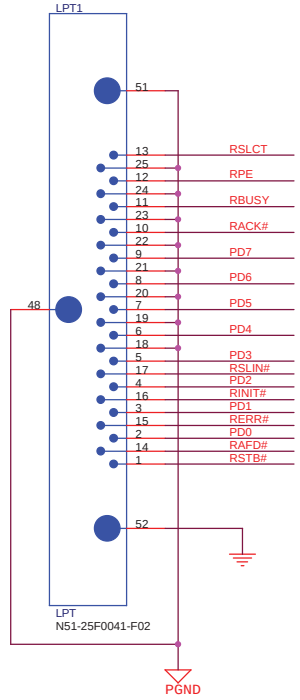
For EMI

Multiple RS232 Drivers and Receivers









Micro Star Restricted Secret		
Title	*LPT / COM Port*	Rev 0E
Document Number	*MS-6702*	
MICRO-STAR INT'L No 69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003	
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RTL8110S STUFF R1677,R1675,R1678

RTL8100C STUFF R1674,R1676

RTL8110S X
RTL8100C 0 OHM
VAUX_18 R1674 VDD25
X0/0805

RTL8110S 0 OHM
RTL8100C X
3VDUAL R1675 VDDH
X0/0805

RTL8110S X
RTL8100C 0 OHM
3VDUAL R1676 VAUX_25
X0/0805

3VDUAL
C334 104P
C315 104P
C291 104P

VAUX_18
C340 104P
C355 104P
C299 102P
C298 104P

Place near GIGA-bits PCI controlor .

VAUX_25
C333 104P
C314 104P
C338 104P

VCC3
C377 104P
C378 104P
C360 104P

Place near Controllor

RTL8110S 0 OHM
RTL8100C X
VAUX_18 R1677
X0/0805
R1679 0

VAUX_18 VDDH 3VDUAL VAUX_25
VDD25

R1678
0
RTL8110S 0 OHM
RTL8100C X

C1566 103P
C1567 103P
C1568 103P
C1569 103P

R236 49.9RST X-F
R243 49.9RST X-F
R260 49.9RST X-F
R270 49.9RST X-F
R225 49.9RST
R242 49.9RST
R259 49.9RST
R269 49.9RST

U20

17,20,21,22,24,27 AD[31..0]

AD0 104
AD1 103
AD2 102
AD3 98
AD4 97
AD5 96
AD6 95
AD7 93
AD8 90
AD9 89
AD10 87
AD11 86
AD12 85
AD13 83
AD14 82
AD15 79
AD16 59
AD17 58
AD18 57
AD19 55
AD20 53
AD21 50
AD22 49
AD23 47
AD24 43
AD25 42
AD26 40
AD27 39
AD28 37
AD29 36
AD30 34
AD31 33

17,20,21,22,24,27 C_BE#[3..0]

C_BE#0 92
C_BE#1 77
C_BE#2 60
C_BE#3 44

16,17,20,21,22 PIRQ#A 25
7,17 PREQ#1 30
7,17 PGNT#1 29
7 GLAN_PCLK 28
7,13,24,27,30,36 PCIDEVRST# 27
16,18,20,21,22,27,30 PCI_PME# 31
17,20,21,22,24,27 DEVSEL# 68
7,17,20,21,22,24,27 FRAME# 61
17,20,21,22,24,27 IRDY# 63
17,20,21,22,24,27 TRDY# 67
17,20,21,22,24,27 PAR 76
17,20,21,22,24 SERR# 75
17,20,21,22,24,27 PERR# 70
7,17,20,21,22,24,27 STOP# 69

AD22 R296 100 46
R284 5.9K1% 127

RTL8100C R824=5.9K
RTL8110S R824=2.49K

NC VDD18/NC 11
VDD18/NC 126
VDD18/NC 116
VDD18/NC 110
VDD18/NC 64
VDD18/NC 45
VDD18/NC 24

VDD18/VDD25 99
VDD18/VDD25 58
VDD18/VDD25 54
VDD18/VDD25 32

NC/AVDD25 12
AVDDH/NC 120
AVDDH/NC 10

VDD33 107
VDD33 84
VDD33 71
VDD33 56
VDD33 41
VDD33 26

AVDDUAVDD33 20
AVDDUAVDD33 7
AVDDUAVDD33 3

AVDDL/NC 16

MDI0+/TX+ 1 MX0+
MDI0-/TX- 2 MX0-
MDI1+/RX+ 5 MX1+
MDI1-/RX- 6 MX1-
MDI2+/NC 14 MX2+
MDI2-/NC 15 MX2-
MDI3+/NC 18 MX3+
MDI3-/NC 19 MX3-

LANWAKEUP 105
LED0 117 LED_TRAFFIC
LED1 115
LED2 114 LINK10/100#
LED3/NC 113 LINK1G#

EECS 106
EESK 111
EEDI 109
EEDO 108

R1685 5.6K
R308 X10K
U15
CS VCC 1 8
SK NC 2 7
DI NC 3 6
DO GND 4 5
AT93C46-3GR/SIC8
M33-93C4603-A26

3VDUAL
C343 X_104P
R618 X_0

CTRL18/NC 125
CTRL25 8
XTAL1 121
C328 22P
Y1
XTAL2 122
25MHZ-18pf/30ppm
C327 22P

SMBDATA 74
SMBCLK 72

M66EN/NC 88
CLKRUNB 65
ISOLATEB 23
R237 1K
VCC
R1680 15K

GND/NC 22
GND/NC 48
GND/NC 62
GND/NC 73
GND/NC 112
GND/NC 118

GND 35
GND 52
GND 80
GND 100

VSS 4
VSS 17
VSS 123
VSS 124
VSS 128

VSS/NC 9
VSS/NC 13

VSSPST 21
VSSPST 38
VSSPST 51
VSSPST 66
VSSPST 81
VSSPST 91
VSSPST 101
VSSPST 119

3VDUAL
R211 G_330
R168 330
VAUX_25
C275 4.7u/0805
C774 X_104P

USB2B
YMD20 #B
AMBER+ 19
AMBER- 20
POWER 13
TD1+ 18
TD1- 12
TD2+ 17
TD2- 11
TD3+ 16
TD3- 10
TD4+ 15
TD4- 9
GND 14
GREEN+ 21
GREEN- 22

LED_TRAFFIC
MX0+
MX0-
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
LINK1G#
LINK10/100#

C236 0/0805
C775 X_104P
N58-22F0031-S42

Near LAN Controllor

3VDUAL VR4
YLT1087S-0.8A
VIN 3
VOUT 2
VOUT 4
ADJ 1
EC25 47U/16V/S
EC27 47U/16V/S
C341 104P
R1691 200-1%
C349 1u
R1692 200-1%
VAUX_25
RTL8110S 2.5V
RTL8100C X

Near LAN Controllor

3VDUAL VR5
YLT1087S-0.8A
VIN 3
VOUT 2
VOUT 4
ADJ 1
EC26 47U/16V/S
R303 432-1%
C345 1u
R1681 200-1%
VAUX_18
RTL8110S 1.8V
RTL8100C 2.5V

Micro Star Restricted Secret

Title	RTL8110S/8100C	Rev 0E
Document Number	MS-6702	
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LINEAR MODE

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

THESE OUTPUT AND INPUT PIN MUST BE PULL HIGH

CPU_GD 5 — CPU PWR_GD OUTPUT
ALL_PWRGD 19,38 — CHIP PWR_GD OUTPUT
SMBCLK1 7,8,9,18 — I2C BUS
SMBDATA1 7,8,9,18 — I2C BUS
RSMRST# 19 — CONNECT TO SOUTH BRIDGE RSMRST# SIGNAL
SUSC# 18 — SOUTH BRIDGE POWER CONTROL(SLP_S4# OR SUSB#) SIGNAL
SUSB# 18 — SOUTH BRIDGE POWER CONTROL(SLP_S3# OR SUSC#) SIGNAL
PW_OK 38 — ATX POWER OK INPUT

FRONT PANEL RESET BUTTON
PCIRST# INPUT

PCIRST# BUFFER OUTPUT

PCI SOLT PCIRST# BUFFER OUTPUT

CLOSE TO CHIP

CHARGE PUMP VOLTAGE OUTPUT

CONNECT TO CPU

WATCHING DOG TIMER SELECT

WD_DET	TIMER
PULL LOW	OFF
PULL HIGH	ON

THE TWO MODE ONLY ONE MODE PRESENT

SINGLE MODE — THIS MODE SELECT BY PIN 47 PULL HIGH 5VSB

DUAL MODE — THIS MODE SELECT BY PIN 47 PULL LOW
3VSB REGULATE BY 5VSB AND VCC3

CONNECT TO SOUTH BRIDGE SUSB# SIGNAL

THE TWO BLOCK CHOICE ONE SUPPORT SYSTEM POWER CONTROL

DDR AND DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

THE VDIMM_HSEN IN LINEAR MODE

DDRTYPE	VDIMM_HSEN VREF
DDR	2.0V
DDR II	1.7V

DDR TERMINATION

THIS POINT VOLT CAN'T SETTING BELOW 2.9V

Micro Star Restricted Secret

Title	ACPI POWER CONTOLLER (MS-6)	Rev 0E
Document Number	MS-6702	
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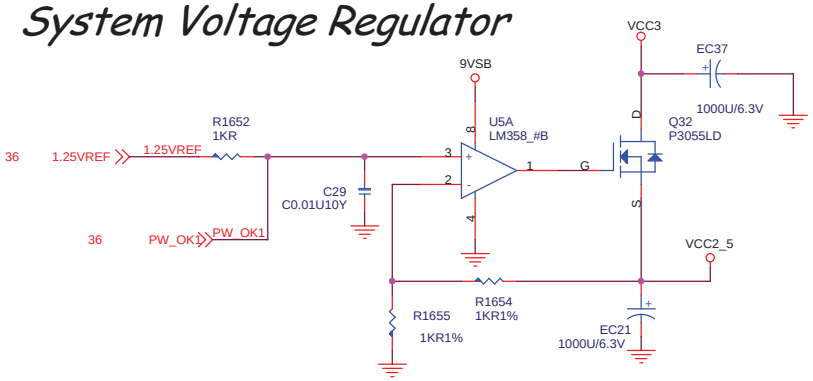
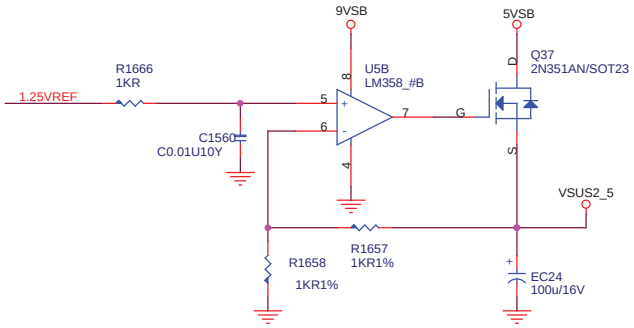
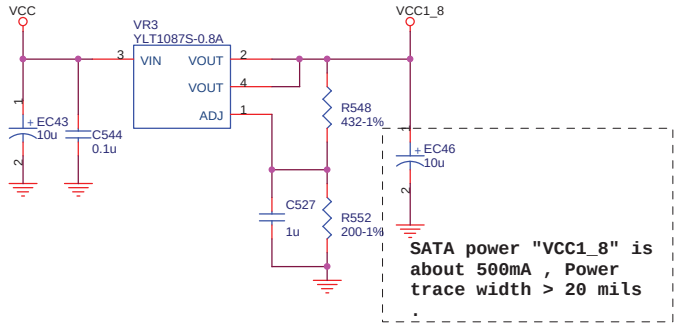
System Voltage Regulator





for SATA & Power Reference .

Power for SATA



SATA power "VCC1_8" is about 500mA , Power trace width > 20 mils .

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Title	System Voltage Regulators	Rev 0E
Document Number	MS-6702	
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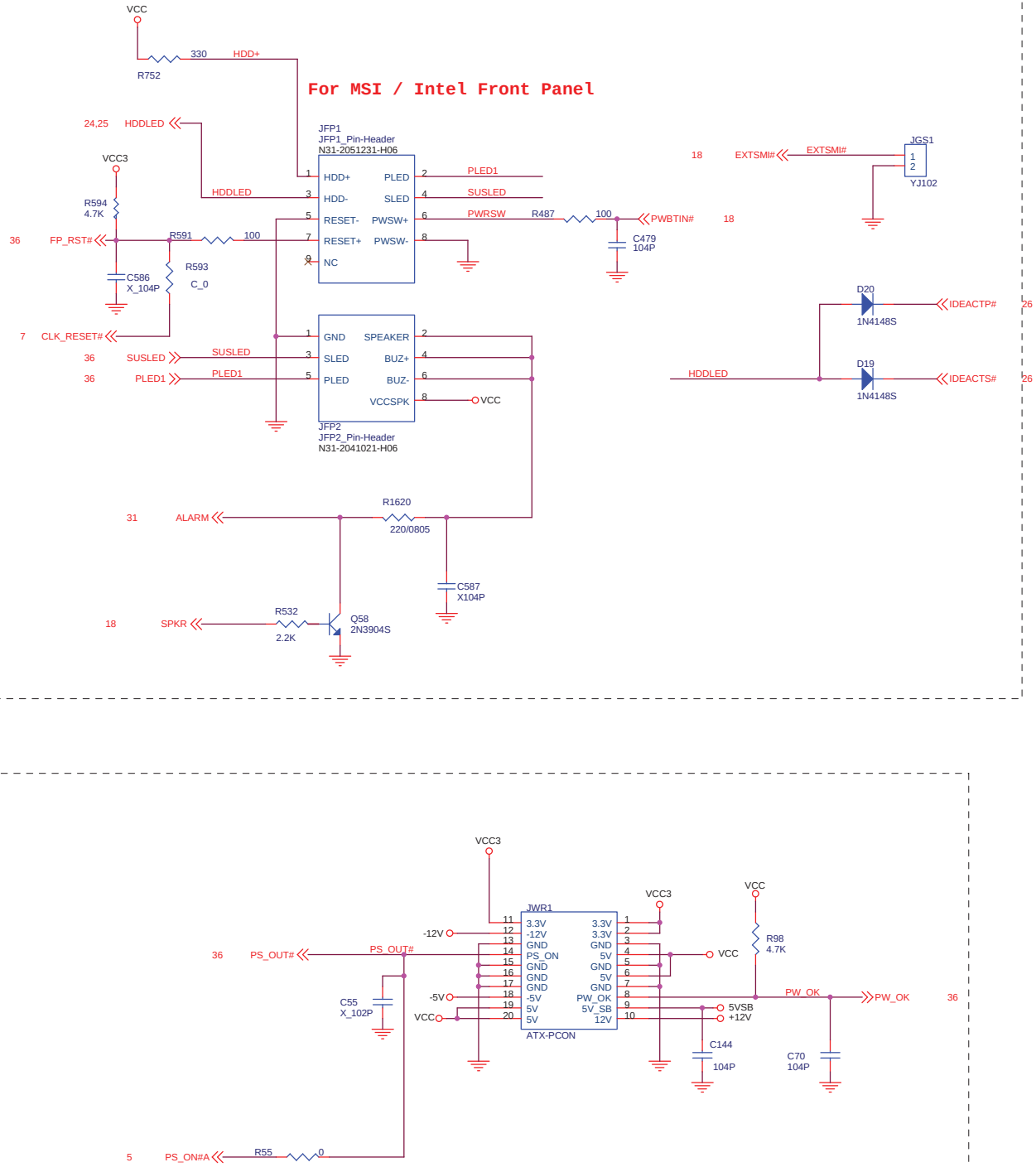
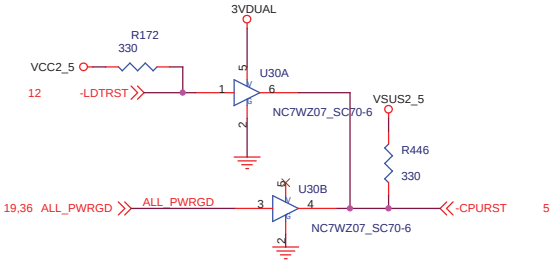
FRONT PANEL



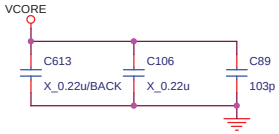
POWER OK Circuits

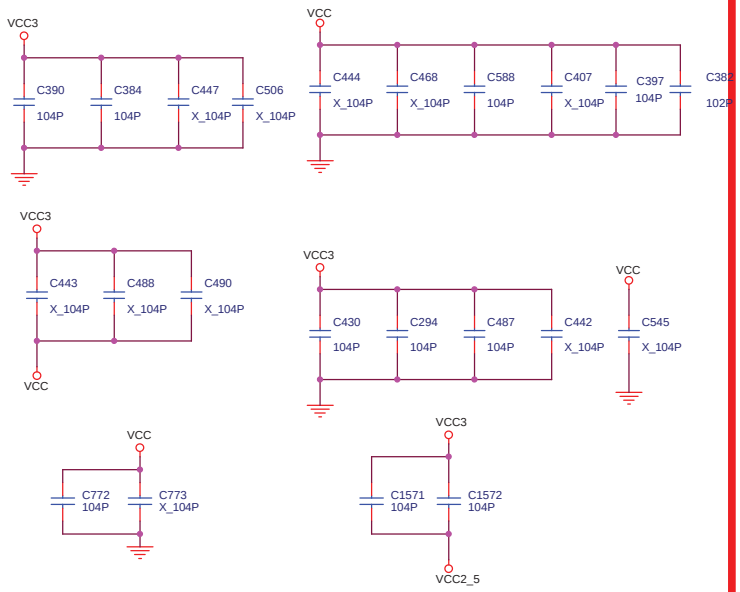


Micro Star Restricted Secret		
Title	*Front Panel &Power OK Circuits*	Rev 0E
Document Number	*MS-6702*	
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, June 25, 2003 Sheet 38 of 42

BULK / Decopuling

Place on CPU Solder side

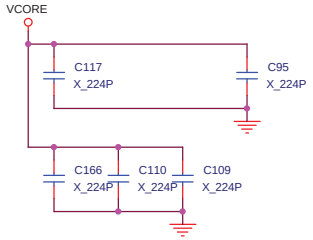




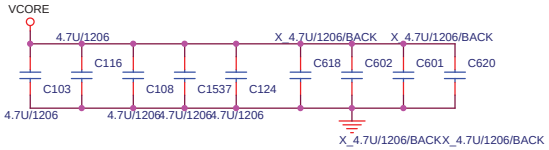
For EMI

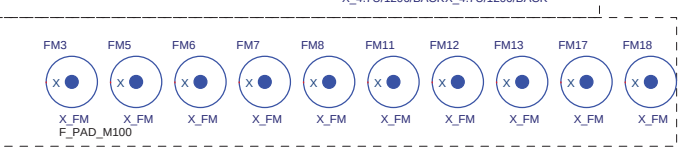
CPU

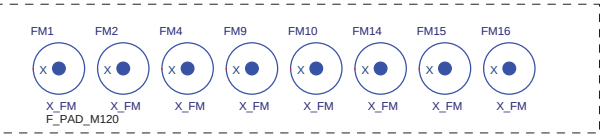
Place on inside of CPU Cavity (10 * 0.22uF/0603 X7R high-freq decoupling Cap.)



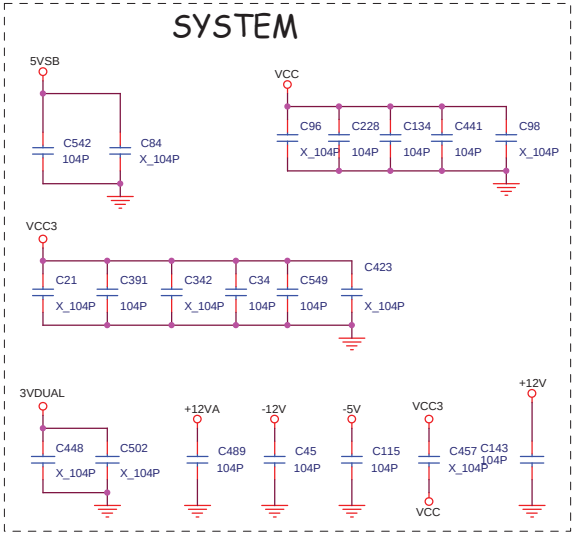
Buck-decoupling Mid-Freq. decoupling Cap. (7 * 4.7uF / 1206 X7R)

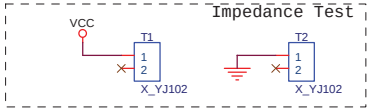




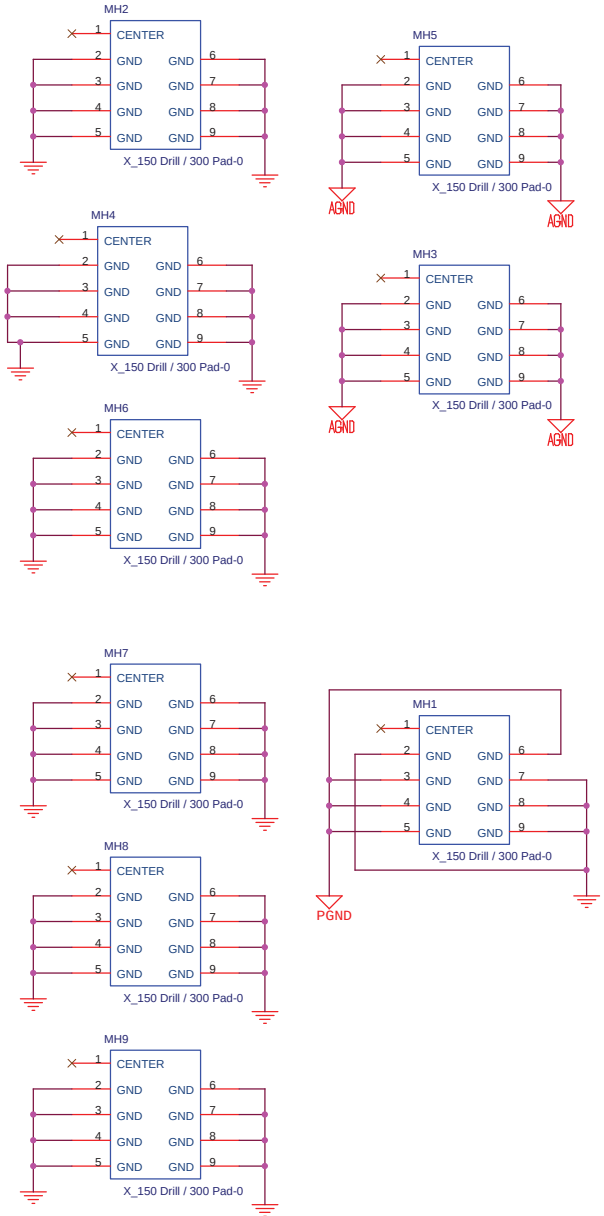


SYSTEM





ATX VIA-Hole * 9



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Title: BULK / Decopuling		Rev: 0E
Document Number: MS-6702		
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, June 25, 2003 Sheet 39 of 42	

K8 CPU Power

CPU Side

- K8 Vcore -> "VCORE" (42A)
- VDDA_2.5 Power -> "VDDA_25" (0.11A)
- HT Power -> "VDD_12_A"&"VLDT0" (2A)

DDR Side

- DDR Power -> "VDD_25_SUS" (9.5A)
- DDR-VTTPower -> "VTT_DDR_SUS" (5.21A)

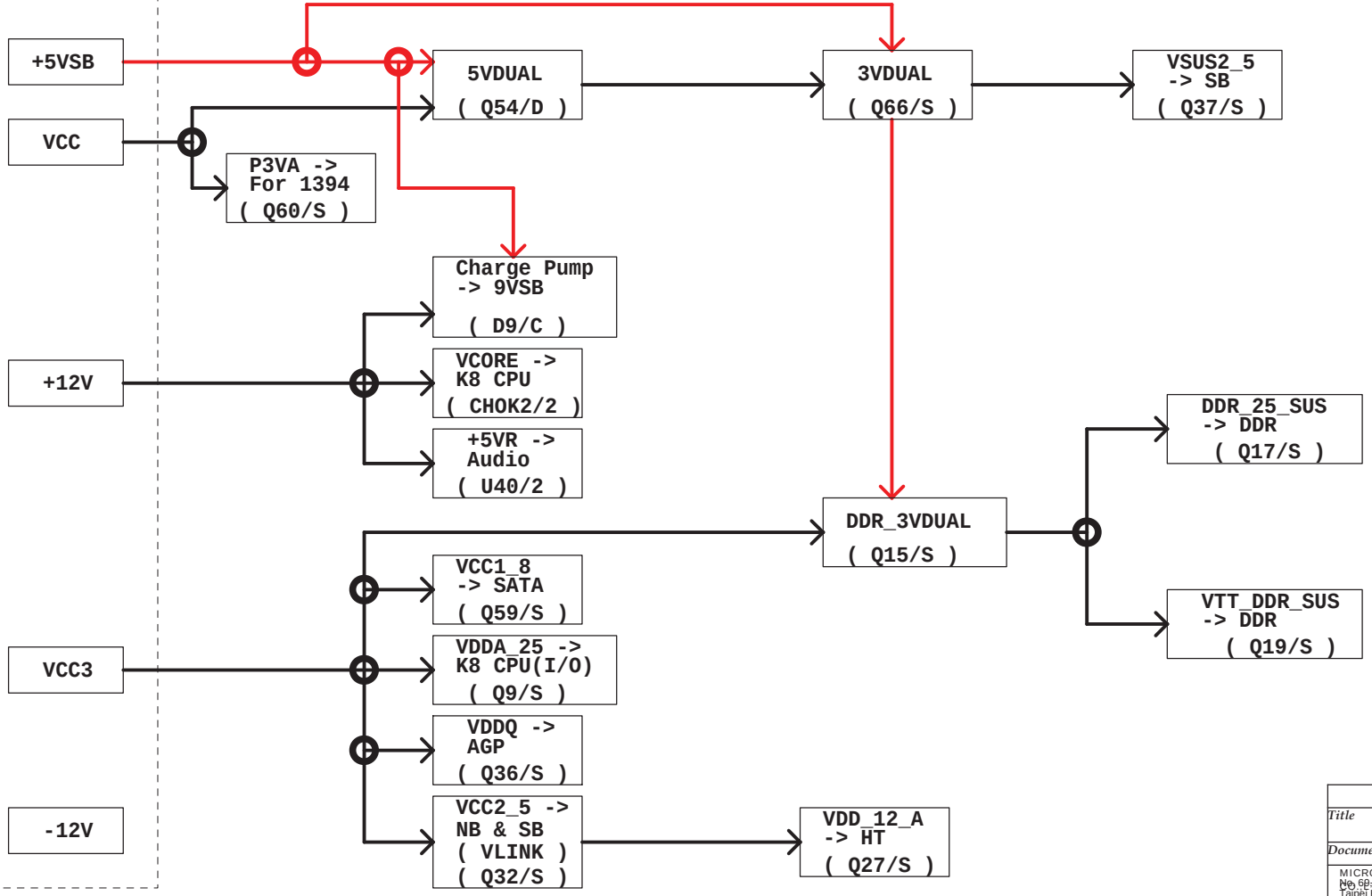
NB & SB & AGP Power

- NB & SB Core-Power -> "VCC2_5" (?A)
- NB & SB Core-Suspend Power -> "VSUS2_5" (?A)
- NB AGP8X Power -> "VDDQ" (1.5A)

Other Power

- 5VDU
- DDR_3VDUAL
- 3VDU
- 9VSB

ATX Power Supply



Micro Star Restricted Secret

Title	Power Generation	Rev 0E
Document Number	MS-6702	
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MS-6702 VER:0C

1.P-4 ADD MSC4,MSC5 TO DDR DIMM3 FOR SUPORTING 5,6 BANK
2.P-5 HDT TEST PORT PULL UP RESISTORS CHANGE TO 8P4R FROM SINGLE RESISTORS
3.P-7 U26(MS-1) REMOVE AND REARRANGE THE DEVICES CLOCK
4.P-9 U8 CLOCK BUFFER DAMPPING RESISTOR REMOVE AND DIRECT SHORT
5.P-15 MODIFY THE MOSFET'S SIZE FROM D2PACK TO DPACK AND ADD THE PWM'S FREQENCY ADJUSTING CIRCUIT.
6.P17-19 SOUTBRIDGE CO-LAYOUT VT8235CE AND VT8237CD(ADD SATAX2,USBX2)
7.P22 REMOVE PCI6
8.P-28 MODIFY 1394 CONNECTORS PORT0 FROM REAR TO FRONT SIDE AND USE SAME POWER
9.P-30 ADD ONE FRONT USB PORT (JUSB2) AND SHARE WITH USB1
10.P-31 USB1 CHANG FROM 2 PORTS TO 4 PORTS FOR VT8237CD
11.P-32 DLED PORT FORM SIO'S GAME PORT
12.P-33 REMOVE PSFAN1
13 P-34 REMOVE COM PORT WAKE-UP FUNCTION.
14. P-36ADD COM2
15.P-38 REMOVE CPU RATING SETTING AND ADD AGP AND DIMM VOLTAGE ADJUSTING CIRCUIT.
16. P-40,41 MODIFY ACPI POWEROK CIRCUIT.
17.CANCEL P-45 PCI AND MS-1 ROUTING DIAGRAM.

MS-6702 VER:0D 3/24/03
1.P-5 A.RESERVER R1164 CROSS Q41 C.E FOR THRM#,WHEN REMOVE Q41,R316.
B.CANCEL THE TRACE "VDDIO_SENSE" TO ACPI POWER AND ADD C1502.
2.P-15 A.FUZZY PWM ,3 STEPS CHANGE TO 2 STEPS,LM324 MODIFY TO LM393.
B.VCORE_EN# DIRECTLY CONTROL FROM MS-6
3.P-17 A.REMOVE RESET BUFFER AND CHANGE TO MS-6.
B.RN1521,RN1515,RN1516 PULL-UP CHANGE TO VCC3 FROM VCC BECAUSE LAYOUT ISSUE.
4.P-18 GPO0 CHANGE FROM SUSLED TO VCORE_ADJ.
5.P-19 REMOVE AGPVS1,AGPVS2,POWERF3.
6.P-24 ADD R1661 TO X'TAL XTLO
7.P-30 XA18 ADD A R1662,AND U23.126 TRACE NAME ERROR,MODIFY TO DLED#3
8.P-31 REMOVE RT1 COME FROM CPU THERMAL DIODE.
9.P-32 ADD A VCORE ADJUST CIRCUIT.
10.P36,P37 ACPI POWER MODIFY TO MS-6
11.P38 REMOVE THERMAL PROTECTION CIRCUIT.

PCB1

1670200E
P01-670200E-L20

VBAT1

YSKTBT
D06-0100101-P01

U10-F

MSI
DDR

NB-HEATSINK-W/Fan
_

U10-H

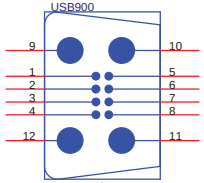
MSI
DDR

NB-HEATSINK-W/O Fan
E31-0400482-A58

U28_1

FLASH/4M/W49F002UP12B
M31-29040P8-W03

USB900



X_USB*2/WO-LAN
N53-08M0031-F02

USB900

F_USB+Tr/10-100M
N58-22F0061-S42

Title: OPTION PART		
Size: Custom	Document Number: MS-6702	Rev: 0E
Date: Wednesday, June 25, 2003	Sheet 42 of 42	