

MS-6580

Version 20

INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

**Willamette/Northwood mPGA-478B
Processor**

**System Brookdale-G
Chipset:**

**INTEL GMCH (North Bridge)
+ INTEL ICH4 (South
Bridge)**

On Board Chipset:

**BIOS --
FWH**

**AC'97 Codec --
ALC201A**

**LPC Super I/O --
W83627HF-AW**

**Clock Generation --
ICS950218AF**

**LAN -- INTEL
82562ET LAN**

**Expansion Slots:
PCI2.2 SLOT * 6**

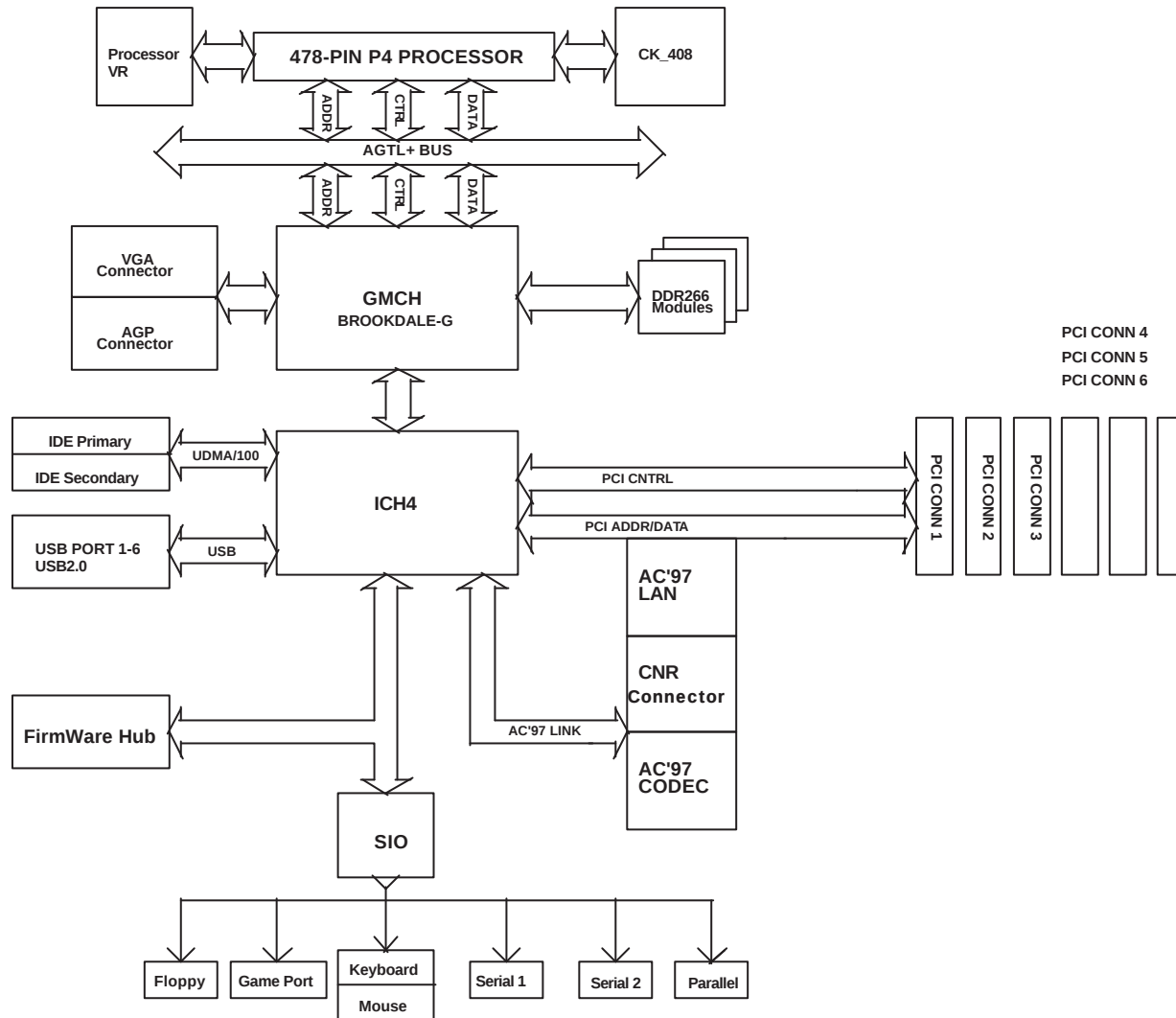
Title

Page

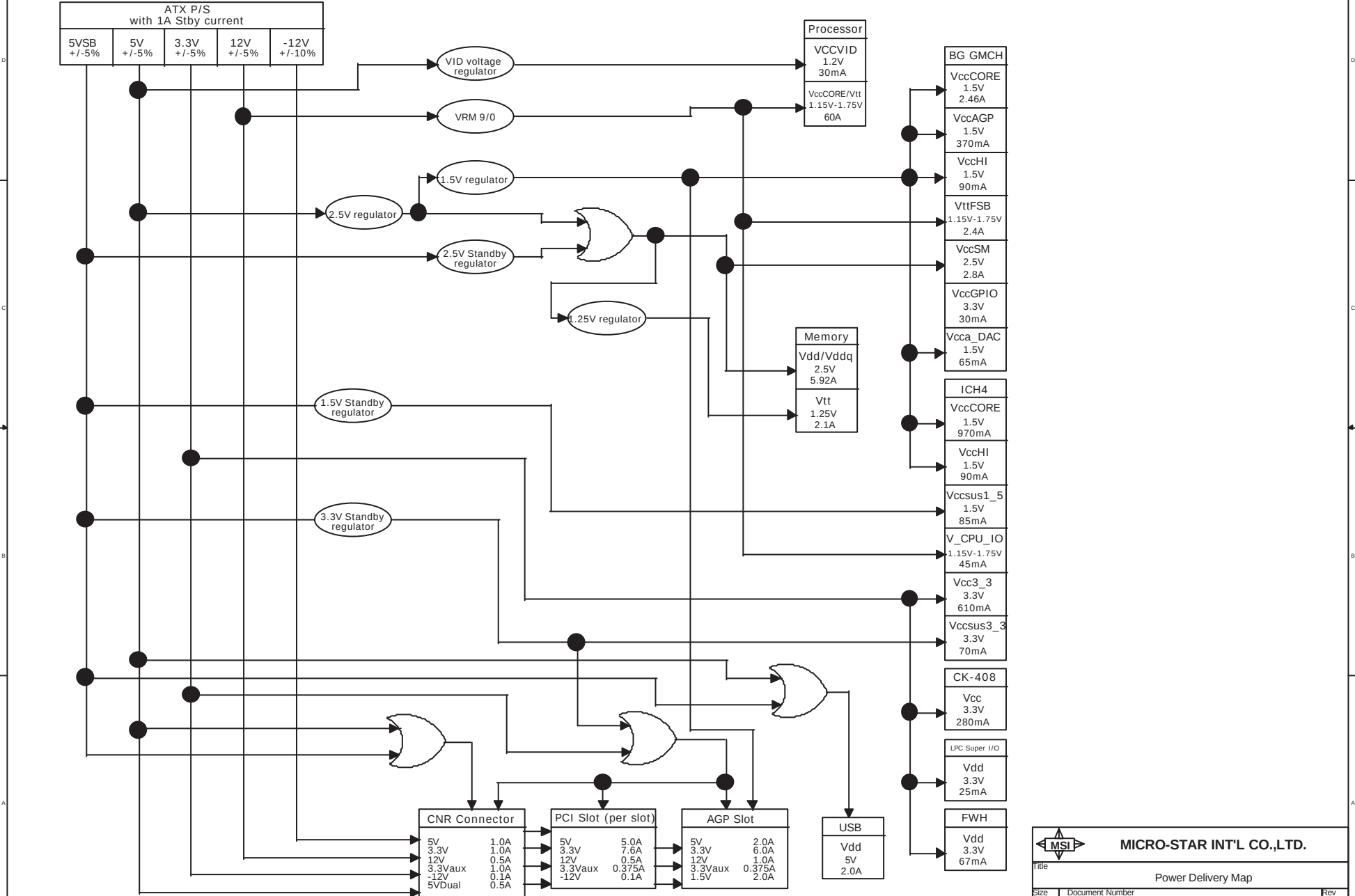
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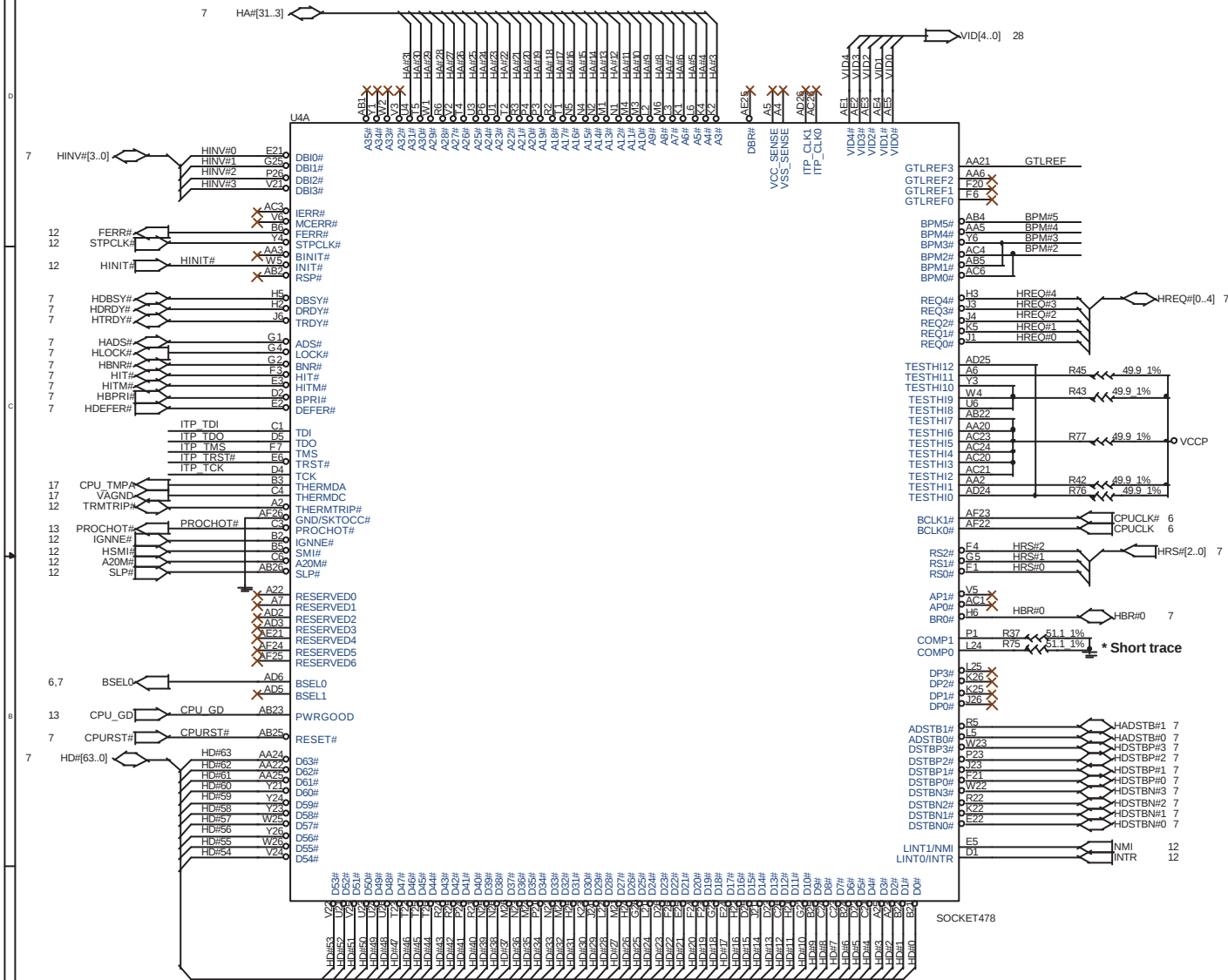
BLOCK DIAGRAM



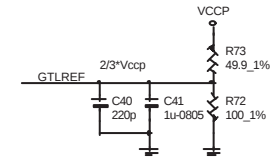
Power Delivery Map



CPU SIGNAL BLOCK

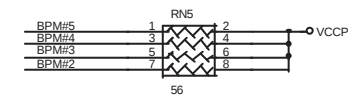


CPU GTL REFERENCE VOLTAGE BLOCK

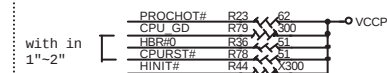


Every pin put one 220pF cap near it.
Trace Width 7mils, Space 10mils.
Keep the voltage divider within 1.5" of the GTLREF pin.

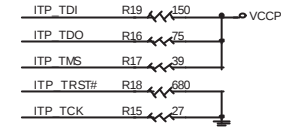
CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU



with in 1"-2"



MICRO-STAR INT'L CO.,LTD.			
Title mPGA478-B INTEL CPU SOCKET Part1			
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[illegible]

CPU DECOUPLING CAPACITORS

Place 14 pcs 1206 size cap
north side of processor

PLACE CAPS WITHIN CPU CAVITY

Place these caps on south
side of processor

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Title

mPGA478-B INTEL CPU Part2

Size

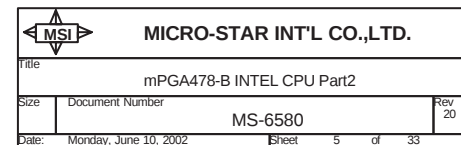
Document Number

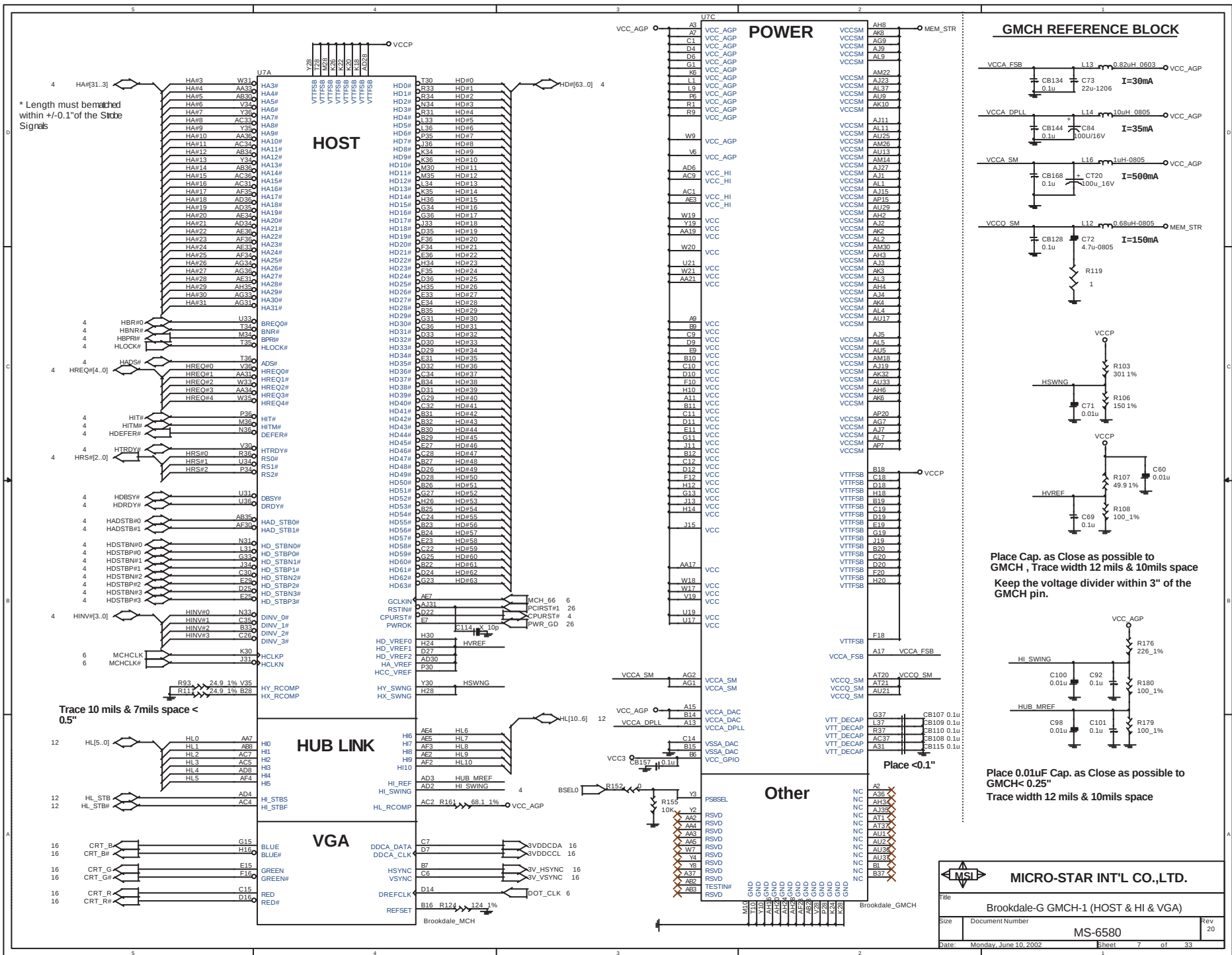
MS-6580

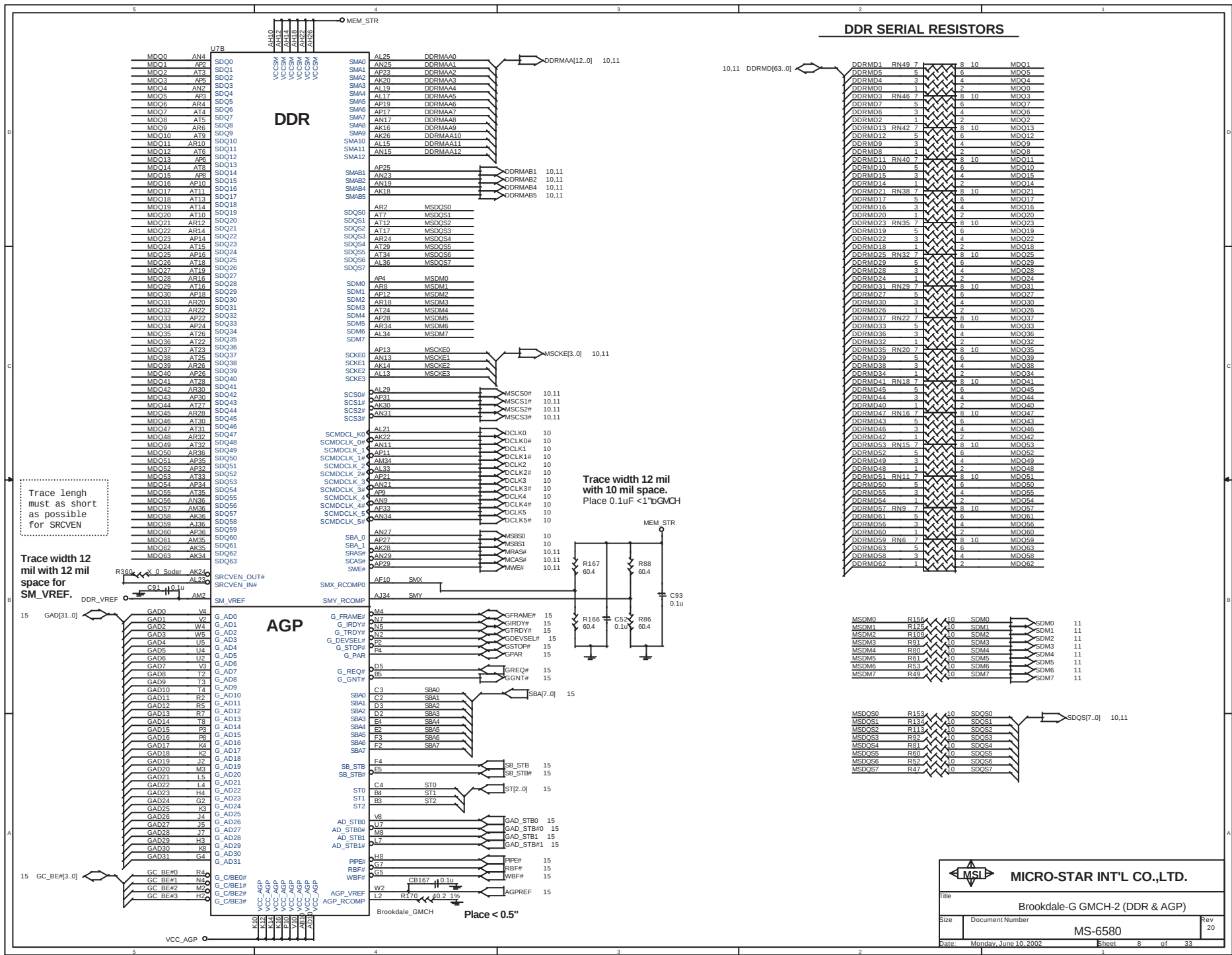
Rev 20

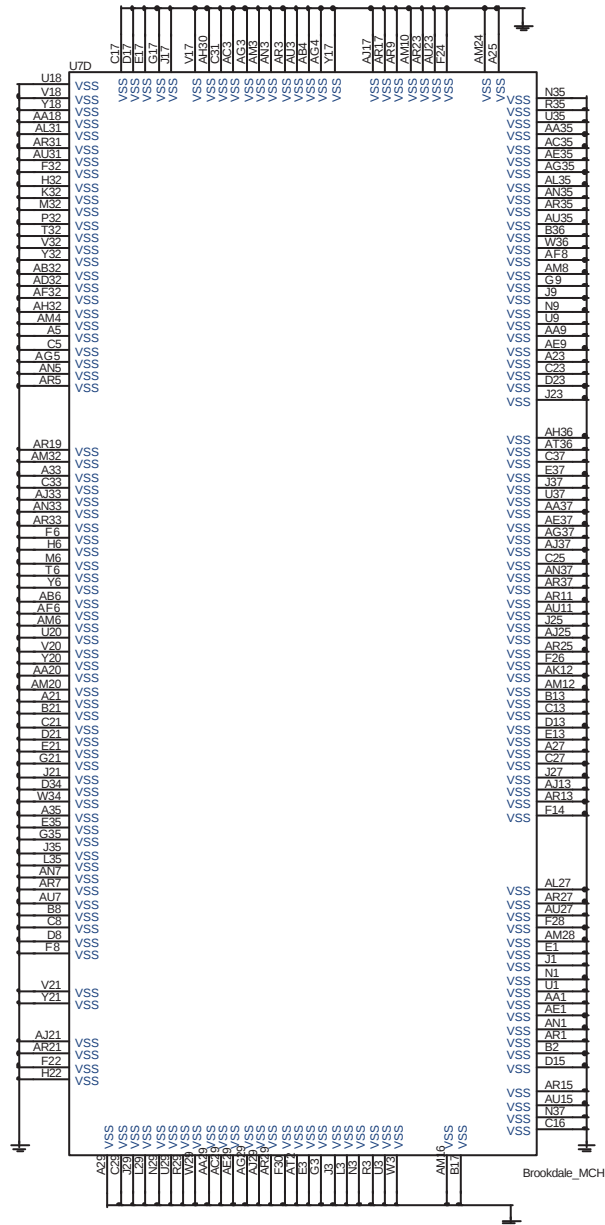
Date: Monday, June 10, 2002

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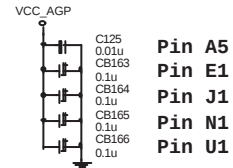








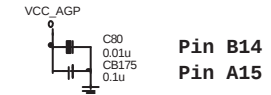
GMCH DECOUPLING CAPACITOR



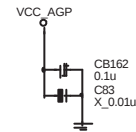
Place decoupling cap
close to GMCH AGP
Interface < 0.1"



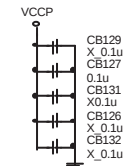
Place decoupling cap
close to GMCH
Hub-Link Interface<
0.1"



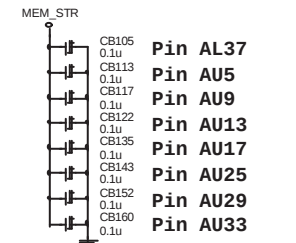
Place decoupling cap
close to GMCH DAC
Interface< 0.1"



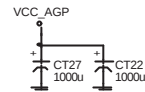
Place decoupling cap
close to GMCH Core
Logic Interface <
0.1"



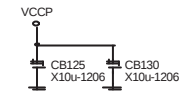
Place decoupling cap
close to GMCH CPU
Interface < 250mil
in the Vtt corridor



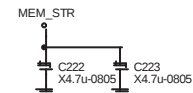
Place decoupling cap
close to GMCH Memory
Interface < 0.1", with
18 mil trach width



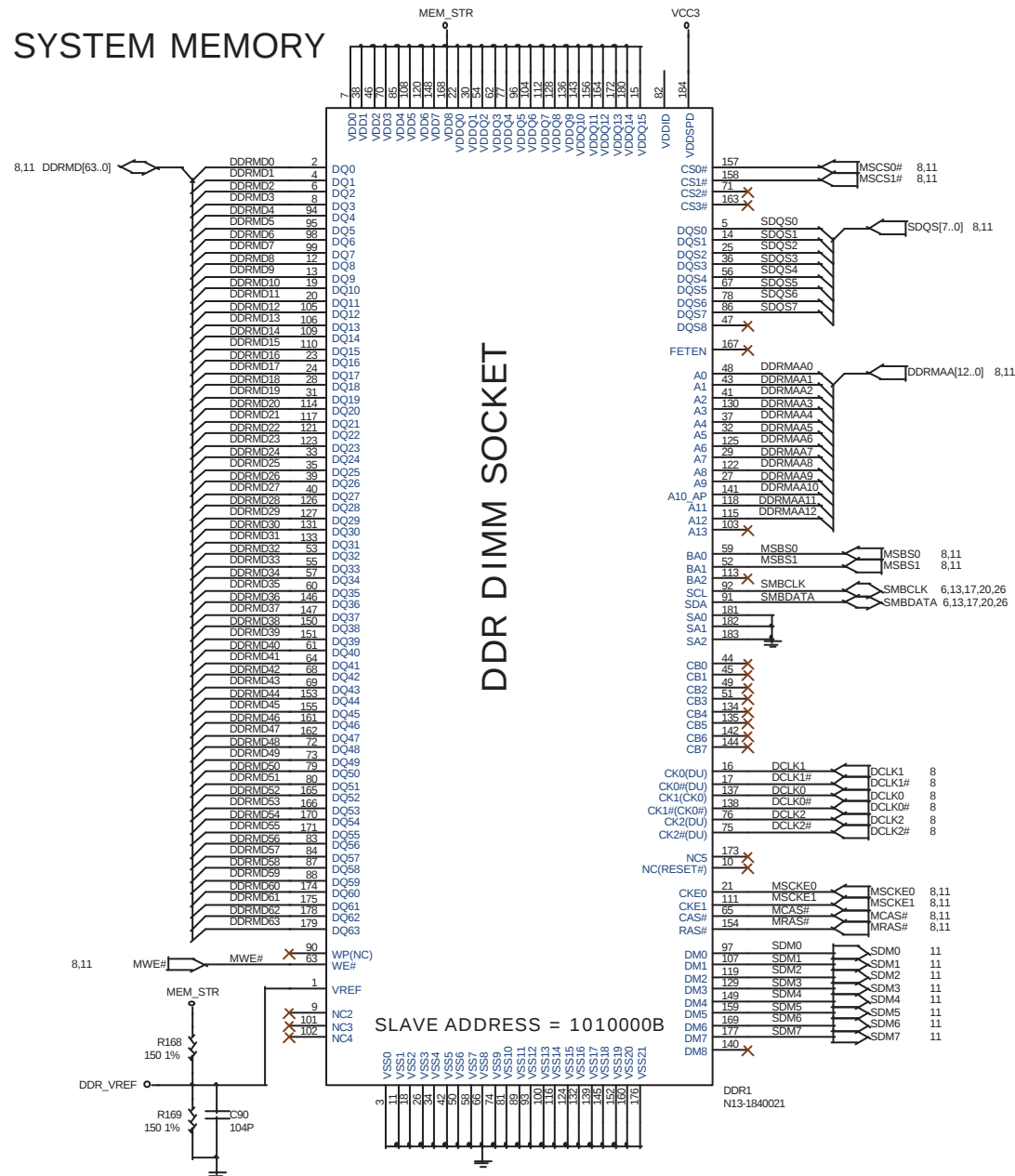
Place Bulk cap for Core Logic,
AGP & Hub Link Interface



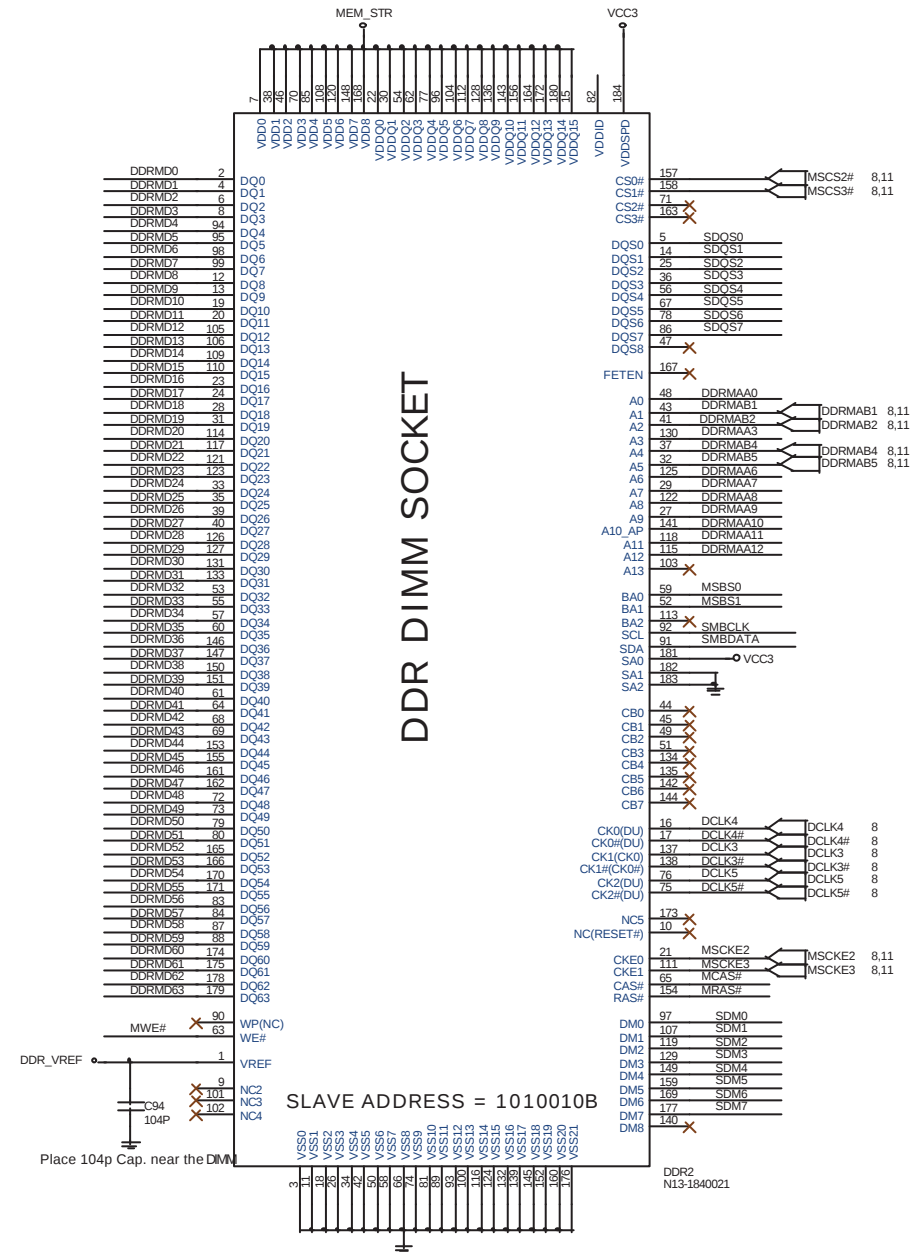
Place Bulk cap between
GMCH & DIMM slot



SYSTEM MEMORY

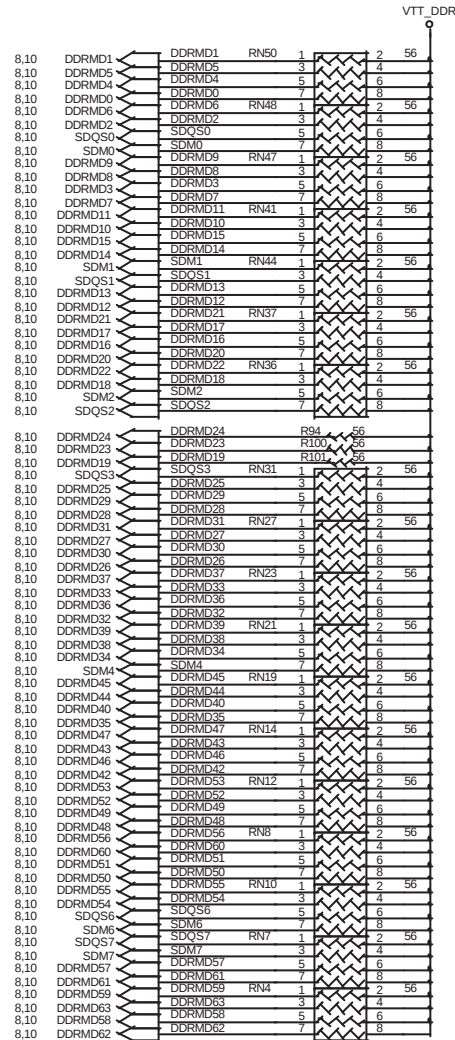
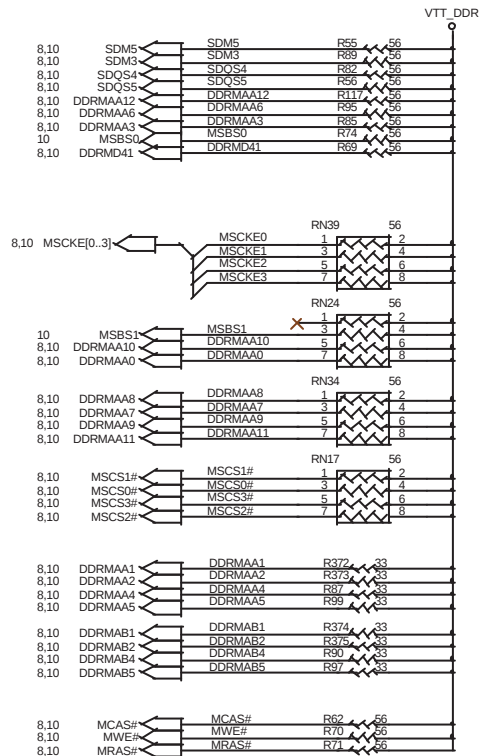


Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
 Place 104p Cap. near the DIMM

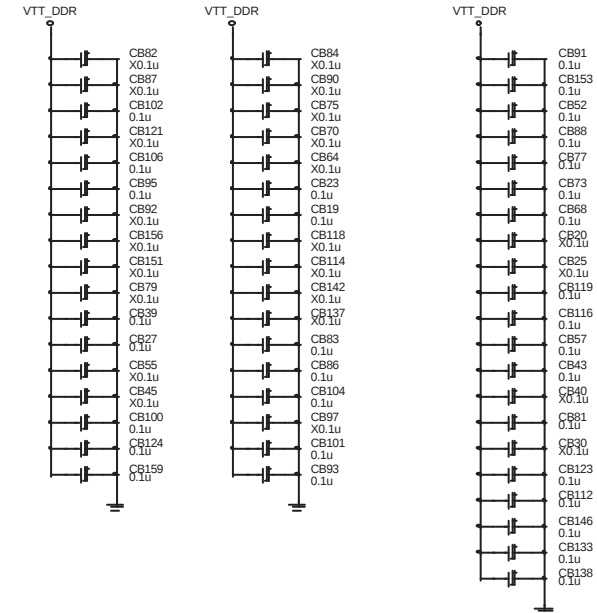


		MICRO-STAR INT'L CO.,LTD.	
Title DDR DIMM1&2			
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DDR TERMINATORS

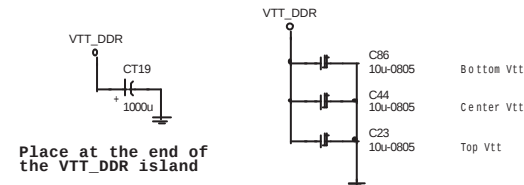


DDR Decoupling Caps

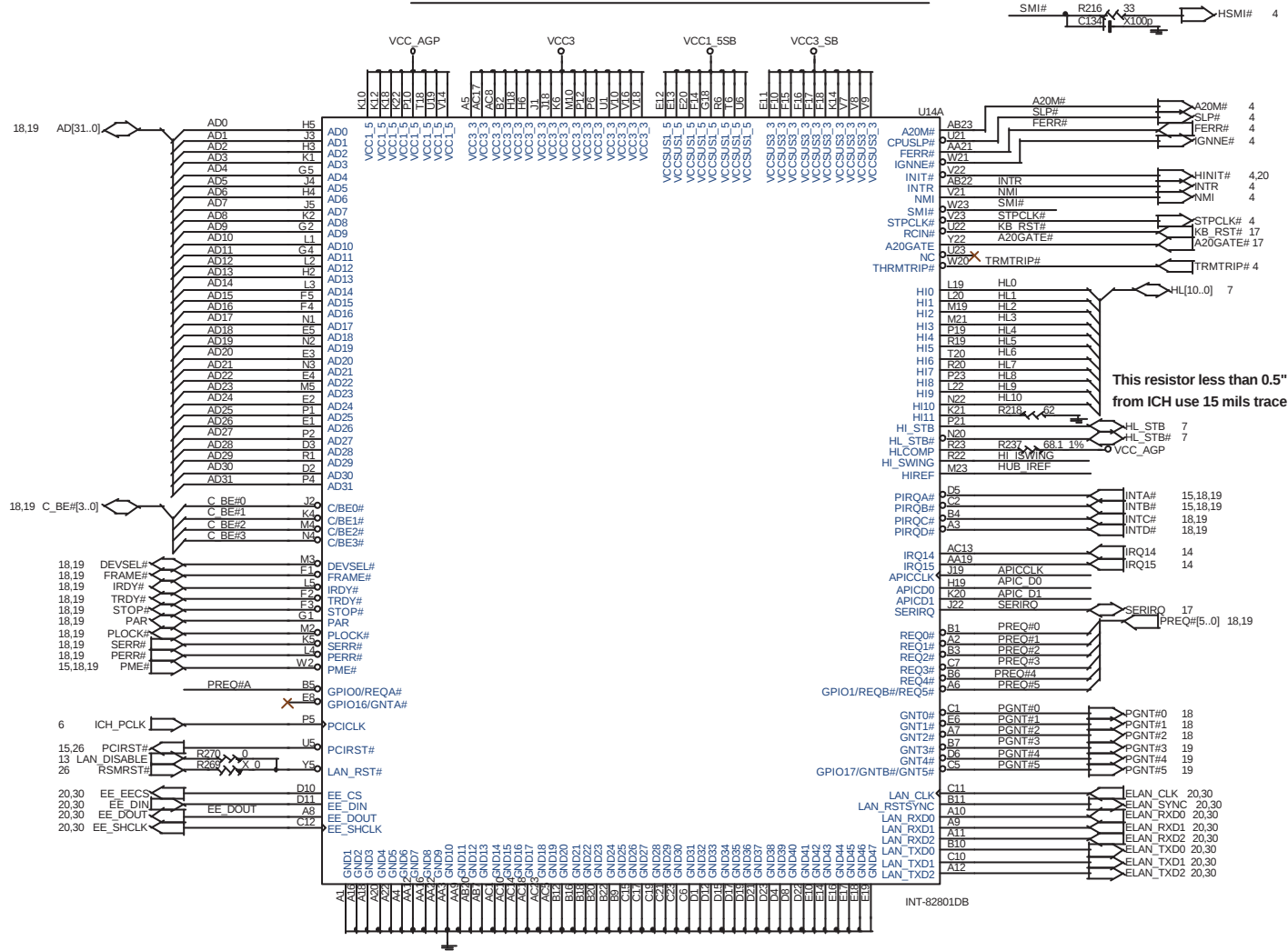


Total 110 signal, need 55 pcs decoupling.

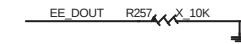
Place for VTT_DDR island



ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

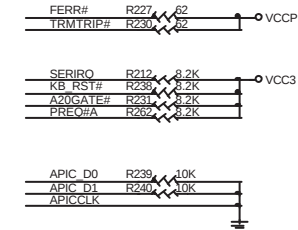


ICH4 STRAPPING RESISTORS

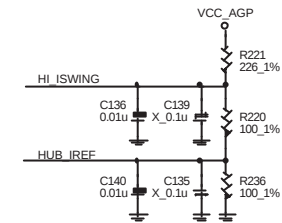


Reserved pull-down resistor for ICH4 reserved function straps.

ICH4 PULL-UP/DOWN RESISTORS

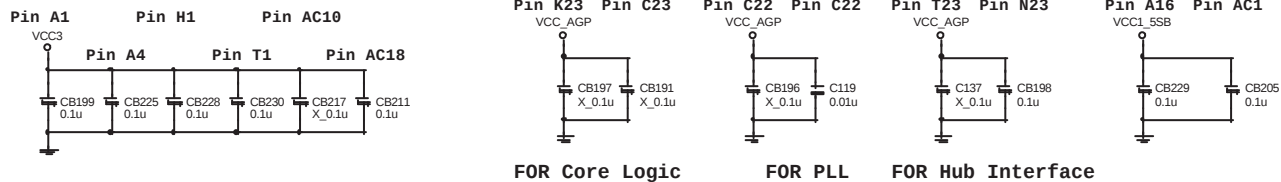


ICH4 REFERENCE VOLTAGE

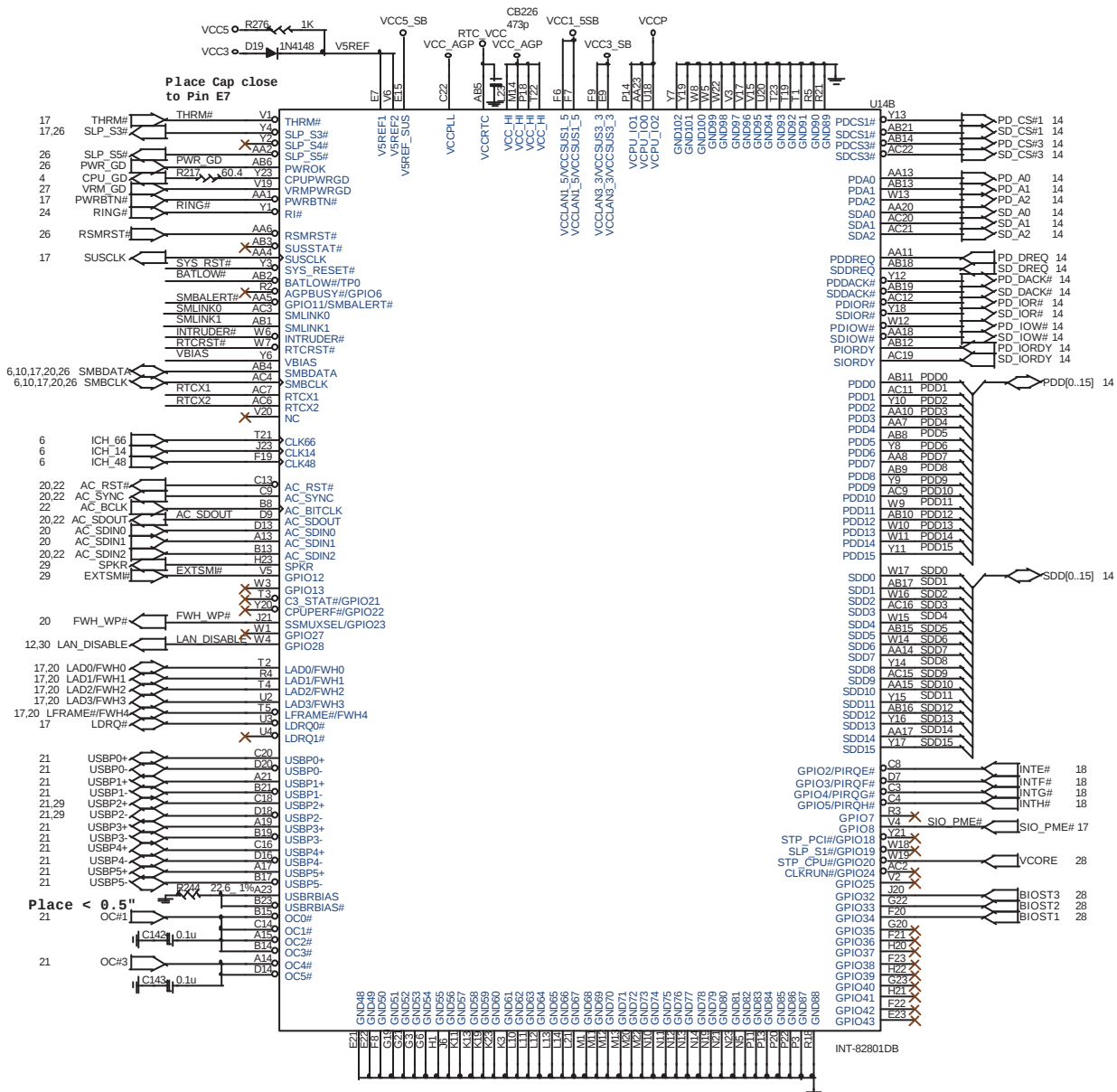


Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

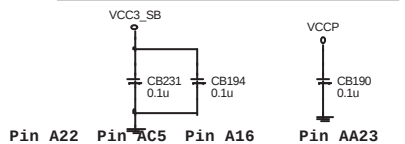
ICH4 DECOUPLING CAPACITORS Place one 0.1u close to ICH4 <100 mil



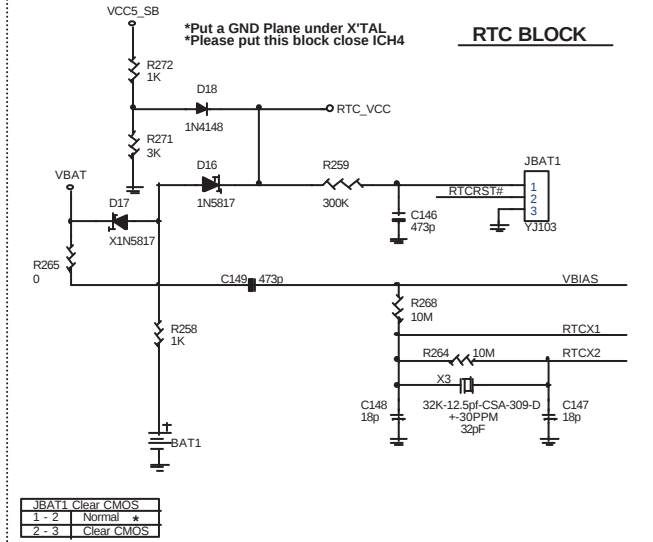
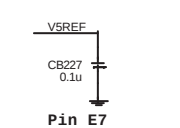
		MICRO-STAR INT'L CO.,LTD.	
Title: ICH4 PCI & Hi & LAN			
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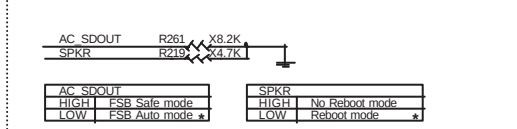
ICH4 DECOUPLING CAPACITOR



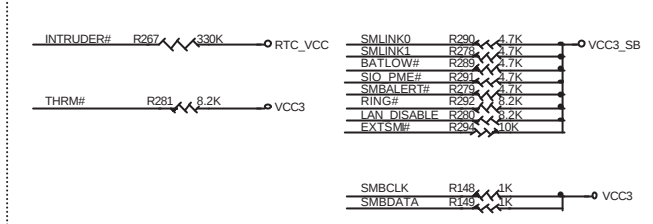
Place one 0.1u close to ICH4 <100 mil



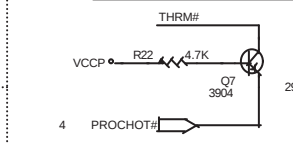
ICH4 STRAPPING RESISTORS



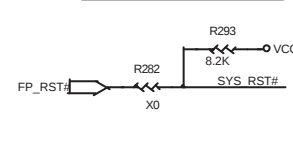
ICH4 PULL-UP/DOWN RESISTORS



PROCHOT BLOCK



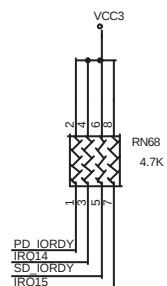
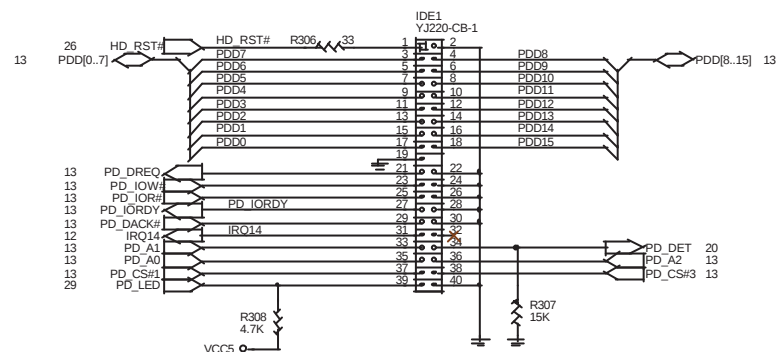
SYSTEM RESET



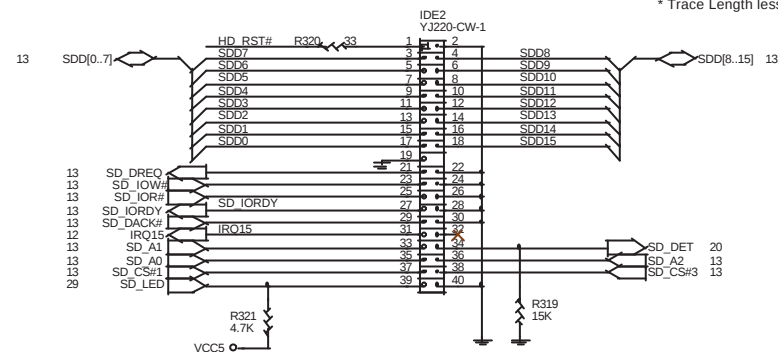
MICRO-STAR INT'L CO.,LTD.			
Title ICH4 ASIC/RTC/AC'97/GPIO/LPC/USB/IDE			
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ATA100 IDE CONNECTORS

PRIMARY IDE BLOCK



SECONDARY IDE BLOCK

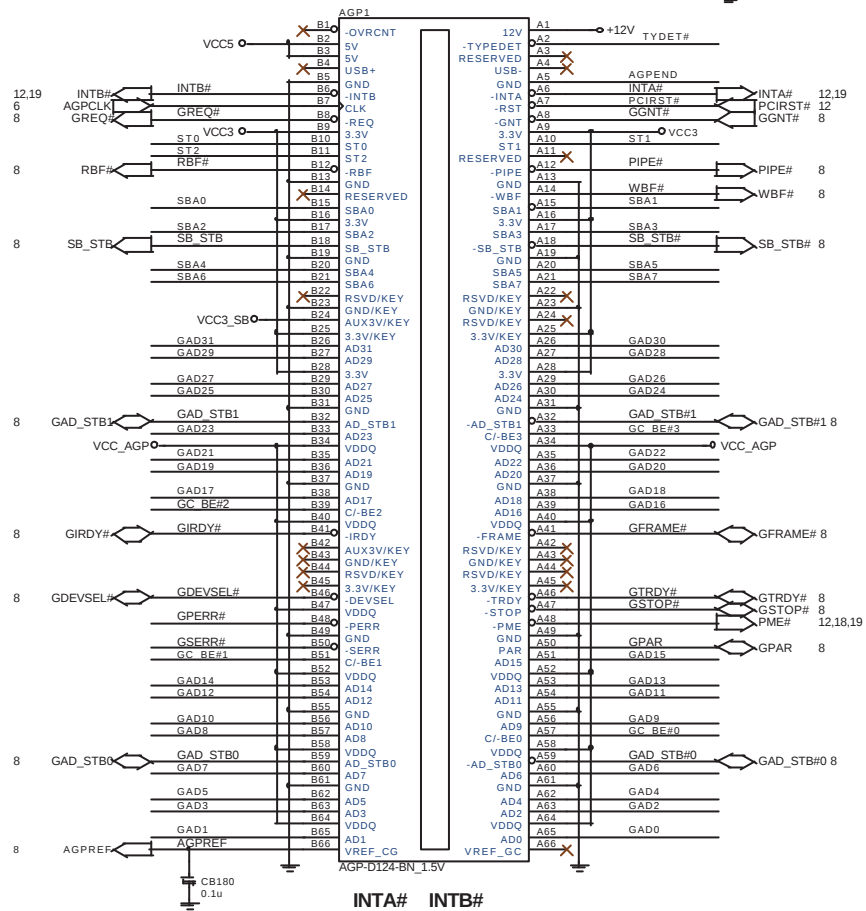


* Trace Width : 5mils
 * Trace Spacing : 7mils
 * Length(longest)-Length(shortest)<0.5"
 * Trace Length less than 5"

MICRO-STAR INT'L CO.,LTD.			
Title: ATA100 IDE Connectors 1&2			
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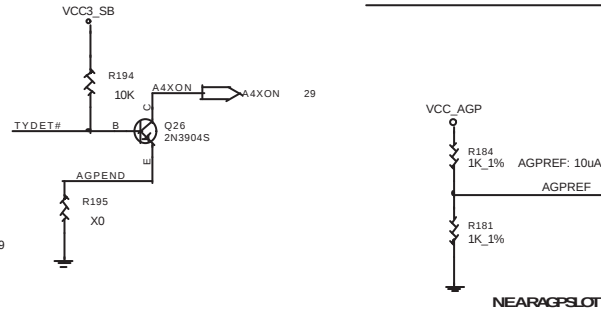
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

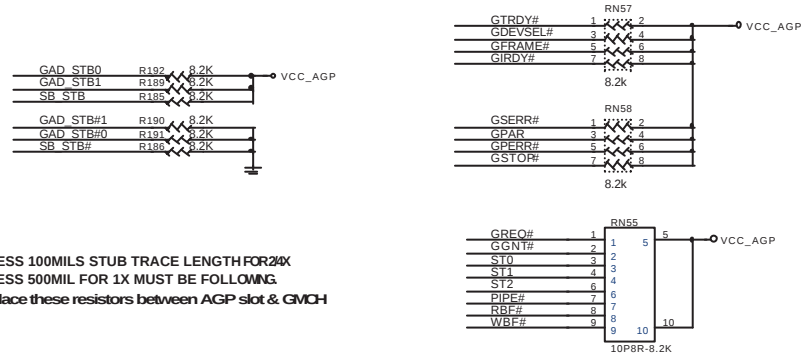


INTA# INTB#

AGP SIGNAL REFERENCE CIRCUIT

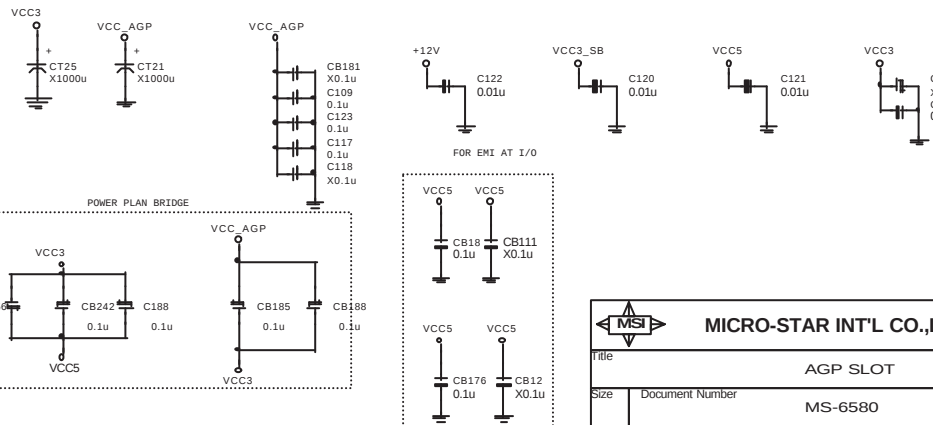


AGP TERMINATION RESISTORS



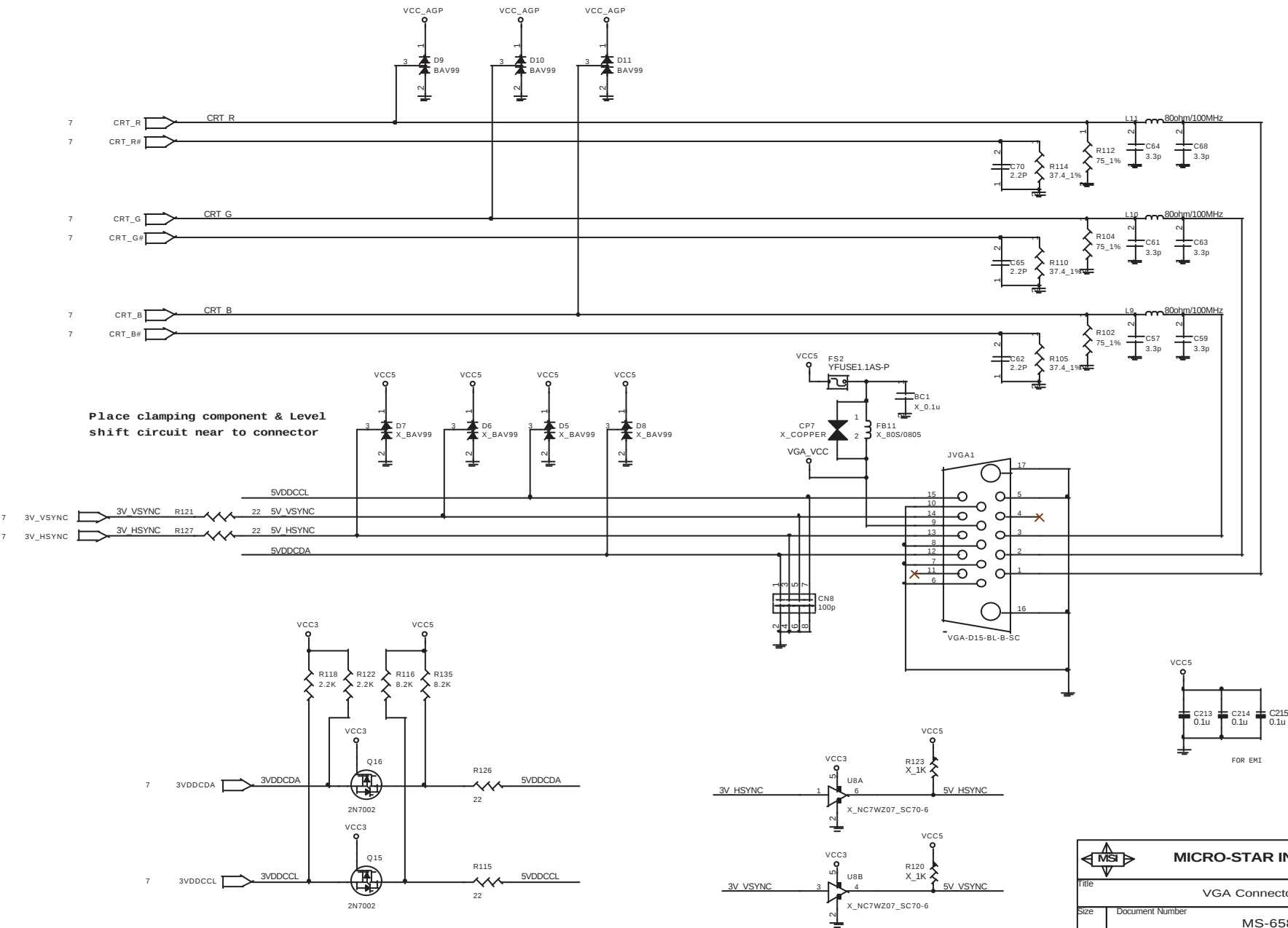
LESS 100MILS STUB TRACE LENGTH FOR 2X
LESS 500MIL FOR 1X MUST BE FOLLOWING
Place these resistors between AGP slot & GMCH

AGP SLOT DECOUPLING CAPACITORS



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File: AGP SLOT			
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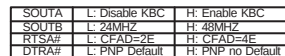
Video Connector



U13



B207 4 7K SOLITA



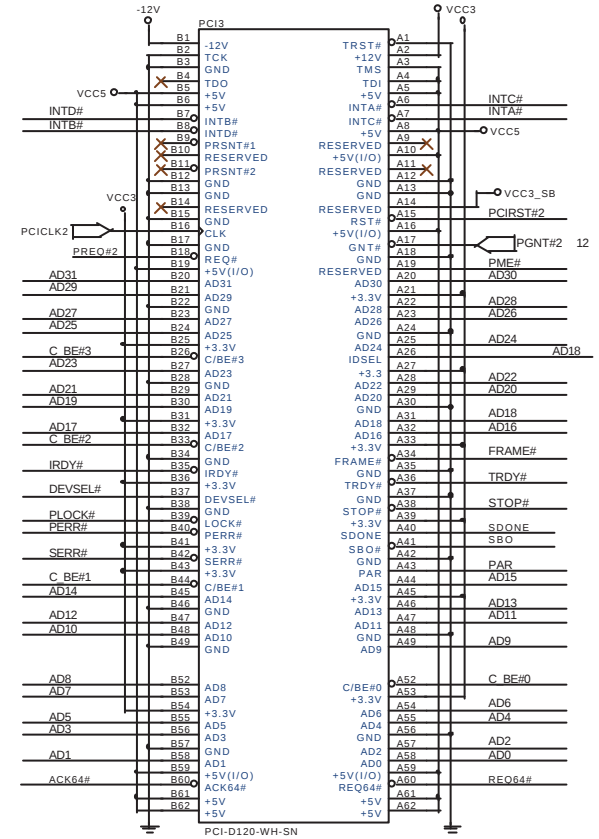
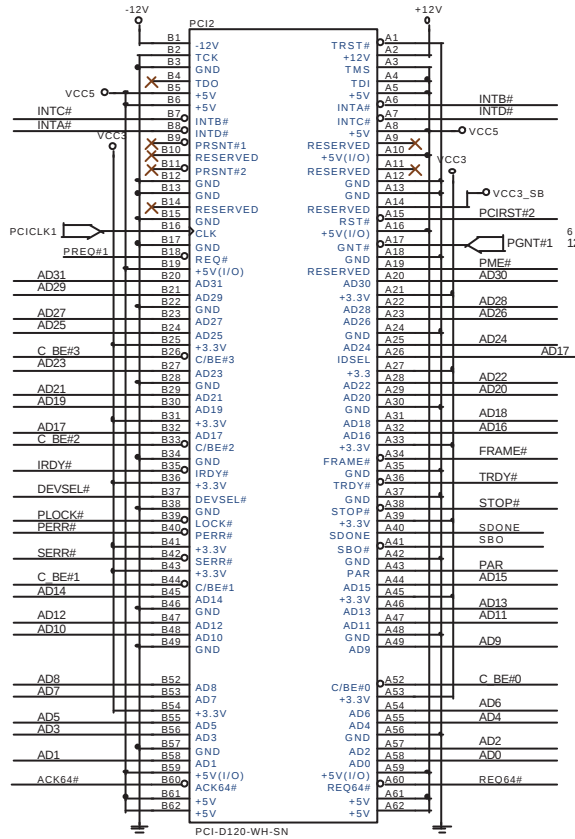
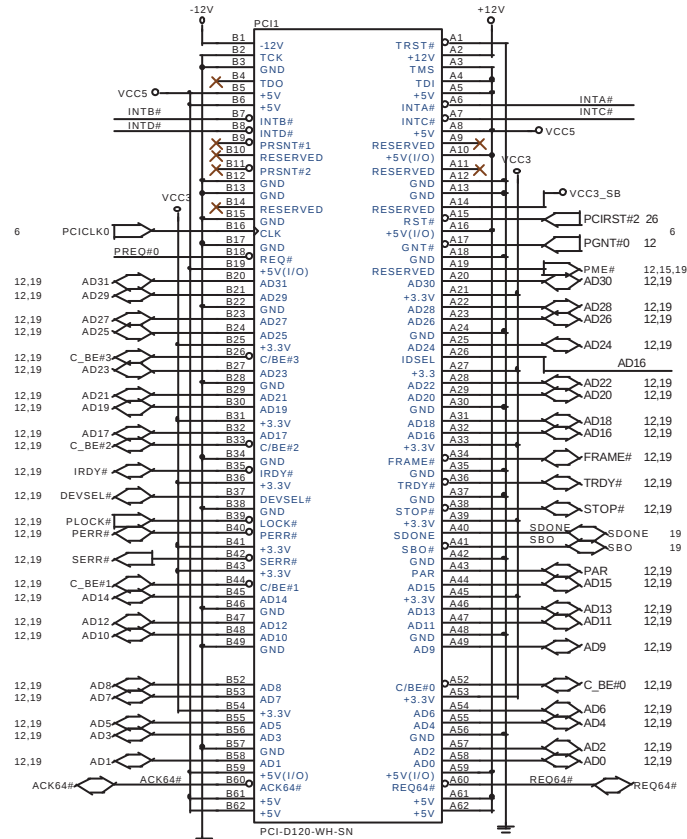
Number

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PCI SLOT 1 (PCI VER: 2.2 COMPLY)

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDESEL = AD16

MASTER = INTA#
PREQ0

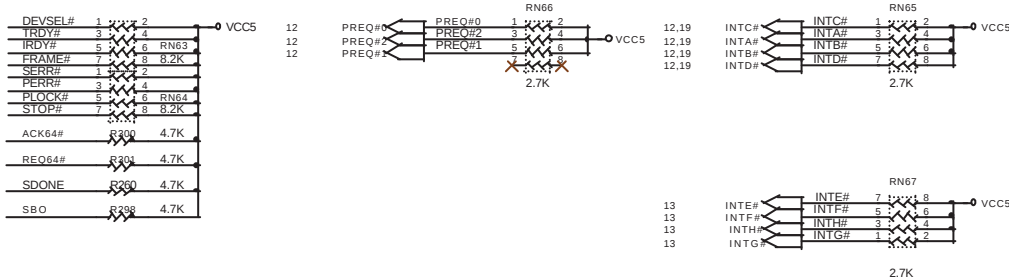
IDESEL = AD17

MASTER = INTB#
PREQ1

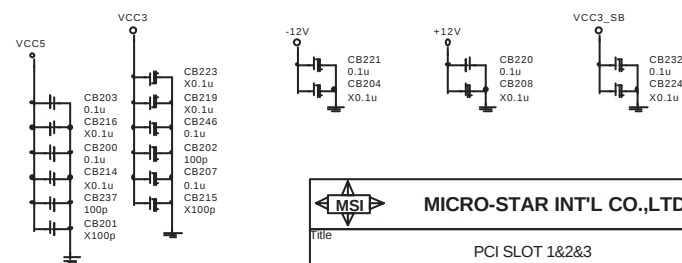
IDESEL = AD18

MASTER = INTD#
PREQ2

PCI PULL-UP / DOWN RESISTORS

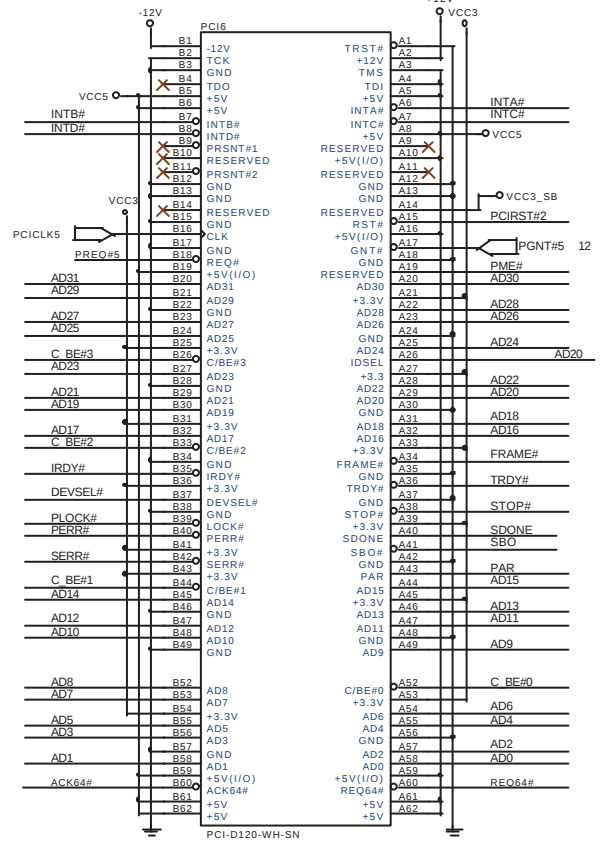


PCI SLOT DECOUPLING CAPACITORS

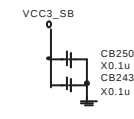
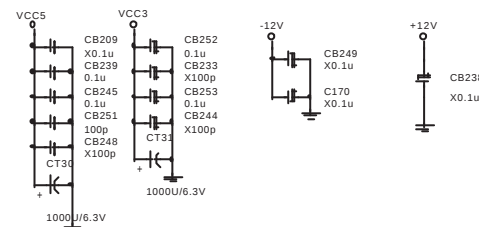


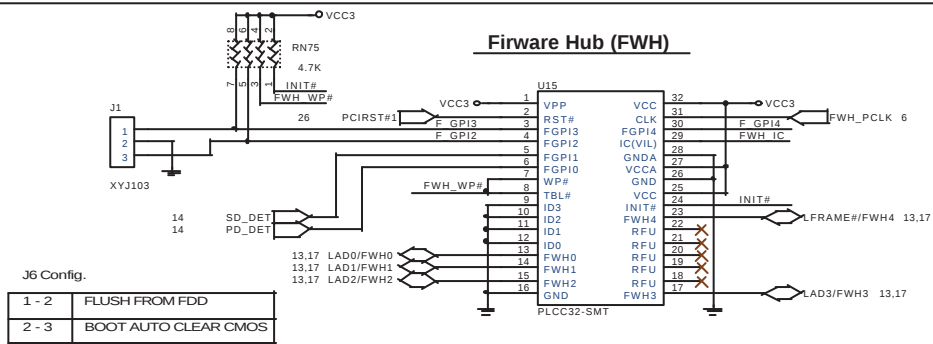
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Title: PCI SLOT 1&2&3	
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PCI SLOT 6 (PCI VER: 2.2 COMPLY)

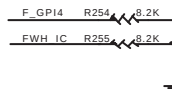


```
IDSEL = AD20
MASTER = PREQ5
INTB#
```

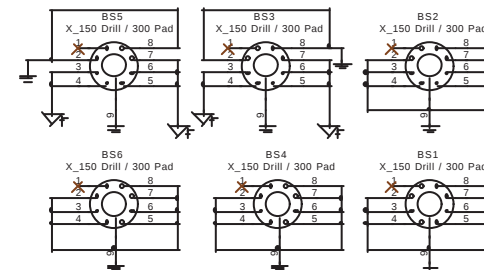
[illegible]



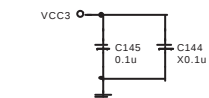
FWH RESISTORS



PCB Mounting Holes

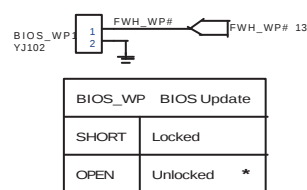


FWH DECOUPLING CAPACITORS

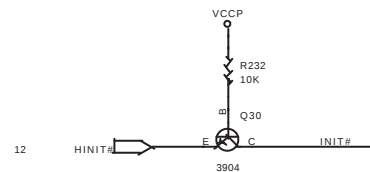


Place Cap. as Close to FWH< 350 mil

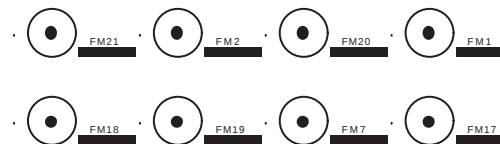
FWH write protect



FWH INIT Signal Voltage Translation Block

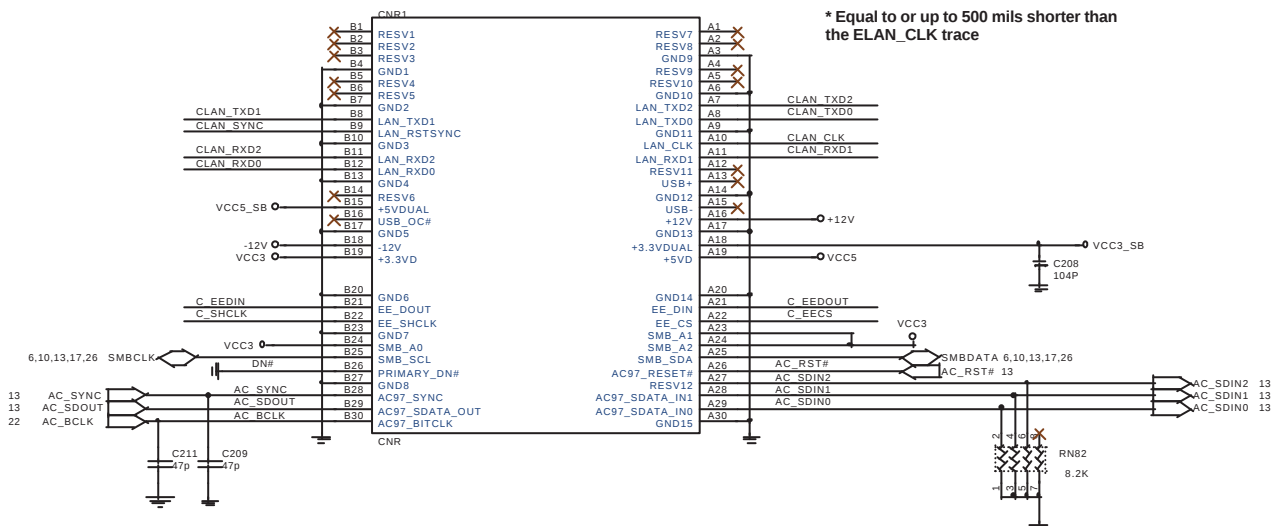


PCB Fiducials

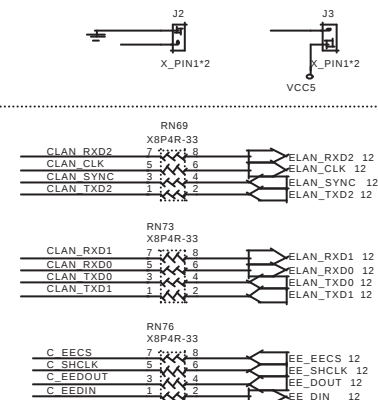


CNR RISER

- * LAN Trace width : 5 mils
- * AC'97 Trace Spacing : 10 mils
- * Maxium trace length < 9.5"
- * Equal to or up to 500 mils shorter than the ELAN_CLK trace



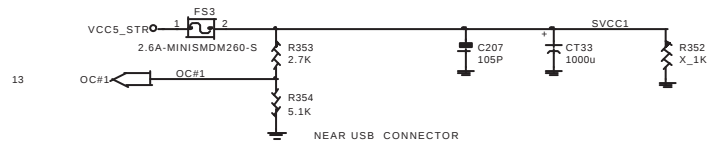
SIMULATION TRACE



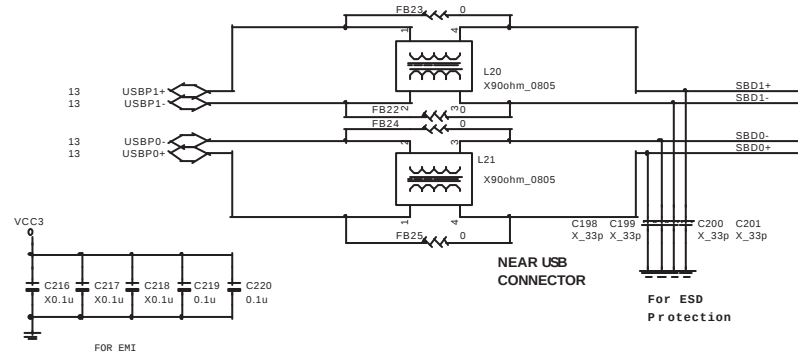
NEAR IC4 , NOT INSTALL WHEN USING AC97 LAN

MICRO-STAR INT'L CO.,LTD.		
Title: FWH & CNR		
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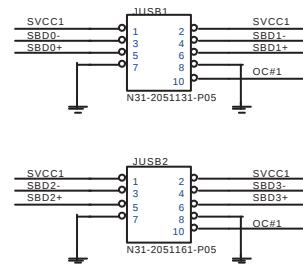
POWER CIRCUIT FOR USB PORT 0,1,2,3



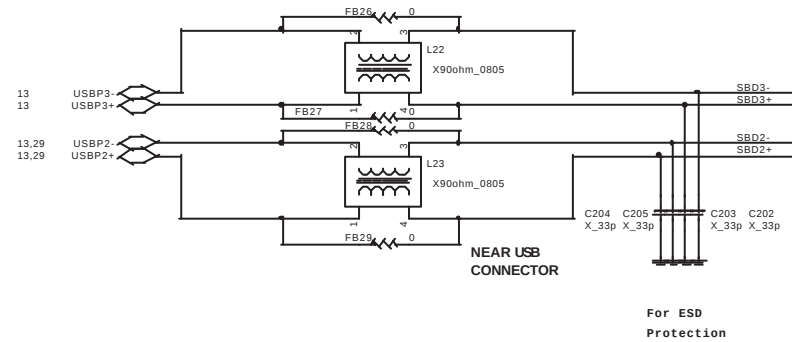
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



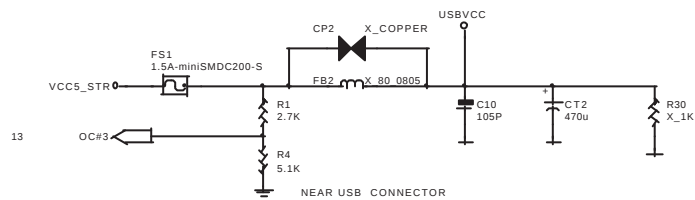
Intel Front USB Header



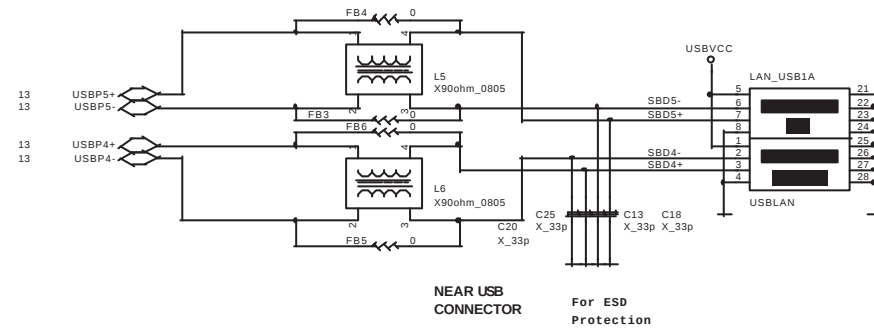
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 4,5



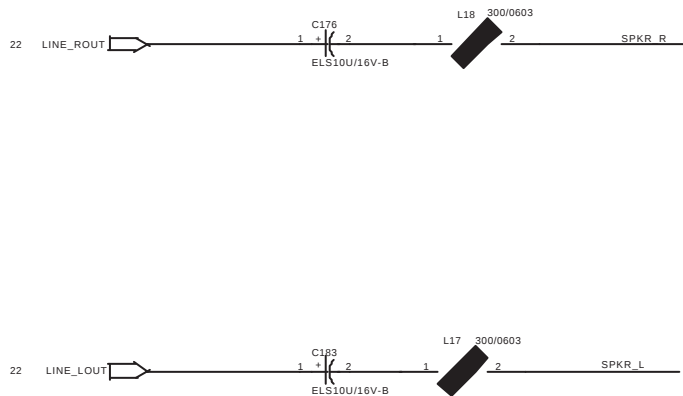
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



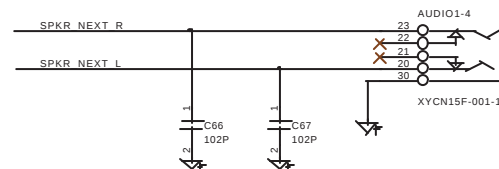
- * USB Trace width :9mils
- * USB Trace Spacing:25mils
- * Differential USB Signlas Trace, Spacing:18mils
- * USB Power Trace must be 40mil width

MICRO-STAR INT'L CO.,LTD.		
Title: USB CONNECTORS		
Size	Document Number	Rev
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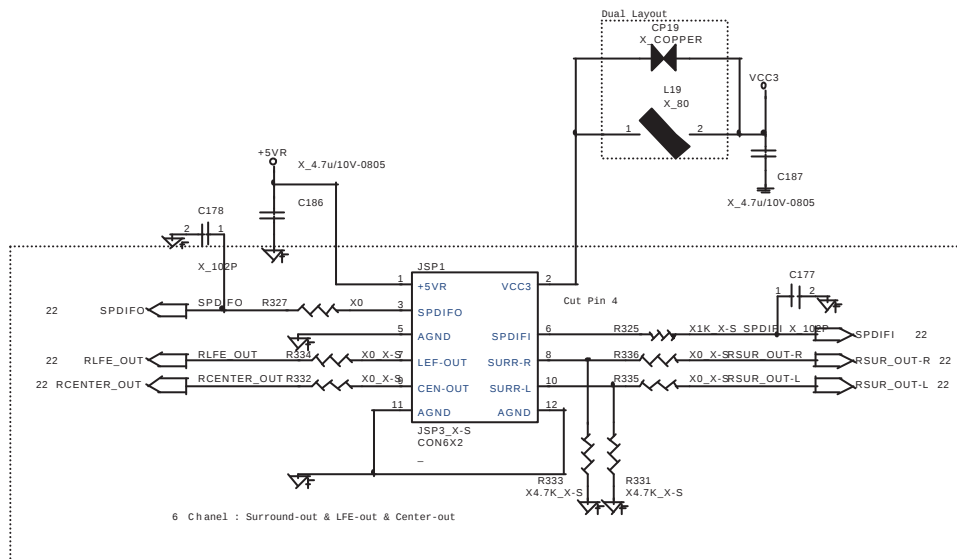
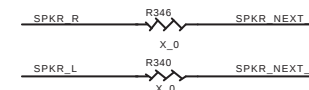
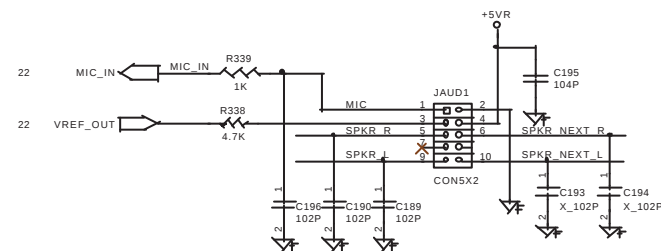
SPEAKER OUT CIRCUIT



SPEAKER OUT JACK



FOR Intel INTERNAL HEADER



		MICRO-STAR INT'L CO.,LTD.	
		AUDIO CONNECTOR	
Size	Document Number	MS-6580	Rev 20
Date:	Monday, June 10, 2002	Sheet	23 of 33

SERIAL PORT 1

The schematic diagram illustrates the hardware for Serial Port 1, centered around a 75232-1 UART chip (U6) and an LPT1B interface.

Power and Grounding:

- +12V:** Connected to VCC (pin 20) and V+ (pin 1) of the 75232-1. Decoupled by capacitor C50 (0.1uF).
- 12V:** Connected to GND (pin 11) and V- (pin 5) of the 75232-1. Decoupled by capacitor C51 (0.1uF).
- Microcontroller (U6):** VCC (pin 20) is connected to +12V. GND (pin 11) is connected to -12V.
- LPT1B:** Powered by +12V and -12V rails. Decoupled by capacitors C54 (0.1uF) and C55 (0.1uF).

Signal Connections:

- Microcontroller (U6) to 75232-1:**
 - DCDA (pin 2) to VCC
 - RXDA (pin 3) to DIN1 (pin 16)
 - RIA (pin 4) to DIN2 (pin 15)
 - CTSA (pin 7) to DIN3 (pin 13)
 - DSRA (pin 8) to DIN4 (pin 11)
 - ROUT1 (pin 19) to DOUT1 (pin 5)
 - ROUT2 (pin 18) to DOUT2 (pin 6)
 - ROUT3 (pin 17) to DOUT3 (pin 8)
 - ROUT4 (pin 14) to DOUT4 (pin 10)
 - ROUT5 (pin 12) to DOUT5 (pin 9)
- 75232-1 to LPT1B:**
 - DTRA# (pin 16) to LPT1B pin 26
 - RTSA# (pin 15) to LPT1B pin 27
 - SOUTA# (pin 13) to LPT1B pin 28
- LPT1B to Interface:**
 - LPT1B pin 31 to DSRA
 - LPT1B pin 32 to RTSA
 - LPT1B pin 33 to CTSA
 - LPT1B pin 34 to RIA

Other Components:

- Diodes:** D2 (1N4148-S-LL34) and D3 (1N4148-S-LL34) are used for signal conditioning.
- Capacitors:** C53, C54, C55 are 0.1uF capacitors. CB94, CB98, CB103, and CB99 are 0.1uF capacitors.

SERIAL PORT 2

The schematic diagram for Serial Port 2 shows the following components and connections:

- 75232-1 IC:** Pins 16 (DIN1), 15 (DIN2), 13 (DIN3), 11 (GND), 5 (DOUT1), 6 (DOUT2), 8 (DOUT3), and 10 (GND).
- U110:** Pins 1 (VCC), 19 (ROUT1), 18 (ROUT2), 17 (ROUT3), 14 (ROUT4), 12 (ROUT5), 20 (VCC), 2 (RIN1), 3 (RIN2), 4 (RIN3), 7 (RIN4), and 9 (RIN5).
- Capacitors:** C108 (0.1uF), C109 (0.1uF), C110 (0.1uF), C112 (0.1uF), C116 (0.1uF), and C102 (0.1uF).
- Power Supply:** VCC5, +12V, -12V, and GND.
- Signal Lines:** DTRB, RIB, RXDB, RIB, CTB, DSRB, DTRB, RIB, TXDB, CTB, and DSRB.

For EM

COM2 HEADER

The pinout for the COM2 header is as follows:

Pin	Signal
1	DTRB
2	RIB
3	RXDB
4	RIB
5	CTB
6	DSRB
7	DTRB
8	RIB
9	TXDB
10	CTB
11	DSRB
12	DTRB
13	RIB
14	TXDB
15	CTB
16	DSRB

PARALLAL PORT

The schematic diagram illustrates the Parallel Port interface. It shows the connection of a microcontroller (pin 17) to various peripheral chips through a series of connectors (CN6, CN5, CN4, CN7) and a diode (IN1448S).

Microcontroller Connections (Pin 17):

- LP_D1, LP_D0, LP_D4, LP_D5, LP_D2, LP_D3, LP_D6, LP_D7, LP_SLCT, LP_PE, LP_BUSY, LP_ACK#, LP_SLIN#, LP_AFD#, LP_ERR#, LP_INIT#, LP_STB#

Peripheral Chip Connections:

- CN6:** LP_D5, LP_D4, LP_D0, LP_D1, LP_D2, LP_D3, LP_D6, LP_D7, LP_ACK#, LP_BUSY, LP_PE, LP_SLCT, LP_INIT#, LP_ERR#, LP_SLIN#, LP_STB#
- CN5:** LP_D2, LP_D3, LP_D6, LP_D7
- CN4:** LP_ACK#, LP_BUSY, LP_PE, LP_SLCT
- CN7:** LP_INIT#, LP_ERR#, LP_SLIN#, LP_STB#
- LPT1A:** LP_STB#, LP_D0, LP_D1, LP_D2, LP_D3, LP_D4, LP_D5, LP_D6, LP_D7, LP_ACK#, LP_BUSY, LP_PE, LP_SLCT
- CP6:** FB10, X80, 0805, K_COPPER

Diode (IN1448S): VCC5, D4

Resistors: RN30, 2.2K, RN28, 2.2K, RN26, 2.2K, RN33, 2.2K, R98, 2.2K

PS2 KEYBOARD & MOUSE CONNECTOR

The diagram illustrates the electrical connections for a PS2 Keyboard & Mouse Connector. It shows a USBVCC supply connected to a network of resistors (RN1, R6) and capacitors (C1, C2). The signal lines are labeled MSCLK, MSCLK, KBCLK, and KBCLK. The connector is labeled CN1 220p. The output is a MINIDINx2-D12-ML connector with pins 1 through 17. The diagram also shows a USBVCC supply connected to a network of resistors (RN1, R6) and capacitors (C1, C2).

None VGA connector then stuff

LPT1C

DCDB 35 40 DSRB
RXDB 36 41 RTSB
TXDB 37 42 CTSB
DTRB 38 43 RIB

LPT-D25-BK-BI

RTSB 2 1
RXDB 4 3
DSRB 6 5
DCDB 8 7

RIB 2 1
CTSDB 4 3
DTRB 6 5
TXDB 8 7

CN16 X220p
CN17 X220p

VCC5_SB

JWR105
XYJ105

R358
R356
R357
R359
X330k
X10K
X104P

Q42 X2N3904S
Q41 X2N3906S
Ic=200mA
Vbe=5V
Vceo=40V

RING# 13

CP9 1 2X COPPER

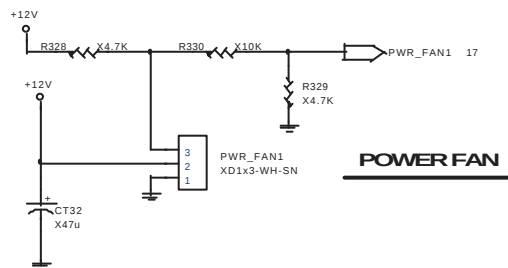
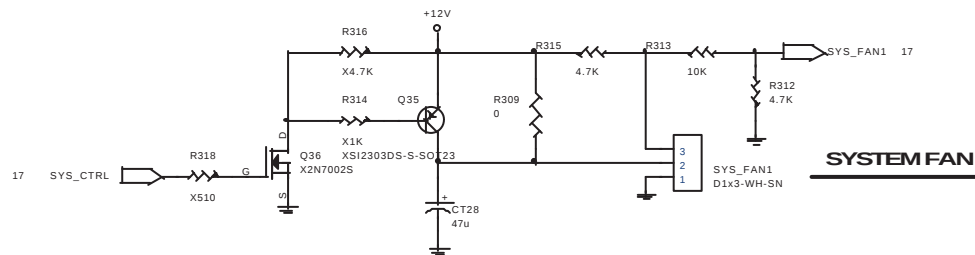
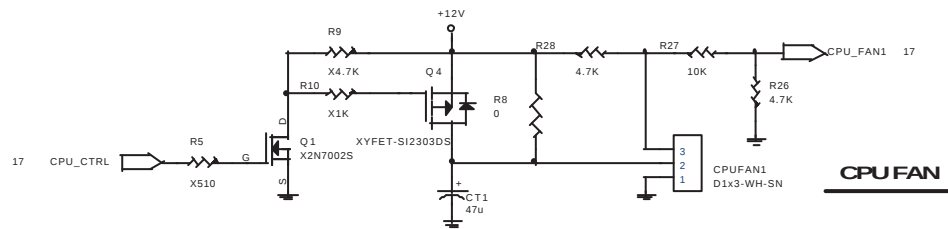
L15 X80 0805

MSI MICRO-STAR INT'L CO.,LTD.

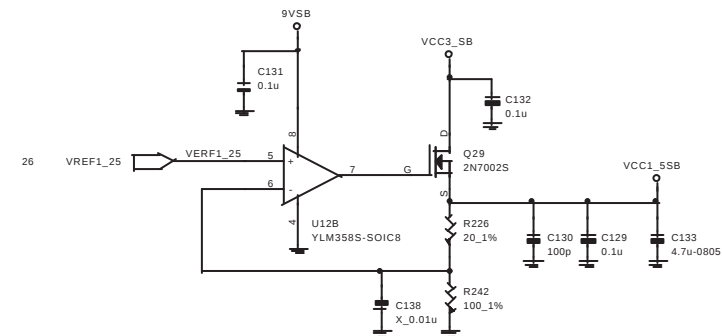
Title I/O CONNECTORS

Size Document Number MS-6580 Rev 20

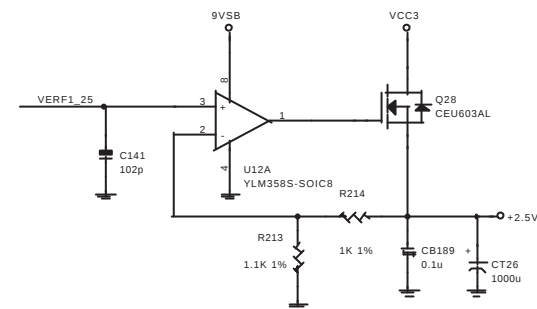
Date: Monday, June 10, 2002 Sheet 24 of 33



1.5V STANDBY POWER TRANSLATOR (40mils trace / 20 mils space)



AGP4X & GMCH 1.5V POWER TRANSLATOR



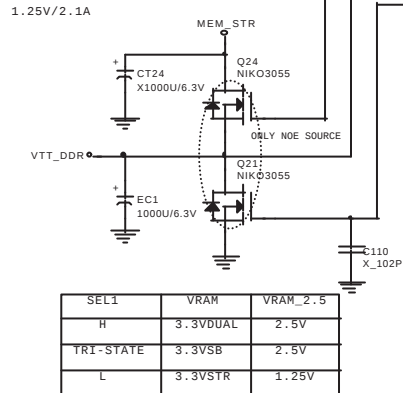
 MICRO-STAR INT'L CO.,LTD.		Title	
		FAN	
Size	Document Number	Rev	
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

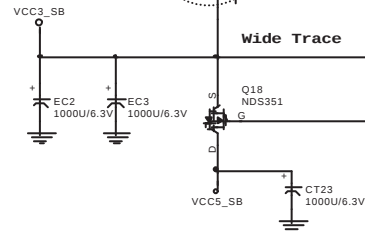
SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

DDR VTT Power

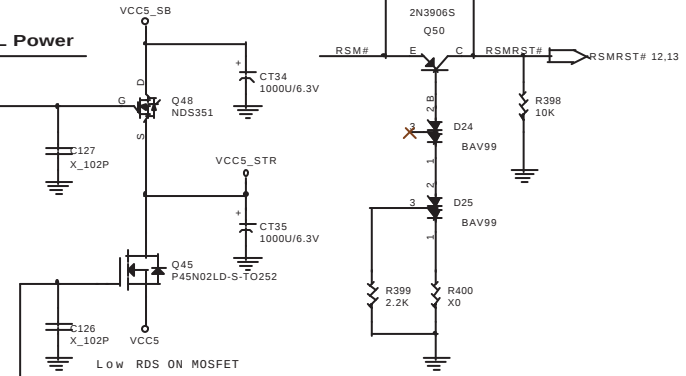


FOR 3VSB OR 3VSTR
SETTING BY SEL1

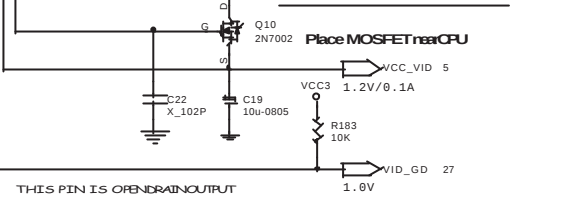


** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

5V DUAL Power

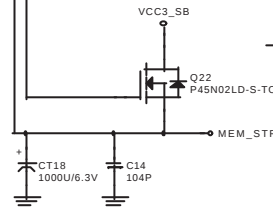


VCC_VID / VID_GOOD

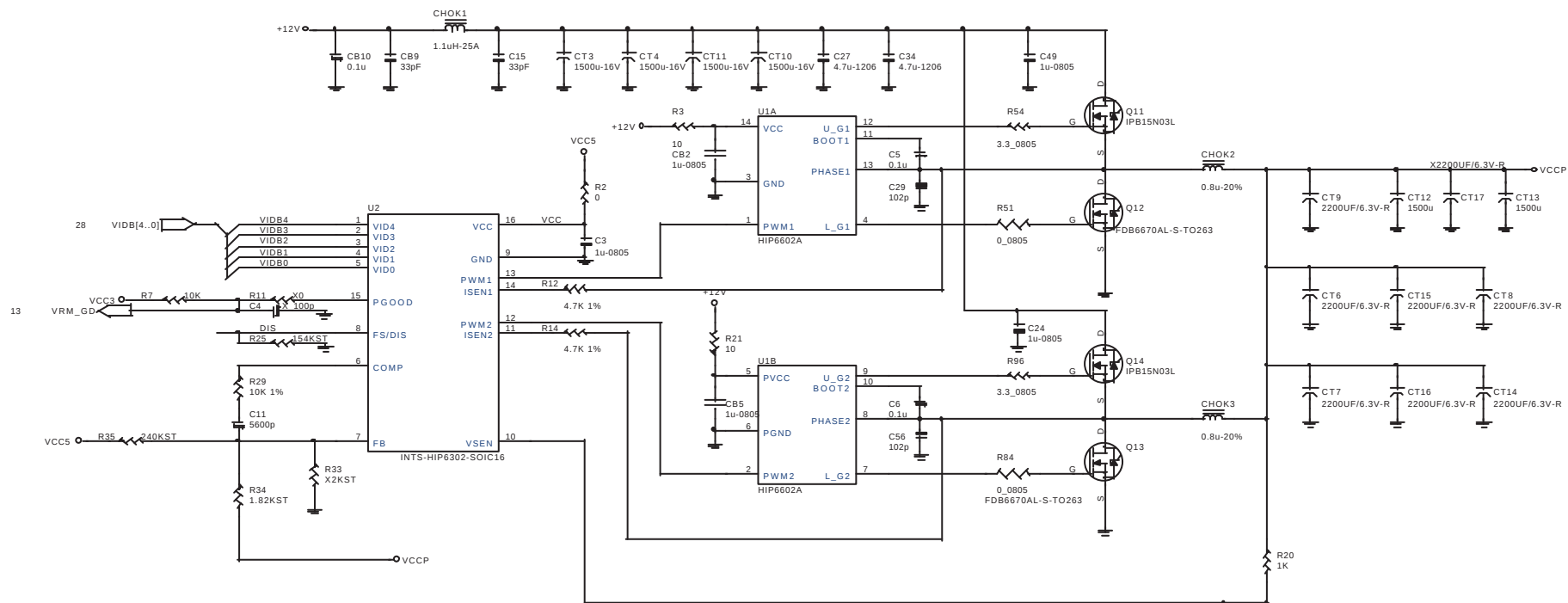


DDR 2.5V Power

2.5V/2.8A+5.92A

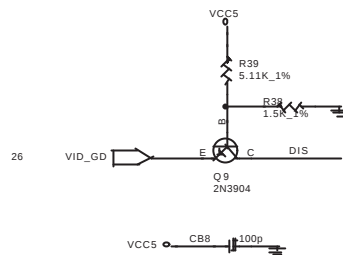


MICRO-STAR INT'L CO.,LTD.			
Title ACPI CONTROLLER			
Size	Document Number	MS-6580	Rev 20
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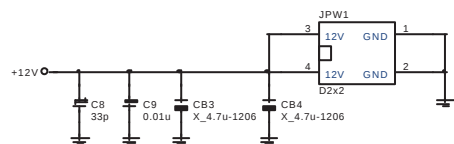


HIP6301 – VRM 9.0/9.2

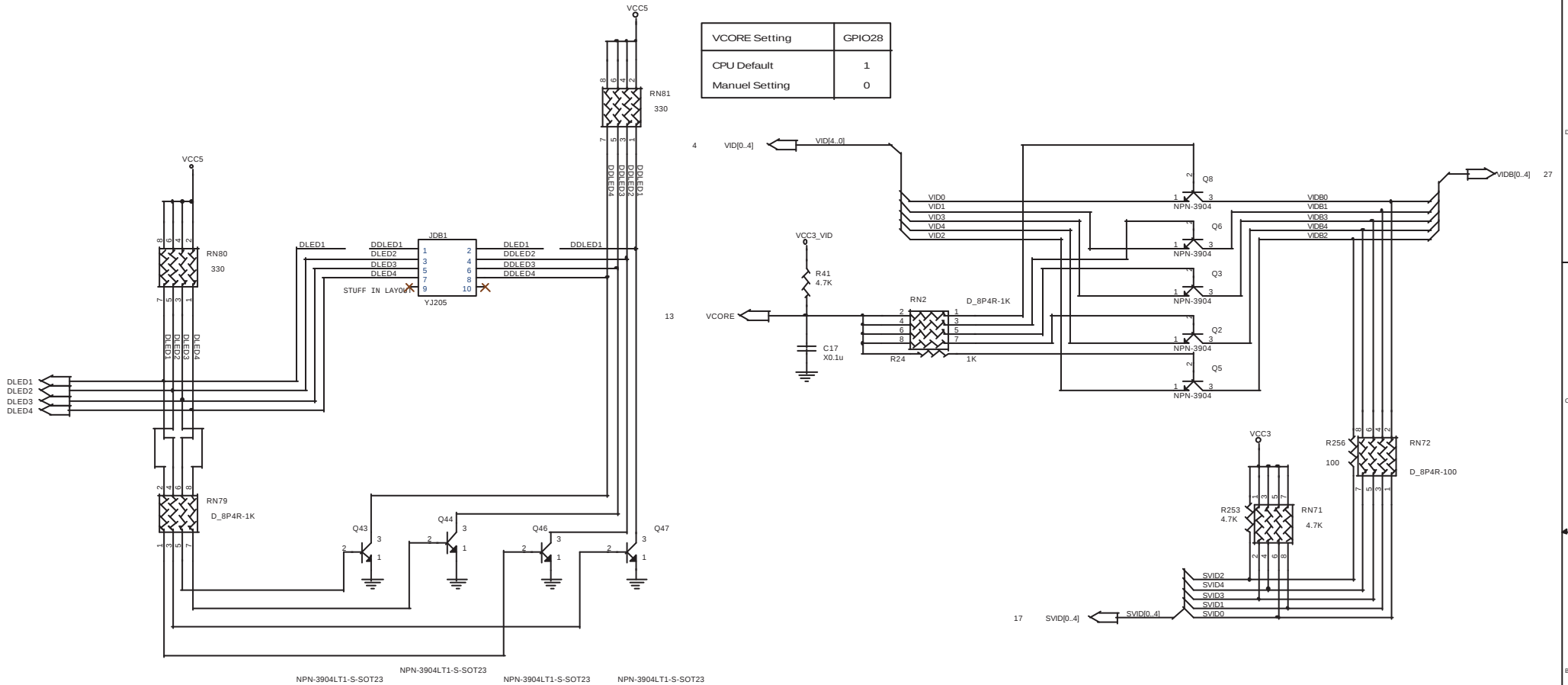
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	1	OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550



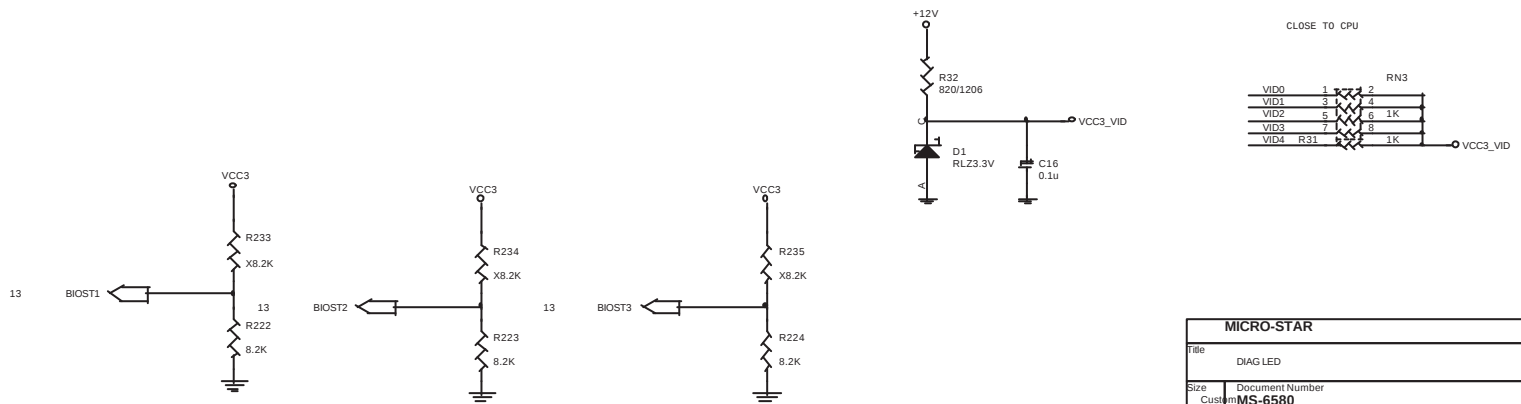
ATX12V POWER CONNECTOR



VCORE Setting	GPIO28
CPU Default	1
Manuel Setting	0

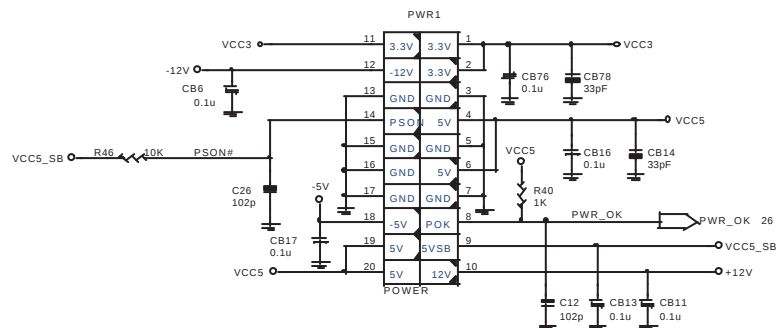


VID PULL-UP RESISTORS

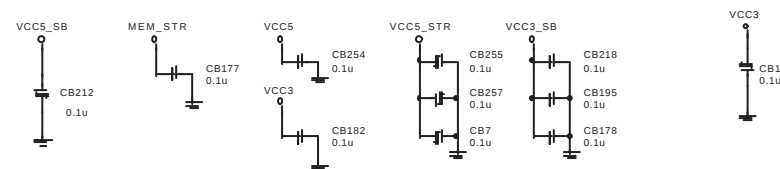


MICRO-STAR			
File	DIAG LED		
Size	Document Number	Rev	
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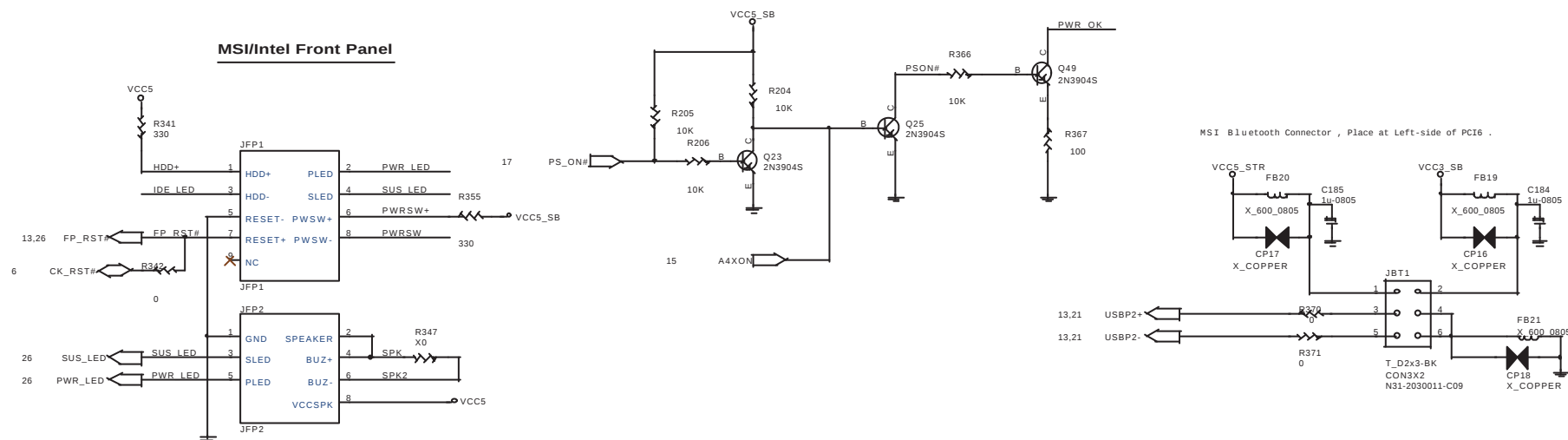
ATX CONNECTOR



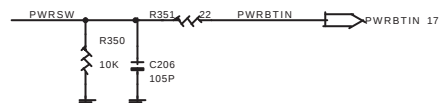
REGULATORS OUTPUT DECOUPLING CAPACITORS



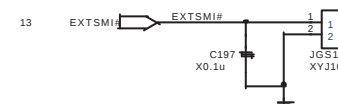
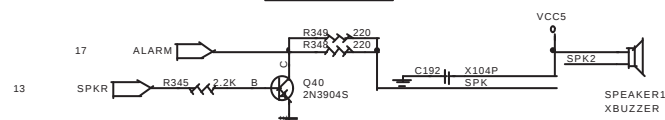
MSI/Intel Front Panel



POWER BUTTON



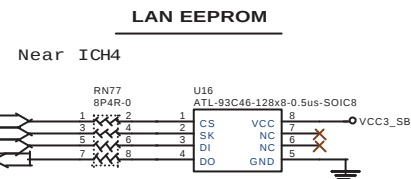
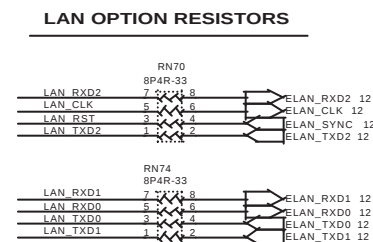
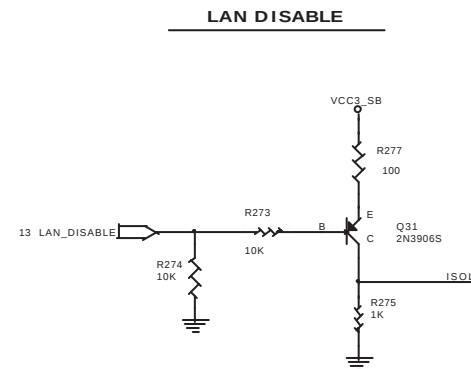
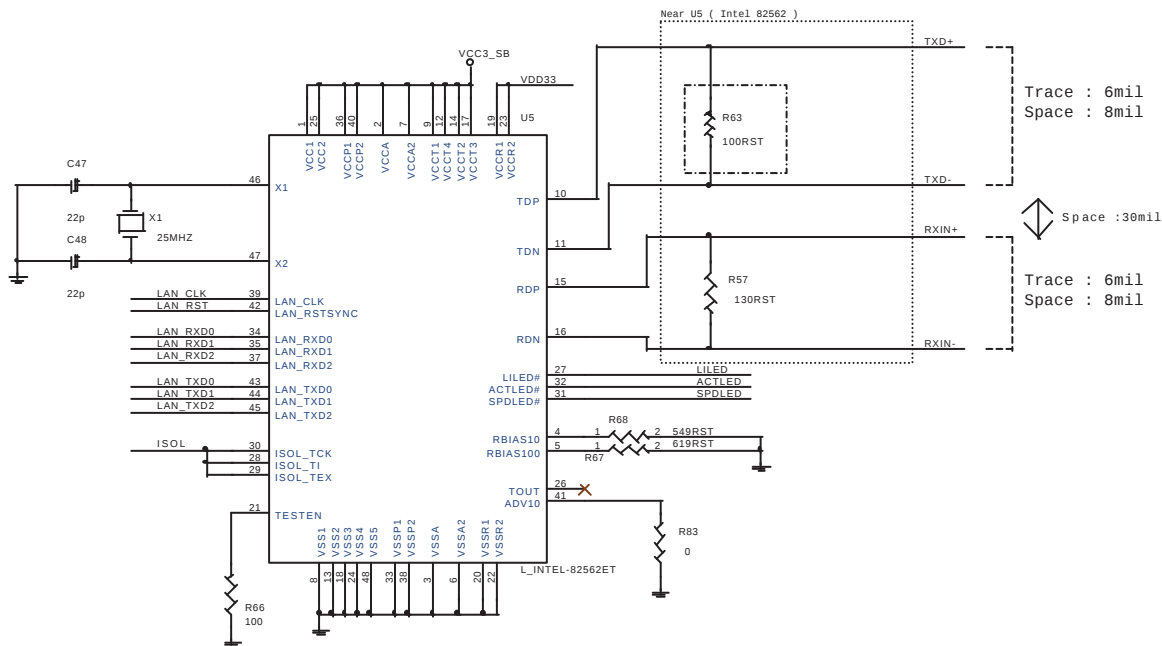
SPEAKER



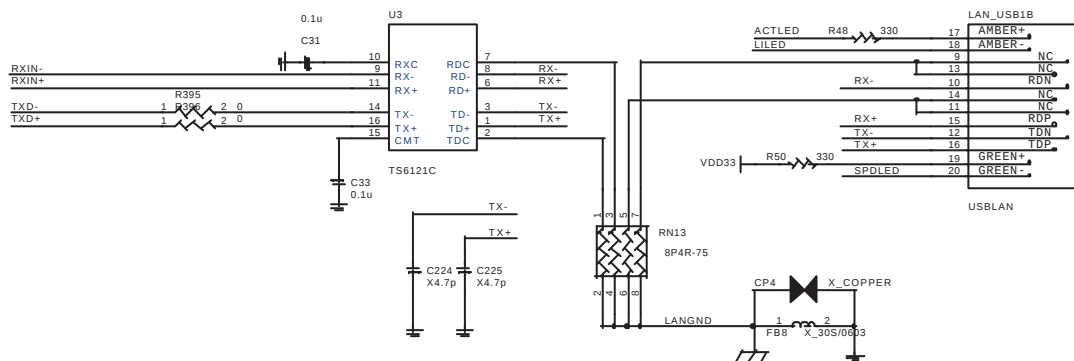
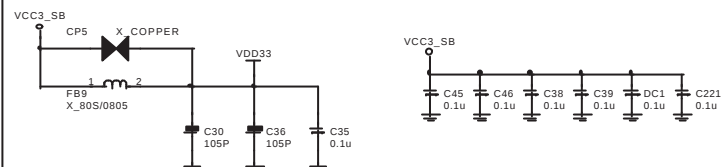
MICRO-STAR INT'L CO.,LTD.

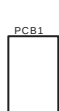
Title			Front Panel & ATX Connector & FAN
Size	Document Number	MS-6580	
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Place Termination R as close to 82562EM as possible

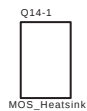
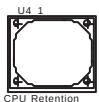
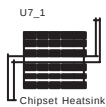


Remark:
82562EM with 93C66:M33-26N0103-A26
82562ET with 93C46:M33-1500203-A26





BAT1_X
BATTERY



JBAT1(1-2)
YJUMPER-MG

JAUDIO1(6-6)
YJUMPER-MG

JAUDIO1(9-10)
YJUMPER-MG

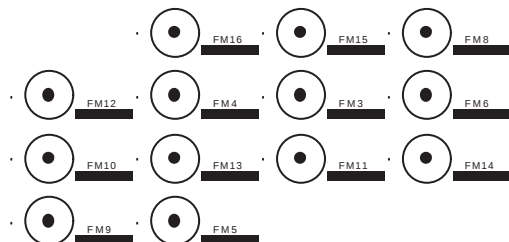
JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

BIOS_WP BIOS Update	
SHORT	Locked
OPEN	Unlocked *

J6 Config. mode	
1 - 2	Normal *
2 - 3	Configuration Mode
OPEN	Recovery

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

COMPONENT Fiducials



MICRO-STAR INT'L CO.,LTD.

Title			
MANUAL PARTS			
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General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	PREQ # 5 (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifunction pin)
GPIO 12	I	Pull down through 10K ohms (unused)
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	PGNT # 5 (multifunction pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	Vcore for cpu voltage adjusting
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	LAN DISABLE
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	BIOST3 FOR BIOS SETTING
GPIO 33	I/O	BIOST2 FOR BIOS SETTING
GPIO 34	I/O	BIOST1 FOR BIOS SETTING
GPIO 35	I/O	No Connected
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE1 DETECT
GPI 1	I	ATA IDE2 DETECT
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0 PREQ#0 PGNT#0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1 PREQ#1 PGNT#1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2 PREQ#2 PGNT#2	12 (PCI5)
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19	PCICLK3 PREQ#3 PGNT#3	6 (PCI0)
PCI Slot 5	INTB# INTC# INTD# INTA#	AD21	PCICLK4 PREQ#4 PGNT#4	7 (PCI1)
PCI Slot 6	INTA# INTB# INTC# INTD#	AD20	PCICLK5 PREQ#5 PGNT#5	8 (PCI2)

* ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

DLED-Super I/O

GPIO Pin	Type	Function
GP24	I/OD	DLED1
GP33	I/OD	DLED2
GP34	I/OD	DLED3
GP23	I/OD	DLED4

 MICRO-STAR INT'L CO.,LTD.		
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