

MS6575E

VERSION:10a

SIS 645DX/651 CHIPSET

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

SIS 645DX/651 (North Bridge)+962 (South Bridge)

On Board Chipset:

LPC Super I/O -- W83697HF

AGERE 1394 PHY FW802A

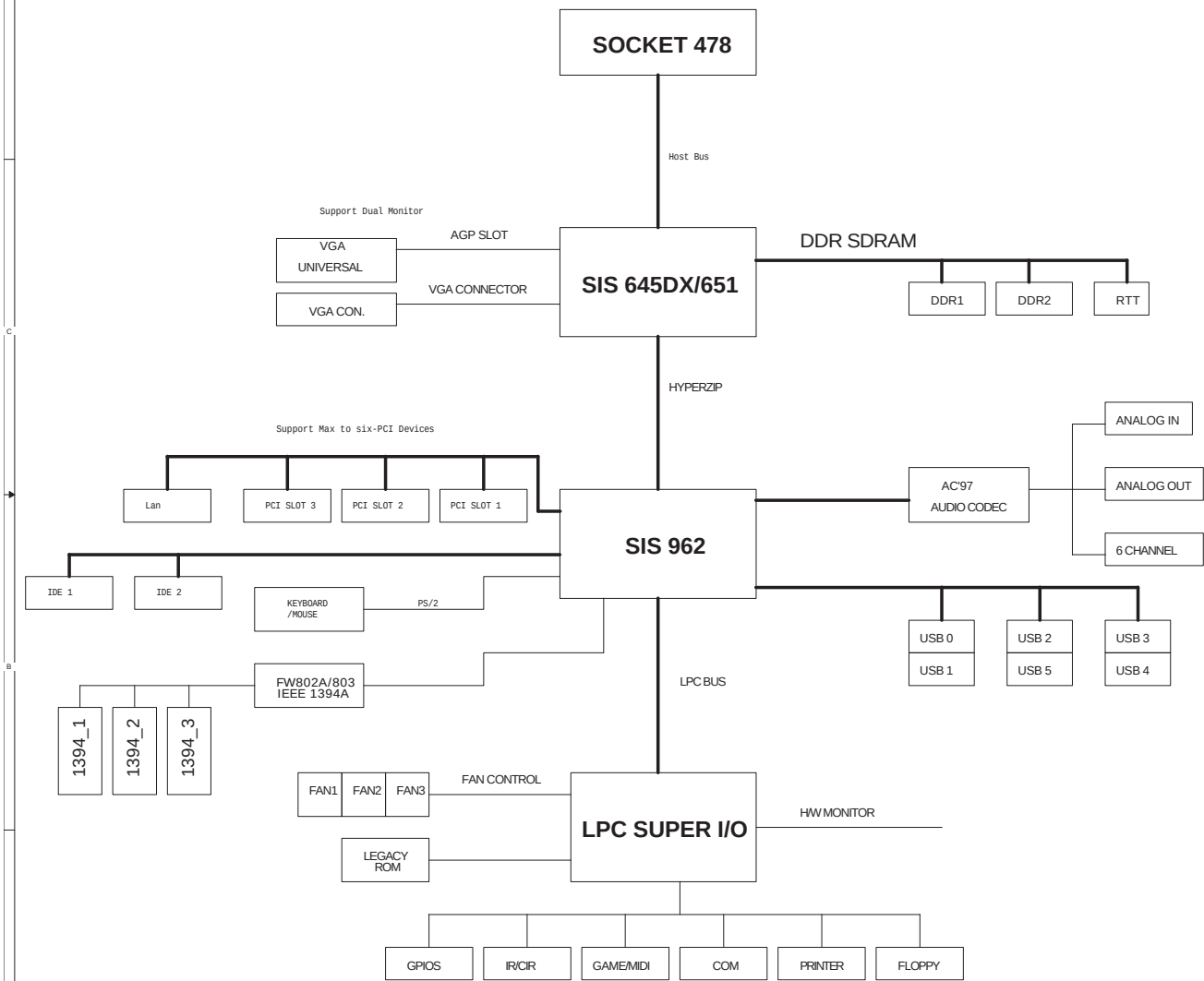
Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT* 3

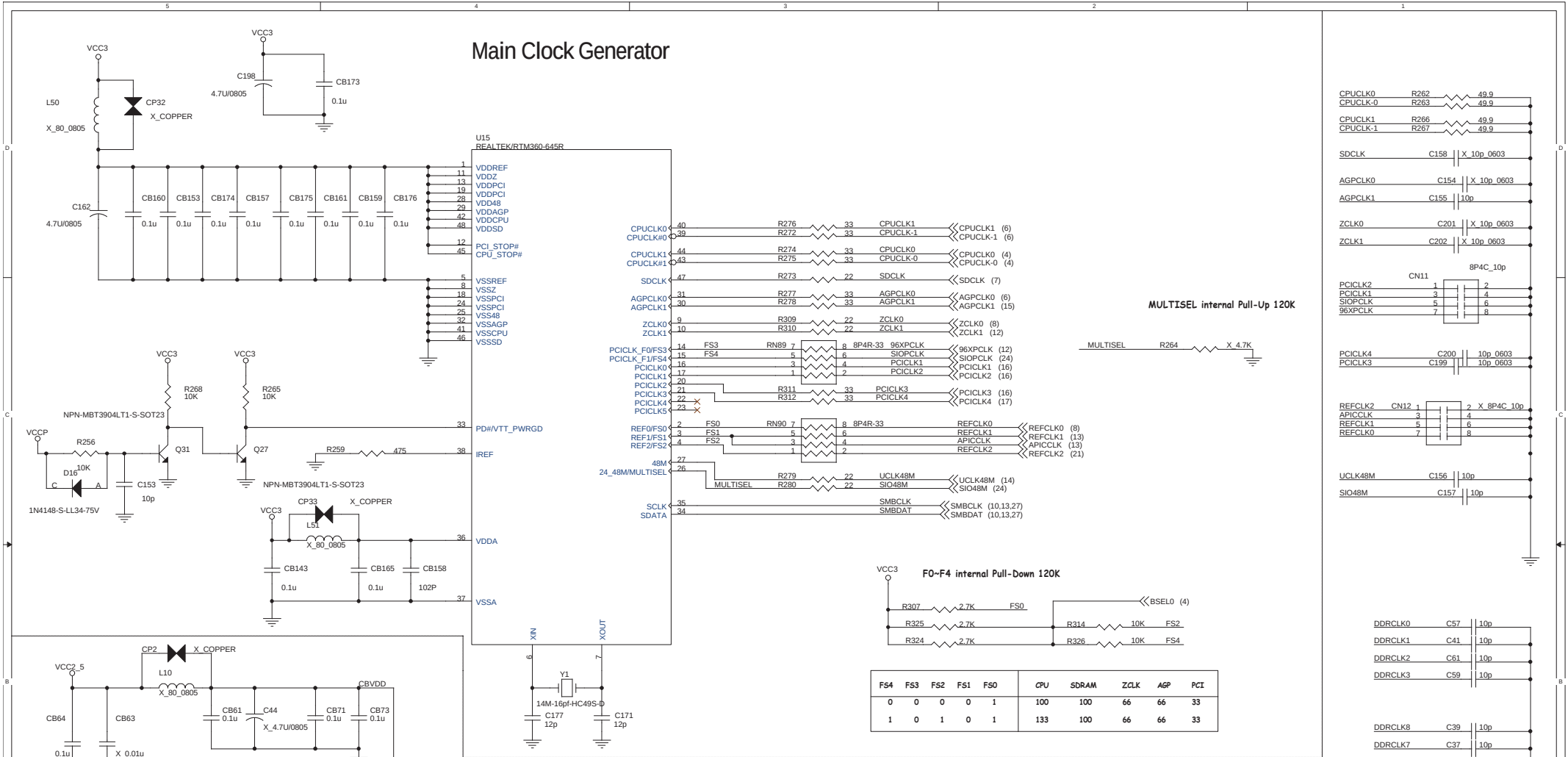
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System Block Diagram

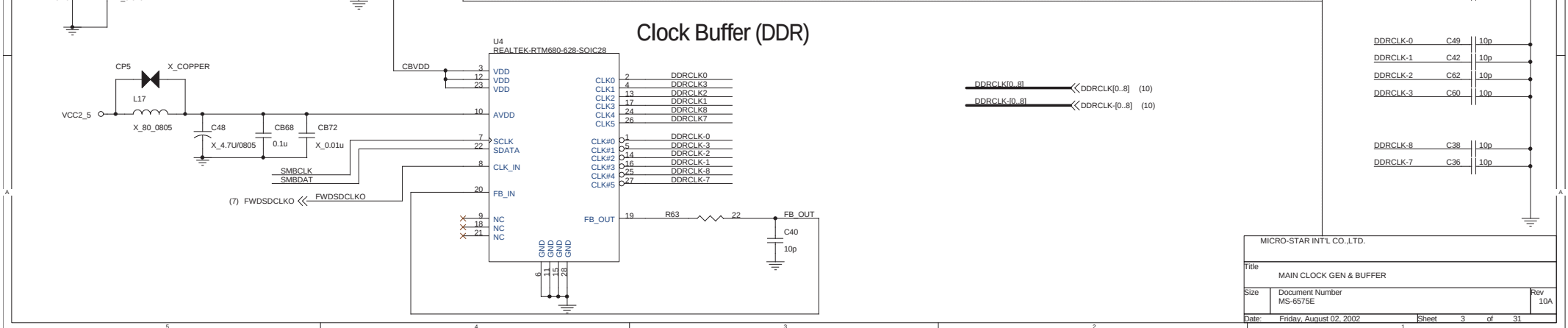


GPIO Table on SIS962			
GPIO_0	I/O	MAIN	Pull-Down
GPIO_1	I/O	MAIN	Pull-Down
GPIO_2	I/O	MAIN	THERM#
GPIO_3	I/O	MAIN	EXTSMI#
GPIO_4	I/O	MAIN	Pull-Down
GPIO_5	I/O	MAIN	PREQ#5(Pull-Up)
GPIO_6	I/O	MAIN	PGNT#5(Pull-Up)
GPI_7	I/O	RESUME	LAN_WAKE#
GPI_8	I	RESUME	RING
GPI_9	I	RESUME	RESERVED
GPI_10	I	RESUME	RESERVED
GPIO_11	I/O	RESUME	RESERVED
GPIO_12	I/O	RESUME	Pull-Down
GPIO_13	I/O	RESUME	Flash Rom protection H: Disable, L: Enable
GPIO_14	I/O	RESUME	Pull-Down
GPIO_15	I/O	RESUME	KBDAT
GPIO_16	I/O	RESUME	KBCLK
GPIO_17	I/O	RESUME	MSDAT
GPIO_18	I/O	RESUME	MSCLK
GPIO_19	I/O	RESUME	SMBCLK
GPIO_20	I/O	RESUME	SMBDAT

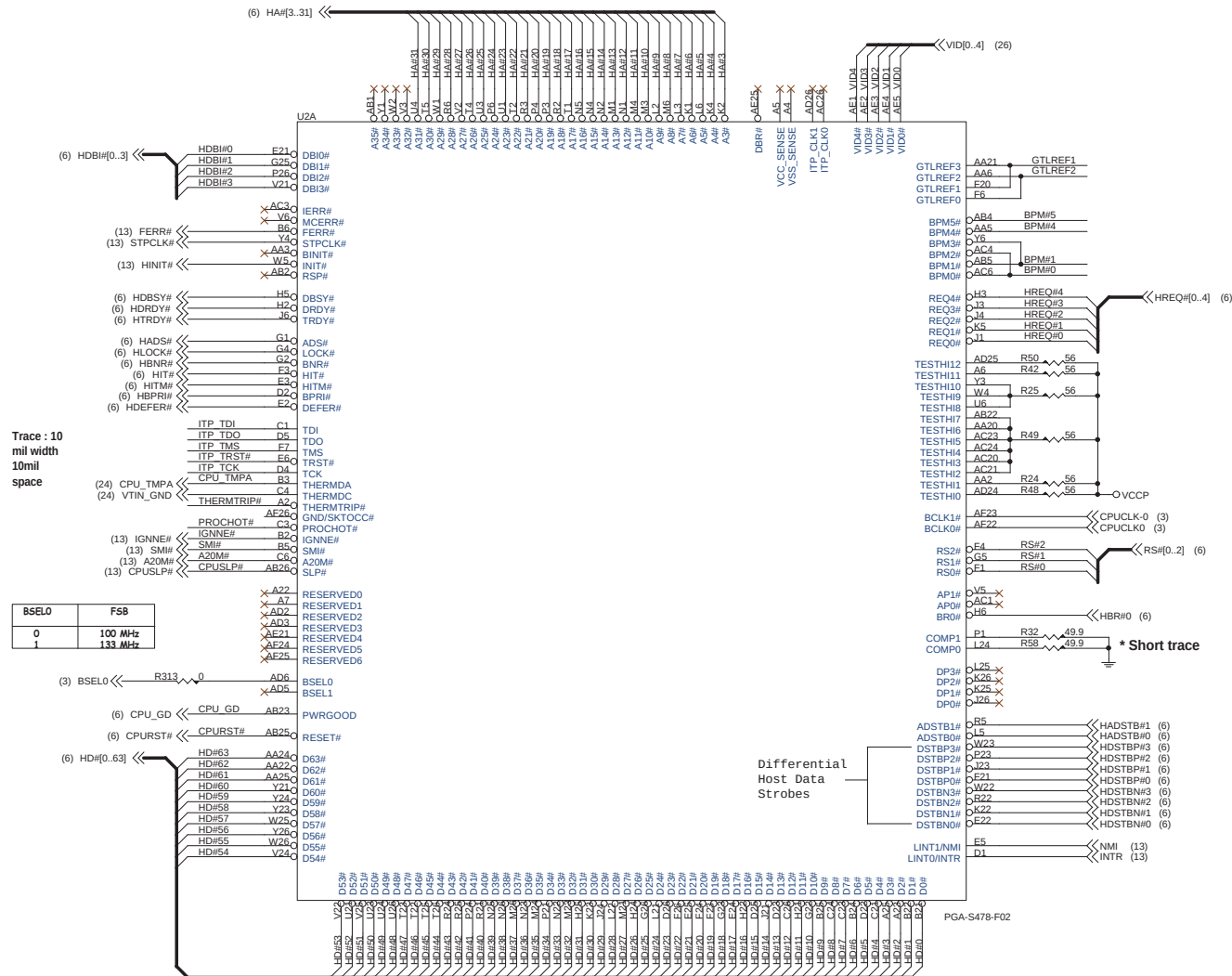
Main Clock Generator



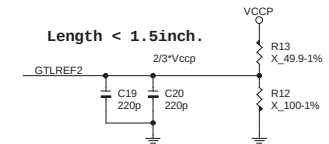
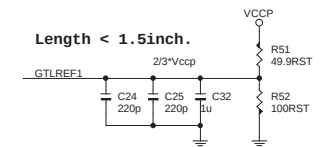
Clock Buffer (DDR)



CPU SIGNAL BLOCK

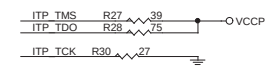


CPU GTL REFERENCE VOLTAGE BLOCK



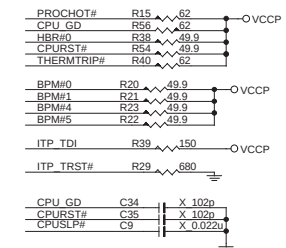
Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK

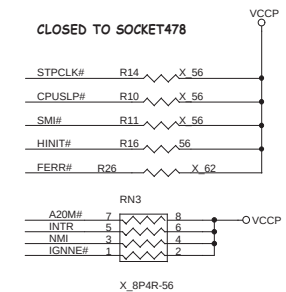


CPU STRAPPING RESISTORS

CLOSED TO SOCKET478

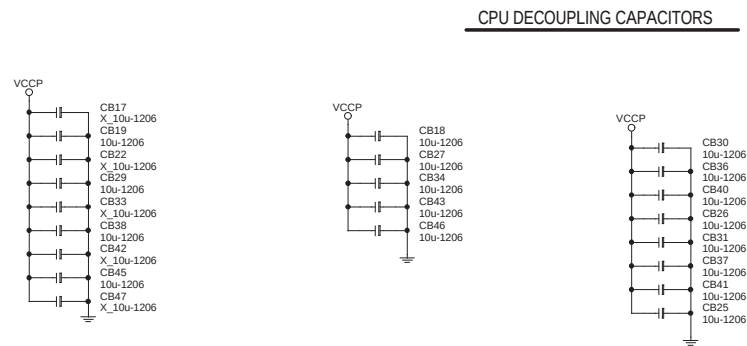
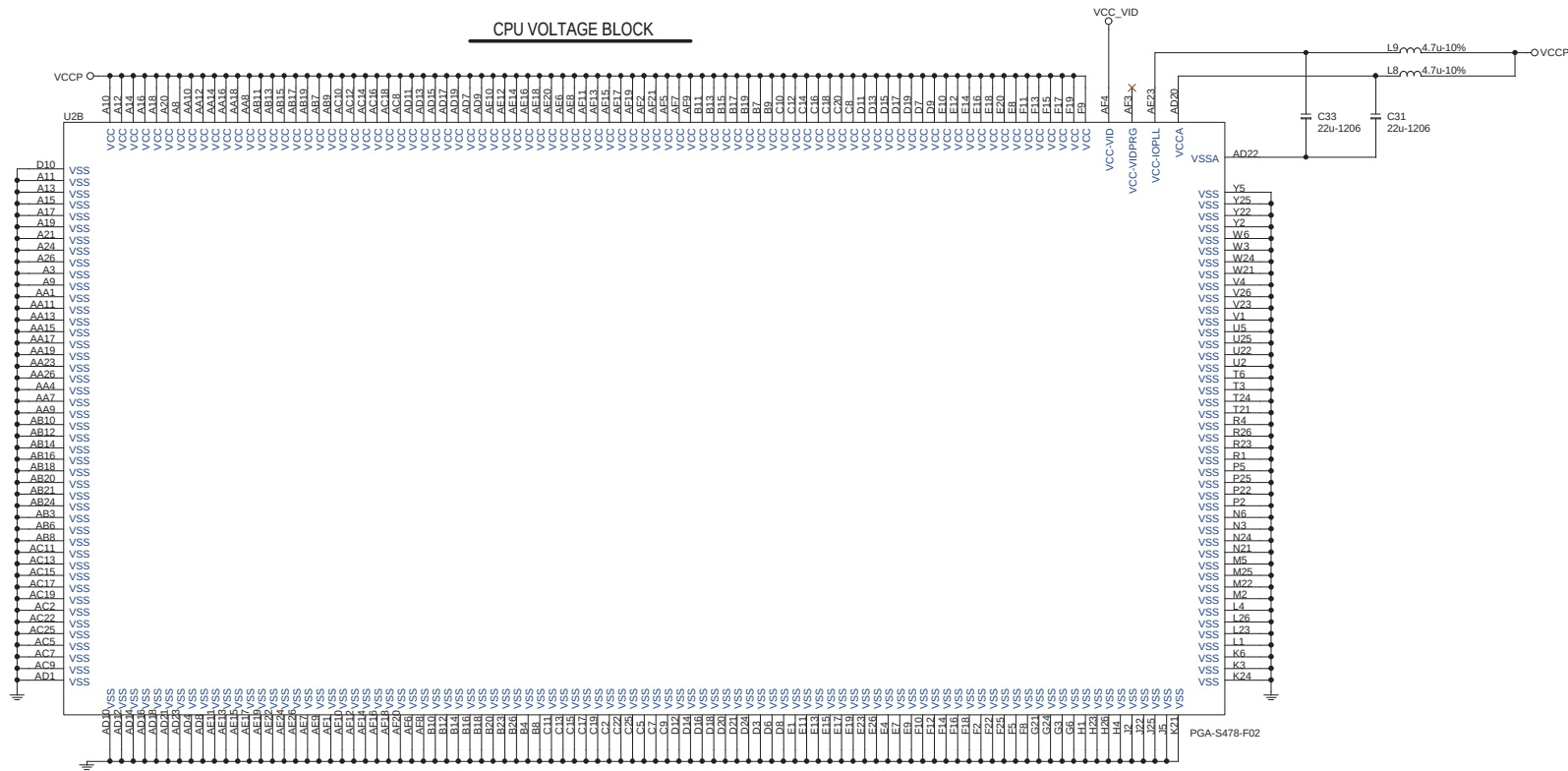


CLOSED TO SOCKET478



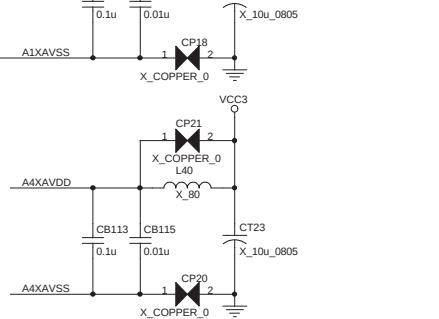
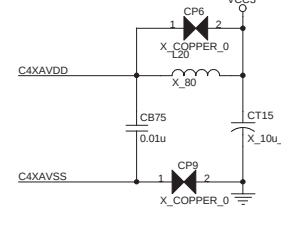
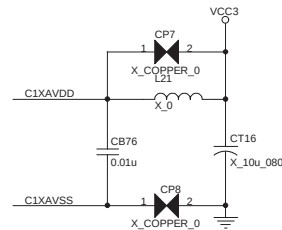
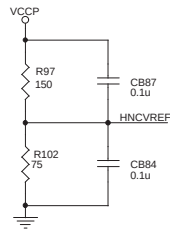
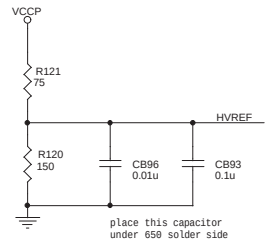
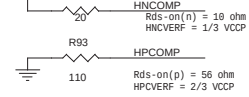
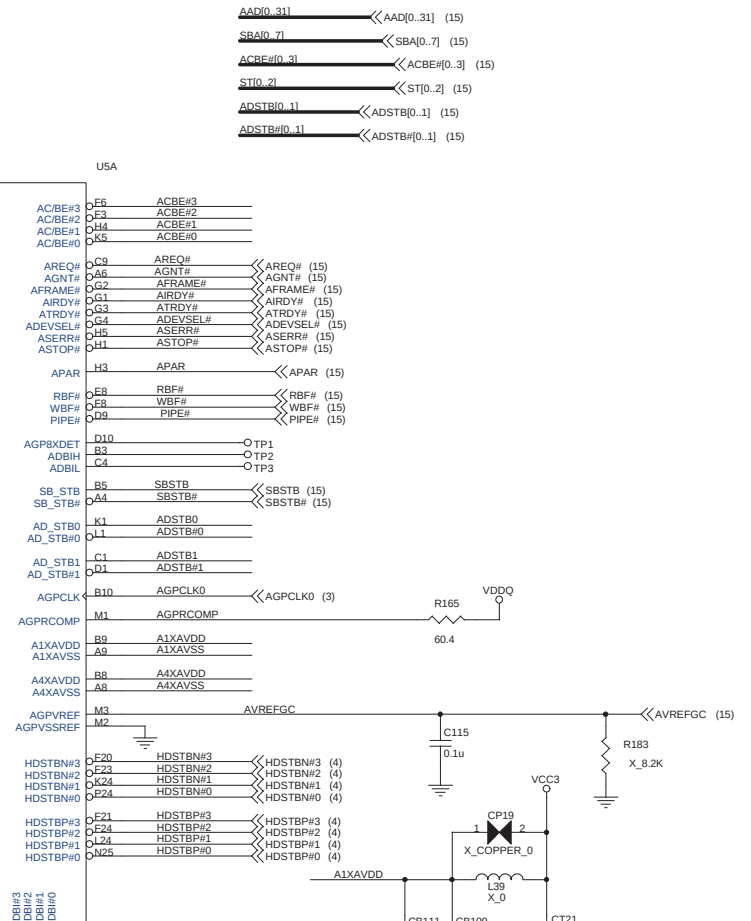
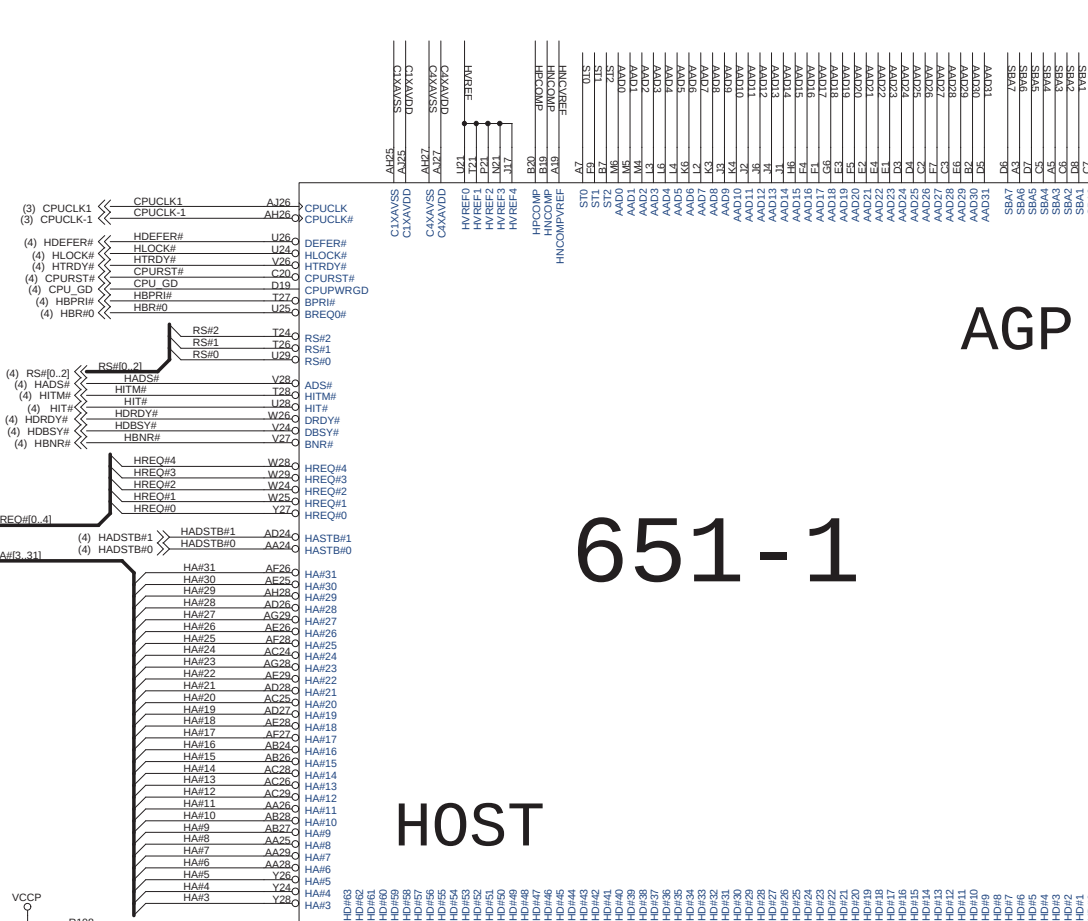
MICRO-STAR INT'L CO.,LTD.

Title			
mPGA478 CPU-1			
Size	Document Number		Rev
	MS-6575E		10A
Date:	Wednesday, August 14, 2002	Sheet	4 of 31



PLACE CAPS WITHIN CPU CAVITY

MICRO-STAR INT'L CO.,LTD.		
Title	mPGA478 CPU-2	
Size	Document Number MS-6575E	Rev 10A
Date:	Wednesday, August 14, 2002	Sheet 5 of 31



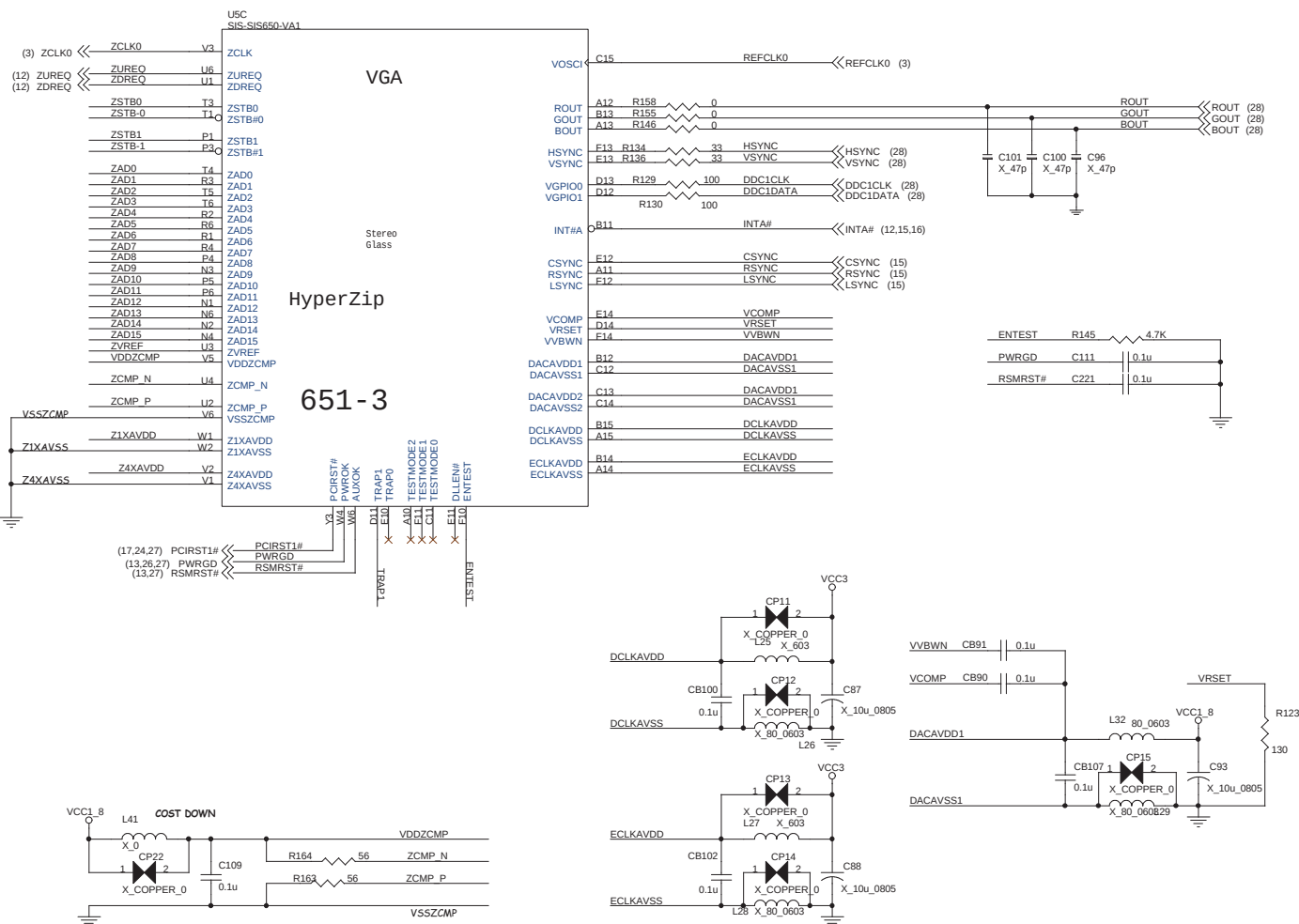
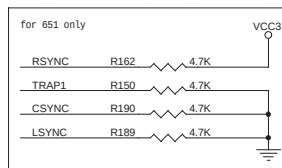
MICRO-STAR INT'L CO., LTD.		
Title	SIS645/650-1	
Size	Document Number	Rev
	MS-6575E	10A
Date:	Friday, August 02, 2002	Sheet 6 of 31

NB Hardware Trap Table

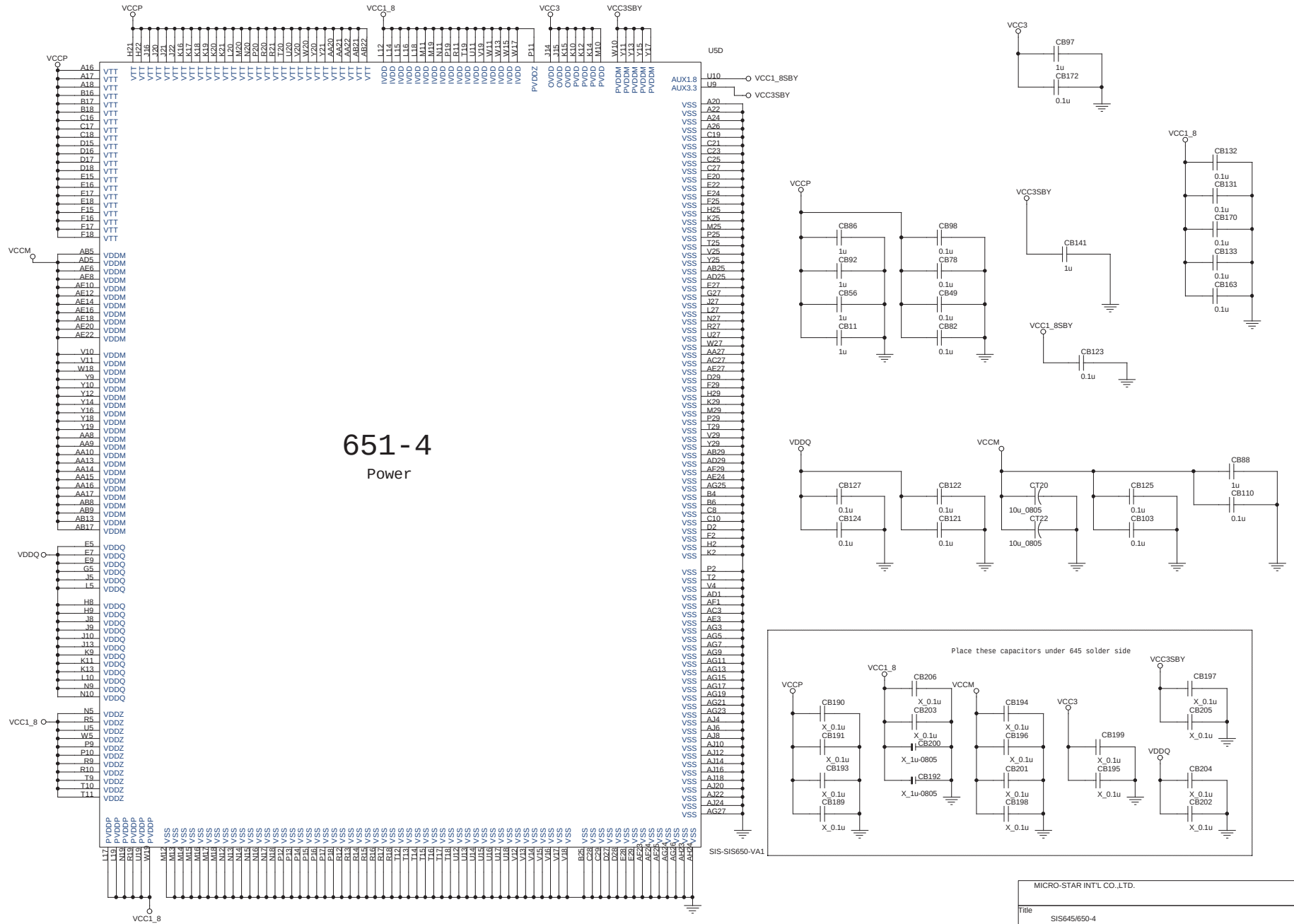
	0	1	Default
DLEN#	enable PLL	disable PLL	0
DRAM_SEL	SDR	DDR	1(DDR)
TRAP#	normal	NB debug mode	0
TRAP1	TV selection, NTSC/PAL(0/1)		0
CSYNC	enable VB		0
RSYNC	enable VGA interface		1
CSYNC	enable game link		0

embedded pull-low
(30-50K Ohm)
yes
yes
yes

for 651 only



651-4 Power



(7.11) RMD[0..63] << RMA[0..14]
(7.11) RMA[0..14] << RDQM[0..7]
(7.11) RDQM[0..7] << RDQS[0..7]

NOTE:

VDDIO IS A TRAP ON THE DIMM
MODULE TO INDICATE:

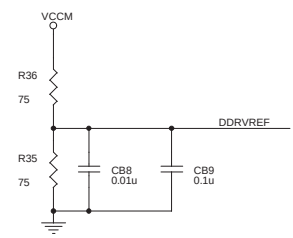
VDDIO	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

MEMORY MUX TABLE:

SR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

VCCM
R69 8.2K

DDRREF GEN. & DECOUPLING



(7.11) RSRAS# << RAS#
(7.11) RSCAS# << CAS#
(7.11) RSW# << WE#

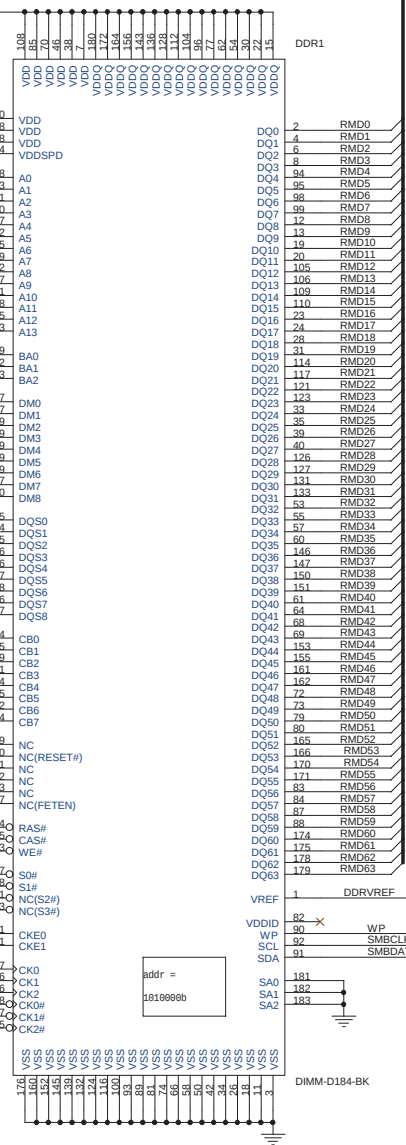
RCS-0
RCS-1

SQ#
SL#
NC(S2#)
NC(S3#)

CKE0
CKE1

DDRCLK1
DDRCLK8
DDRCLK2
DDRCLK-1
DDRCLK-8
DDRCLK-2

(7.11) RCS-[0..3] << RCS-[0..3]
(7) CKE-[0..3] << CKE-[0..3]
(3) DDRCLK-[0..8] << DDRCLK-[0..8]
(3) DDRCLK-[0..8] << DDRCLK-[0..8]

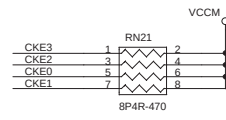


addr =
1810990b

VREF 1 DDRVREF
VDDID 82 WP
SCL 92 SMBCLK
SDA 91 SMBDAT

SA0 181
SA1 182
SA2 183

DIMM-D184-BK



RMD[0..63]
RMA[0..14]
RDQM[0..7]
RDQS[0..7]

VCCM

VCCM
R66 8.2K

(7.11) RSRAS# << RAS#
(7.11) RSCAS# << CAS#
(7.11) RSW# << WE#

RCS-0
RCS-1

SQ#
SL#
NC(S2#)
NC(S3#)

CKE0
CKE1

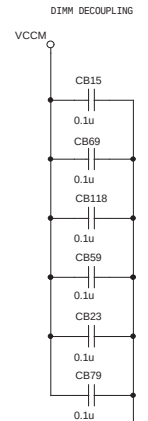
DDRCLK0
DDRCLK7
DDRCLK-0
DDRCLK-7
DDRCLK-3

addr =
18109901b

VREF 1 DDRVREF
VDDID 82 WP
SCL 92 SMBCLK
SDA 91 SMBDAT

SA0 181
SA1 182
SA2 183

DIMM-D184-BK

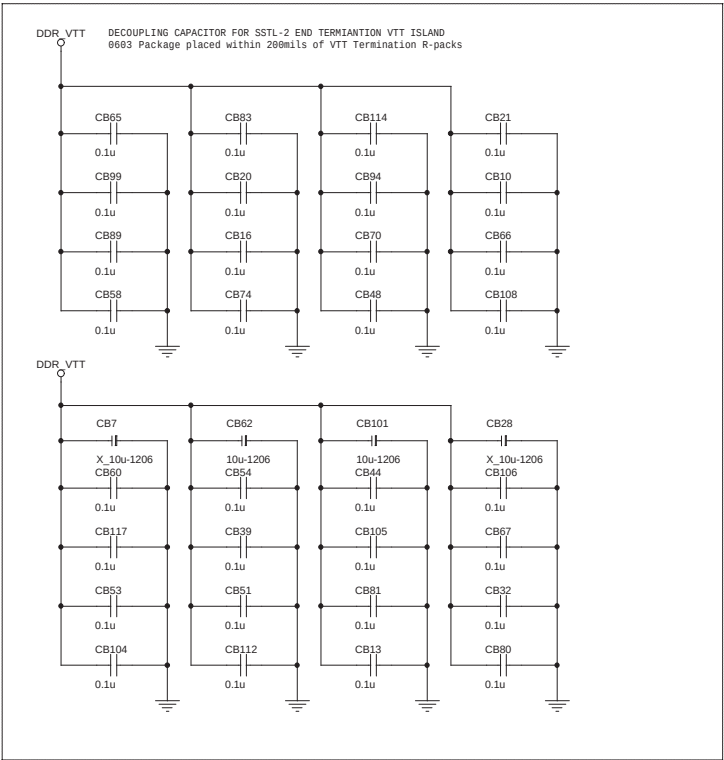
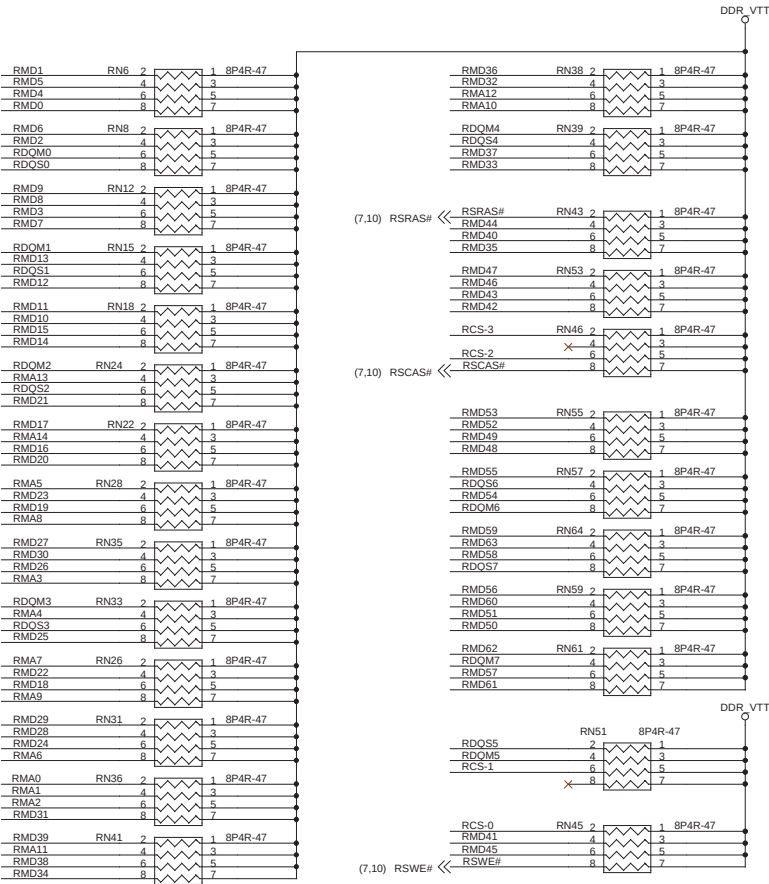


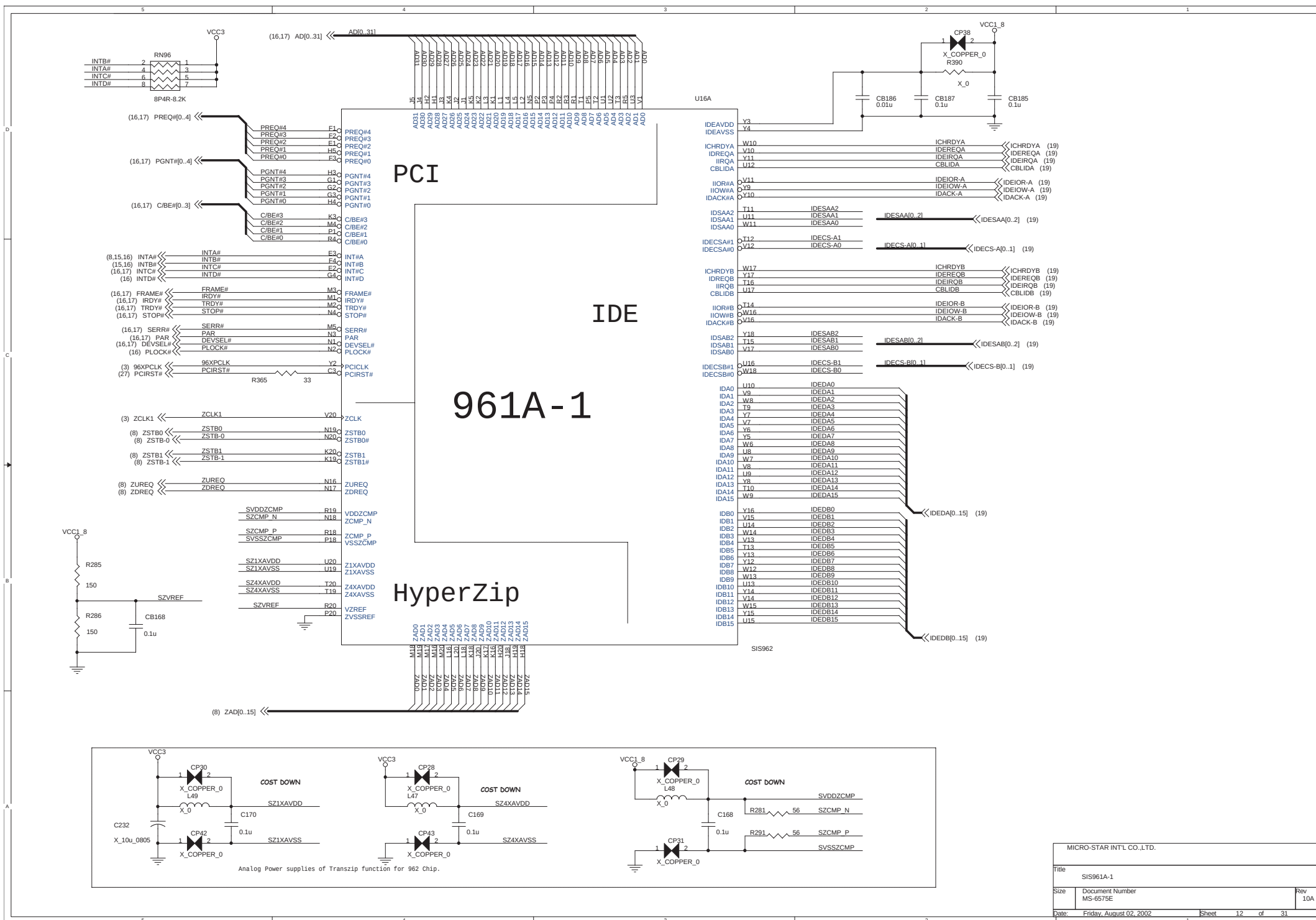
MICRO-STAR INT'L CO.,LTD.		
Title DDR1 & DDR2		
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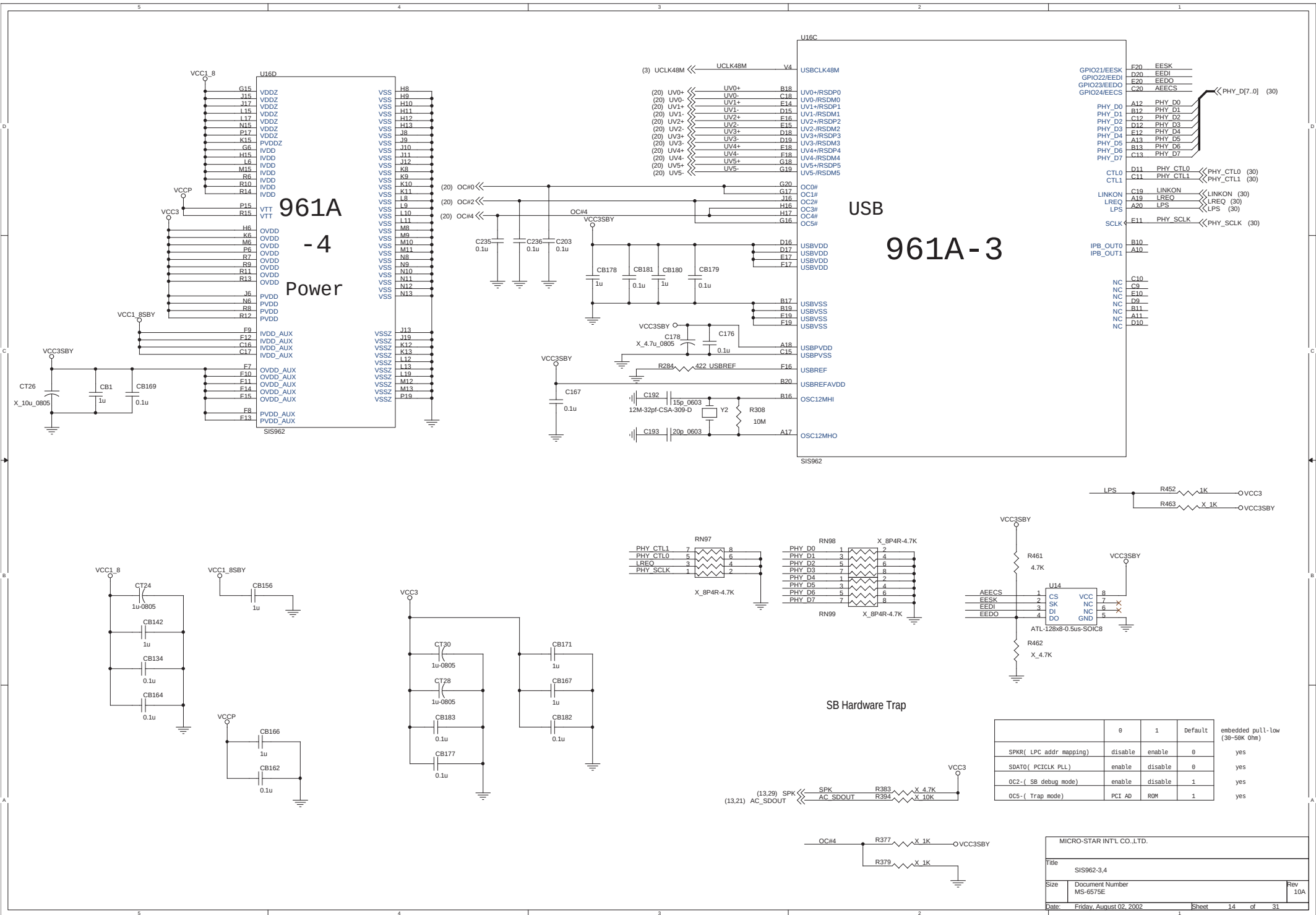
SSTL-2 Termination Resistors



	DDR	DDR	DDR	DDR	DDR
NO/DQM(/DQS)	LV-CMOS	Rs	SSTL-2	Rs	Rtt
NA/Control	LV-CMOS	8/18/-	SSTL-2	18	47
CS	LV-CMOS	8	SSTL-2	8	47
CKE	DD 3.3V		DD 2.5V		

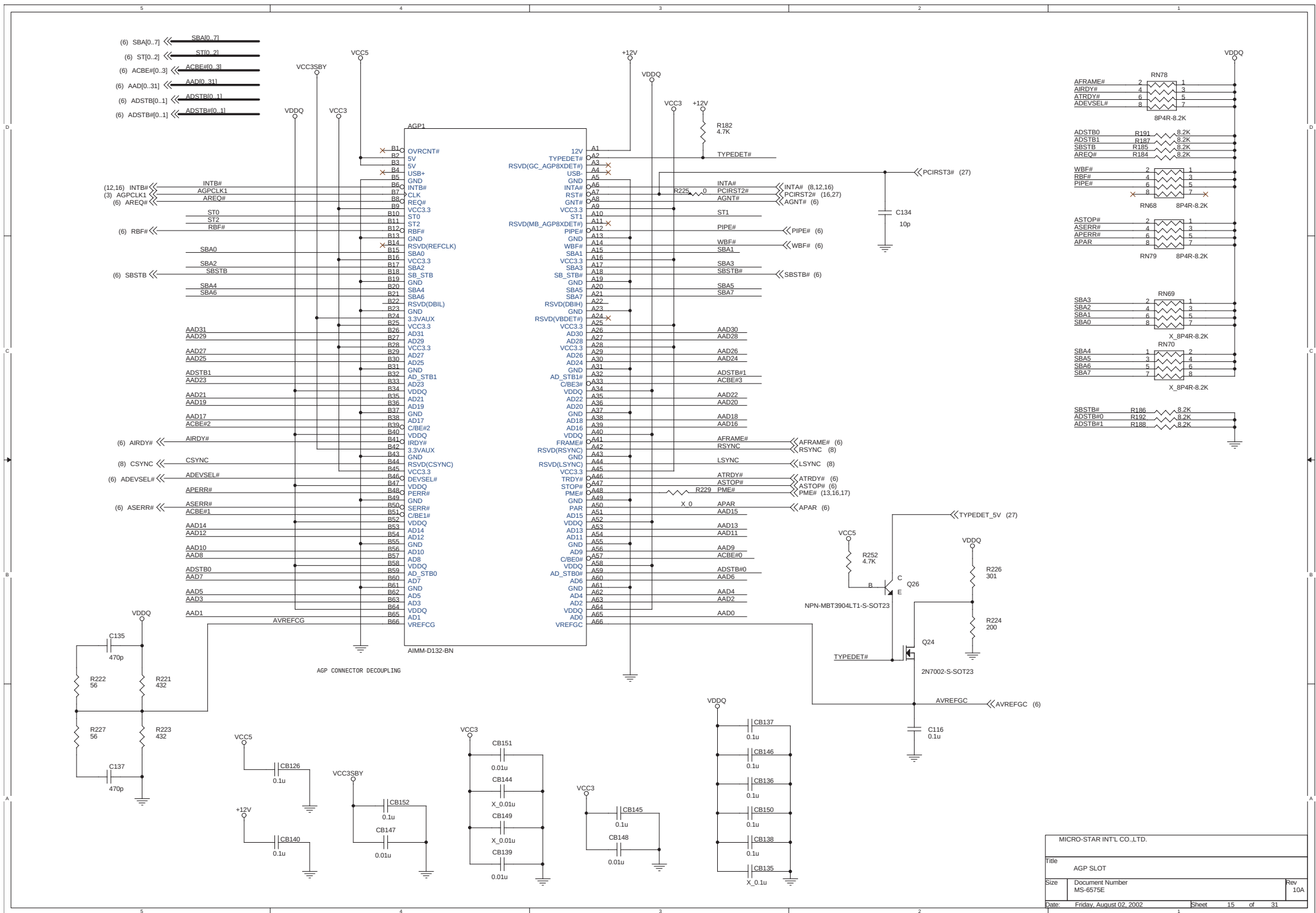




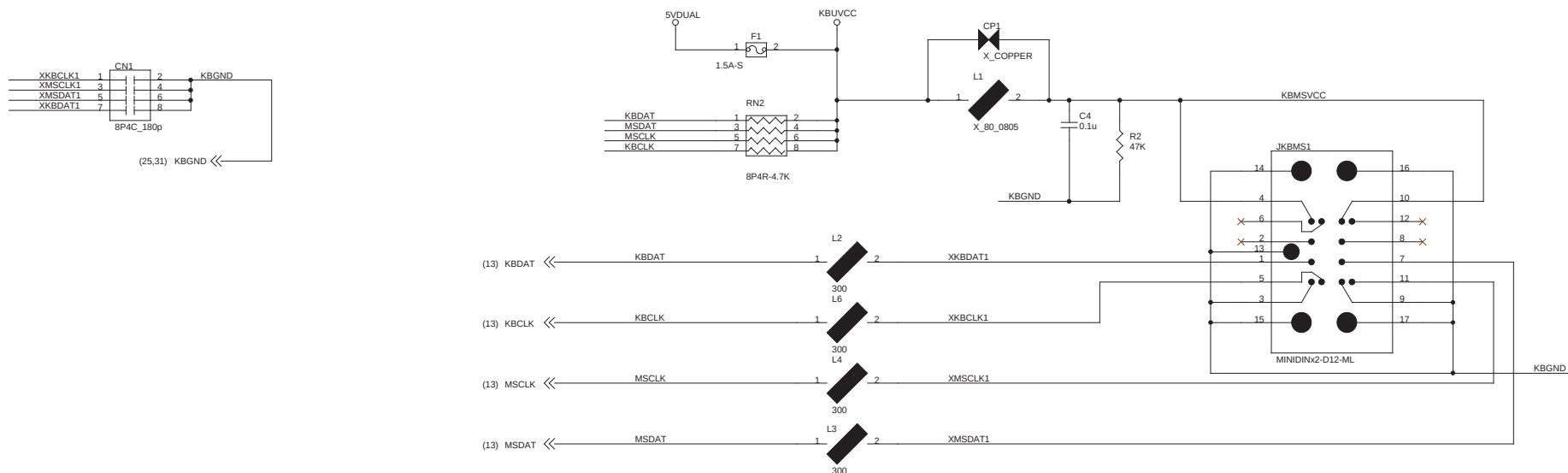


	0	1	Default	embedded pull-low (38-59K Ohm)
SPKR(LPC addr mapping)	disable	enable	0	yes
SDAT0(PCICLK PLL)	enable	disable	0	yes
OC2- (SB debug mode)	enable	disable	1	yes
OC5- (Trap mode)	PCI AD	ROM	1	yes

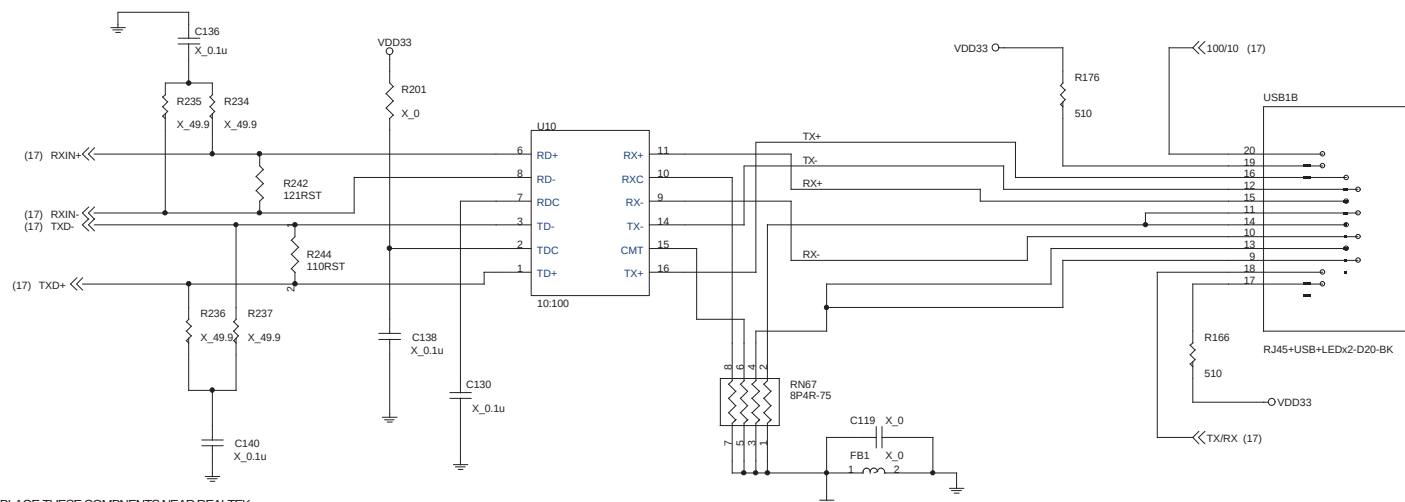
MICRO-STAR INT'L CO.,LTD.			
Title SIS962-3.4			
Size	Document Number MS-6575E	Rev 10A	
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KEYBOARD/MOUSE PORTS

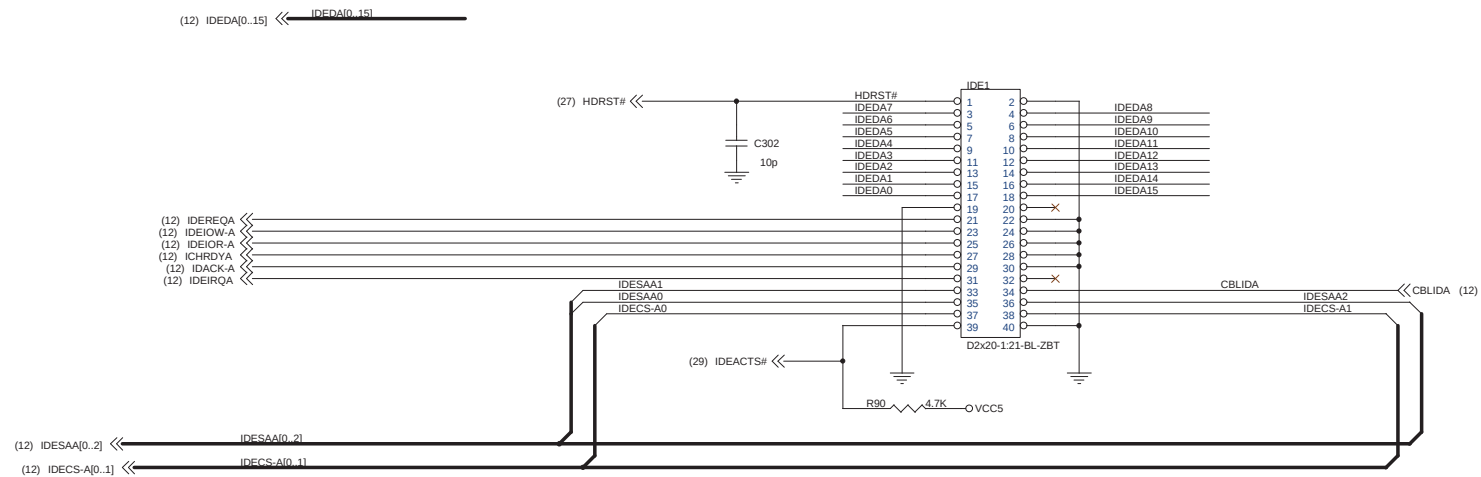


RJ45 CONNECTOR



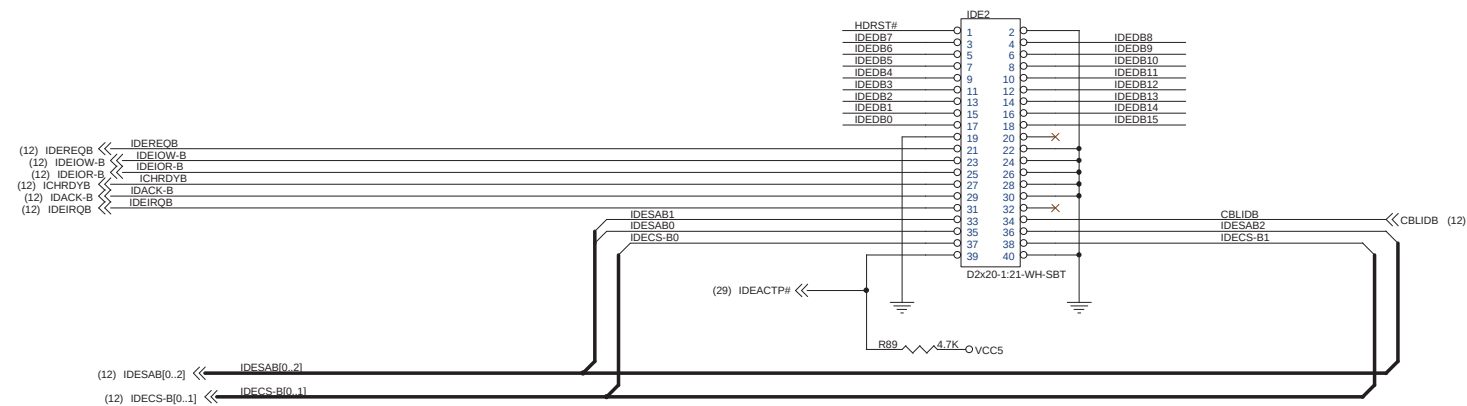
PLACE THESE COMPONENTS NEAR REALTEK 8100BL

MICRO-STAR INT'L CO.,LTD.			
Title	RJ45 & PS/2		
Size	Document Number	Rev	
	MS-6575E	10A	
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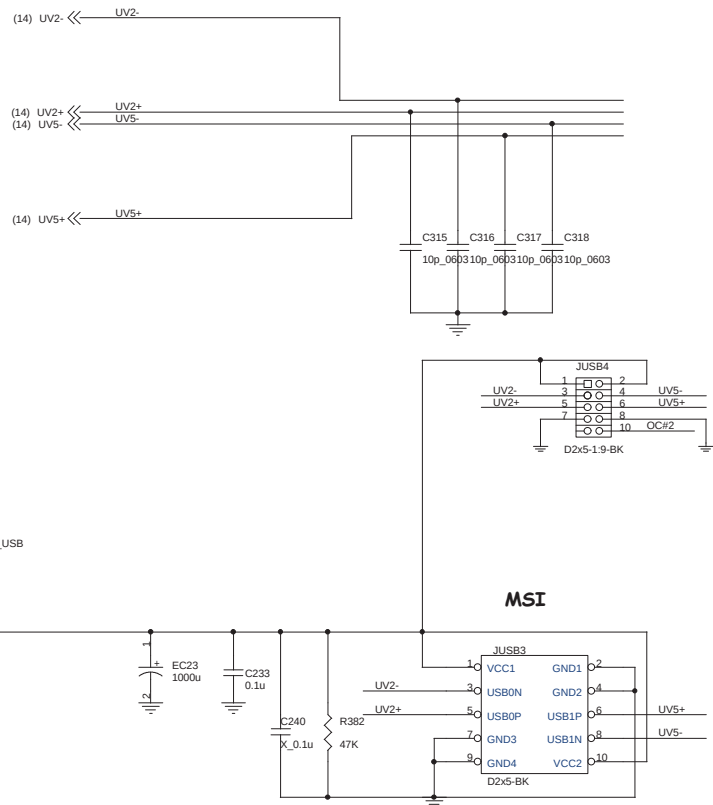


(12) IDEDB[0..15] << IDEDB[0..15]

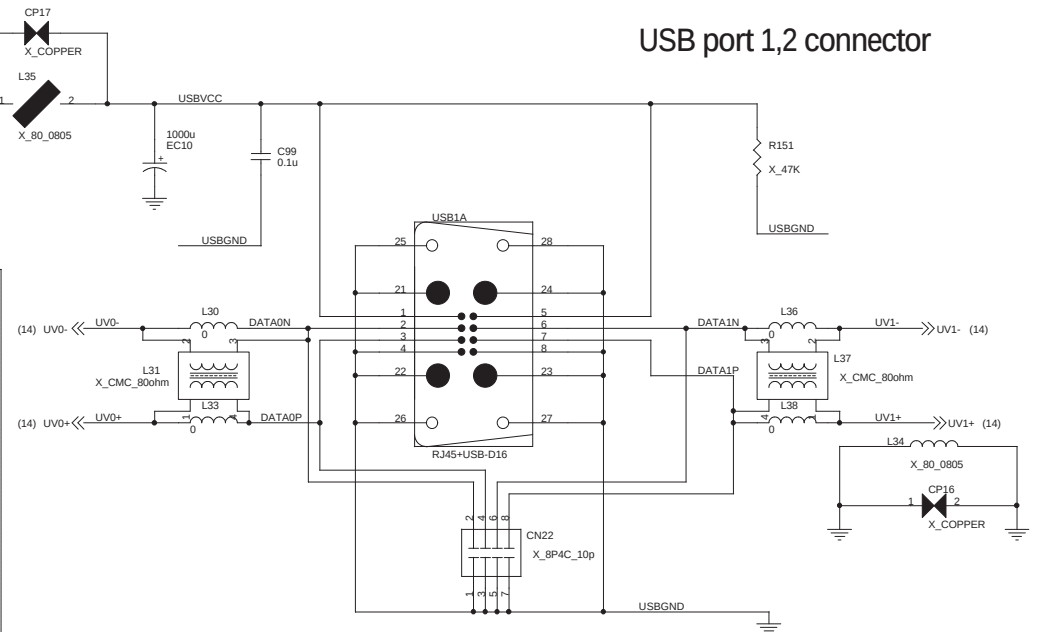
- NOTE
1. RN80/81/82/83/88/89/90/92 R275/280/304/312/315/326 NEAR IDE CONNECTOR
 2. OTHERS NEAR SIS961A/B



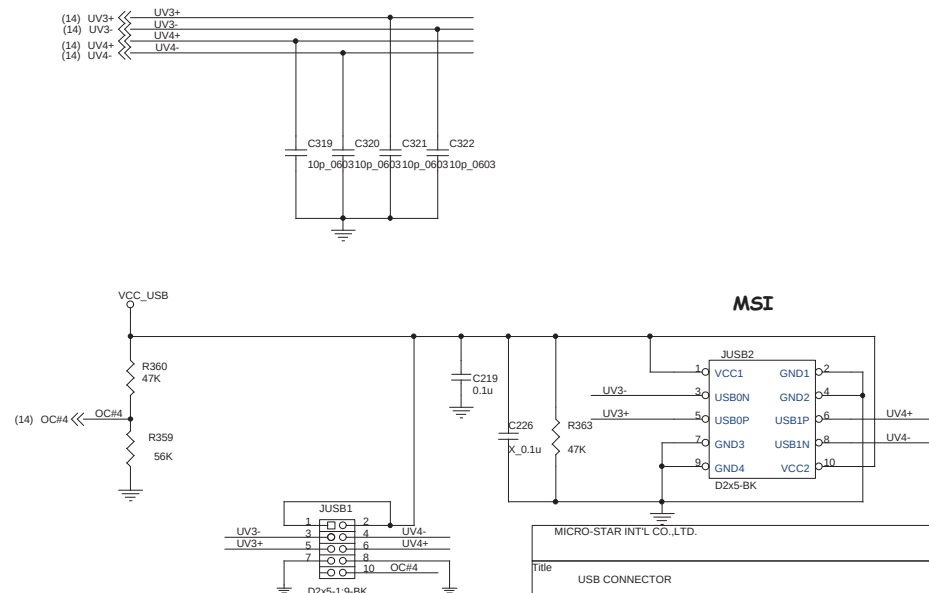
USB port 2,5 connector



USB port 1,2 connector



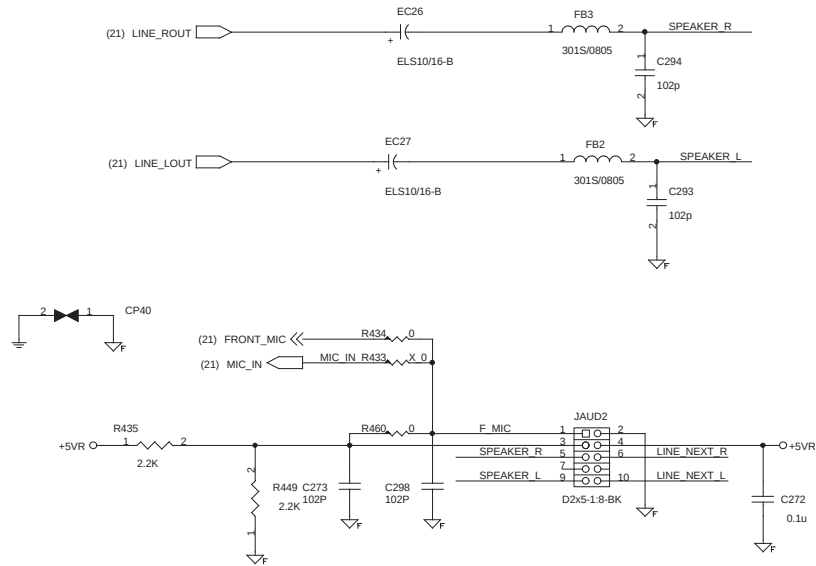
USB port 3,4 connector



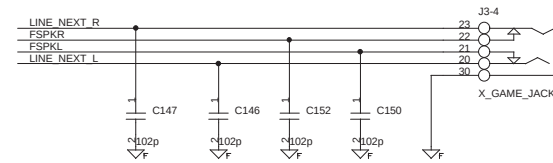
MICRO-STAR INT'L CO.,LTD.

Title		
USB CONNECTOR		
Size	Document Number	Rev
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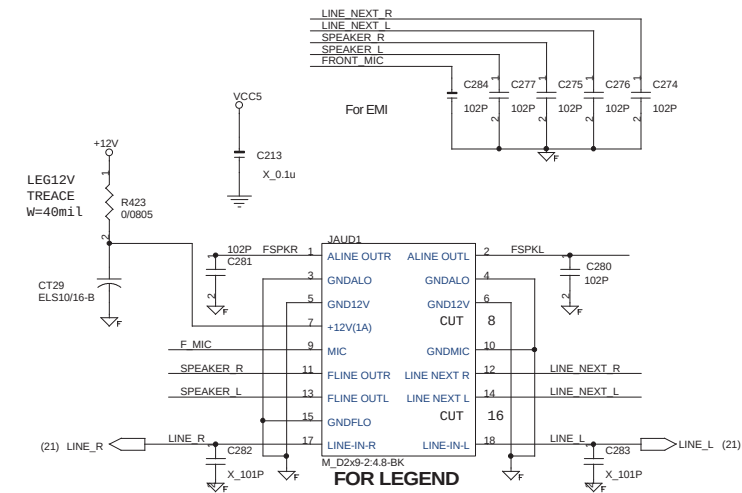
SPEAKER OUT CIRCUIT



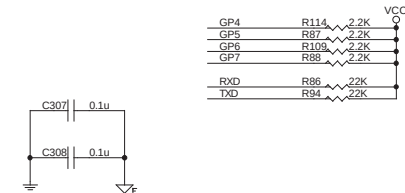
SPEAKER OUT JACK



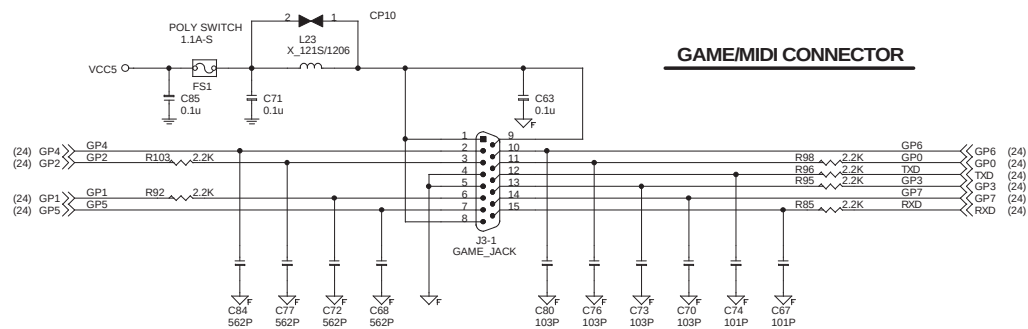
FOR MSI INTERNAL HEADER



FOR LEGEND

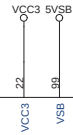
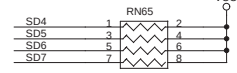
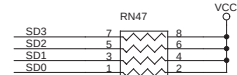
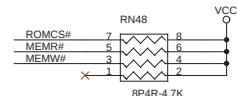
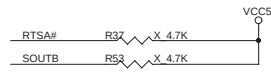


GAME/MIDI CONNECTOR

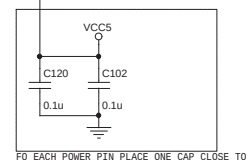
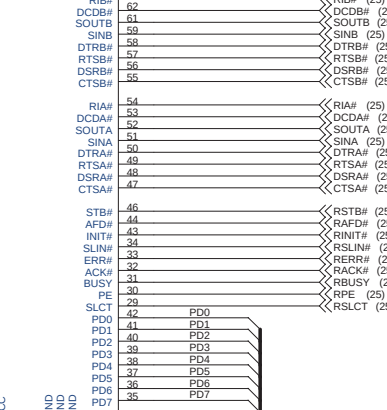


RTSA#	L: CFAD=2E	H: CFAD=4E
SOUTB	L: 24MHZ	H: 48MHZ

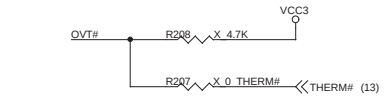
STRAPS



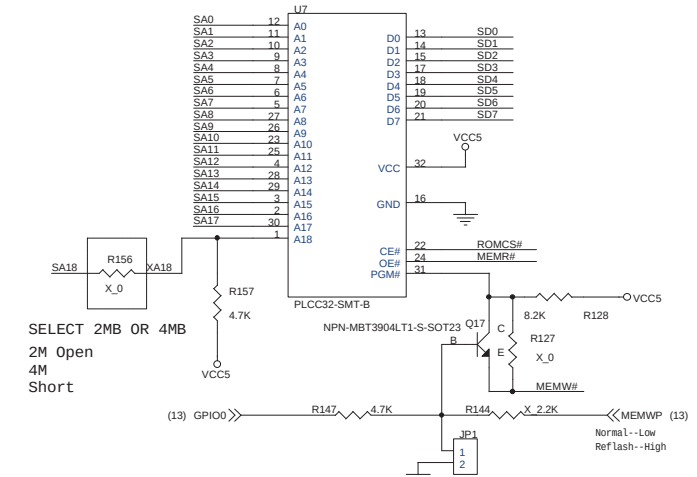
W83697HF



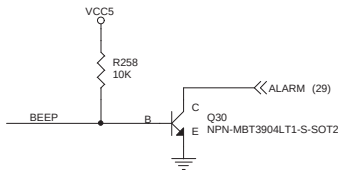
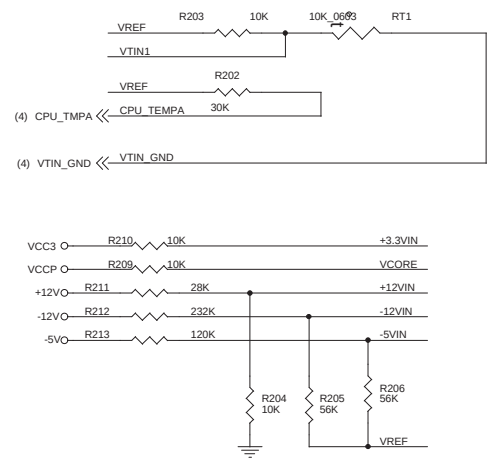
FO EACH POWER PIN PLACE ONE CAP CLOSE TO



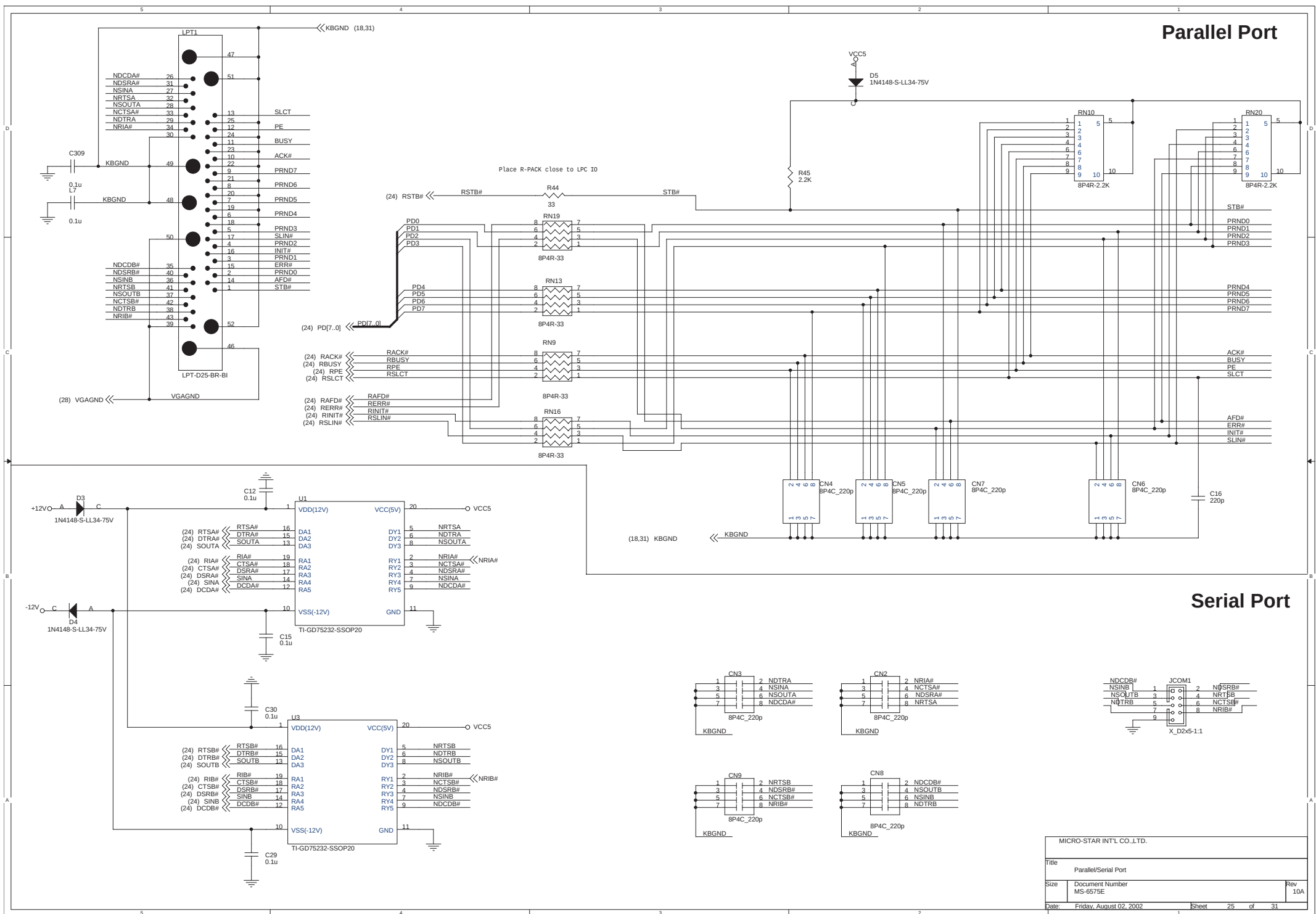
Flash Rom

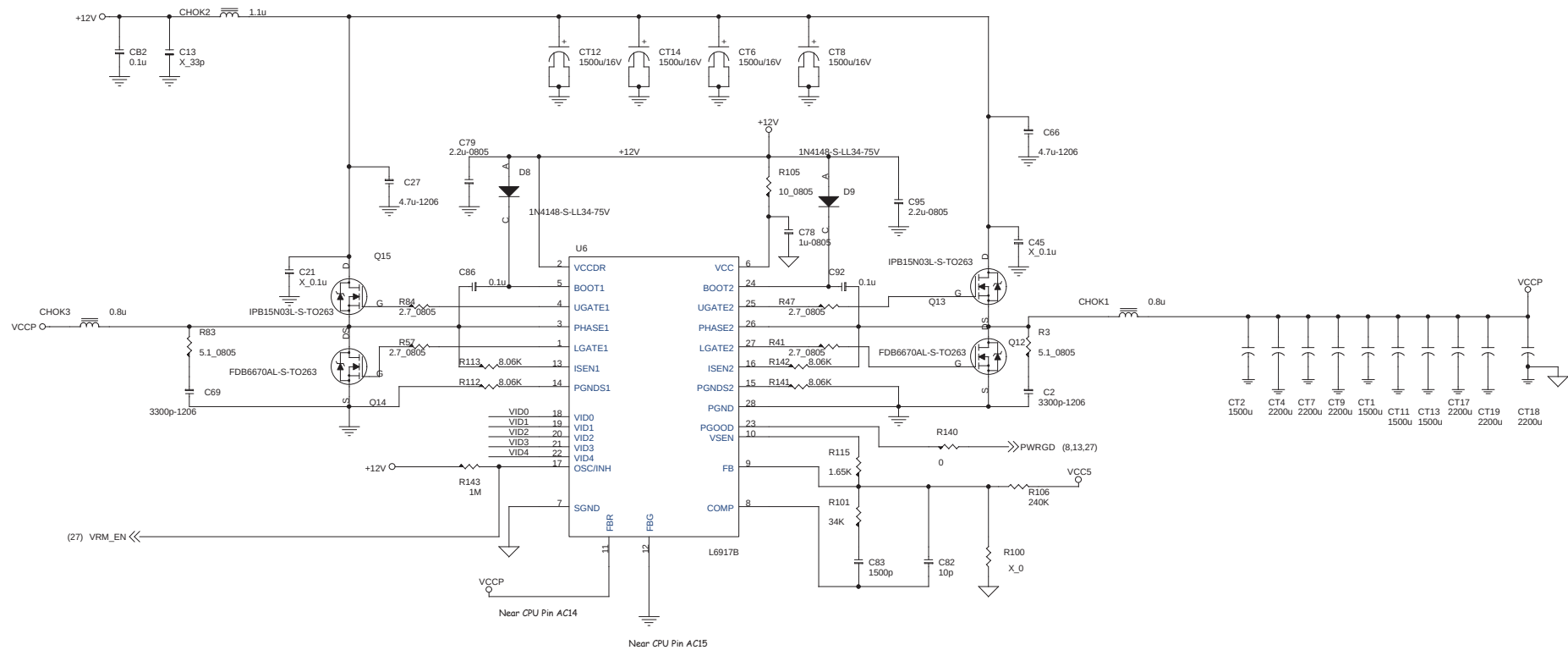


Hardware Monitor

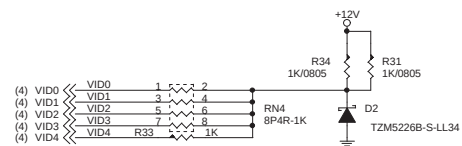


MICRO-STAR INT'L CO.,LTD.		
Title LPC I/O(W83697HF)		
Size	Document Number MS-6575E	Rev 10A
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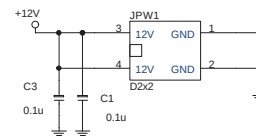




VID PULL-UP RESISTORS



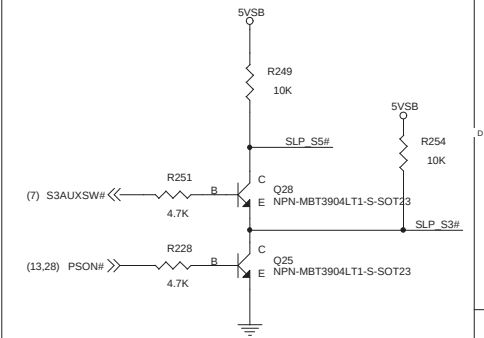
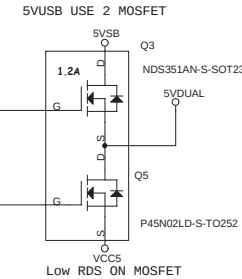
ATX12V POWER CONNECTOR



MICRO-STAR INT'L CO.,LTD.		
Title	VRM 9.0	
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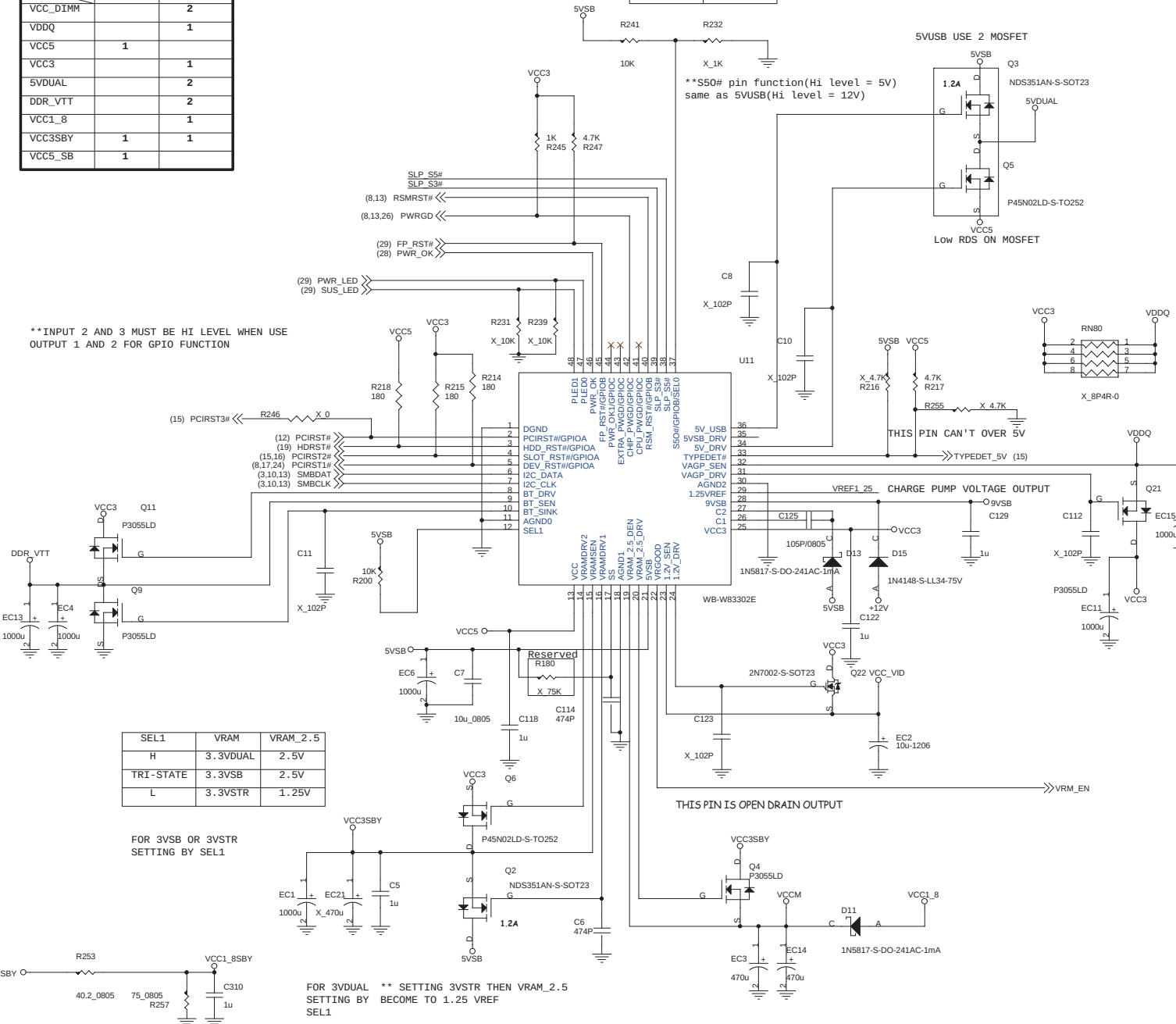
POWER Bulk Decuping		
	470UF	1000UF
VCC_DIMM		2
VDDQ		1
VCC5	1	
VCC3		1
5VDUAL		2
DDR_VTT		2
VCC1_B		1
VCC3SBY	1	1
VCC5_SB	1	

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET



	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION



SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

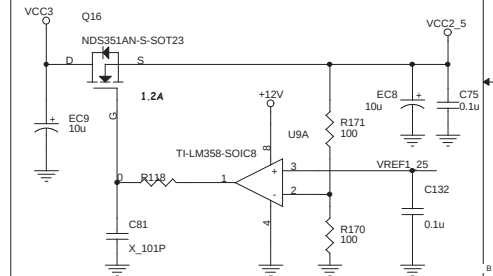
FOR 3VSB OR 3VSTR
SETTING BY SEL1

```

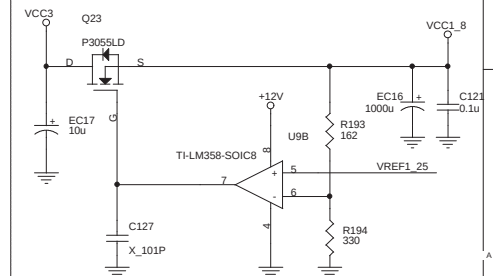
FOR 3VDUAL  ** SETTING 3VSTR THEN VRAM_2.5
SETTING BY  BECOME TO 1.25 VREF
SEL1

```

2.5V POWER TRANSLATOR

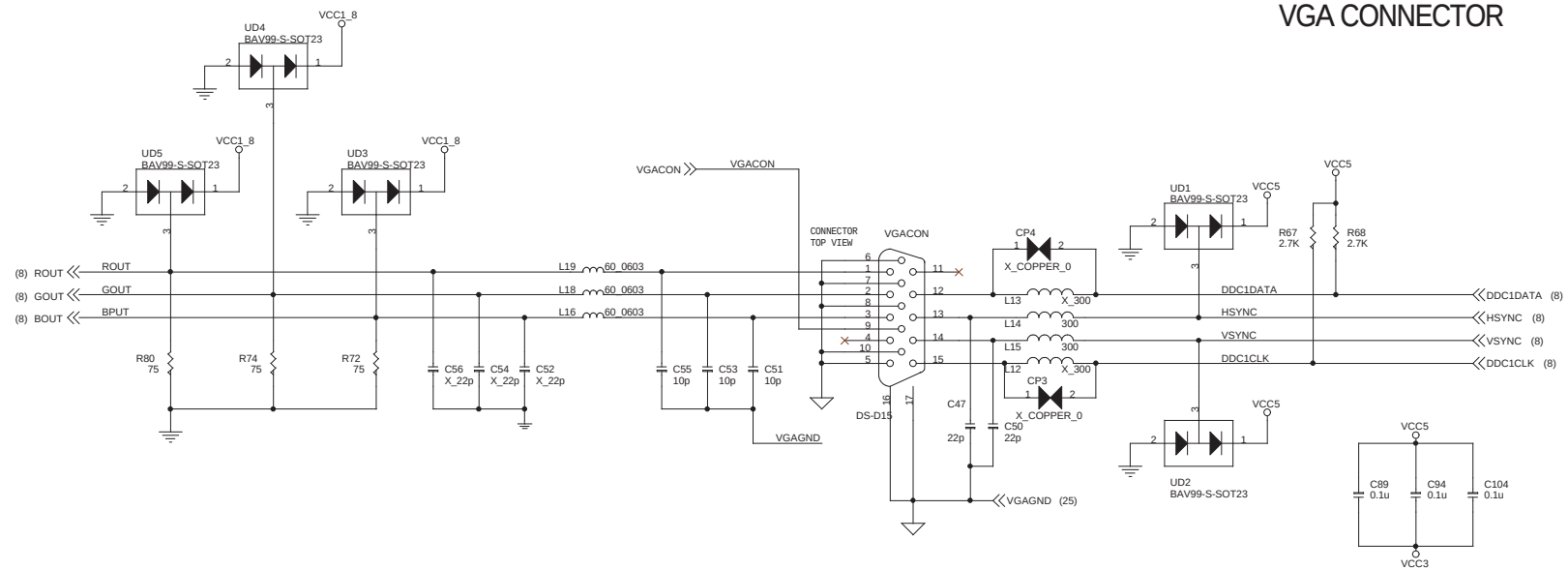
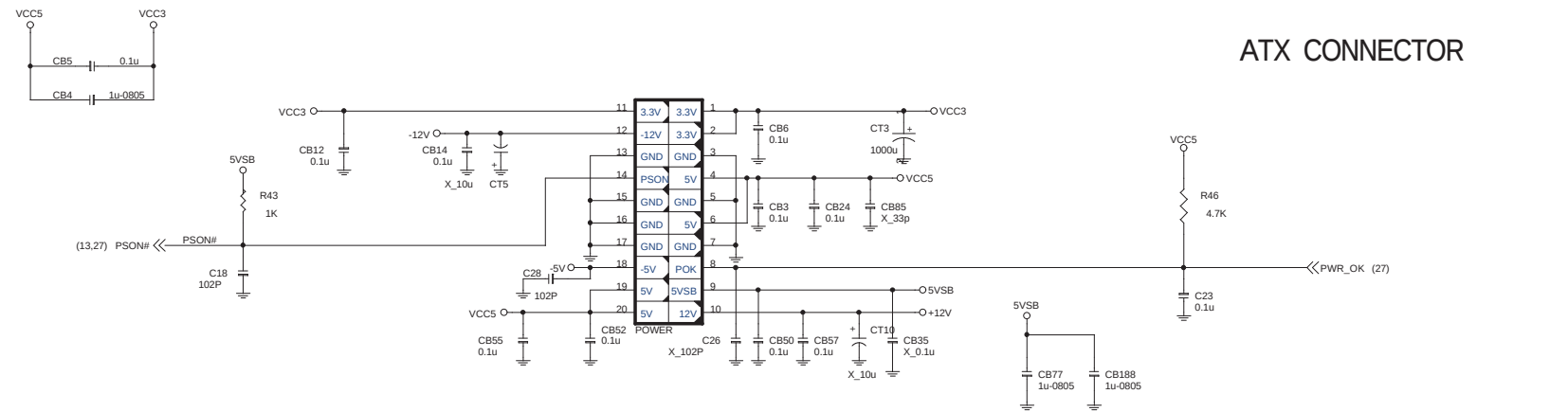


1.8V POWER TRANSLATOR

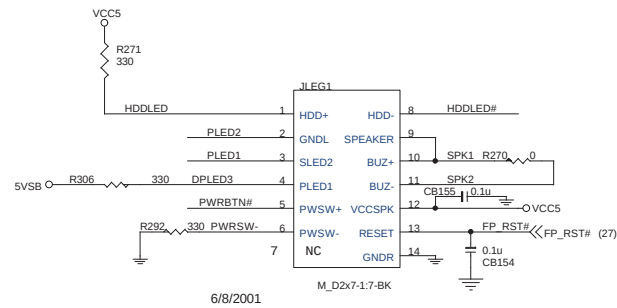
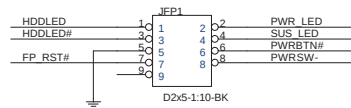


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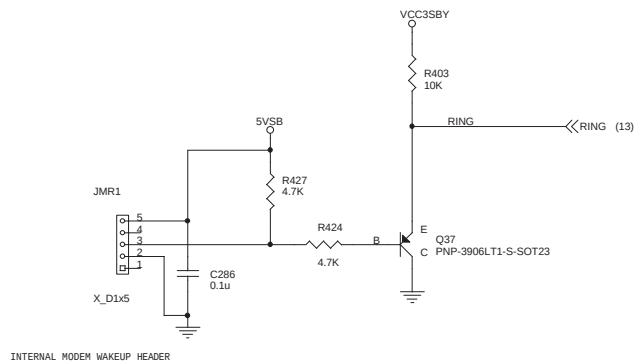


LEGEND FRONT PANEL-M

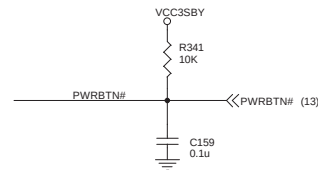
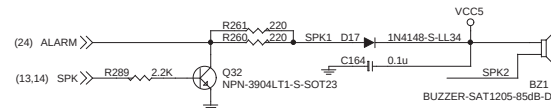
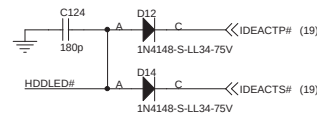


6/8/2001

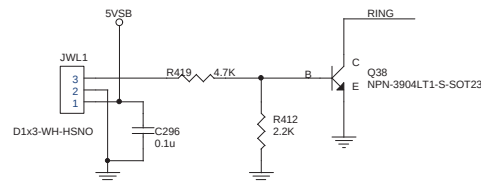
Wake by Modem



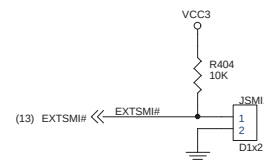
INTERNAL MODEM WAKEUP HEADER



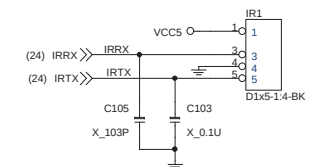
Wake by LAN



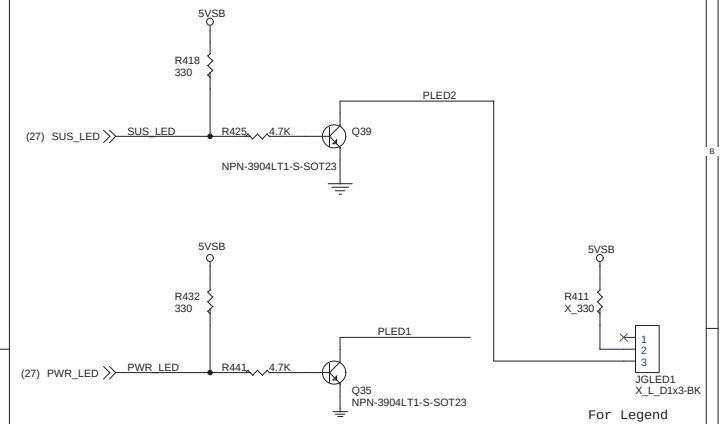
Sleep Button



IR HEADER

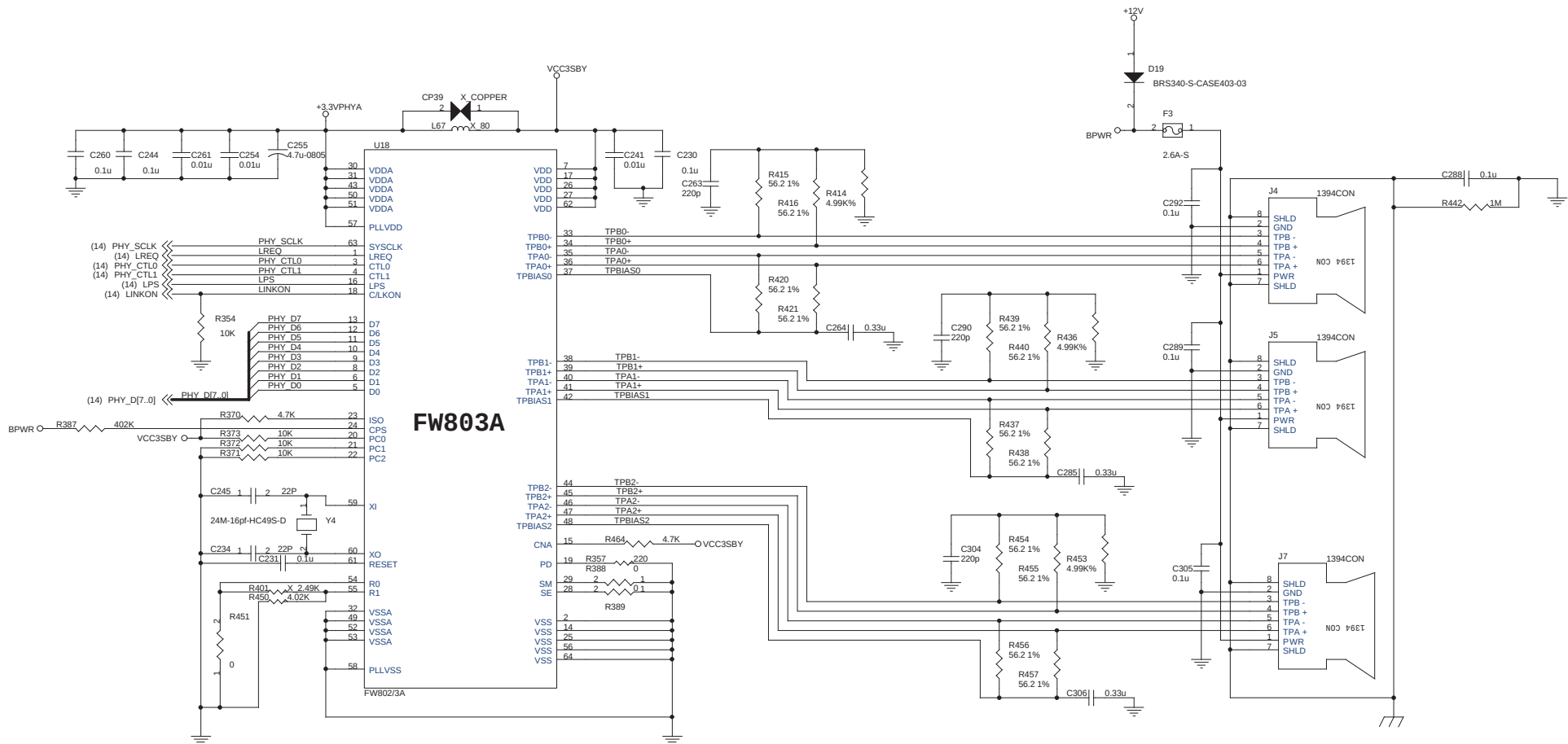


Dual Color LED Block



For Legend

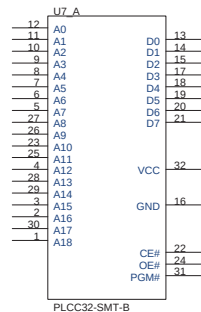
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JBAT1 Clear CMOS		
1-2	Normal	★
2-3	Clear CMOS	

JBAT1(1-2)
YJUMPER-MG

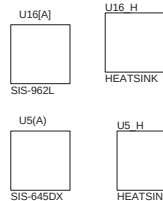
BAT SOCKET



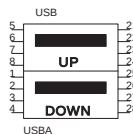
LEGEND AUDIO



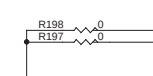
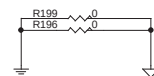
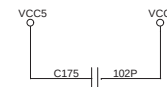
INTEL AUDIO



BIOS WRITE PROTECT



High Freq. return current decoupling



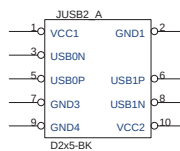
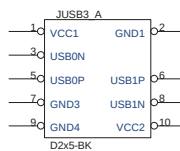
RTL8801

FW803A

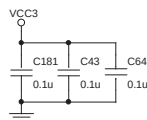
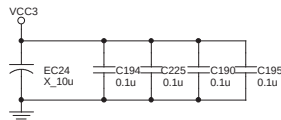
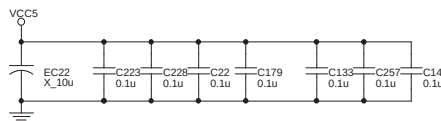
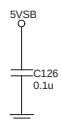
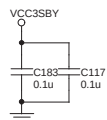
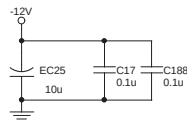
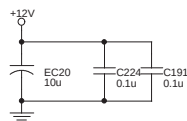
MS6575E PCB



C231(4) 499KST



System Decoupling Capacitors



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