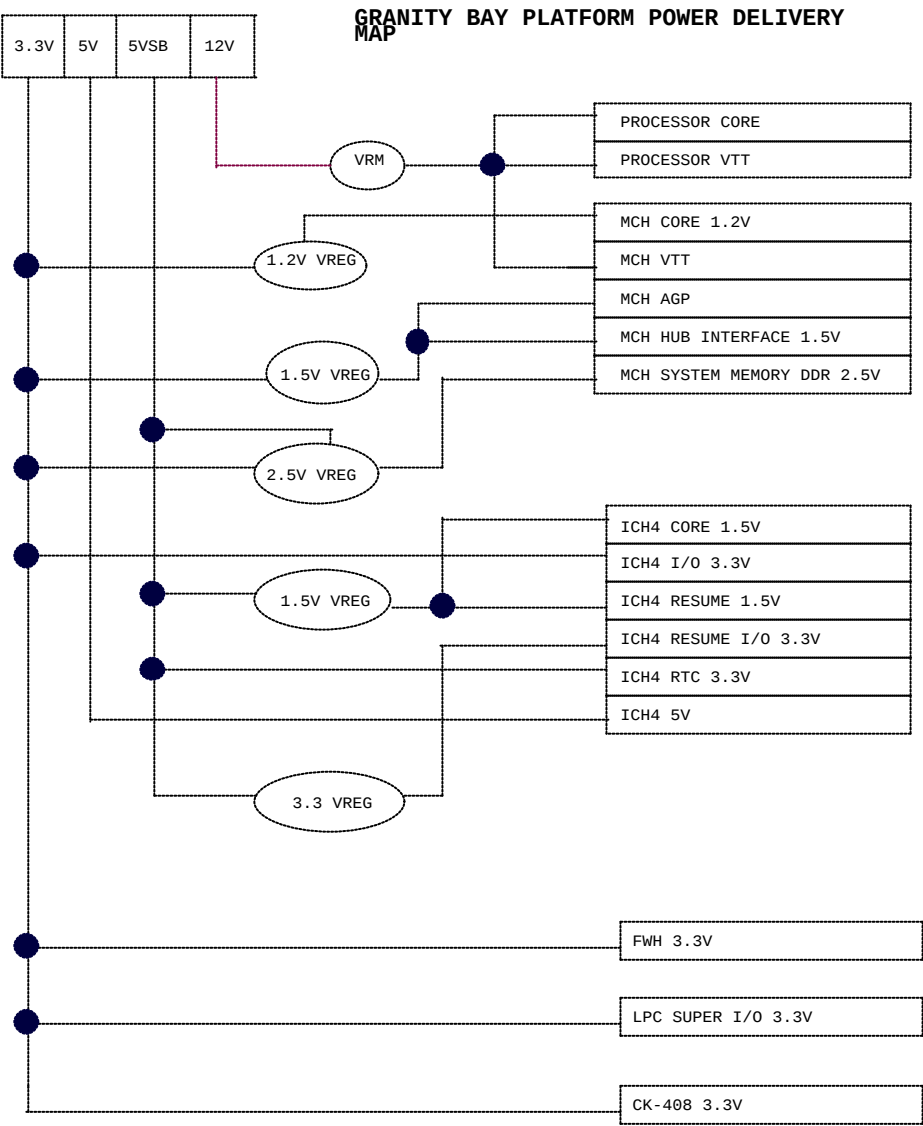
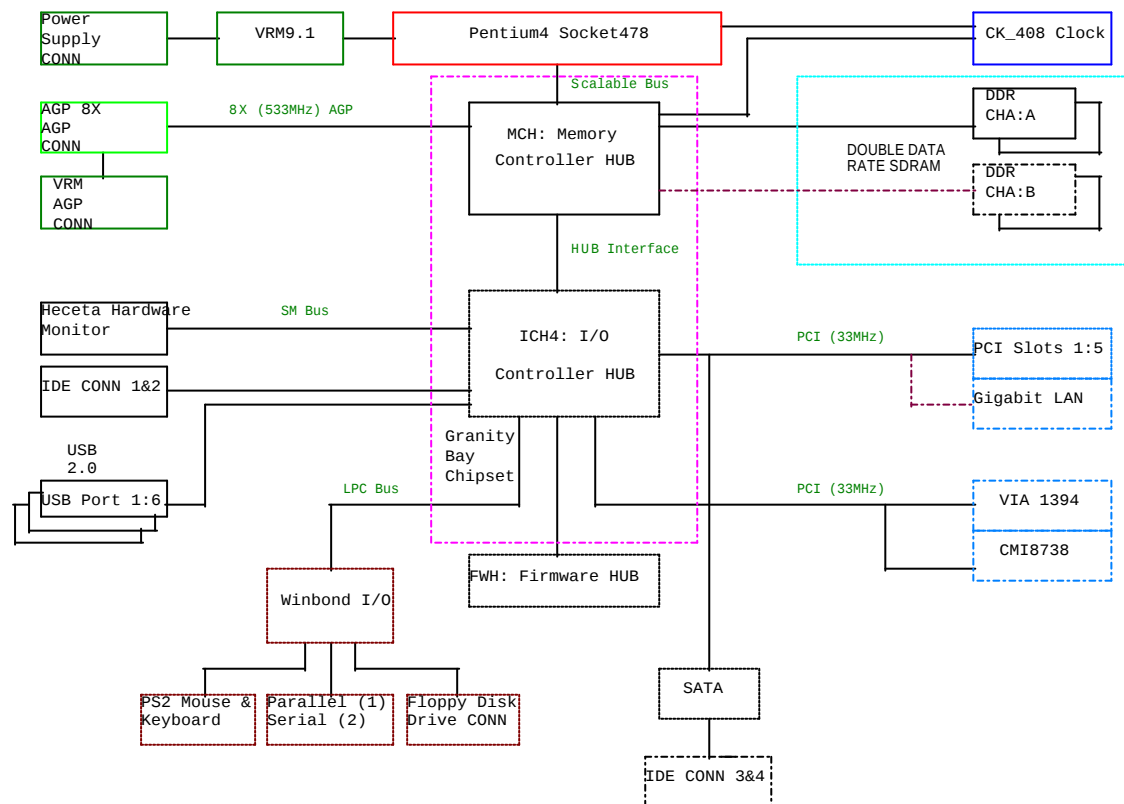


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Preliminary Spec

* Intel Granite Bay Chipset / ICH4

* Supporting Northwood 478 CPUs

* 6 Layer ATX For Factor

* ITP Connector on board

* 4 DDR unbuffered DIMMs (2 Channel)

* Universal 8X AGP/1.5V Keyed

* USB 2.0

* 4 master, 1 slave PCI slots

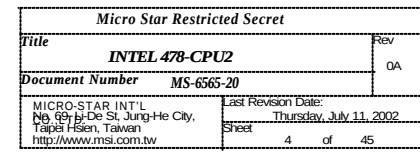
* Gigabit Lan Kenai-32 (82540EM)/ LAVON Dual Layout.

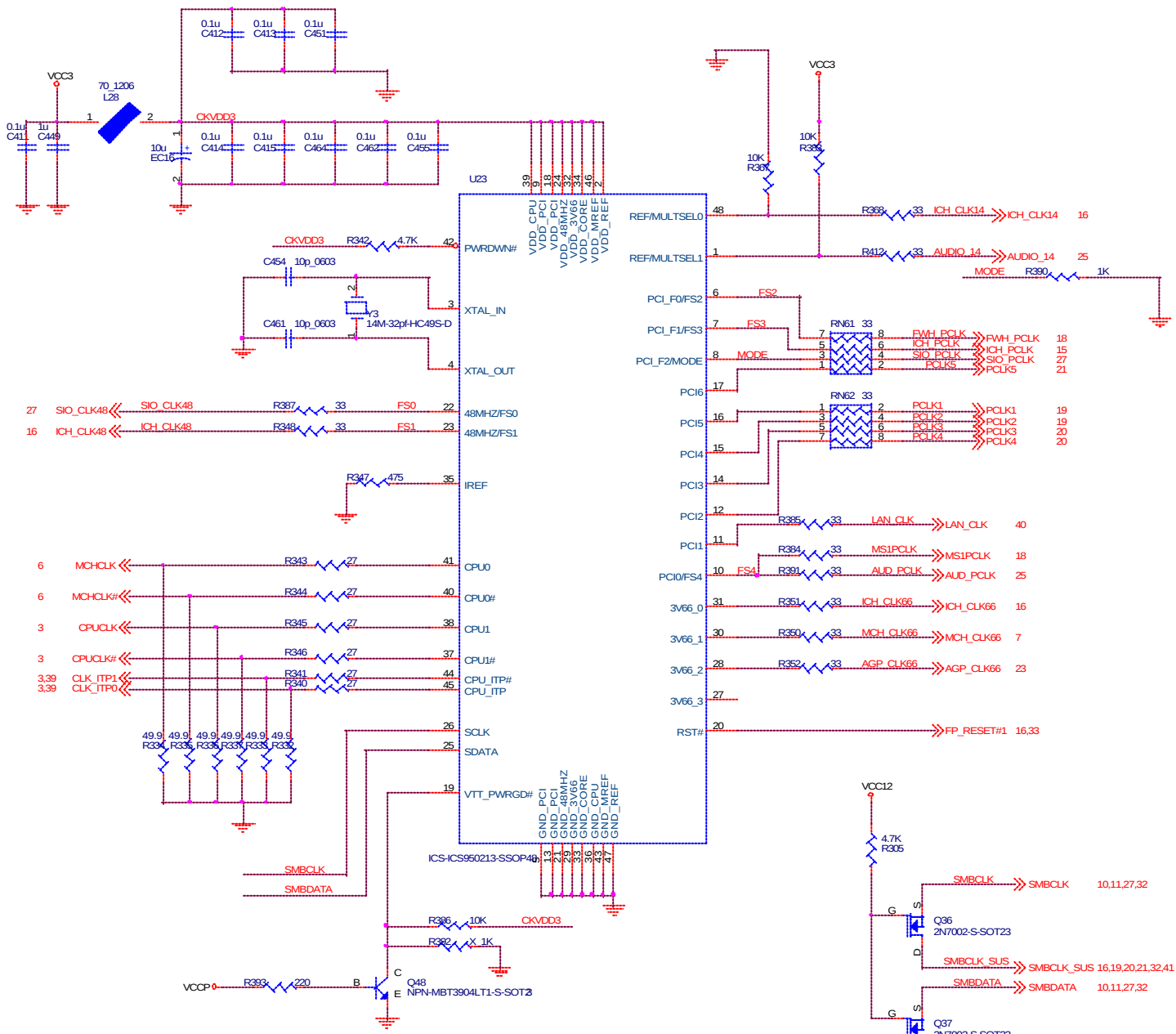
* S-ATA on board

HW AUDIO
CMI8738

VIA 1394

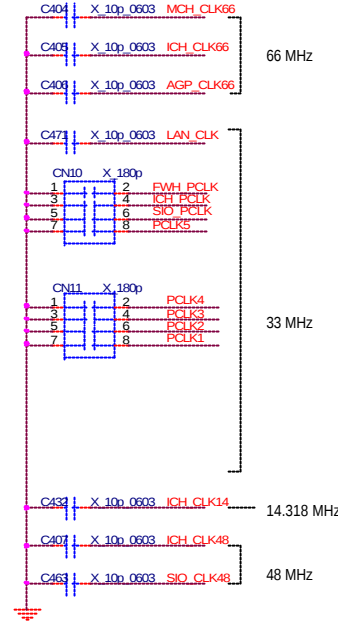
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Title	BLOCK DIAGRAM	Rev 0A
Document Number	MS-6565-20	
MICRO-STAR INT'L No. 65, De St. Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, June 19, 2002
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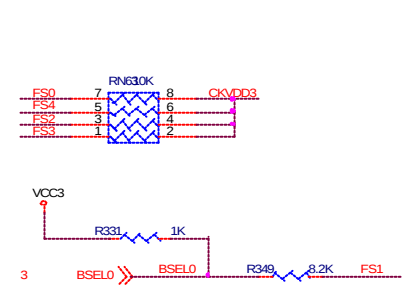


Pull-Down Capacitors

VERY CLOSE CLOCK GENERATOR.

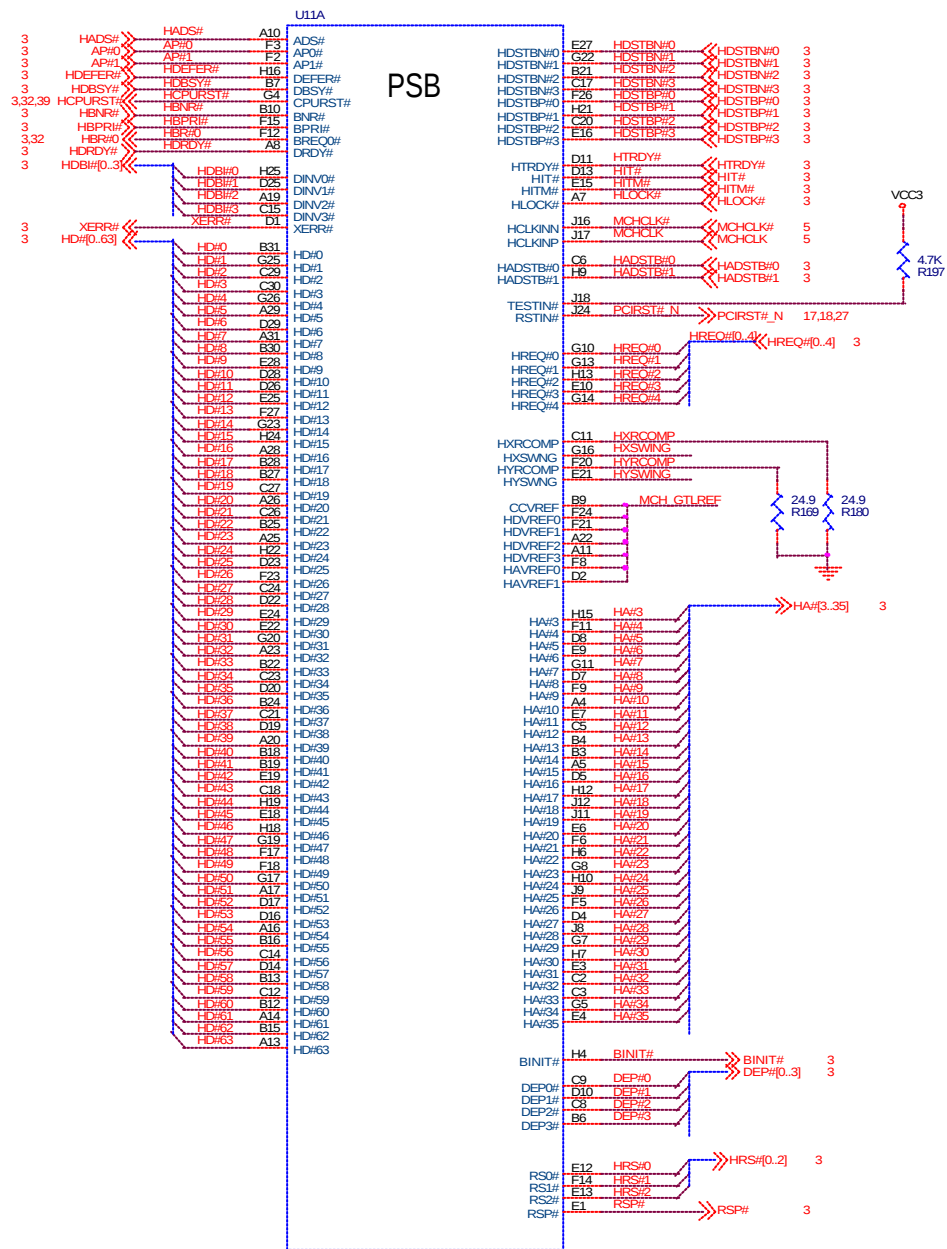


CLOCK STRAPPING.



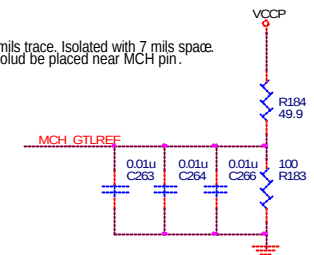
CPU Freq.	FS0	FS1	CPU Freq.	JP4
400MHz	1	0	400MHz	2-3
533MHz	1	1	533MHz	1
		By CPU	1-2	

Micro Star Restricted Secret			
Title	CLOCK GENERATOR		
Document Number	MS-6565-20		
MICRO-STAR INT'L No. 69, Ji-De St. Jung-Hsi City, Taippei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 5 of 45	

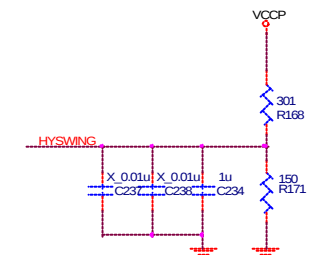
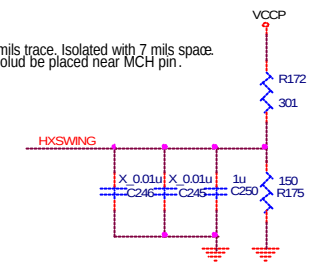


MCH Reference Voltage

Use 10 mils trace. Isolated with 7 mils space.
Caps should be placed near MCH pin.

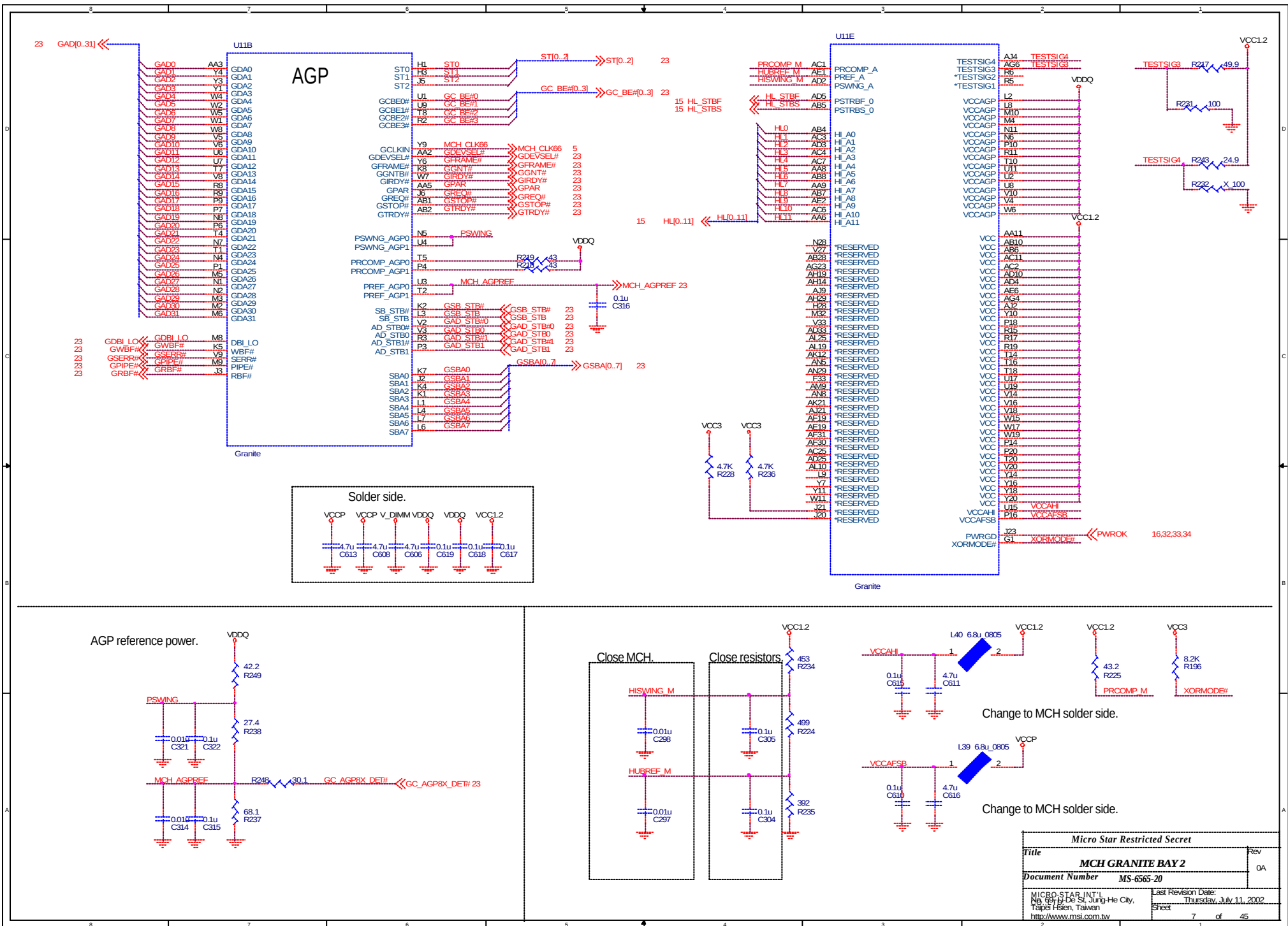


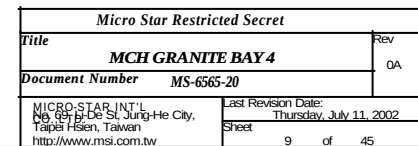
Use 10 mils trace. Isolated with 7 mils space.
Caps should be placed near MCH pin.

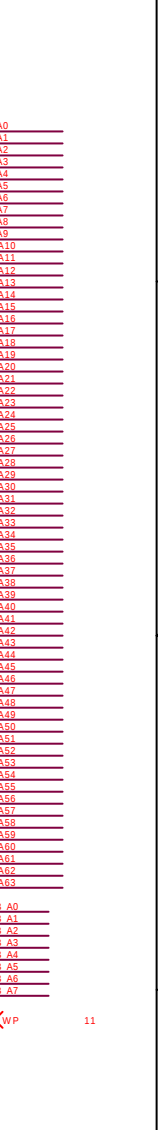
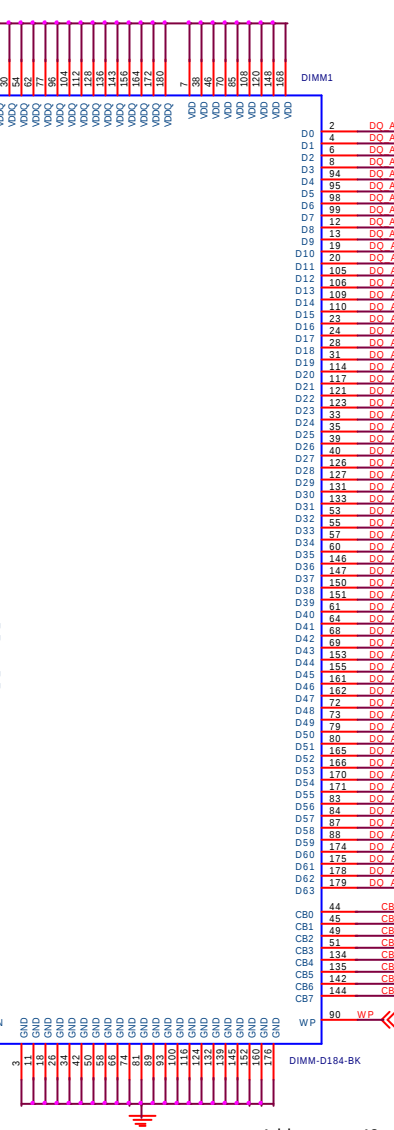
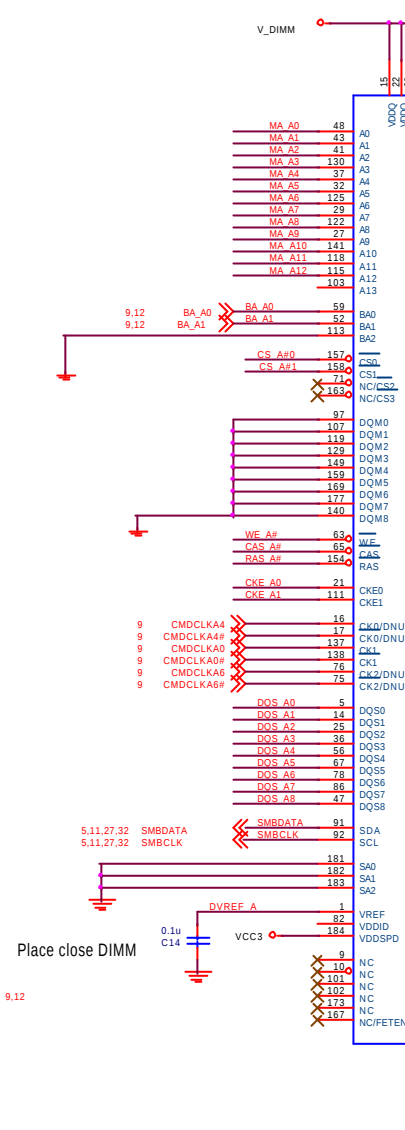
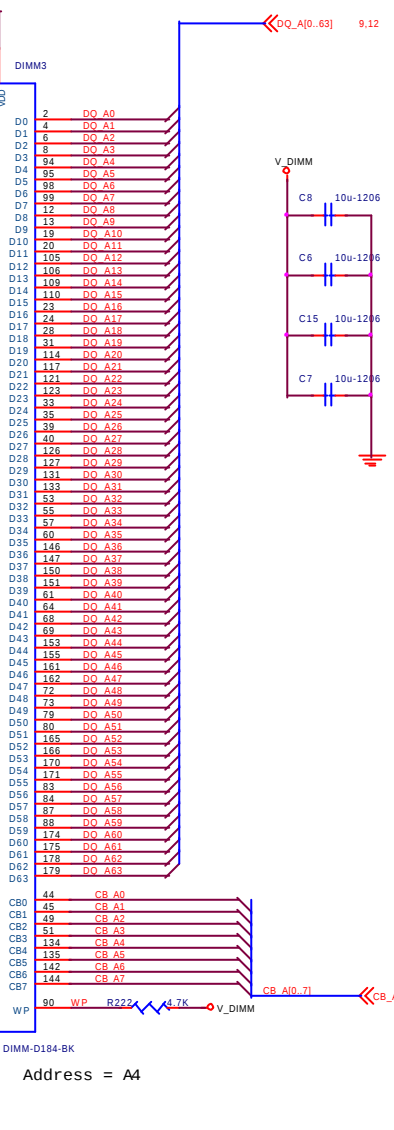
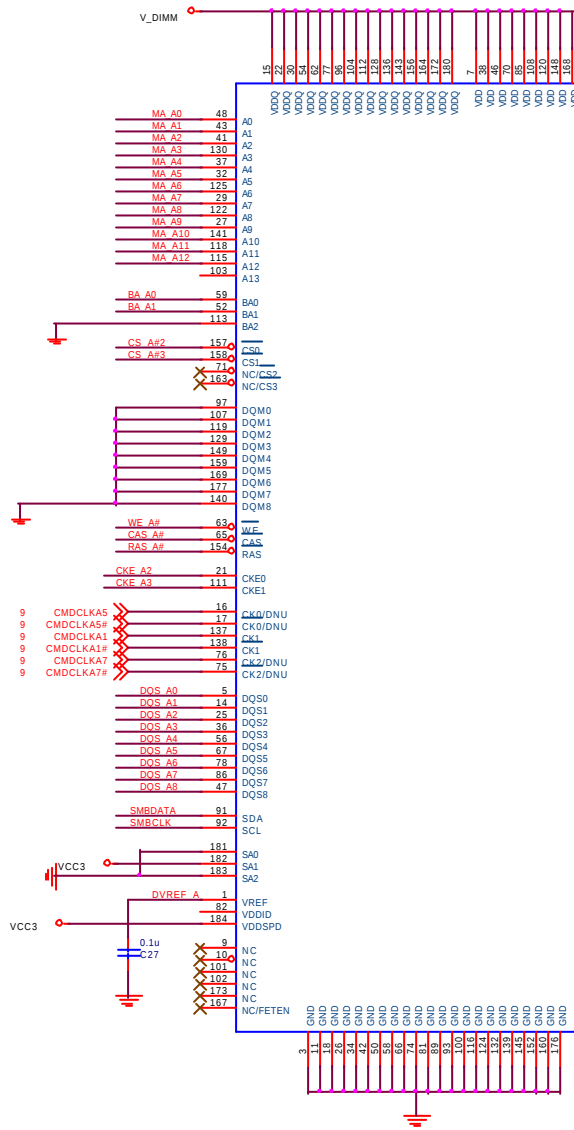


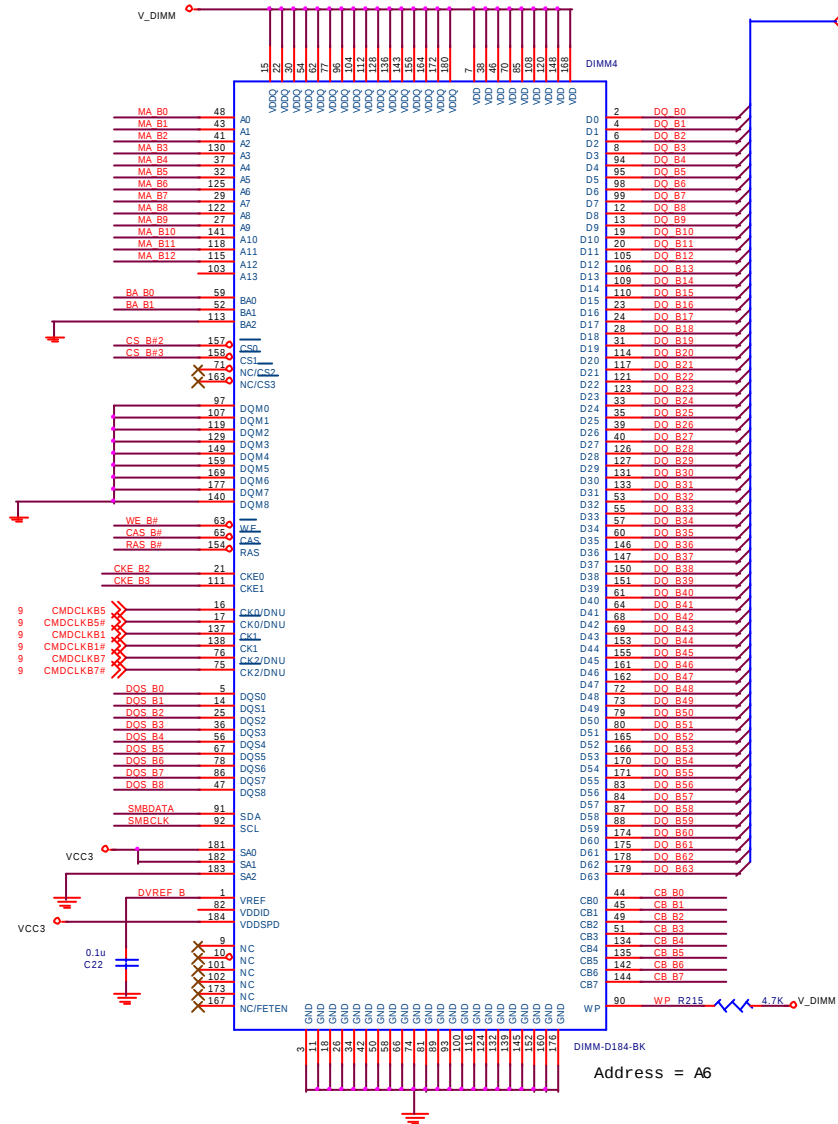
Micro Star Restricted Secret

Title	REV
MCH GRANITE CONTROLLER	0A
Document Number	MS-6565-20
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, July 11, 2002 Sheet 6 of 45







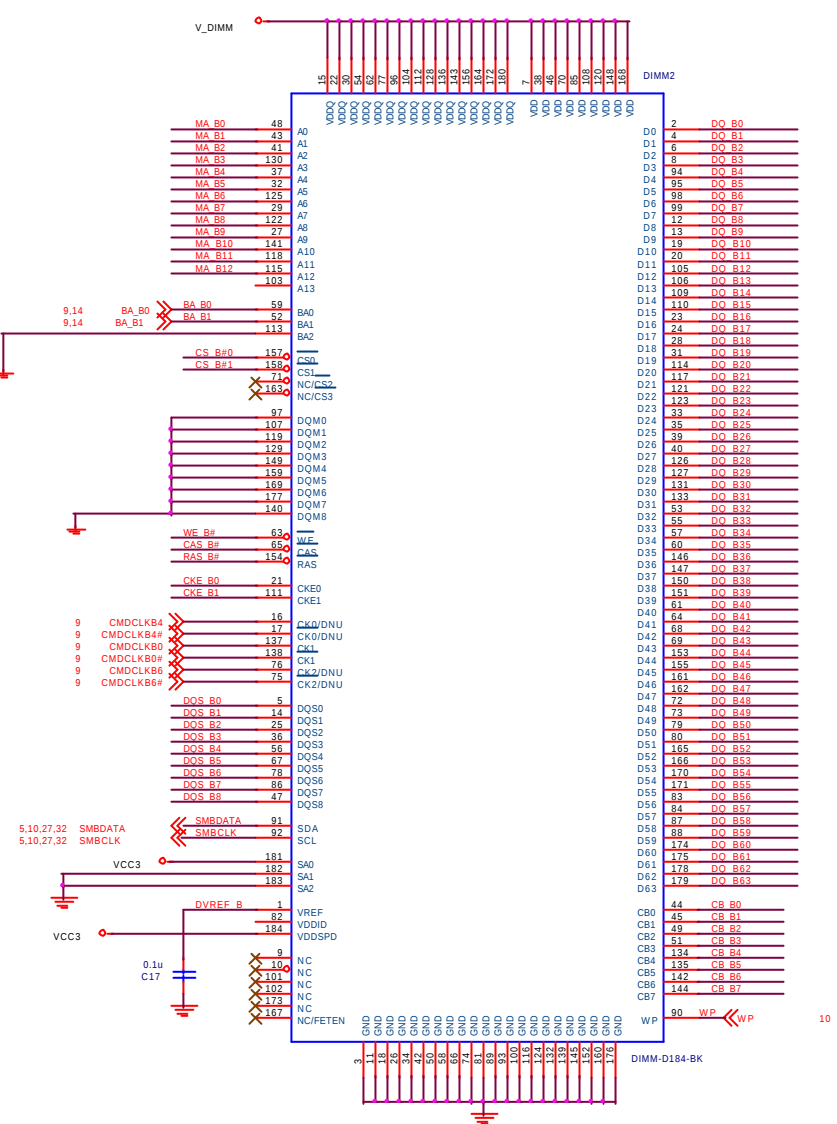


RAS B# 9.14
CAS B# 9.14
WE B# 9.14
DVREF_B 9

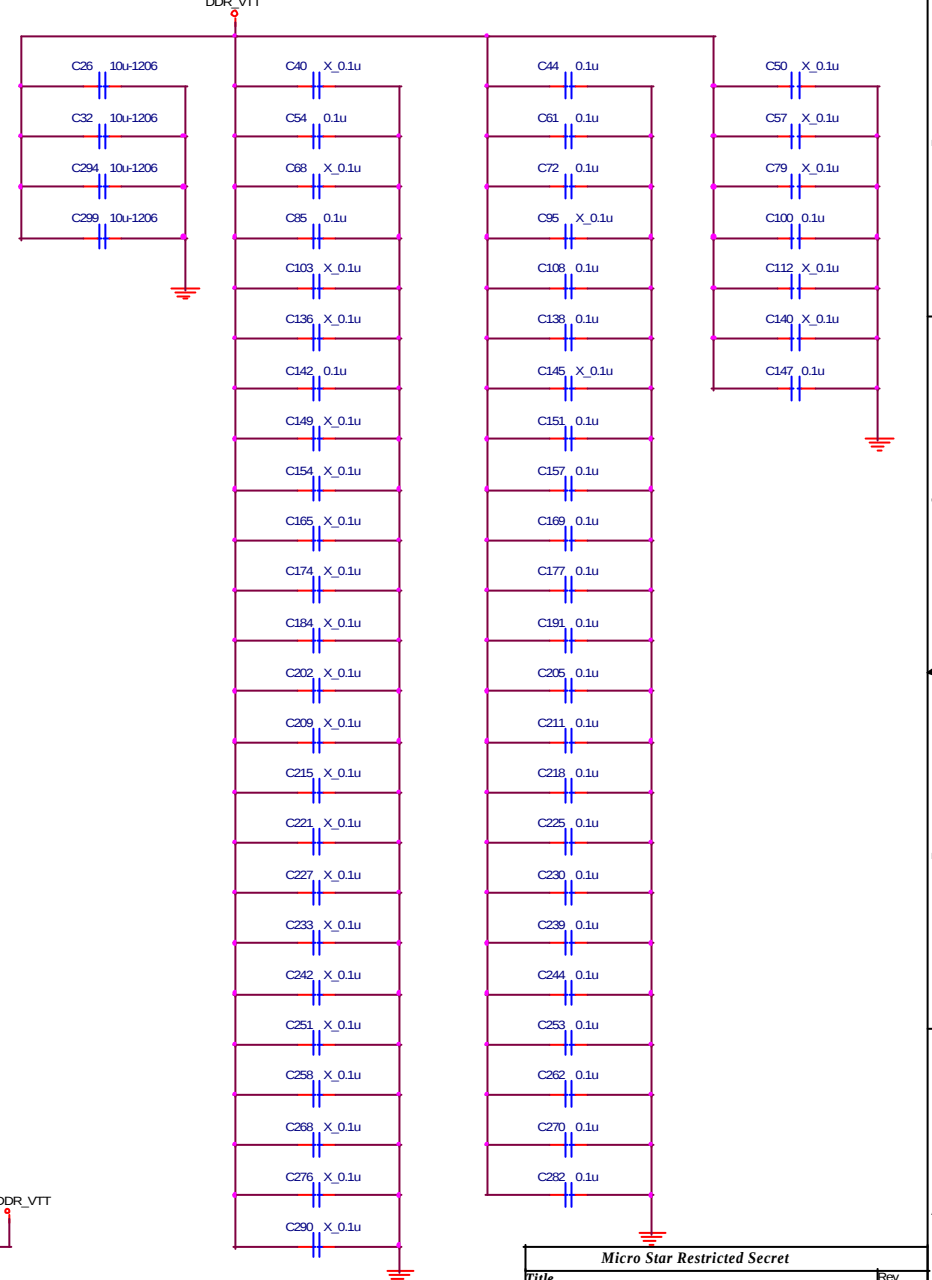
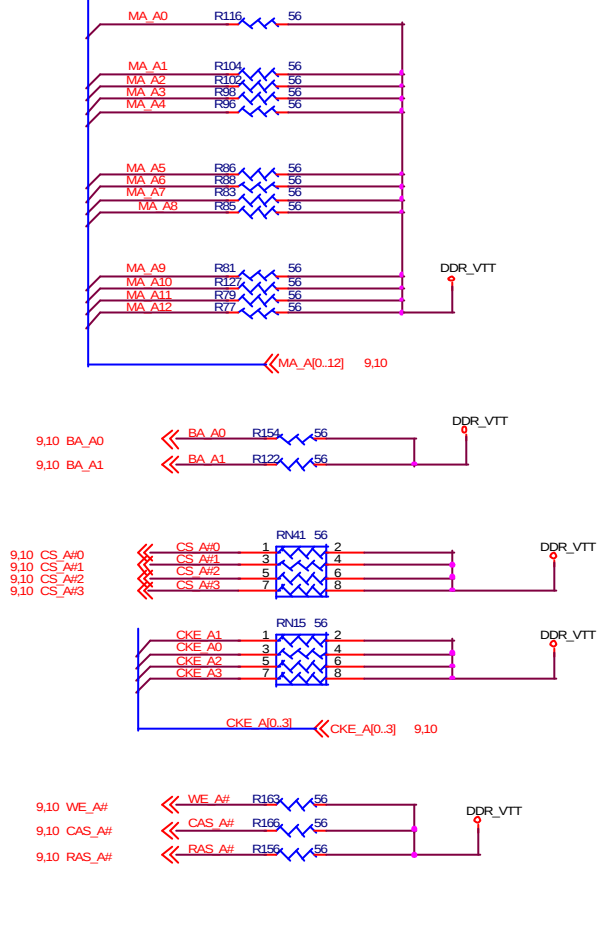
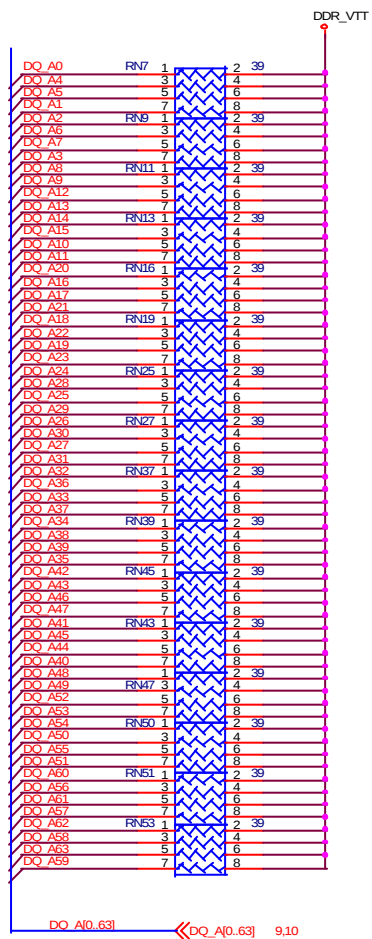
MA B[0..12] 9.14
DQS B[0..8] 9.14
CS_B#[0..3] 9.14
CKE_B[0..3] 9.14

CB B0
CB B1
CB B2
CB B3
CB B4
CB B5
CB B6
CB B7

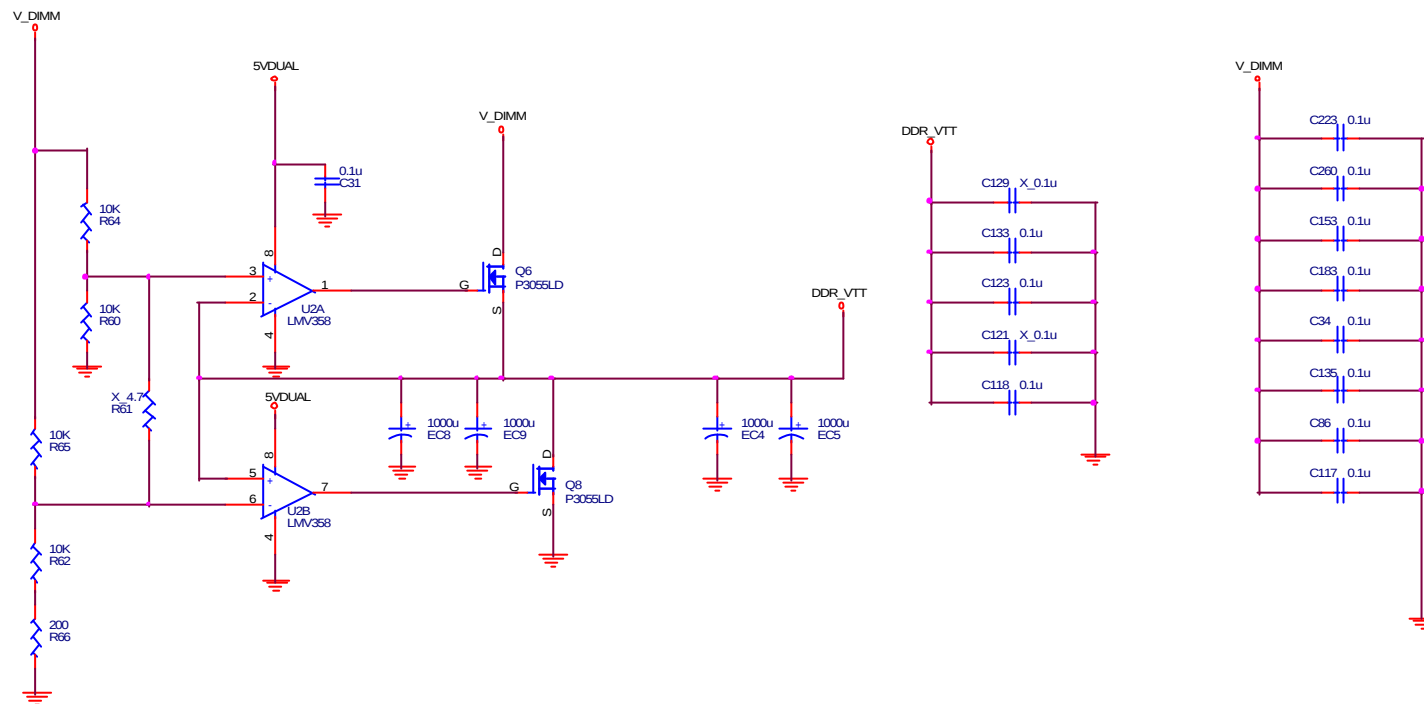
CB B[0..7] 9.14



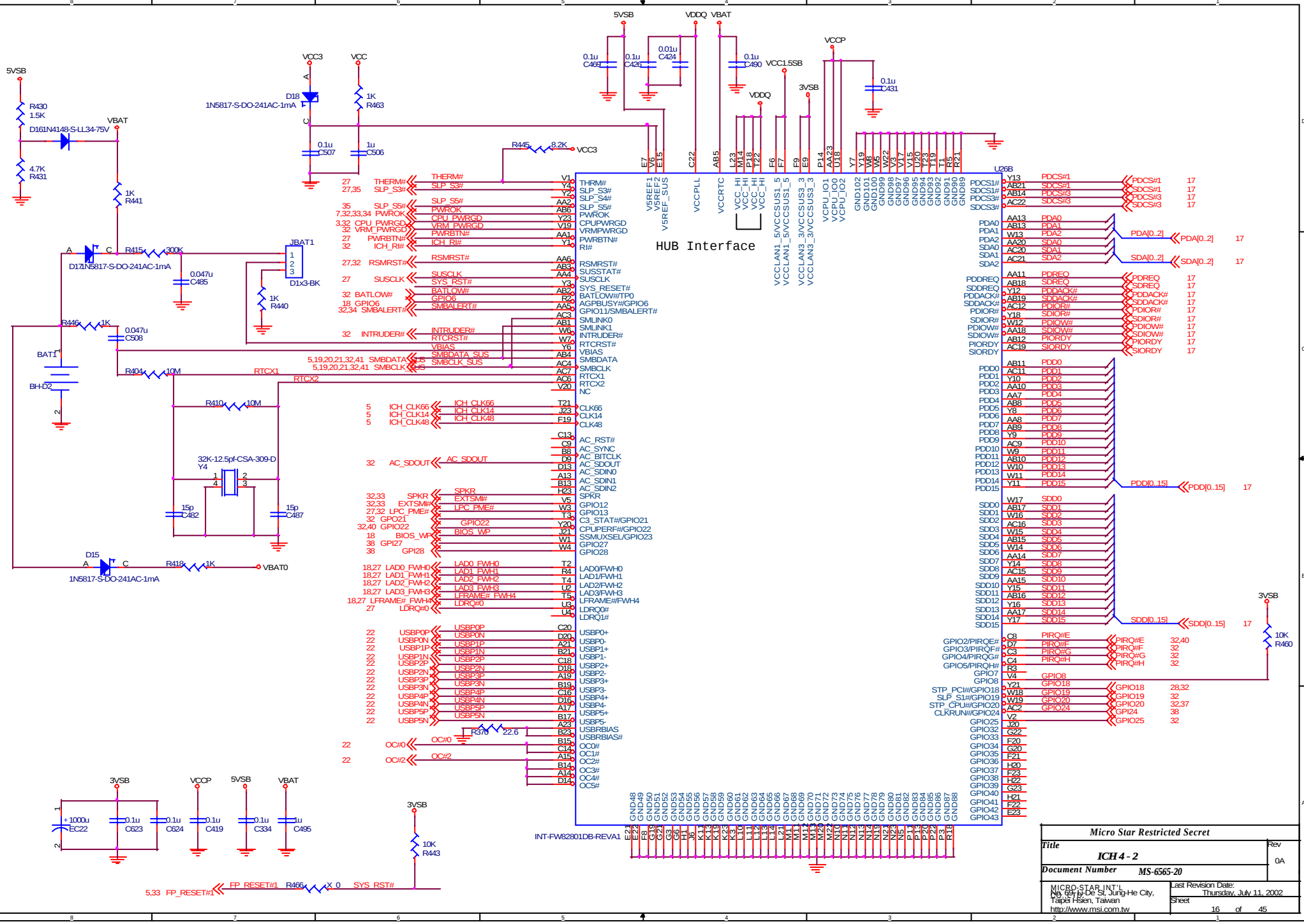
Address = A2



Micro Star Restricted Secret			
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Document Number	MS-6565-20		0A
MICRO-STAR INT'L No. 95, De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 12 of 45	



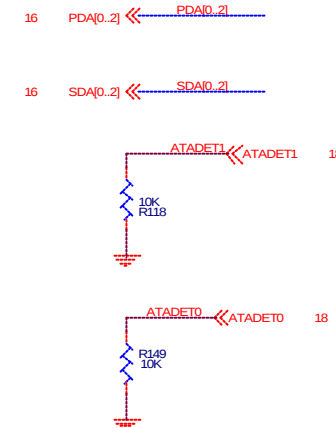
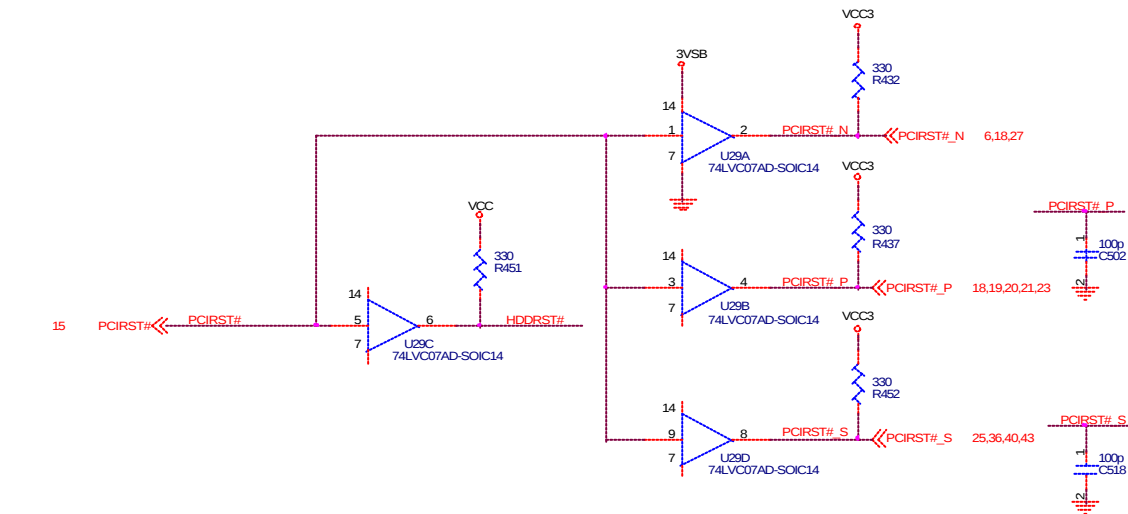
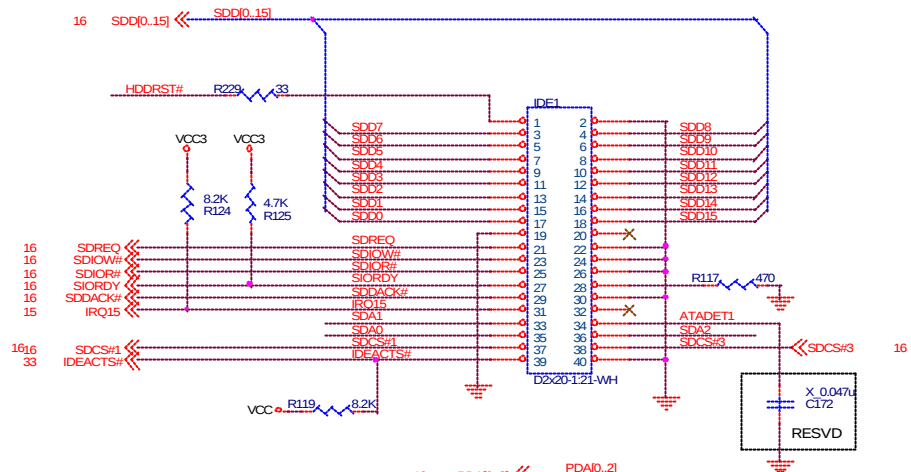
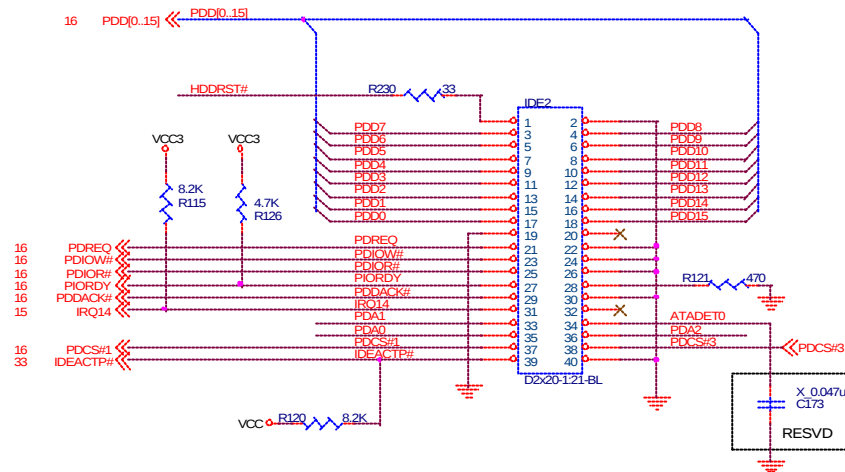
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Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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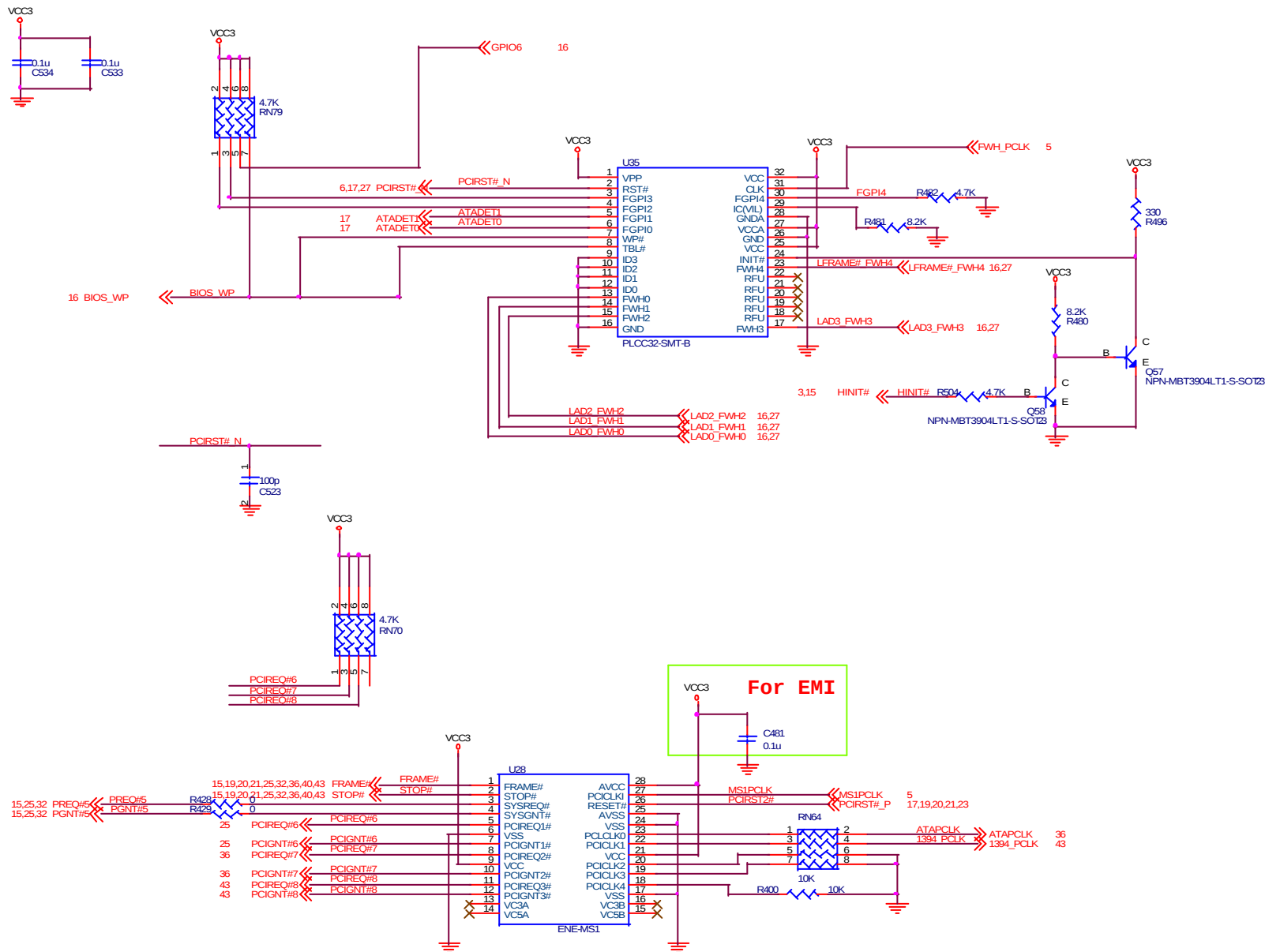
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Document Number	MS-6565-20	0A
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PRIMARY IDE CONN.

SECONDARY IDE CONN.

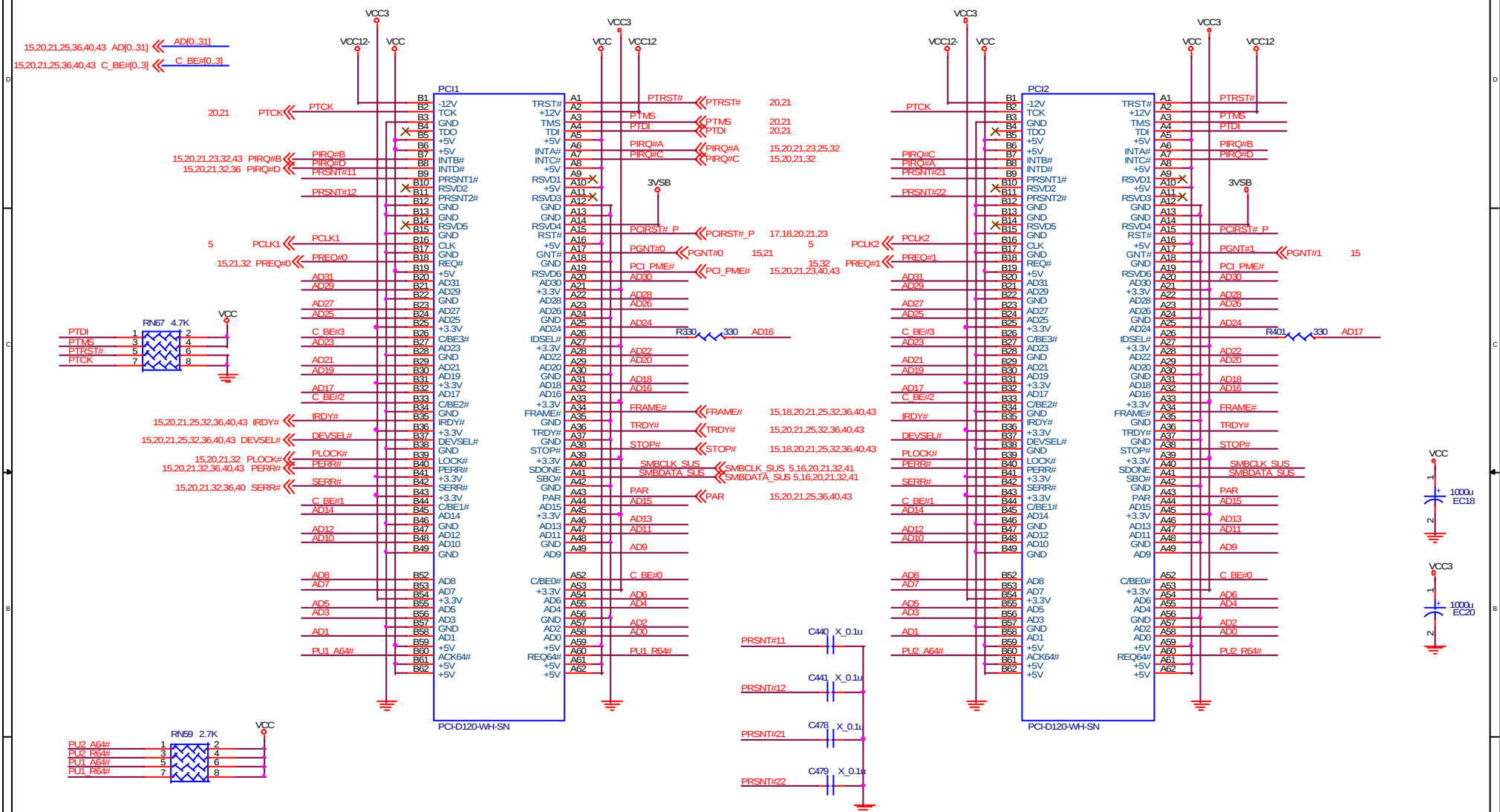


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Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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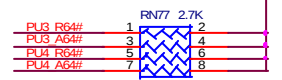
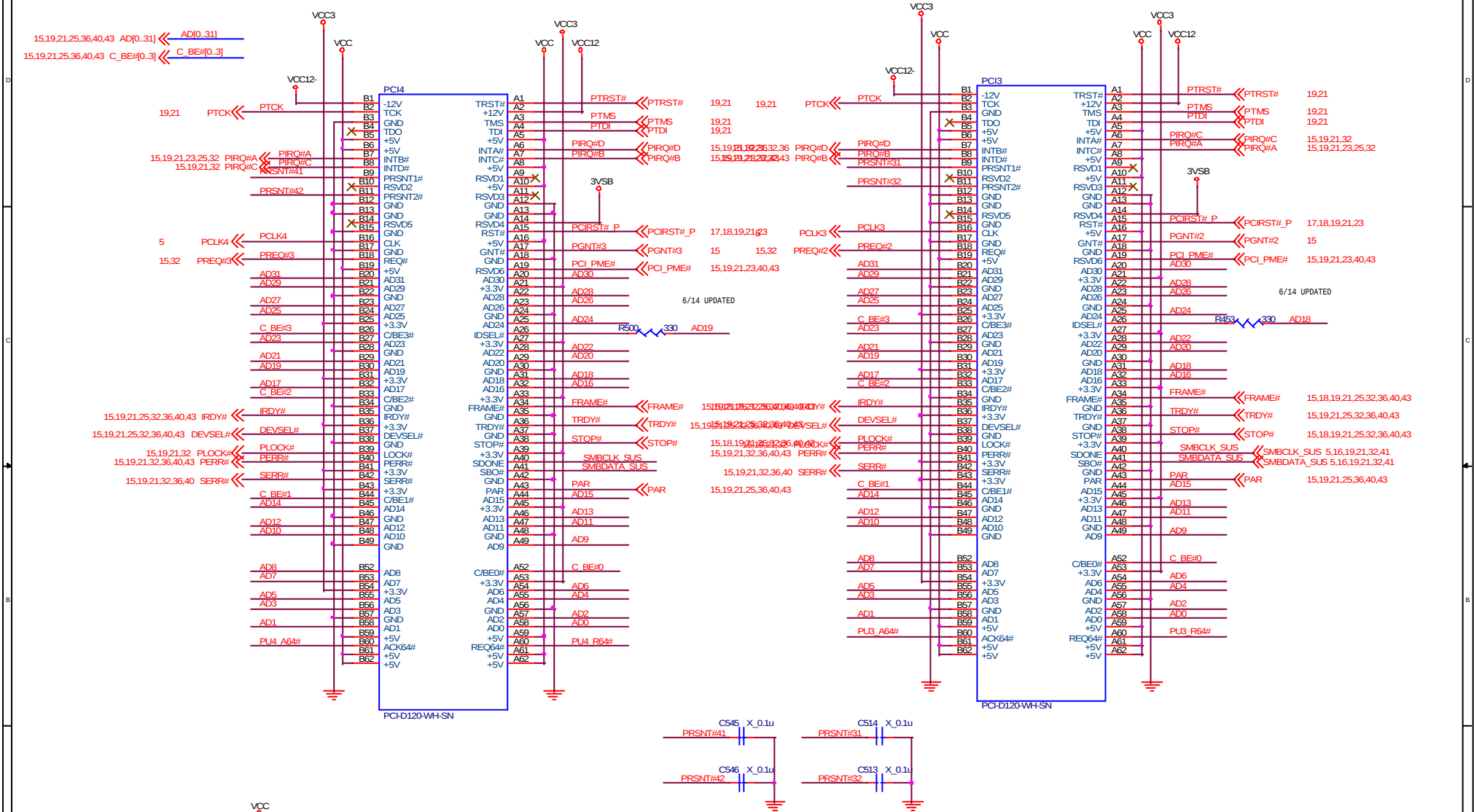
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Document Number	MS-6565-20	0A
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32/33 PCI Connector 1 & 2



Micro Star Restricted Secret		
Title		Rev
PCI 1 & PCI 2		0A
Document Number		MS-6565-20
MICRO STAR INT'L No. 66, 4/F, De St. Jung-Ho City, Tapei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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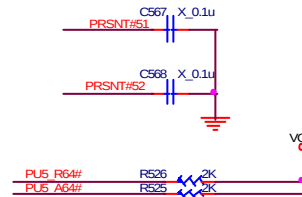
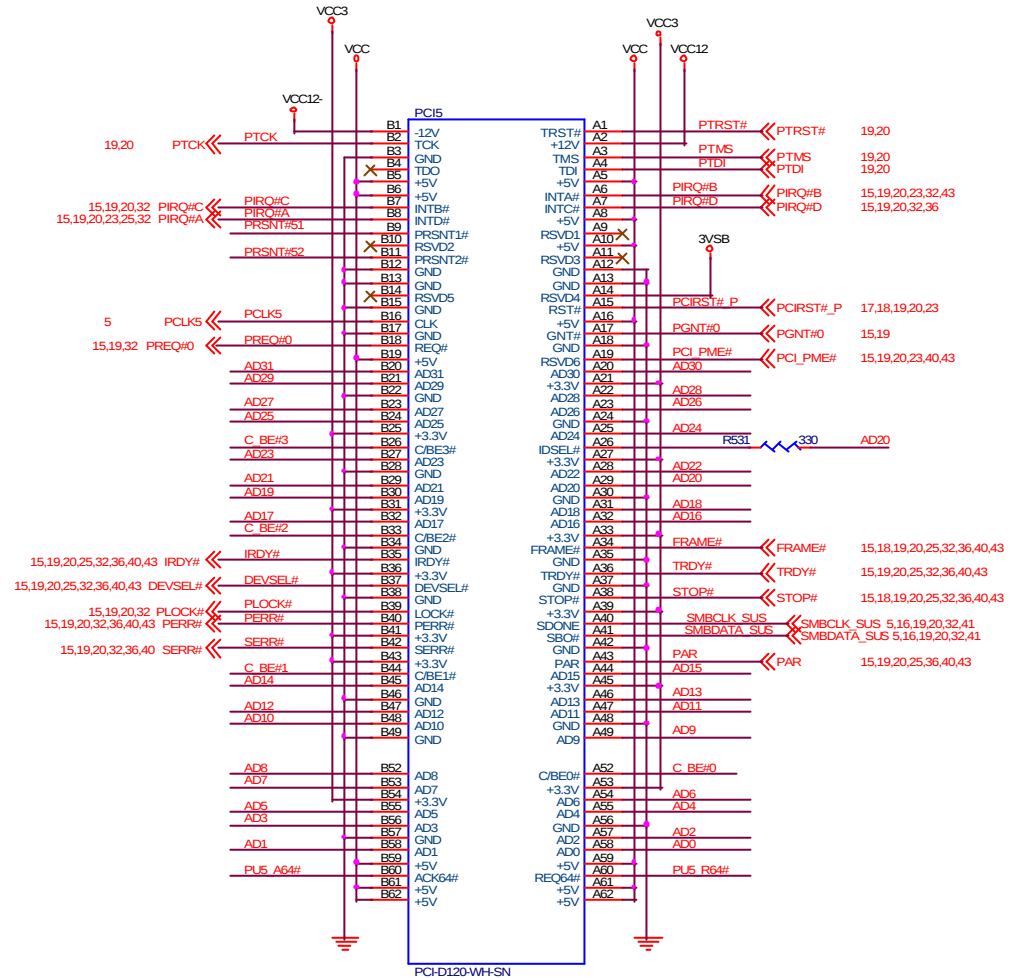
32/33 PCI Connector 3 & 4



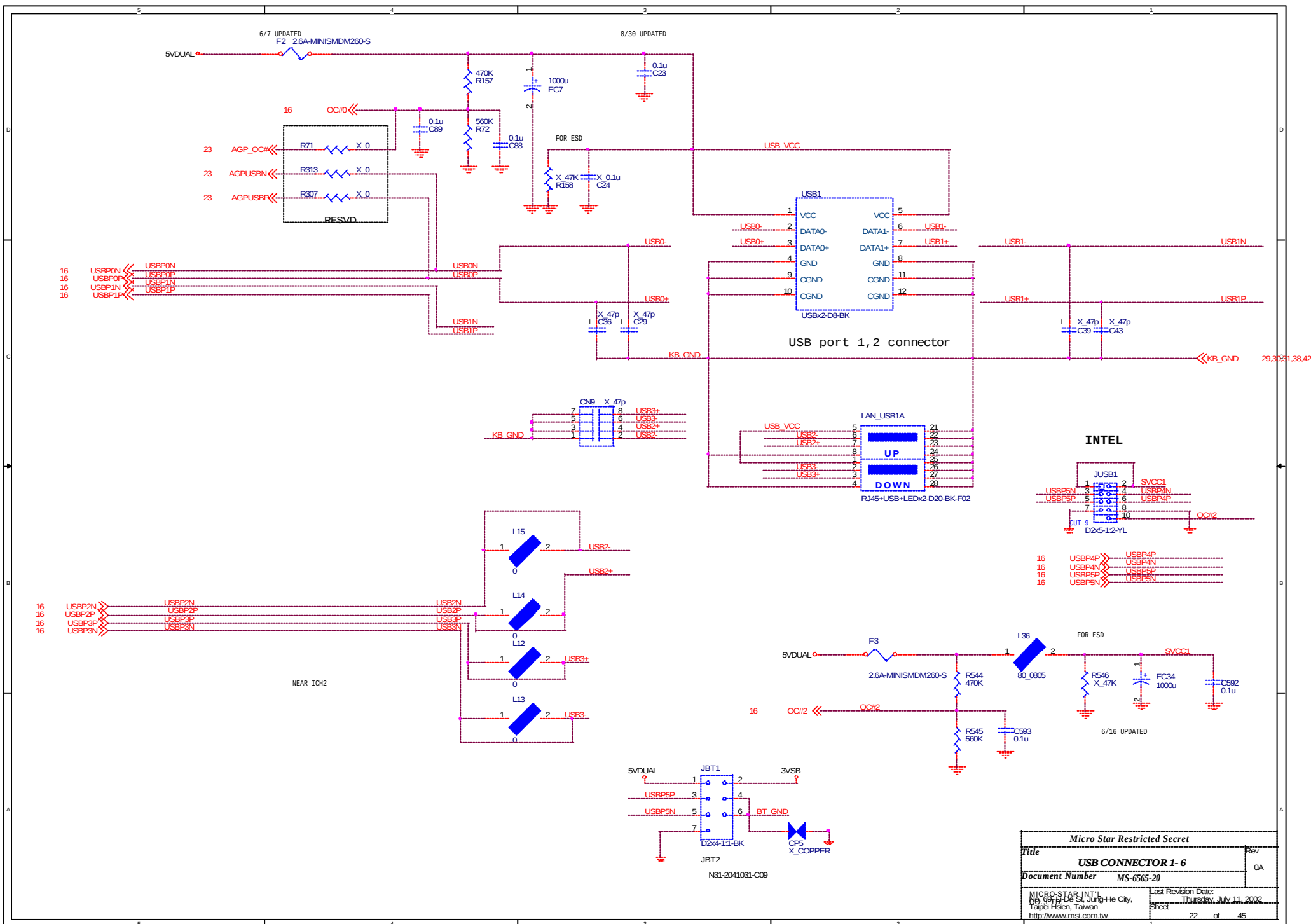
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Title	PCI 3 & PCI 4	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, St. Jung-He City, Taipai Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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32/33 PCI Connector 5 & 6

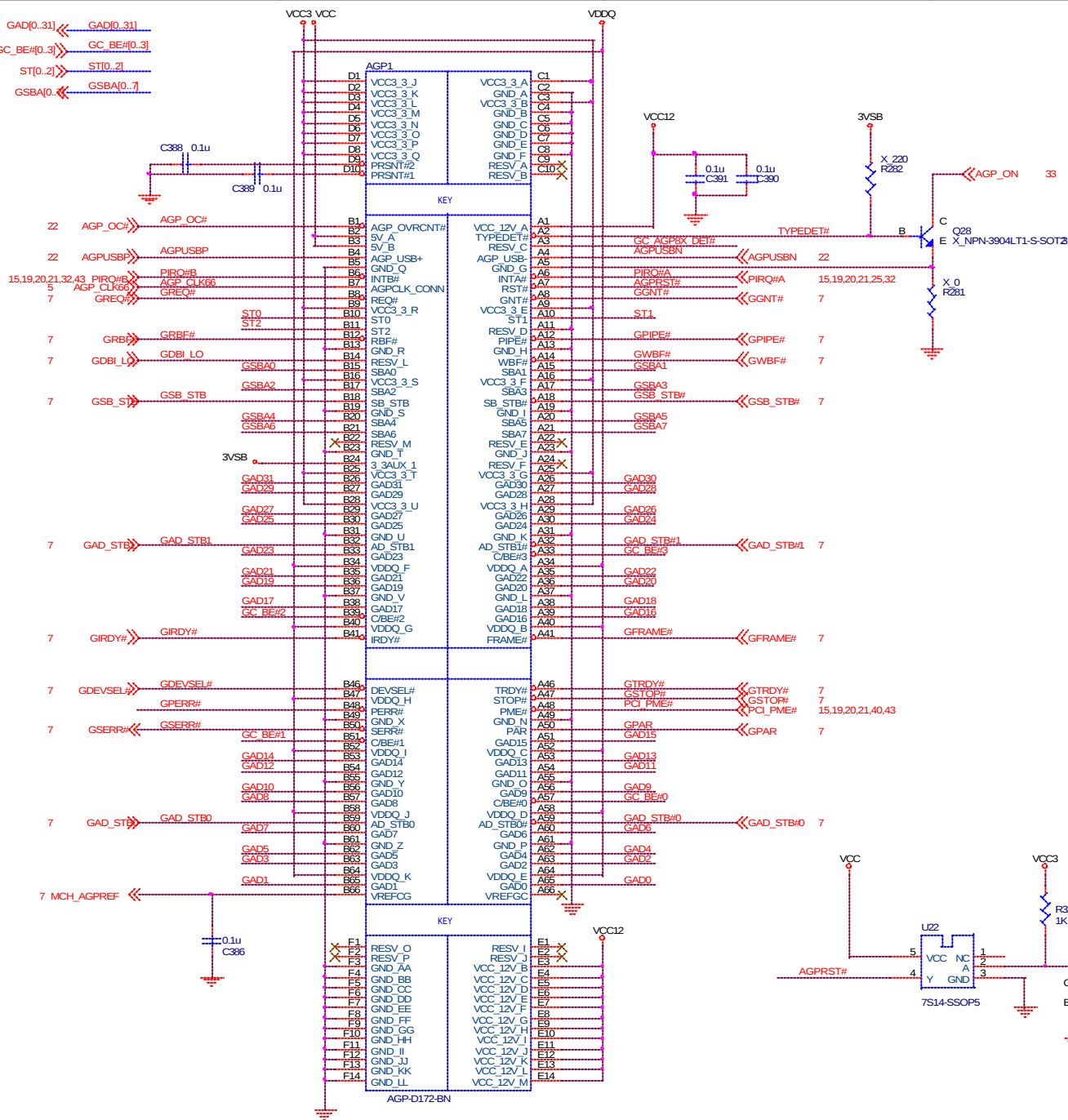
15,19,20,25,36,40,43 AD[0..31] << AD[0..31]
15,19,20,25,36,40,43 C_BE#[0..3] << C_BE#[0..3]



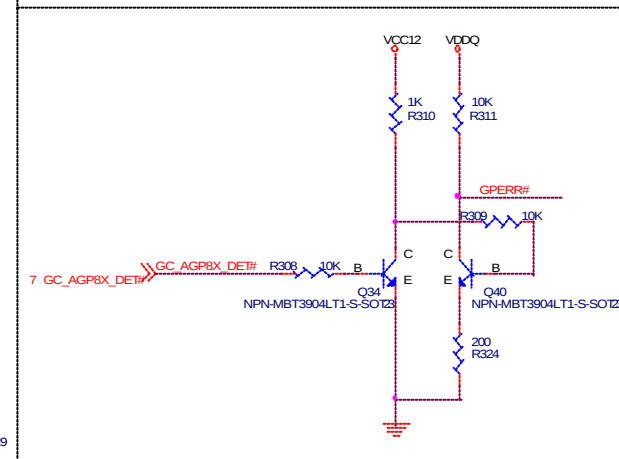
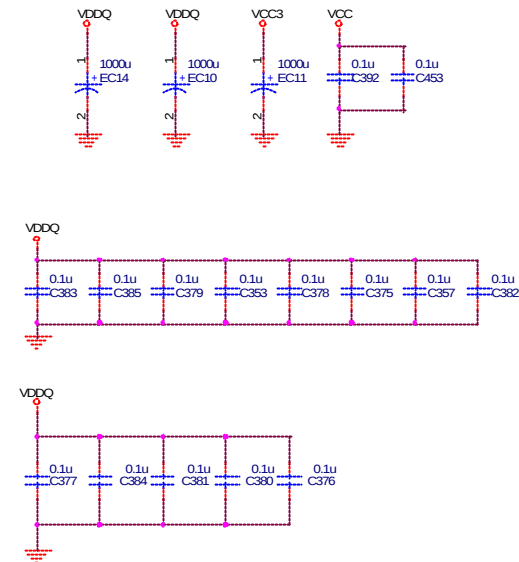
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Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, St. Jung-He City, Taipai Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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7 GAD[0..31] << GAD[0..31]
7 GC_BE#[0..3] << GC_BE#[0..3]
7 ST[0..2] << ST[0..2]
7 GSBA[0..7] << GSBA[0..7]

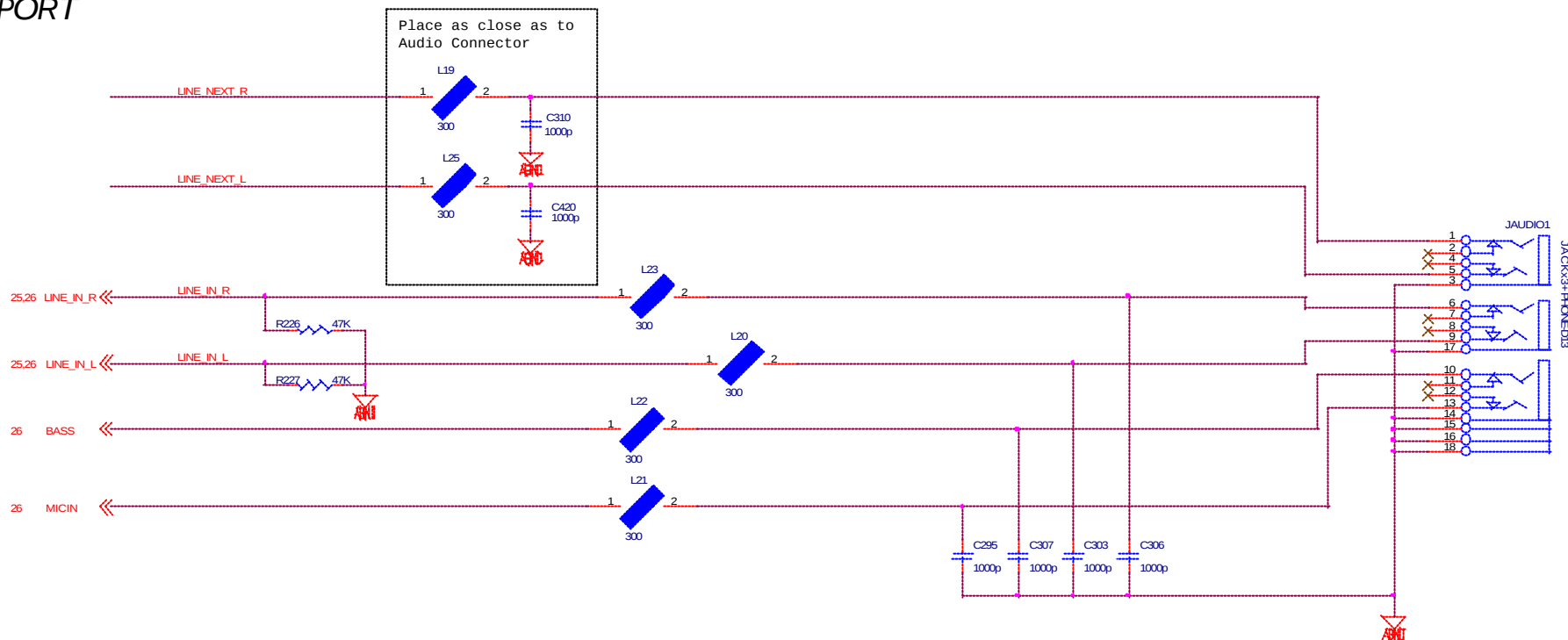


CLOSE AGP SLOT

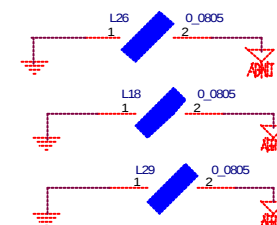
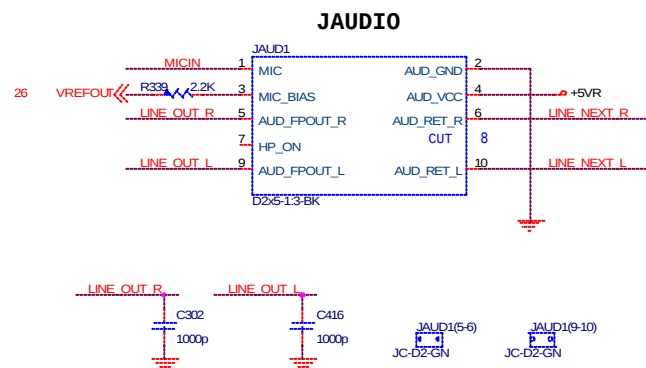
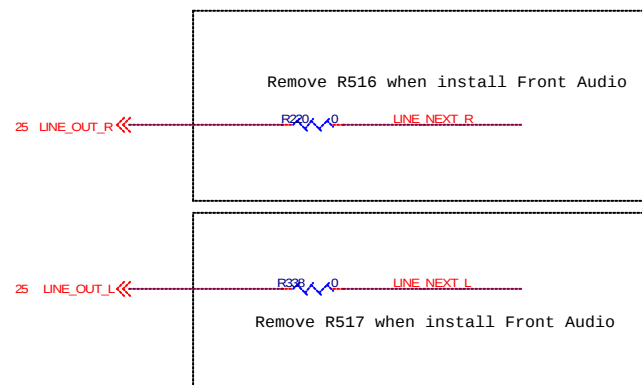


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Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taippei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 23 of 45

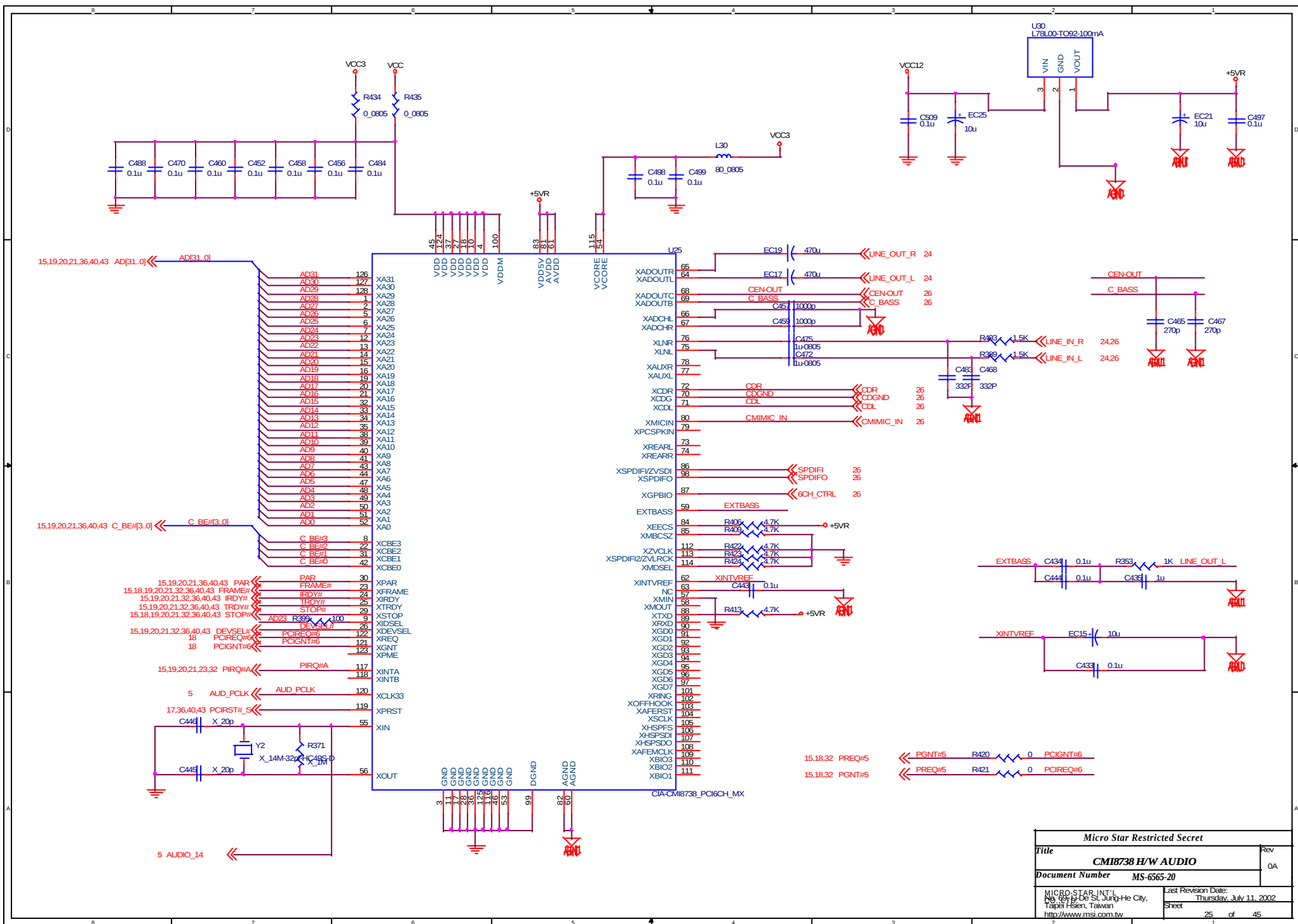
AUDIO PORT



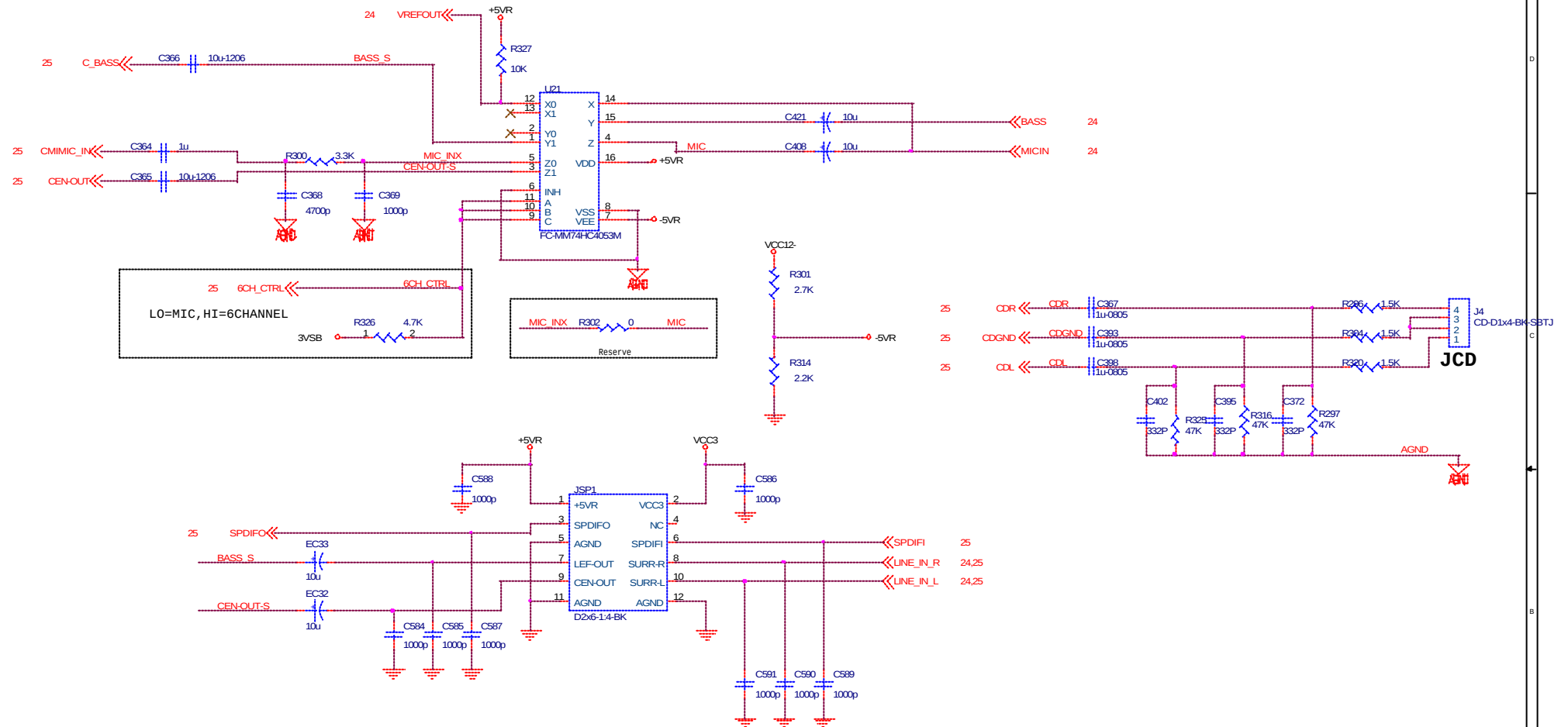
Audio Connector



Micro Star Restricted Secret		
Title	AUDIO CONNECTOR	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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Audio SPDIF / 6 channel connector



Micro Star Restricted Secret		
Title	SPDIF / 6CH Controller	REV
Document Number	MS-6565-20	0A
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FLOPPY DISK HEADER

IR HEADER

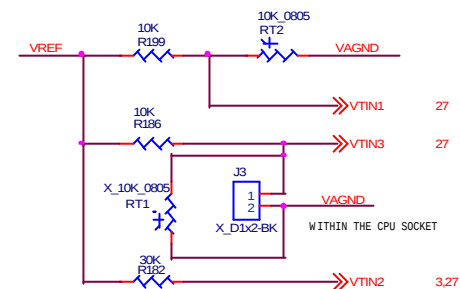
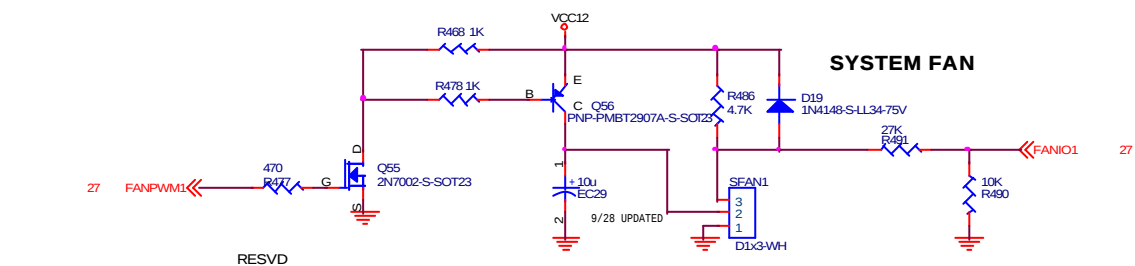
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

SIO

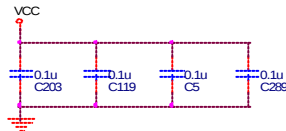
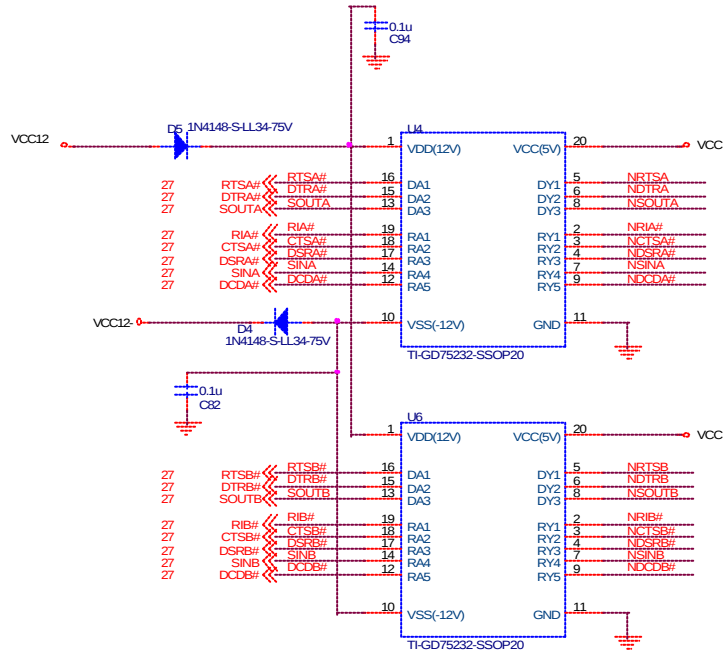
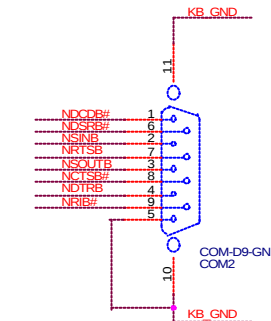
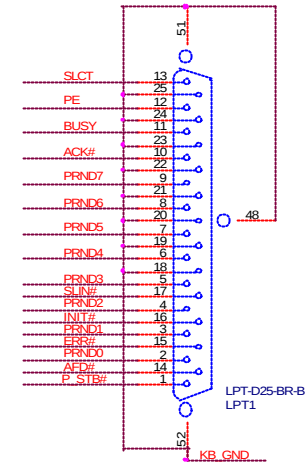
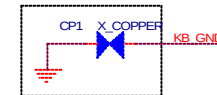
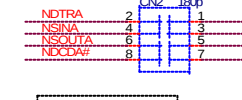
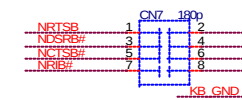
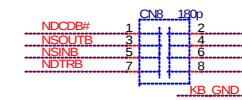
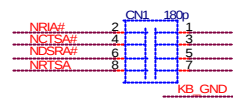
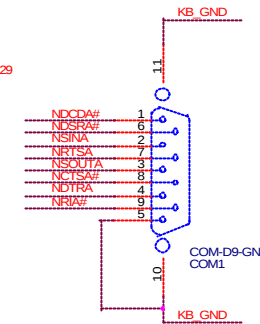
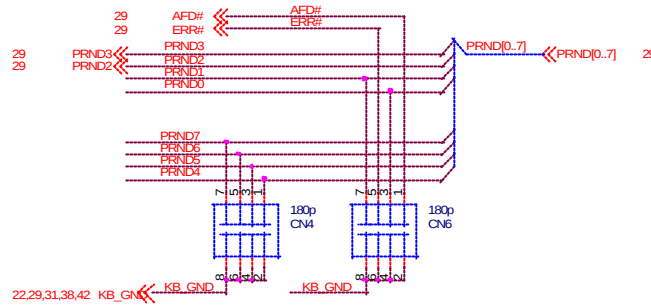
Resume Reset Circuitry

Distribute near the VCC power pin of the LPC

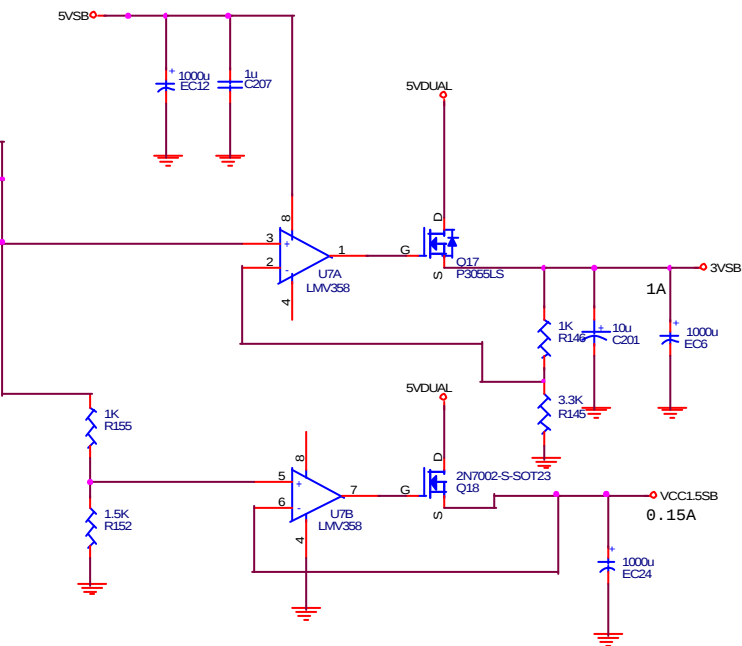
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Document Number	MS-6565-20	0A
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ACK# <-> ACK# 29
 BUSY <-> BUSY 29
 PE <-> PE 29
 SLCT <-> SLCT 29
 AFD# <-> AFD# 29
 ERR# <-> ERR# 29
 INIT# <-> INIT# 29
 SLIN# <-> SLIN# 29
 P_STB# <-> P_STB# 29

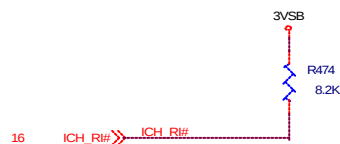
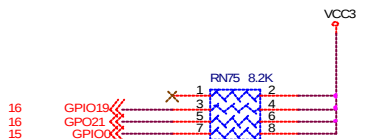
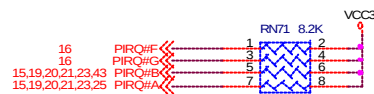
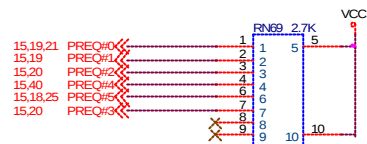
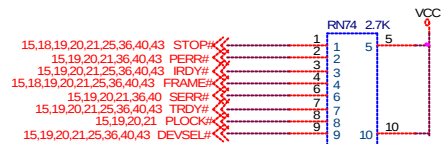


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Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 30 of 45

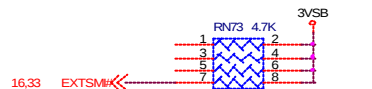
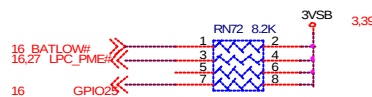
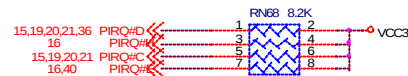
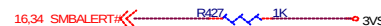
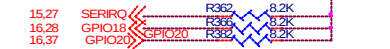


Micro Star Restricted Secret		
Title	KB/MS & 3VSB/1.5SB POWER	REV
Document Number		0A
MS-6565-20		
MICRO-STAR INT'L No. 96, Sec. 2, Jung-Ho City, Taipei, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 31 of 45

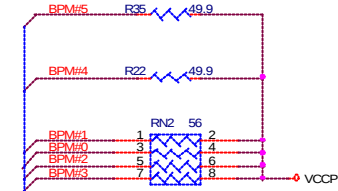
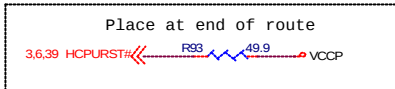
PCI BUS



ICH

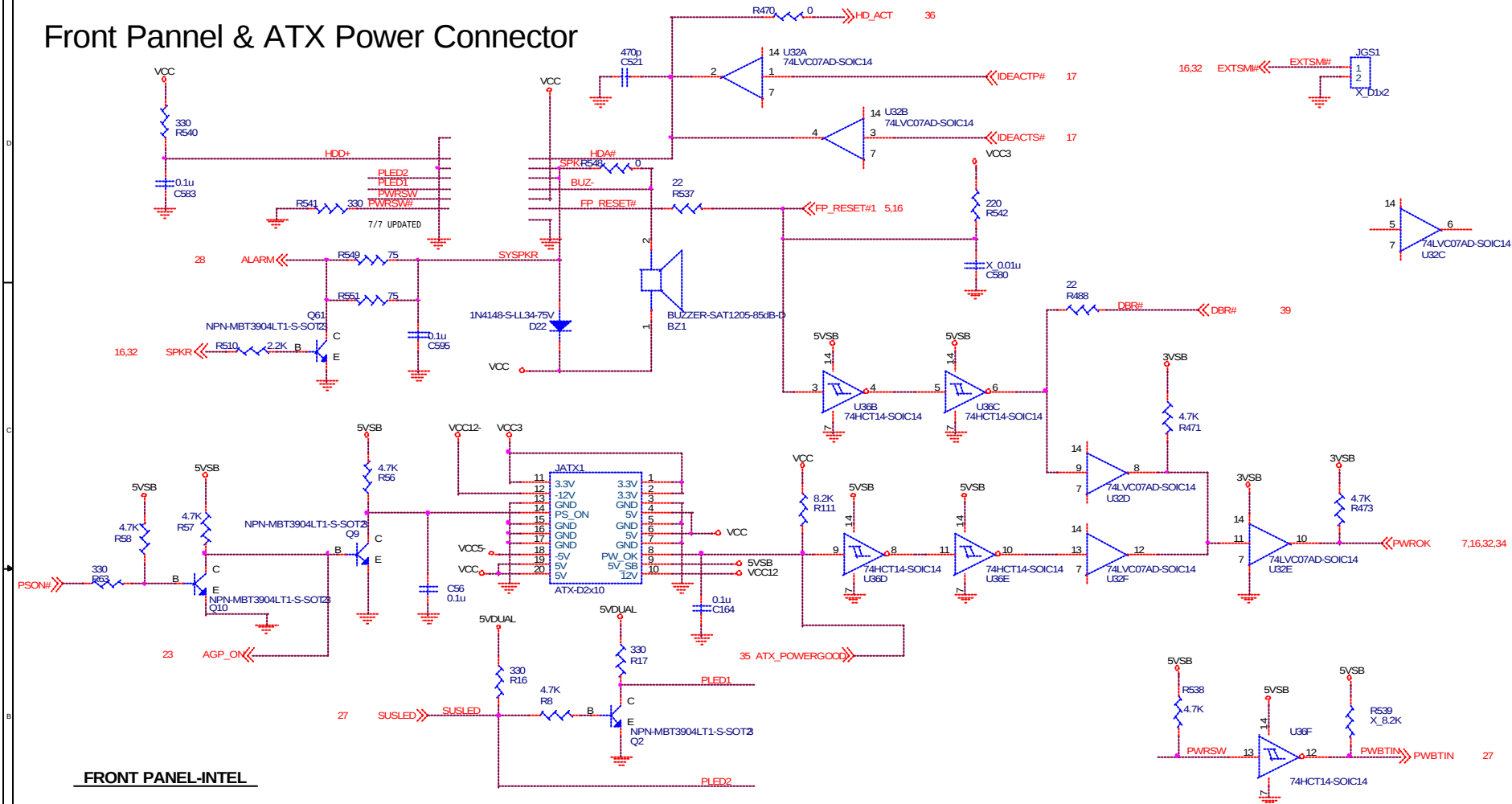


CPU

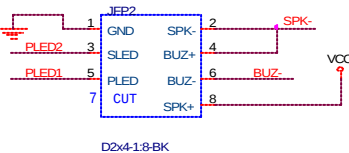
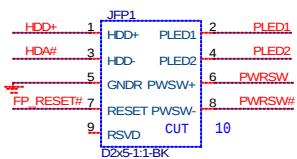


Micro Star Restricted Secret		
Title	PULL UP RESISTORS	REV
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 32 of 45

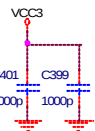
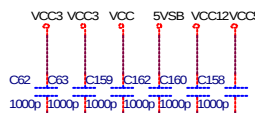
Front Panel & ATX Power Connector



FRONT PANEL-INTEL

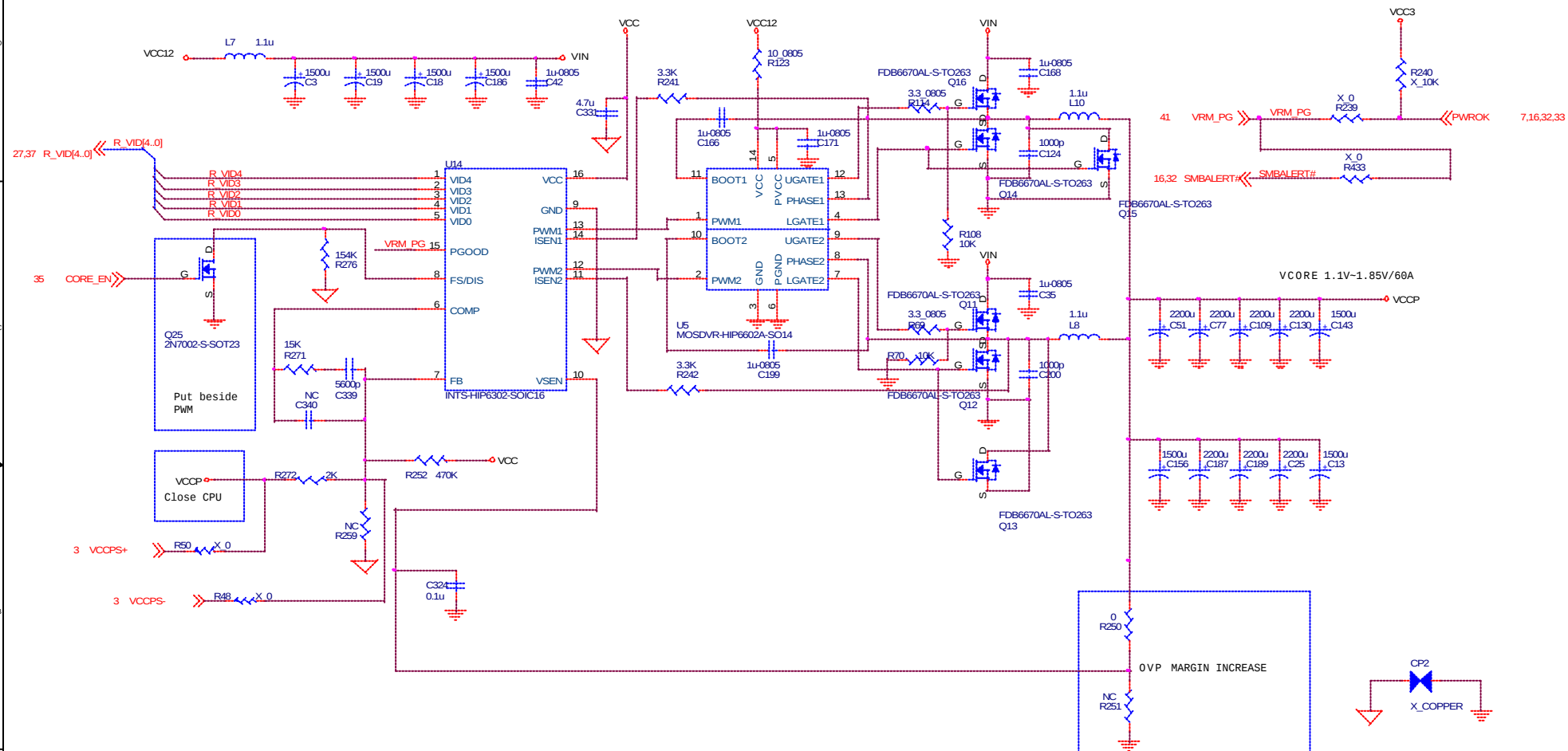


Add around ATX connector.

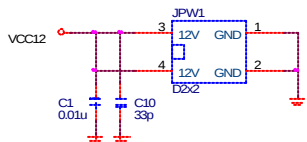


Micro Star Restricted Secret		
Title	FRONT PANNEL & ATX POWER	REV 0A
Document Number	MS-6565-20	
MICRO-STAR INT'L No. 99, Sec. 2, St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 33 of 45

HIP6302 FOR INTEL Granite Bay POWER CKT



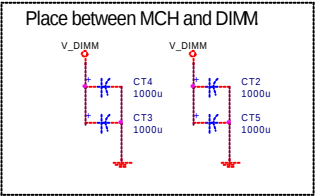
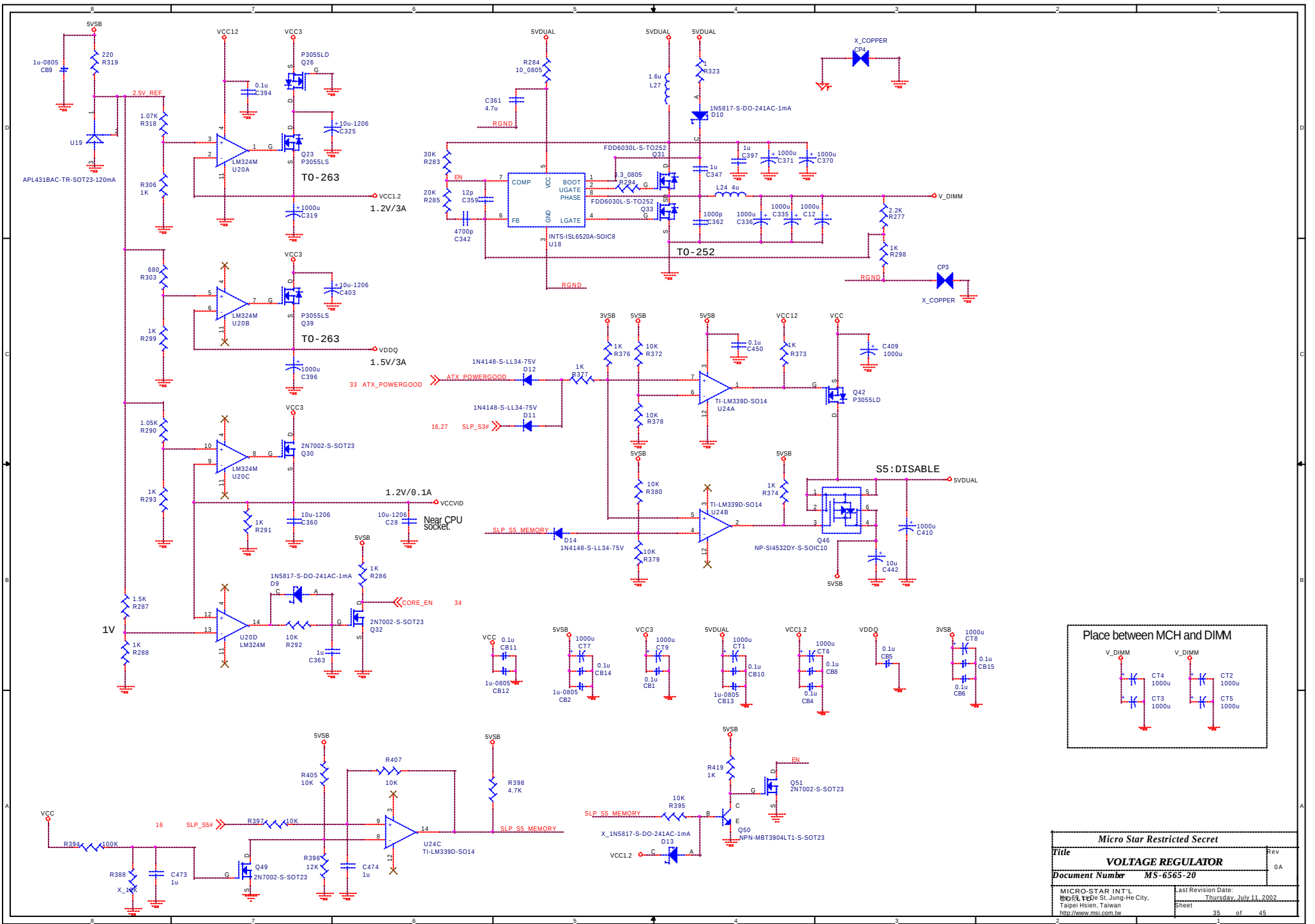
ATX12V POWER CONNECTOR



HIP6301 - VRM 9.0/9.2

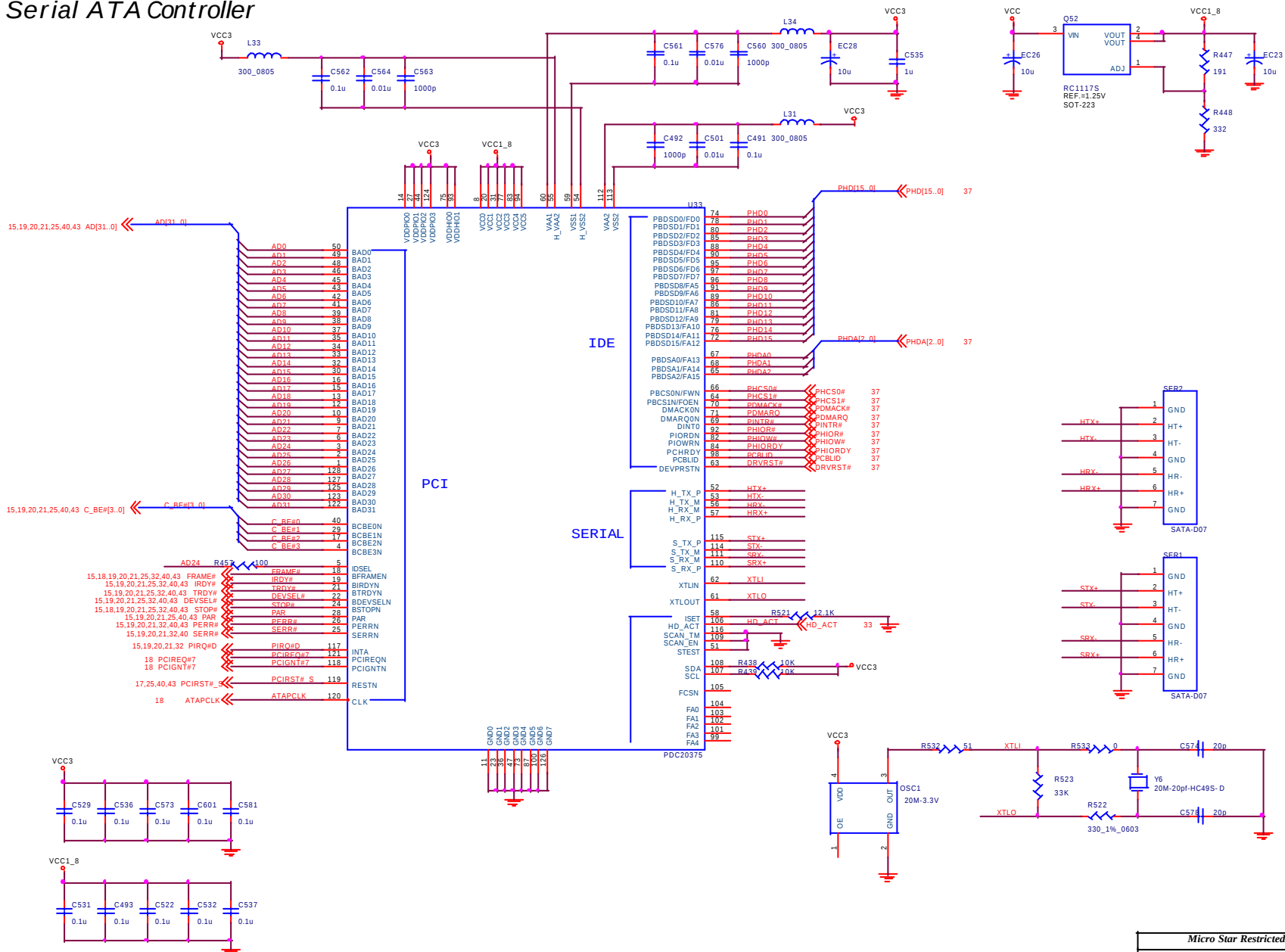
VID4	VID3	VID2	VID1	VID0	VDC(V)	VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30	0	1	0	0	0	1.650
1	0	0	1	1	1.425	0	0	1	1	1	1.675
1	0	0	0	0	1.45	0	0	1	1	0	1.70
0	1	1	1	1	1.475	0	0	1	0	1	1.725
0	1	1	1	0	1.500	0	0	1	0	0	1.75
0	1	1	0	1	1.525	0	0	0	1	1	1.775
0	1	1	0	0	1.550	0	0	0	1	0	1.80
0	1	0	1	1	1.575	0	0	0	0	1	1.825
0	1	0	1	0	1.600	0	0	0	0	0	1.85
0	1	0	0	1	1.625	1	1	1	1	1	OFF

Micro Star Restricted Secret		
Title	VRM9.1 INTERSIL HIP6302	Rev
Document Number	MS-6565-20	0A
MICRO STAR, INC. No. 69, Sec. 2, Jung-Ho City, Taippei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 34 of 45

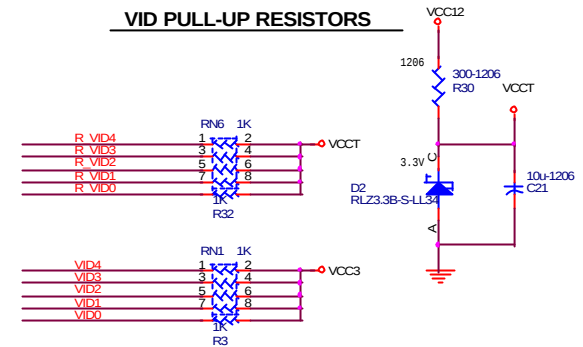
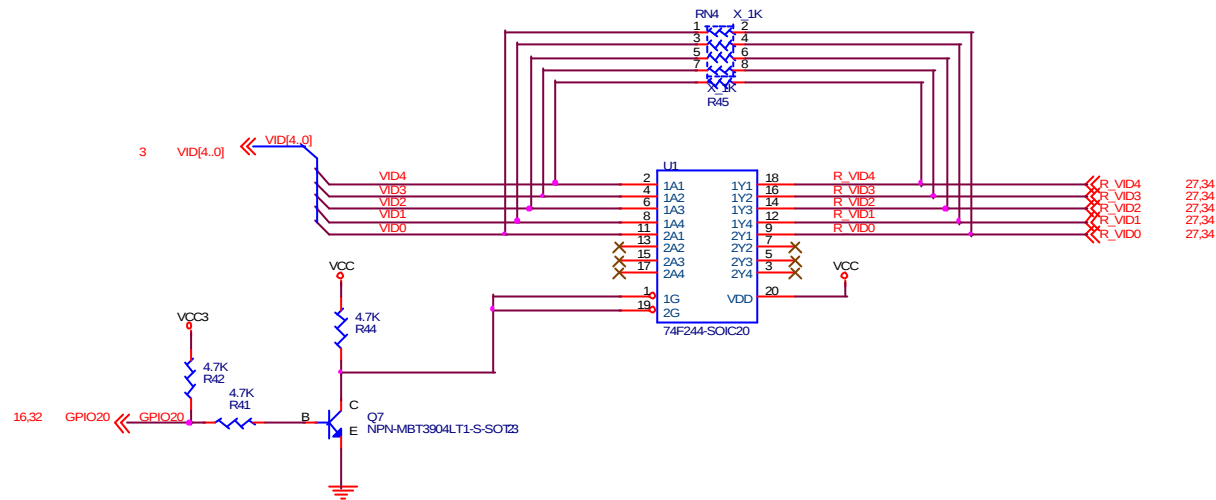


Micro Star Restricted Secret		
Title	VOLTAGE REGULATOR	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L 10094, 105th St. Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
		Sheet 35 of 45

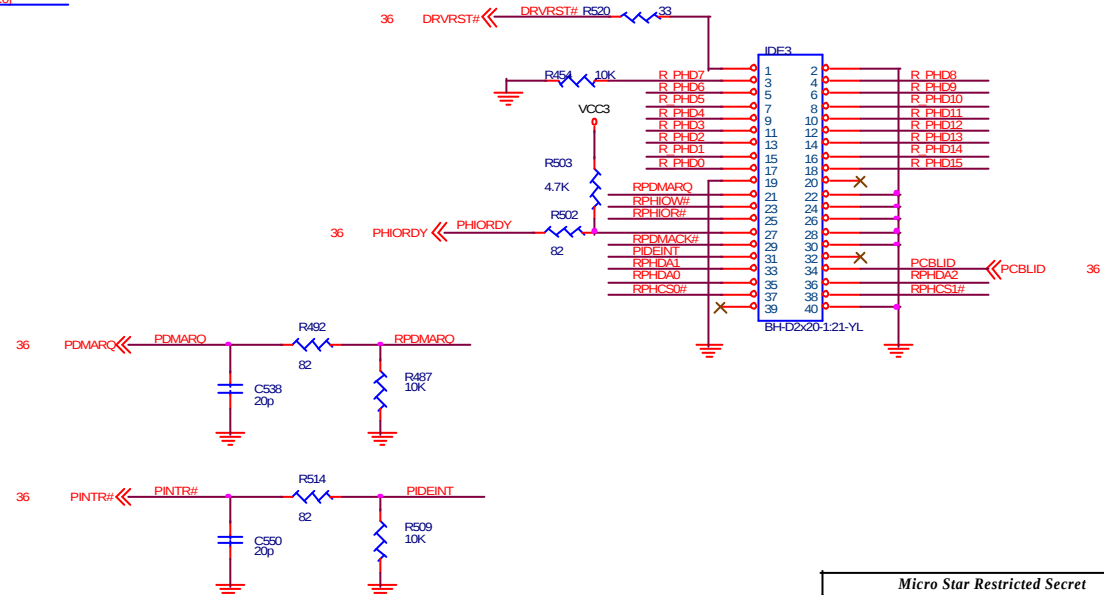
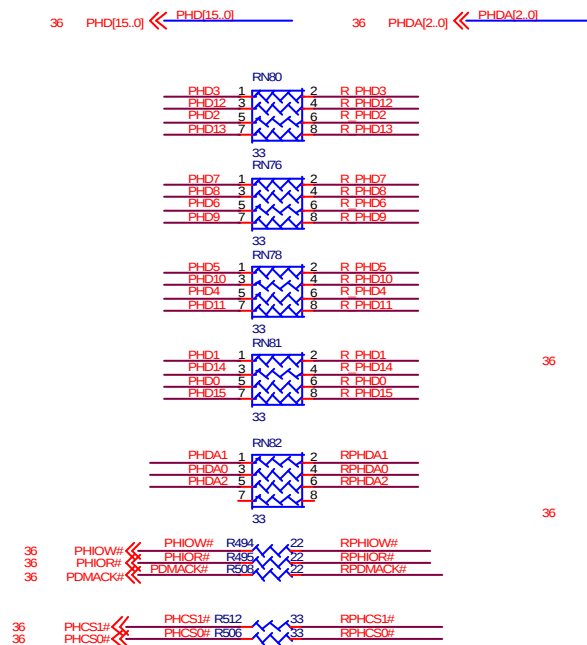
Serial ATA Controller



Micro Star Restricted Secret		
Title	SERIAL ATA	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L 80841 Ede St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday July 11 2002 Sheet 36 of 45

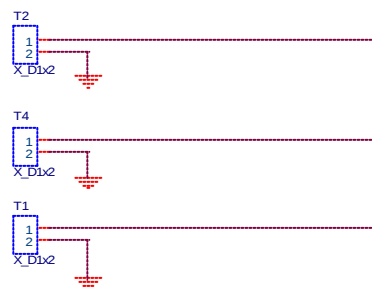
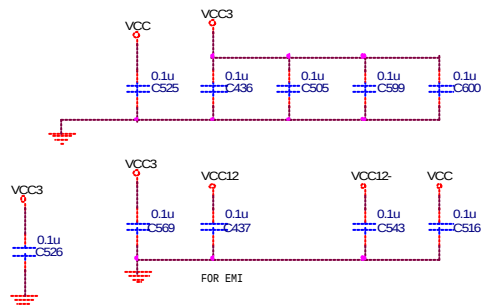
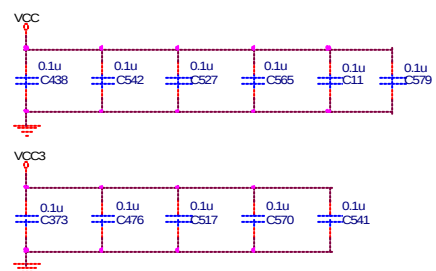
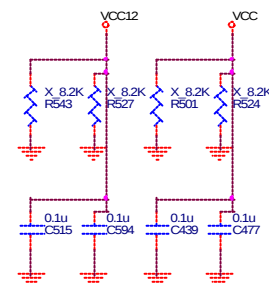
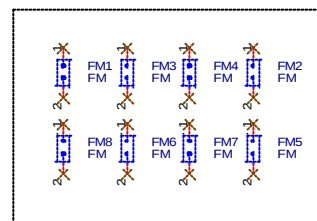
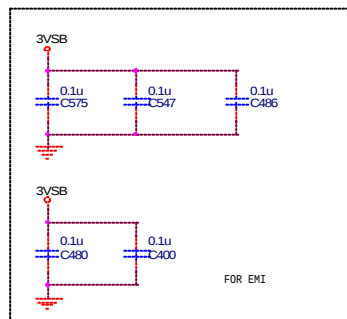
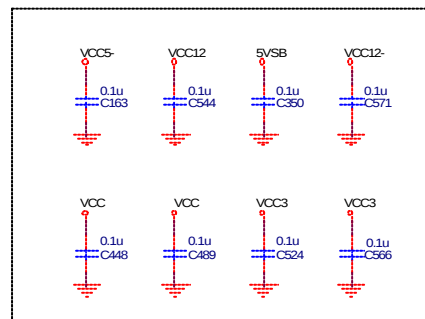
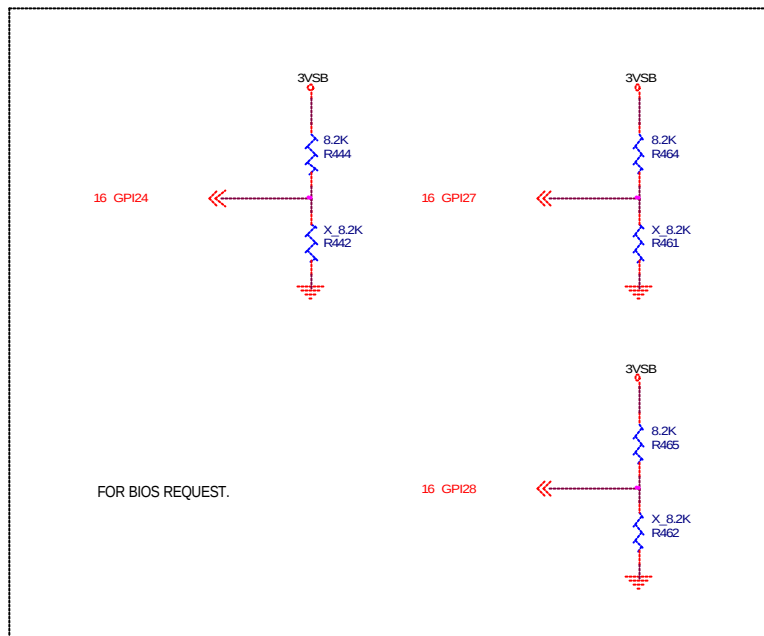
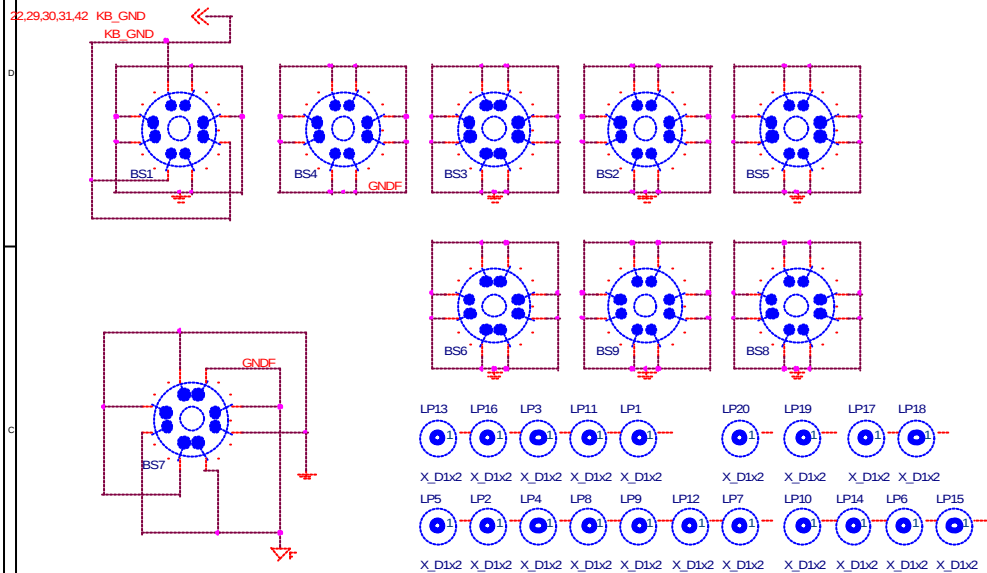


Serial ATA Connector

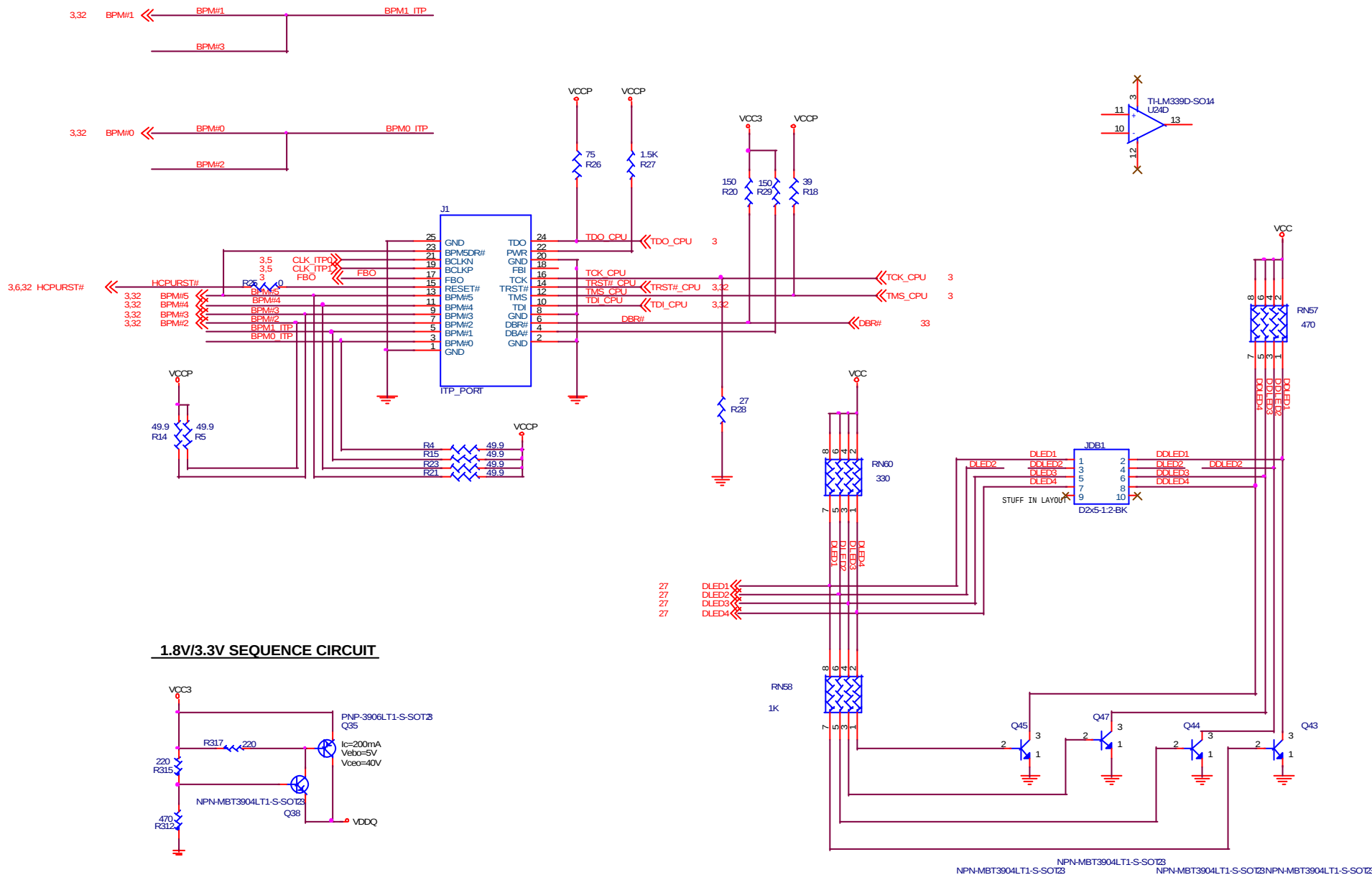


Micro Star Restricted Secret		
Title	CORE VOLTAGE ADJ / IDE 3	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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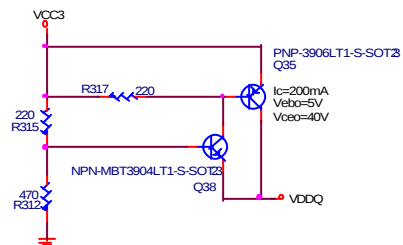
PCB OTHER COMPONENT



Micro Star Restricted Secret		
Title	MISC	REV
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002 Sheet 38 of 45

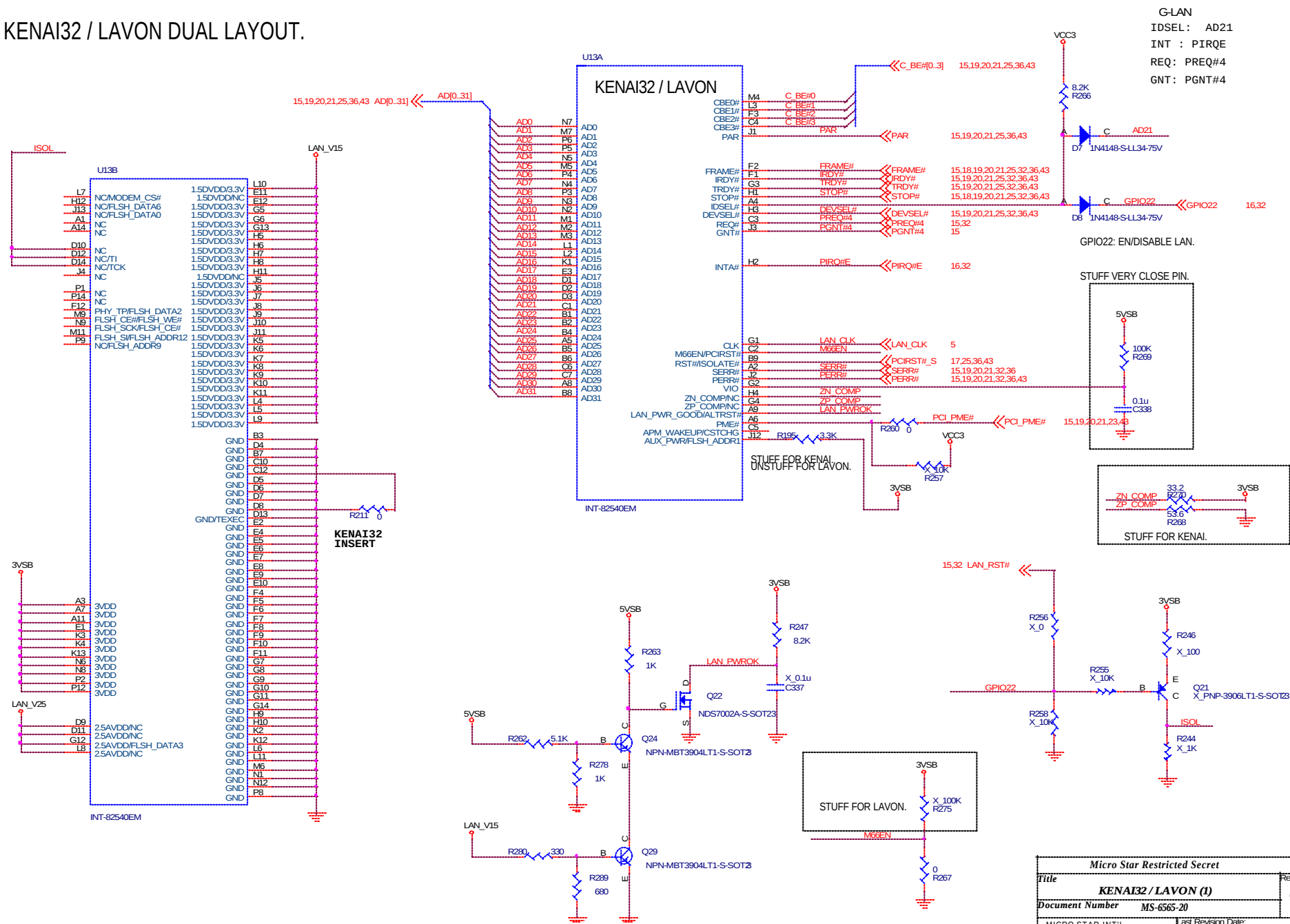


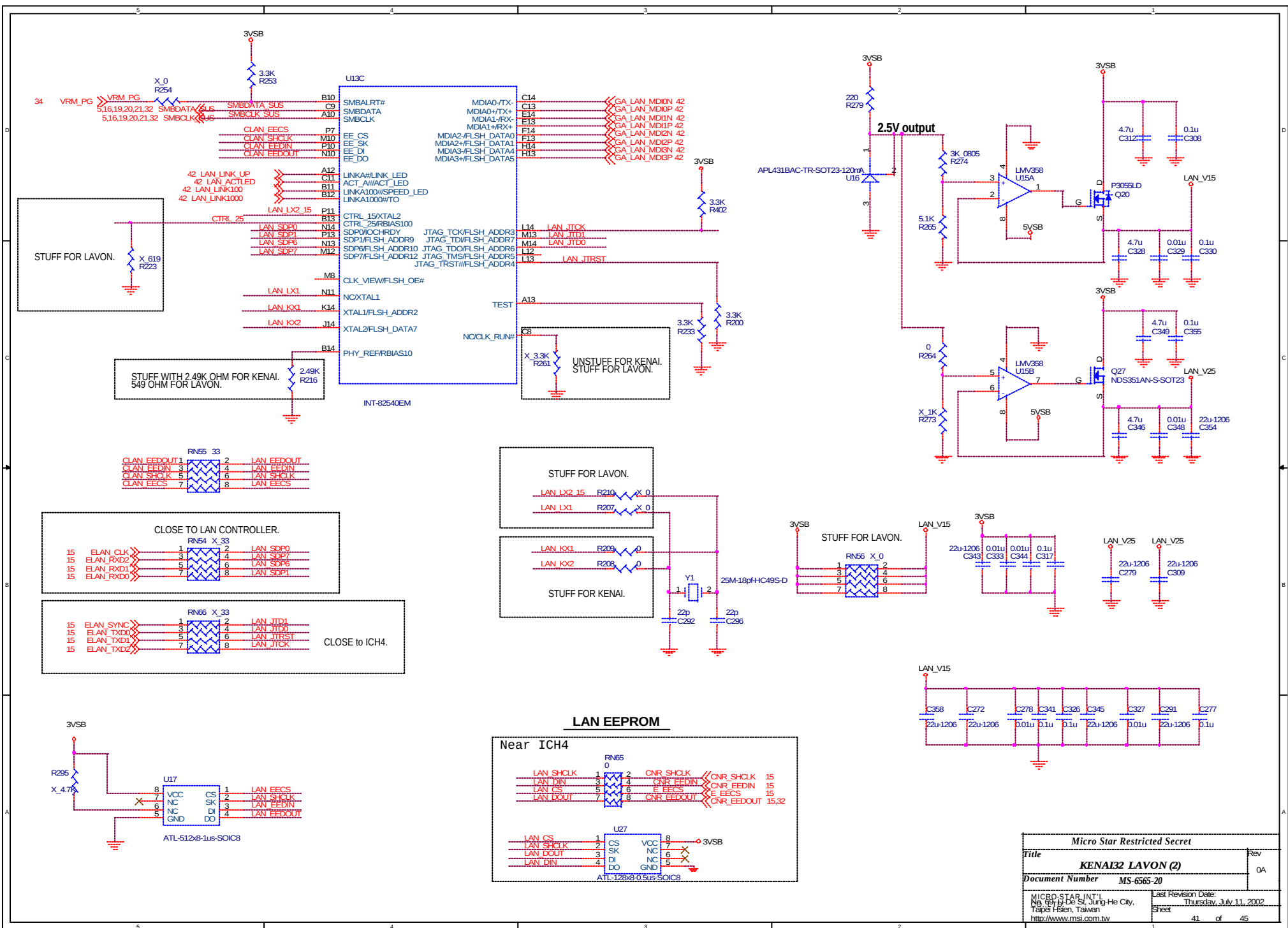
1.8V/3.3V SEQUENCE CIRCUIT

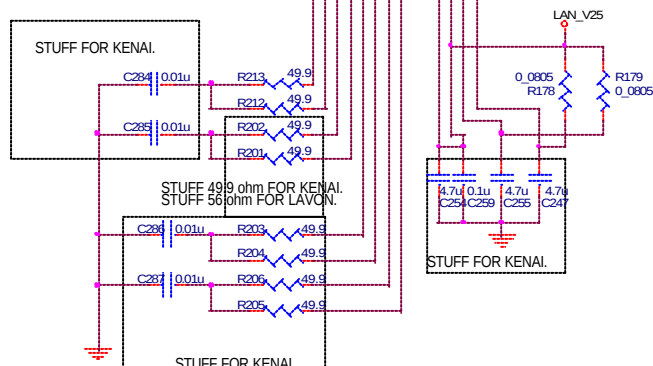
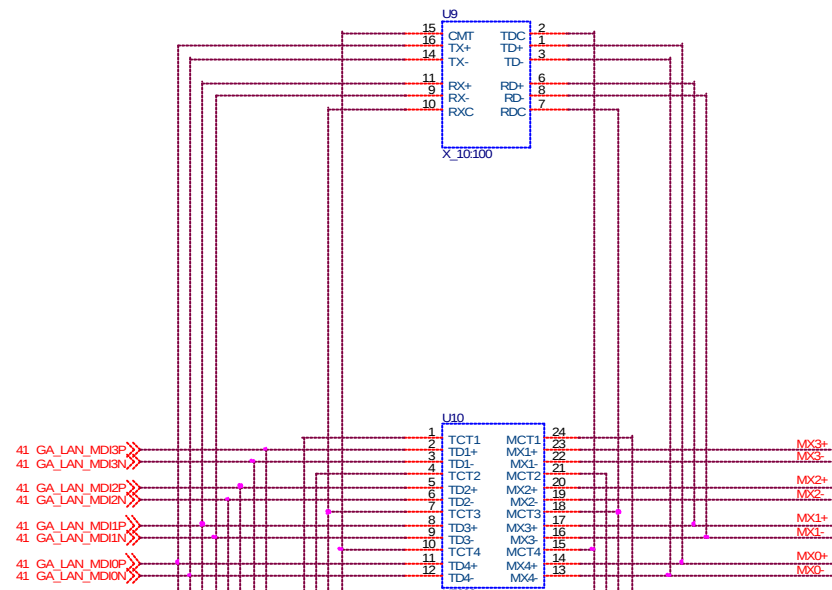
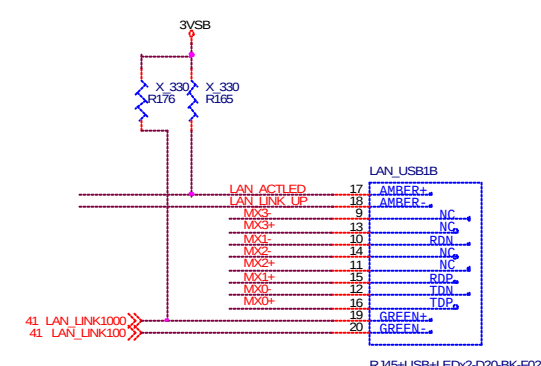
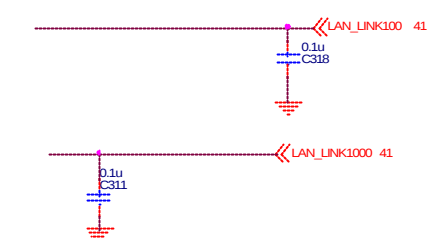


Micro Star Restricted Secret		
Title	ITP PORT & DLED	Rev
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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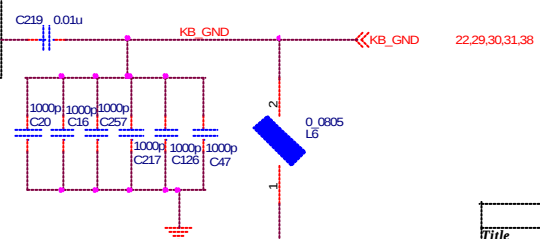
KENAI32 / LAVON DUAL LAYOUT.





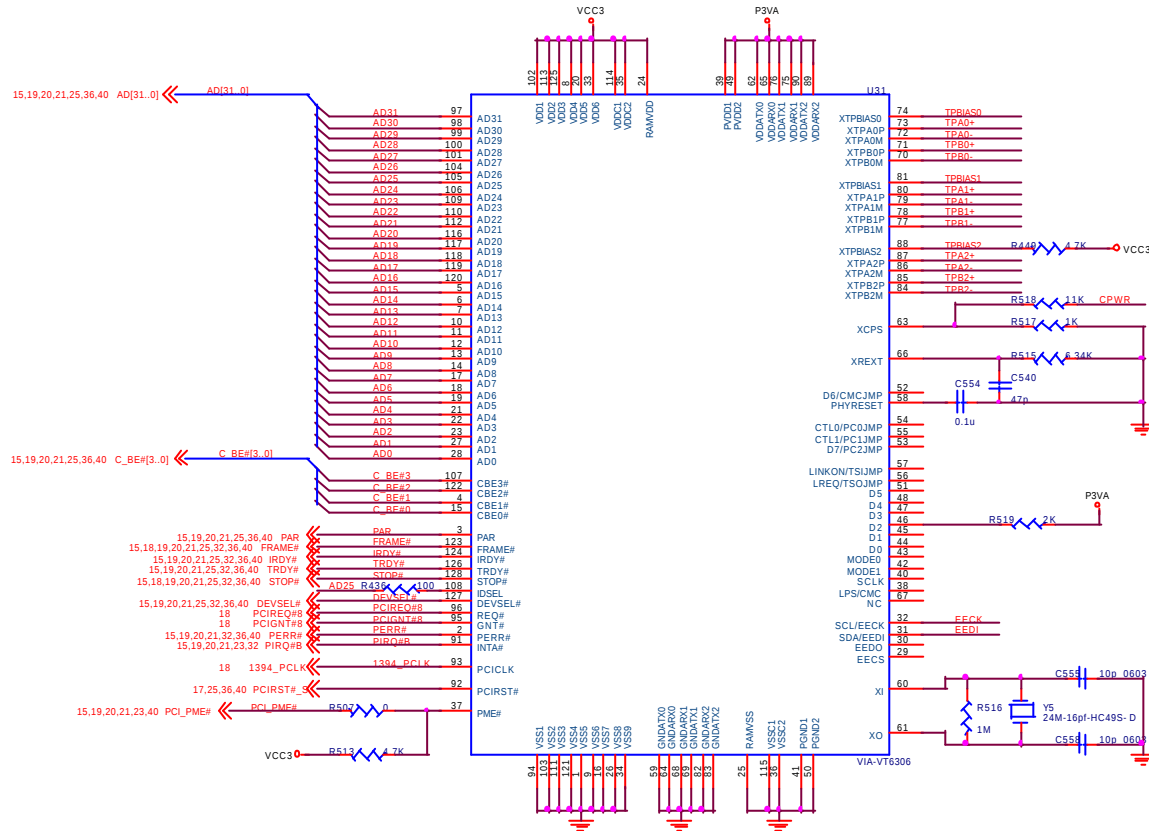


Reserved larger plane.



Micro Star Restricted Secret		
Title	LAN CONNECTOR	REV
Document Number	MS-6565-20	0A
MICRO-STAR INT'L No. 99, Sec. 2, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, July 11, 2002
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1394a OHCI Link Layer Controller



HISTORY

Version: 0A

12/21 update

1.Modified circuit review from 12/19/01
2.Add OVER-VOLTAGE circuit.

12/31 update

1.Add KENAI32 / LAVON dual layout mark
2.Modified LAN 2.5/1.5V power transistors toSOT 223
3.Modified LAN crystal capacitor to 22pF.
4.Add six capacitors between GIGA_GND andGND.
5.Add a Test Point in LAN chip pin M8

01/02 update

1.Change AGP slot to AGPPRO co-layout
2.Modified DQS_B and CB_B on termination for signalerror.
3.Separate SMBus to suspend and vcc_core.
4.Add SMBus on PCI slot 1.
5.Change LAN and USB connector.
6.Change LAN chip SMBALRT# to VRM_PG
7.Change ICH4 SMBALRT# toNC.
8.Add a Test Point on LAN CLK_VEW.
9.Remove an additional differential pair on LAN transformer.
10.Add 5 DDR_VTT and 16 V_DIMM bypass capacitors.
11.Remove OVP protection.
12.Remove Parallel port and serial port protectiondiodes.

01/04 update

1.Modified 33MHz to capacitor array.
2.Remove single gate on 32.768Khz.
3.Reserved a resistor on AC_BITCLK of codec.
4.Reserved some capacitors on Game Port and Audio header.
5.Add some capacitors around ATX power connector.

01/09 update

1.Swap pin of DIMM clk and termination.
2.Swap pin of I/O bypass and pullup.

01/14 update

1.Add 4 common mode chokes on USB port.
2.Disconnect BSEL1 and modified BSEL0 to F50.
3.Add CPU 400/533 select jumper.

01/15 update

1.Add LAN 1.5/2.5V control 100k pull-down resisors.
2.Add 10M resistor on SATA crystal.

01/17 update

1.Modified S-ATA circuit for silicon image suggest.
2.Add a circuit to trun off RSTRST# when 5VSB drop to36V. (Prevent VBAT drop too low when AC lose)

01/21 update

1.Modified LAN controller library to KENAI32/LAVON dualmark.
--

01/21 update

1.Change LANRST# to GPIO28
2.Delete external pull high of RTC crystal.

02/05 update

1.Left GRANITE BAY G2 pin as a floating pin.
2.Modified TESTHI pin pullup.

02/19 update

1.Add HA[32..35] for INTEL suggest.
2.Add some decoupling capacitor behindMCH

02/20 update

1.Delete resistors between LAN connector and transformer.
2.Add a test point of LAN chip M8 pin with an additionalGNDpad.

02/21 update

1.Change LAN power generated circuit.
2.Add a reserved connect between VRM_PG to ICH4 SMBALRT#.

02/21 update

1.LAN_GND is a separated GND below connector andtransformer.

Version: 0B

03/19 update

1.Add KENAI32 pin C12 to GND.
2.Add 10:100 transformer dual layout.
3.Modified DDR power on sequency in S3 to S0 state.
4.Change MCH core voltage to 15V.
5.Mdified transformer to connectorrouting.

Version: 0C

04/19 update

1.Modified AGP DBI_LO to B14 pin.
2.Add USB port 4,5
3.Add MCH pin G2 to GND.
4.Modified Hub link to 7:13
5.Modified AGP VREF to 0.35V when in AGP8X
6.Modified AGPRST# for NV17.
7.All PCI slot support ASF.

Version: 0D

05/09 update

1.Modified DDR,AGP,HunLink traces to meet INTEL new length matching file version0.9
2.Modified Gigabit LAN 2.5V/1.5V power trace and add more capacitors for better performance.
3.Add two resistors pull up to 3.3V in MCH J20,J21 pin.
4.Remove 1/100 transformer and change 1000 transformer toH5007.
5.Add SATA RAID enable/disable select.

05/30 update

1.Modified I/O shield to KB_GND.
2.Modified I/O shield to INTEL standard.
3.Modified 5VDUAL trace more wider forUSB20

06/06 update

1.Modified TESTSIG3,4 to pull up 24.9 ohm and divided 49.9 to100ohm.
2.Add 3 100UF SP cap to solder side beyond CPU socket.
3.Add model name " Jwo Shoei Shi " to TEXT side

Version 0D1

06/06 update

1.Create 0D1 version and rotate transformer to90 degree.
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Micro Star Restricted Secret		
Title	HISTORY	Rev 0A
Document Number	MS-6565-20	
MICRO-STAR INT'L 80664, No. 1, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, June 19, 2002 Sheet 44 of 45

