

MS-6564

SIS 645/650 CHIPSET

Willamette/Northwood 478pin mPGA-B Processor Schematics

VERSION : 10B

07/22/2002 Update

CPU:

Willamette/Northwood mPGA-478B Processor

System Chipset:

SIS 645/650 (North Bridge)
+961A (South Bridge)

On Board Chipset:

LPC Super I/O -- W83697HF
Clock Generation -- ICS952001AF
PCI SOUND -- C-MEDIA CMI8738MX
PCI 1394 --VIA VT6306

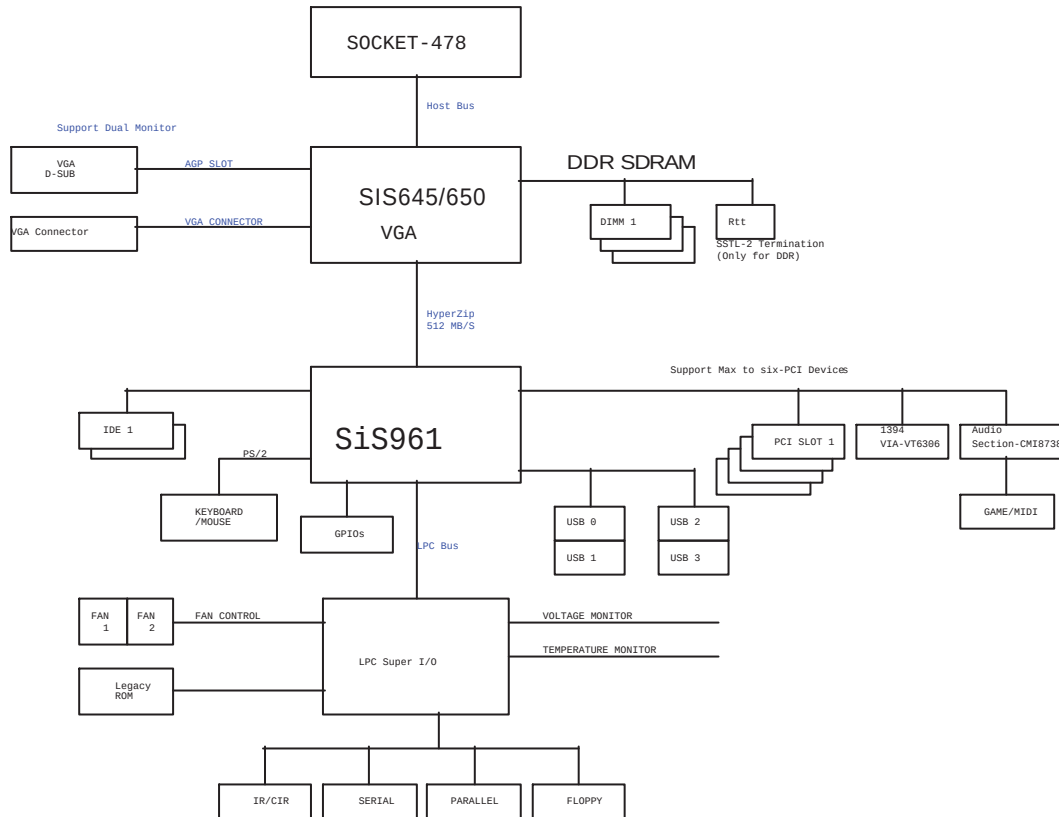
Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT* 4

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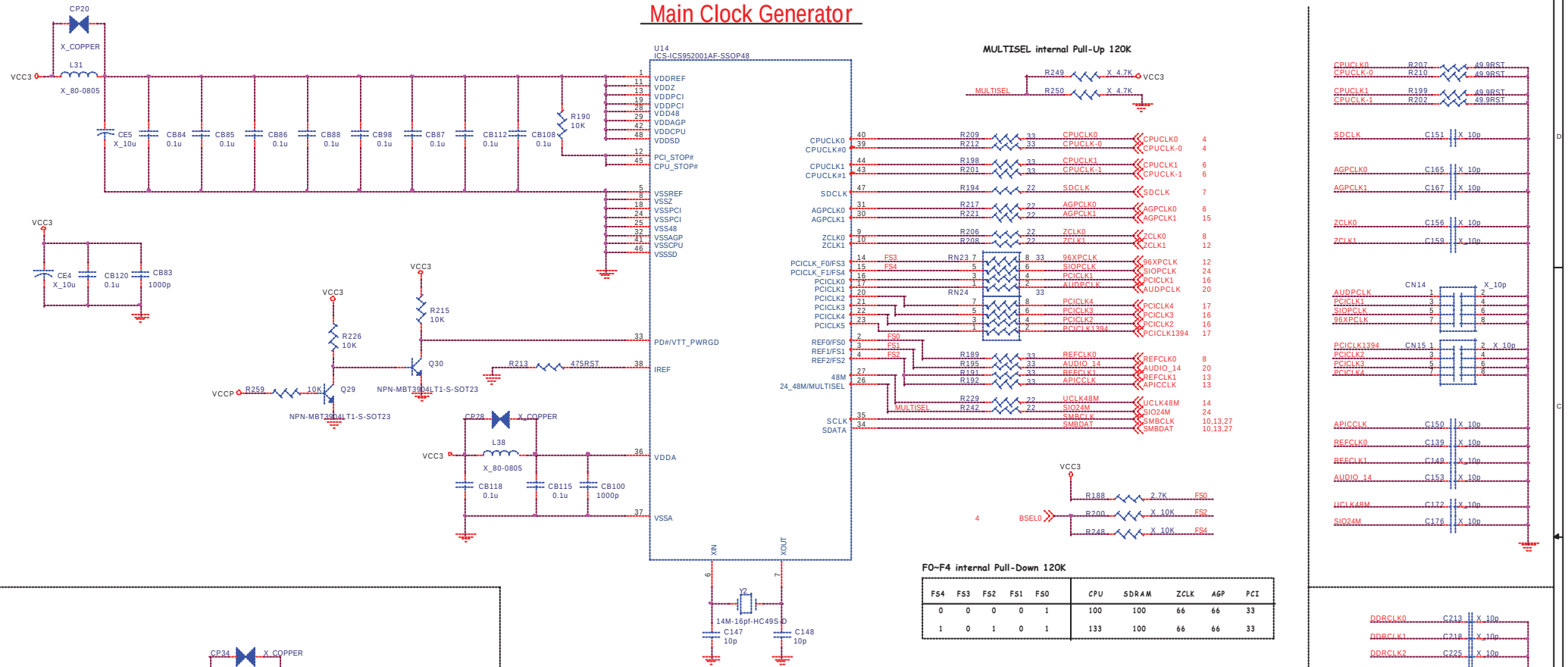
System Block Diagram



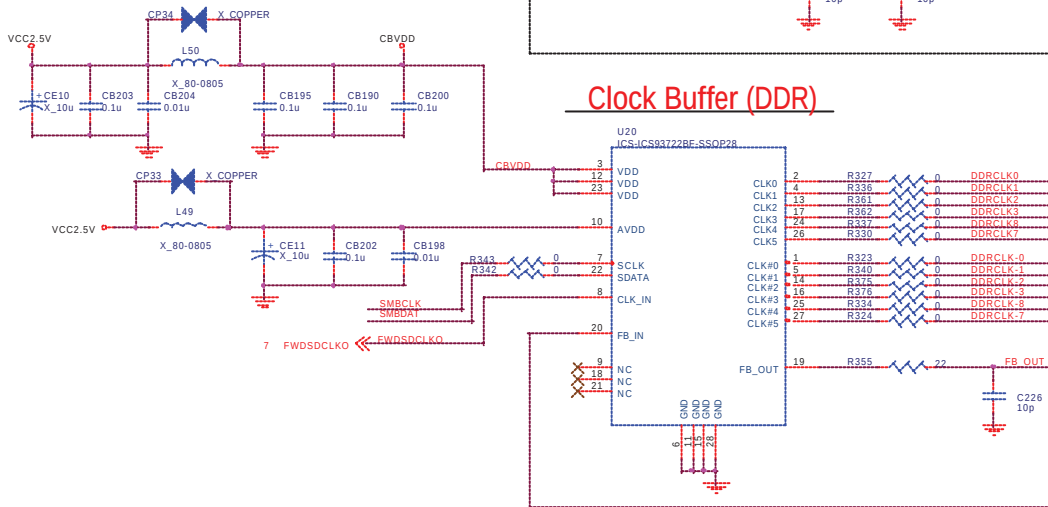
GPIO Table on SiS961

GPIO_0	I/O	MAIN	Pull-Up
GPIO_1	I/O	MAIN	Pull-Down
GPIO_2	I/O	MAIN	THERM#
GPIO_3	I/O	MAIN	EXTSMI#
GPIO_4	I/O	MAIN	Pull-Up
GPIO_5	I/O	MAIN	PREQ#5(Pull-Up)
GPIO_6	I/O	MAIN	PGNT#5(Pull-Up)
GPI_7	I/O	RESUME	Pull-Up
GPI_8	I	RESUME	RING
GPI_9	I	RESUME	RESERVED
GPI_10	I	RESUME	RESERVED
GPIO_11	I/O	RESUME	RESERVED
GPIO_12	I/O	RESUME	Pull-Up
GPIO_13	I/O	RESUME	Flash Rom protection H: Disable, L: Enable
GPIO_14	I/O	RESUME	LAN_WAKE#
GPIO_15	I/O	RESUME	KBDAT
GPIO_16	I/O	RESUME	KBCLK
GPIO_17	I/O	RESUME	MSDAT
GPIO_18	I/O	RESUME	MSCLK
GPIO_19	I/O	RESUME	SMBCLK
GPIO_20	I/O	RESUME	SMBDAT

Main Clock Generator

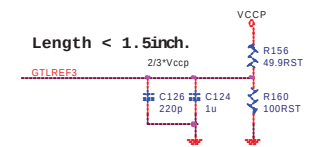
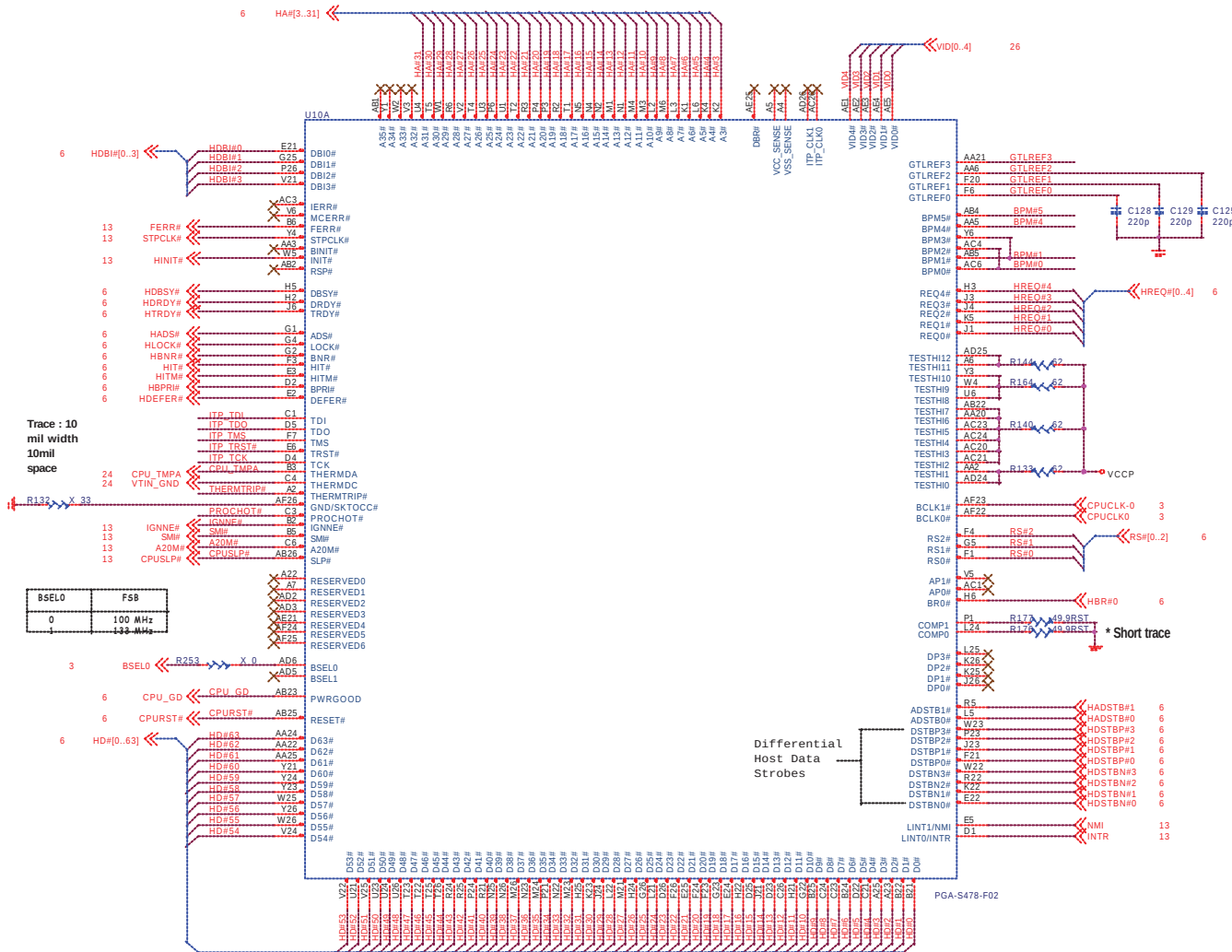


Clock Buffer (DDR)



FO-F4 internal Pull-Down 120K

F54	F53	F52	F51	F50	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	1	100	100	66	66	33
1	0	1	0	1	133	100	66	66	33



ITP TMS R167 39
ITP TDO R168 75
ITP TCK R172 27

VCCP

Signal	Pin	Value	Supply
PROCHOT#	R175	82	VCCP
CPU_GD	R145	82	
HBR9D	R205	220	
CPURST#	R159	49.9R5	
TPM2TRST#	R203	82	
RFPM4D	R139	49.9R5	VCCP
RFPM1#	R142	49.9R5	
RFPM3#	R157	49.9R5	
RFPM5#	R155	49.9R5	
ITP_TDI	R204	150	VCCP
ITP_TRST#	R170	880	VCCP
CPU_GD	C121	X 1000P	
CPURST#	C123	X 1000P	
CPUSLP#	C122	X 0.022u	

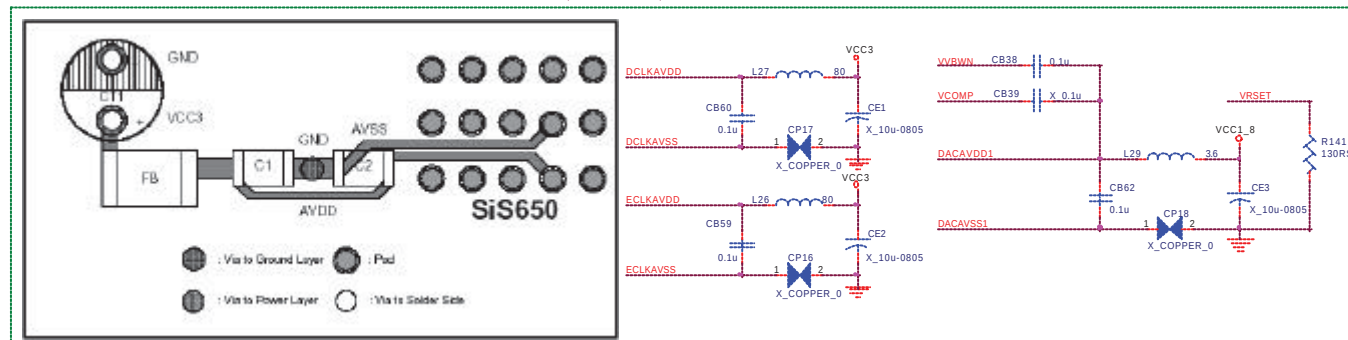
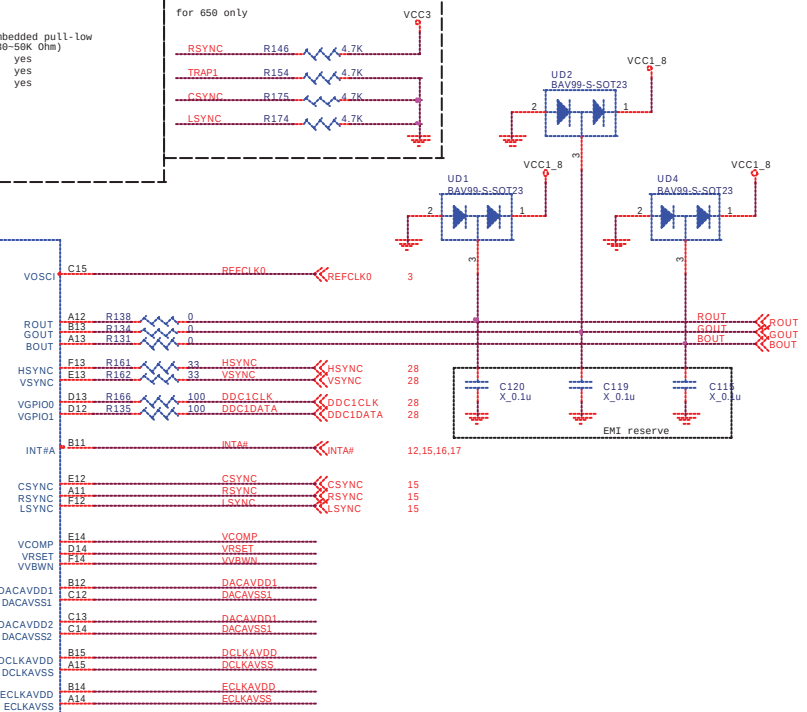
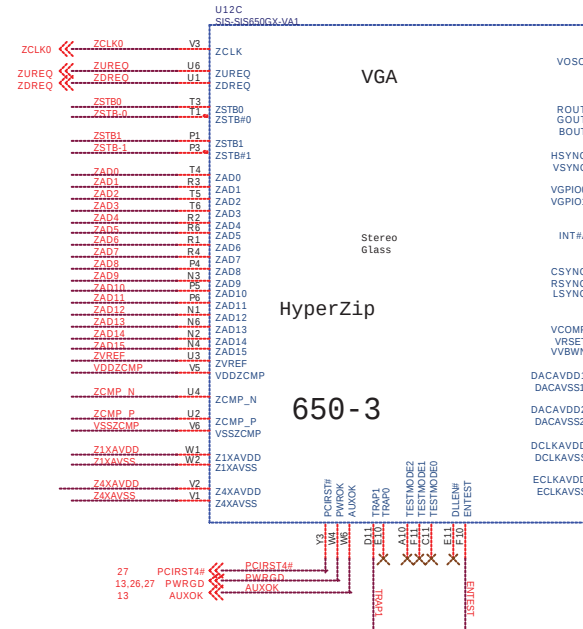
NB Hardware Trap Table			
	0	1	Default
DLEN#	enable PLL	disable PLL	0
DRAWN_SEL	SDR	DDR	1 (DDR)
TRAP0	normal	NB debug mode	0

TRAP1	TV selection, NYSCTPAL (87.1)	0
CSYNC	enable VB	0
RSYNC	enable VGA interface	1
LSYNC	enable panel link	0

embedded pull-low (30-50K Ohm)

for 650 only

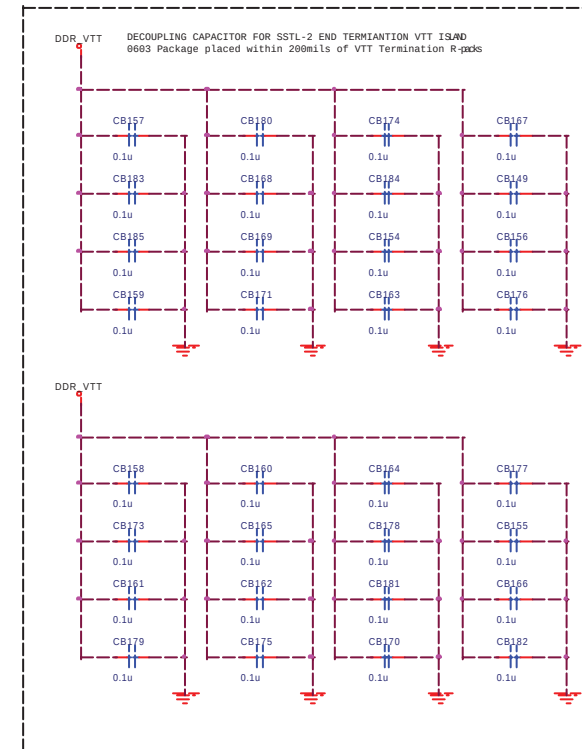
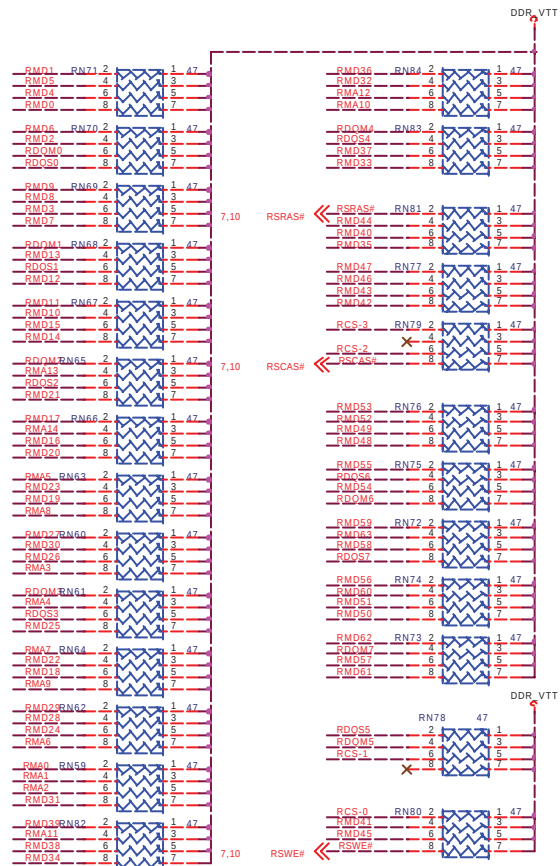
The diagram shows four pull-down resistors connected to a common VCC3 rail. The resistors are labeled R146, R154, R175, and R174. The nodes they connect are RSYNC, TRAP1, CSYNC, and LSYNC respectively. Each resistor has a value of 4.7K.

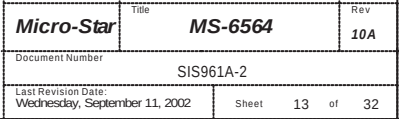


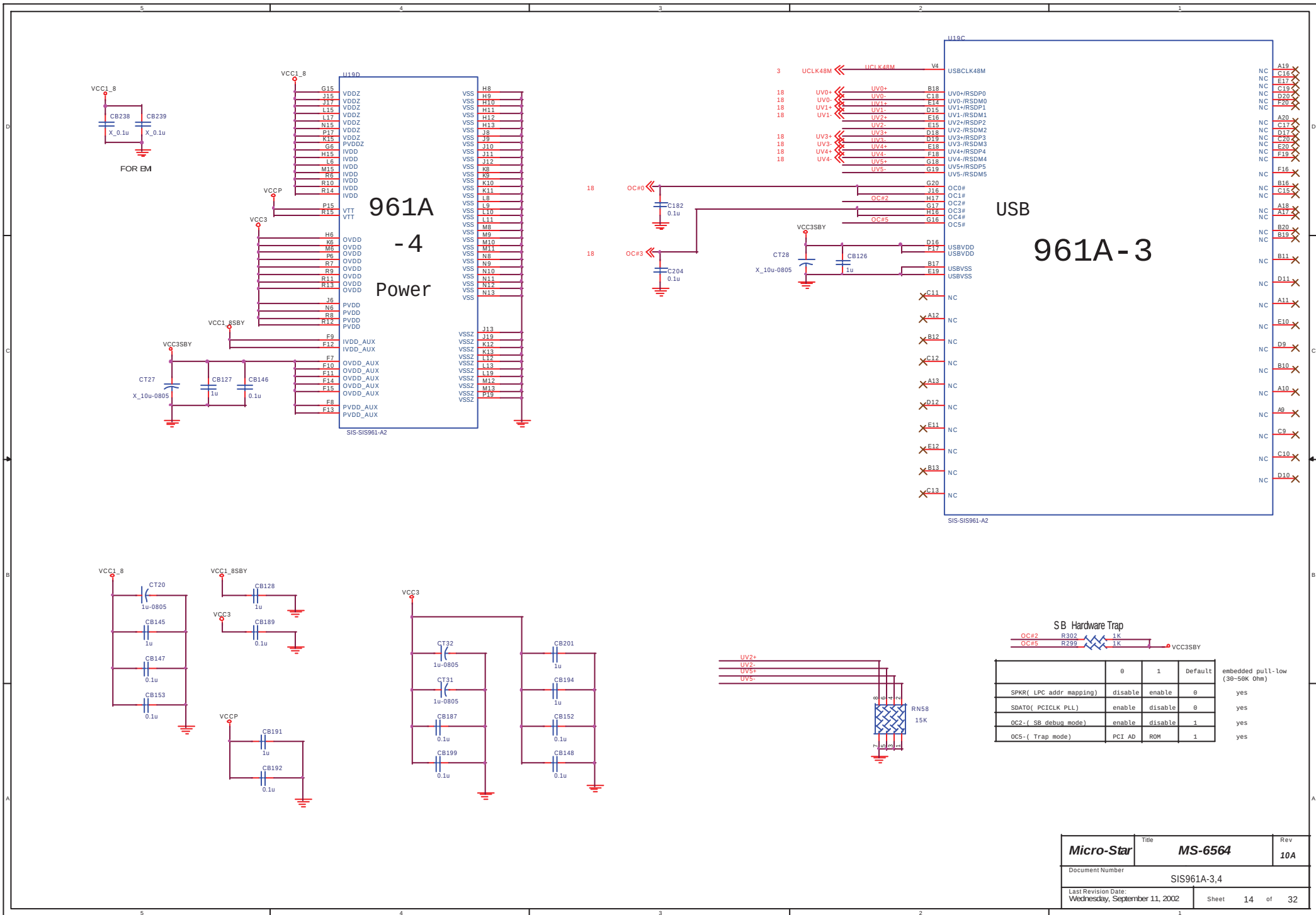
SSTL-2 Termination Resistors

Signal	Termination	Value	Location	Value	Location
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	RLT
MA/Control	LV-CMOS	0	SSTL-2	9	RLT
CS	LV-CMOS	0	SSTL-2	9	RLT
CKE	DD 3.3V	0	DD 2.5V	9	RLT

7.10 RMD[0..63]	← RMD[0..63]	7.10 RCS[0..5]	← RCS[0..5]
7.10 RMA[0..14]	← RMA[0..14]	7.10 CKE[0..3]	← CKE[0..3]
7.10 RDQM[0..7]	← RDQM[0..7]	3.10 DDRCLK[0..8]	← DDRCLK[0..8]
7.10 RDQS[0..7]	← RDQS[0..7]	3.10 DDRCLK[0..8]	← DDRCLK[0..8]







6 SBA[0..7] << SBA[0..7]
 6 ST[0..2] << ST[0..2]
 6 ACBE#[0..3] << ACBE#[0..3]
 6 AAD[0..31] << AAD[0..31]
 6 ADSTB[0..1] << ADSTB[0..1]
 6 ADSTB# [0..1] << ADSTB# [0..1]

12,16,17 INTB# << INTB#
 3 AGPCLK1 << AGPCLK1
 6 AREQ# << AREQ#

6 RBF# << RBF#

6 SBSTB << SBSTB

AAD31
 AAD29
 AAD27
 AAD25
 ADSTB1
 AAD23

AAD21
 AAD19
 AAD17
 ACBE#2

6 AIRDY# << AIRDY#

8 CSYNC << CSYNC

6 ADEVSEL# << ADEVSEL#

6 ASERR# << ASERR#

AAD14
 AAD12
 AAD10
 AAD8
 ADSTB0
 AAD7
 AAD5
 AAD3
 AAD1
 AVREFCG

VCC3SBY
 VCC5
 VDDQ
 VCC3

VDDQ

VCC3

VDDQ

VCC3

VDDQ

VCC3

VDDQ

VCC3

VDDQ

VCC3

VDDQ

VCC3

VDDQ

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VDDQ

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VCC3

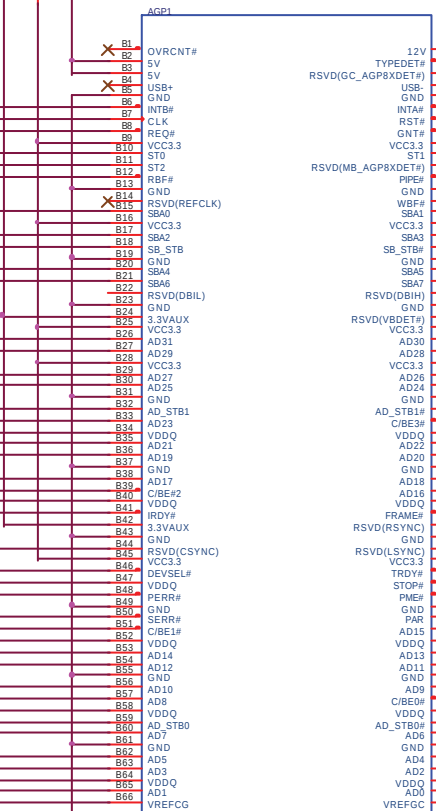
VDDQ

VCC3

VDDQ

VCC3

VDDQ



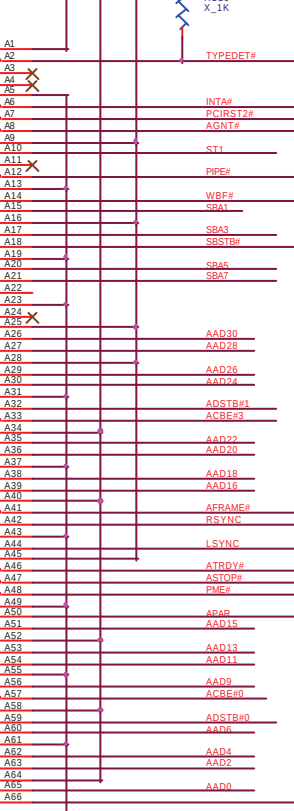
AGP CONNECTOR DECOUPLING

VCC3SBY

VCC3

VCC3

VCC3



VCC3

VCC3

VCC3

VCC3

VCC3

VCC3

VDDQ

VDDQ

VDDQ

VDDQ

VDDQ

VDDQ

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VDDQ

VDDQ

8,12,16,17
 16,17,27
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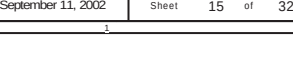
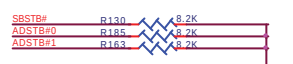
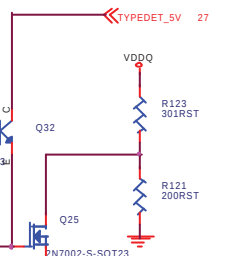
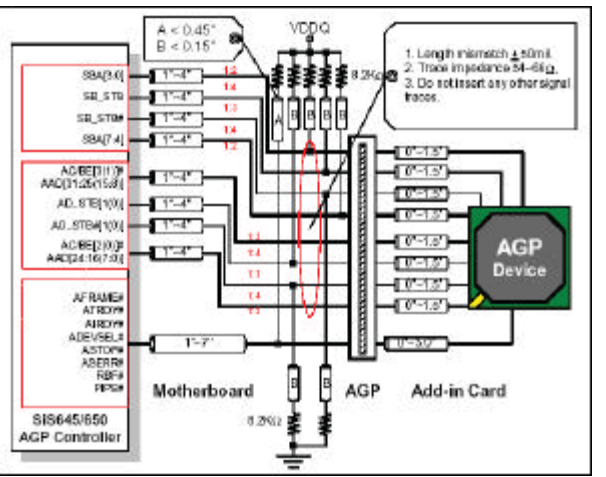
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6

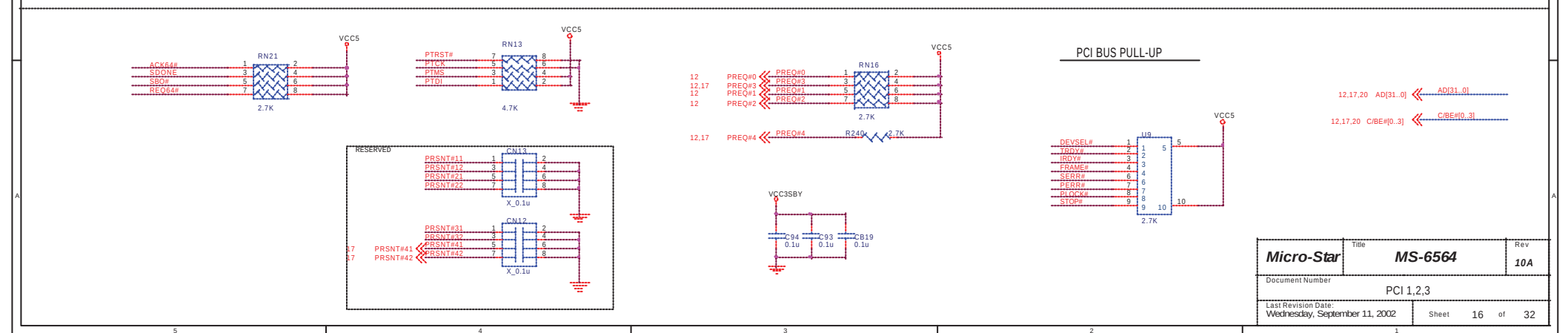
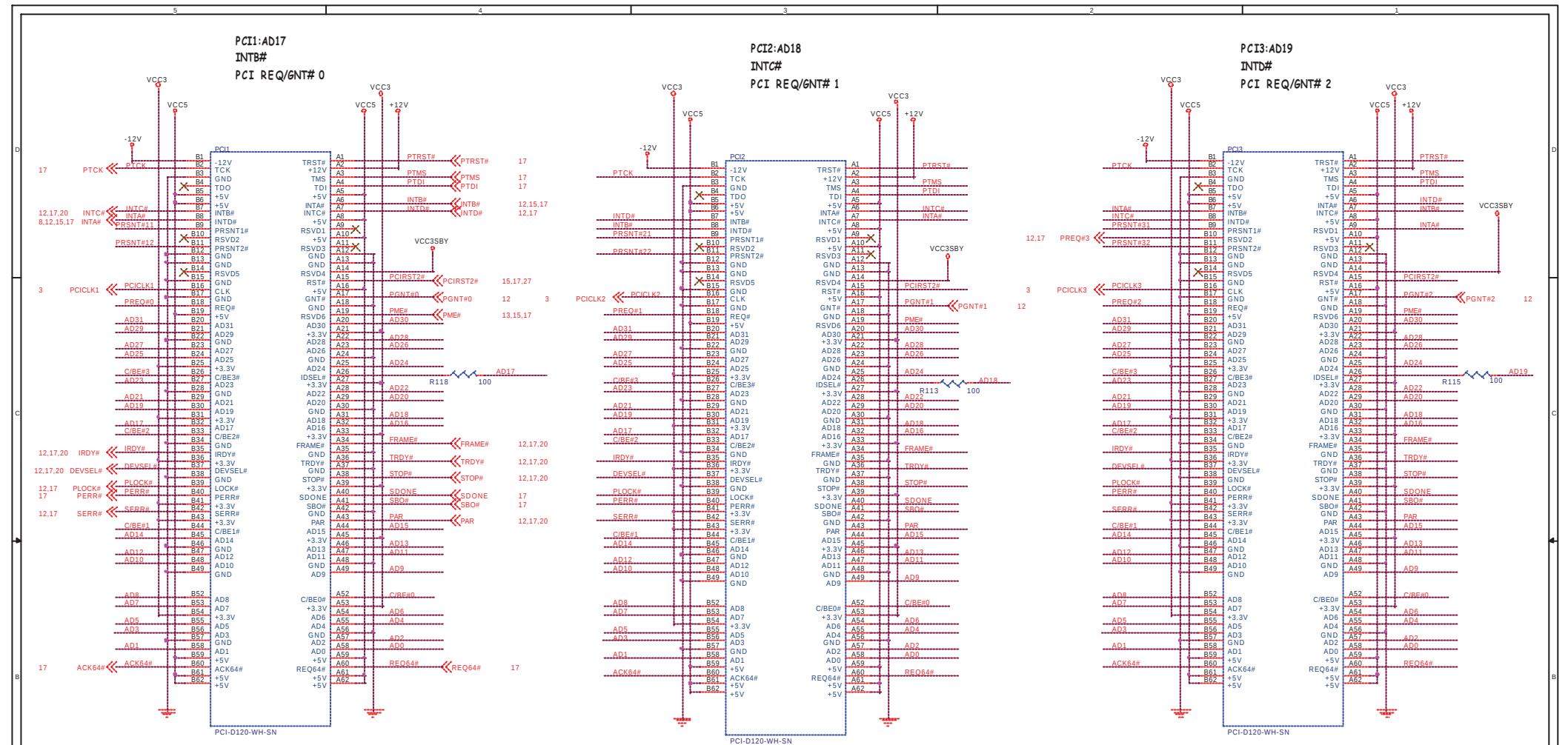
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6

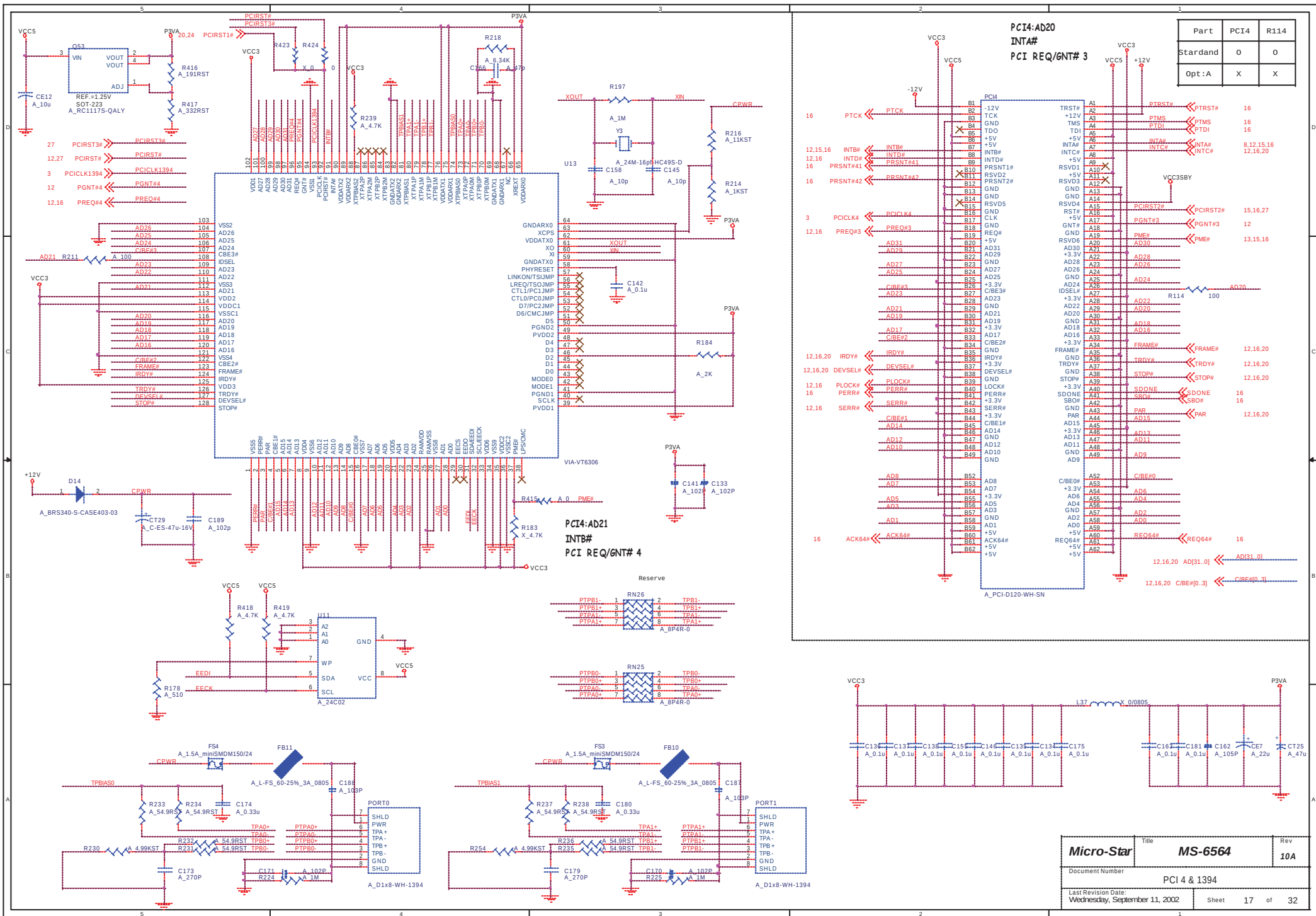
6



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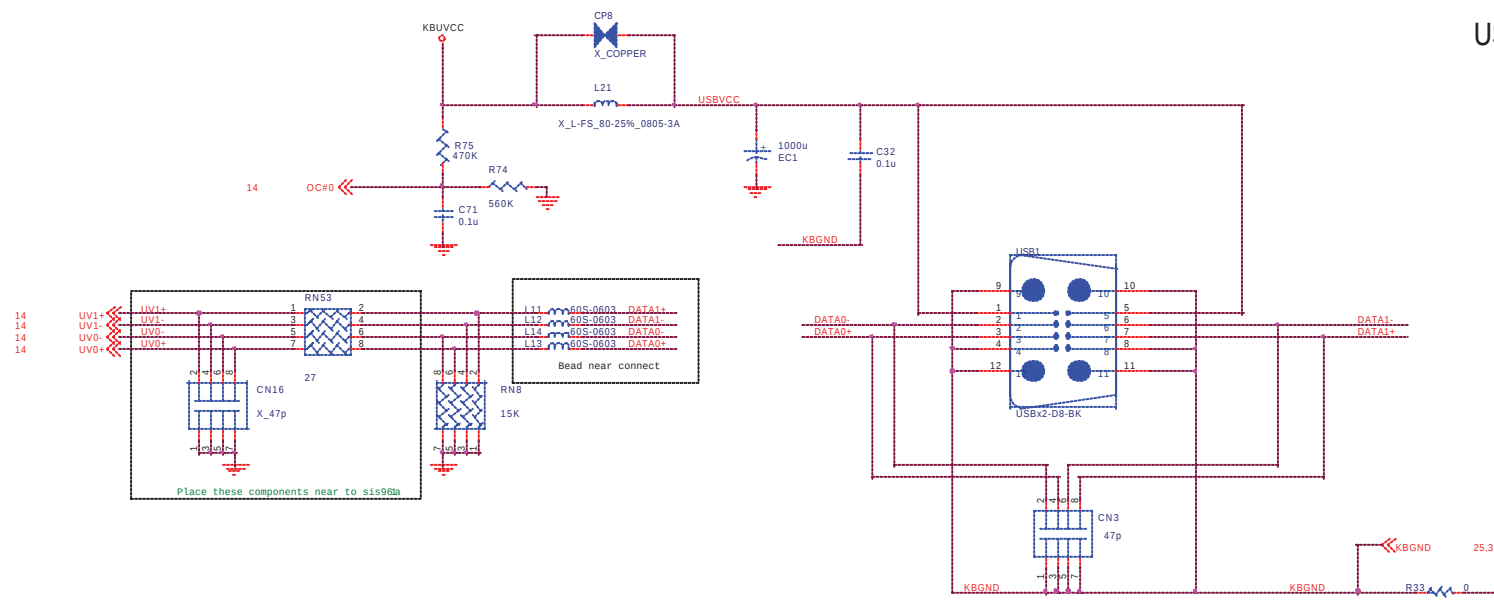


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PCI 1,2,3			
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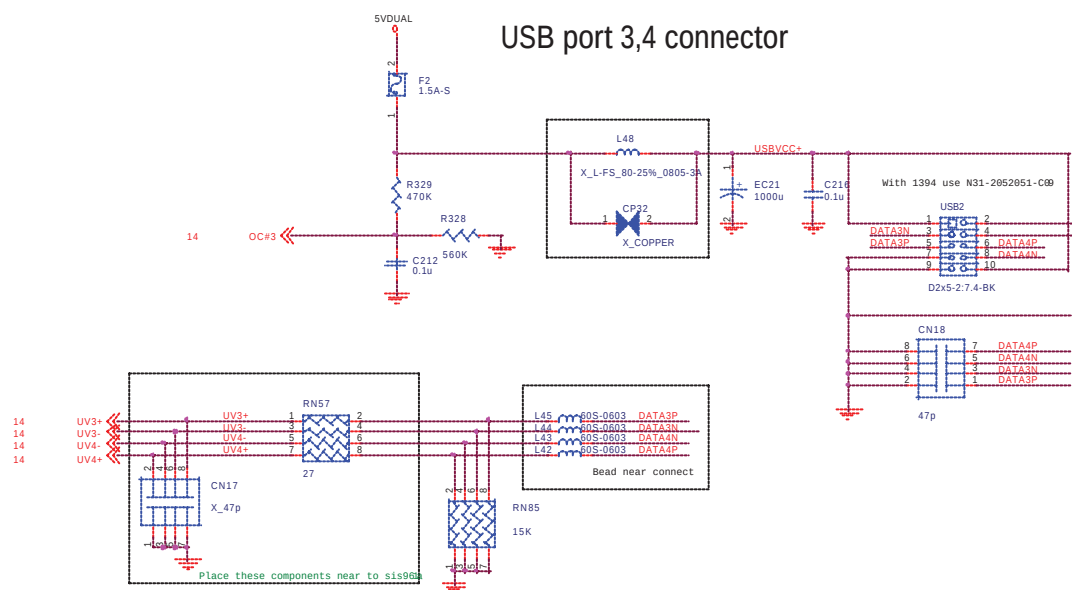


Part	PCI4	R114
Standard	O	O
Opt:A	X	X

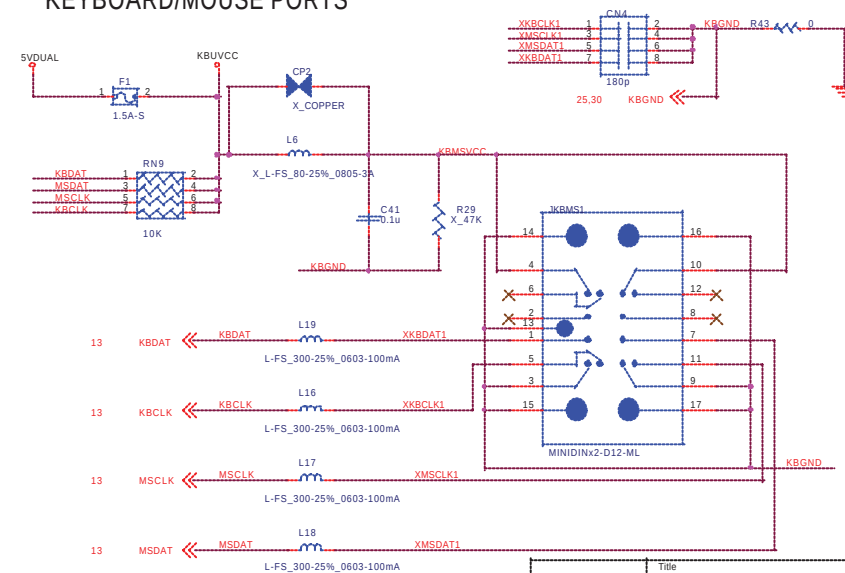
USB port 1,2 connector

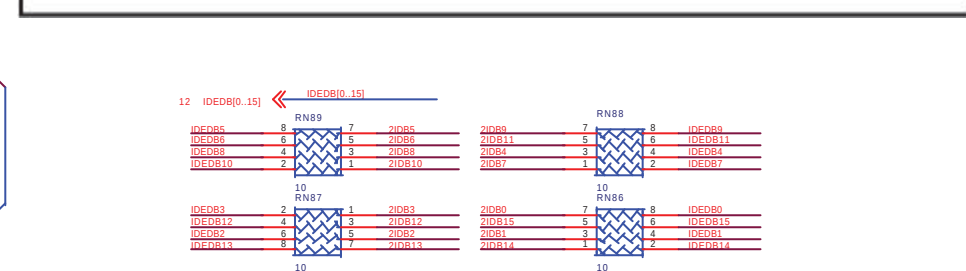
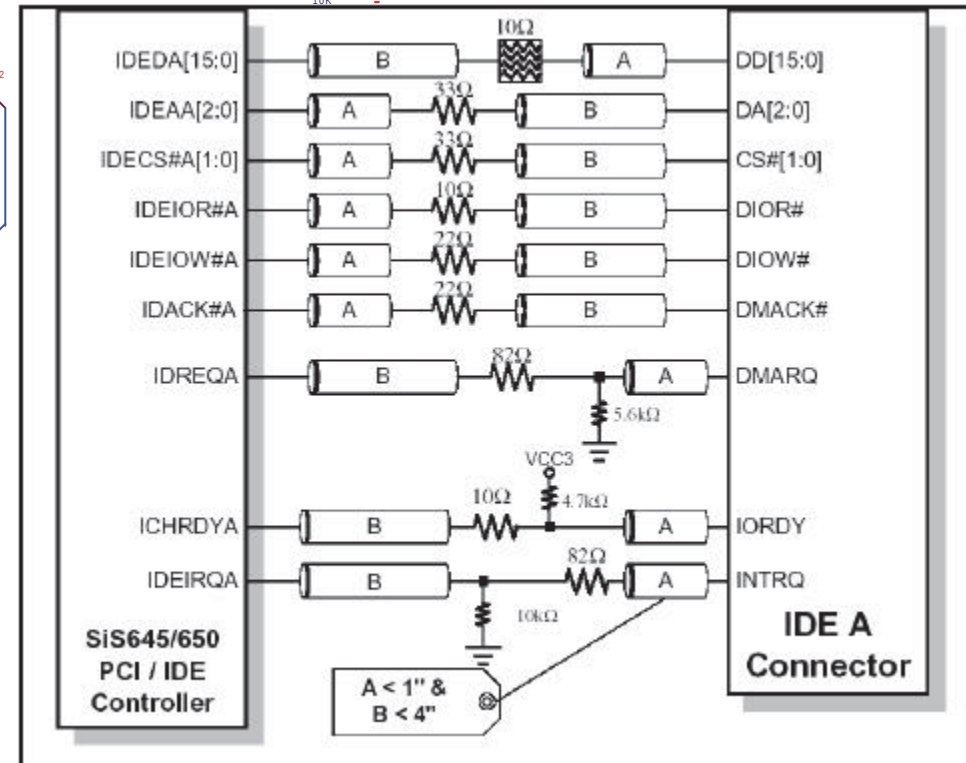
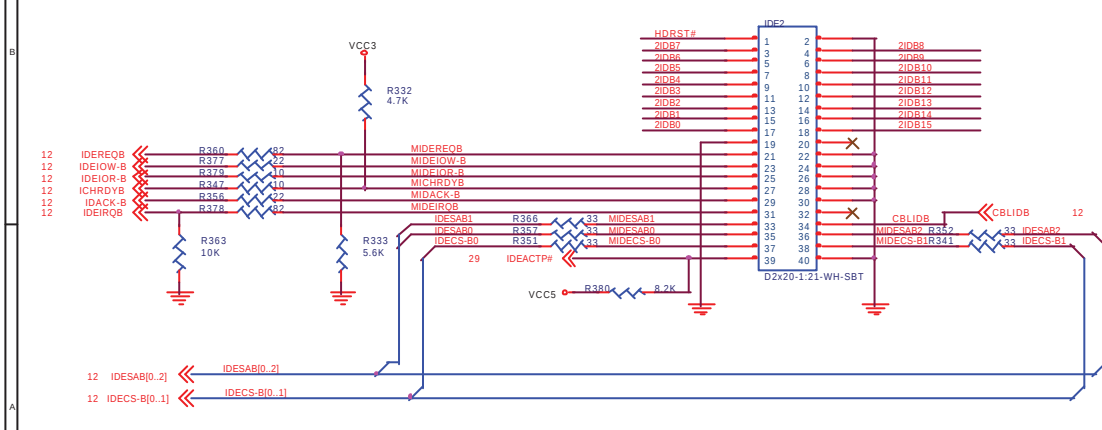
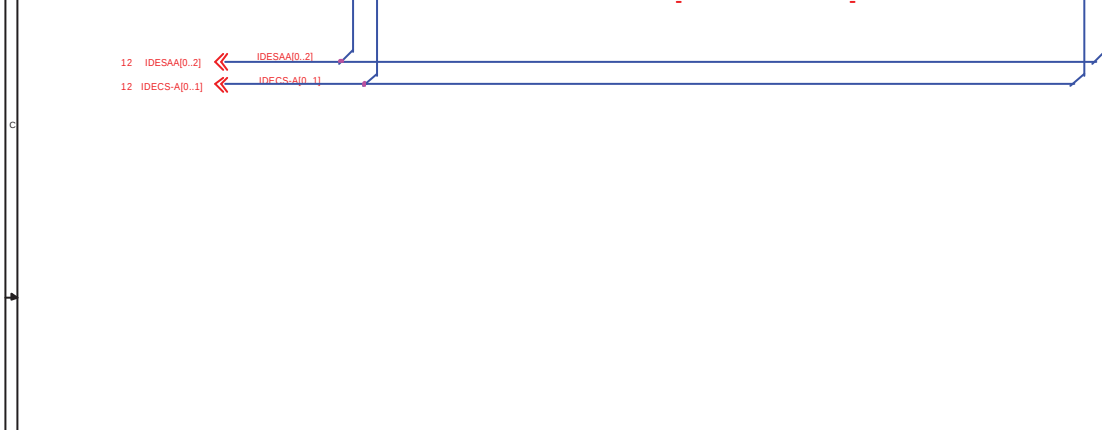
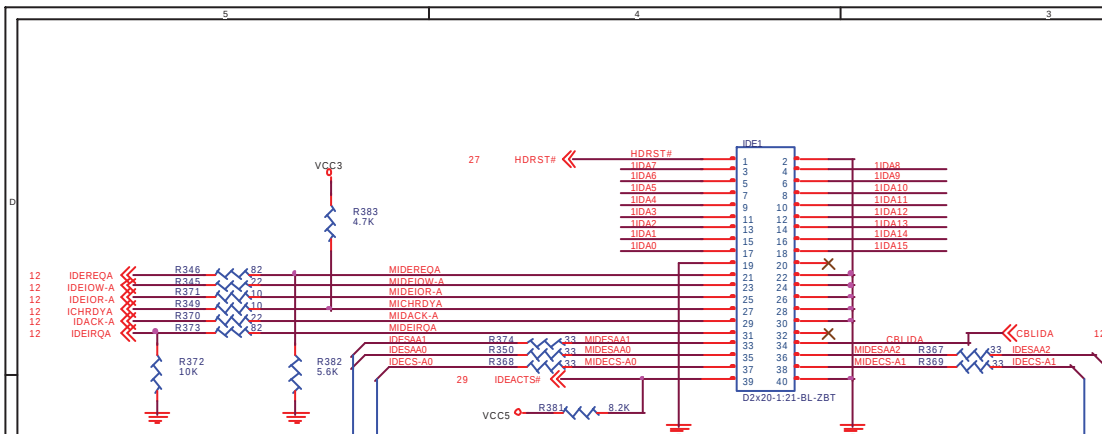


USB port 3,4 connector



KEYBOARD/MOUSE PORTS





C-MEDIA CMI8738MX PCI AUDIO

SOFTWARE CONTROL
HI=6CHANNEL

21 6CH_CTRL

C168 near U19 pin81,88

PCI4:AD22
INTC#
PCI REQ/GNT# 5

U3
<1ST PART FIELD>

4 Channel need 270P CAP

6 Channel NC 104P CAP

JP6 HIW AUDIO	
1-2	DISABLE
2-3	ENABLE *

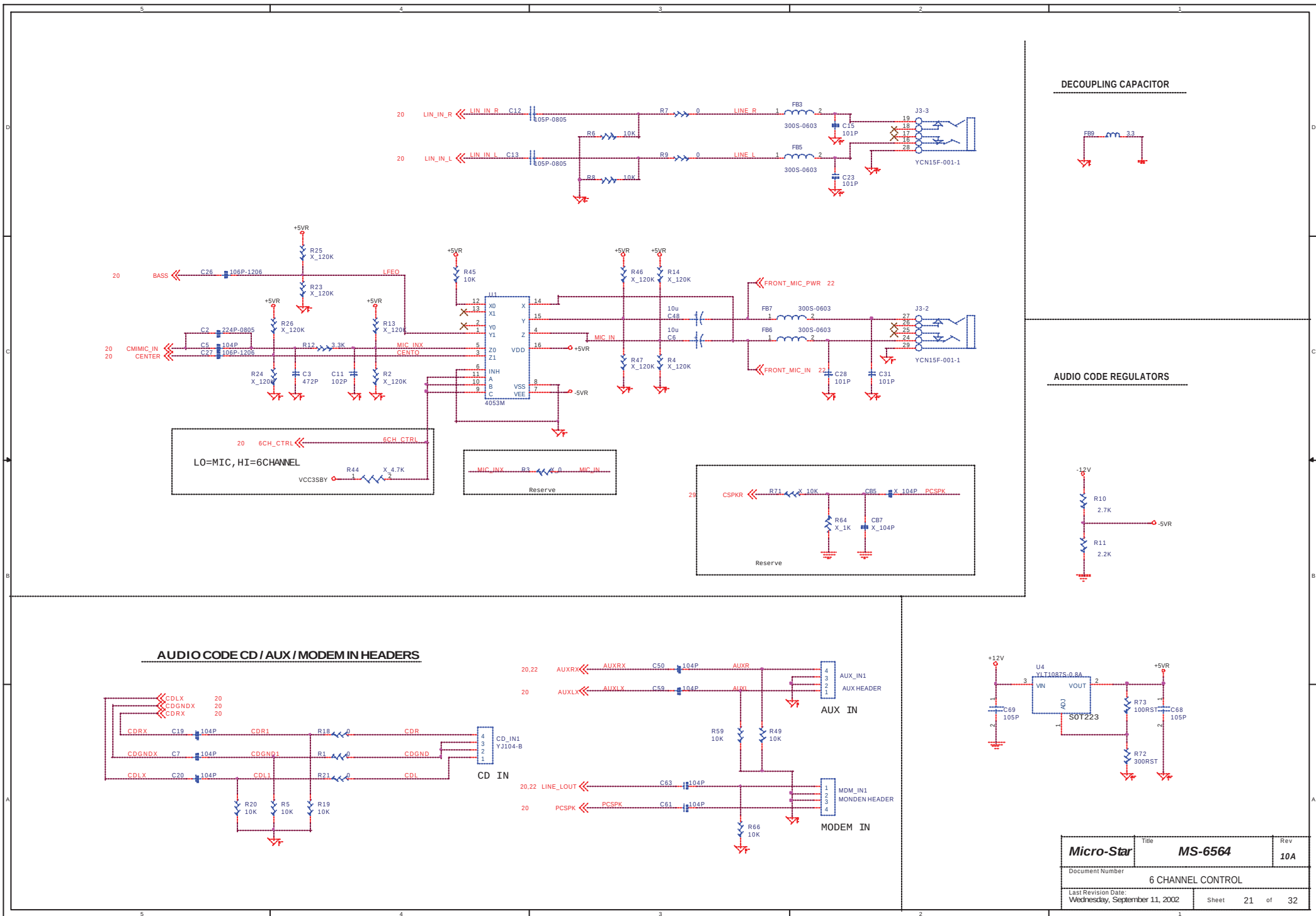
From M/B South Bridge GPIO CONTROL
ENABLE

* MBCSZ : AUDIO CHIP SELECT
HI : DISABLE
LOW : ENABLE

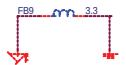
Internal ID
Selection

4 Channel Chipset use 5V
6 Channel Chipset use 3.3V

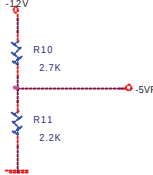
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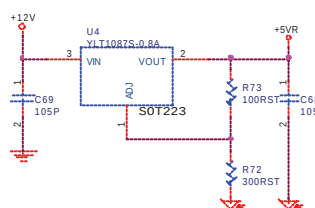
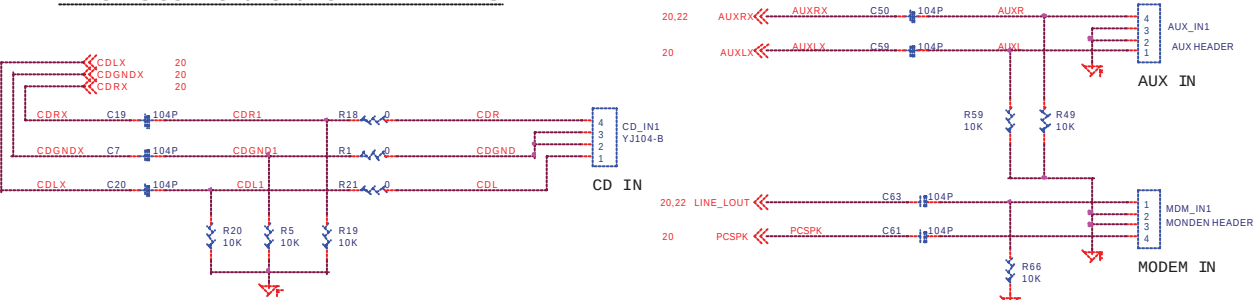
DECOUPLING CAPACITOR



AUDIO CODE REGULATORS

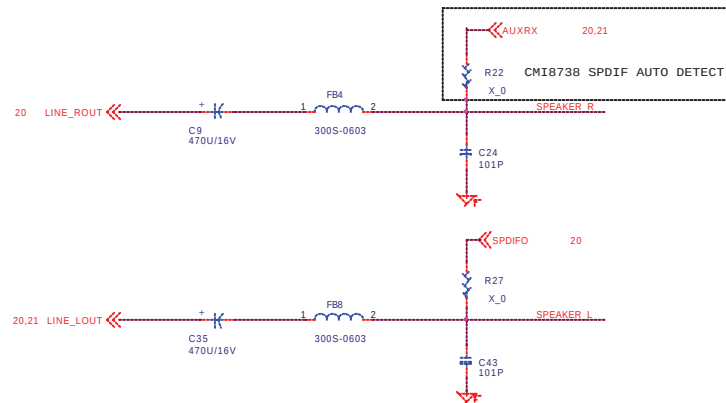


AUDIO CODE CD / AUX / MODEM IN HEADERS

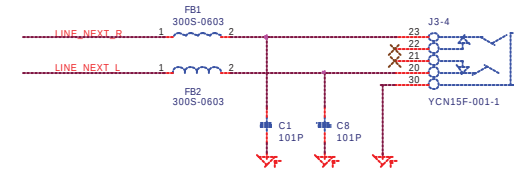


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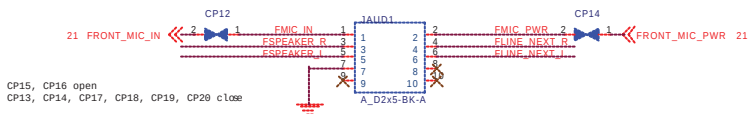
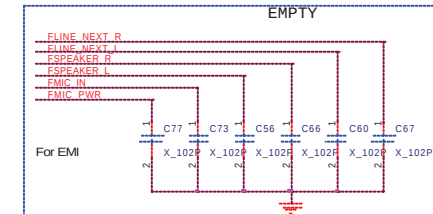
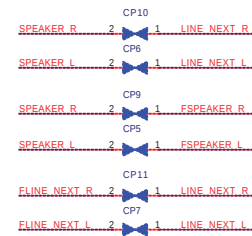
SPEAKER OUT CIRCUIT



SPEAKER OUT JACK



FOR MSI INTERNAL HEADER

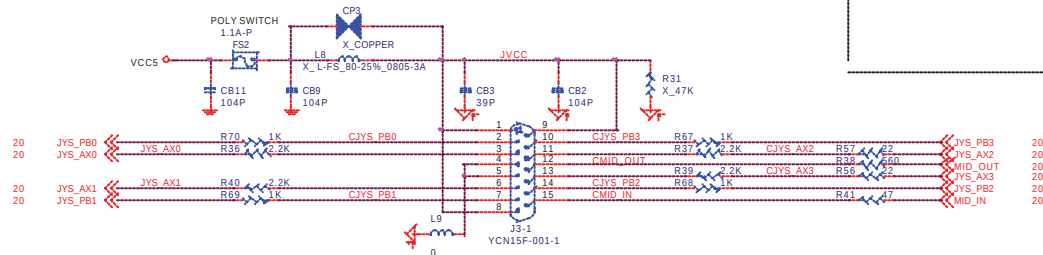
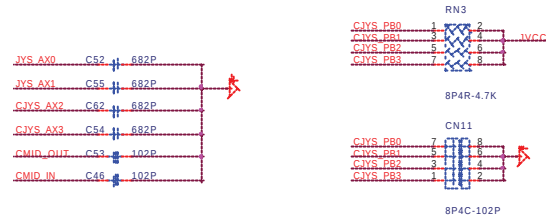


CP15, CP16 open
CP13, CP14, CP17, CP18, CP19, CP20 close

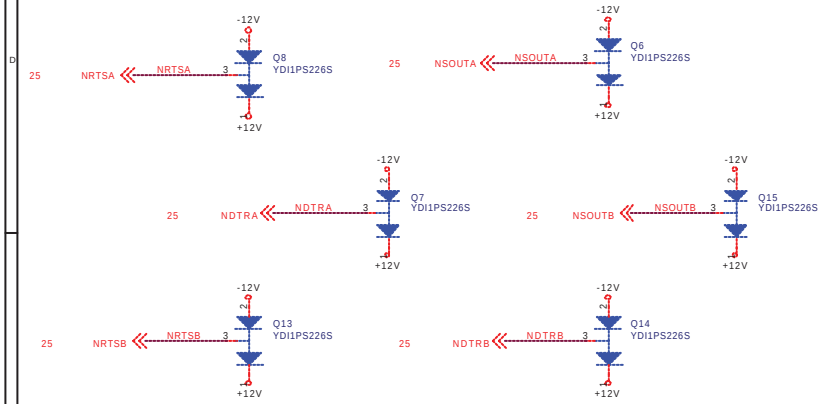


Part	R65	R48	Jaud1	C77	C73	C56	C66	C60	C67
Standard	X	X	0	X	X	X	X	X	X
Opt:A	X	X	0	X	X	X	X	X	X

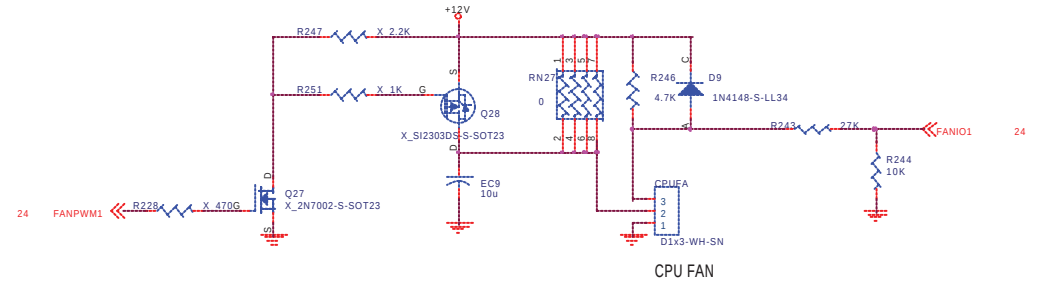
GAME/MIDI CONNECTOR



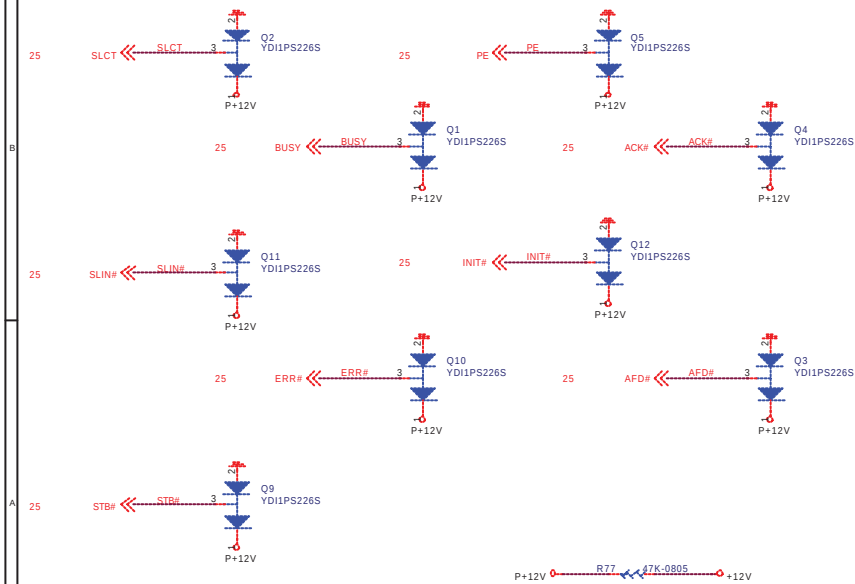
Serial port protection diode



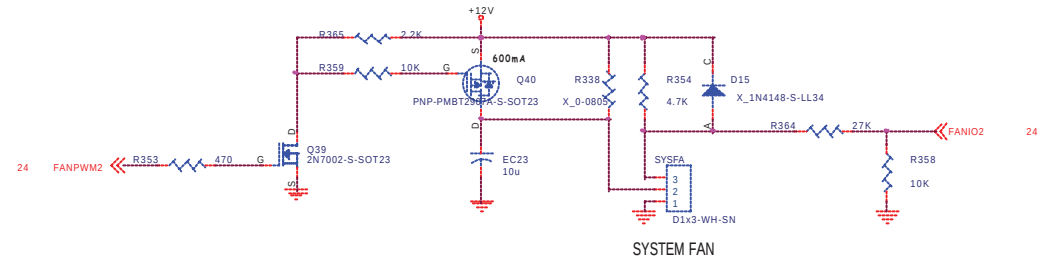
CPU FAN



Parallel port protection diode

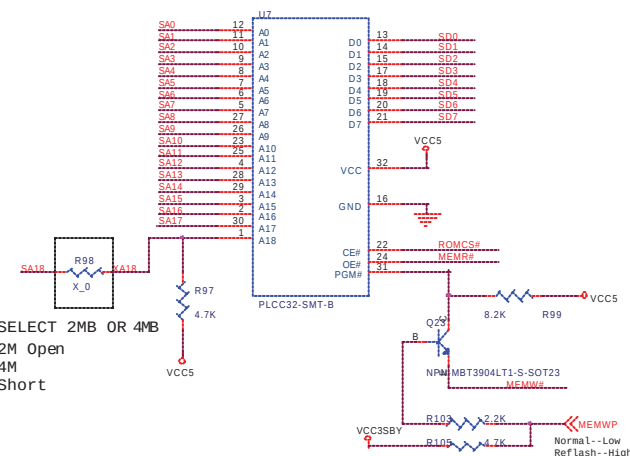


SYSTEM FAN

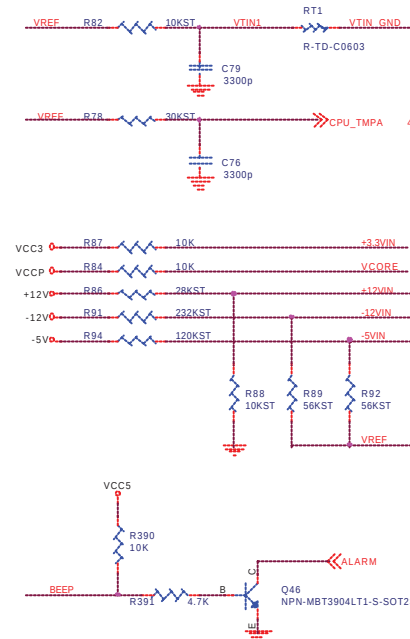


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Flash Rom



Hardware Monitor



configuration I/O port s address : 2EH

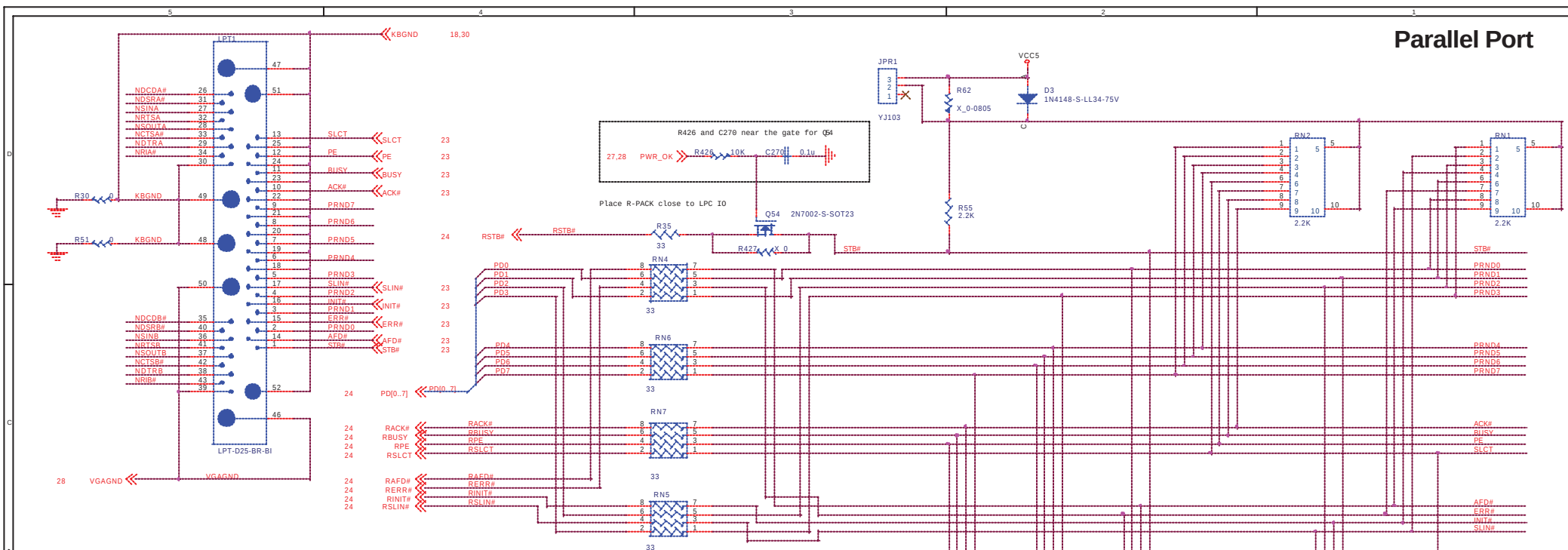
W83697HF

Default is 24MHz input

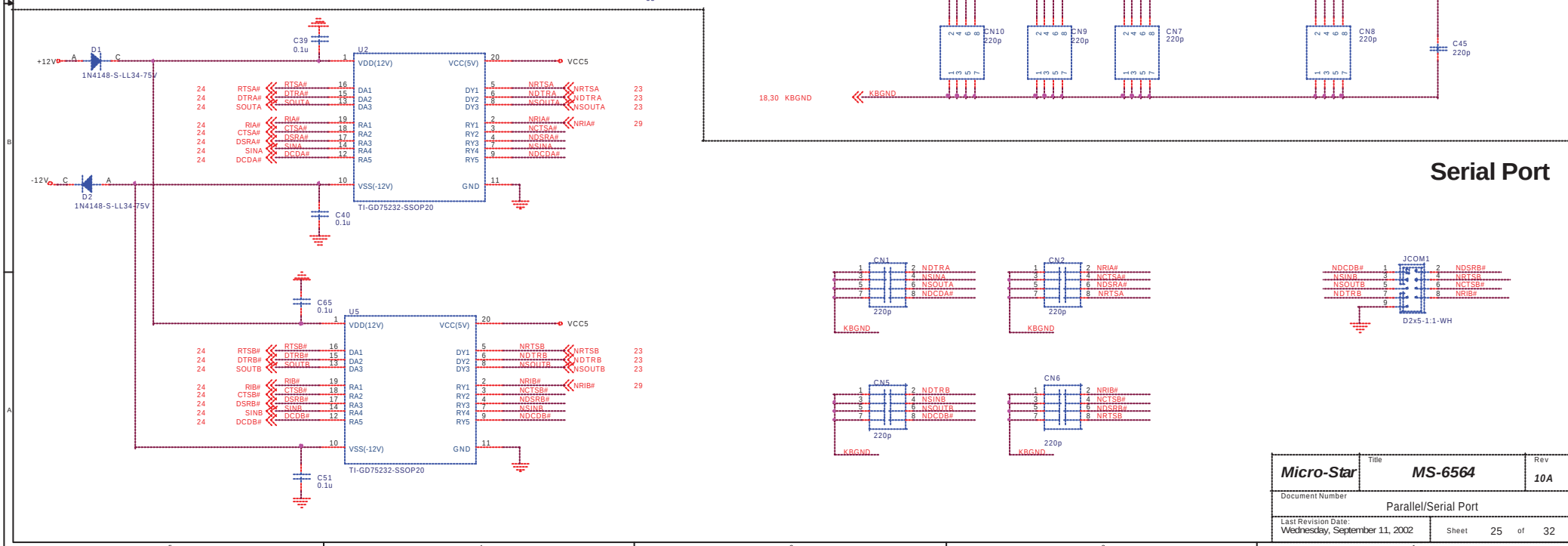
PO EXCH POWER PIN PLACE ONE CAP CLOSE TO

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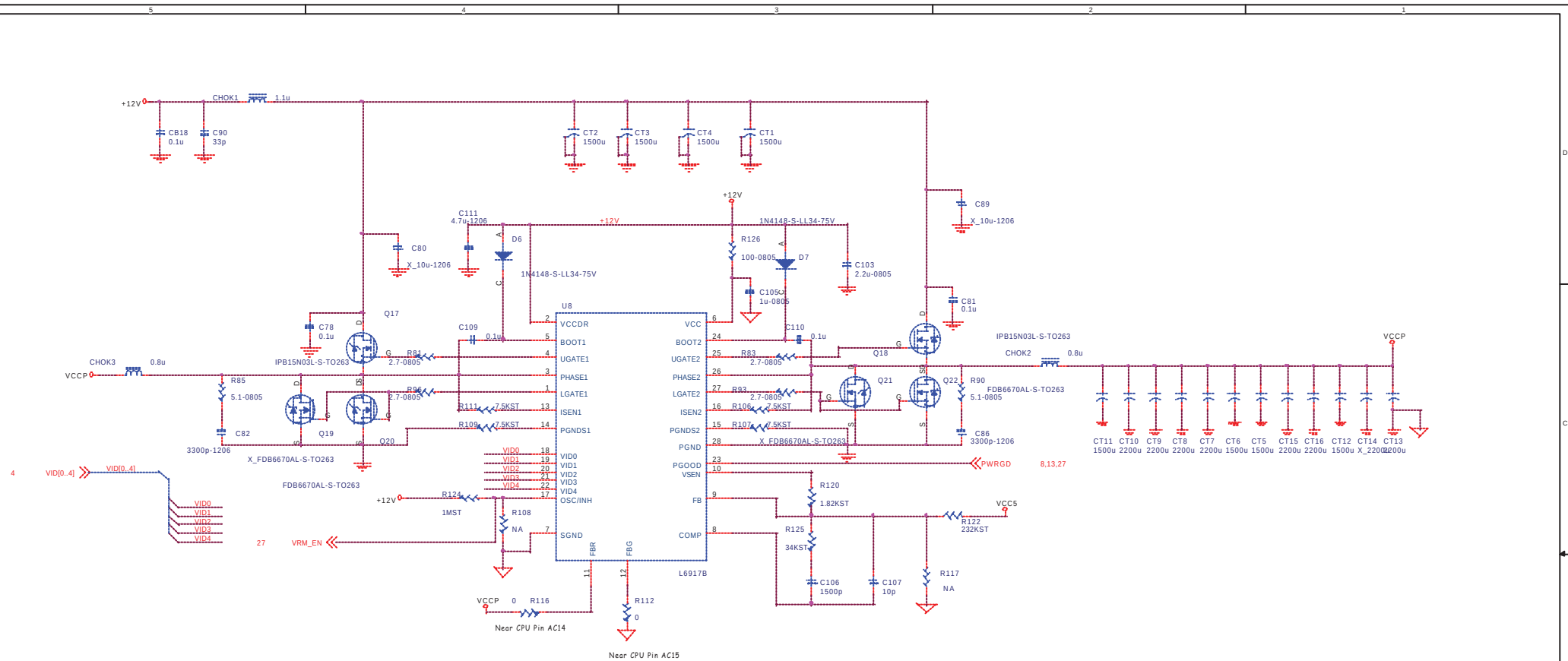
Parallel Port



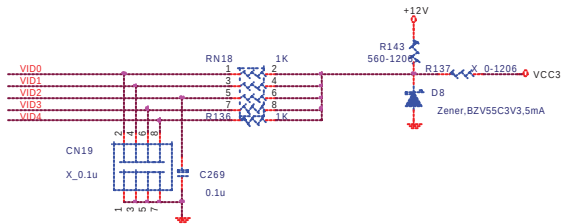
Serial Port



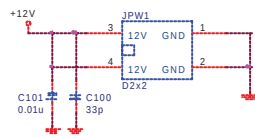
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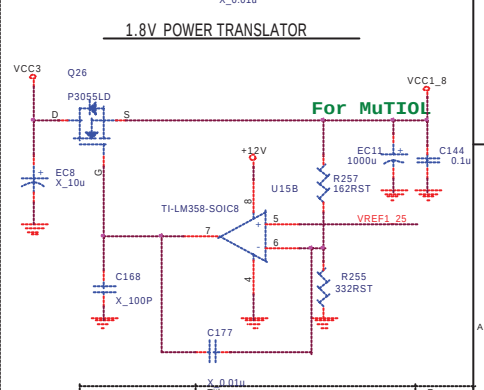
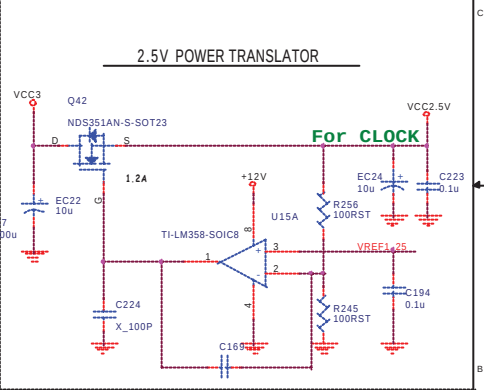
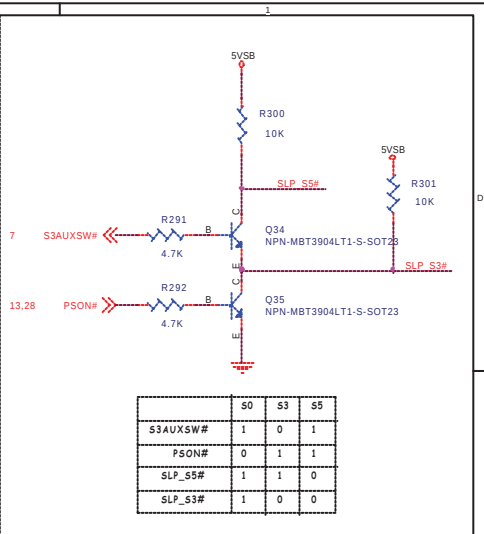
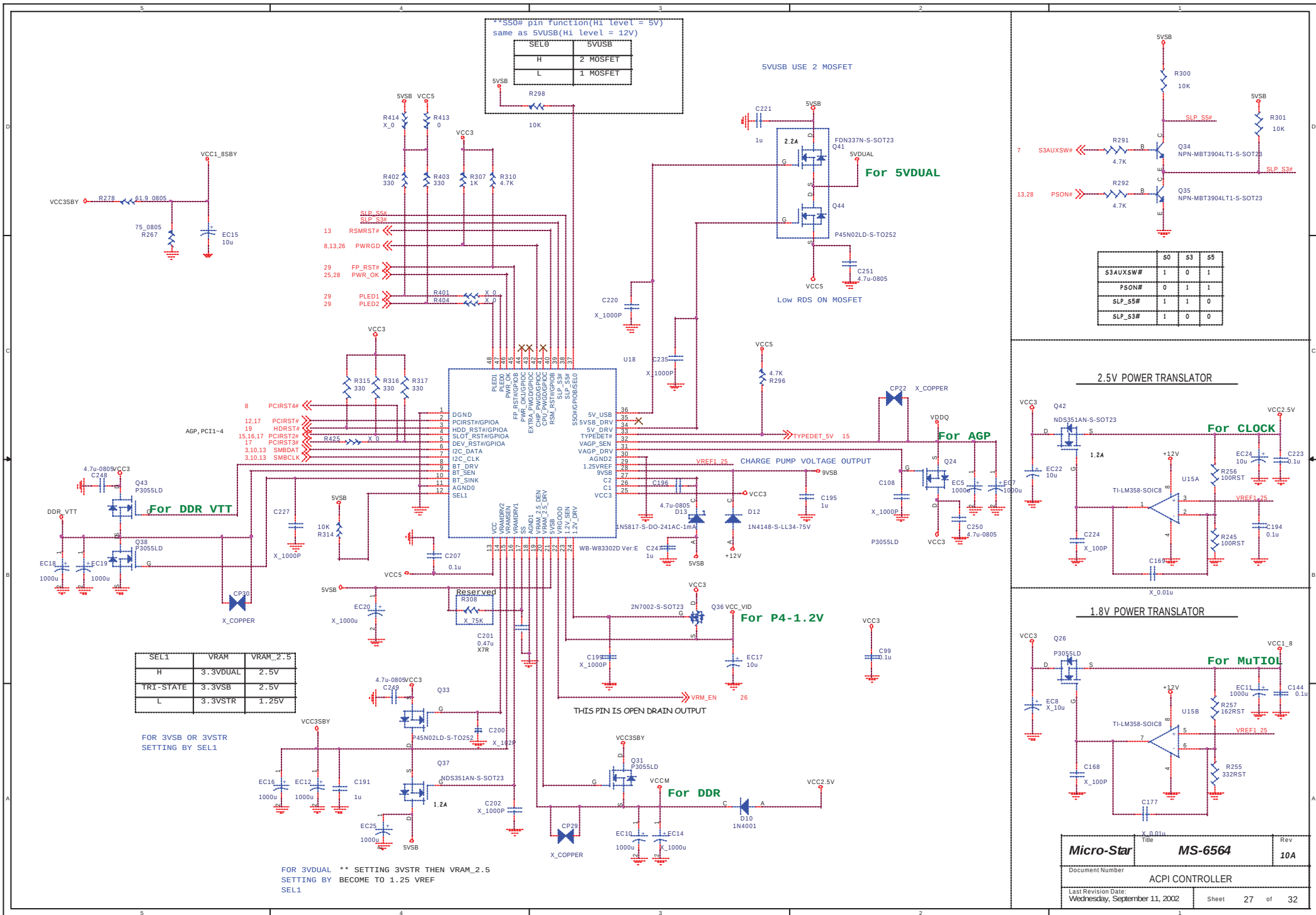
VID PULL-UP RESISTORS

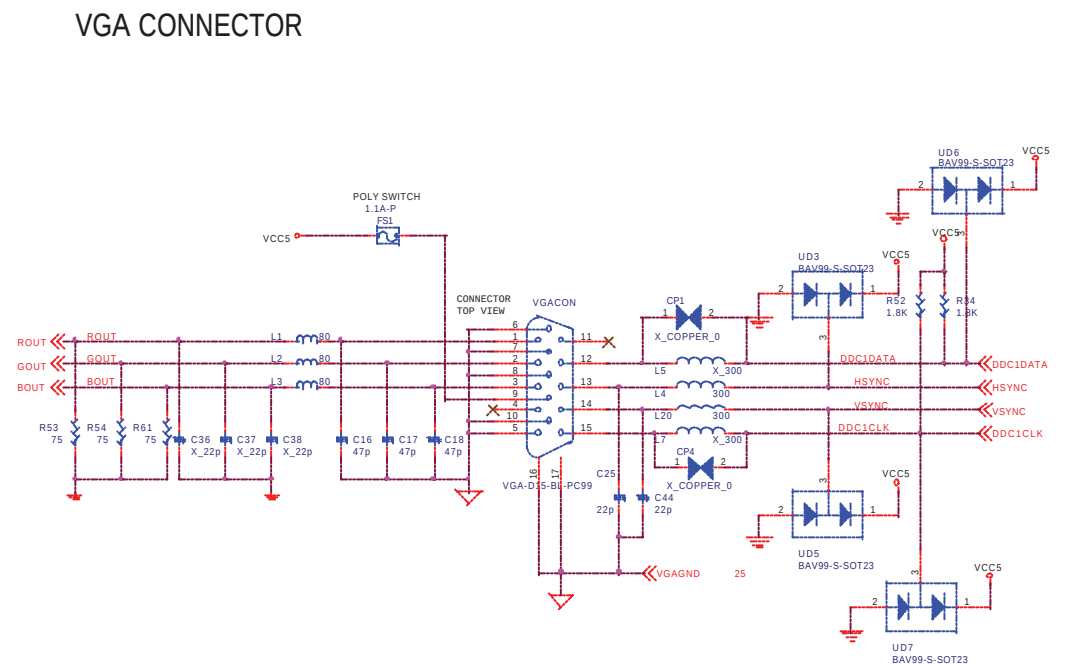
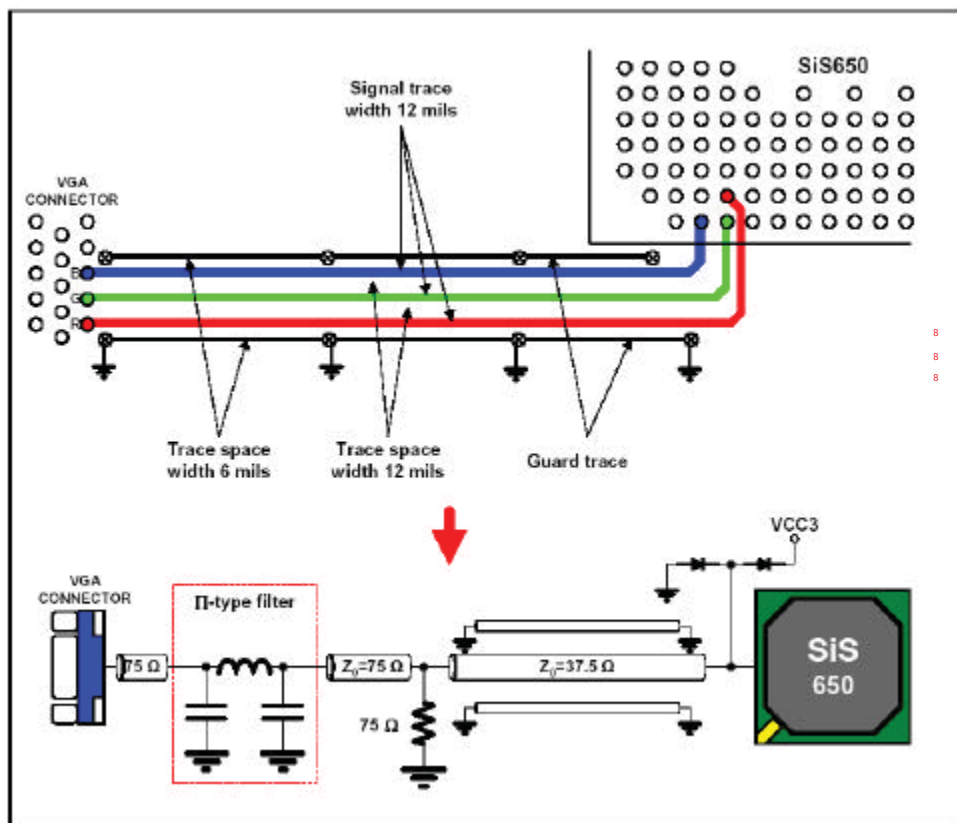
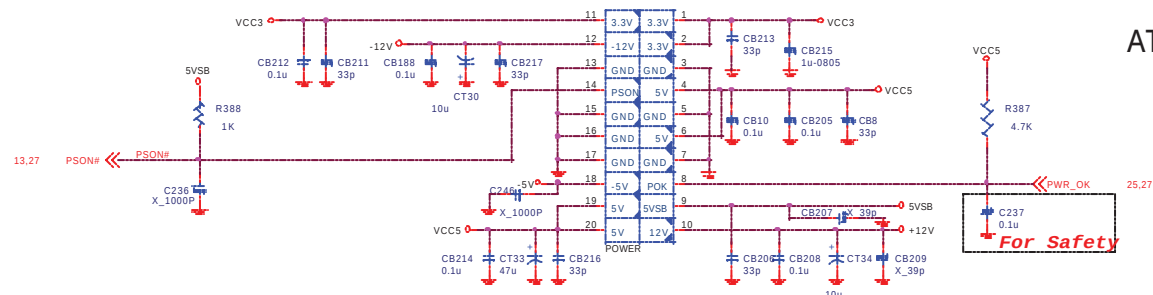


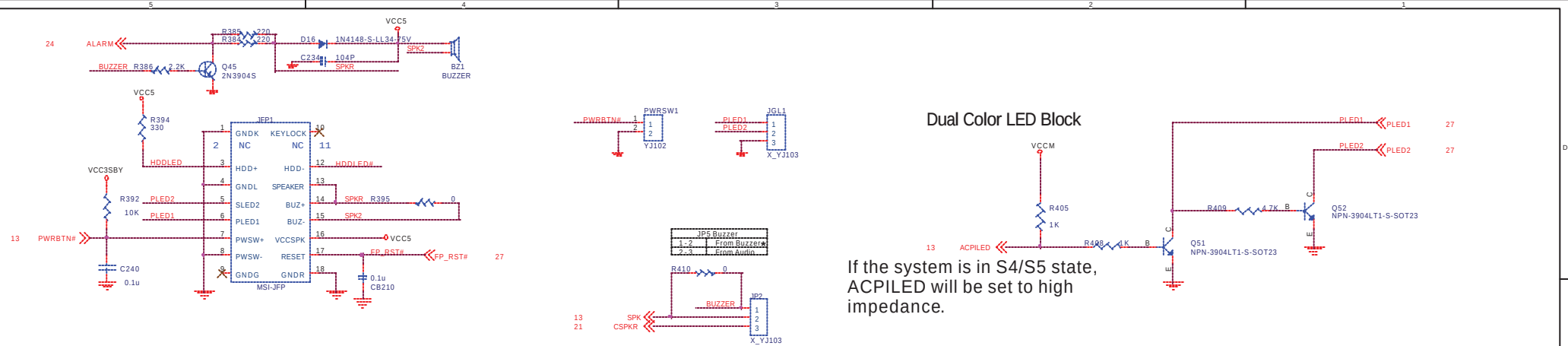
ATX12V POWER CONNECTOR



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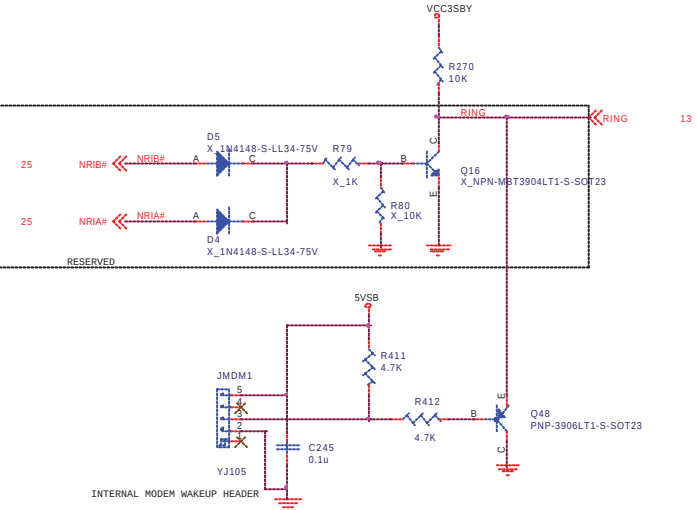




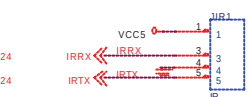


If the system is in S4/S5 state, ACPILED will be set to high impedance.

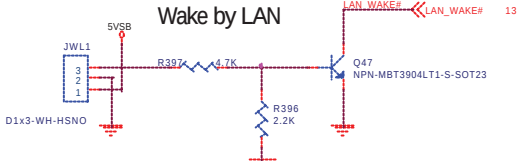
Wake by Modem



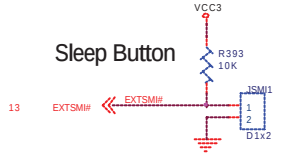
IR



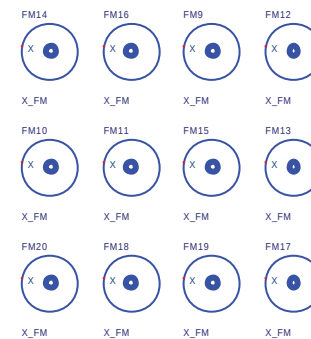
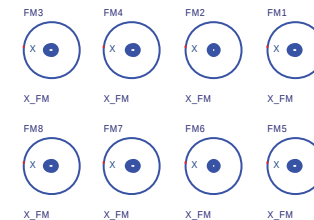
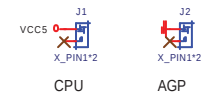
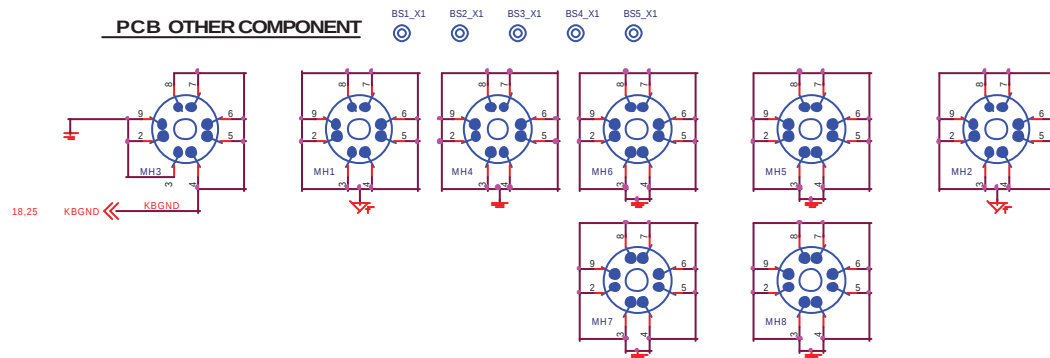
Wake by LAN



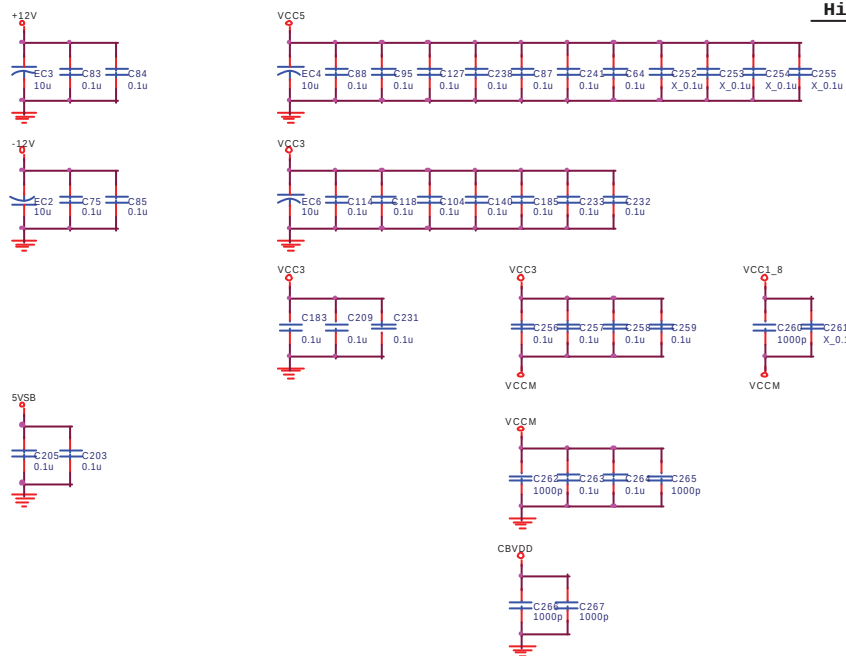
Sleep Button



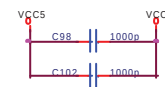
PCB OTHER COMPONENT



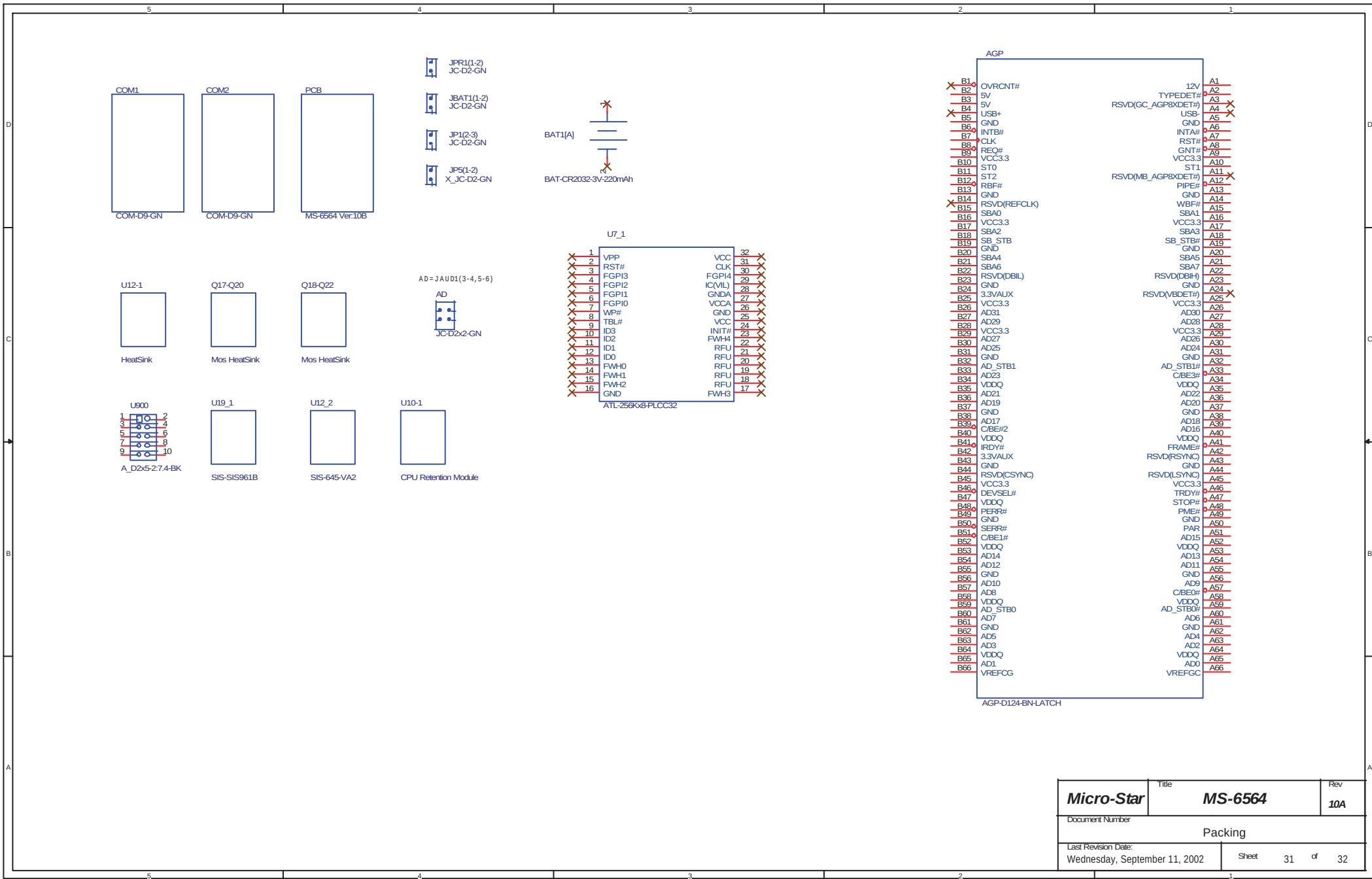
System Decoupling Capacitors



High Freq. return current decoupling



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Revision History

Revision History (Changes from Rev 0A)

Sheet	Description
13	Connect U19.A6 through RN56 4.7K to GND for SiS recommecnd.
17	Change U11 pin 5 & pin6 for circuit error.
	Change U13 pin 49,39 and R184 from VCC3SB to P3VA for 1394 S3 resume issue.
	Remove U16,U17 for 1394 trace meet VIA recommend.
20	Change U3 pin 124,4,10,18,27,37,45 from VCC3 to VCC5 for C-MEDIA recommend.
22	Change JAUD1 pim7 & C77,C73,C56,C66,C60,C67 for GNDF to GND for EMI request.
25	Add JPR1 1x3 pin for LG request.
27	Add C248,C249,C247,C250,C251 for ACPI controller decouping use.
	Add R413,R414 for PLED1/PLED2 pull up VCC5/5VSB choose.
28	Add UD6,UD7 diode for LG request.
	Change VCC and GND layer for ESD issue.
	Move CD_IN for mechanic issue.
	Change CD_IN and MDM_IN for LG request.
	Slove PCI1 B54 VCC3 for layout error.
	Change Audio CMI8738 and 4053 layout for C-MEDIA recommend.
	Separate VGA and Audio GND for Audio noise.
	Move L34,L36,CT19,CT23,CB99,CB103 for LG request.
	Move power connect for LG request.
	Change M/B size the same 6527 for LG request.

Revision History (Changes from Rev 10A)

Sheet	Description
30	Change screw hole VCC layer gap

Revision History (Changes from Rev 100)

Sheet	Description
25	Add R426,427, C270, Q54 for HP print issue by LG request.