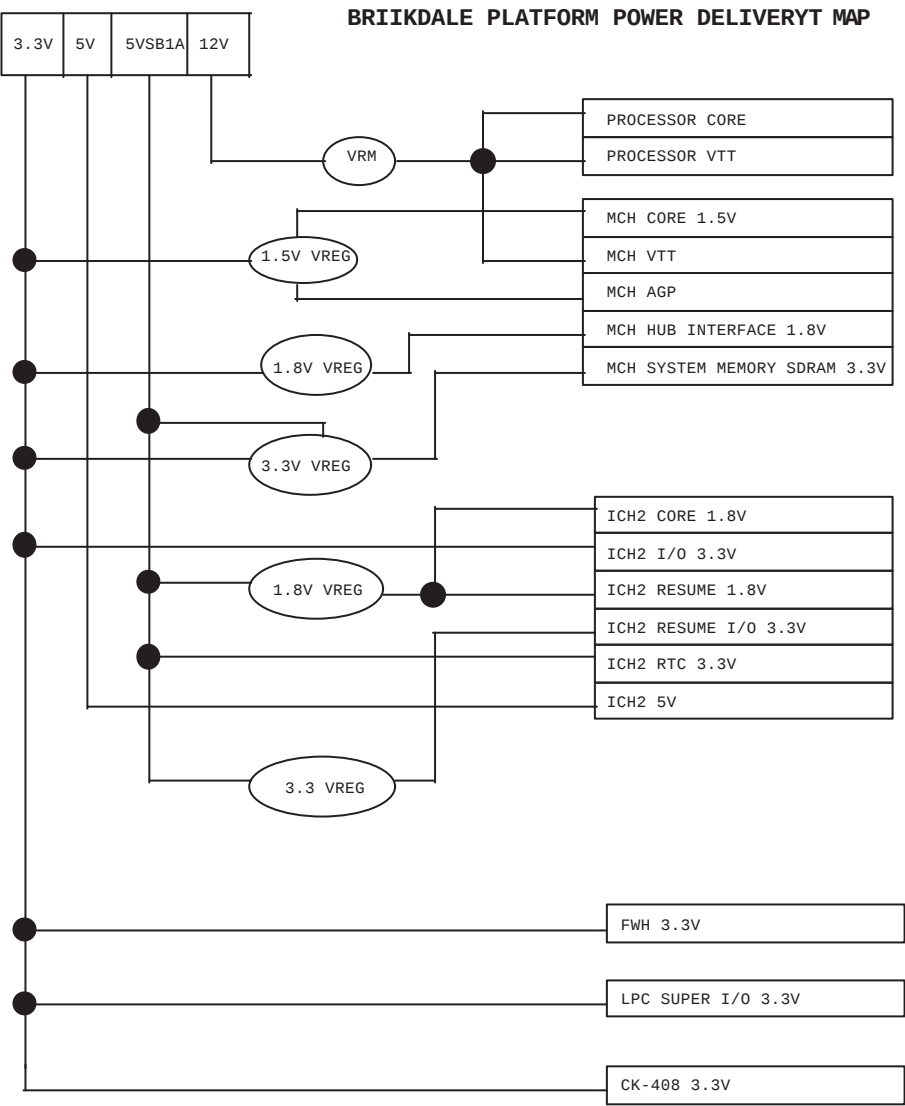
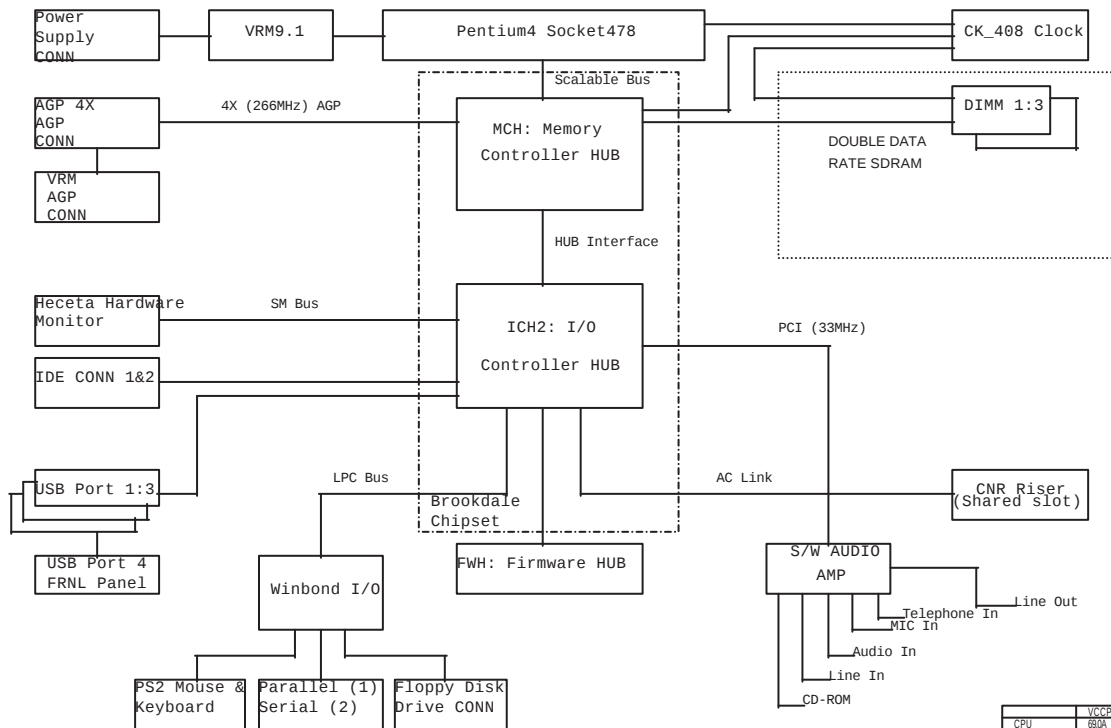


MS-6562 INTEL (R)
Brookdale/ICH2
CHIPSET
Pentium 4 in 478 pinPackage/Northwood
Processor SCHEMATICS

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POWER CONSUMPTION

	VCCP	VCC AGP	VCC1.8	VCC3 DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	800A	0	0	0	0	0	0	NOTE4	0
PNCH	24A	NOTE1	0.2A	20A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CLOCK	0	0	0	0	0	0	0	0	0
CODEC	0	0	0	0	0	0	0	0	0
FWH	0	0	0	0	0	0	0	0	0
LAN	0	0	0	0	0	0	0	0	0
SIO	0	0	0	0	0	0	0	0	0
782D	0	0	0	0	0	0	0	0	0
SC2E3	0	0	0	0	0	0	0	0	0
SC426	0	0	0	0	0	0	0	0	0
SC457	0	0	0	0	0	0	0	0	0
DMM	0	0	0	NOTE2	0	0	NOTE2	0	0
CNR	0	0	0	0	0	0	0	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0	0	0	0	0	0
USB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
OTHER	0	0	0	0	0	0	0	0	0

NOTE1--MCH
 $VCC_AGP = VCC1_5(15A) + VCC_AGP(0.37A)$

NOTE2--DIMM
 S0 STATE --- $2.0A * 3 = 6.0A \rightarrow VCC3$
 S1/S3 STATE --- $200mA * 3 = 600mA \rightarrow VCC3_SB$
 $VCC3_SB \rightarrow 600mA * 3.3V/5V = 396mA \rightarrow VCC5_SB$

NOTE3 -- ICH2

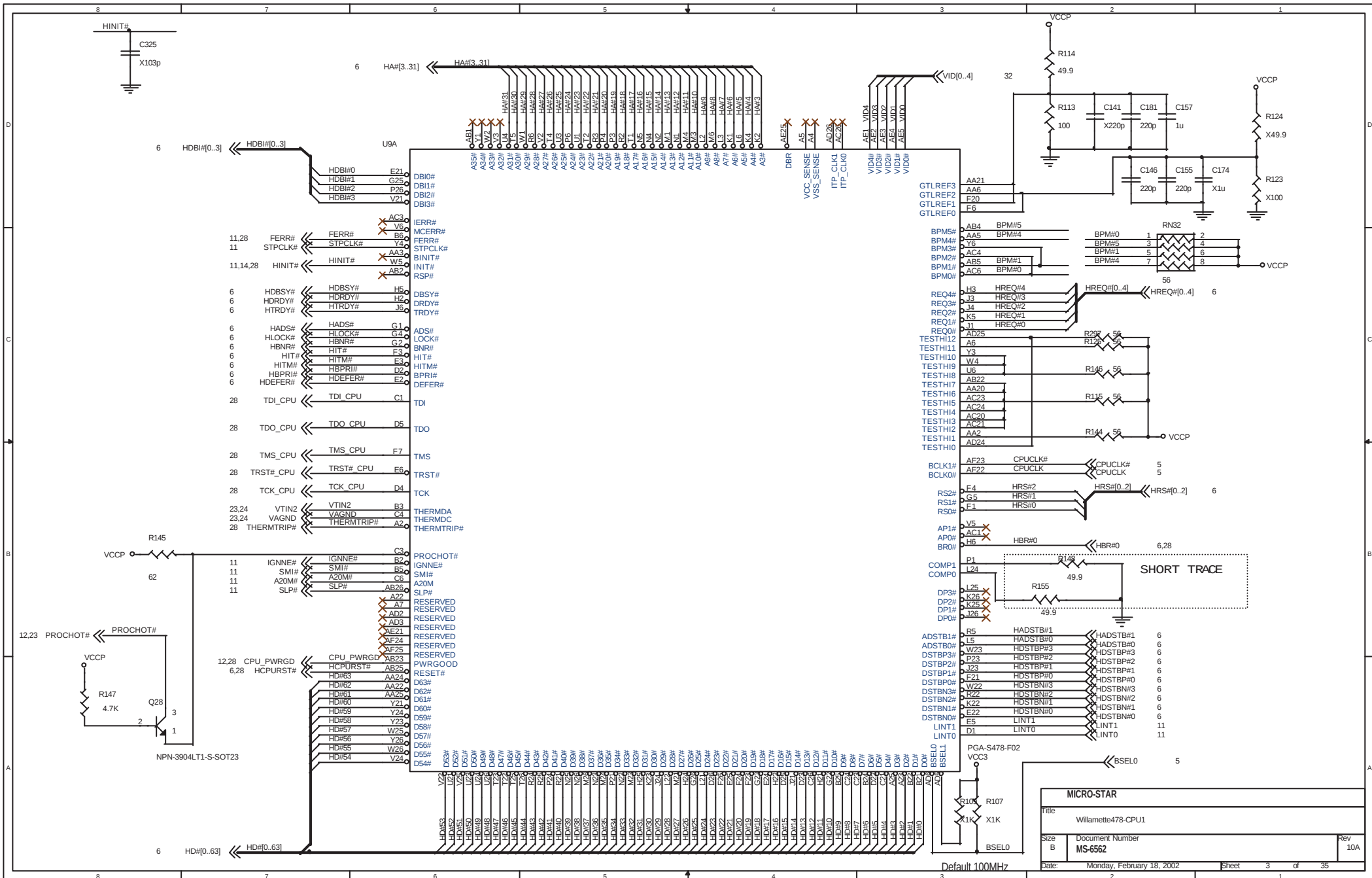
Power	S0	S1	S3/S4/S5
18V	30mA	100mA	N/A
18V LAN	30mA	20mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	40mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	08mA	N/A

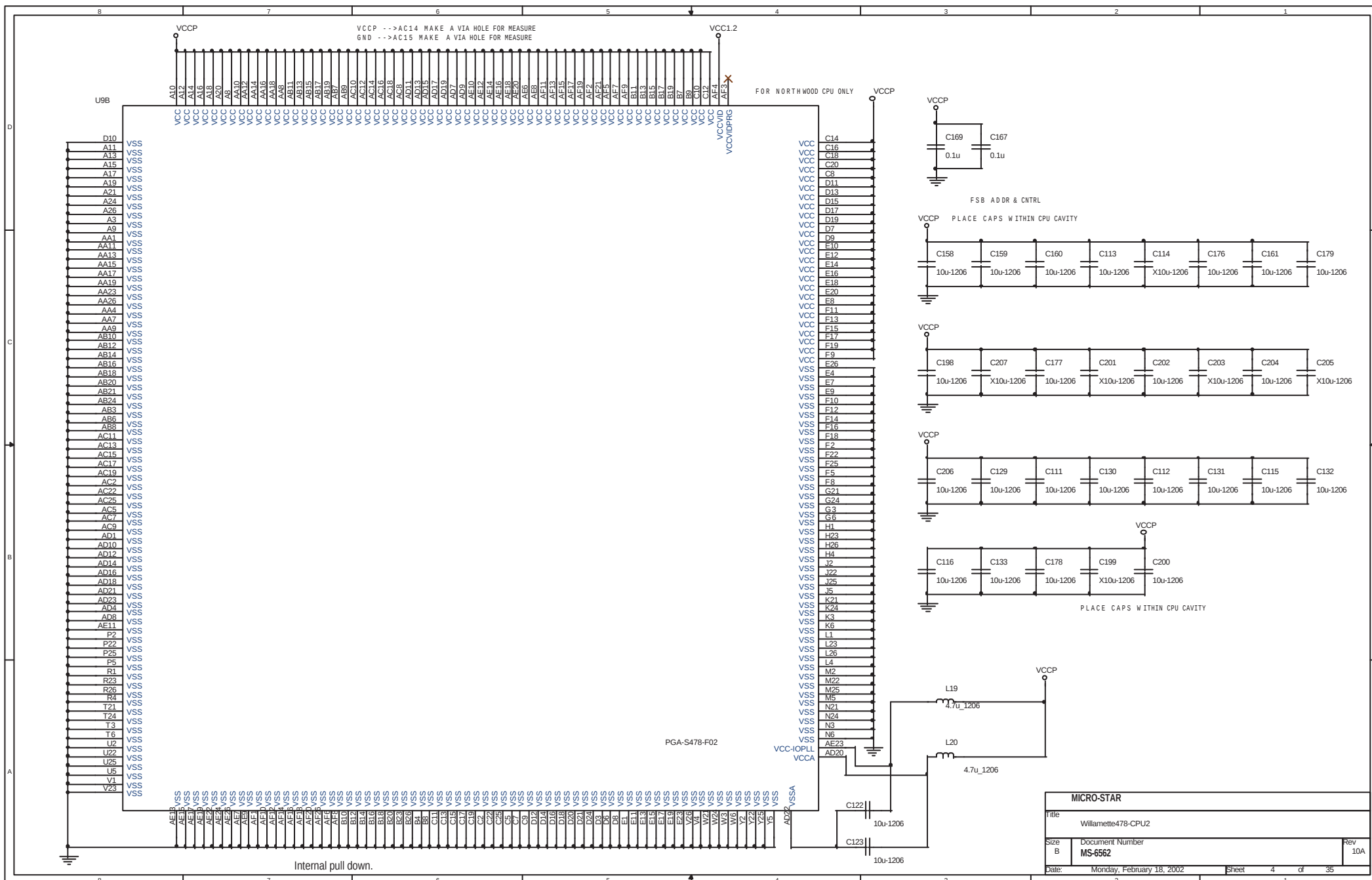
$VCC3_SB =$
 $VCC1_8SB =$
 $VCC5_SB = VCC3_SB + VCC1_8SB$

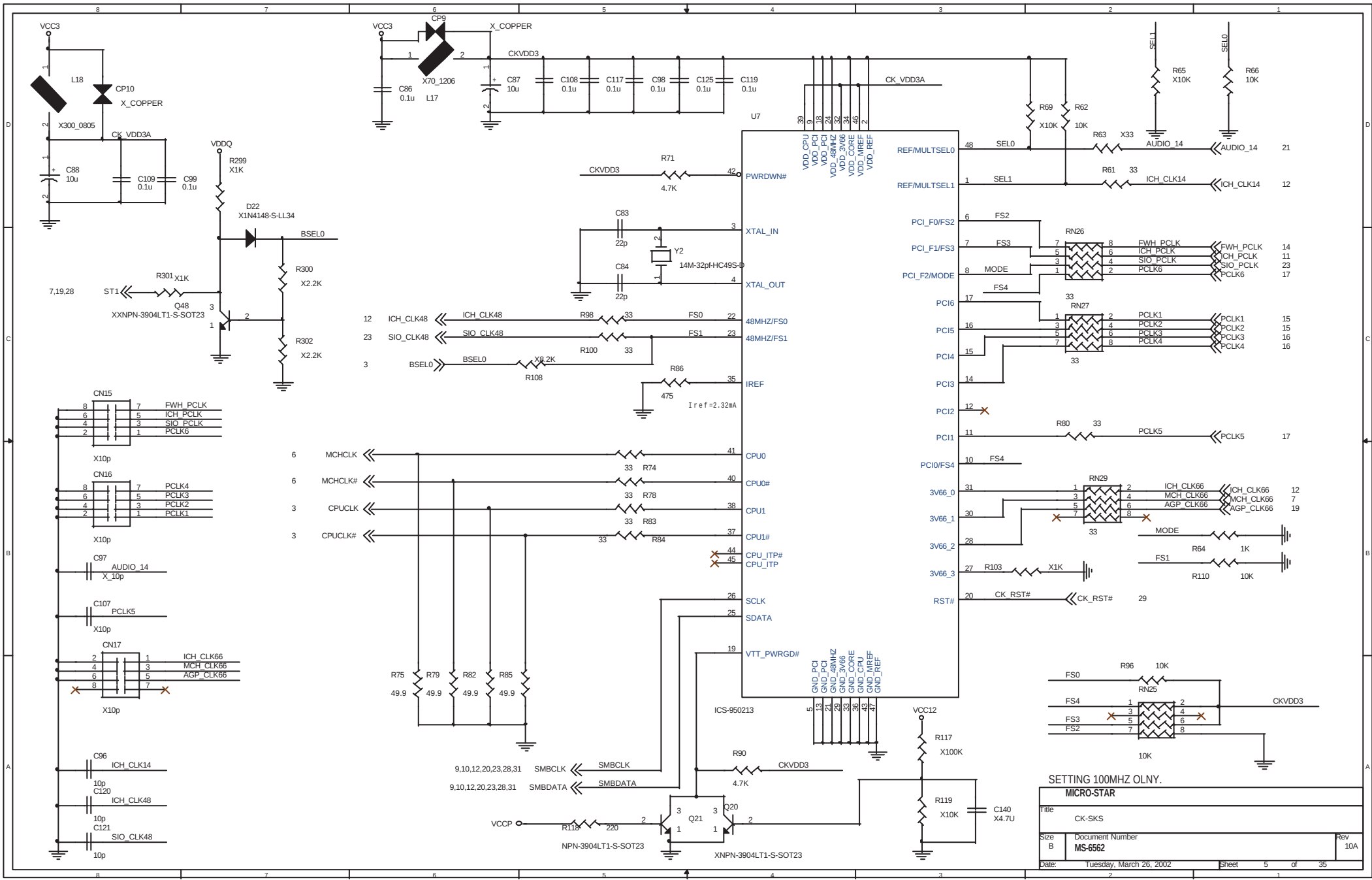
H/W Project Leader : Andy Chen
 H/W Project Engineer : Prudence Wang

MICRO-STAR

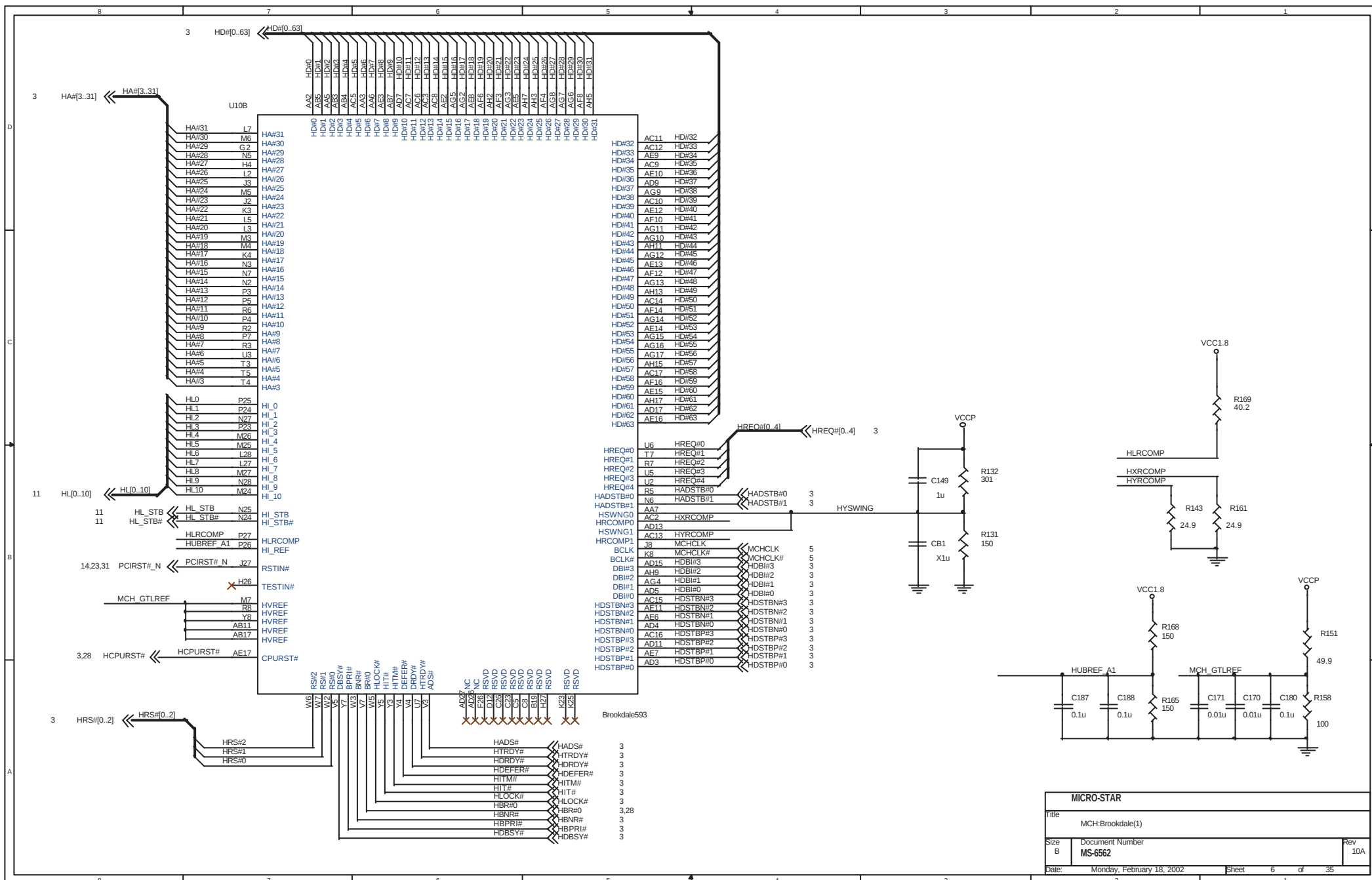
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Block Diagram		
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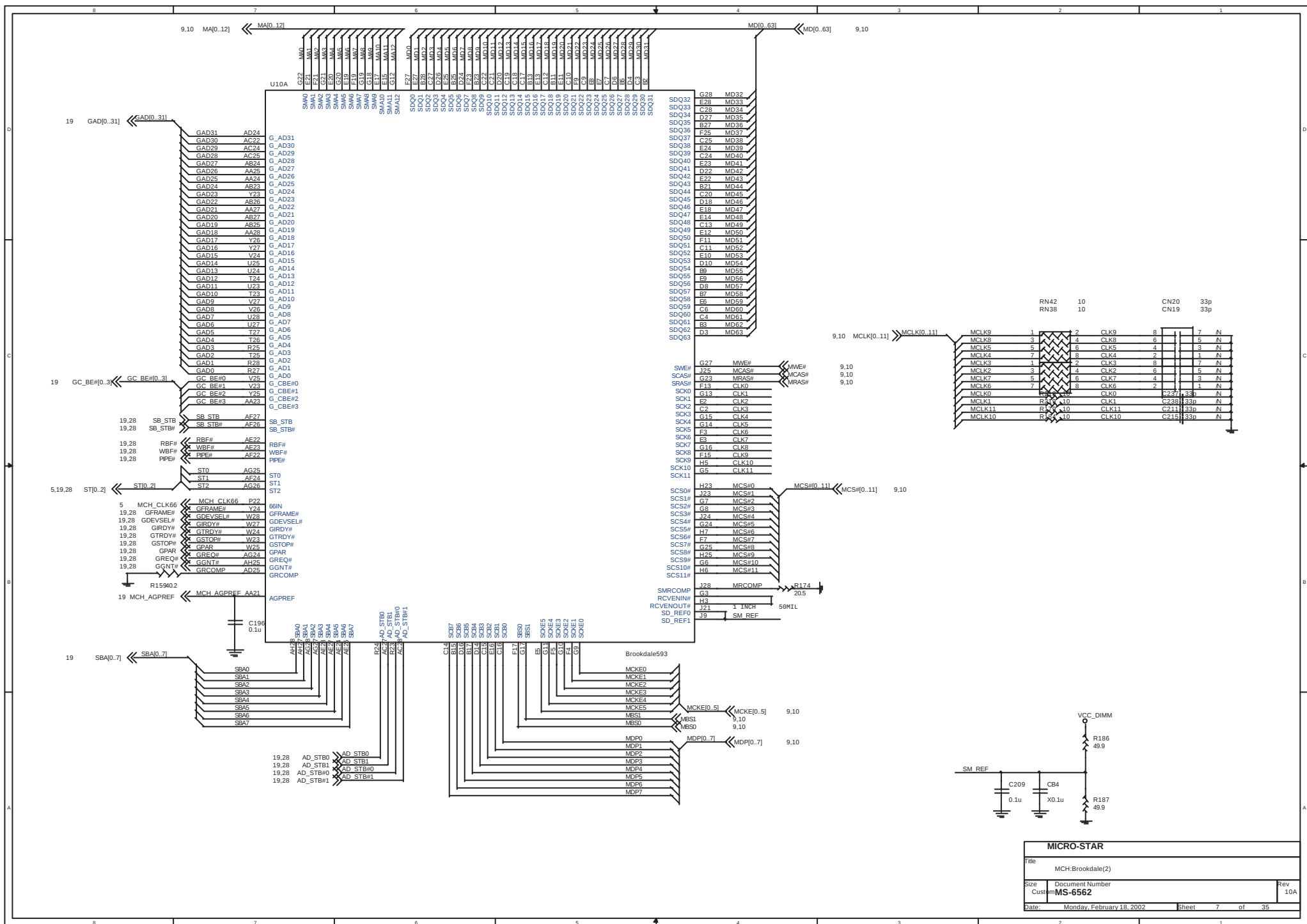


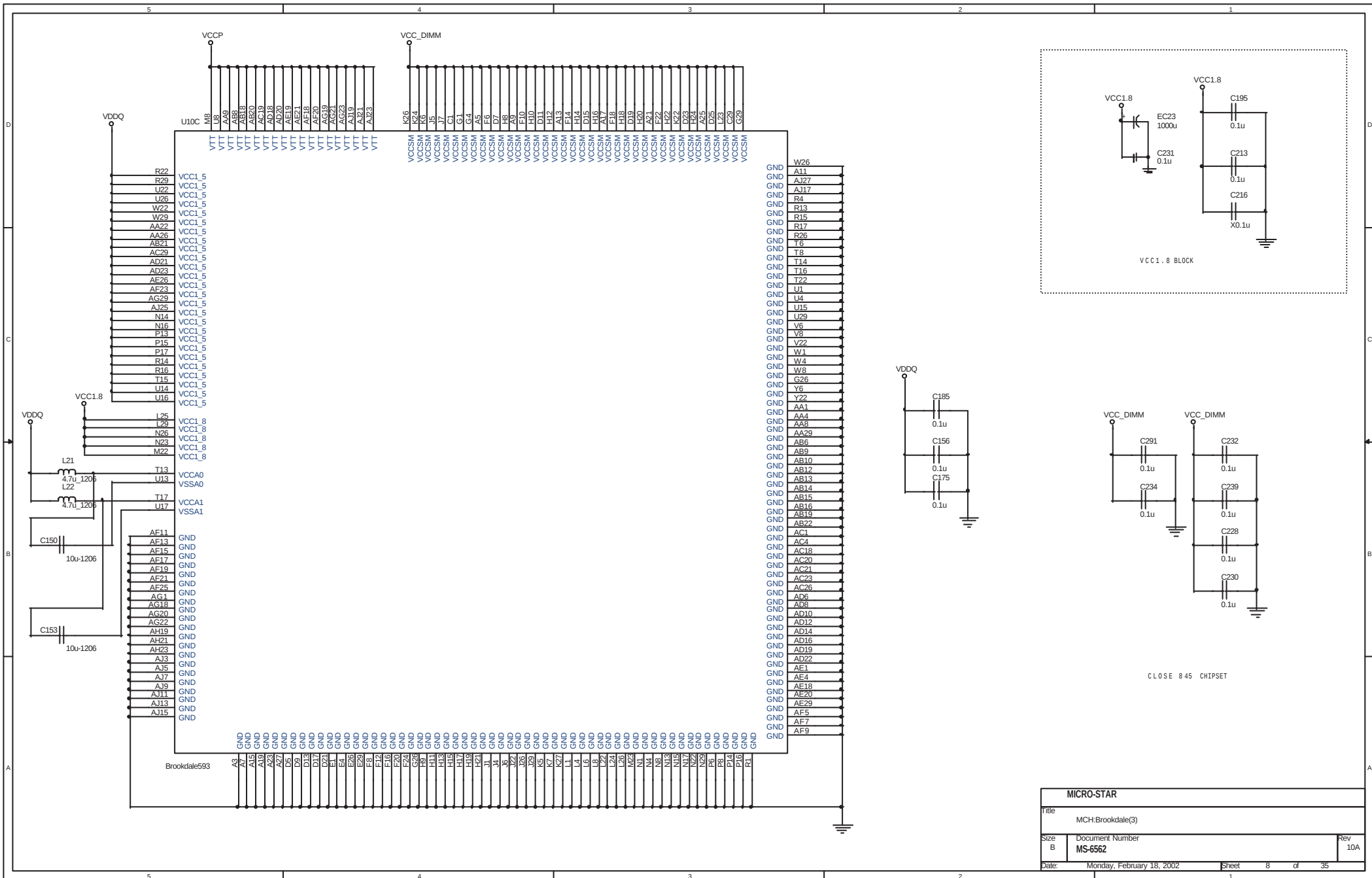


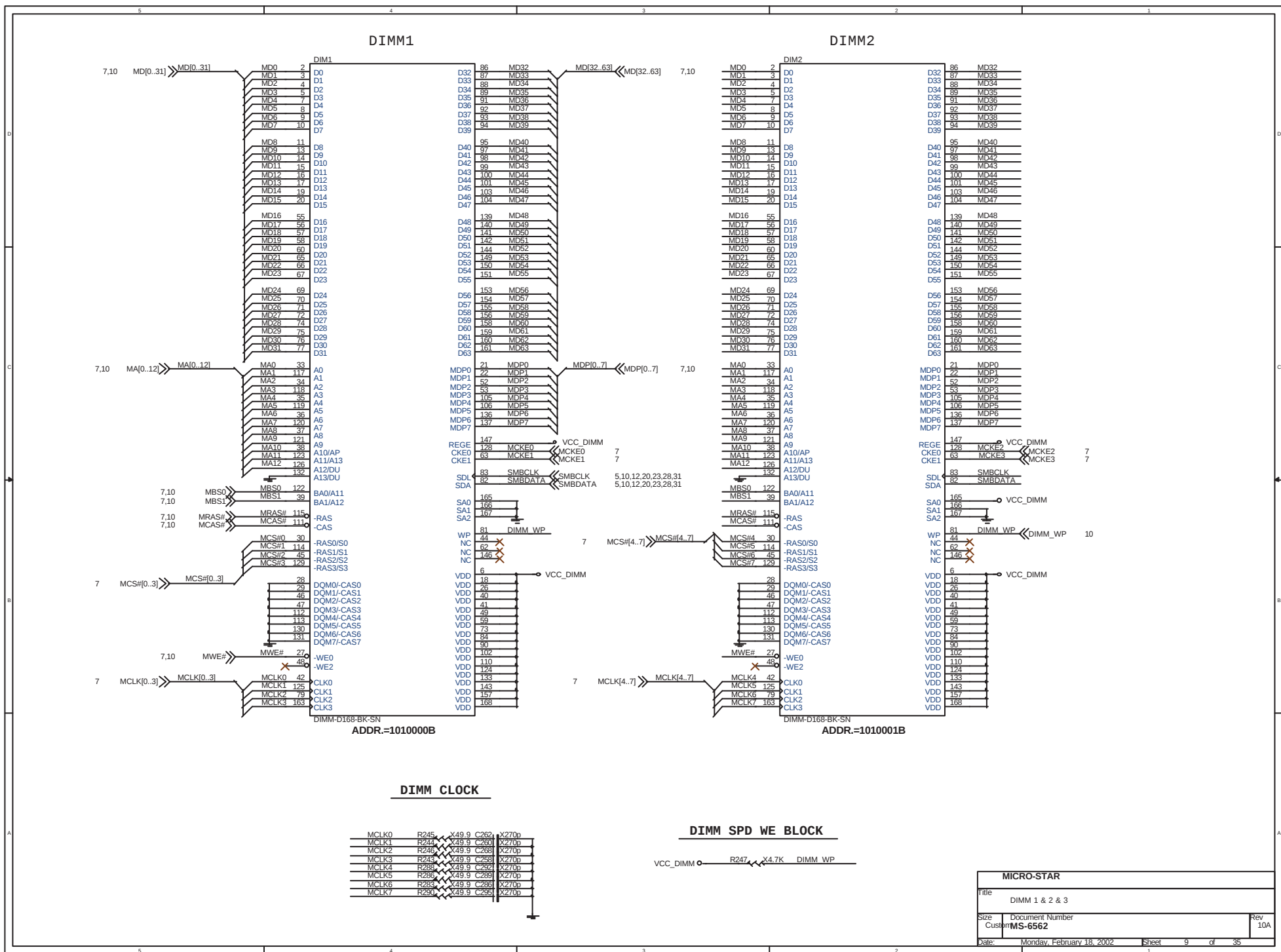


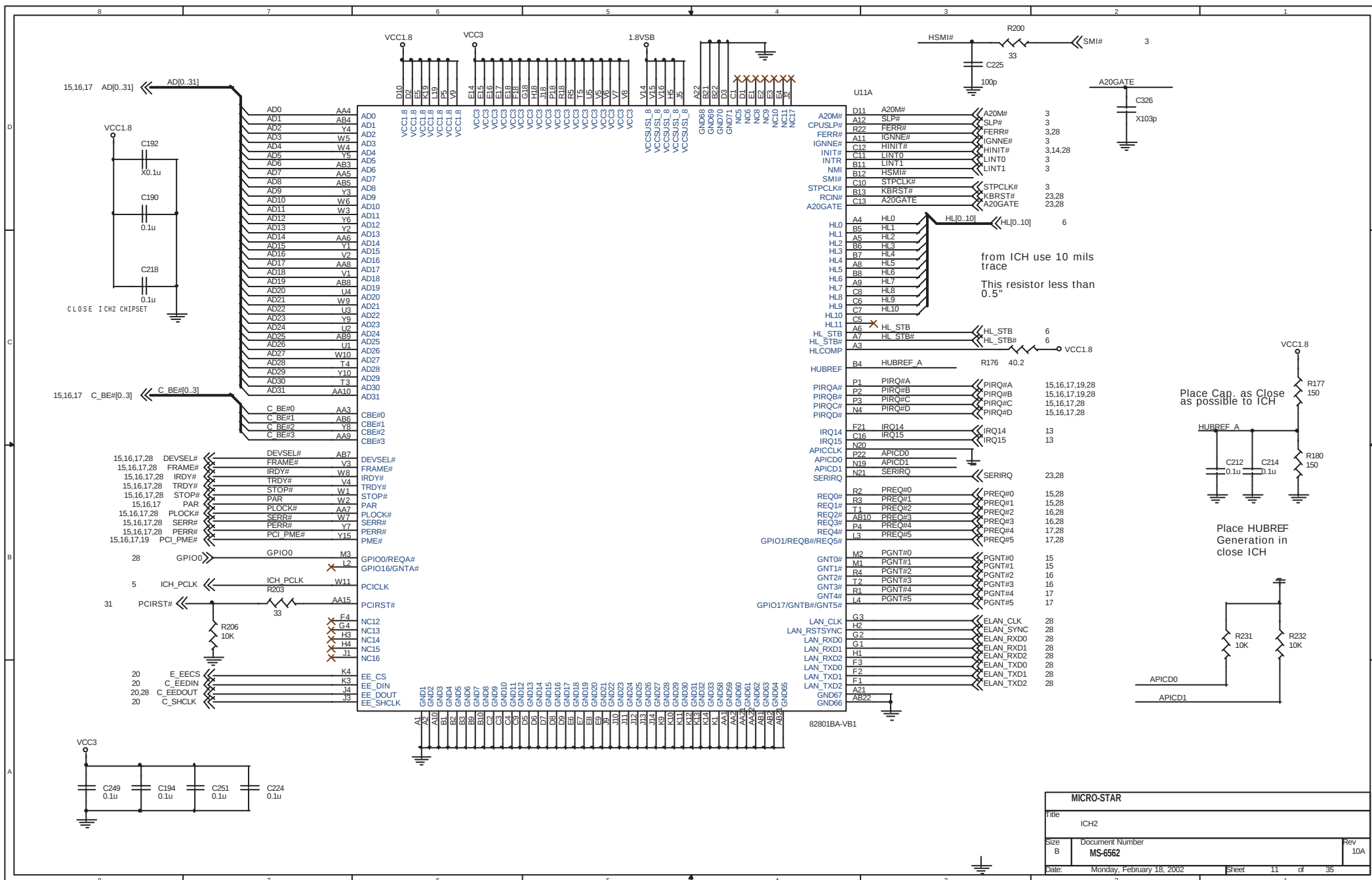
SETTING 100MHZ OLNLY.		
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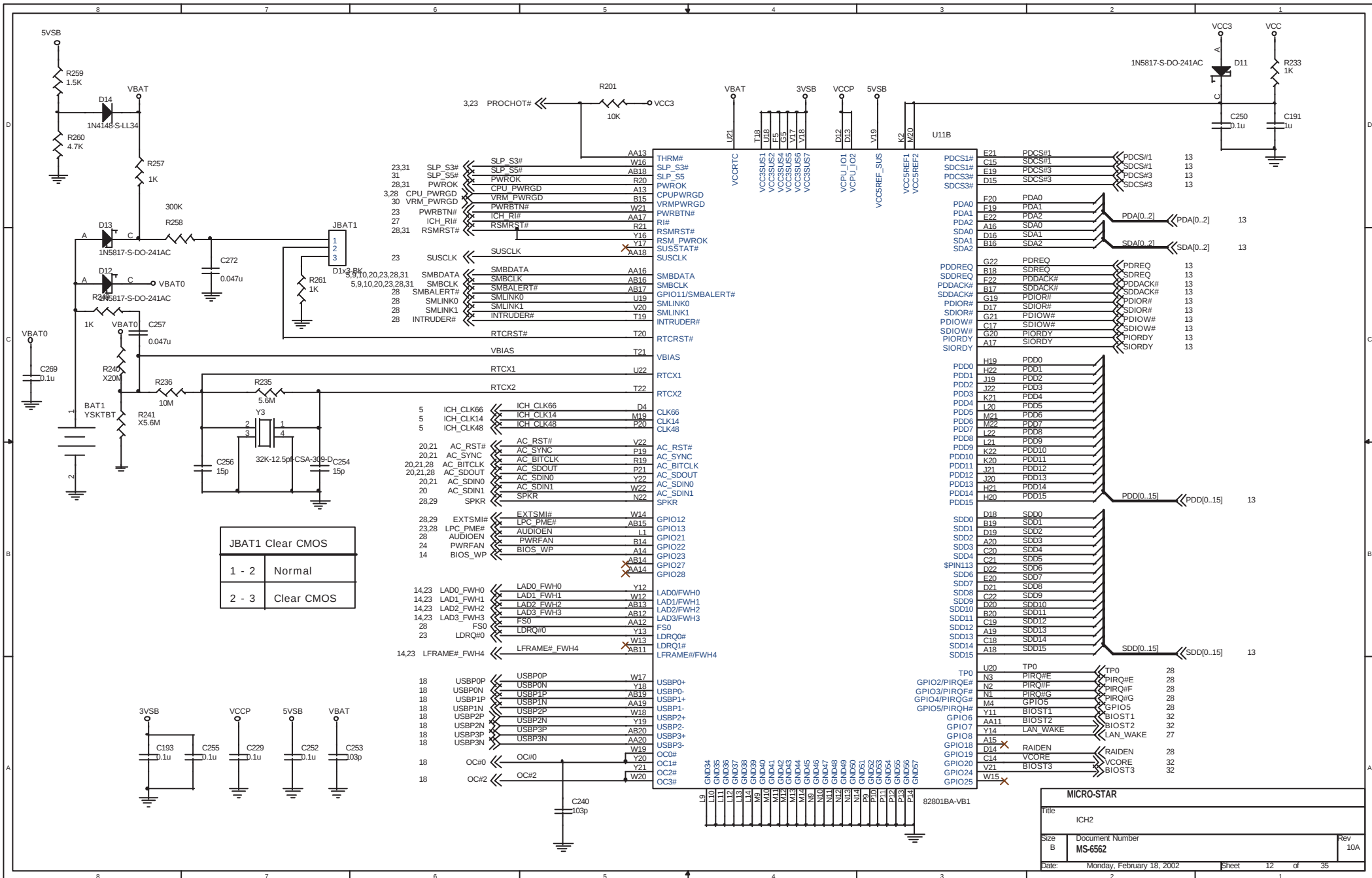






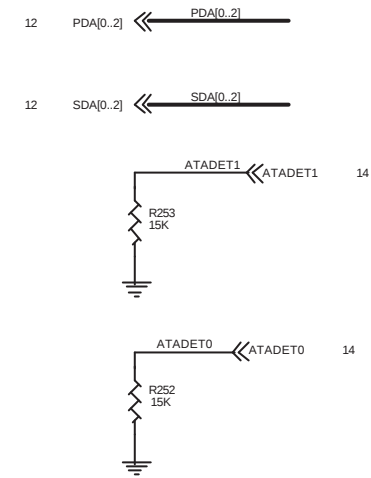
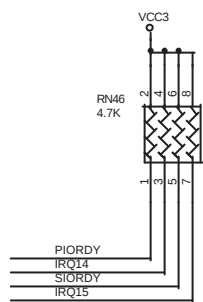
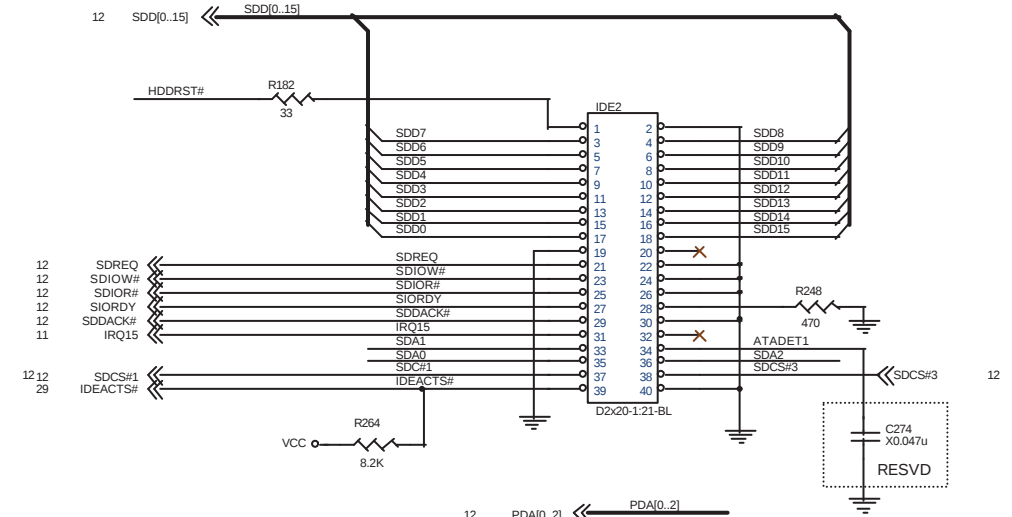
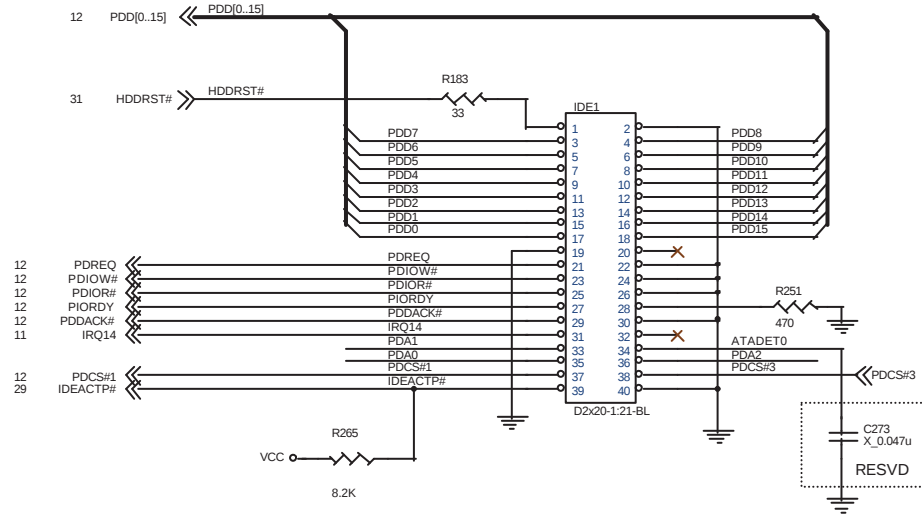


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ICH2									
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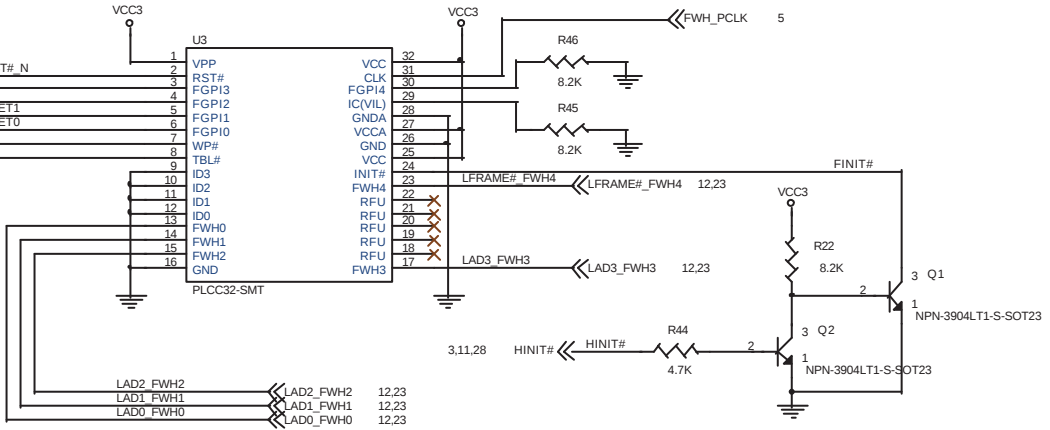
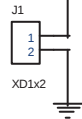
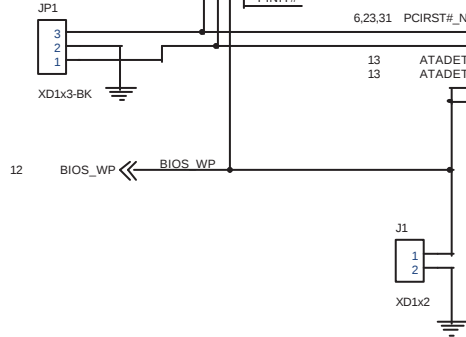
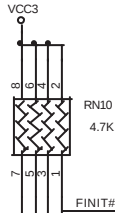
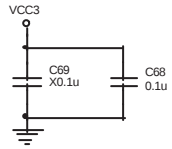


PRIMARY IDE CONN.

SECONDARY IDE CONN.



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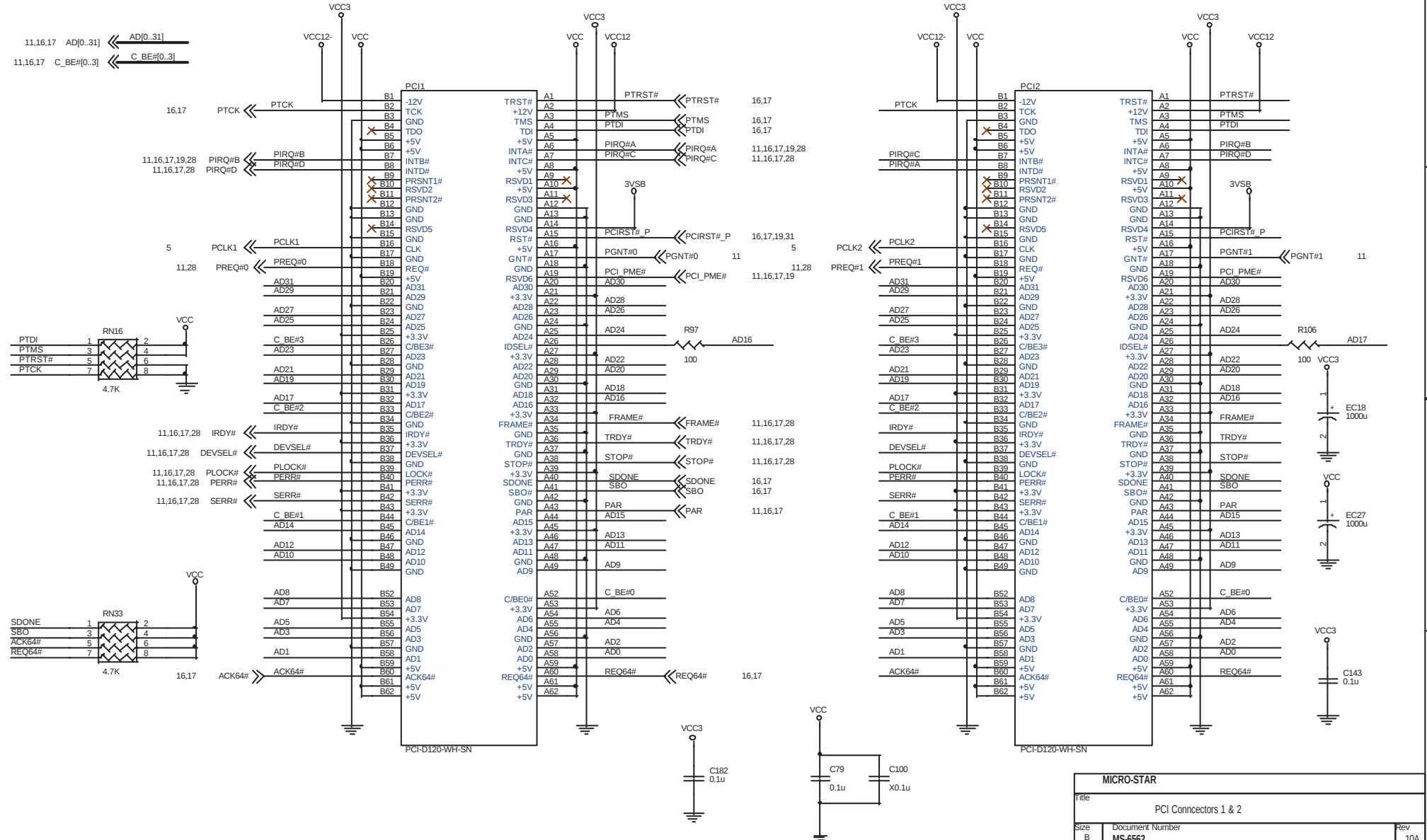
JP1 Gateway	
1 - 2	Flash from FDD
2 - 3	Boot auto clear CMOS

J6 BIOS PROTECT	
SHORT	Locked
OPEN	Unlocked

*

MICRO-STAR		
Title	FWH	
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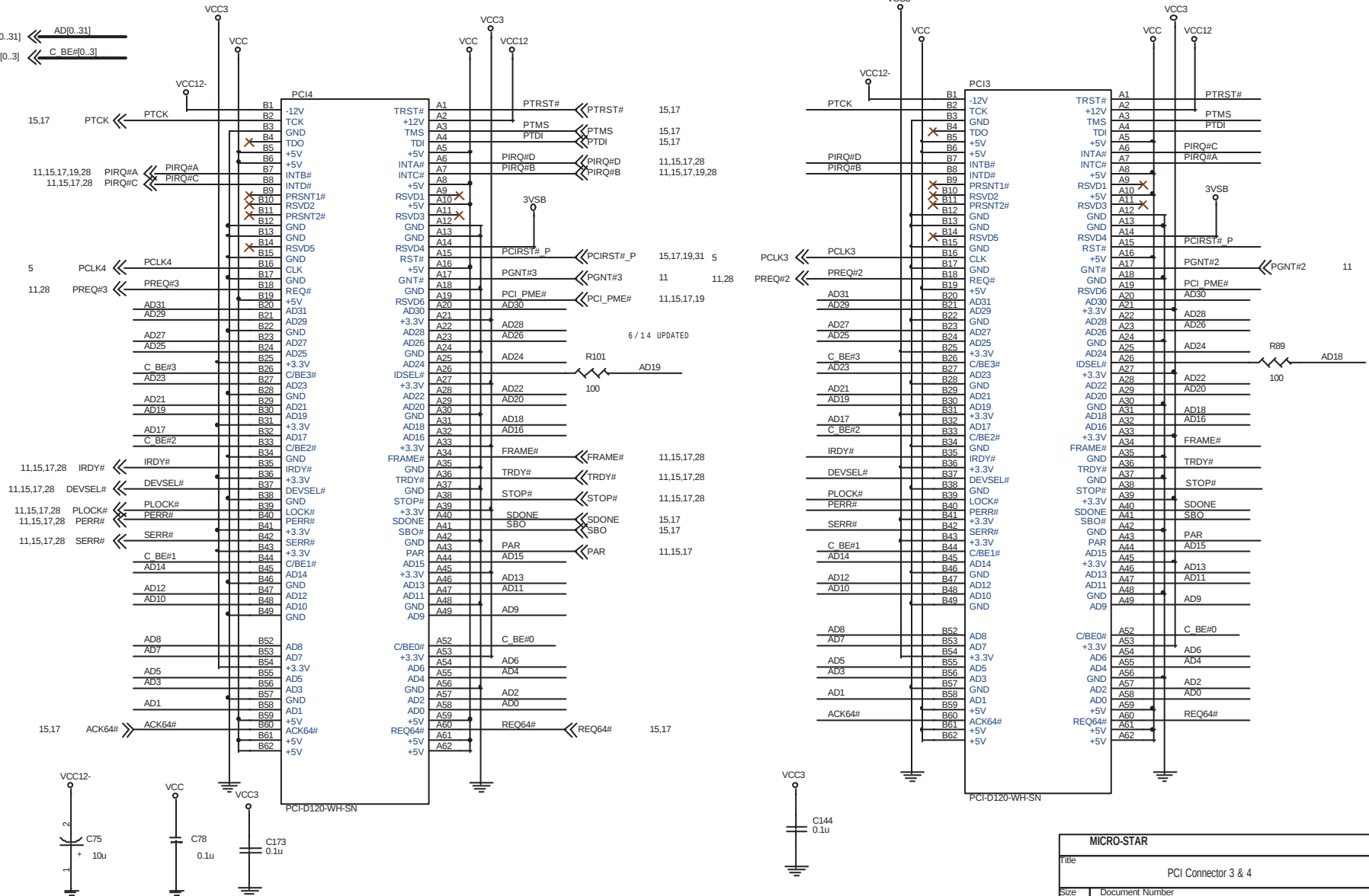
PCI Connector 1 & 2



MICRO-STAR		
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PCI Connectors 1 & 2		
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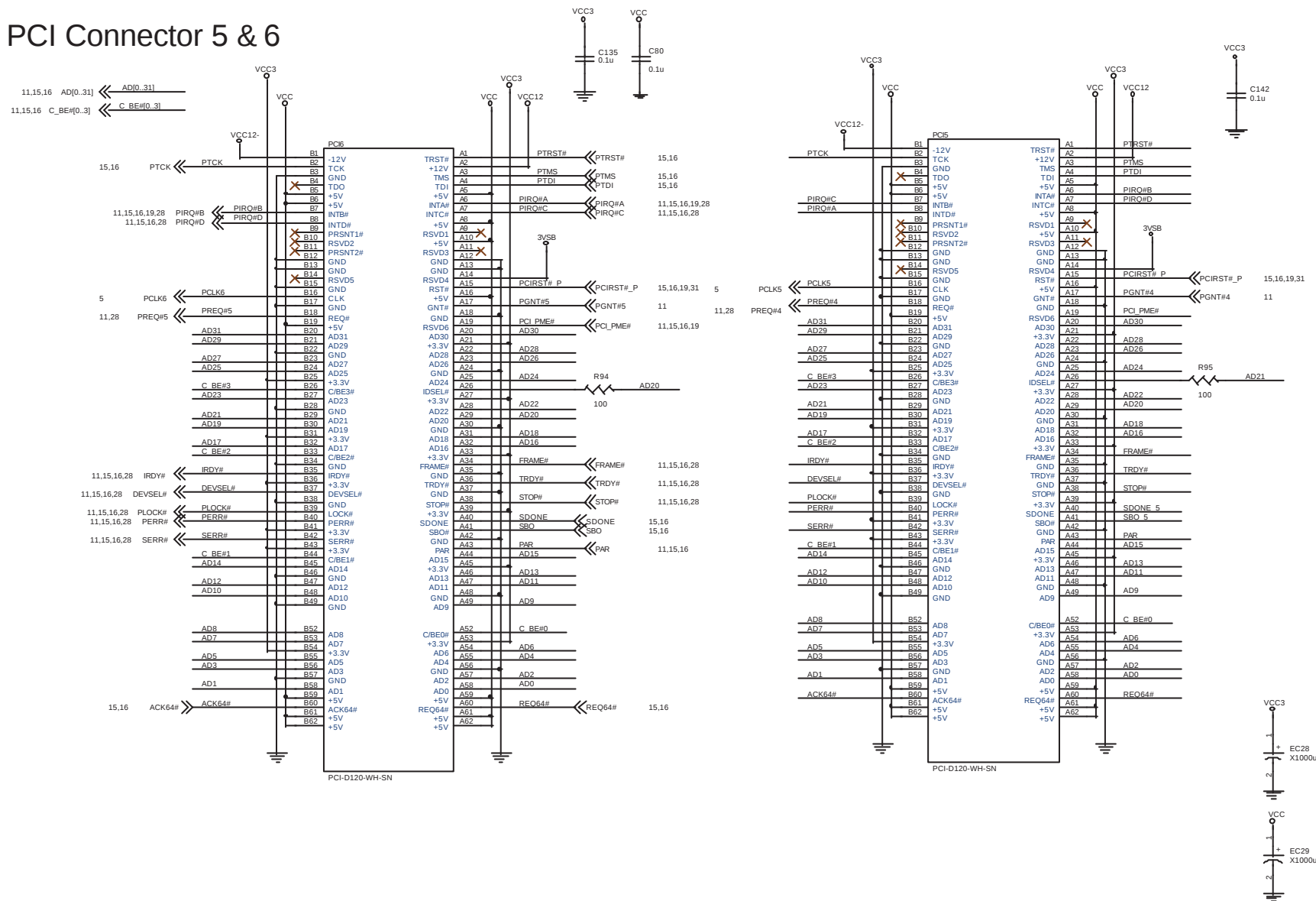
32/33 PCI Connector 3 & 4

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11,15,17 C_BE#[0..3] << C_BE#[0..3]

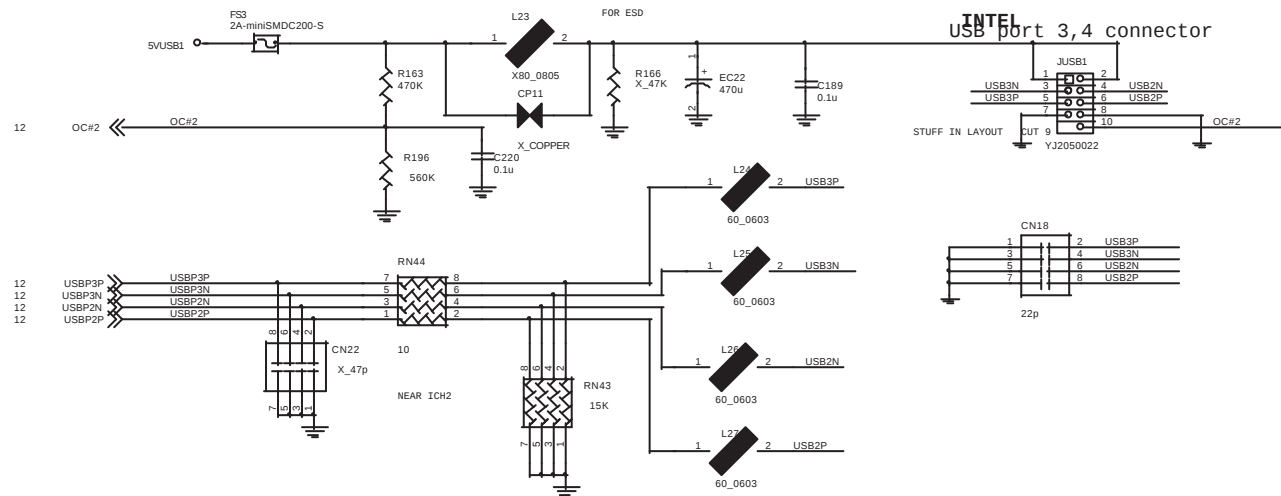
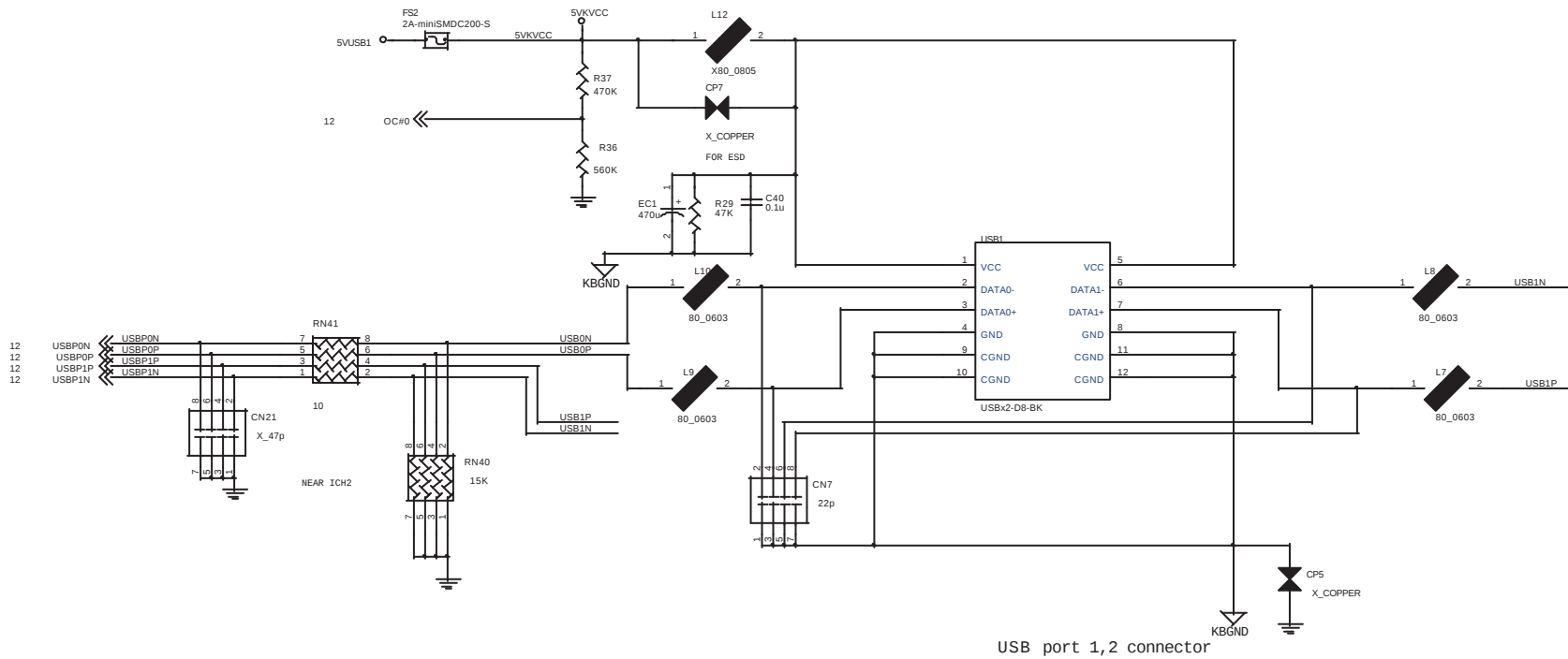


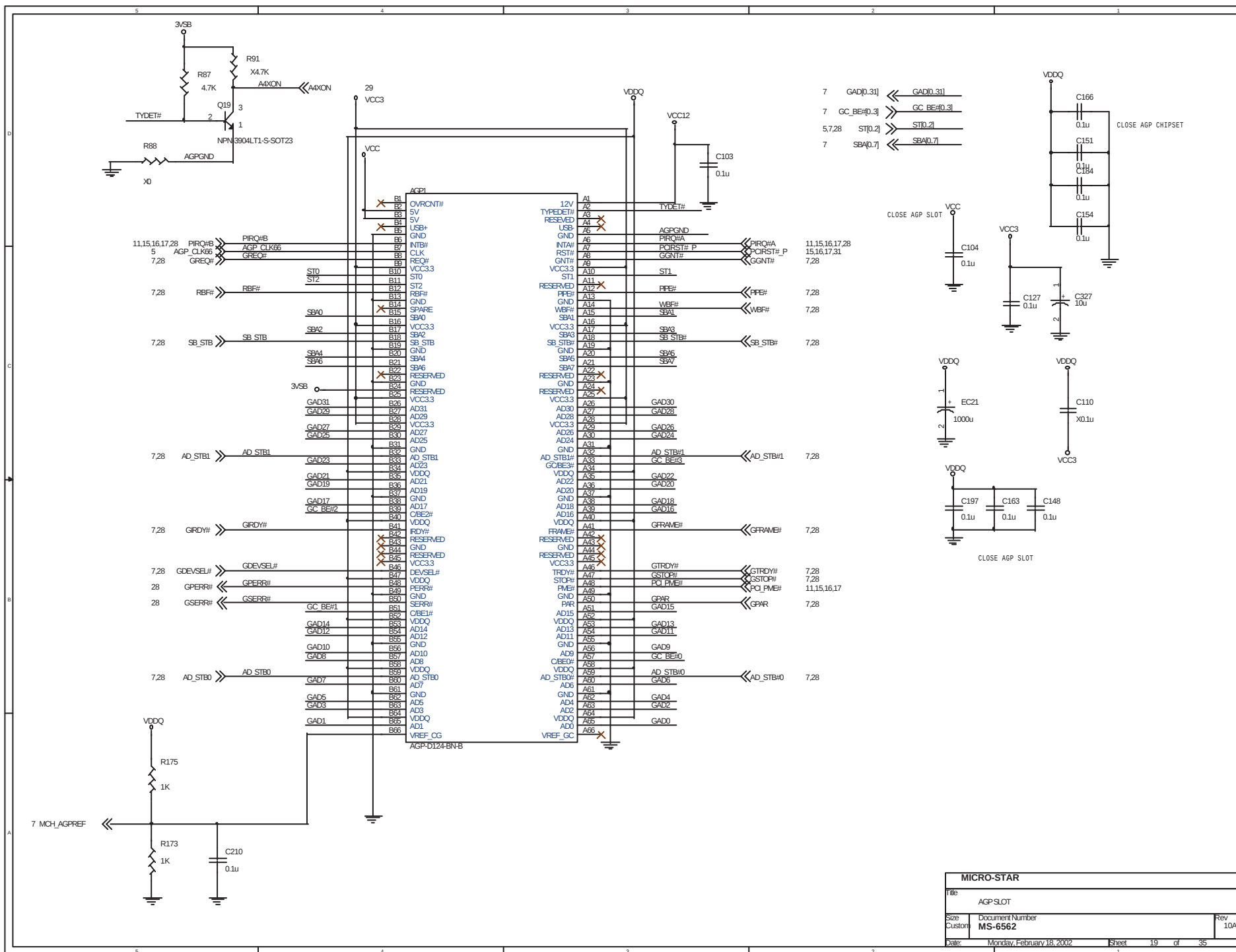
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PCI Connector 3 & 4		
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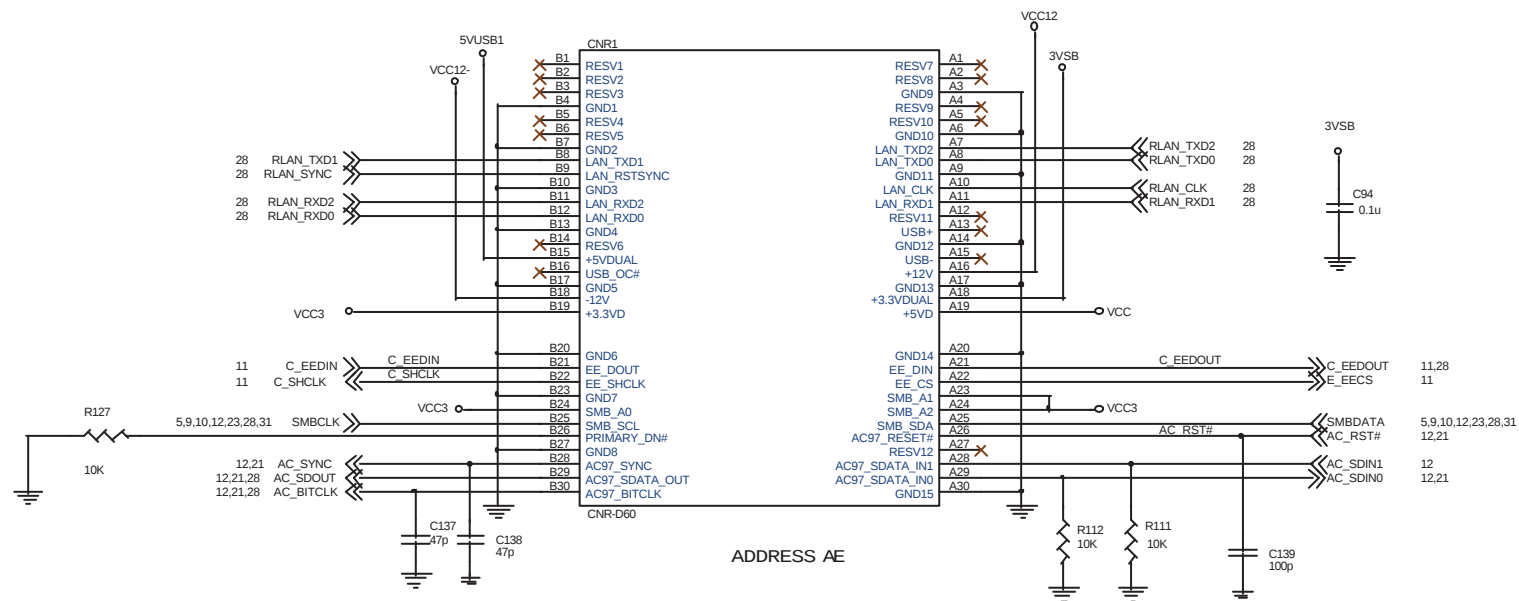
PCI Connector 5 & 6



MICRO-STAR			
Title PCI Connector5&6			
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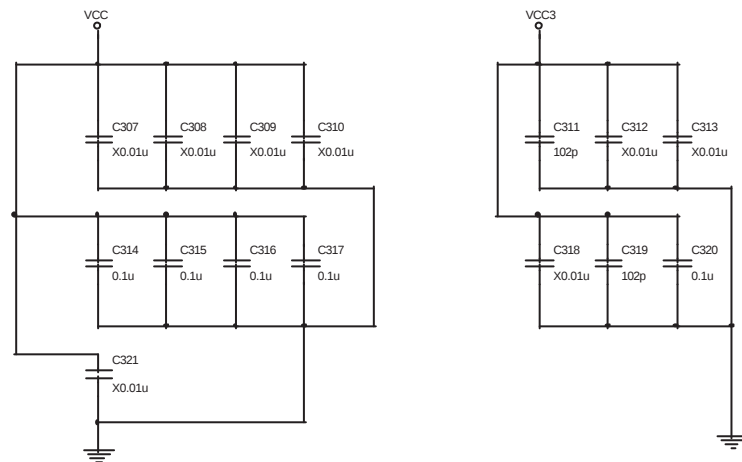


ADDRESS AE

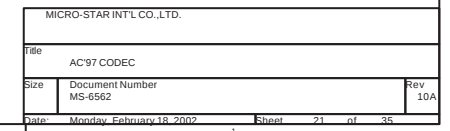
EMI REQUEST

FOR I/O AT THE LEFT SIDE OF W/B

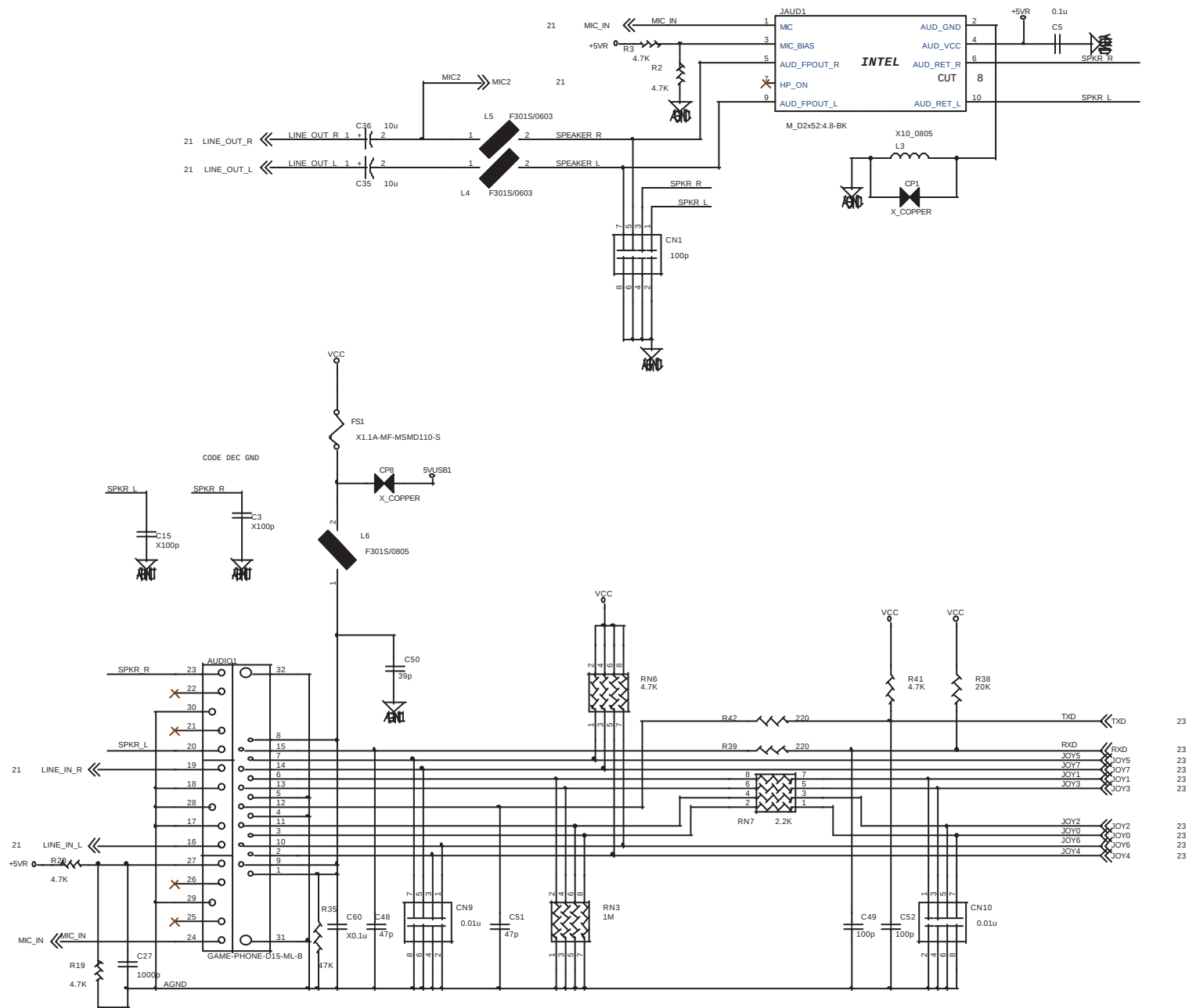
FOR CLOCKGEN



MICRO-STAR		
Title		
CNR AND AUDIO HEADER		
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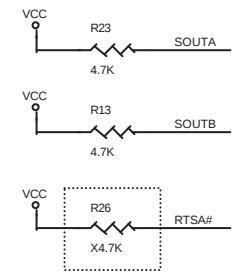
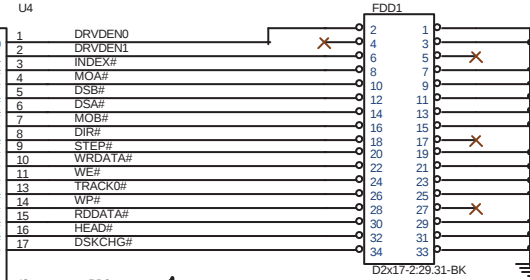
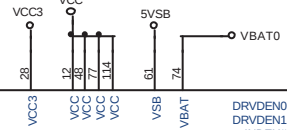


MSI/INTEL AUDIO CONNECTOR



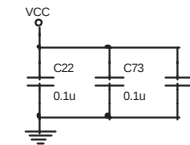
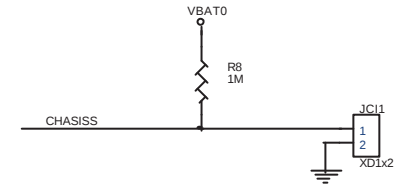
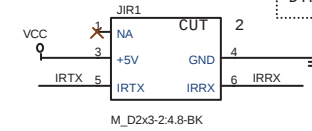
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MIDI/GAMEPORT			
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FLOPPY DISK HEADER

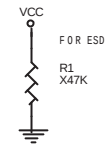


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	L: PNP no Default

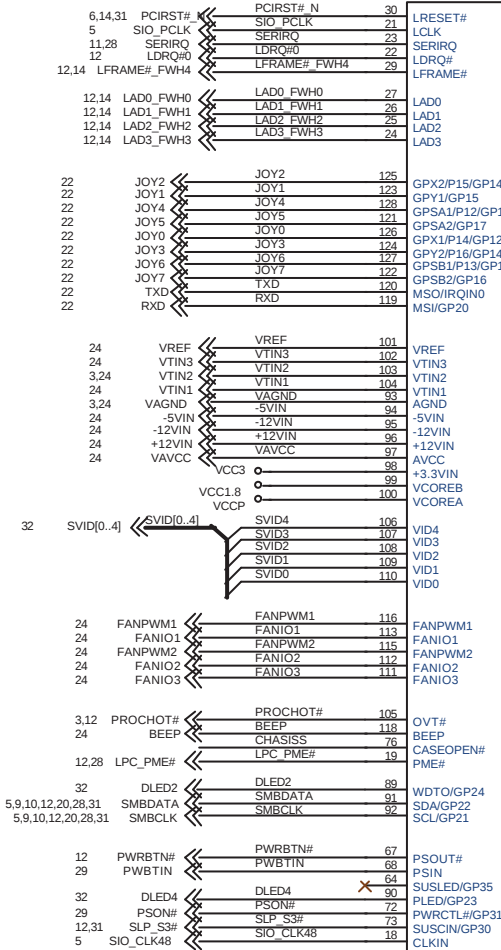
IR HEADER



Distribute near the VCC power pin of the LPC



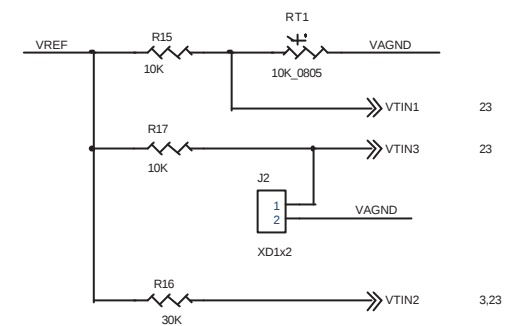
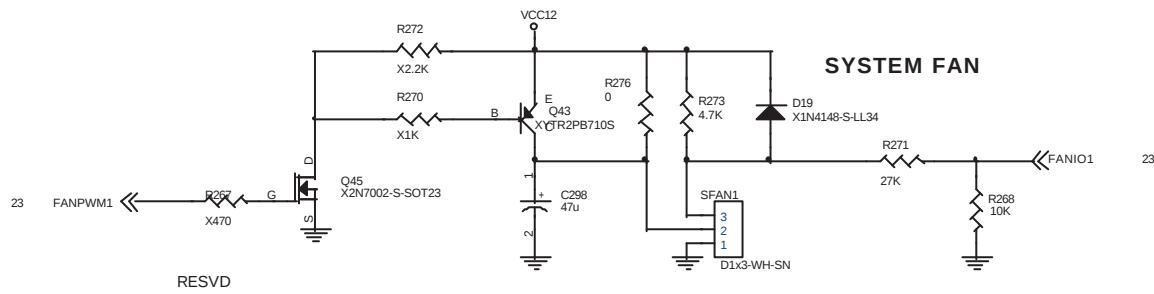
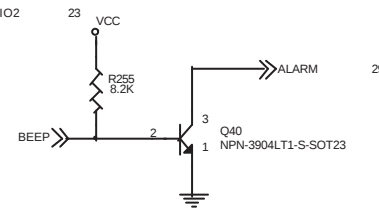
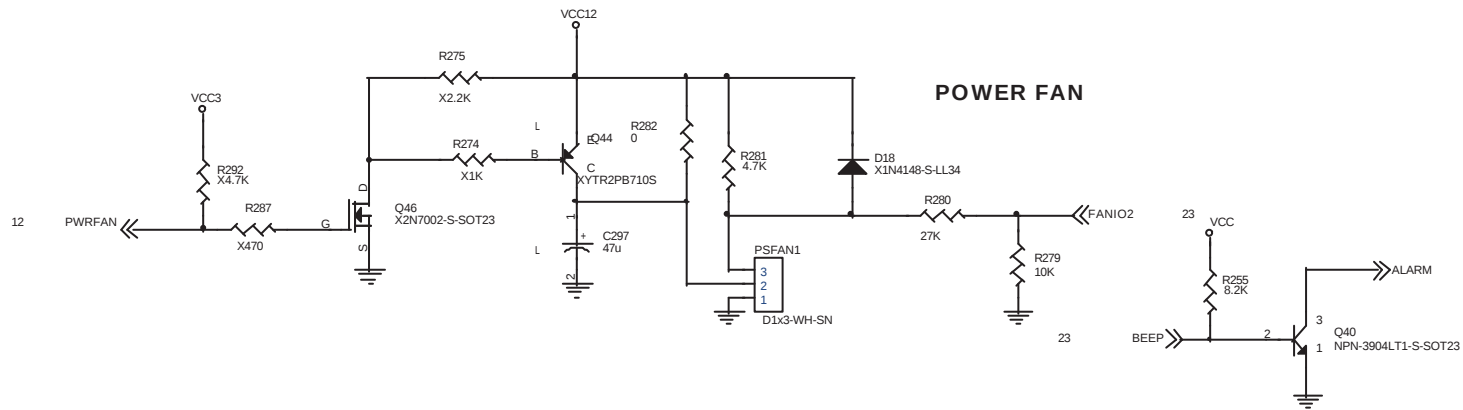
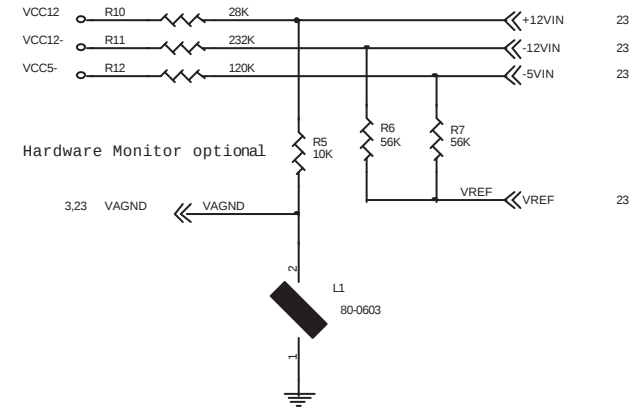
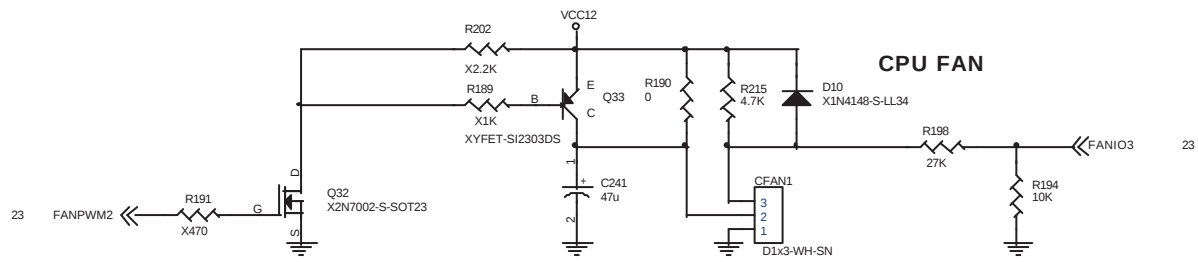
SIO



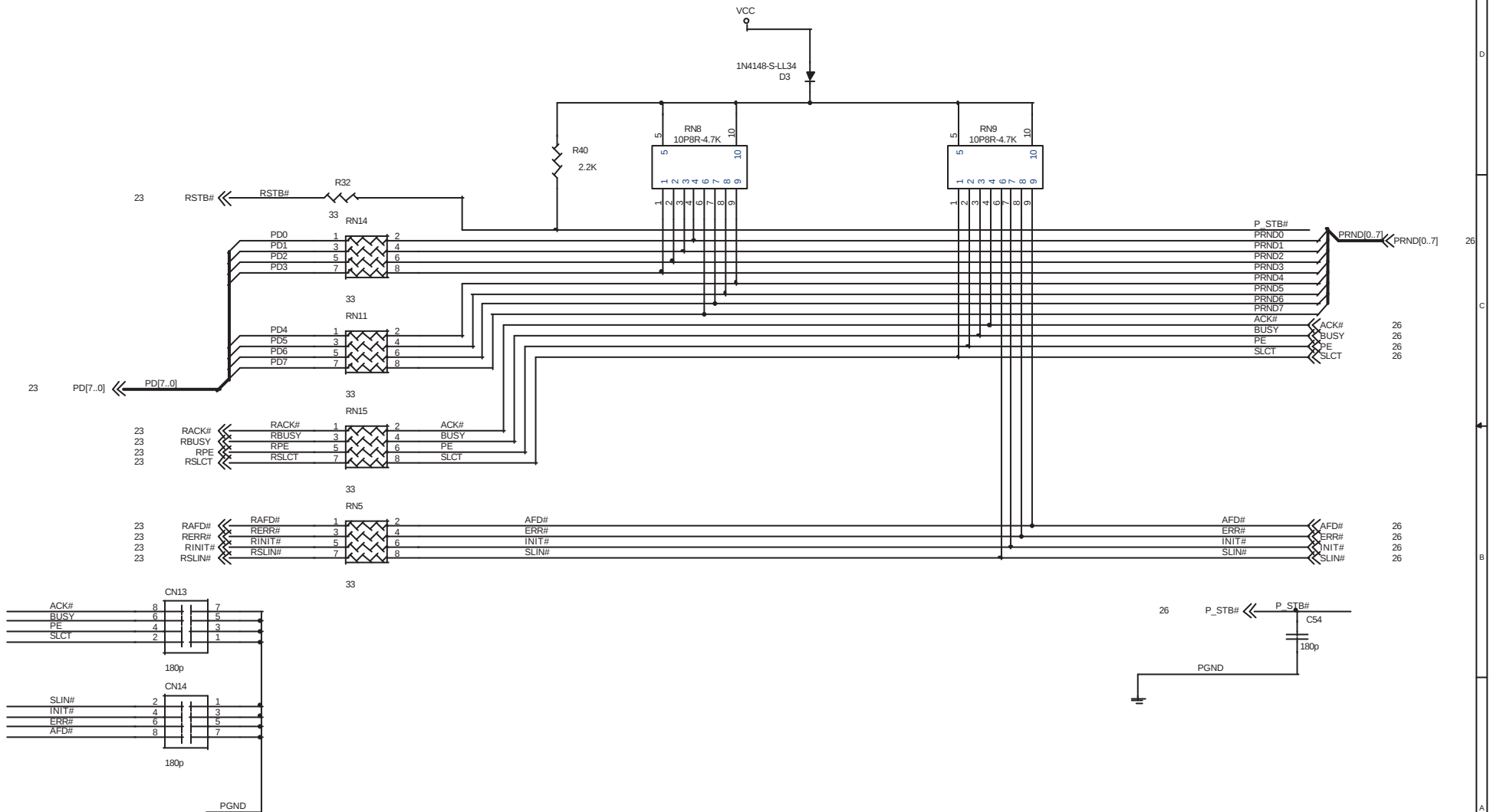
83627HF-REV6

WB-W83627HF-AW-VG

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LPC SIO		
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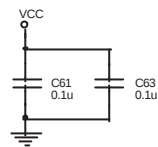
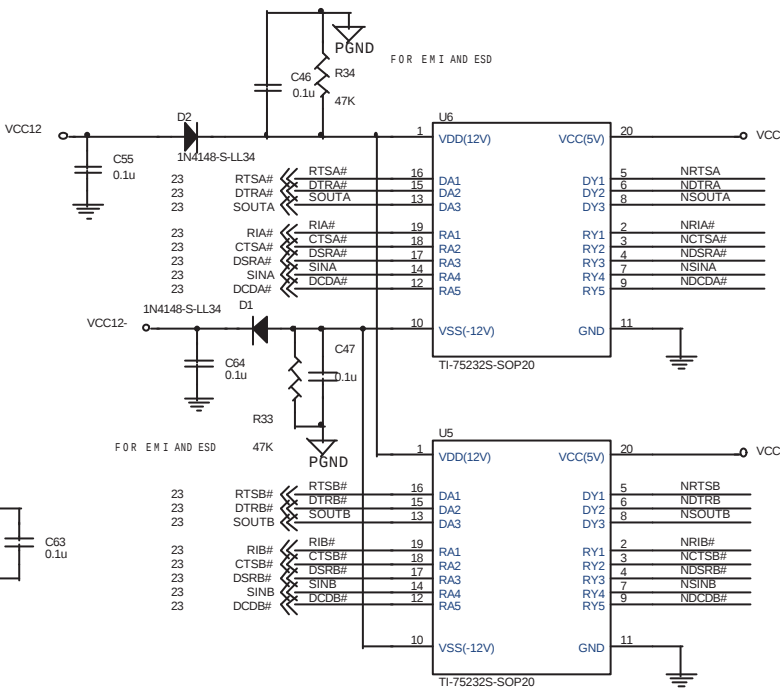
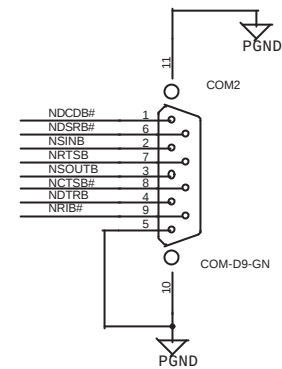
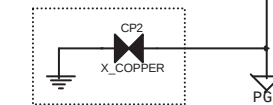
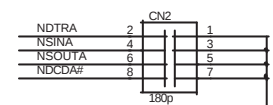
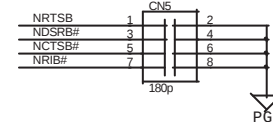
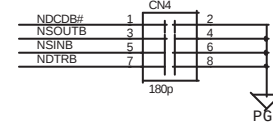
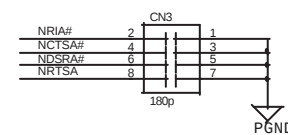
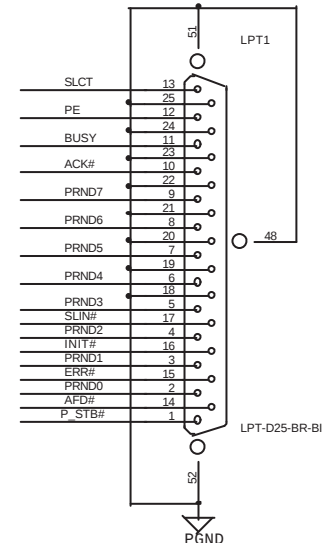
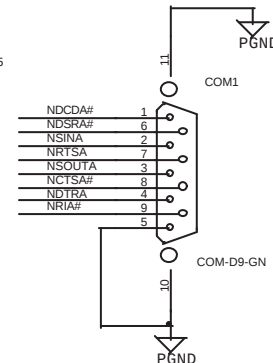
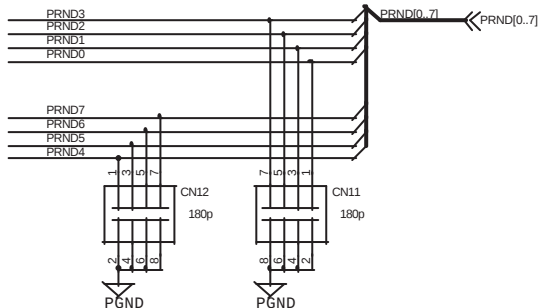


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Hardware Monitor		
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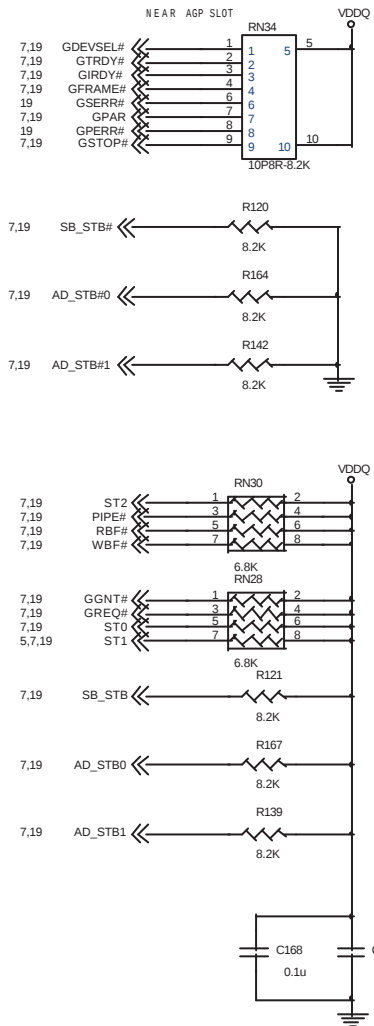
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 PE <> PE 25
 SLCT <> SLCT 25
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 ERR# <> ERR# 25
 INIT# <> INIT# 25
 SLIN# <> SLIN# 25
 P_STB# <> P_STB# 25



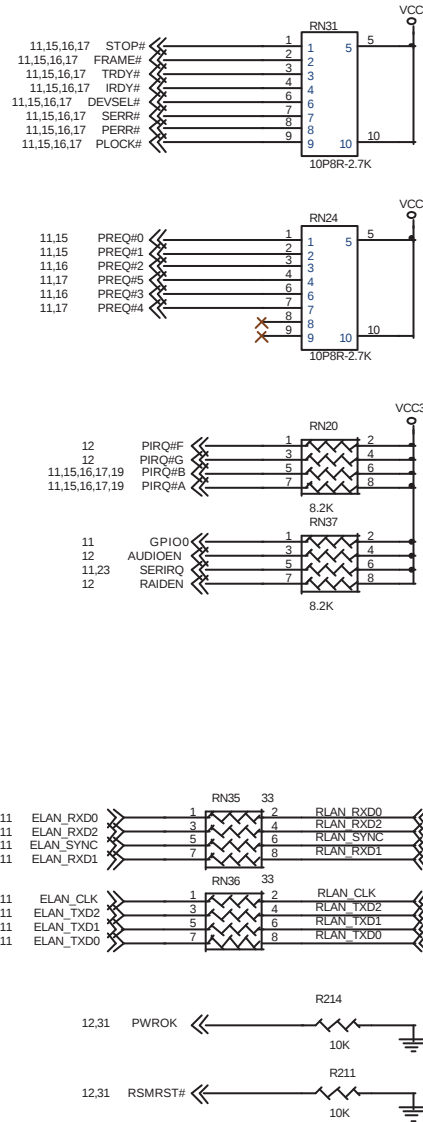
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File	LPT/COM Port	
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PULL-UP RESISTORS

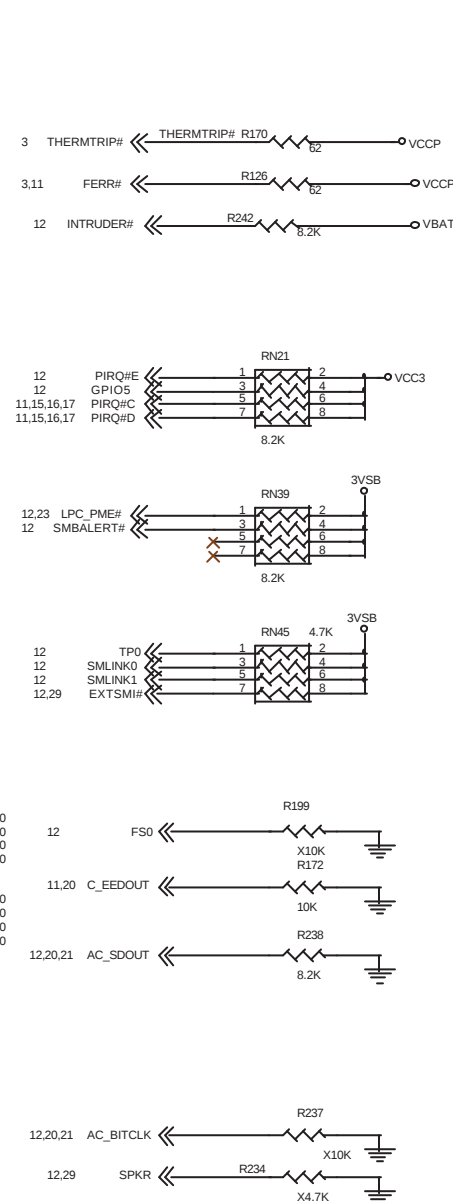
AGP



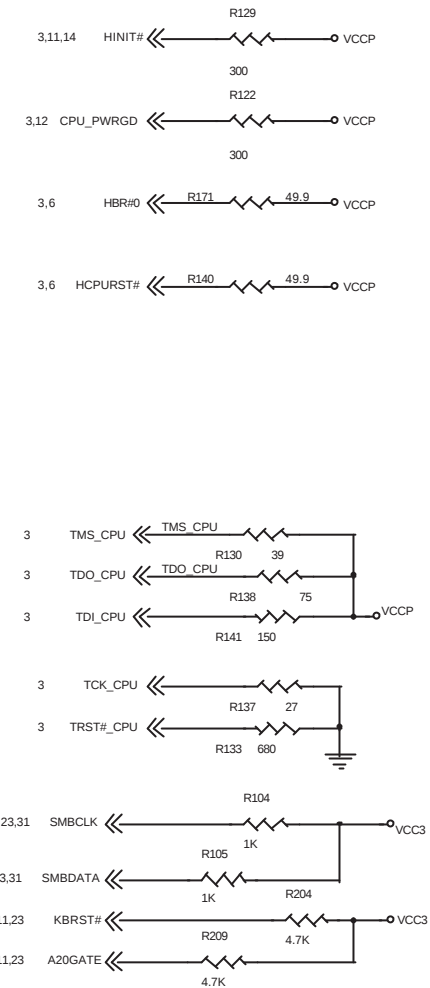
PCI BUS



ICH



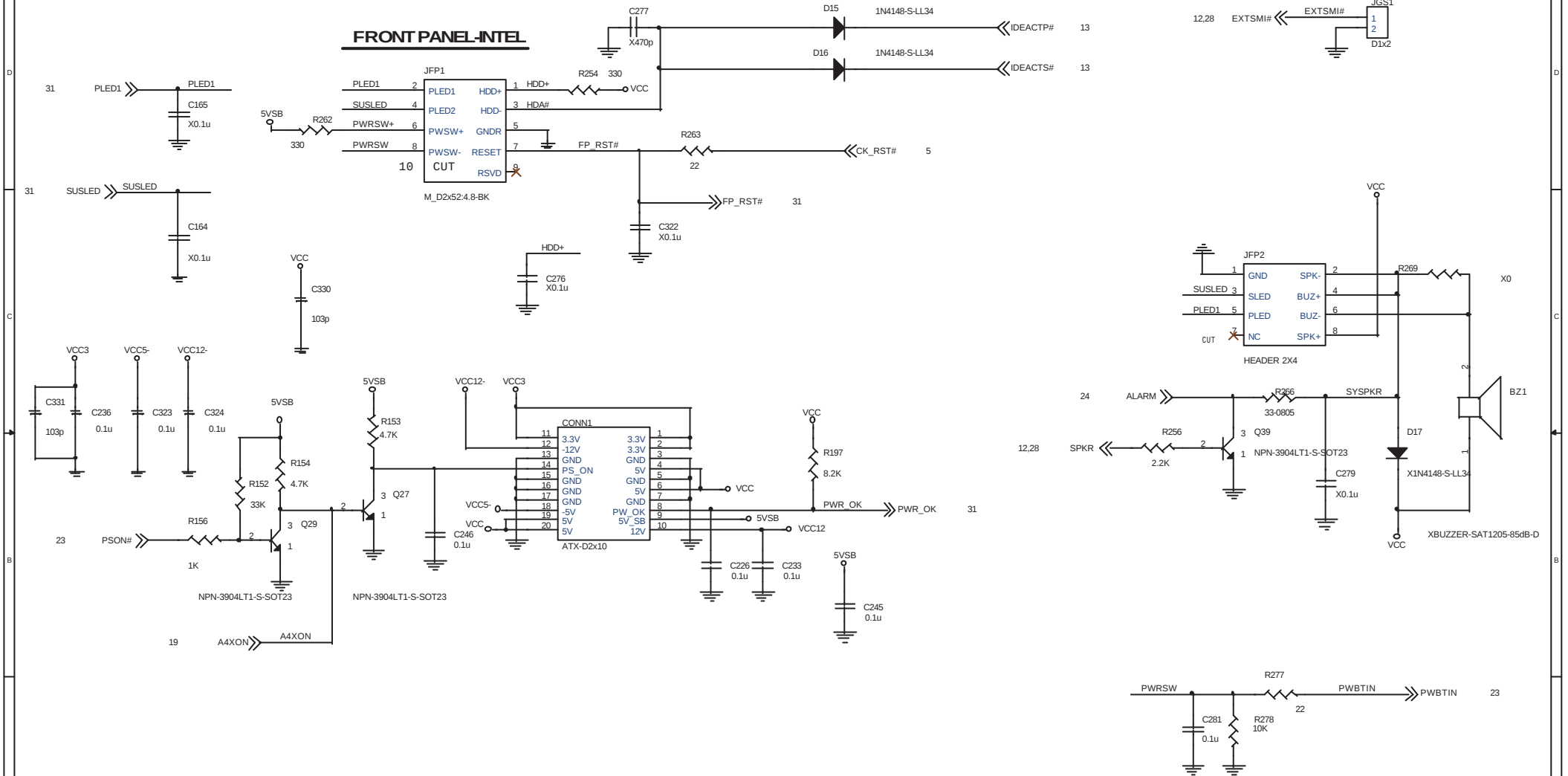
CPU



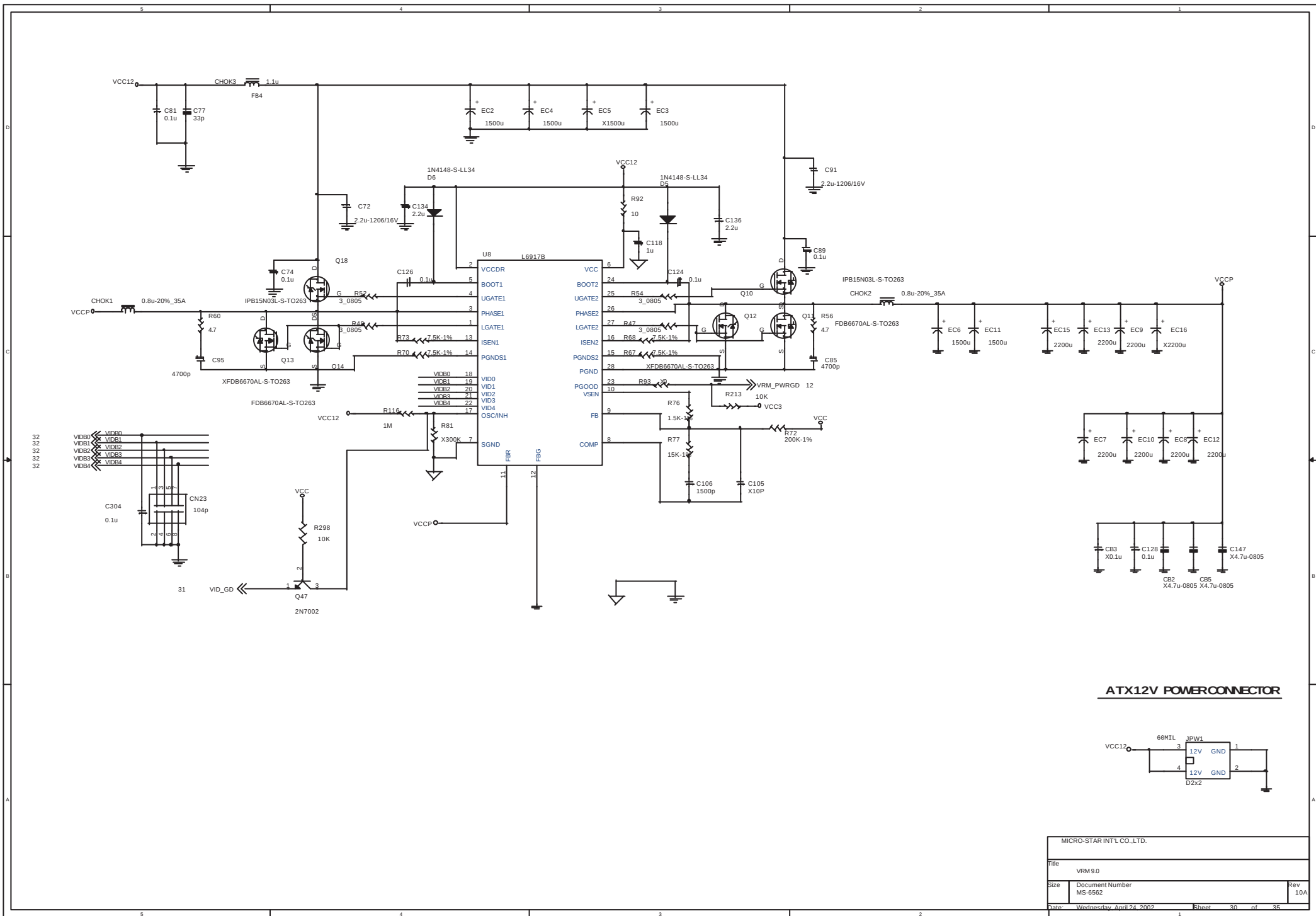
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Pull-up Resistors		
Size	Document Number	Rev
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Front Pannel & ATX Power Connector

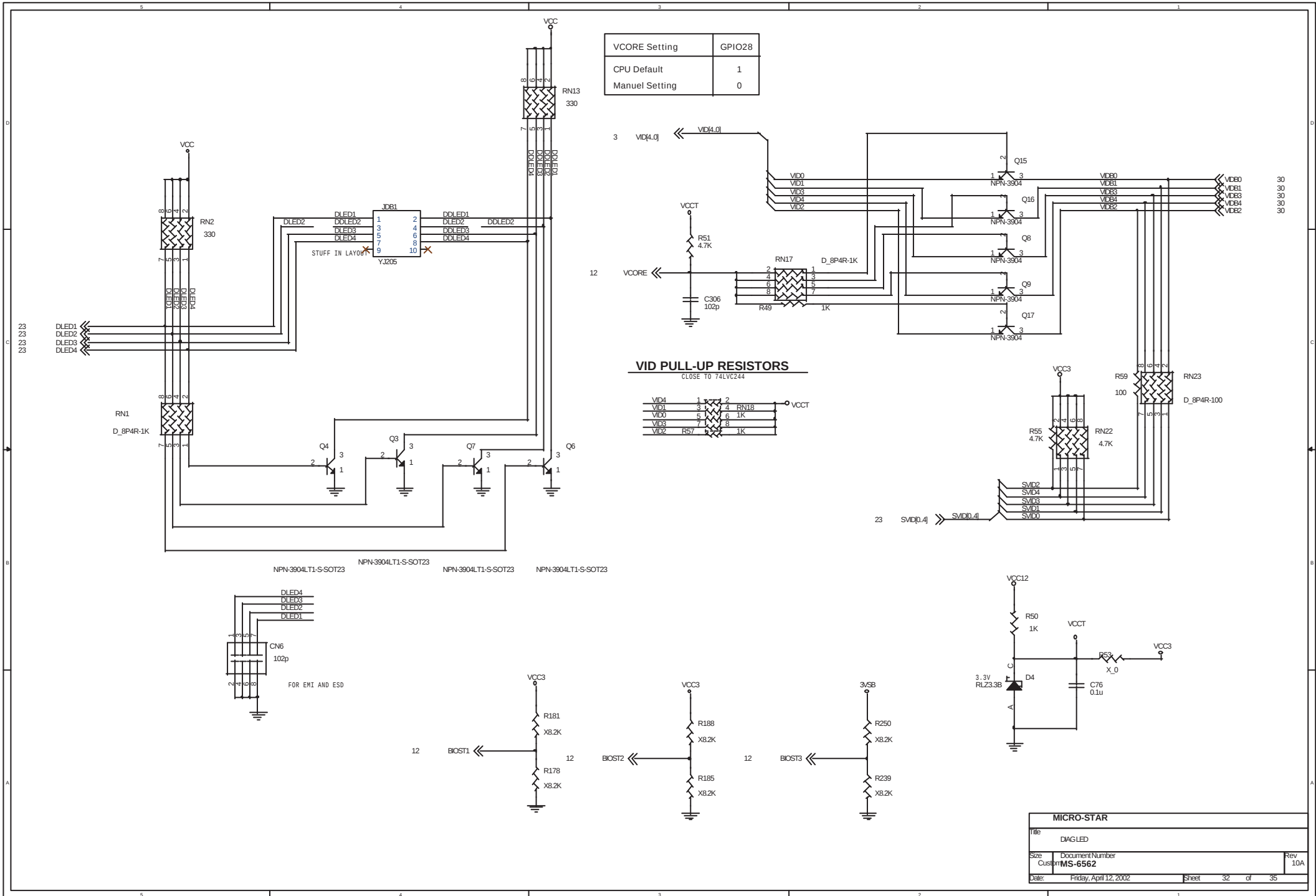
FRONT PANEL-INTEL



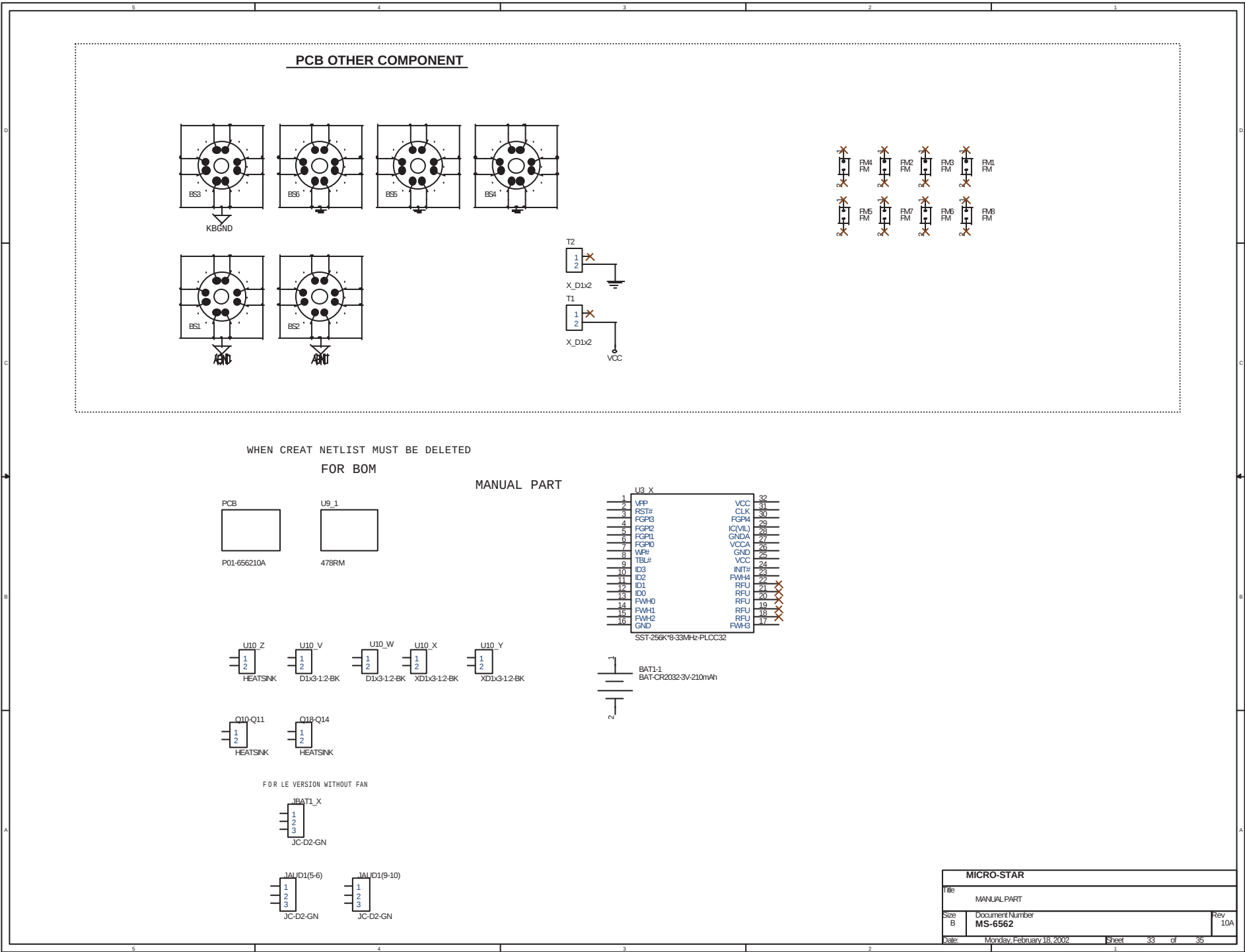
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Title		
Front Pannel & ATX Power Connector		
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VCORE Setting	GPIO28
CPU Default	1
Manuel Setting	0



MICRO-STAR			
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A	Revision Initial ver: 0A on 10/15/01 Schematic Initial Revision 0A. GERBER RELEASE 11/06/01 Revision change from ver: 0A to ver: 0B on 12/6/01 GERBER RELEASE 12/05/01 P - 27 JWOL1 RENAME JWL1 JMDM1 RENAME JWR1 P - 29 DELETE JGL1 CIRCUIT AND USE MS-5'S POWER LED FUNCTION DELETE JFP2 (MSI STANDARD FRONT SIDE CONNECT) CHANGE TO INTEL SOLUTION P - 30 DELETE Q23 BECAUSE VID_G0 ACTIVE LOWER FROM MS-5 SO IT DID NOT NEED INVERTER AGAIN P - 31 Q38 D AND S ERROR SO IT CAN NOT ADJUST VOLTAGE AND U12.7 CHANGE TO SMBCLK U12.6 CHANGE TO SMBDATA, U12.34 ADD U12.35 ADD A SERIER 0 OHM RESISTOR FOR CHANGE VERSION USE 1.8VSB CIRCUIT CHANGE P - 32 JOB1.7 CHANGE TO DLED4 AND PIN8 IS DDLED4 DELETE RW19,RS8 P - 33 ADD MOS HEADSINK				
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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	PULL UP VCC3.8.2K
GPIO 1	I	REQ#5
GPIO 2~4	I	PIRQE~F#
GPIO 5	I	PIRQH#
GPIO 6	I	BIOST1
GPIO 7	I	BIOST2
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data1 In
GPIO 10	I	Not Implemented
GPIO 11	I	SMBALTER#
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	GNT5#
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	VCORE
GPIO 21	O	Not Implemented
GPIO 22	OD	PWRFAN
GPIO 23	O	BIOS WP
GPIO 24	O	BIOST3
GPIO 25	O	Not Implemented
GPIO 26	O	Not Implemented
GPIO 27	I/O	Not Implemented
GPIO 28	I/O	Not Implemented
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DLED-Super I/O

GPIO Pin	Type	Function
GP32	I/OD	DLED1
GP24	I/OD	DLED2
GP34	I/OD	DLED3
GP33	I/OD	RSMRST#
GP23	I/OD	DLED4

DEVICE	ICH INT Pin	IDSEL	
PCI Slot 1	INTA# INTB# INTC# INTD#	AD 16	PREQ0# PGNT0# PCLK1
PCI Slot 2	INTB# INTC# INTD# INTA#	AD 17	PREQ1# PGNT1# PCLK2
PCI Slot 3	INTC# INTD# INTA# INTB#	AD 18	PREQ2# PGNT2# PCLK3
PCI Slot 4	INTD# INTA# INTB# INTC#	AD 19	PREQ3# PGNT3# PCLK4
PCI Slot 5	INTB# INTC# INTD# INTA#	AD 21	PREQ4# PGNT4# PCLK5
PCI Slot6	INTA# INTB# INTC# INTD#	AD 20	PREQ7# PGNT7# PCLK7

MICRO-STAR			
Title			
GPIO SPEC			
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