MS-6561 VER:1.0

CPU: AMD Socket-462 Processor

Chipset: SiS 745

LPC I/O: W83697HF

AC'97 CODEC:Realtek ALC201A

IEEE1394 : TI TSB41LV02(OPTION)

Expansion:

1.AGP Slot * 1
2.PCI Slot * 5
3.CNR Slot * 1

Title: Cover Sheet		Rev: 1.0
Document Number: MS-6561		
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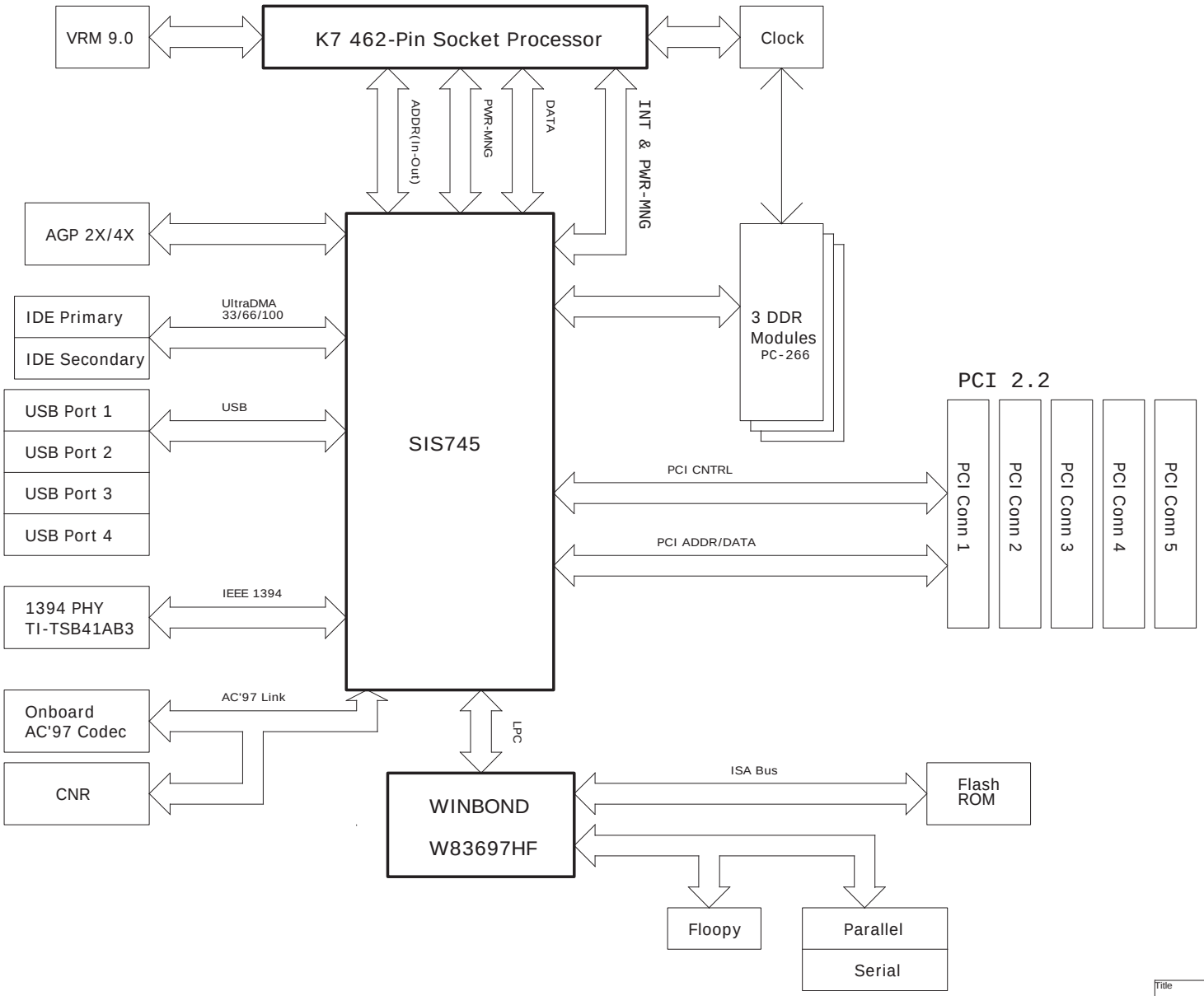

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Title	Block Diagram	Rev
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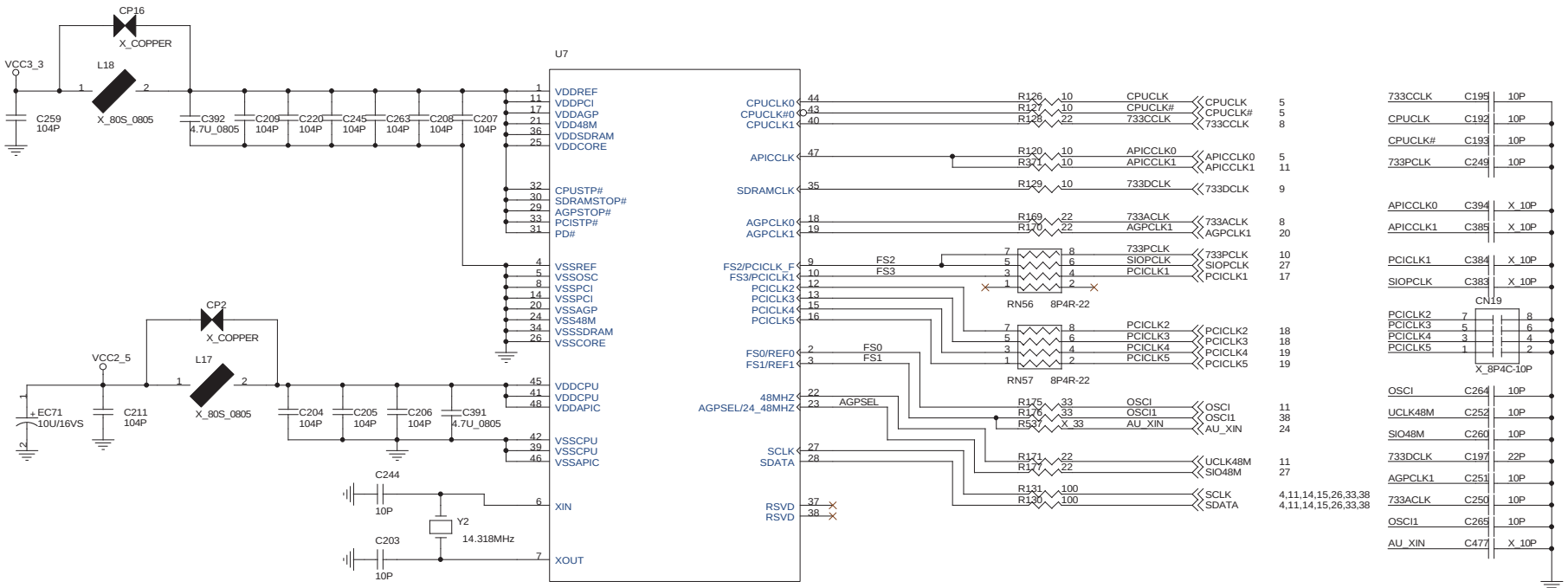

ICS9248-199

SIS745 CLOCK							AGPCLK (MHz)	
(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0	AGPSEL=1
0	0	0	0	66.6	66.6	33.3	66.6	50
0	0	0	1	100	100	33.3	66.6	50
0	0	1	0	166	166	33.3	66.6	55.6
0	0	1	1	133	133	33.3	66.6	50
0	1	0	0	66.6	100	33.3	66.6	50
0	1	0	1	100	66.6	33.3	66.6	50
0	1	1	0	100	133	33.3	66.6	50
0	1	1	1	133	100	33.3	66.6	50
1	0	0	0	112	112	33.6	67.2	56
1	0	0	1	124	124	31	62	46.5
1	0	1	0	138	138	34.5	69	51.8
1	0	1	1	150	150	30	60	50
1	1	0	0	66.6	133	33.3	62.5	49.84
1	1	0	1	133	166	33.3	66.6	55.3
1	1	1	0	150	100	30	60	50
1	1	1	1	160	120	30	60	48

NOTE:
PCICLK<34.5MHz

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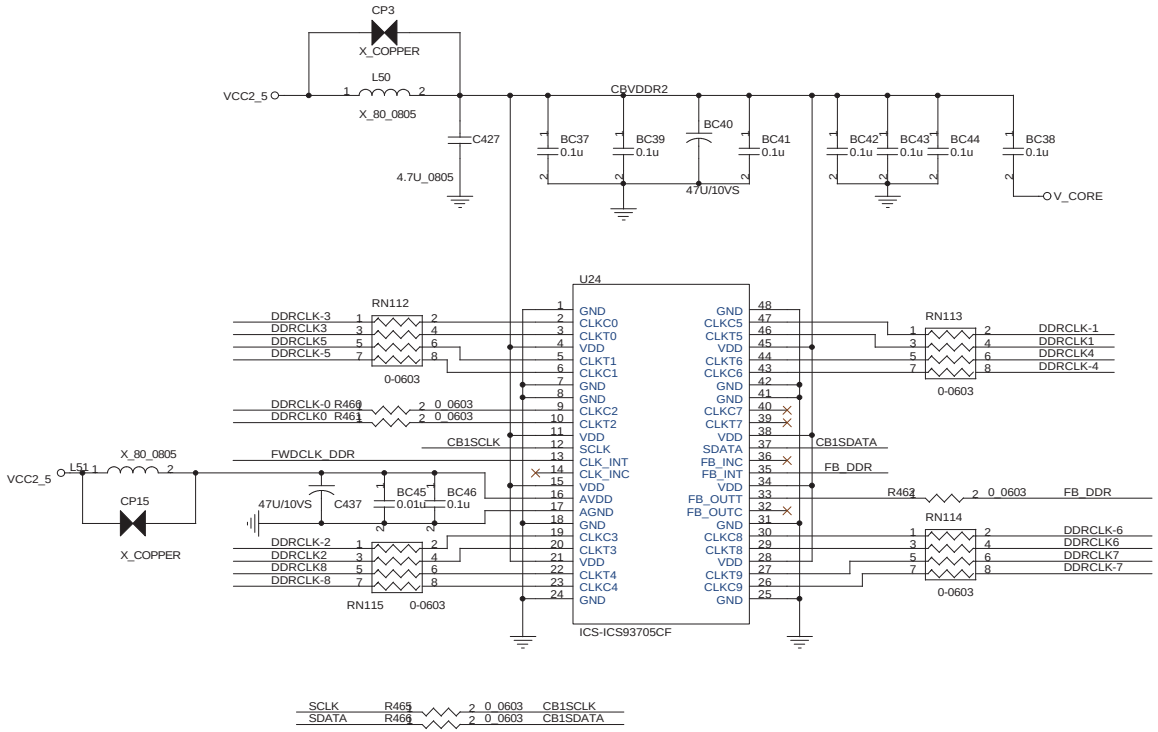
Clock Buffer (DDR)



DDRCLK[0..8] — DDRCLK[0..8] 14,15

DDRCLK-[0..8] — DDRCLK-[0..8] 14,15

SCLK — SCLK 3,11,14,15,26,33,38

SDATA — SDATA 3,11,14,15,26,33,38

FWDCLK_DDR — FWDCLK_DDR 9

By-Pass Capacitors
Place near to the Clock Buffer

DDRCLK3	C428	10p-0603
DDRCLK-5	C429	10p-0603
DDRCLK0	C430	10p-0603
DDRCLK-2	C431	10p-0603
DDRCLK-1	C432	10p-0603
DDRCLK-8	C433	10p-0603
DDRCLK4	C434	10p-0603
DDRCLK7	C435	10p-0603
DDRCLK6	C436	10p-0603
DDRCLK-3	C438	10p-0603
DDRCLK5	C439	10p-0603
DDRCLK-0	C440	10p-0603
DDRCLK2	C441	10p-0603
DDRCLK1	C442	10p-0603
DDRCLK8	C443	10p-0603
DDRCLK-4	C444	10p-0603
DDRCLK-7	C445	10p-0603
DDRCLK-6	C446	10p-0603
FB_DDR	C447	10p-0603

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Title	Clock Buffer	Rev
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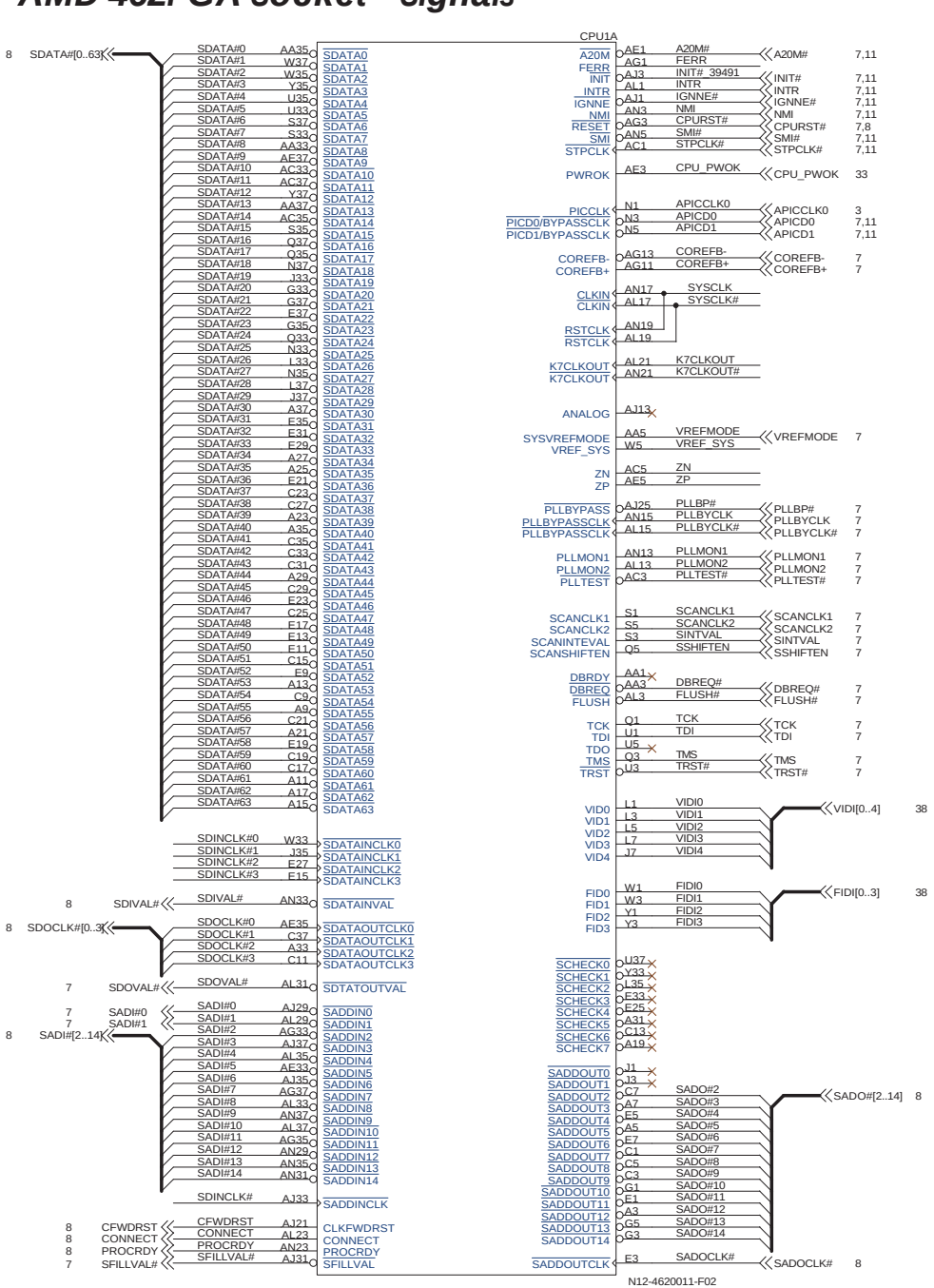
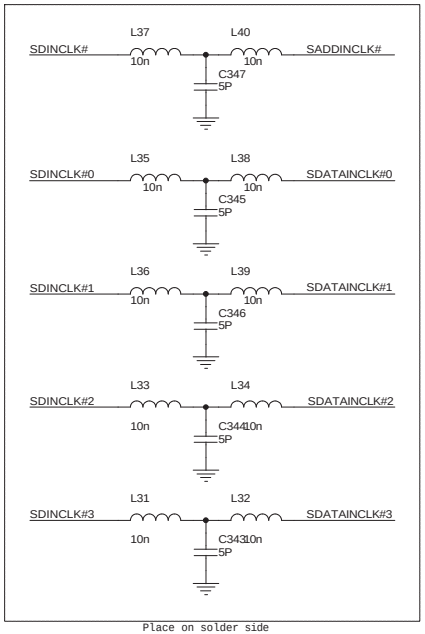
AMD 462PGA Socket - Signals

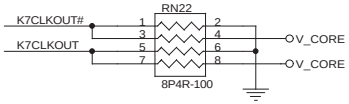


N12-4620011-F02



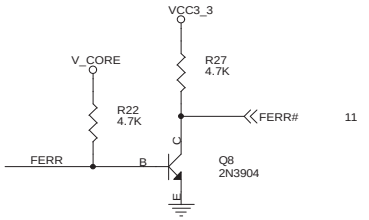
Place on solder side

CPU K7CLKOUT BLOCK

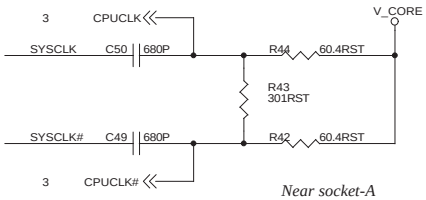


**** Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"***

CPU FERR BLOCK

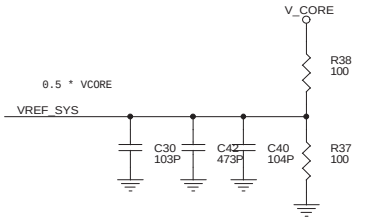


CPU SYSCLK BLOCK

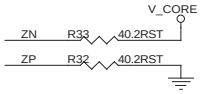


Near socket-A

CPU SYSCLK REFERNCE BLOCK



CPU ZN / ZP BLOCK



match the transmission line

Push-pull compensation circuit

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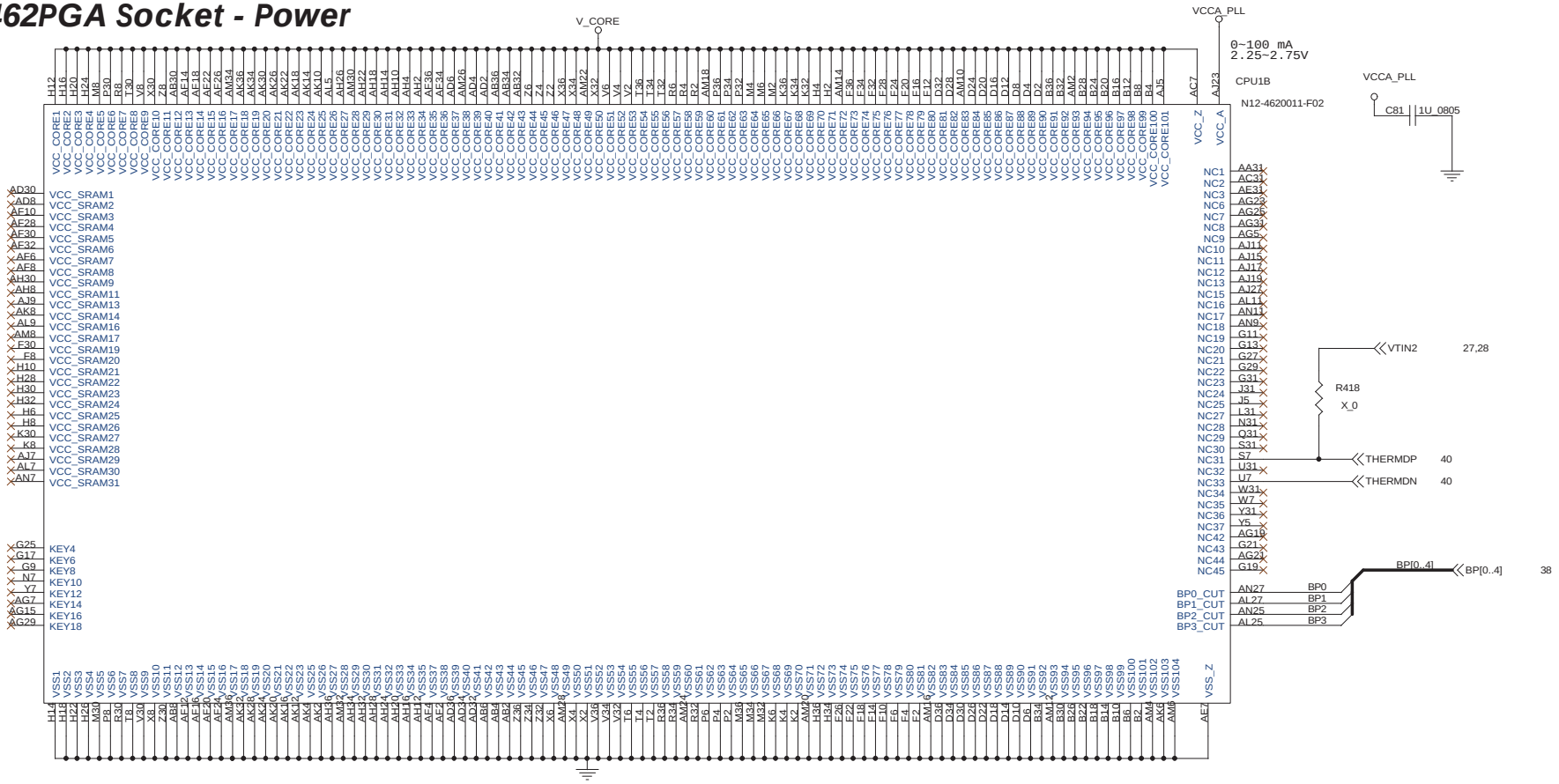
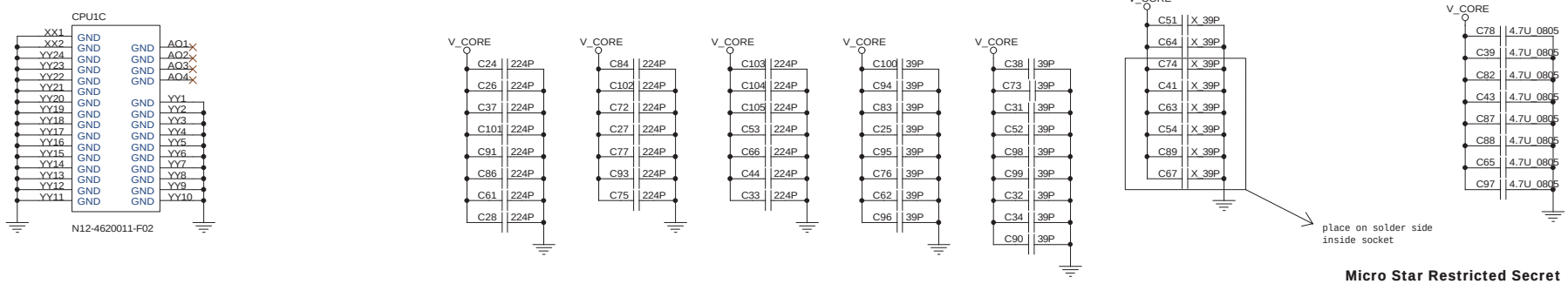
AMD 462PGA Socket - Power



CPU DECOUPLING CAPACITORS



DECOUPLING CAPACITOR INSIDE SOCKET

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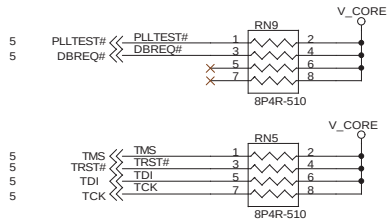
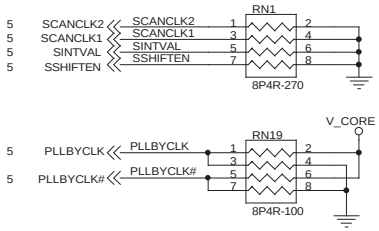
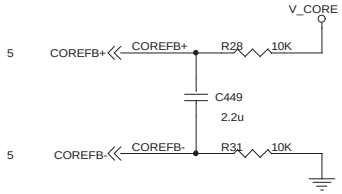
AMD 462PGA Socket - Pull up / down Block

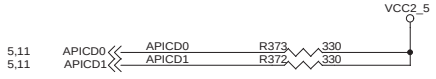






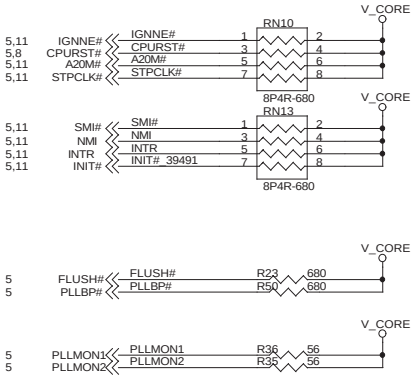
**All CPU interface are
2.5V tolerant**

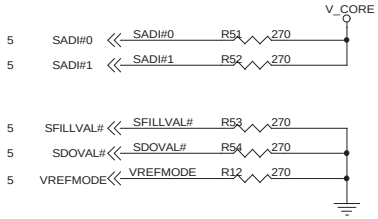
CPU APIC BLOCK



for test only
Pull to VCCA_PLL

CPU PULL-UP / DOWN BLOCK





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Title	Socket A_Pull up / Pull down	Rev
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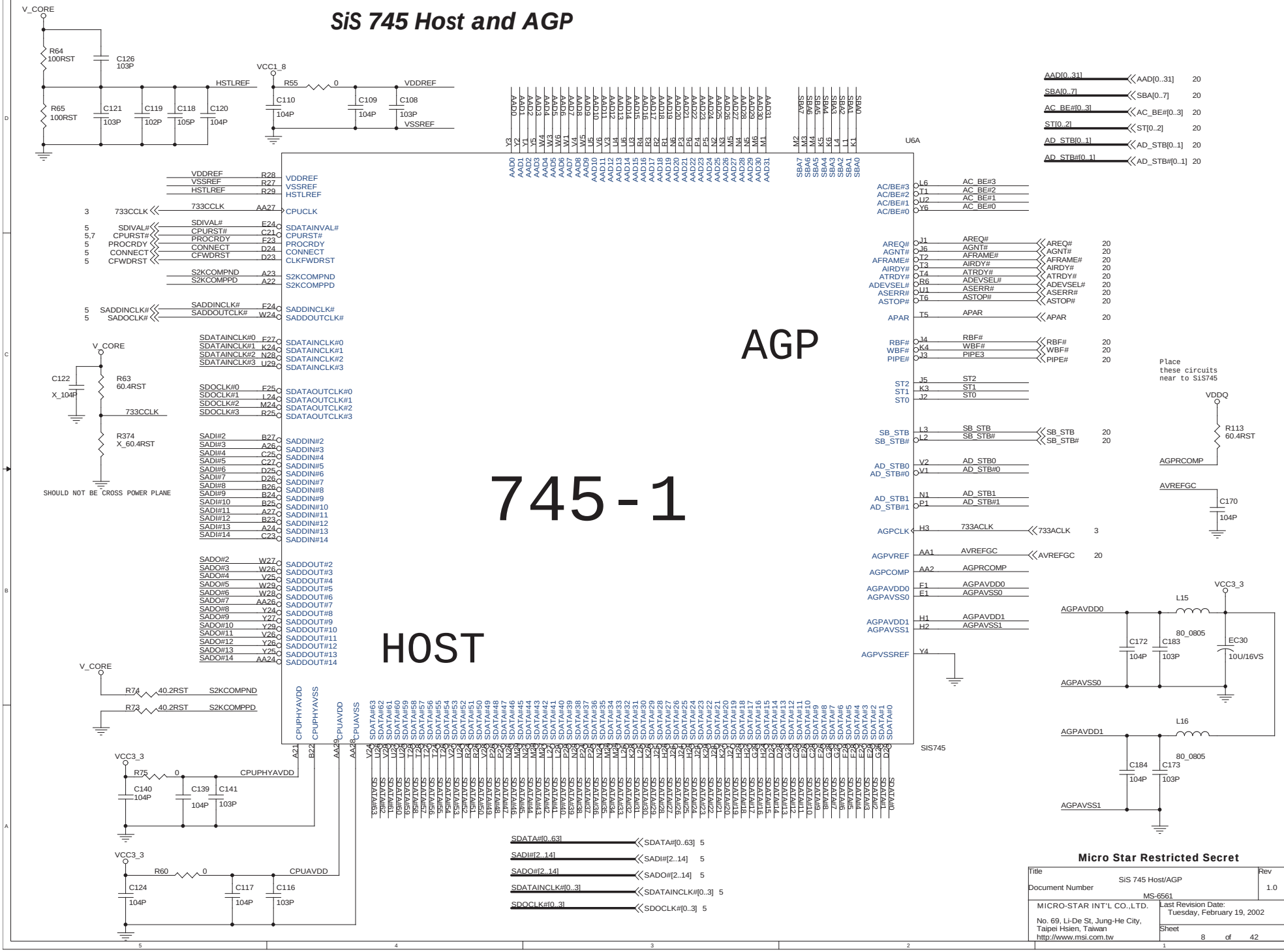
SiS 745 Host and AGP



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Title	SiS 745 Host/AGP	Rev 1.0
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SiS 745 Memory

RN88 10-0603
DMD1 1 2 MD1
DMD5 3 4 MD5
DMD0 5 6 MD0
DMD4 7 8 MD4

RN90 10-0603
DMD6 1 2 MD6
DMD2 3 4 MD2
DDQS0 5 6 DQS0
DDQM0 7 8 DQM0

RN91 10-0603
DMD8 1 2 MD8
DMD13 3 4 MD13
DMD3 5 6 MD3
DMD7 7 8 MD7

RN93 10-0603
DMD11 1 2 MD11
DMD10 3 4 MD10
DMD15 5 6 MD15
DMD14 7 8 MD14

RN95 10-0603
DDQM1 1 2 DQM1
DDQS1 3 4 DQS1
DMD9 5 6 MD9
DMD12 7 8 MD12

RN97 10-0603
DMD17 1 2 MD17
DDQS2 3 4 DQS2
DMD16 5 6 MD16
DMD20 7 8 MD20

RN99 10-0603
DMD22 1 2 MD22
DMD18 3 4 MD18
DDQM2 5 6 DQM2
DMD21 7 8 MD21

RN94 10-0603
DMD28 8 7 MD28
DMD24 6 5 MD24
DMD23 4 3 MD23
DMD19 2 1 MD19

RN92 10-0603
DMD31 8 7 MD31
DMD27 6 5 MD27
DMD30 4 3 MD30
DMD26 2 1 MD26

RN103 10-0603
DDQM3 1 2 DQM3
DDQS3 3 4 DQS3
DMD25 5 6 MD25
DMD29 7 8 MD29

RN104 10-0603
DMD33 1 2 MD33
DMD37 3 4 MD37
DMD32 5 6 MD32
DMD36 7 8 MD36

RN105 10-0603
DMD38 1 2 MD38
DDQM4 3 4 DQM4
DDQS4 5 6 DQS4
DMD34 7 8 MD34

RN102 10-0603
DMD40 8 7 MD40
DMD44 6 5 MD44
DMD35 4 3 MD35
DMD39 2 1 MD39

RN107 10-0603
DDQM5 1 2 DQM5
DMD41 3 4 MD41
DDQS5 5 6 DQS5
DMD45 7 8 MD45

RN108 10-0603
DMD47 1 2 MD47
DMD46 3 4 MD46
DMD43 5 6 MD43
DMD42 7 8 MD42

RN109 10-0603
DMD55 1 2 MD55
DMD54 3 4 MD54
DDQS6 5 6 DQS6
DDQM6 7 8 DQM6

RN110 10-0603
DMD53 1 2 MD53
DMD49 3 4 MD49
DMD52 5 6 MD52
DMD48 7 8 MD48

RN111 10-0603
DMD56 1 2 MD56
DMD60 3 4 MD60
DMD51 5 6 MD51
DMD50 7 8 MD50

RN87 10-0603
DDQS7 1 2 DQS7
DDQM7 3 4 DQM7
DMD61 5 6 MD61
DMD57 7 8 MD57

RN89 10-0603
DMD59 1 2 MD59
DMD63 3 4 MD63
DMD58 5 6 MD58
DMD62 7 8 MD62

DMD[0..63] DMD[0..63] 14,15,16
DDQM[0..7] DDQM[0..7] 14,15,16
DMA[0..14] DMA[0..14] 14,15,16
DDQS[0..7] DDQS[0..7] 14,15,16
DCS-[0..5] DCS-[0..5] 14,15,16

U6B

MD0 AD28 MD0
MD1 AB26 MD1
MD2 AC26 MD2
MD3 AC24 MD3
MD4 AD29 MD4
MD5 AB25 MD5
MD6 AD26 MD6
MD7 AE29 MD7
DQM0 AB24 DQM0
DQS0 AD27 DQS0
MD8 AE29 MD8
MD9 AD25 MD9
MD10 AG29 MD10
MD11 AF26 MD11
MD12 AE28 MD12
MD13 AE27 MD13
MD14 AD24 MD14
MD15 AH28 MD15
DQM1 AE26 DQM1
DQS1 AE27 DQS1
MD16 AG26 MD16
MD17 AE24 MD17
MD18 AJ26 MD18
MD19 AJ25 MD19
MD20 AG27 MD20
MD21 AJ27 MD21
MD22 AH25 MD22
MD23 AG25 MD23
DQM2 AE25 DQM2
DQS2 AH27 DQS2
MD24 AE22 MD24
MD25 AD21 MD25
MD26 AH22 MD26
MD27 AD20 MD27
MD28 AE22 MD28
MD29 AG23 MD29
MD30 AE21 MD30
MD31 AE21 MD31
DQM3 AG22 DQM3
DQS3 AJ23 DQS3
MD32 AE18 MD32
MD33 AE18 MD33
MD34 AH18 MD34
MD35 AG17 MD35
MD36 AD17 MD36
MD37 AH19 MD37
MD38 AG18 MD38
MD39 AE17 MD39
DQM4 AD16 DQM4
DQS4 AJ18 DQS4
MD40 AE15 MD40
MD41 AG14 MD41
MD42 AJ13 MD42
MD43 AD13 MD43
MD44 AD14 MD44
MD45 AJ15 MD45
MD46 AH13 MD46
MD47 AG13 MD47
DQM5 AE14 DQM5
DQS5 AJ14 DQS5
MD48 AE13 MD48
MD49 AD12 MD49
MD50 AE12 MD50
MD51 AE12 MD51
MD52 AJ12 MD52
MD53 AE13 MD53
MD54 AD11 MD54
MD55 AJ11 MD55
DQM6 AG12 DQM6
DQS6 AH12 DQS6
MD56 AG11 MD56
MD57 AF11 MD57
MD58 AG10 MD58
MD59 AE9 MD59
MD60 AE10 MD60
MD61 AJ10 MD61
MD62 AE10 MD62
MD63 AJ9 MD63
DQM7 AD10 DQM7
DQS7 AH10 DQS7

SIS745

MA0 AD18 MA0
MA1 AG20 MA1
MA2 AD19 MA2
MA3 AE20 MA3
MA4 AJ21 MA4
MA5 AH24 MA5
MA6 AJ24 MA6
MA7 AG24 MA7
MA8 AD22 MA8
MA9 AE23 MA9
MA10 AF19 MA10
MA11 AJ17 MA11
MA12 AG19 MA12
MA13 AD23 MA13
MA14 AF24 MA14

RN101 8P4R-0
MA0 2 1 DMA0
MA1 4 3 DMA1
MA2 6 5 DMA2
MA3 8 7 DMA3

RN100 8P4R-0
MA4 2 1 DMA4
MA6 4 3 DMA6
MA5 6 5 DMA5
MA8 8 7 DMA8

RN96 8P4R-0
MA10 1 2
MA12 3 4 DMA10
MA11 5 6 DMA12
7 8 DMA11

RN98 8P4R-0
MA14 1 2 DMA14
MA13 3 4 DMA13
MA9 5 6 DMA9
MA7 7 8 DMA7

RAS# AG16 RAS# R447 0 DRAS- DRAS- 14,15,16
CAS# AD15 CAS# R448 0 DCAS- DCAS- 14,15,16
WE# AE16 DDWE# R449 0 DWE- DWE- 14,15,16

RN106 8P4R-0
CSA#0 AE16 8 7 DCS-2
CSA#1 AH16 6 5 DCS-0
CSA#2 AJ16 4 3 DCS-3
CSA#3 AH15 2 1 DCS-1
CSA#4 AG15
CSA#5 AE15
R450 0 DCS-4
R451 0 DCS-5

CKE C10 735CKE R453 0 MCKE MCKE 15,34
SDCLK AB27 733DCLK 733DCLK 3
SDRCLKI AJ20
FWDSDCLKO AJ19 R455 22 FWDCLK_DDR FWDCLK_DDR 4
C426 10P

SDAVDD AB29 SDAVDD
SDAVSS AB28 SDAVSS
DDRAVDD AC29 DDRAVDD
DDRAVSS AC27 DDRAVSS
DDRVREFH AJ22 DDRVREFH
DDRVREF AH21 DDRVREF0
DDRVREFL AG21 DDRVREFL
DDRVSSREF AE19

VCC3_3
SDAVDD L48 121S
C422 104P C423 103P EC60 X_10U/16VS
SDAVSS

VCC3_3
DDRAVDD L49 121S
C424 104P C425 103P EC61 10U/16VS
DDRAVSS

VCC2_5
BC31 0.1u R452 191RST
DDRVREFH
BC32 0.1u R454 274RST

VCC2_5
BC34 0.1u R457 274RST
DDRVREFL
BC36 0.1u R459 191RST

VCC2_5
BC33 0.1u R456 150RST
DDRVREF0
BC35 0.1u R458 143RST

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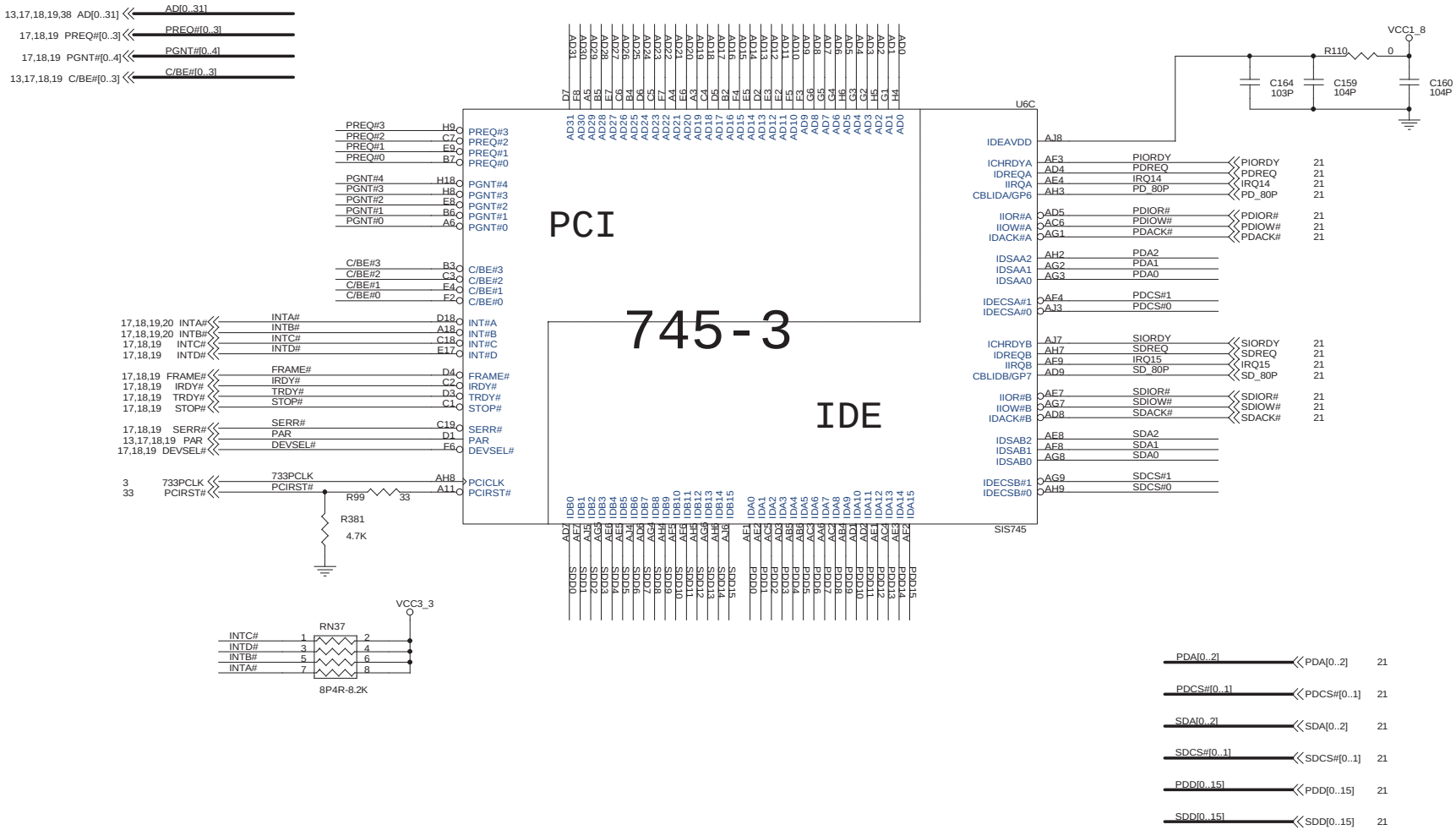
SiS 745 PCI and IDE



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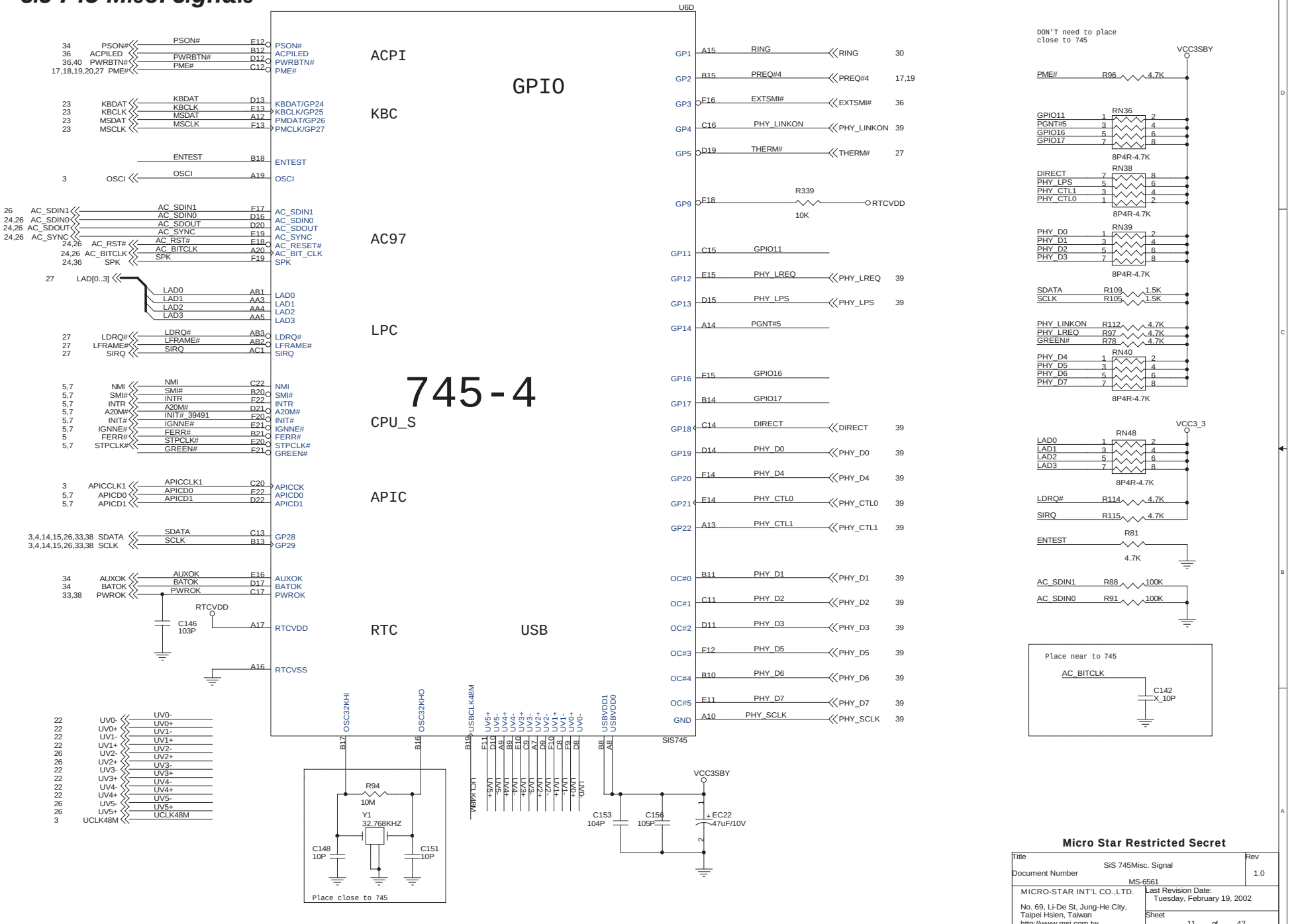
SiS 745 Misc. Signals



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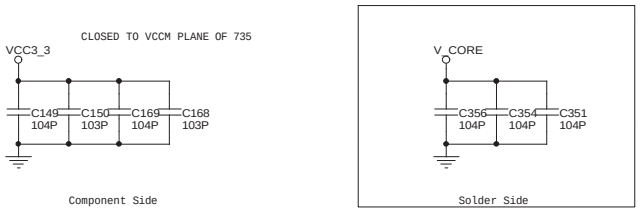
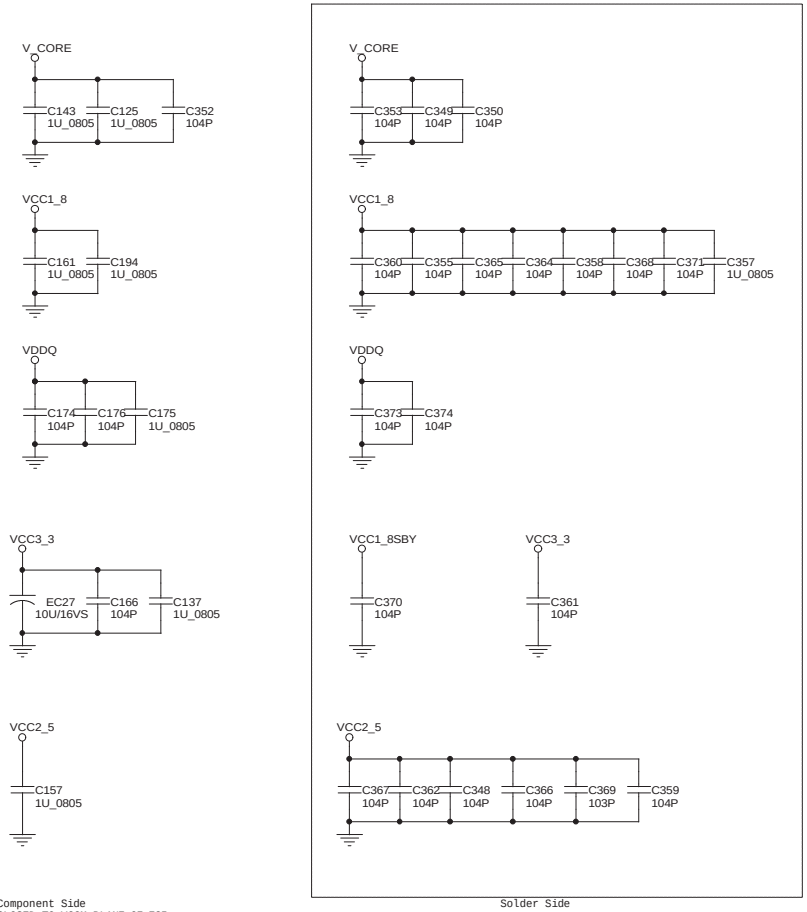
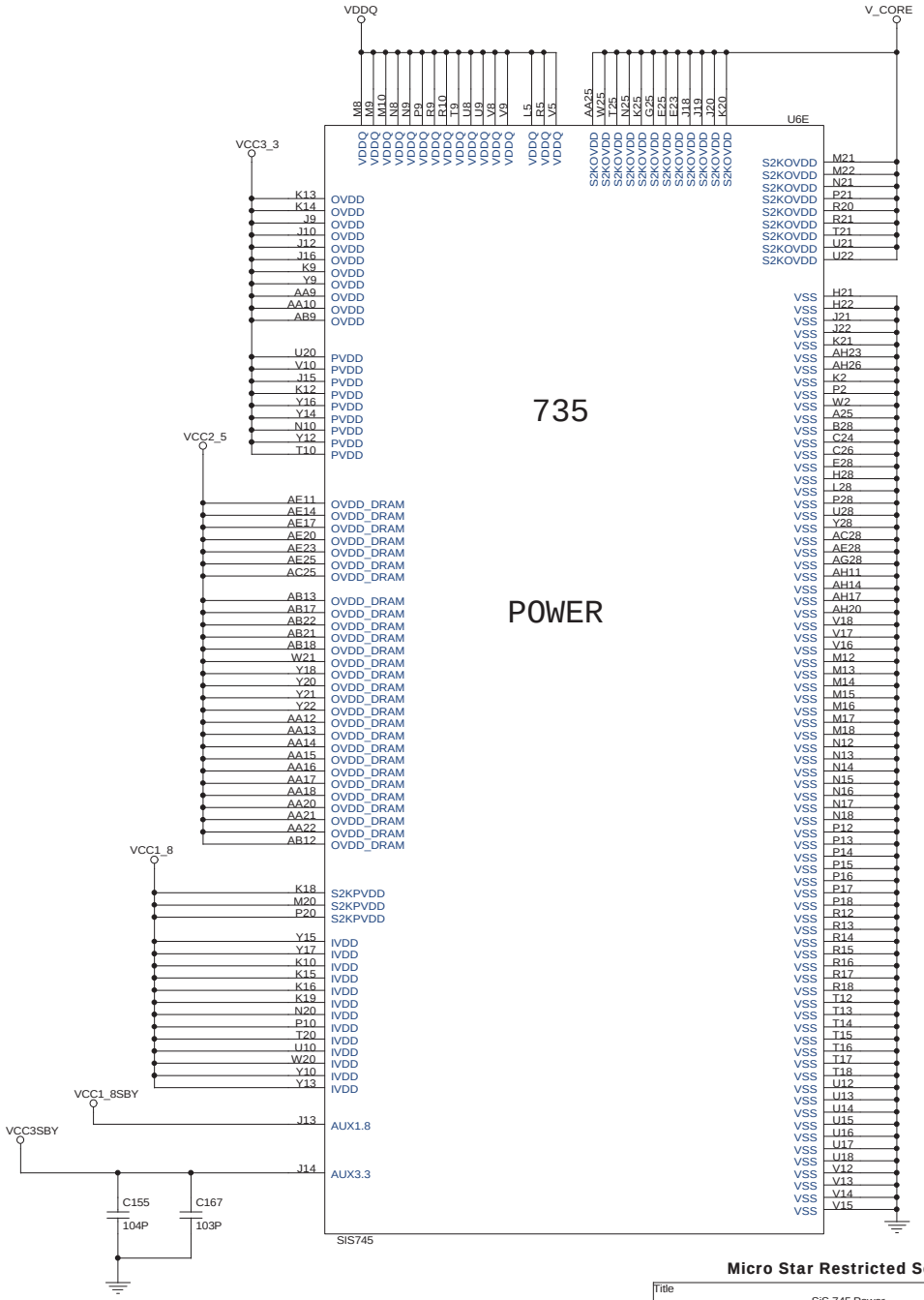
SiS 735 Power

SiS 735 Four Coner Decoupling Capacitor



SiS 735 Power Decoupling Capacitor





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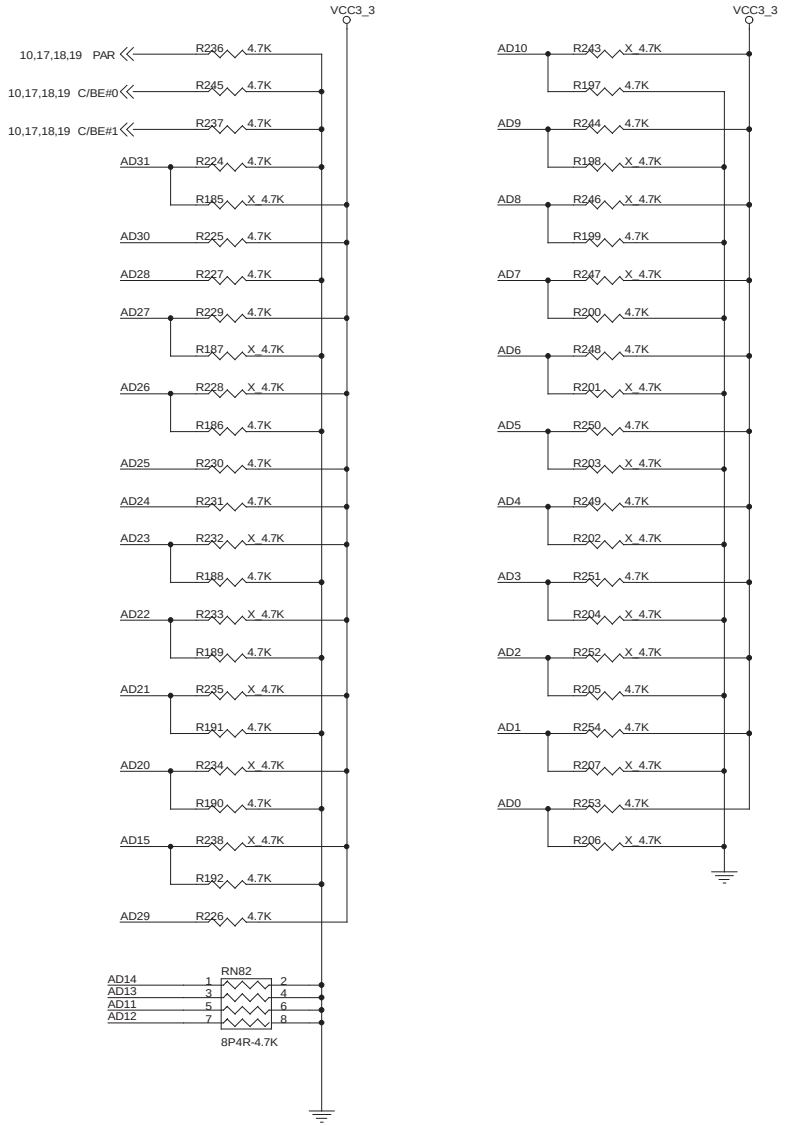
SiS 745 Hardware Trap Define



AD31: Allow the ROM address
from FFF8_XXXX to FFFF_XXXXh
0:Disable (Recommend)
1:Enable

AD30: System Auto-Reset Function Enable
0:Disable
1:Enable (Default)

AD28: Clock Forward Offset
0:Delay 1000ps (Default)
1:No Delay

AD27: Processor Forward Clock Delay Mode
0:Disable
1:Enable (Default)

AD26: Receiver Delay Enable
0: Processor forward clock delay mode
1: NB forward clock delay mode

AD23 AD22: S2K Bus Length

0	0	Short (Default)
0	1	
1	0	
1	1	Long

AD21 AD20: System Clock Speed

0	0	100MHz (Default)
0	1	66MHz
1	0	90MHz
1	1	133MHz

AD15: Receive clock delay control mode
0: Use DLL control value
1: Use hardware trap value
(AD[14..11]) (Default)

AD[14..11]: Receive Forward Clock Delay
0000:minimum delay
1111:maxmum delay

AD[10..9]: Slew (Output Slew Rate)
00:minimum slew rate
11:maximum slew rate

AD8: S2K output Buffer Driving Strength Control Mode
0: Use conpensation logic control value
1: Use hardware trap value (AD[3..0] and AD[7..4])

AD[7..4]: S2K output Buffer NMOS Driving Strength
0000: minimum driving strength
1111: maximum driving strength

AD[3..0]: S2K Output Buffer PMOS Driving Strength
0000: maximum driving strength
1111: minimum driving strength

PAR: CPU, SDRAM, PCI, AGP Clock
PLL/DLL Circuit Enable
0: Enable
1: Disable

C/BE#0: IDE Test Enable
0: Disable
1: Enable

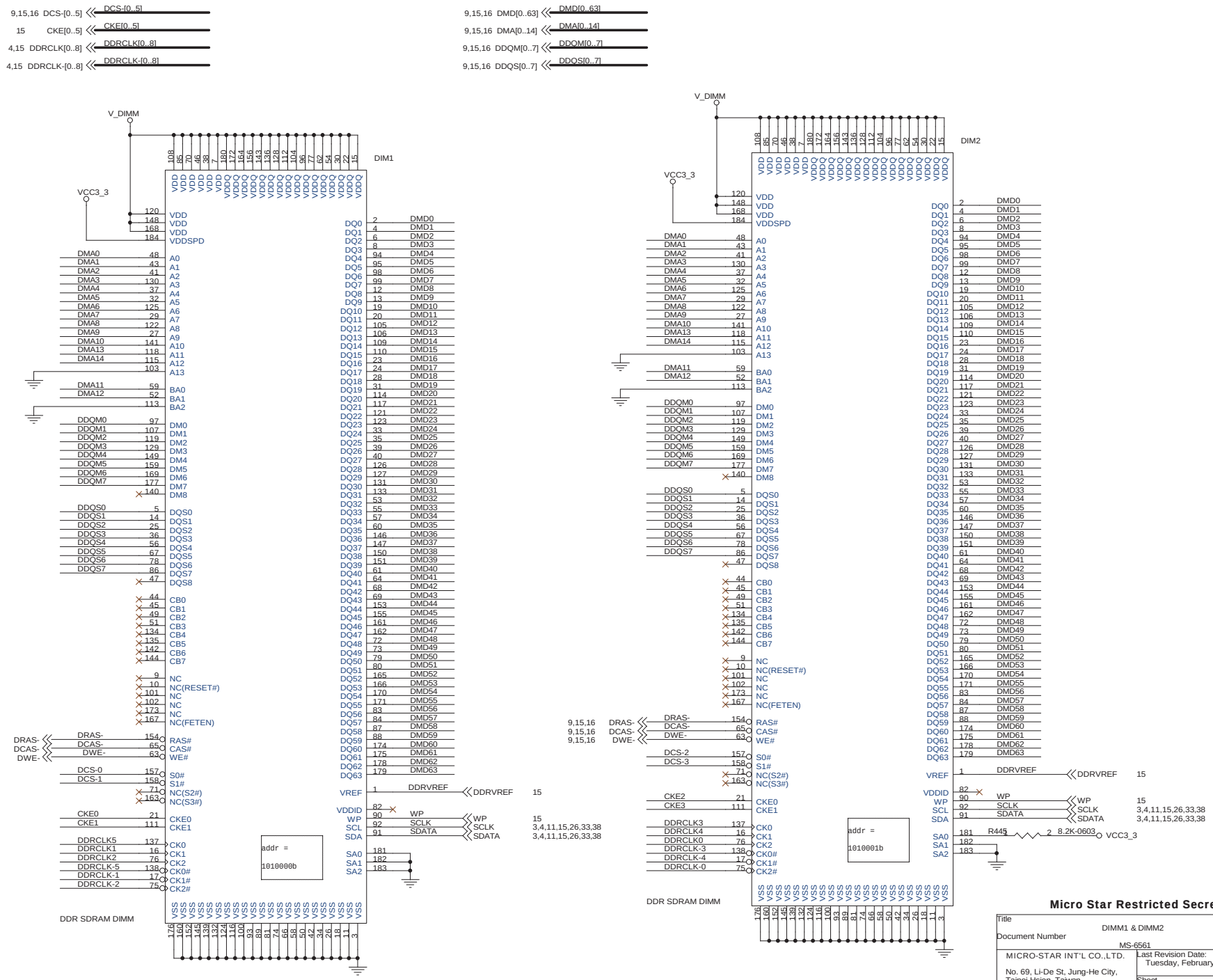
C/BE#1: Debug Test Enable
0: Disable
1: Enable

10,17,18,19,38 AD[0..31] <<< AD[0..31]

10,17,18,19 C/BE#[0..1] <<< C/BE#[0..1]

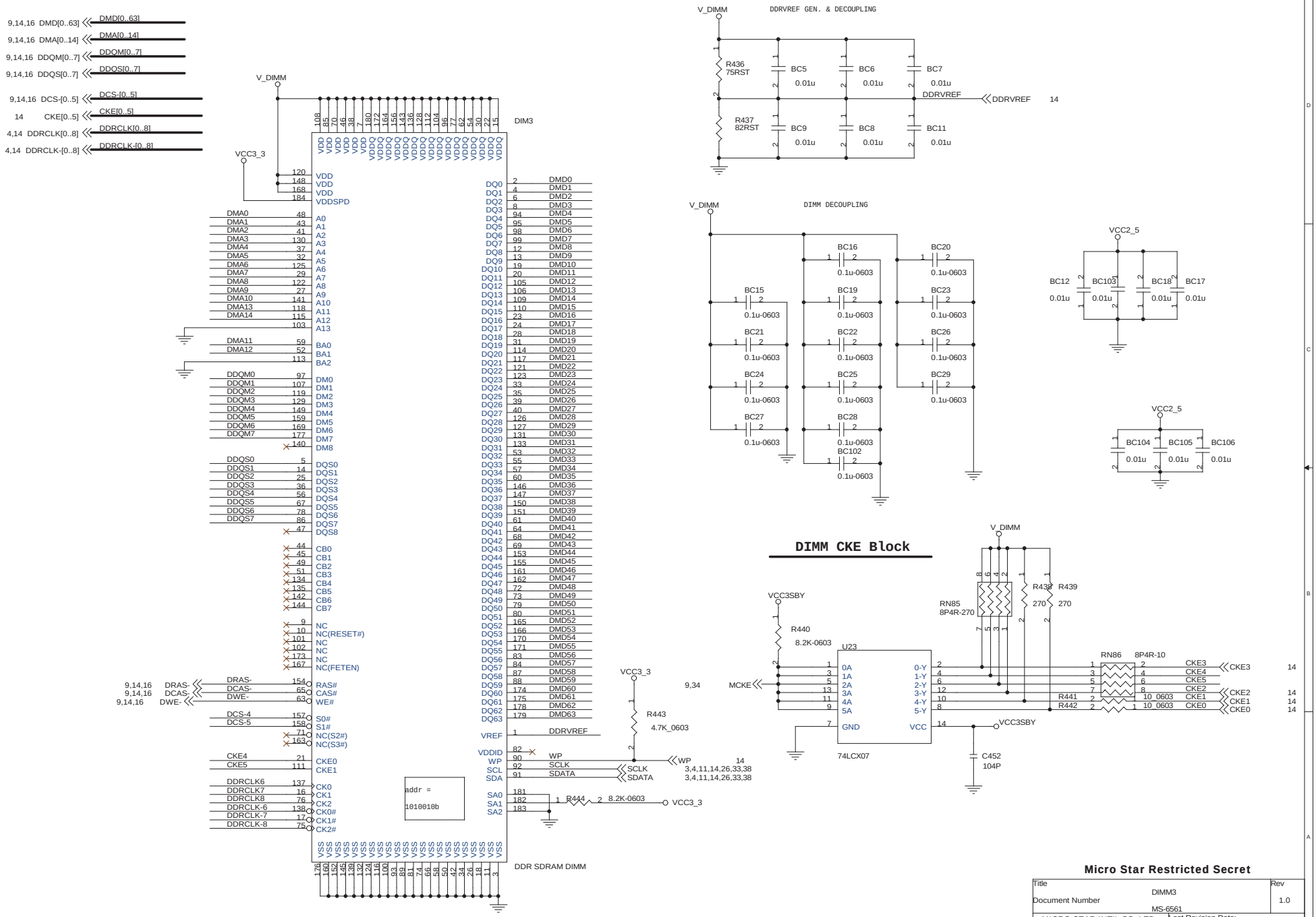
Micro Star Restricted Secret

Title	SiS 745 Hardware Straping	Rev 1.0
Document Number	MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 13 of 42	



Micro Star Restricted Secret

Title: DIMM1 & DIMM2	Rev: 1.0
Document Number: MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002
	Sheet 14 of 42


9,14,16 DMD[0..63]
9,14,16 DMA[0..14]
9,14,16 DDQM[0..7]
9,14,16 DDQS[0..7]
9,14,16 DCS-[0..5]
14 CKE[0..5]
4,14 DDRCLK[0..8]
4,14 DDRCLK-[0..8]
V_DIMM
VCC3_3
DIM3
DDR SDRAM DIMM
DDRVREF GEN. & DECOUPLING
R436 75RST
R437 82RST
BC5 0.01u
BC6 0.01u
BC7 0.01u
BC9 0.01u
BC8 0.01u
BC11 0.01u
DDRVREF
DIMM DECOUPLING
BC15 0.1u-0603
BC16 0.1u-0603
BC19 0.1u-0603
BC20 0.1u-0603
BC21 0.1u-0603
BC22 0.1u-0603
BC23 0.1u-0603
BC24 0.1u-0603
BC25 0.1u-0603
BC26 0.1u-0603
BC27 0.1u-0603
BC28 0.1u-0603
BC29 0.1u-0603
BC102 0.1u-0603
VCC2_5
BC12 0.01u
BC103 0.01u
BC18 0.01u
BC17 0.01u
BC104 0.01u
BC105 0.01u
BC106 0.01u
DIMM CKE Block
R440 8.2K-0603
U23
74LCX07
RN85 8P4R-270
R438 270
R439 270
RN86 8P4R-10
R441 10_0603
R442 10_0603
C452 104P
R443 4.7K_0603
R444 8.2K-0603
MCKE
CKE3
CKE4
CKE5
CKE2
CKE1
CKE0
VCC3SBY
addr = 1010010b
Micro Star Restricted Secret
Title DIMM3
Document Number MS-6561
Rev 1.0
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Tuesday, February 19, 2002
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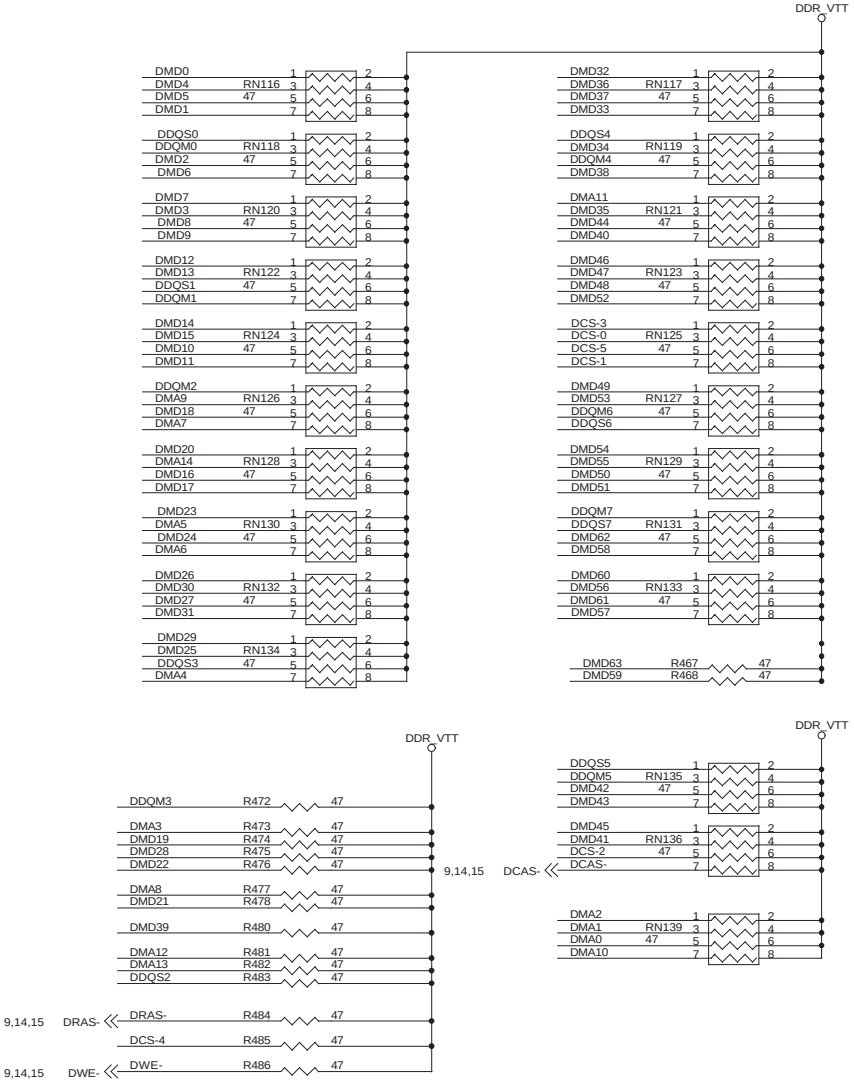
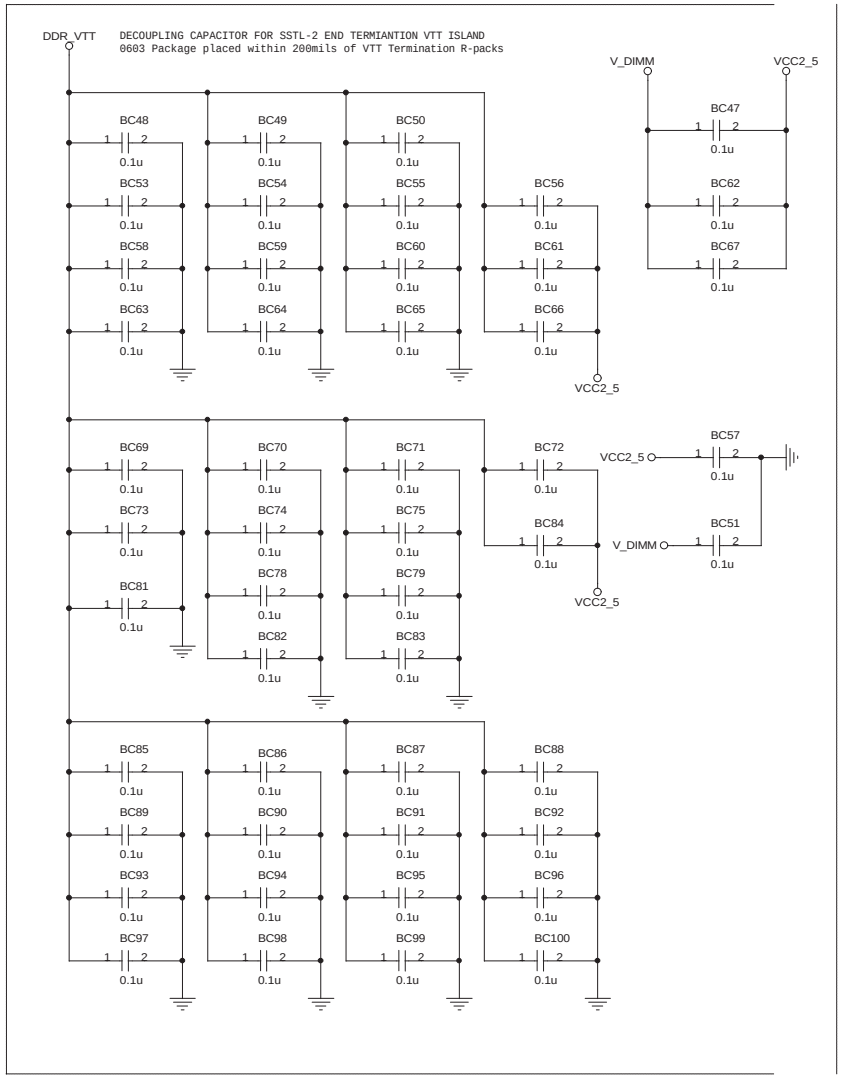
DMD[0..63] DMD[0..63] 9,14,15
DDQM[0..7] DDQM[0..7] 9,14,15
DDQS[0..7] DDQS[0..7] 9,14,15
DMA[0..14] DMA[0..14] 9,14,15
DCS-[0..5] DCS-[0..5] 9,14,15

SSTL-2 Termination Resistors

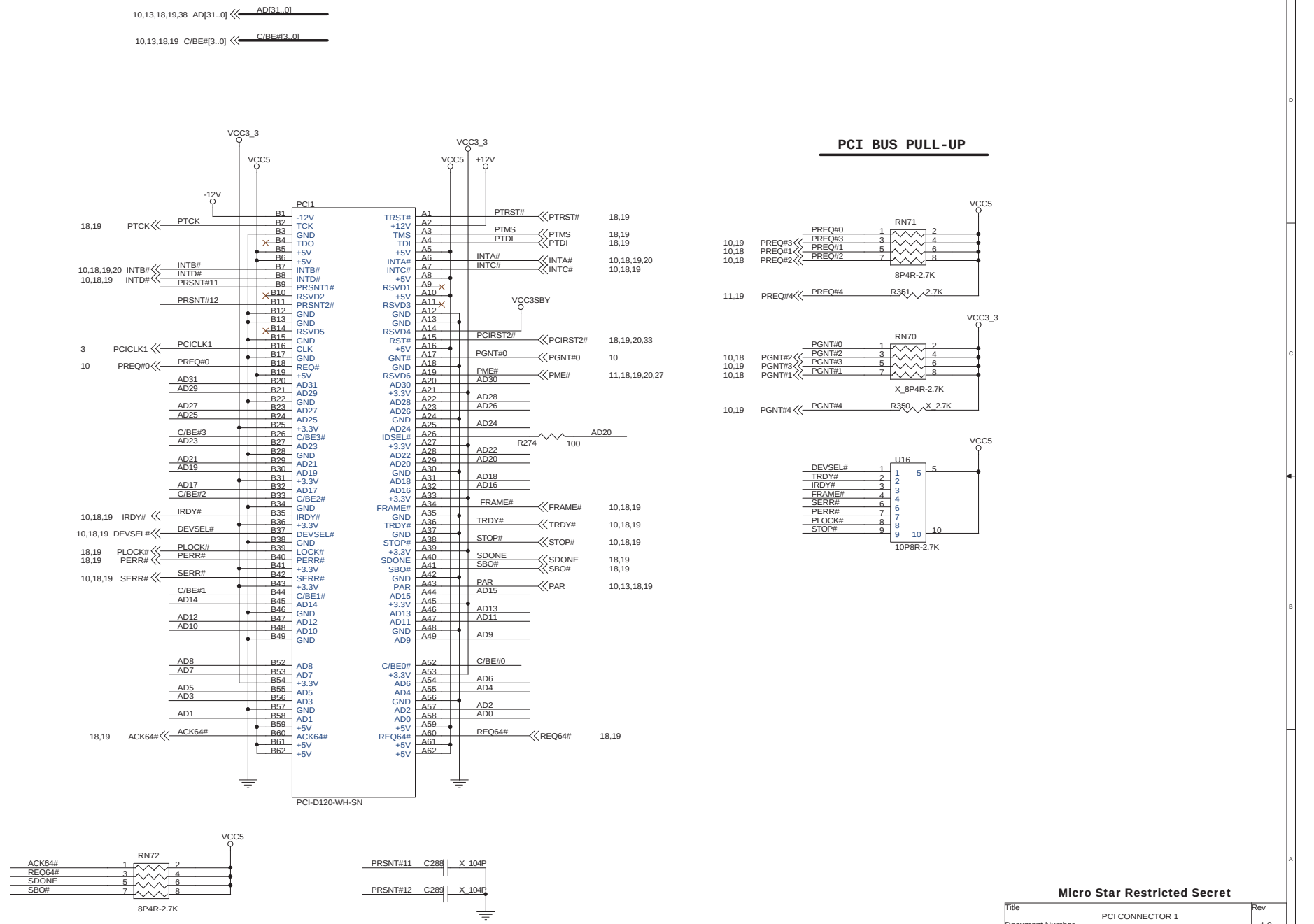
(Note: The termination resistors are only for DDR application)





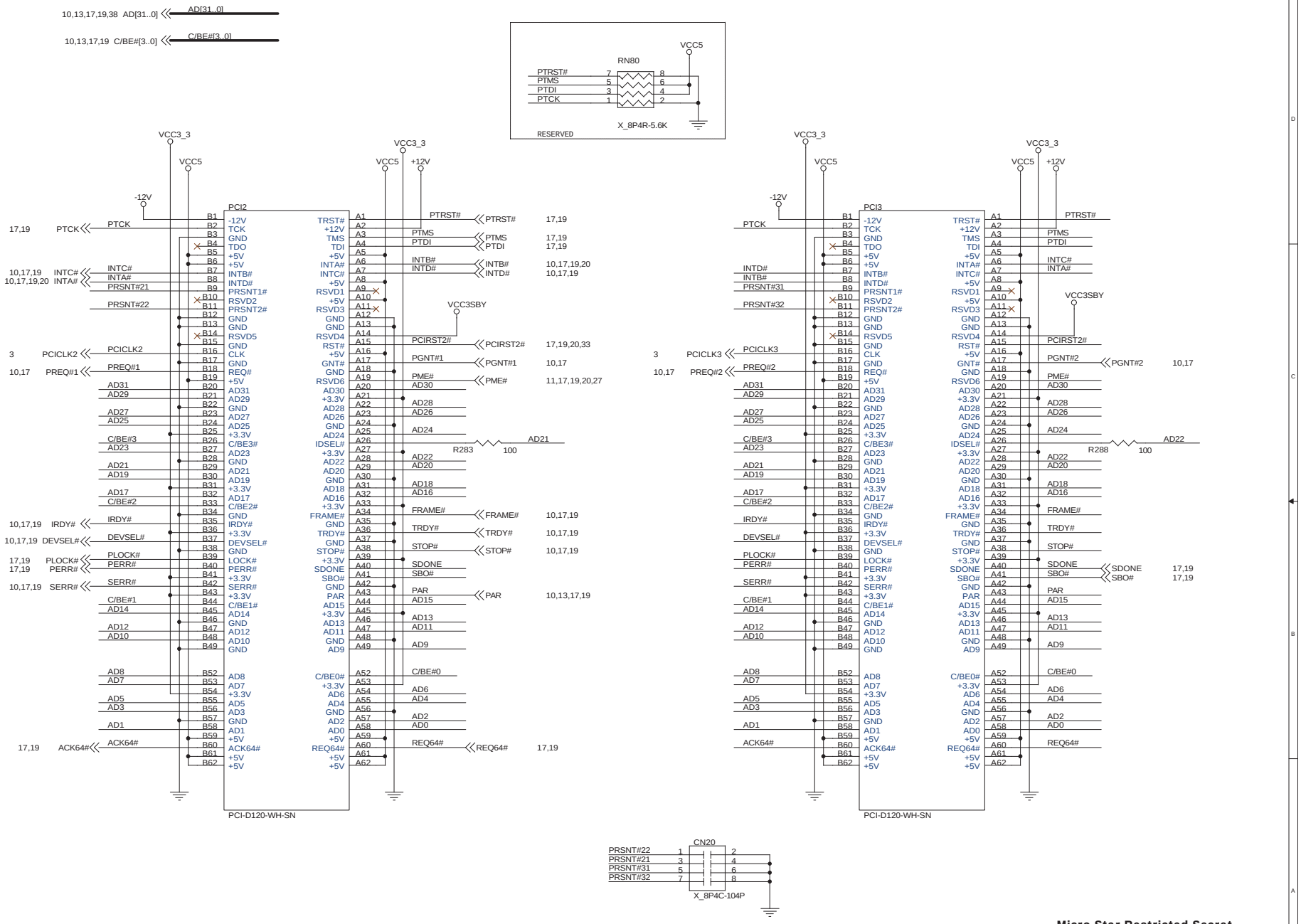
Micro Star Restricted Secret

Title	DDR TERMINATOR	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 16 of 42	



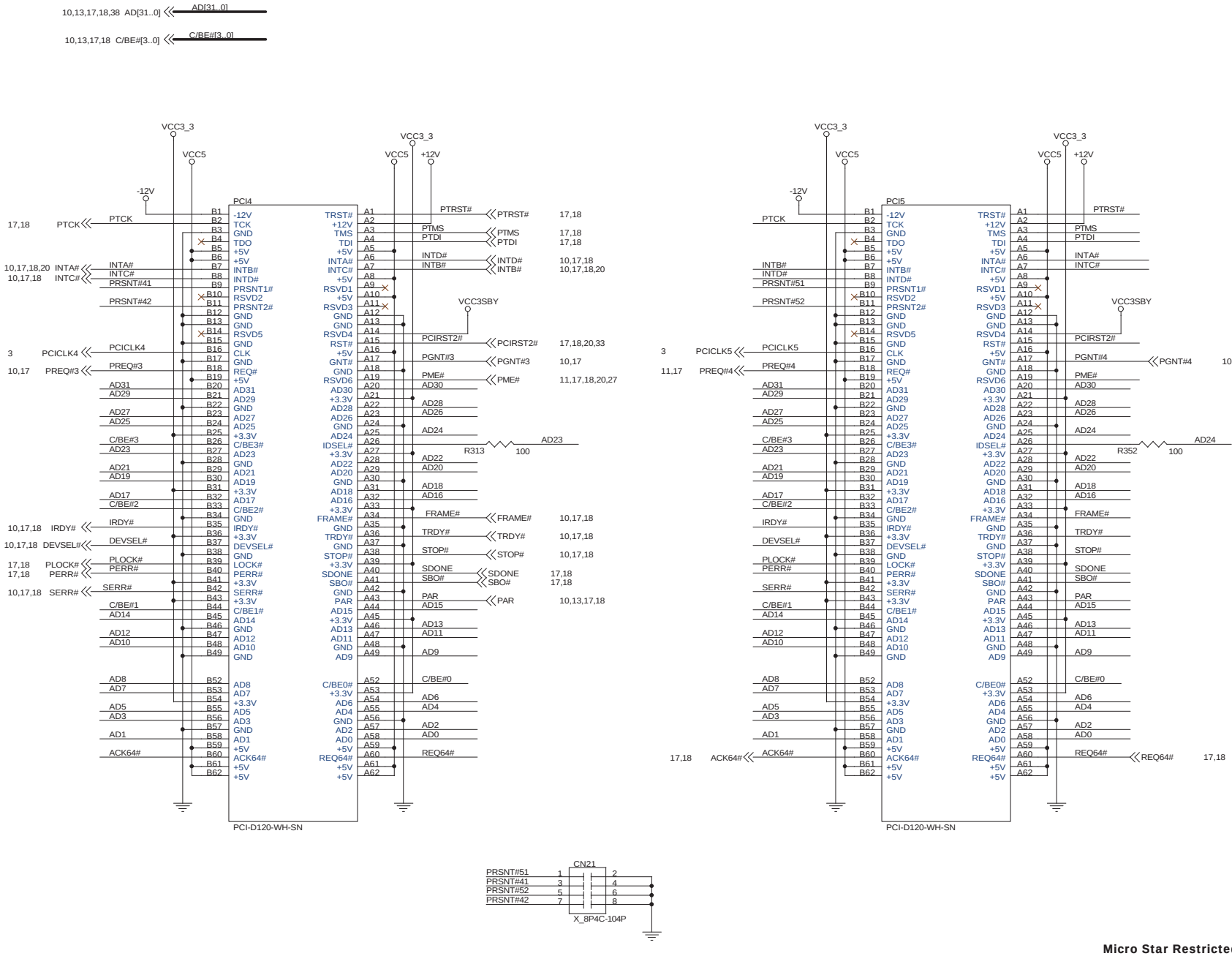
Micro Star Restricted Secret

Title	PCI CONNECTOR 1	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 17 of 42	



Micro Star Restricted Secret

Title	PCI2 & PCI3	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	Sheet 18 of 42


10,13,17,18,38 AD[31..0]
AD[31..0]
10,13,17,18 C/BE#[3..0]
C/BE#[3..0]
PCI4
PCI5
PCI-D120-WH-SN
VCC3_3
VCC5
+12V
-12V
VCC3SBY
PCICLK4
PCICLK5
R313
R352
100
CN21
X_8P4C-104P
Micro Star Restricted Secret
Title
PCI4 & PCI5
Rev
1.0
Document Number
MS-6561
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Tuesday, February 19, 2002
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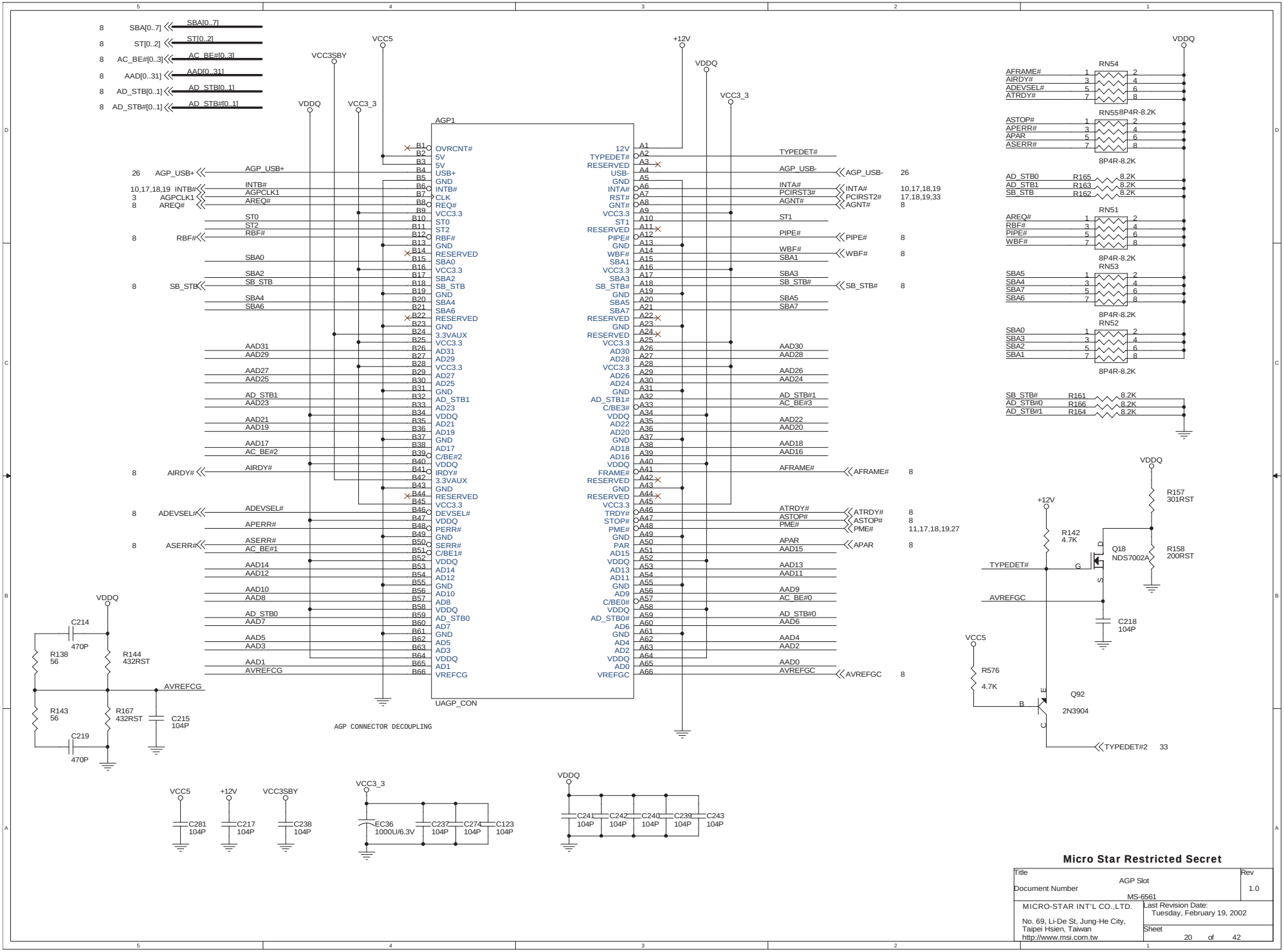
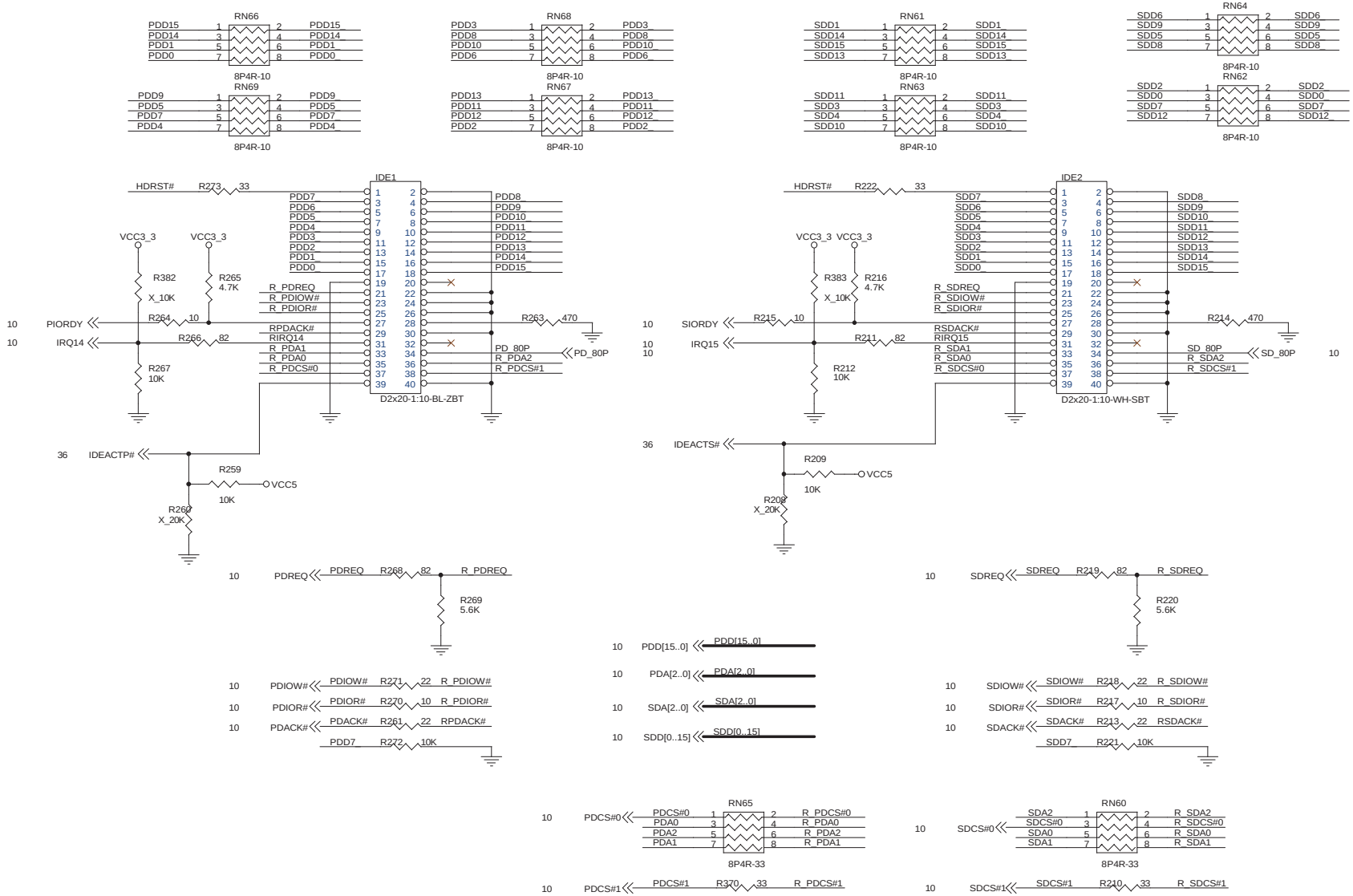


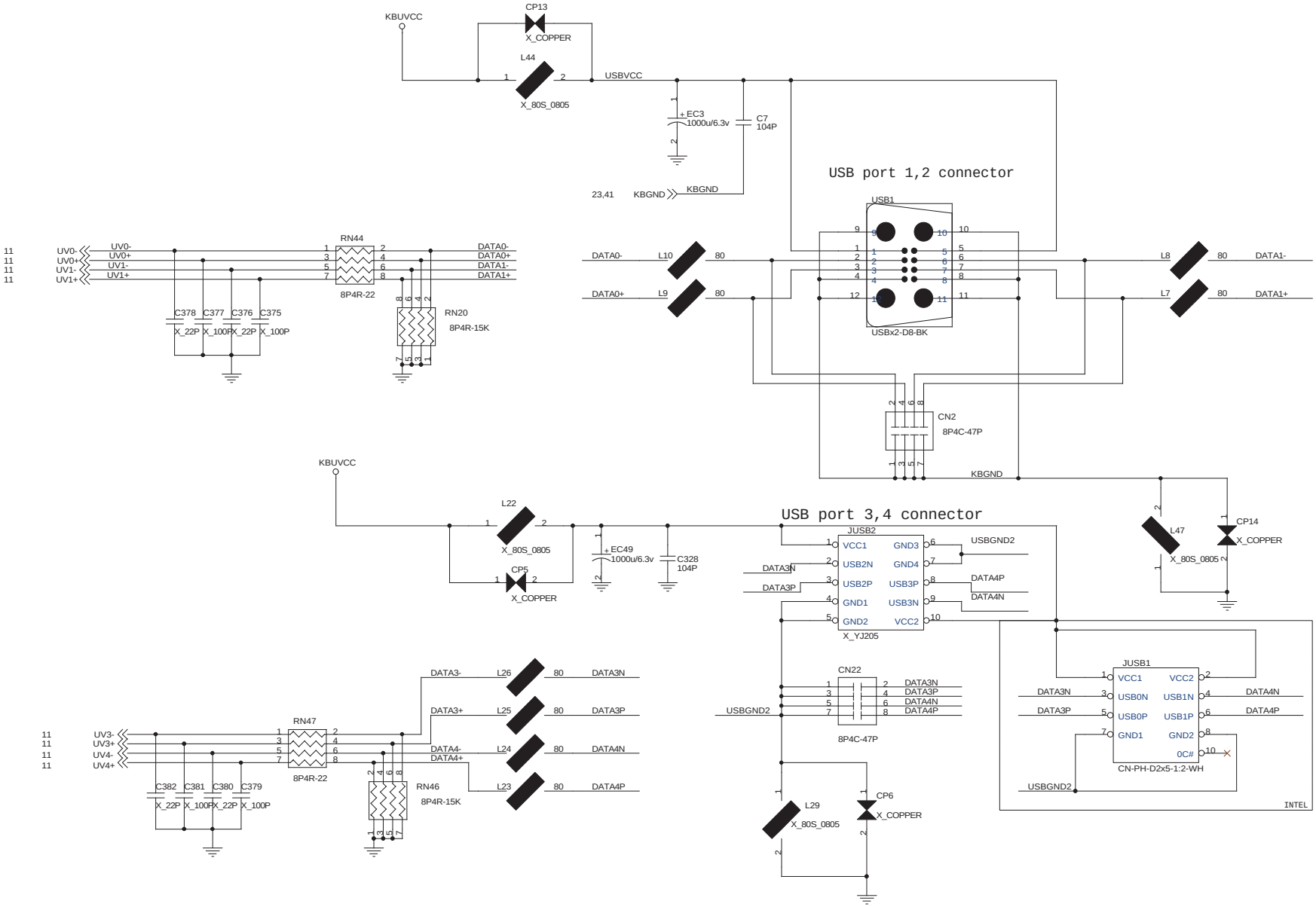
Micro Star Restricted Secret

Title: AGP Slot		Rev: 1.0
Document Number: MS-6561		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	Sheet 20 of 42



Micro Star Restricted Secret

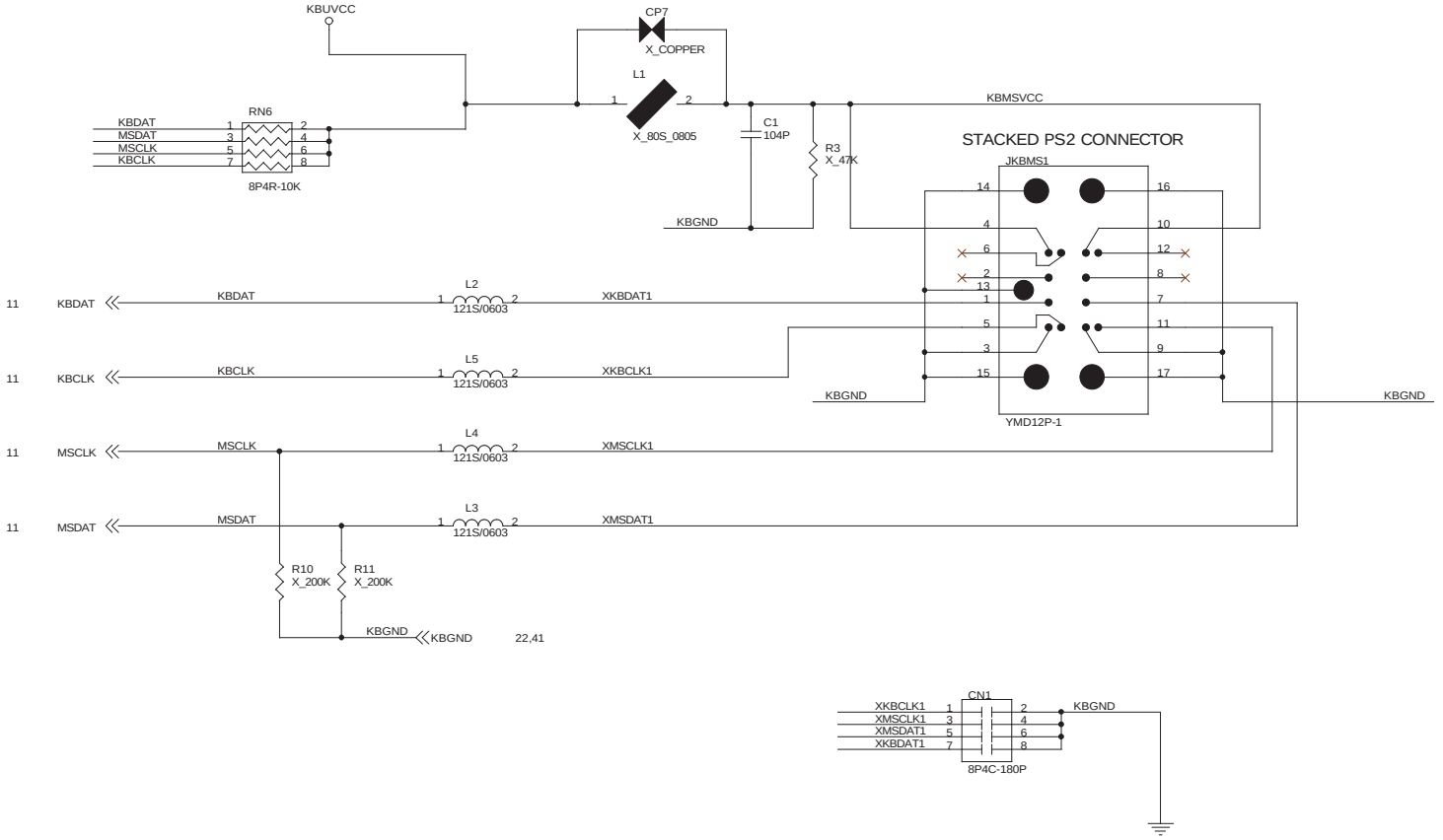
Title	IDE CONNECTOR	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 21 of 42	



Micro Star Restricted Secret

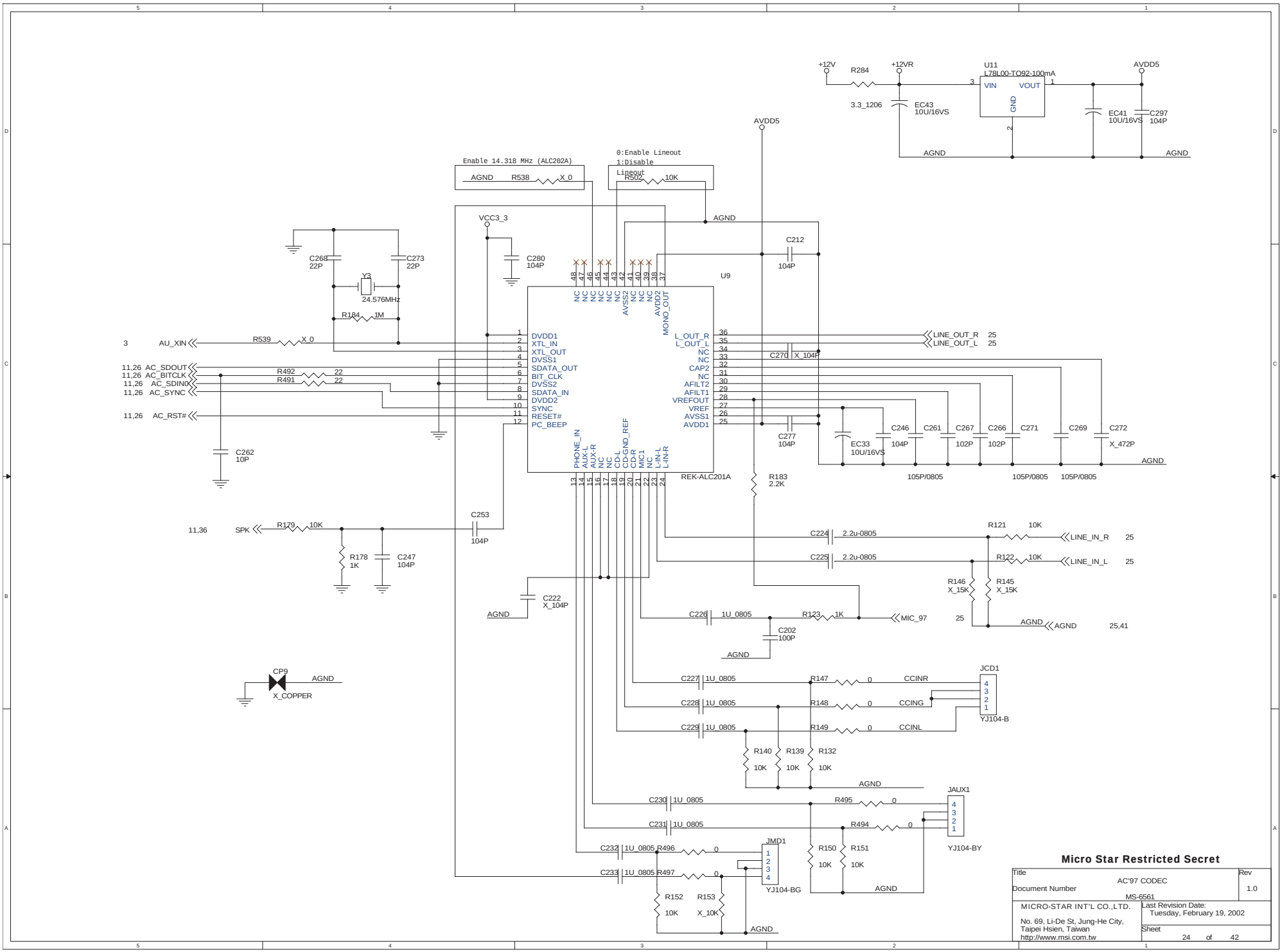
Title	USB Connector	Rev 1.0
Document Number	MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	Sheet 22 of 42

KEYBOARD/MOUSE PORTS



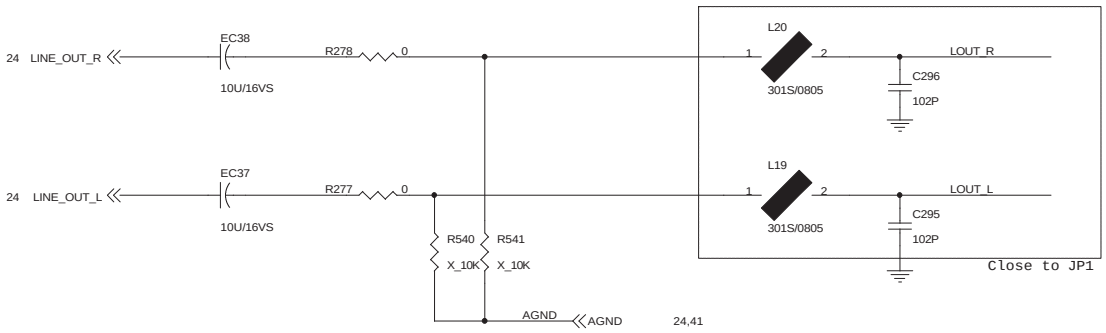
Micro Star Restricted Secret

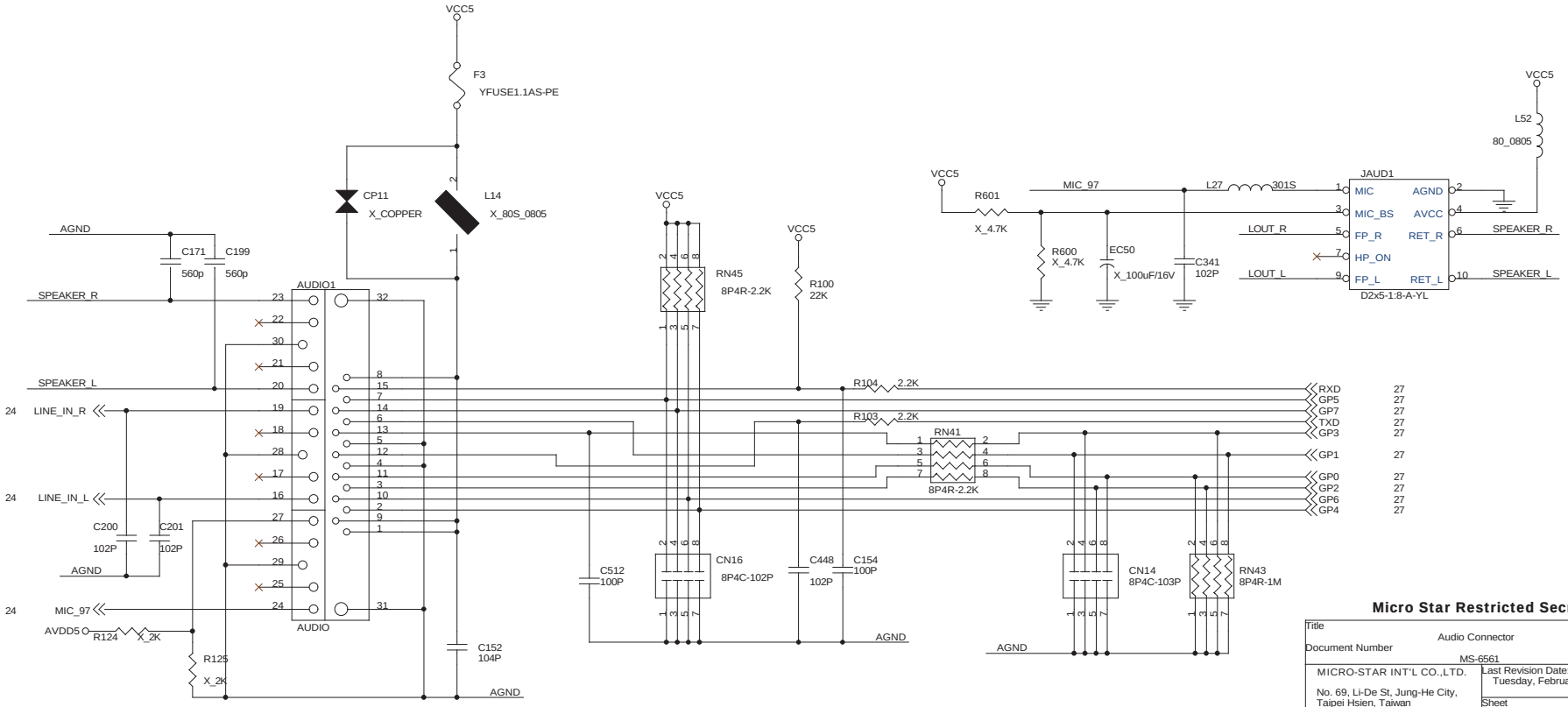
Title	Keyboard/Mouse Connector	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 23 of 42	



Micro Star Restricted Secret

Title	AC'97 CODEC	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 24 of 42	





Micro Star Restricted Secret

Title	Audio Connector	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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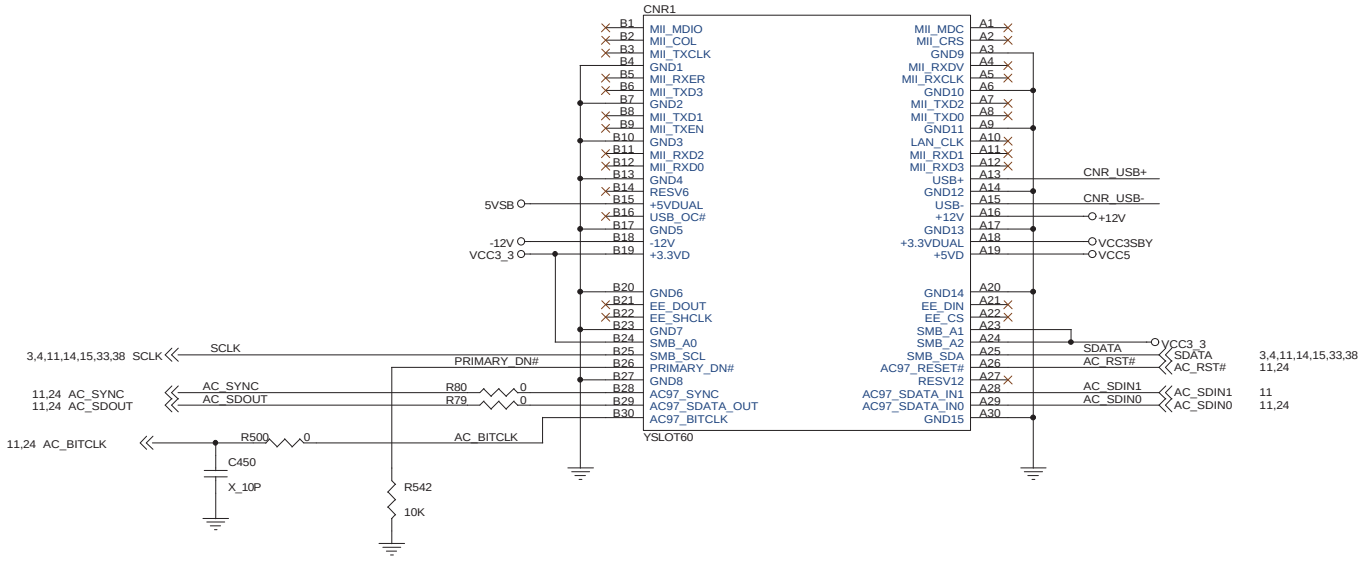
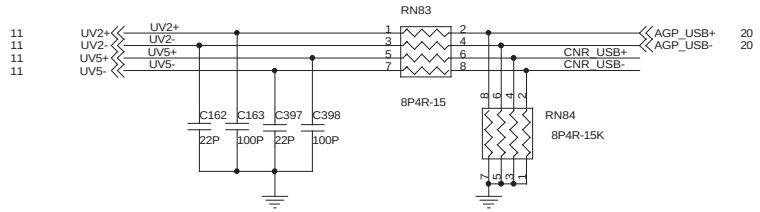
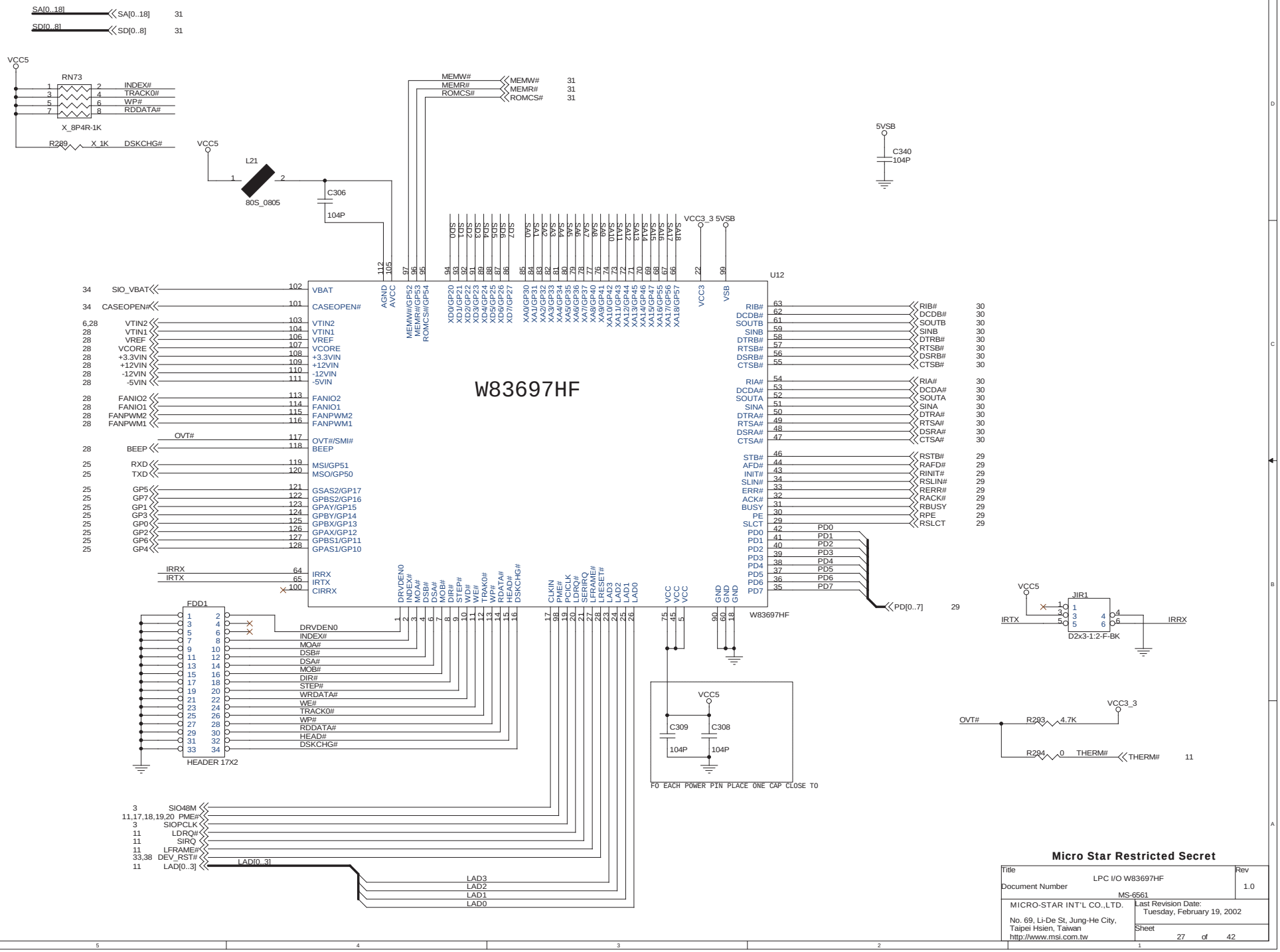




Micro Star Restricted Secret

Title	CNR Slot	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 26 of 42	


W83697HF
U12
SA[0..18]
SD[0..8]
RN73
X_8P4R-1K
R289 X_1K DSKCHG#
L21
80S_0805
C306
104P
C340
104P
C309
C308
104P
104P
FDD1
HEADER 17X2
JIR1
D2x3-1:2-F-BK
R293 4.7K
R294 0 THERM#
FO EACH POWER PIN PLACE ONE CAP CLOSE TO
Micro Star Restricted Secret
LPC I/O W83697HF
MS-6561
1.0
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Tuesday, February 19, 2002
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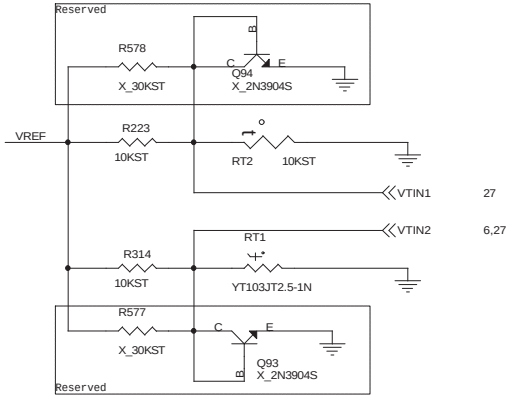
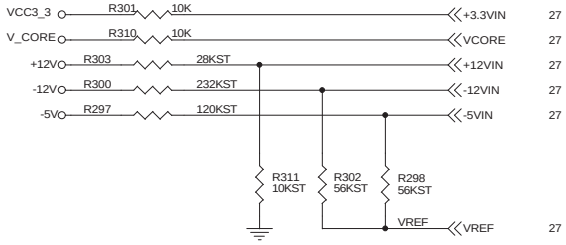
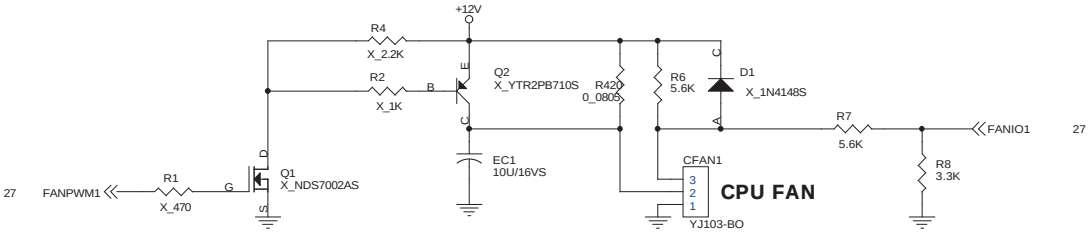
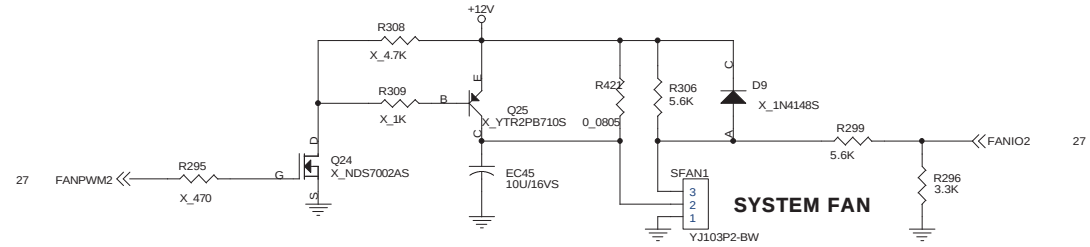
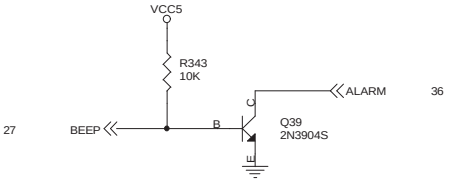
Hardware Monitor





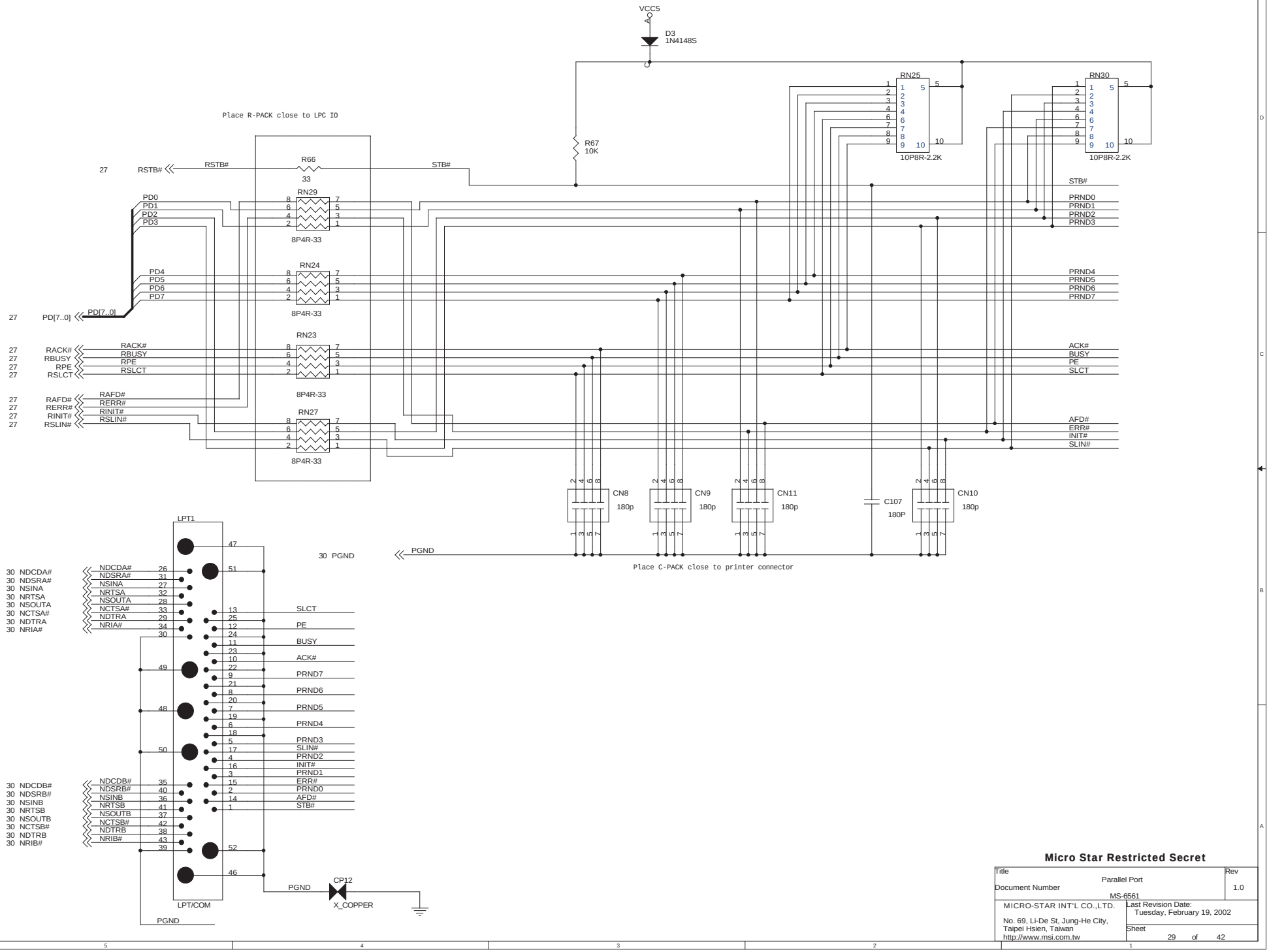






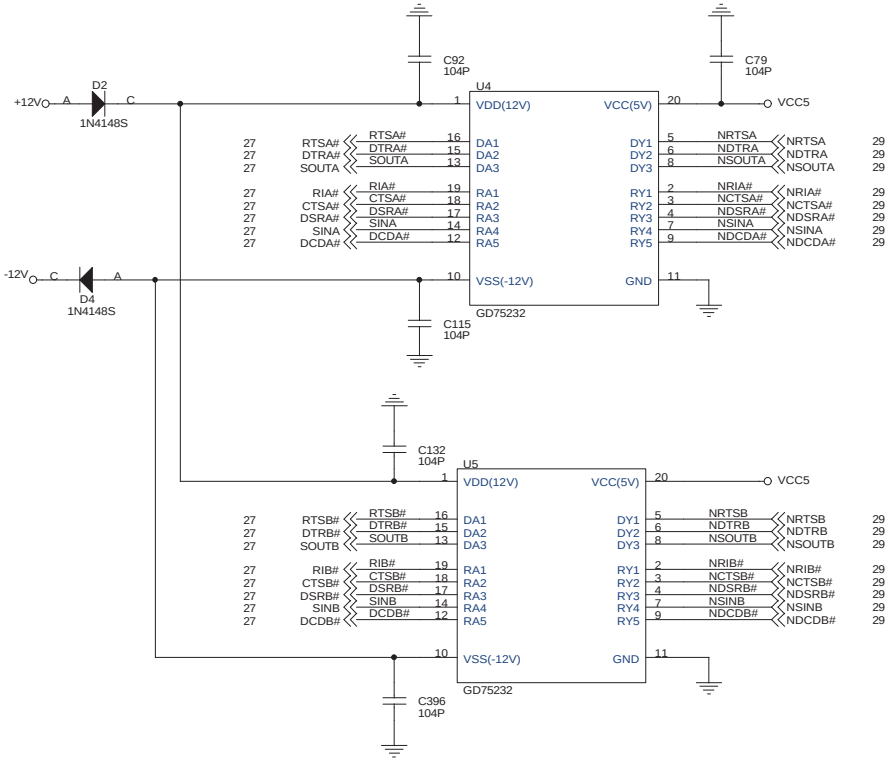
Micro Star Restricted Secret

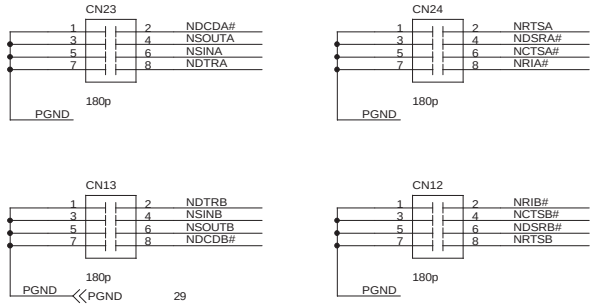
Title	Hardware Monitor	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 28 of 42	

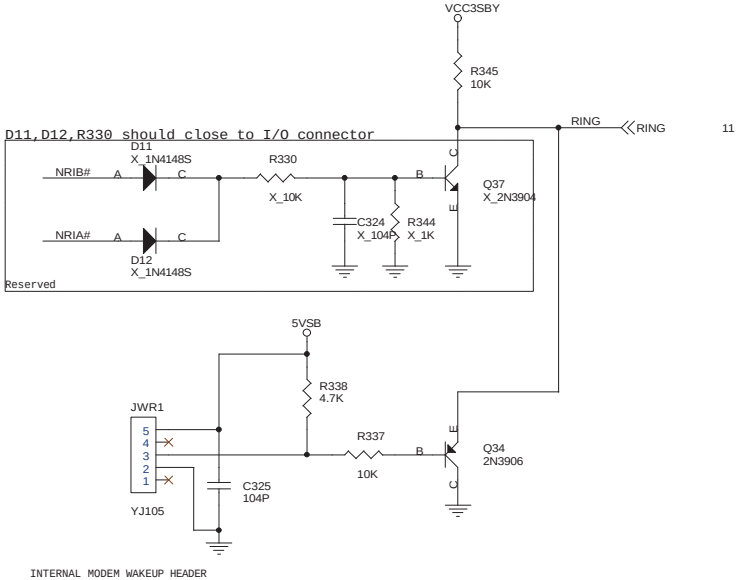


Micro Star Restricted Secret

Title: Parallel Port		Rev: 1.0
Document Number: MS-6561		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	Sheet 29 of 42

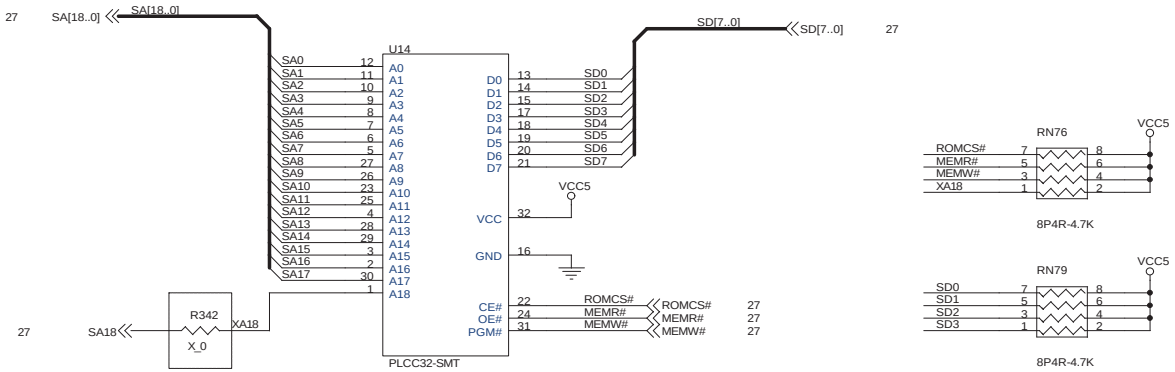






Micro Star Restricted Secret

Title	Serial Port	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 30 of 42	

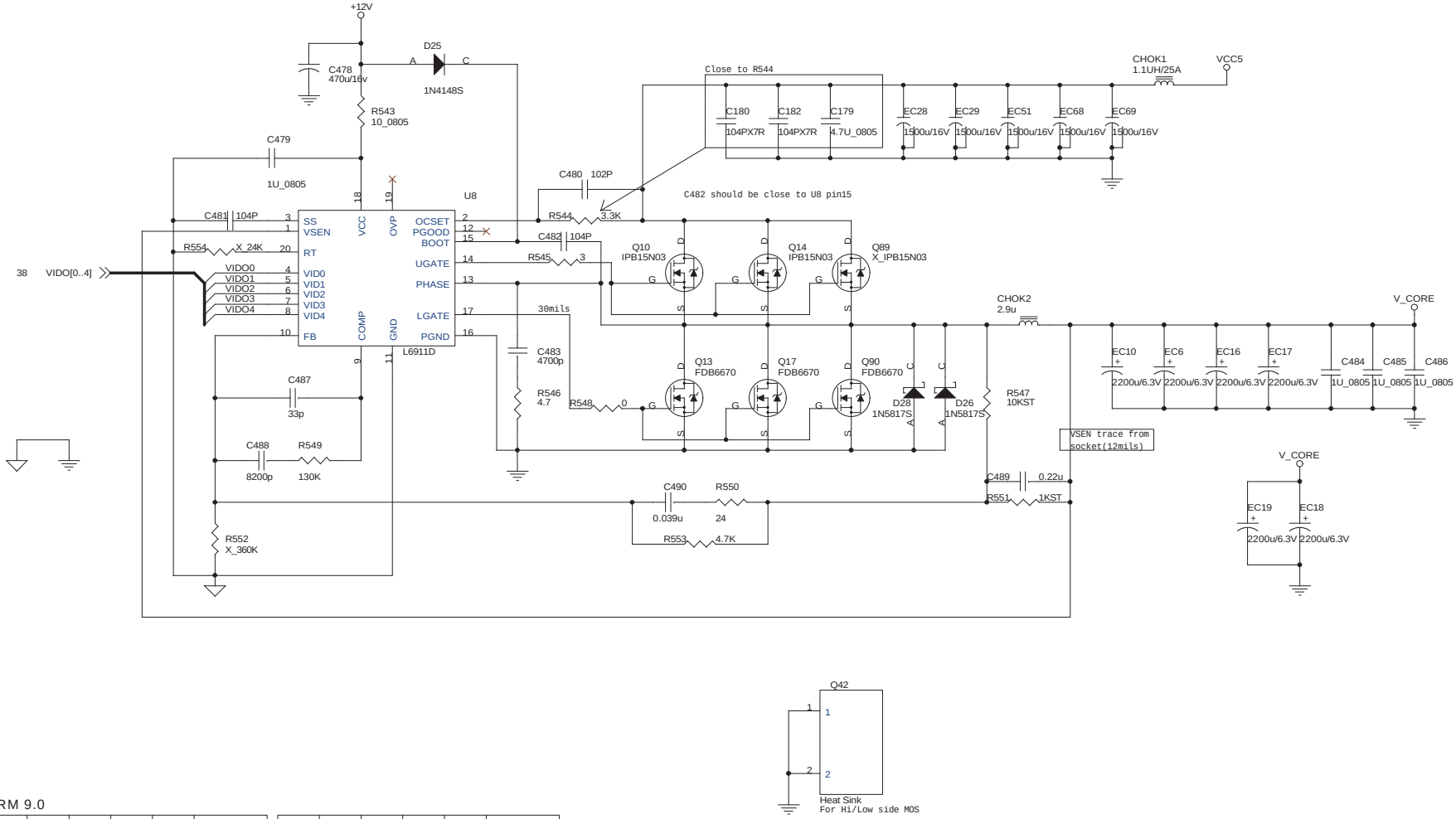


SELECT 2MB OR 4MB

2M UNSTALL
4M INSTALL

Micro Star Restricted Secret

Title	Flash Memory	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
	Sheet 31 of 42	



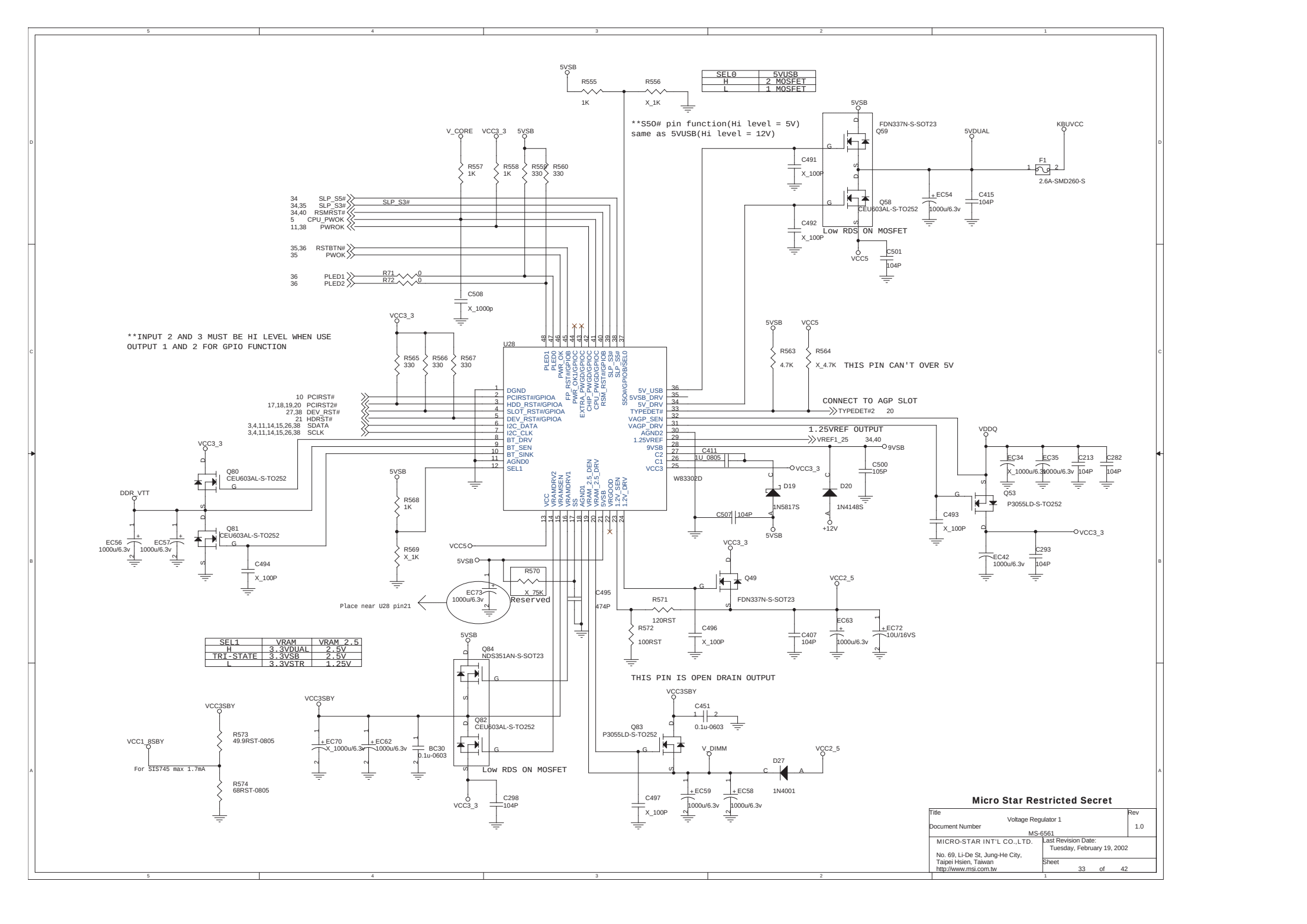
VRM 9.0

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

Micro Star Restricted Secret

Title: PWM_CS5322	Rev: 1.0
Document Number: MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002 Sheet 32 of 42


5VSB
R555
1K
R556
X_1K
SEL0 | 5VUSB
H | 2 MOSFET
L | 1 MOSFET
**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
FDN337N-S-SOT23
Q59
5VDUAL
KBUVCC
F1
2.6A-SMD260-S
C491
X_100P
Q58
CEU603AL-S-TO252
EC54
1000u/6.3v
C415
104P
C492
X_100P
Low RDS ON MOSFET
VCC5
C501
104P
V_CORE
VCC3_3
5VSB
R557
1K
R558
1K
R559
330
R560
330
34 SLP_S5#
34,35 SLP_S3#
34,40 RSMRST#
5 CPU_PWOK
11,38 PWROK
35,36 RSTBTN#
35 PWOK
36 PLED1
36 PLED2
R71
R72
0
0
C508
X_1000p
**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION
R565
330
R566
330
R567
330
U28
PLED1
PLED2
PWR_OK
FP_RST#/GPIOB
PWR_OK1/GPIOC
EXTRA_PWGD/GPIOC
CHIP_PWGD/GPIOC
CPU_PWGD/GPIOC
RSM_RST#/GPIOB
SLP_S3#
SLP_S5#
S5O#/GPIOB/SEL0
10 PCIRST#
17,18,19,20 PCIRST2#
27,38 DEV_RST#
21 HDRST#
3,4,11,14,15,26,38 SDATA
3,4,11,14,15,26,38 SCLK
DGND
PCIRST#/GPIOA
HDD_RST#/GPIOA
SLOT_RST#/GPIOA
DEV_RST#/GPIOA
I2C_DATA
I2C_CLK
BT_DRV
BT_SEN
BT_SINK
AGND0
SEL1
5V_USB
5VSB_DRV
5V_DRV
TYPEDET#
VAGP_SEN
VAGP_DRV
AGND2
1.25VREF
9VSB
C2
C1
VCC3
VCC
VRAMDRV2
VRAMSEN
VRAMDRV1
SS
AGND1
VRAM_2.5_DEN
VRAM_2.5_DRV
5VSB
SYSGOOD
1.2V_SEN
1.2V_DRV
R563
4.7K
R564
X_4.7K
THIS PIN CAN'T OVER 5V
CONNECT TO AGP SLOT
TYPEDET#2 20
1.25VREF OUTPUT
VREF1_25
34,40 9VSB
C411
1U_0805
W83302D
VCC3_3
C500
105P
D19
1N5817S
D20
1N4148S
C507
104P
5VSB
+12V
VDDQ
EC34
X_1000u/6.3v
EC35
1000u/6.3v
C213
104P
C282
104P
Q53
P3055LD-S-TO252
C493
X_100P
EC42
1000u/6.3v
C293
104P
VCC3_3
Q80
CEU603AL-S-TO252
DDR_VTT
Q81
CEU603AL-S-TO252
EC56
1000u/6.3v
EC57
1000u/6.3v
C494
X_100P
R568
1K
R569
X_1K
VCC5
5VSB
R570
X_75K
Reserved
EC73
1000u/6.3v
Place near U28 pin21
Q49
C495
474P
R571
120RST
FDN337N-S-SOT23
VCC2_5
R572
100RST
C496
X_100P
C407
104P
EC63
1000u/6.3v
EC72
10U/16VS
SEL1 | VRAM | VRAM_2.5
H | 3.3VDUAL | 2.5V
TRI-STATE | 3.3VSB | 2.5V
L | 3.3VSTR | 1.25V
Q84
NDS351AN-S-SOT23
THIS PIN IS OPEN DRAIN OUTPUT
VCC3SBY
C451
0.1u-0603
Q83
P3055LD-S-TO252
V_DIMM
VCC2_5
D27
1N4001
EC59
1000u/6.3v
EC58
1000u/6.3v
C497
X_100P
VCC1_8SBY
R573
49.9RST-0805
For SIS745 max 1.7mA
R574
68RST-0805
EC70
X_1000u/6.3v
EC62
1000u/6.3v
BC30
0.1u-0603
Q82
CEU603AL-S-TO252
Low RDS ON MOSFET
C298
104P
Micro Star Restricted Secret
Title
Voltage Regulator 1
Rev
1.0
Document Number
MS-6561
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Tuesday, February 19, 2002
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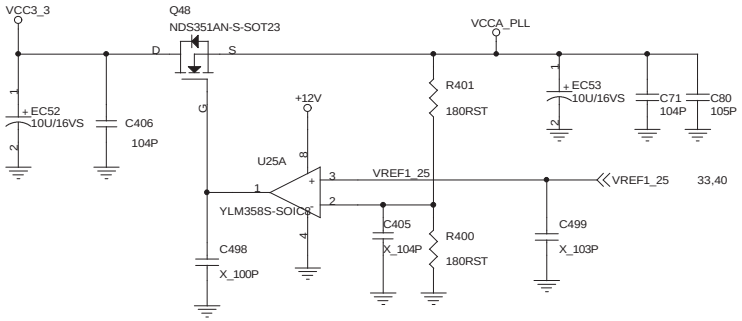
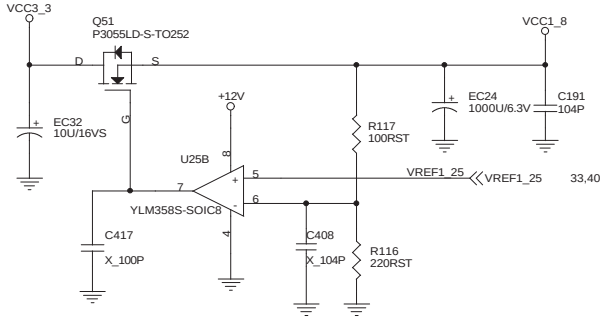
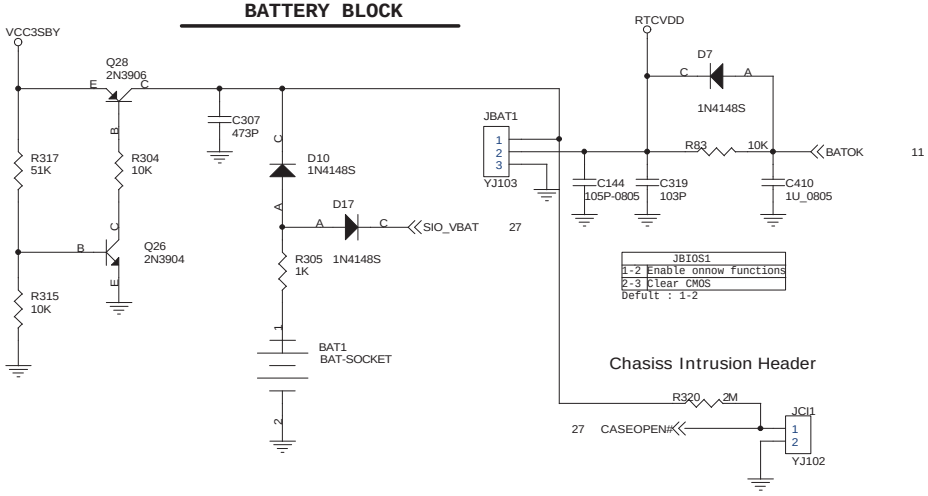
2.5V POWER TRANSLATOR
(30mils trace / 15 mils space)

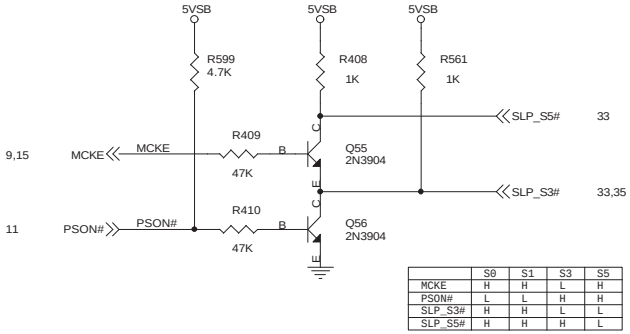


1.8V POWER TRANSLATOR
(50mils trace / 15 mils space)



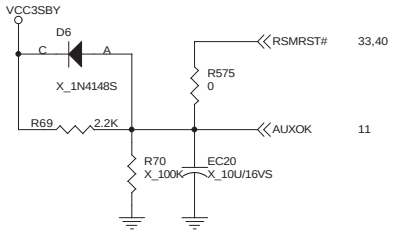
BATTERY BLOCK





	S0	S1	S3	S5
MCKE	H	H	L	H
PSON#	L	L	H	H
SLP_S3#	H	H	L	L
SLP_S5#	H	H	H	L

AUX_OK BLOCK



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Title	Voltage Regulator 2	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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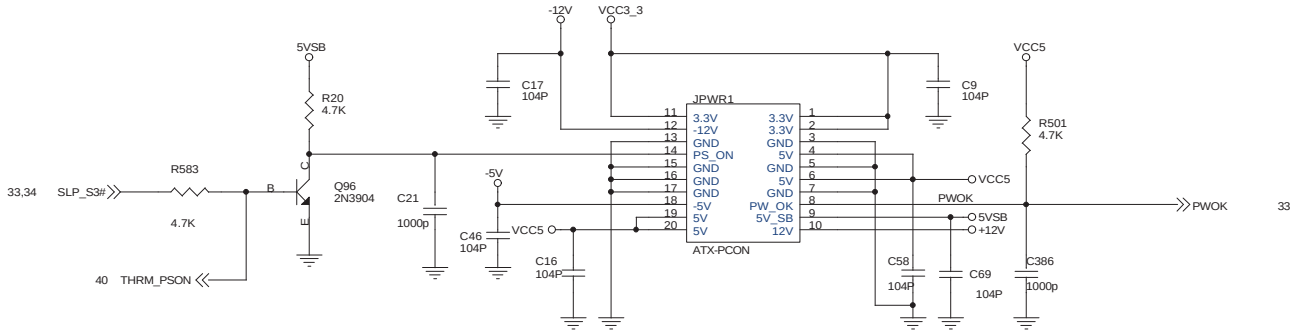

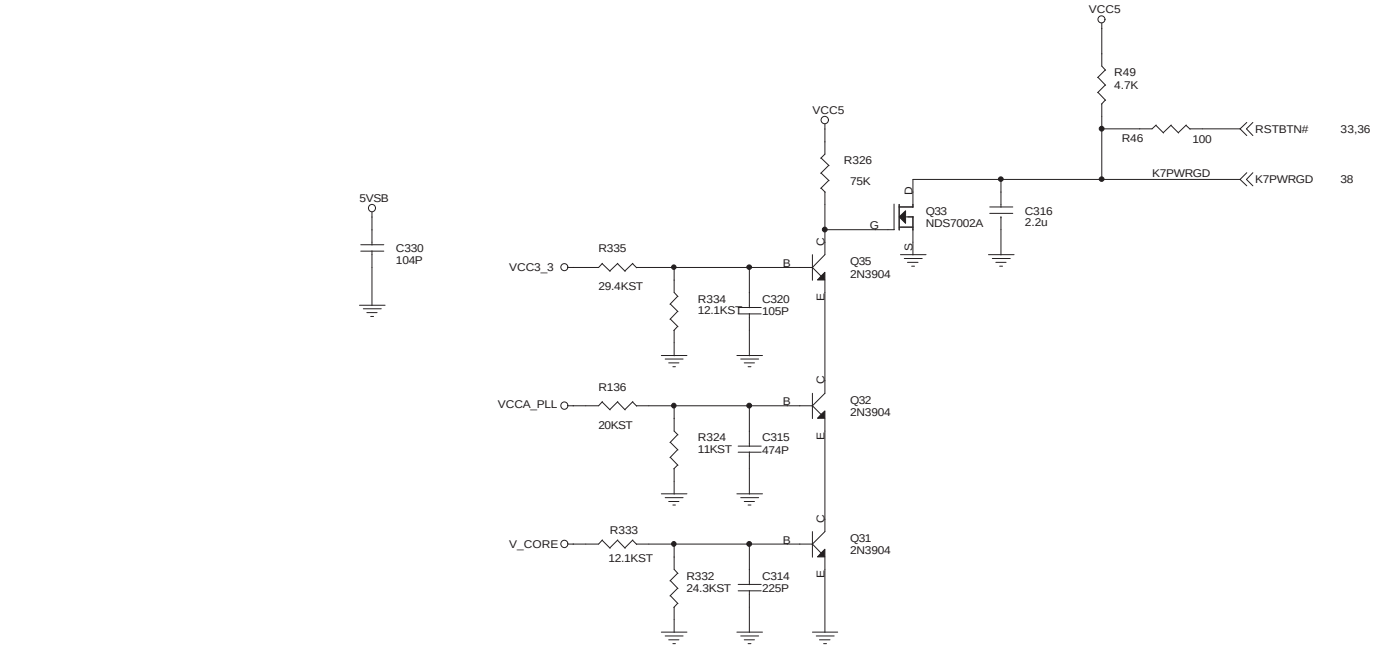

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Title	ATX Connector	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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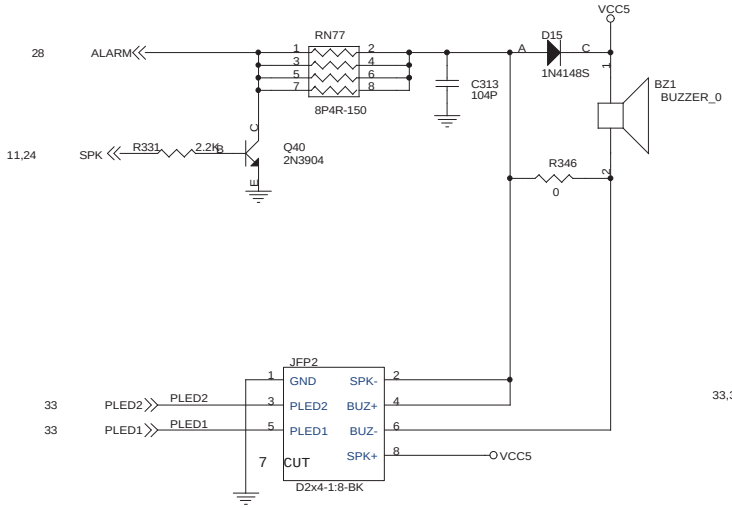

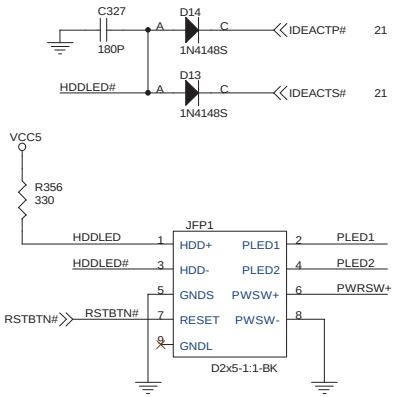

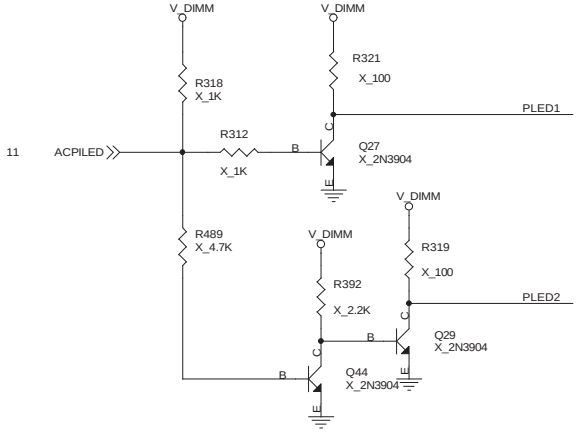

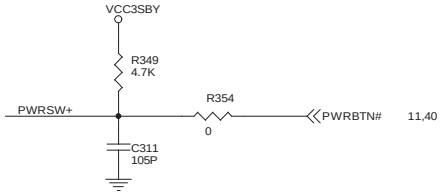

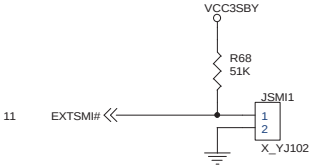

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Title: Front Pannel		Rev: 1.0
Document Number: MS-6561		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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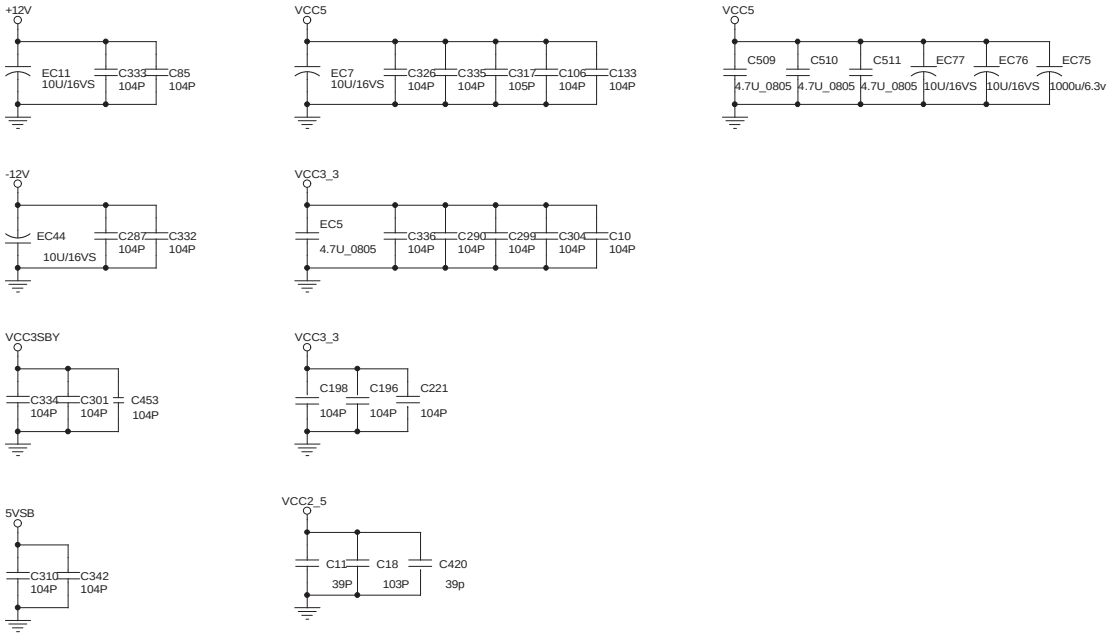
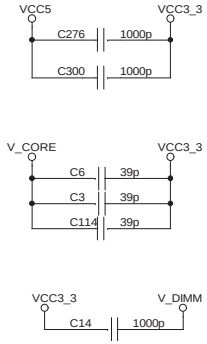
System Decoupling Capacitors



High Freq. return current decoupling



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Title: System Decoupling		Rev: 1.0
Document Number: MS-6561		
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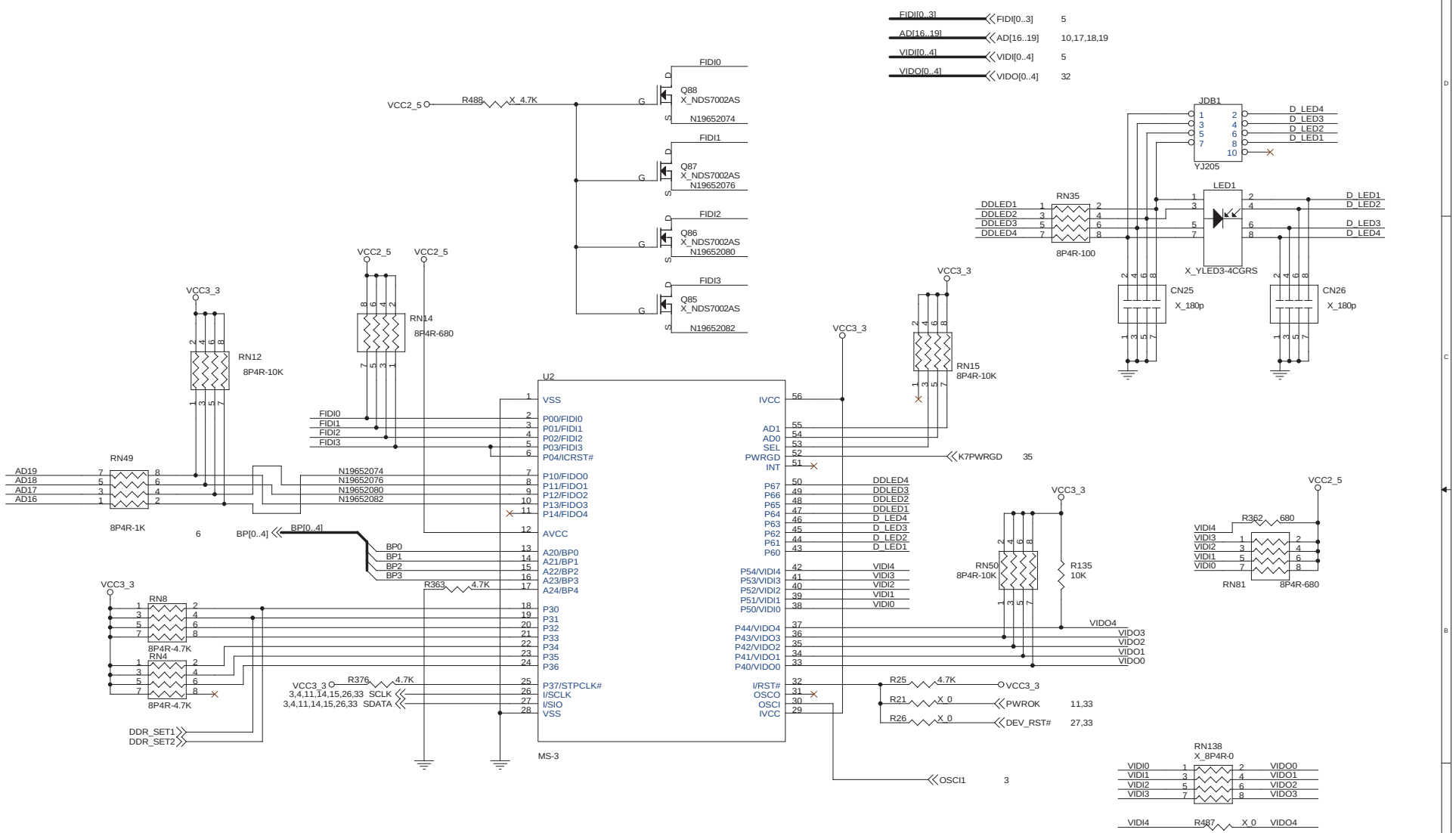

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Title	MS3 and D-LED	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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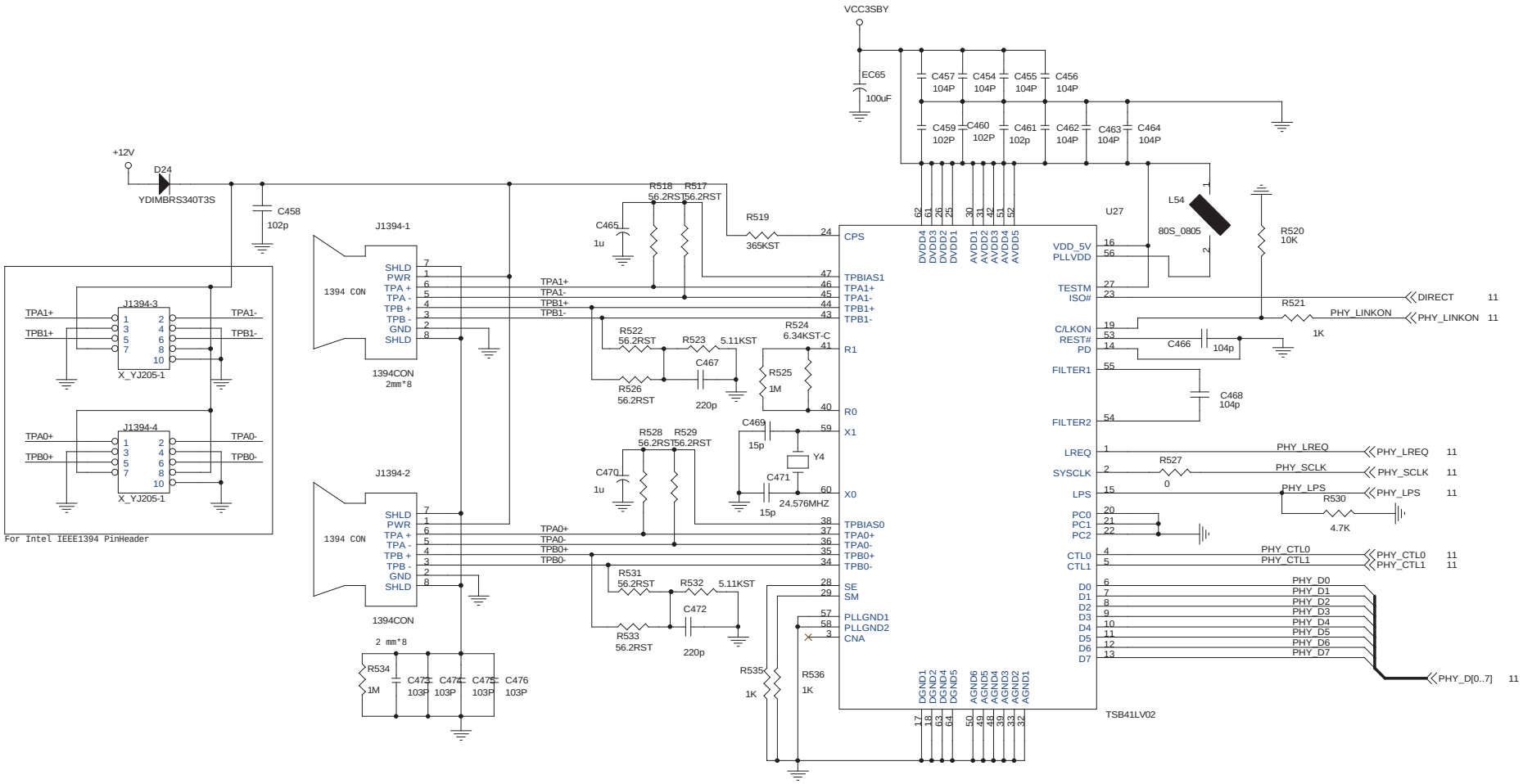

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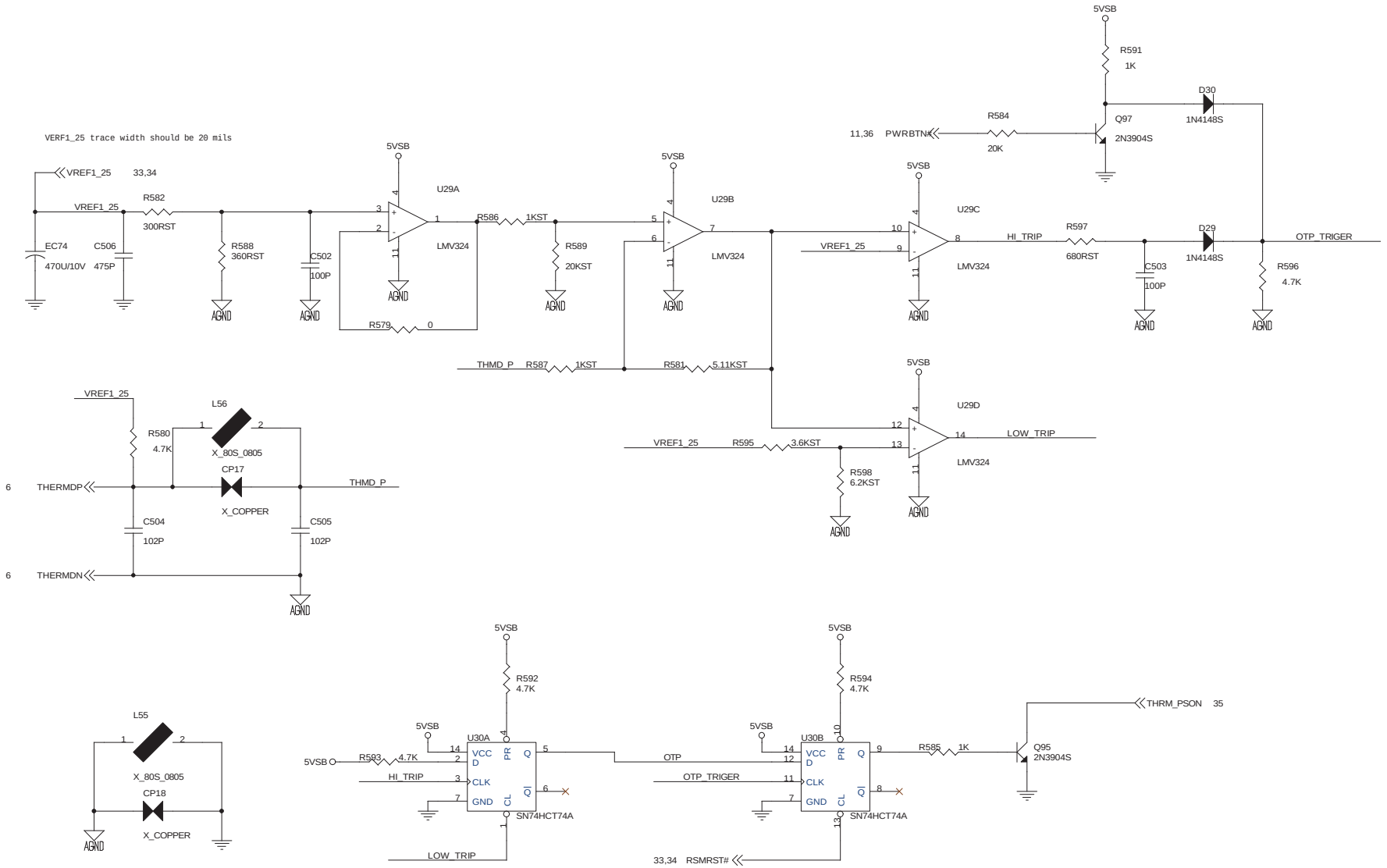
Title	IEEE1394 PHY	Rev 1.0
Document Number	MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	Sheet 39 of 42



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Title	AMD Thermal Protection	Rev
Document Number	MS-6561	1.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002	
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MANUAL PART

U14_X
Flash-ROM

PCB
M/B

BAT1_X
BATTERY

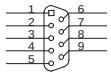
U6_X
Heat Sink

FOR SIS745

JBAT1(1-2)

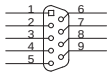
JC-D2-RD

LPT1_X



COM1

LPT1_Y

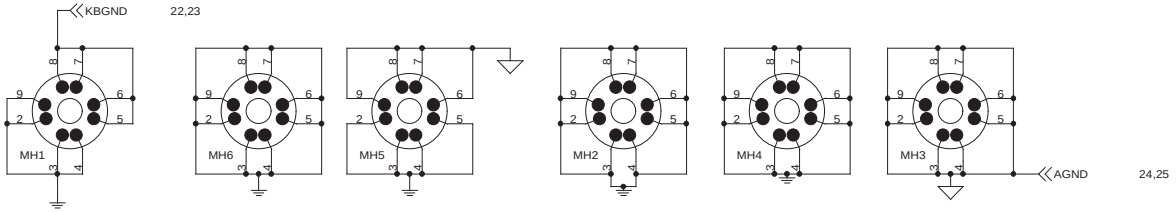


COM2

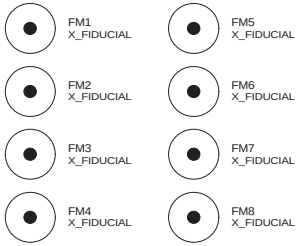
JAUD1(5-6) JAUD1(9-10)

JC-D2-RD JC-D2-RD

PCB OTHER COMPONENT



FIDUCIALS



FOR TEST

JIP1
X_PIN1*2
CPU

JIP2
VCC5
X_PIN1*2
AGP

BS1_X1 BS2_X1 BS3_X1 BS4_X1 BS5_X1

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Title: Manul Part		Rev: 1.0
Document Number: MS-6561		
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PCI Config.

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD20
PCI Slot 2	INTB# INTC# INTD# INTA#	AD21
PCI Slot 3	INTC# INTD# INTA# INTB#	AD22
PCI Slot 4	INTD# INTA# INTB# INTC#	AD23
PCI Slot 5	INTA# INTB# INTC# INTD#	AD24

Chipset General Purpose I/O (SIS745)

GPIO	PIN	TYPE	Function Description	Normal	Active
GPIO1	A15	I	RING(for modem & lan wake up)	H	L
GPIO2	B15	I	PREQ#4		
GPIO3	F16	I	EXTSMI#		
GPIO4	C16	I	IEEE1394 Link on		
GPIO5	D19	I	THERM#(Thermal Detect)		
GPIO6	AH3	I	Primary Ultra-66 Cable ID		
GPIO7	AD9	I	Secondary Ultra-66 Cable ID		
GPIO12	E15	O	IEEE1394 Link Request		
GPIO18	C14	I	IEEE1394 DIRECT		
GPIO19	D14	I/O	IEEE1394 DATA 0		
GPIO20	F14	I/O	IEEE1394 DATA 4		
GPIO21	E14	I/O	IEEE1394 Control 0		
GPIO22	A13	I/O	IEEE1394 Control 1		
GPIO24	D13	I	KBDATA(Keyboard data)		
GPIO25	E13	I	KBCLK(Keyboard clock)		
GPIO26	A12	I	MSDAT(Mouse data)		
GPIO27	F13	I	MSCLK(Mouse clock)		
GPIO28	C13	O	SDATA		
GPIO29	B13	O	SCLK		

MS-3 GPIO SPEC.

Name	Pin	Function
P0[0:4]	2,3,4,5,6	FIDI[0:3]
P1[0:3]	7,8,9,10	FIDO[0:3]
SCLK	26	SCLK
SIO	27	SDATA
P6[0:3]	43,44,45,46	D_LED[1:4]
P6[4:7]	47,48,49,50	DDLED[1:4]
P5[0:4]	38,39,40,41,42	VIDI[0:4]
P4[0:4]	33,34,35,36,37	VIDO[0:4]

W83302D GPIO SPEC.

Name	Pin	Function
GP10	2	PCIRST# INPUT
GP11	3	PCIRST# OUTPUT for SLOT
GP12	4	PCIRST# OUTPUT for Device
GP13	5	PCIRST# OUTPUT for HDD
GP20	41	PWOK for CPU
GP21	42	PWOK for CHIP
GP31	43	RSMRST# connect to AUXOK(sis745)
GP32	44	FP_RST#(reset button) INPUT

Title: GPIO SPEC.	Rev: 1.0
Document Number: MS-6561	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 19, 2002
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