THE RED PAGES ARE MSI BOM NOT FOR IBM SPEC

Last Schematic Update Date:

11/06/2002

MS-6557 *VERSION:2.1A*

STD:
INTEL 845G (B01-0845G15-I06)+ ICH4 + Kinnereth-R(B06-562EZ05-I06)
OPTION A:
INTEL 845G (B01-0845G15-I06)+ ICH4 + KENAI32(B06-8254005-I06)
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Chipset:

INTEL 845G (North Bridge) + ICH4 (South Bridge)

On Board Chip:

LPC Super I/O -- SMsC LPC47M133
BIOS -- FWH
AC' 97 CODEC -- ADI1981A / 1981B / ALC650
CLOCK GENERATION -- ICS 950201AF
LAN -- INTEL Kenai 1000 / Kinnereth-R
DVO -- CH7009 DV+ TV-OUT
1394 -- NEC uPD72874(Optional)

Expansion Slots:

PCI2.2 SLOT* 1 (RISER CARD PCI*2)

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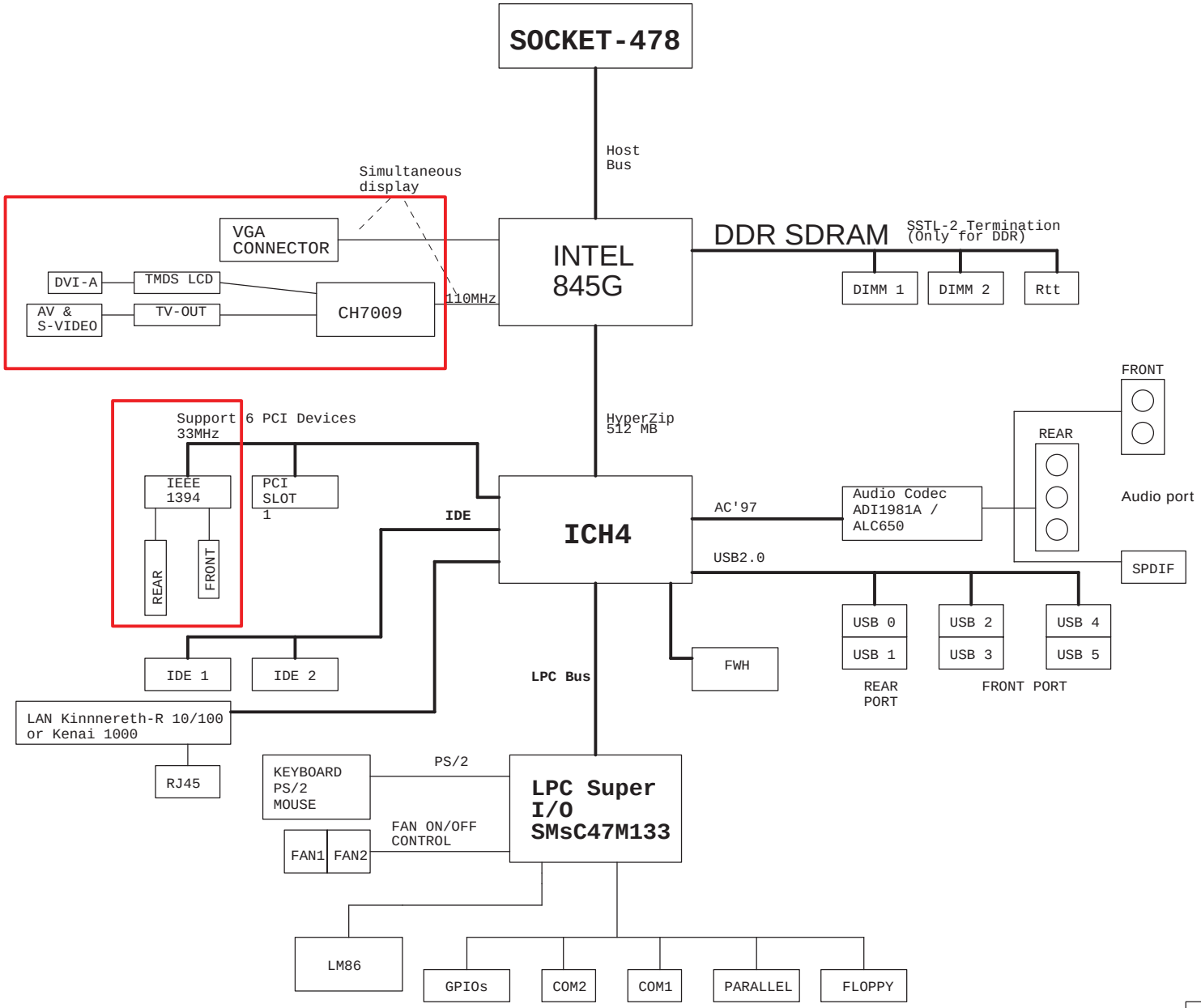
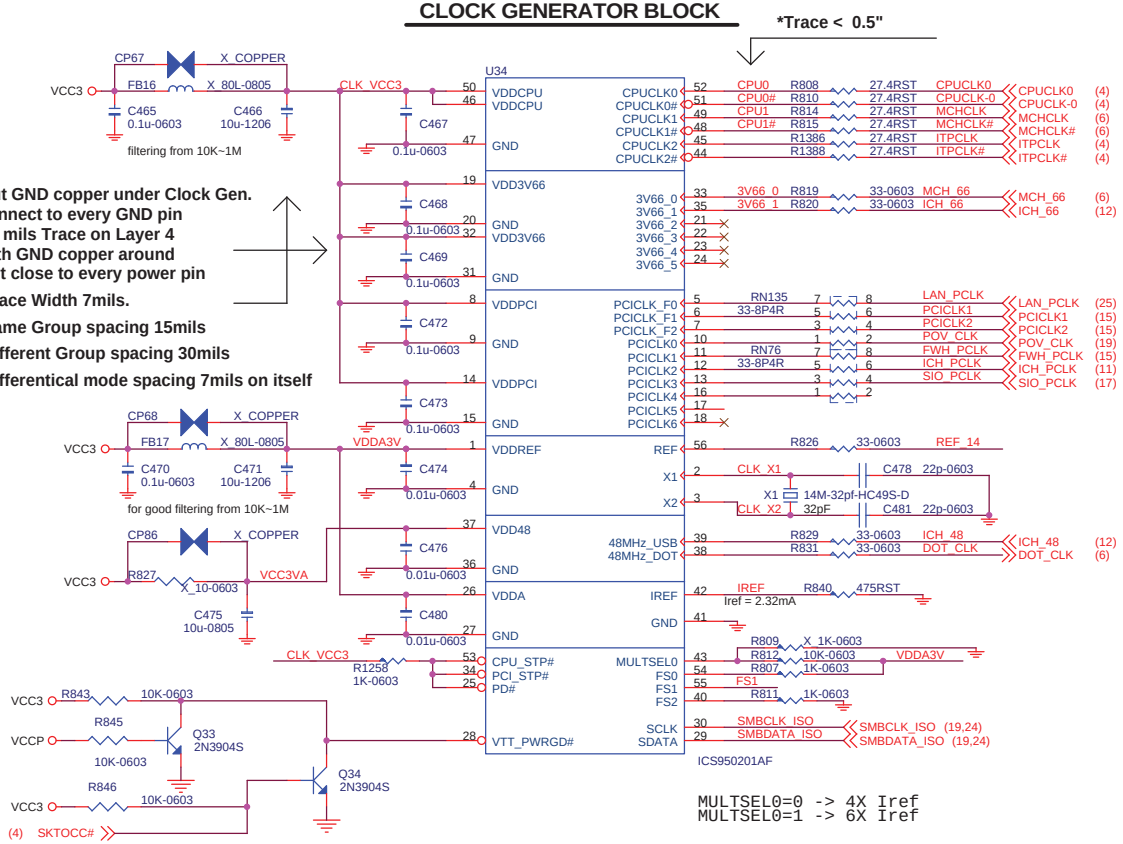
Title	COVER PAGE	
Size C	Document Number MS-6557	Rev 2.1A
Date: Thursday, November 28, 2002	Sheet 1 of 34	

System Block Diagram



MICRO-STAR INT'L CO.,LTD.		
Title: System Block Diagram		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 2 of 34	

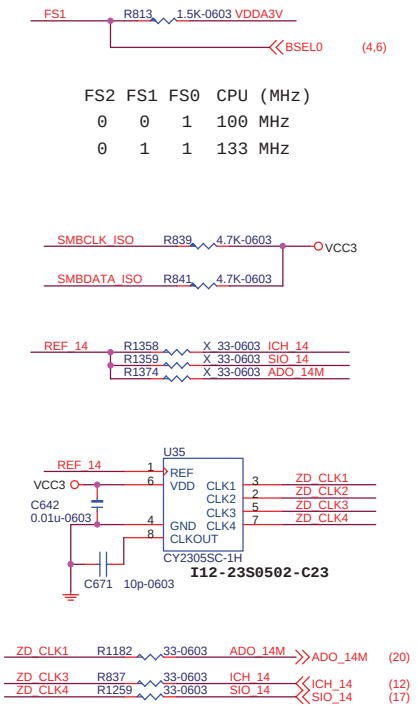
CLOCK GENERATOR BLOCK



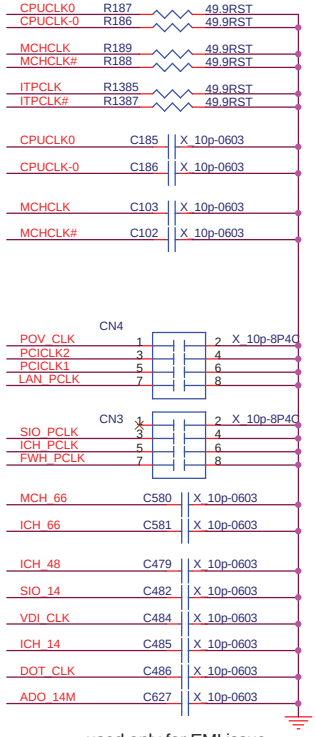
* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
  Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differentical mode spacing 7mils on itself
*

MULTSEL0=0 -> 4X Iref
MULTSEL0=1 -> 6X Iref

CLOCK STRAPPING RESISTORS



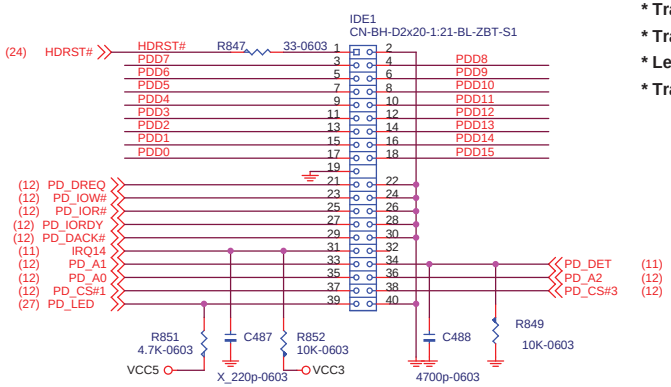
Trace less 0.2"
49.9ohm for 50ohm M/B impedance



used only for EMI issue

Trace less 0.2"

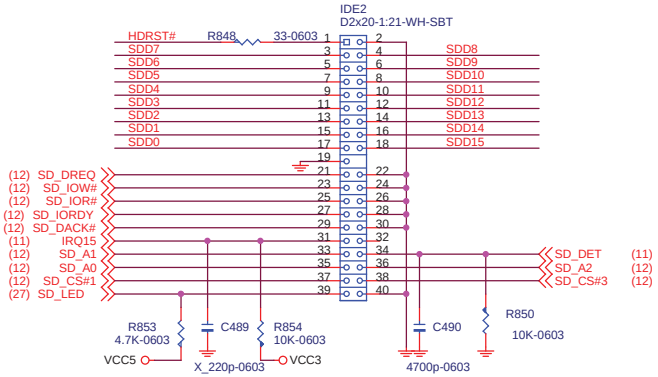
PRIMARY IDE BLOCK



ATA100 IDE CONNECTORS

* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than 6"

SECONDARY IDE BLOCK



PDD[0..15] (12)
SDD[0..15] (12)

MICRO-STAR INT'L CO.,LTD.		
Title: MAIN CLOCK GEN / IDE		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 3 of 34	

CPU SIGNAL BLOCK

For ITP debug

R1391 0-0603 DBRESET# → DBRESET# (12,19,27)

ITPCLK# → ITPCLK# (3)

ITPCLK → ITPCLK (3)

VID[0..4] (23)

(6) HA#[3..31]

A3~A16#, HREQ#0~4 is strobed by HADSTB#0

A17~A35# is strobed by HADSTB#1

U19A

(6) HDBI#[0..3] — HDBI#0 F21 DBI0# / HDBI#1 G25 DBI1# / HDBI#2 P26 DBI2# / HDBI#3 V21 DBI3#

AC3 IERR# / V6 MCERR#

(11) FERR# B6 FERR# / (11) STPCLK# Y4 STPCLK#

AA3 BINIT# / (11,15) HINIT# W5 INIT# / AB2 RSP#

(6) HDBSY# H5 DBSY# / (6) HDRDY# H2 DRDY# / (6) HTRDY# J6 TRDY#

(6) HADS# G1 ADS# / (6) HLOCK# G4 LOCK# / (6) HBNR# G2 BNR# / (6) HIT# F3 HIT# / (6) HITM# E3 HITM# / (6) HBPRI# D2 BPRI# / (6) HDEFER# E2 DEFER#

Trace : 10 mil width 10mil space

ITP_TDI C1 TDI / ITP_TDO D5 TDO / ITP_TMS F7 TMS / ITP_TRST# E6 TRST# / ITP_TCK D4 TCK

(17) CPU_TMPA B3 THERMDA / C4 THERMDC

(11,17) TRMTRIP# A2 THERMTRIP#

(3) SKTOCC# AE26 GND/SKTOCC#

(12) PROCHOT# C3 PROCHOT# / (11) IGNNE# B2 IGNNE# / (11,15,17) HSMI# B5 SMI# / (11) A20M# C6 A20M# / (11) CPUSLP# AB26 SLP#

A22 RESERVED0 / A7 RESERVED1 / AD2 RESERVED2 / AD3 RESERVED3 / AE21 RESERVED4 / AF24 RESERVED5 / AF25 RESERVED6

(3,6) BSEL0 AD6 BSEL0 / AD5 BSEL1

(12) CPU_GD AB23 PWRGOOD

(6) CPURST# AB25 RESET#

(6) HD#[0..63] — HD#63 AA24 D63# / HD#62 AA22 D62# / HD#61 AA25 D61# / HD#60 Y21 D60# / HD#59 Y24 D59# / HD#58 Y23 D58# / HD#57 W25 D57# / HD#56 Y26 D56# / HD#55 W26 D55# / HD#54 V24 D54#

D53# D52# D51# D50# D49# D48# D47# D46# D45# D44# D43# D42# D41# D40# D39# D38# D37# D36# D35# D34# D33# D32# D31# D30# D29# D28# D27# D26# D25# D24# D23# D22# D21# D20# D19# D18# D17# D16# D15# D14# D13# D12# D11# D10# D9# D8# D7# D6# D5# D4# D3# D2# D1# D0#

HD#53 V23 HD#52 U25 HD#51 V25 HD#50 U23 HD#49 U24 HD#48 U26 HD#47 T23 HD#46 T25 HD#45 T26 HD#44 R24 HD#43 R25 HD#42 P24 HD#41 R23 HD#40 N25 HD#39 N26 HD#38 M26 HD#37 M23 HD#36 M24 HD#35 P23 HD#34 P21 HD#33 N22 HD#32 M23 HD#31 H25 HD#30 K23 HD#29 J24 HD#28 L22 HD#27 M21 HD#26 H24 HD#25 G26 HD#24 L21 HD#23 D26 HD#22 F26 HD#21 E25 HD#20 F24 HD#19 F23 HD#18 G23 HD#17 E24 HD#16 H23 HD#15 D25 HD#14 J23 HD#13 D23 HD#12 C26 HD#11 H22 HD#10 G25 HD#9 B26 HD#8 C24 HD#7 C23 HD#6 B24 HD#5 C22 HD#4 A25 HD#3 A23 HD#2 B23 HD#1 B22 HD#0 B25

A35# A34# A33# A32# A31# A30# A29# A28# A27# A26# A25# A24# A23# A22# A21# A20# A19# A18# A17# A16# A15# A14# A13# A12# A11# A10# A9# A8# A7# A6# A5# A4# A3#

AB1 HA#31 / Y1 HA#30 / W2 HA#29 / V3 HA#28 / U4 HA#27 / T5 HA#26 / W1 HA#25 / R6 HA#24 / V2 HA#23 / T4 HA#22 / U3 HA#21 / P6 HA#20 / U1 HA#19 / T2 HA#18 / R3 HA#17 / P4 HA#16 / P3 HA#15 / R2 HA#14 / T1 HA#13 / N5 HA#12 / N4 HA#11 / N2 HA#10 / M1 HA#9 / N1 HA#8 / M4 HA#7 / M3 HA#6 / L2 HA#5 / M6 HA#4 / L3 HA#3 / K1 HA#2

DBR# AE25 / VCC_SENSE A5 / VSS_SENSE A4 / ITP_CLK1 AD26 / ITP_CLK0 AC26

VID4# AE1 VID4 / VID3# AE2 VID3 / VID2# AE3 VID2 / VID1# AE4 VID1 / VID0# AE5 VID0

GTLREF3 AA21 / GTLREF2 AA6 / GTLREF1 F20 / GTLREF0 F6 — GTLREF1

BPM5# AB4 BPM#5 / BPM4# AA5 BPM#4 / BPM3# Y6 / BPM2# AC4 / BPM1# AB5 BPM#1 / BPM0# AC6 BPM#0

REQ4# H3 HREQ#4 / REQ3# J3 HREQ#3 / REQ2# J4 HREQ#2 / REQ1# K5 HREQ#1 / REQ0# J1 HREQ#0 → HREQ#[0..4] (6)

TESTHI12 AD25 / TESTHI11 A6 R855 49.9RST / TESTHI10 Y3 R856 49.9RST / TESTHI9 W4 R857 49.9RST / TESTHI8 U6 R858 49.9RST / TESTHI7 AB22 / TESTHI6 AA20 / TESTHI5 AC23 / TESTHI4 AC24 / TESTHI3 AC20 / TESTHI2 AC21 / TESTHI1 AA2 R1108 49.9RST → VCCP / TESTHI0 AD24

BCLK1# AF23 → CPUCLK-0 (3) / BCLK0# AF22 → CPUCLK0 (3)

RS2# F4 HRS#2 / RS1# G5 HRS#1 / RS0# F1 HRS#0 → HRS#[0..2] (6)

AP1# V5 / AP0# AC1 / BR0# H6 → HBR#0 (6)

COMP1 P1 R343 49.9RST / COMP0 L24 R233 49.9RST

* Short trace

DP3# L25 / DP2# K26 / DP1# K25 / DP0# J26

ADSTB1# R5 → HADSTB#1 (6) / ADSTB0# L5 → HADSTB#0 (6)

DSTBP3# W23 → HDSTBP#3 (6) / DSTBP2# P23 → HDSTBP#2 (6) / DSTBP1# J23 → HDSTBP#1 (6) / DSTBP0# F21 → HDSTBP#0 (6)

DSTBN3# W22 → HDSTBN#3 (6) / DSTBN2# R22 → HDSTBN#2 (6) / DSTBN1# K22 → HDSTBN#1 (6) / DSTBN0# F22 → HDSTBN#0 (6)

Differential Host Data Strobes

LINT1/NMI E5 → NMI (11) / LINT0/INTR D1 → INTR (11)

PGA-S478-F02

MSI part number = N12-4780010-A10

= N12-4780010-M06

D00~D15, HDBI#0 is strobed by HDSTBN/P#0

D16~D31, HDBI#1 is strobed by HDSTBN/P#1

D32~D47, HDBI#2 is strobed by HDSTBN/P#2

D48~D63, HDBI#3 is strobed by HDSTBN/P#3

CPU GTL REFERNCE VOLTAGE BLOCK

Length < 1.5inch.

VCCP — R227 49.9RST — 2/3*Vccp — GTLREF1 — C260 220p-0603 — C261 0.1u-0603 — C237 1u-0603 — R226 100RST

Every pin put one 220pF cap near it.

Trace Width 15mils, Space 15mils.

Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

A20M# R1145 X 62-0603 → VCCP

CPUSLP# R1146 X 62-0603

IGNNE# R1147 X 62-0603

HINIT# R1148 X 62-0603

INTR R1149 X 62-0603

NMI R1150 X 62-0603

HSMI# R1151 X 62-0603

STPCLK# R1152 X 62-0603

FERR# R1153 X 62-0603

CPU ITP BLOCK

ITP_TMS R337 39-0603 → VCCP

ITP_TDO R332 75-0603

ITP_TCK R344 27-0603

CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU

PROCHOT# R345 62-0603 → VCCP

CPU_GD R224 300-0603

HBR#0 R290 150-0603

CPURST# R222 49.9RST

RN46 47-8P4R

BPM#0 1 2 → VCCP

BPM#1 3 4

BPM#5 5 6

BPM#4 7 8

ITP_TDI R297 150-0603 → VCCP

ITP_TRST# R330 680-0603

CPU_GD C236 X 102p-0603

CPURST# C234 X 102p-0603

CPUSLP# C235 X 223p-0603

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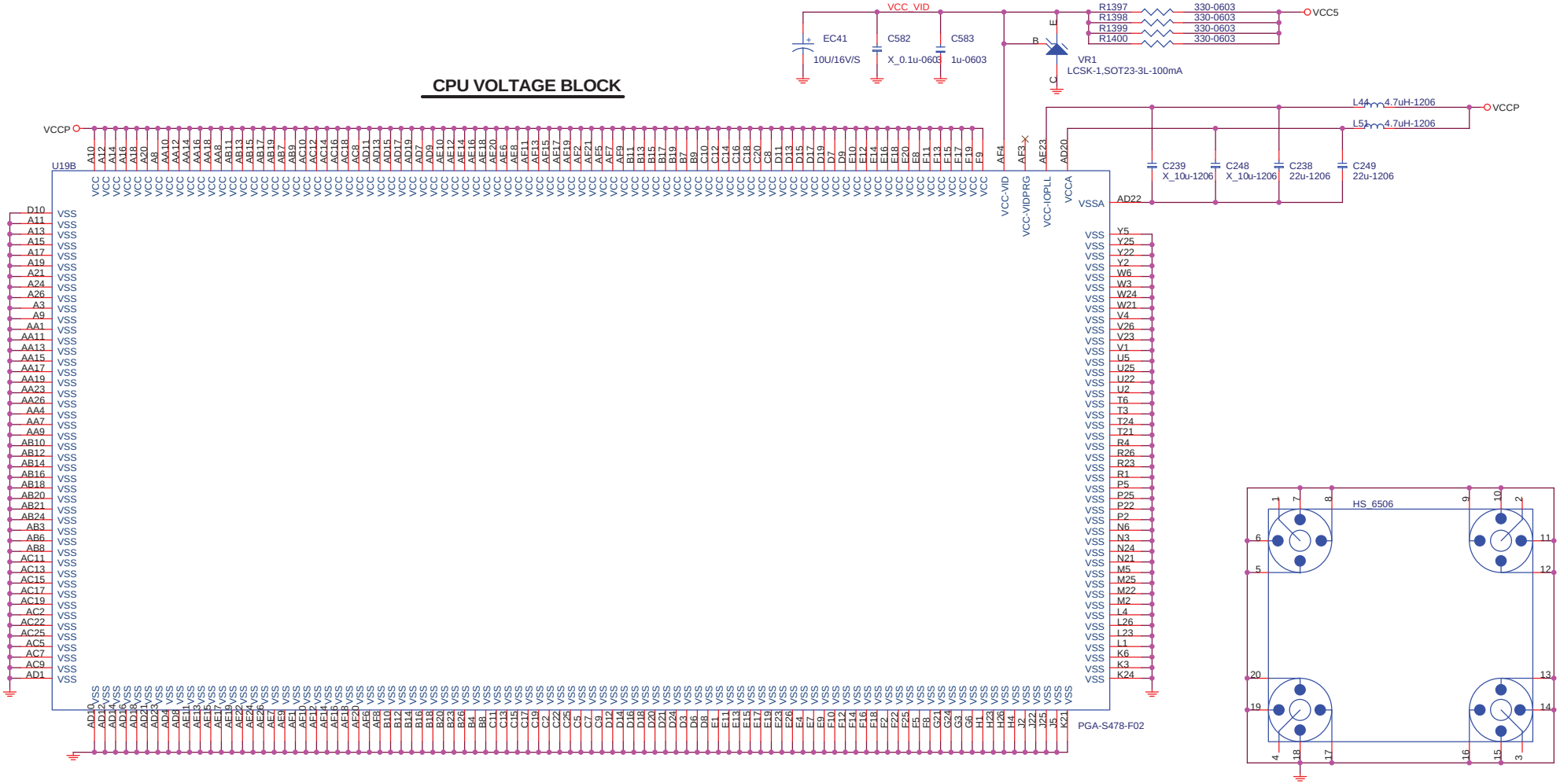
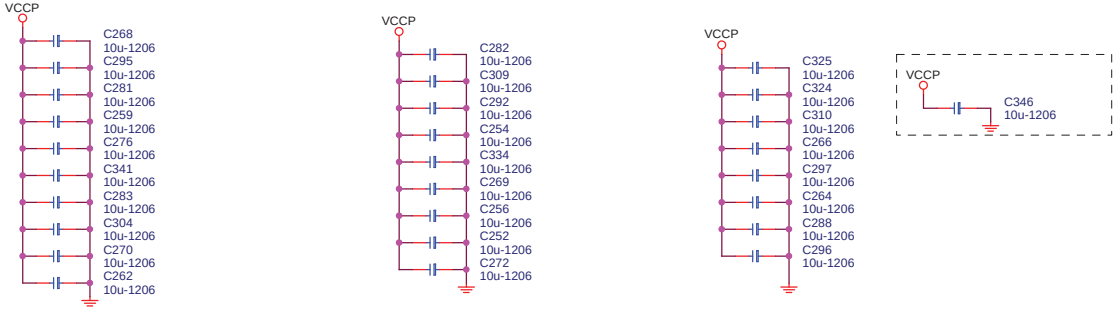
Title: mPGA478 CPU-1		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 4 of 34	

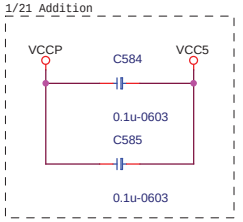
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

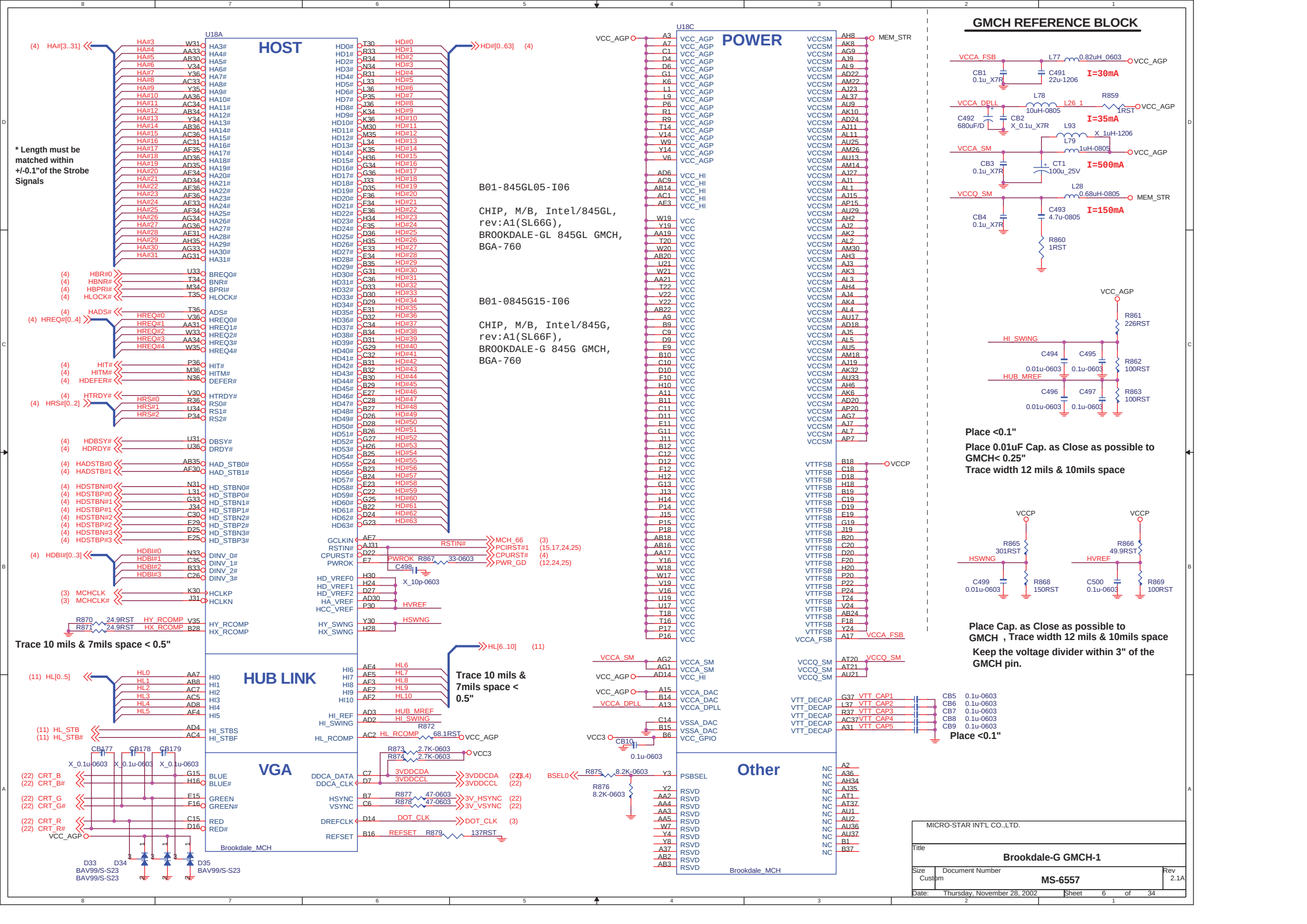


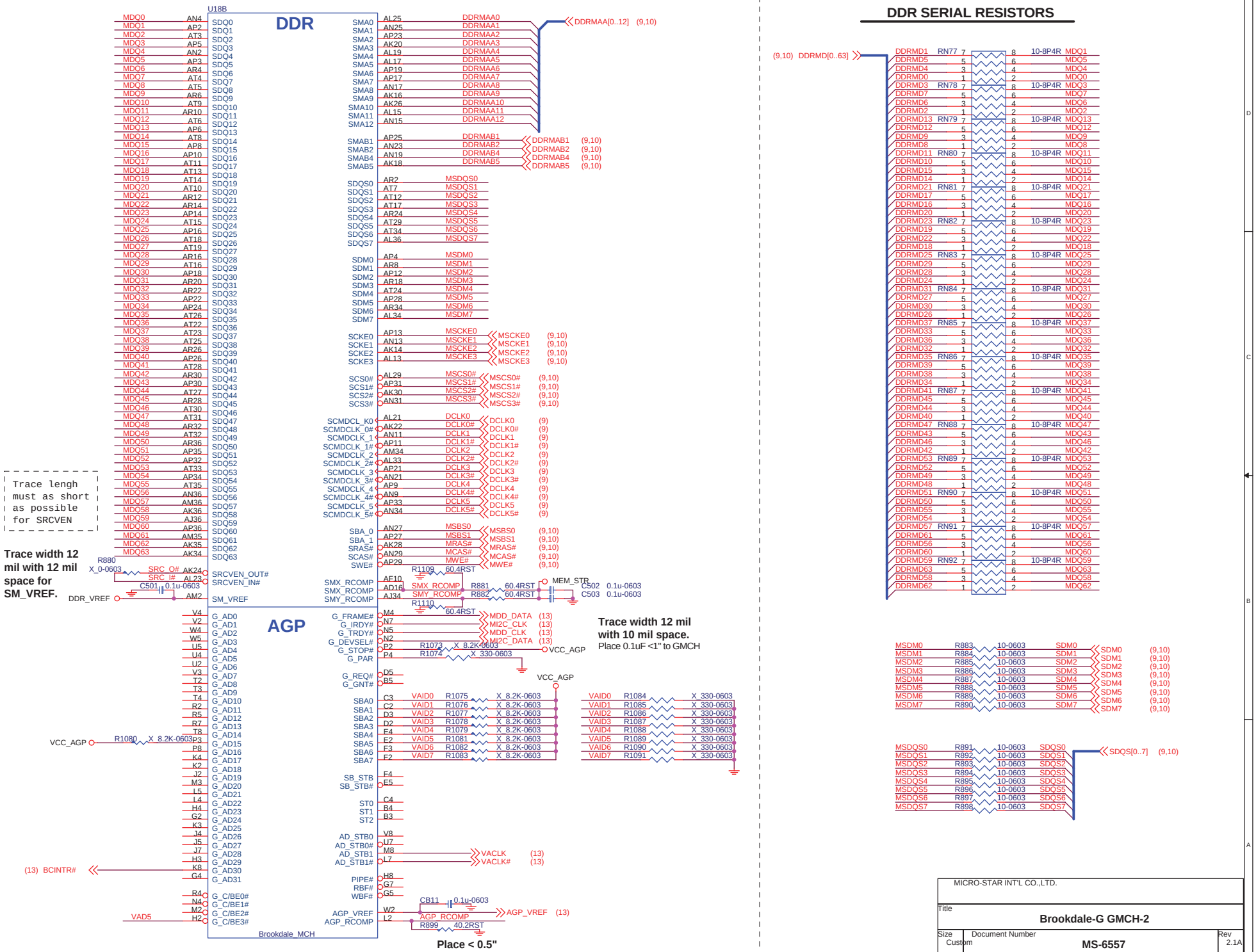
MICRO-STAR INT'L CO.,LTD.

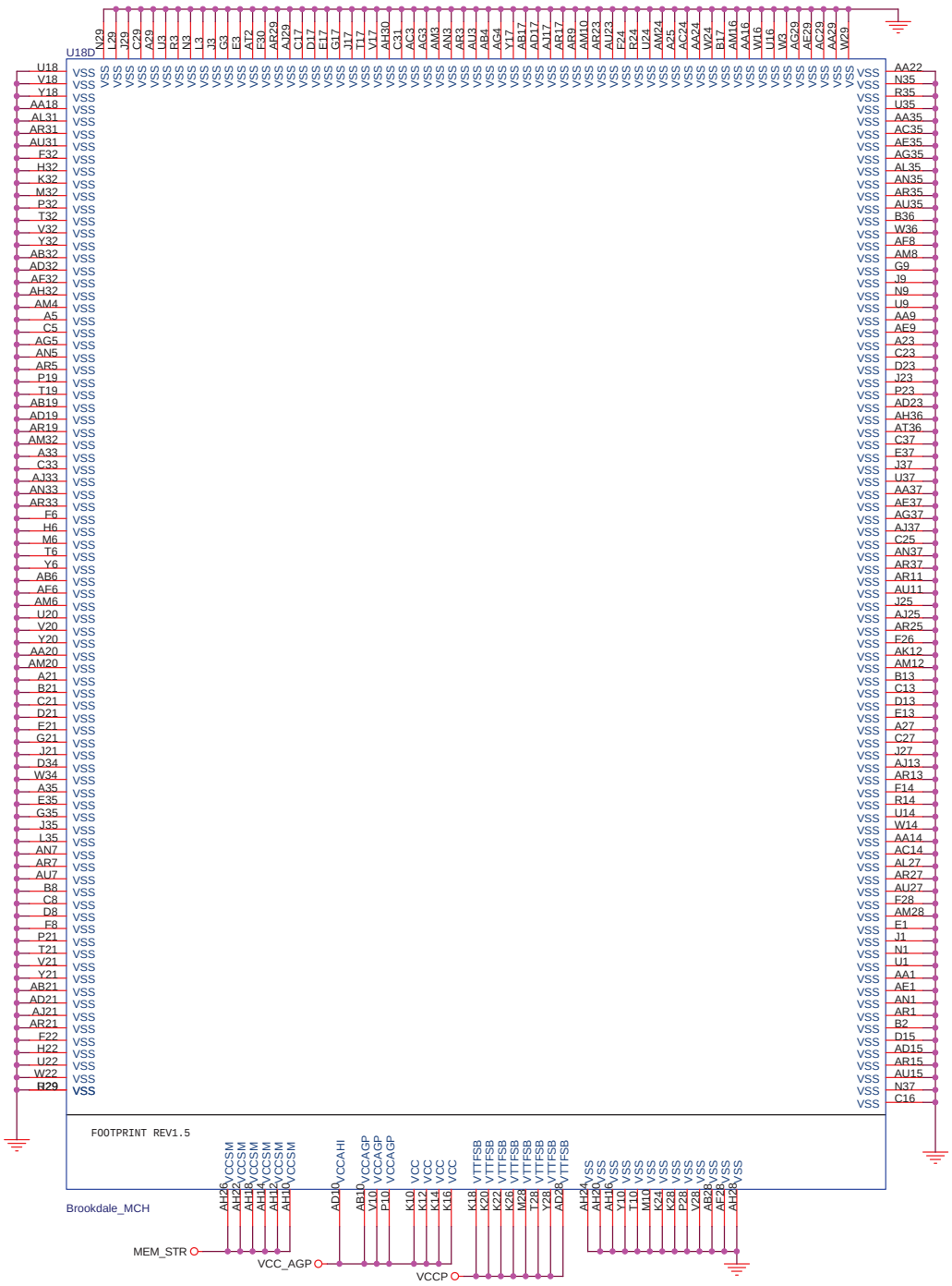
Title: **mPGA478 CPU-2**

Size: Custom | Document Number: **MS-6557** | Rev: 2.1A

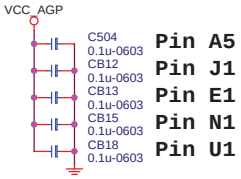
Date: Thursday, November 28, 2002 | Sheet 5 of 34


HOST
U18A
HUB LINK
VGA
Brookdale_MCH
POWER
U18C
Other
Brookdale_MCH
* Length must be matched within +/-0.1"of the Strobe Signals
B01-845GL05-I06
CHIP, M/B, Intel/845GL, rev:A1(SL66G), BROOKDALE-GL 845GL GMCH, BGA-760
B01-0845G15-I06
CHIP, M/B, Intel/845G, rev:A1(SL66F), BROOKDALE-G 845G GMCH, BGA-760
Trace 10 mils & 7mils space < 0.5"
Trace 10 mils & 7mils space < 0.5"
GMCH REFERENCE BLOCK
I=30mA
I=35mA
I=500mA
I=150mA
Place <0.1"
Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space
Place Cap. as Close as possible to GMCH ，Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the GMCH pin.
Place <0.1"
MICRO-STAR INT'L CO.,LTD.
Title
Brookdale-G GMCH-1
Size
Custom
Document Number
MS-6557
Rev
2.1A
Date:
Thursday, November 28, 2002
Sheet
6
of
34


DDR
AGP
U18B
Brookdale_MCH
Trace lengh must as short as possible for SRCVEN
Trace width 12 mil with 12 mil space for SM_VREF.
Trace width 12 mil with 10 mil space.
Place 0.1uF <1" to GMCH
Place < 0.5"
DDR SERIAL RESISTORS
MICRO-STAR INT'L CO.,LTD.
Title
Brookdale-G GMCH-2
Size
Custom
Document Number
MS-6557
Rev
2.1A
Date: Thursday, November 28, 2002
Sheet 7 of 34



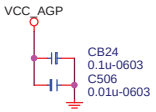
GMCH DECOUPLING CAPACITOR



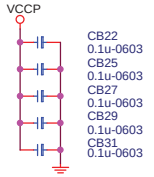
Place decoupling cap close to GMCH AGP Interface < 0.1"

Place decoupling cap close to GMCH Hub-Link Interface< 0.1"

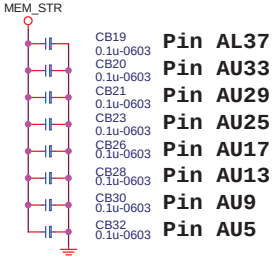
Place decoupling cap close to GMCH DAC Interface< 0.1"



Place decoupling cap close to GMCH Core Logic Interface < 0.1"

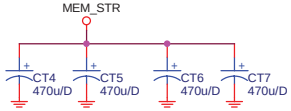


Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor

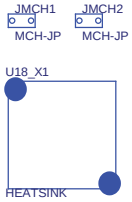


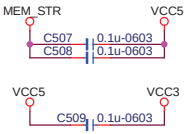
Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width

Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot





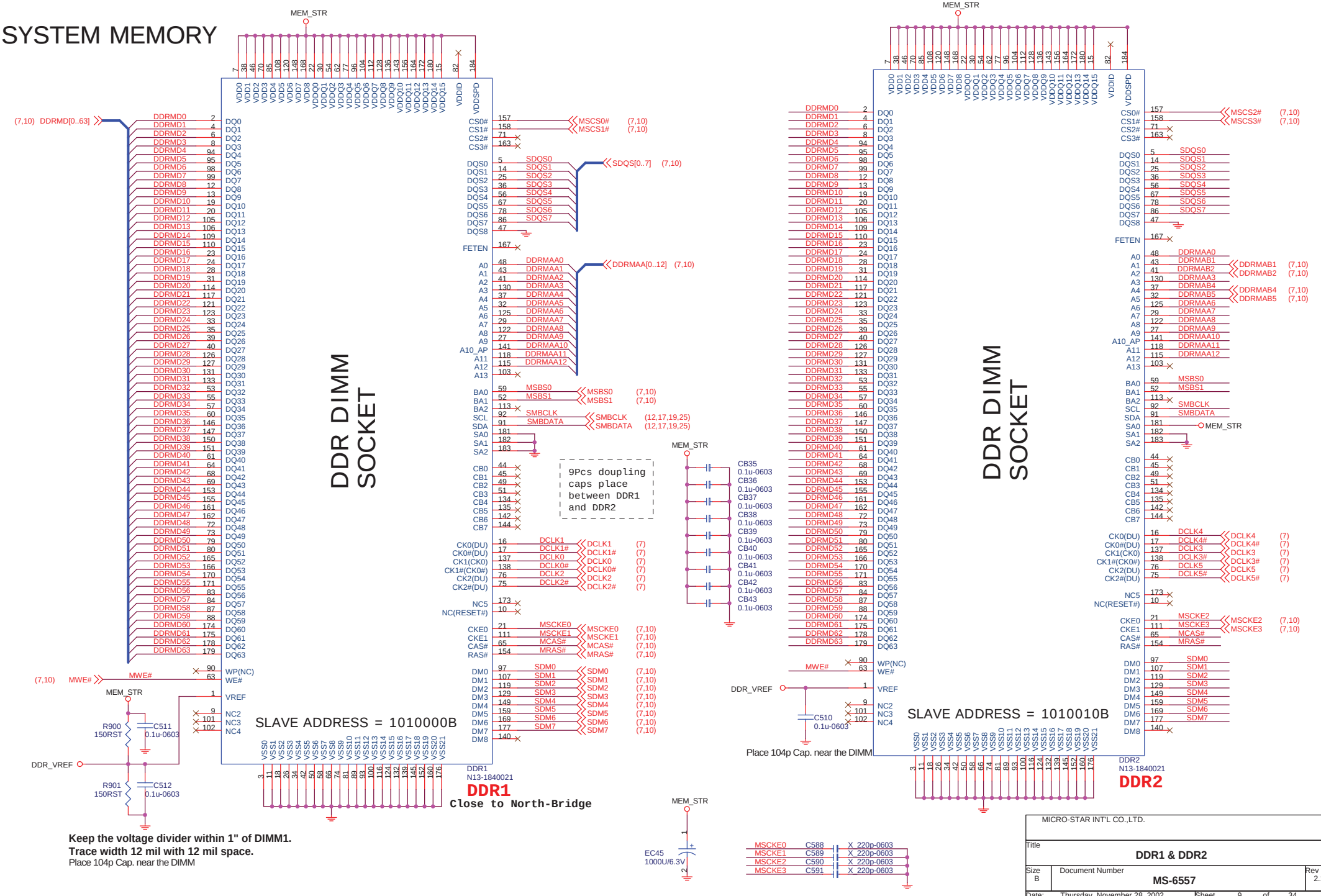
MICRO-STAR INT'L CO.,LTD.

Title: Brookdale-G GMCH-3

Size: Custom | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 8 of 34

SYSTEM MEMORY



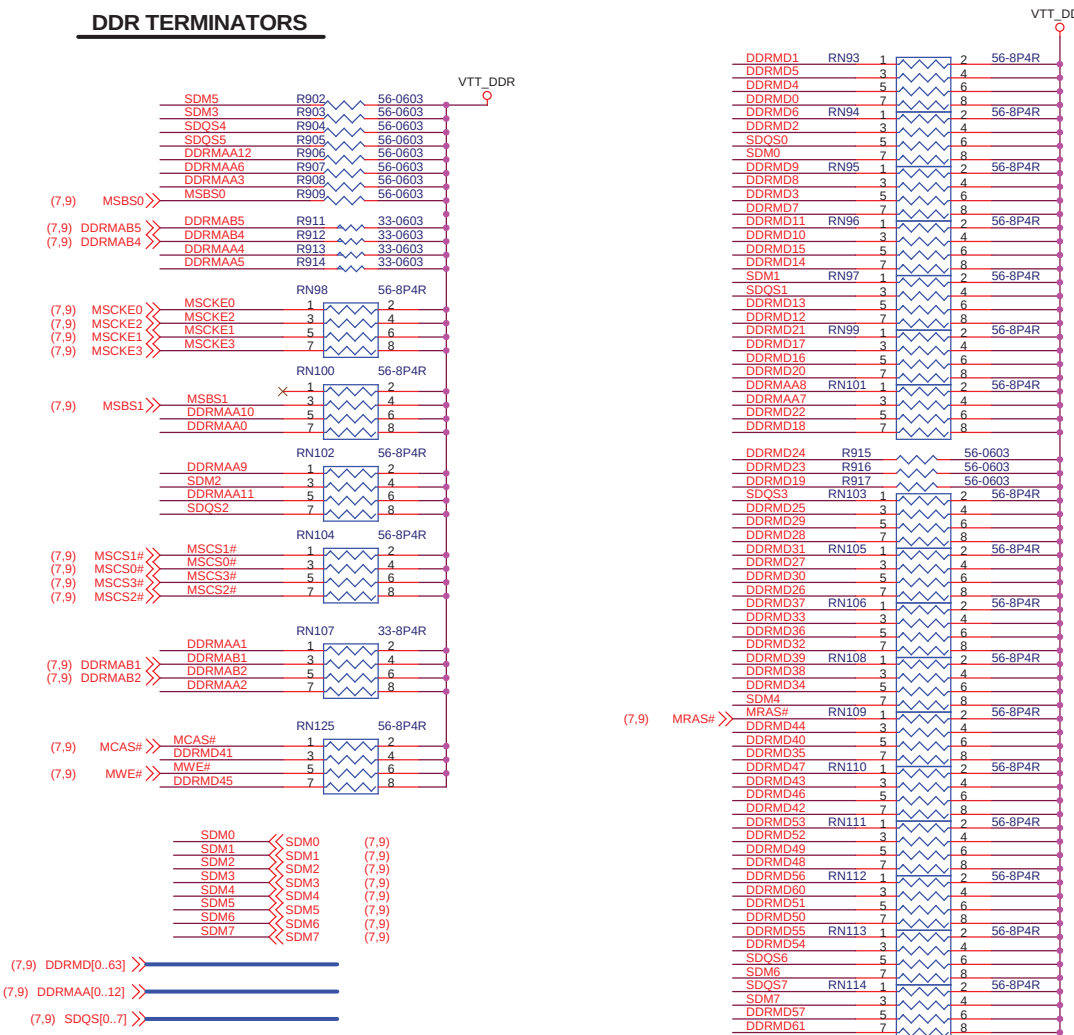
MICRO-STAR INT'L CO.,LTD.

Title: DDR1 & DDR2

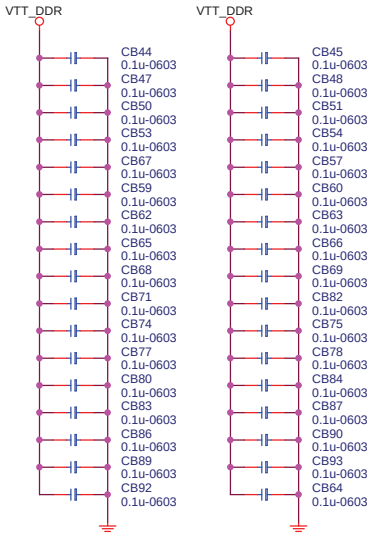
Size: B | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 9 of 34

DDR TERMINATORS

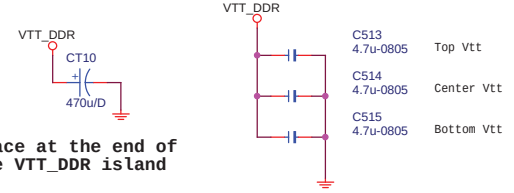


DDR Decouping Caps



Total 110 signal, need 55 pcs decoupling.

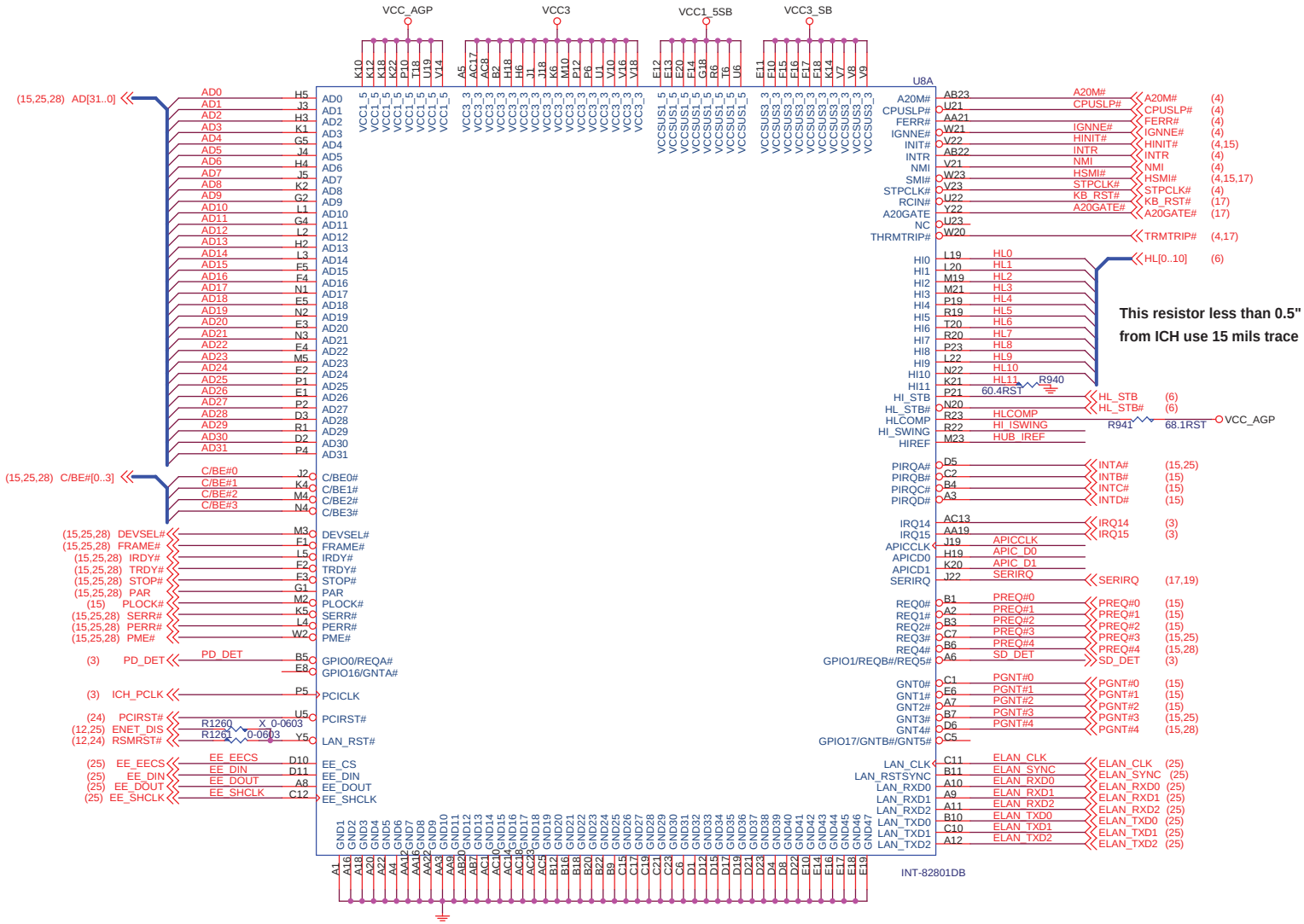
Place for VTT_DDR island



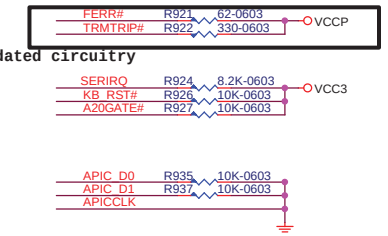
Place at the end of the VTT_DDR island

MICRO-STAR INT'L CO.,LTD.		
Title: DDR TERMINATOR		
Size: B	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 10 of 34	

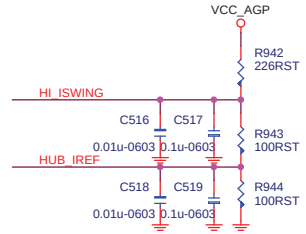
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



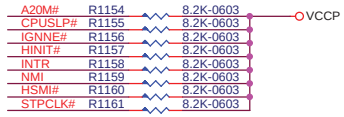
ICH4 STRAPPING RESISTORS



ICH4 REFERENCE VOLTAGE

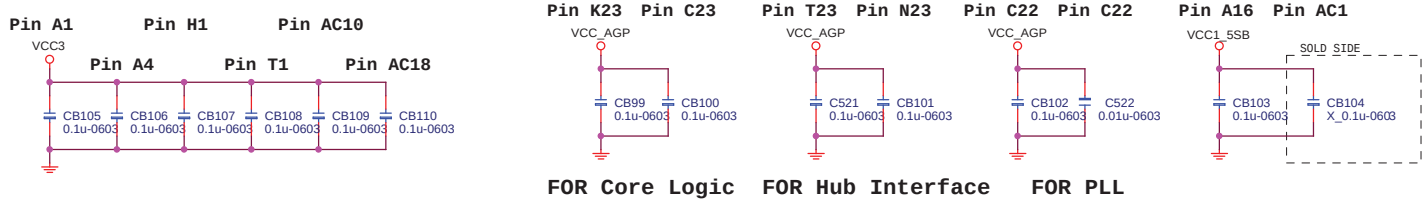


Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space



ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil

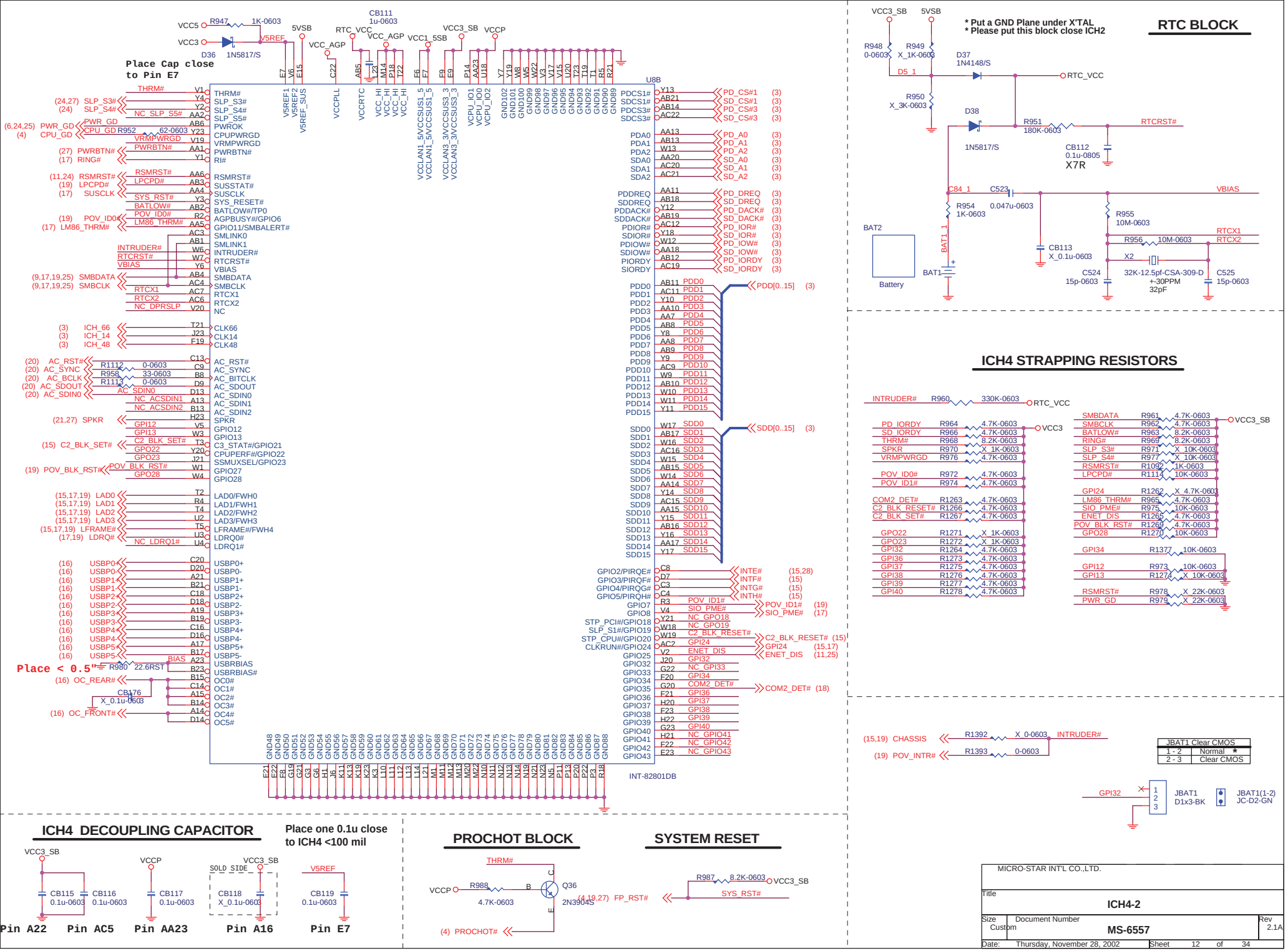


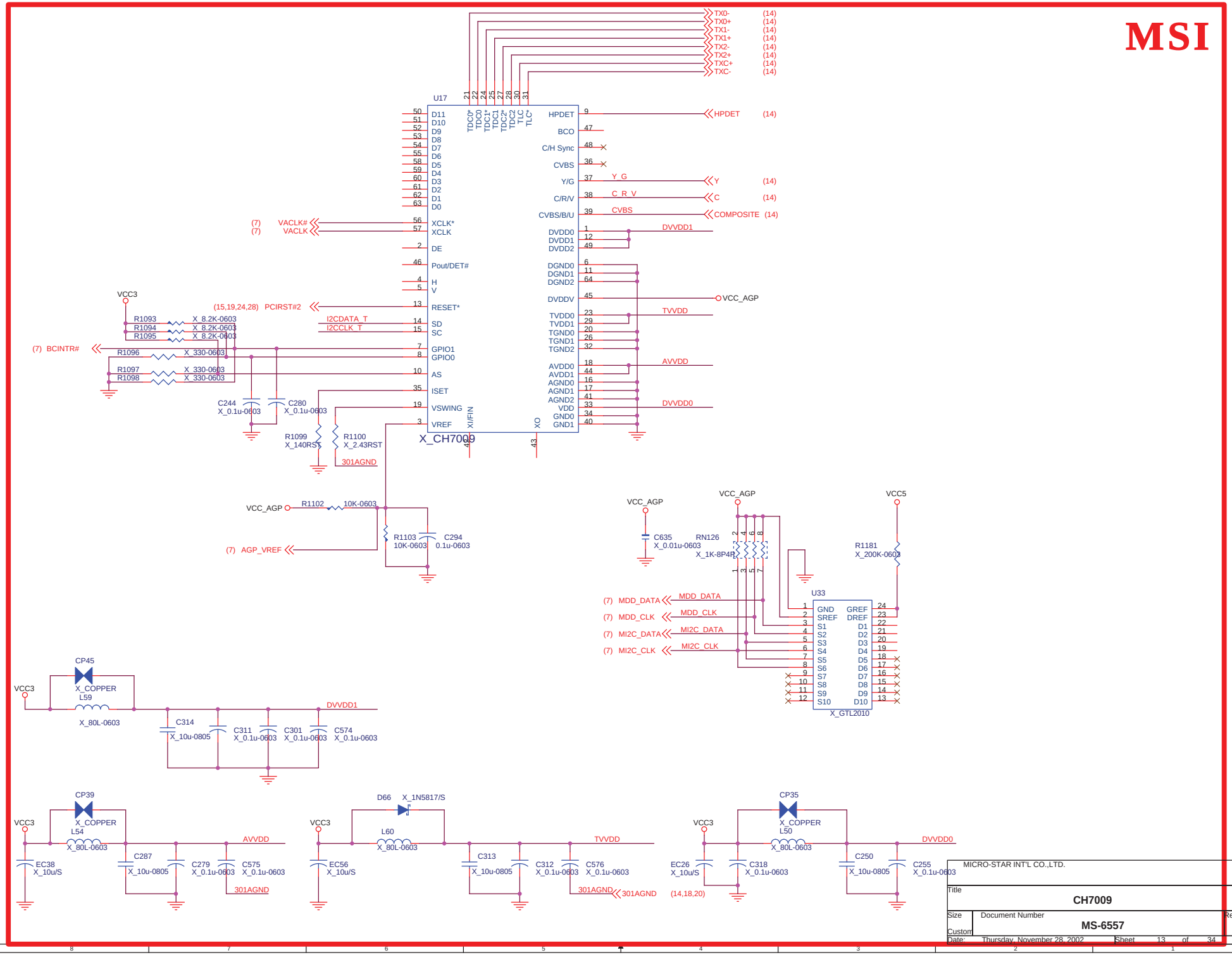
MICRO-STAR INT'L CO.,LTD.

Title: ICH4-1

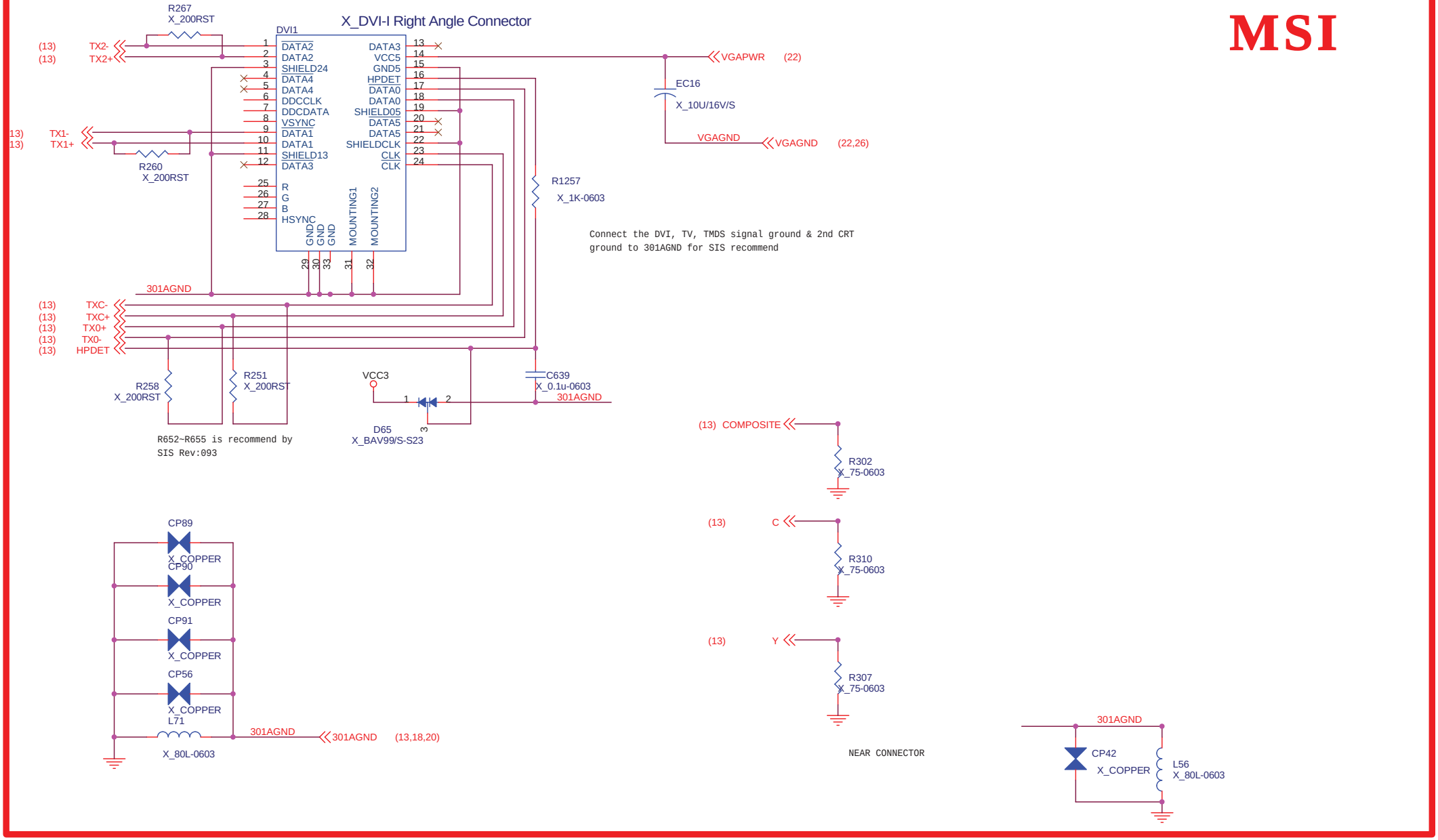
Size: Custom | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 11 of 34


Place Cap close to Pin E7
U8B
INT-82801DB
RTC BLOCK
* Put a GND Plane under X'TAL
* Please put this block close ICH2
ICH4 STRAPPING RESISTORS
ICH4 DECOUPLING CAPACITOR
Place one 0.1u close to ICH4 <100 mil
PROCHOT BLOCK
SYSTEM RESET
Pin A22
Pin AC5
Pin AA23
Pin A16
Pin E7
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
MICRO-STAR INT'L CO.,LTD.
Title
ICH4-2
Size Custom
Document Number MS-6557
Rev 2.1A
Date: Thursday, November 28, 2002
Sheet 12 of 34


MSI
U17
X_CH7009
TX0- (14)
TX0+ (14)
TX1- (14)
TX1+ (14)
TX2- (14)
TX2+ (14)
TXC+ (14)
TXC- (14)
HPDET (14)
Y (14)
C (14)
COMPOSITE (14)
DVVDD1
VCC_AGP
TVVDD
AVVDD
DVVDD0
(7) VACLK#
(7) VACLK
(15,19,24,28) PCIRST#2
(7) BCINTR#
I2CDATA_T
I2CCLK_T
R1093 X_8.2K-0603
R1094 X_8.2K-0603
R1095 X_8.2K-0603
R1096 X_330-0603
R1097 X_330-0603
R1098 X_330-0603
C244 X_0.1u-0603
C280 X_0.1u-0603
R1099 X_140RST
R1100 X_2.43RST
301AGND
R1102 10K-0603
R1103 10K-0603
C294 0.1u-0603
(7) AGP_VREF
C635 X_0.01u-0603
RN126 X_1K-8P4R
R1181 X_200K-0603
VCC5
U33
X_GTL2010
(7) MDD_DATA
MDD_DATA
(7) MDD_CLK
MDD_CLK
(7) MI2C_DATA
MI2C_DATA
(7) MI2C_CLK
MI2C_CLK
CP45
X_COPPER
L59
X_80L-0603
C314 X_10u-0805
C311 X_0.1u-0603
C301 X_0.1u-0603
C574 X_0.1u-0603
CP39
L54
EC38 X_10u/S
C287 X_10u-0805
C279 X_0.1u-0603
C575 X_0.1u-0603
D66 X_1N5817/S
L60
EC56 X_10u/S
C313 X_10u-0805
C312 X_0.1u-0603
C576 X_0.1u-0603
CP35
L50
EC26 X_10u/S
C318 X_0.1u-0603
C250 X_10u-0805
C255 X_0.1u-0603
(14,18,20)
MICRO-STAR INT'L CO.,LTD.
Title
CH7009
Size
Document Number
MS-6557
Rev 2.1A
Custom
Date: Thursday, November 28, 2002
Sheet 13 of 34

DVI Interface



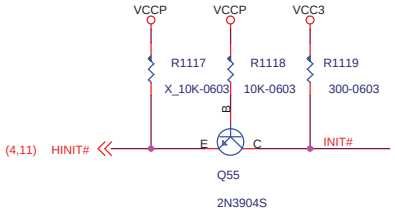
MSI COMPUTER		
Title: DVI, TV-OUT, 2nd CRT CONN		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 14 of 34	

PCI SLOT

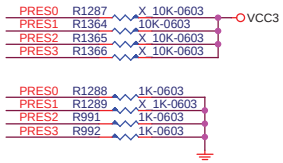
AD17 INTB#

PCI RISER CARD PCI1 & 2 : AD17 & AD18

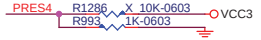
FWH INIT Signal Voltage Translation Block



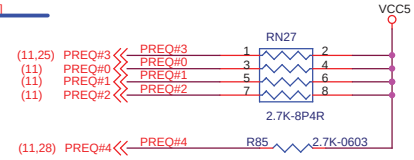
FWH RESISTORS

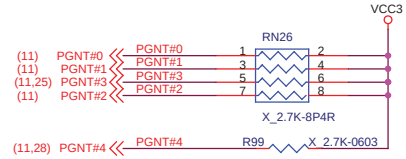


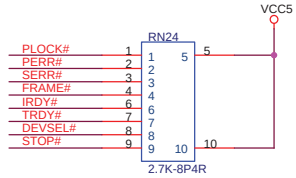
PULL UP 10/100 ethernet
PULL DOWN Gigabit ethernet

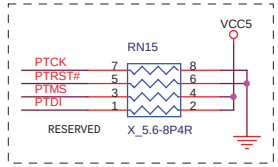


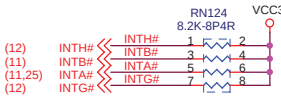
PCI BUS PULL-UP

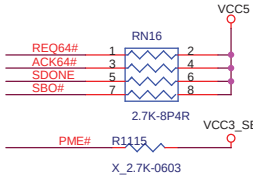




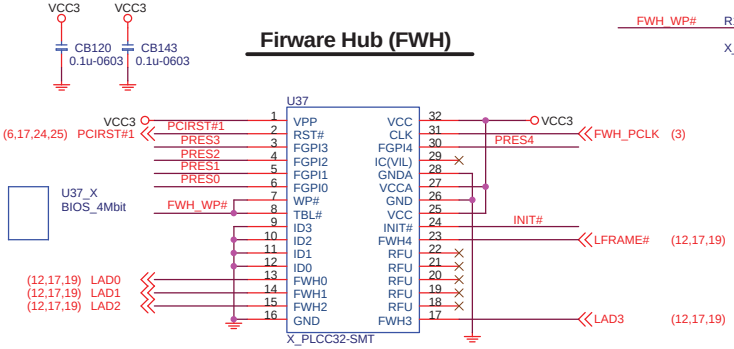








Firware Hub (FWH)



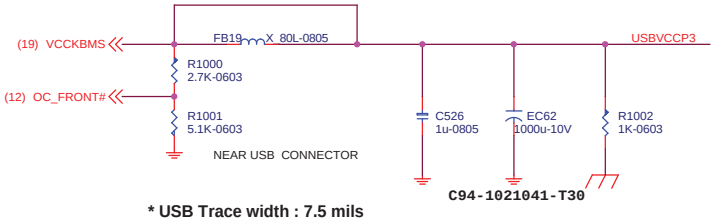
FWH Write Protect Circuit

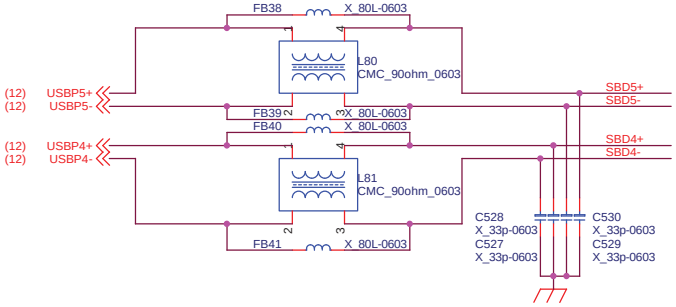
PCI-D120-WH-SN

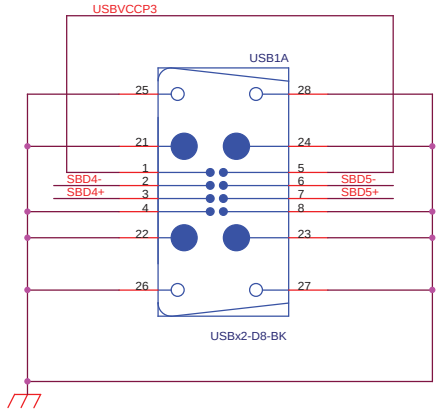
WIDE TRACE FOR PC2001

MICRO-STAR INT'L CO.,LTD.	
Title	PCI SLOT / FWH
Size: Custom	Document Number: MS-6557
Rev	2.1A
Date: Thursday, November 28, 2002	Sheet 15 of 34

POWER CIRCUIT FOR USB PORT 4,5

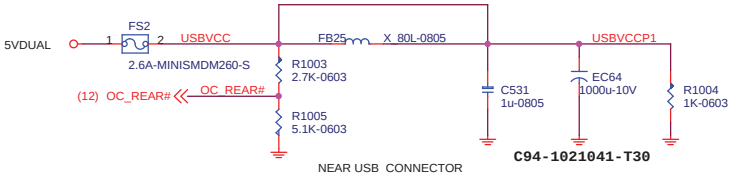


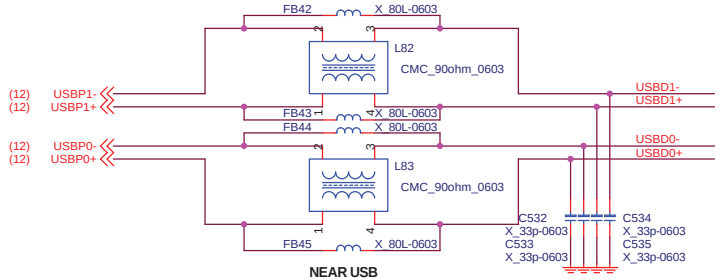


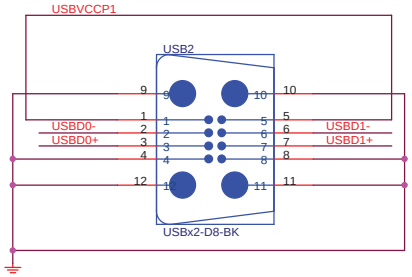


* USB Trace width : 7.5 mils
* USB Trace Spacing : Low speed 20 mils, High speed 50 mils
* Differential USB Signlas Trace, Spacing : 7.5 mils
* USB Power Trace must be 40mils width
* Length(longest)-Length(shortest)<150mils
* Maxium trace length <16"

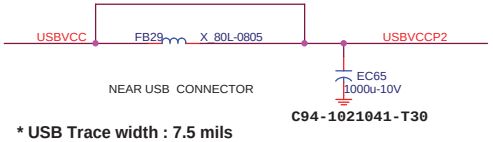
POWER CIRCUIT FOR USB PORT 0,1

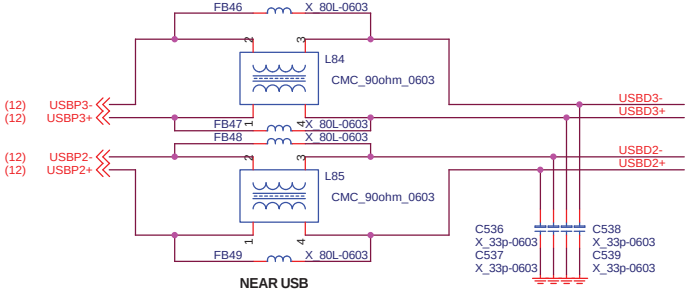


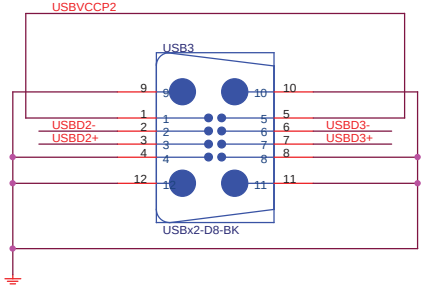




POWER CIRCUIT FOR USB PORT 2,3







* USB Trace width : 7.5 mils
* USB Trace Spacing : Low speed 20 mils, High speed 50 mils
* Differential USB Signlas Trace, Spacing : 7.5 mils
* USB Power Trace must be 40mils width
* Length(longest)-Length(shortest)<150mils
* Maxium trace length <5"

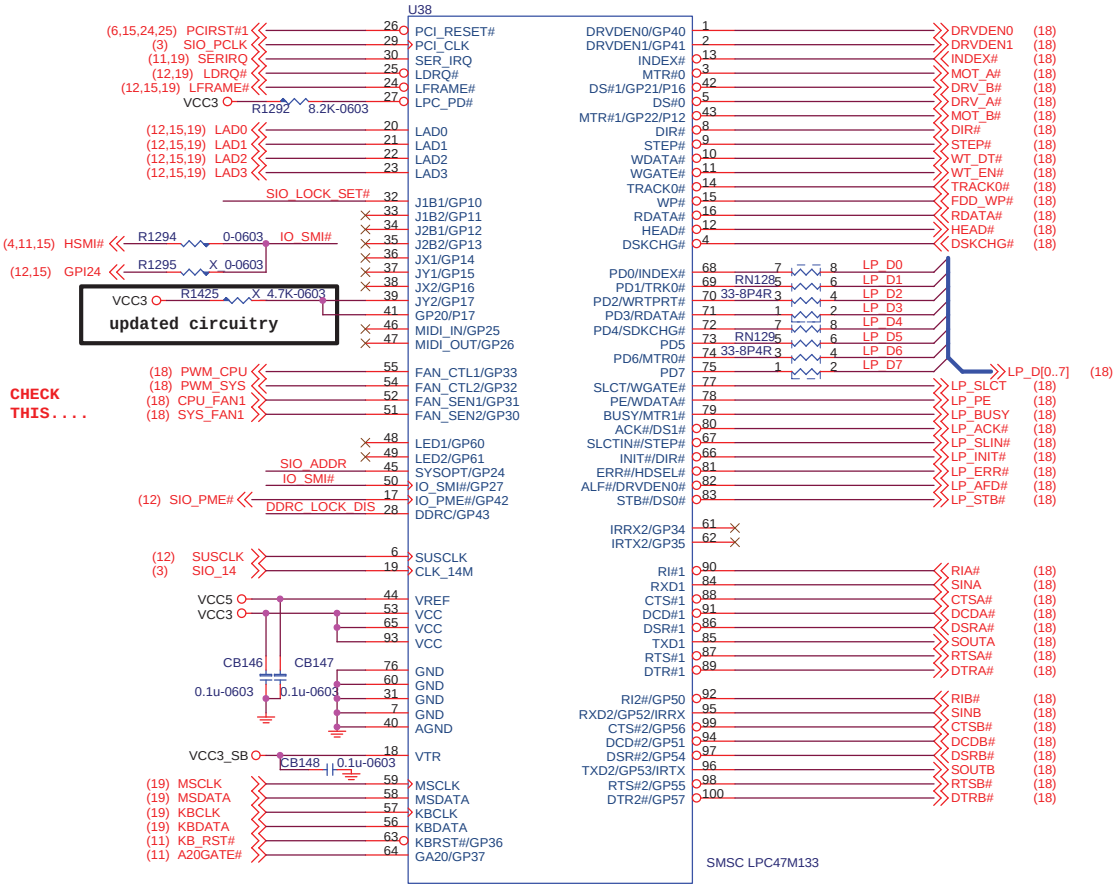
MICRO-STAR INT'L CO.,LTD.

Title: USB CONNECTOR

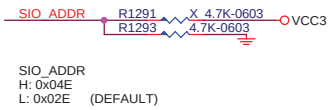
Size	Document Number	Rev
Custom	MS-6557	2.1A

Date: Thursday, November 28, 2002 Sheet 16 of 34

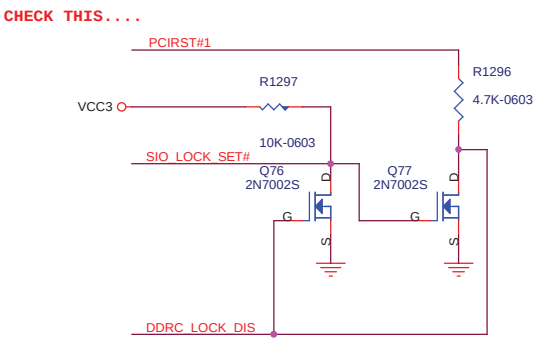
LPC SUPER I/O LPC47M133



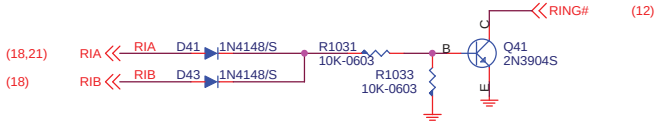
LPC I/O STRAPPING RESISTOR



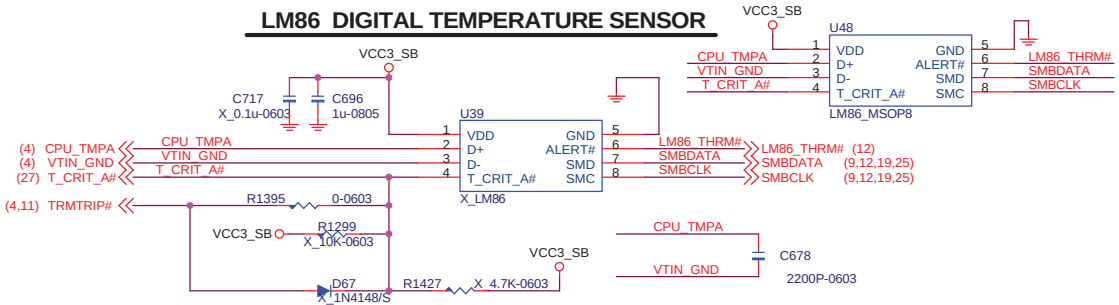
FDD WRITE-PROTECT LATCH



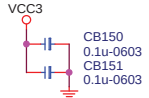
Wake On Modem Header



LM86 DIGITAL TEMPERATURE SENSOR



LPC I/O DECOUPLING CAPACITORS



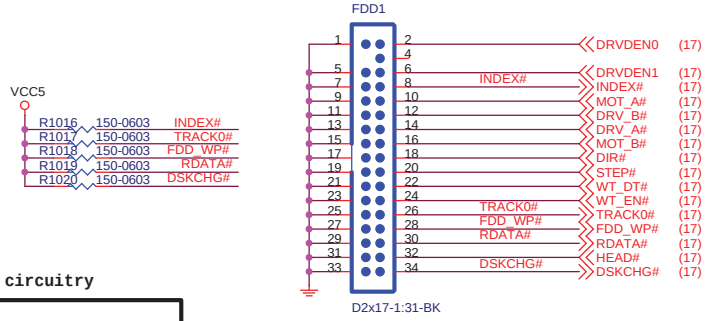
MICRO-STAR INT'L CO.,LTD.

Title: SMsC_LPC47M133

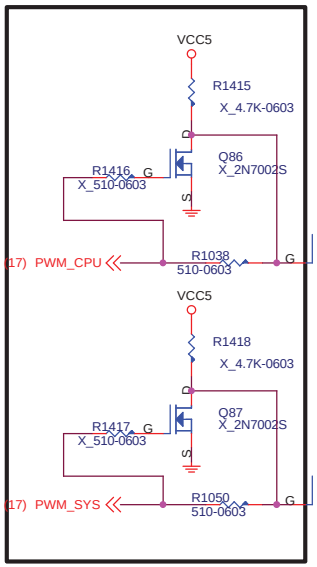
Size: Custom | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 17 of 34

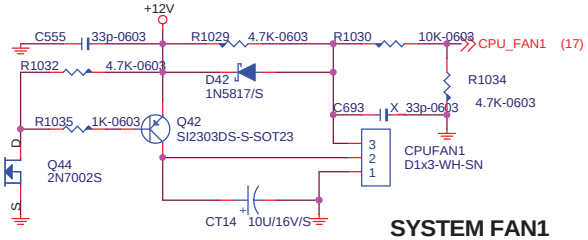
FLOPPY CONNECTOR



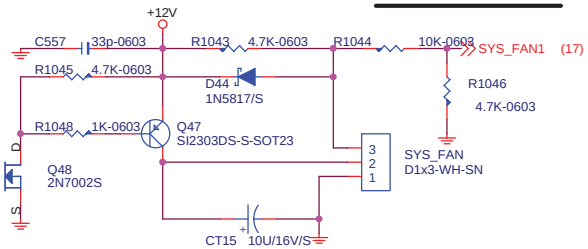
updated circuitry

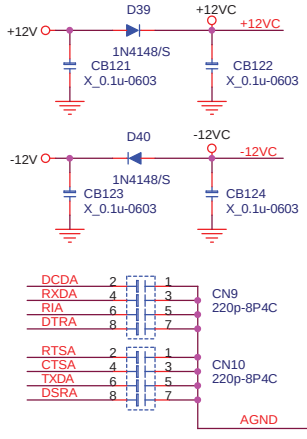


CPU FAN

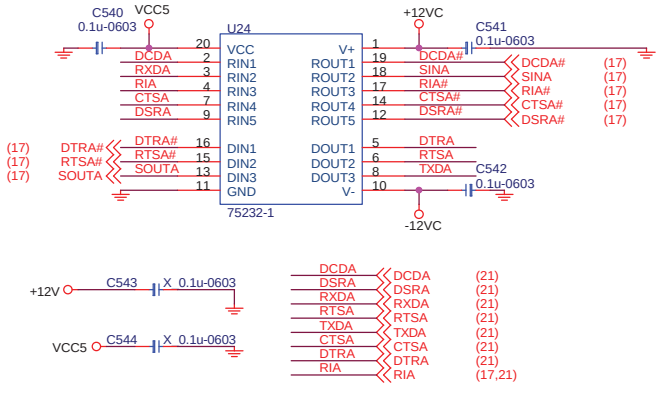


SYSTEM FAN1

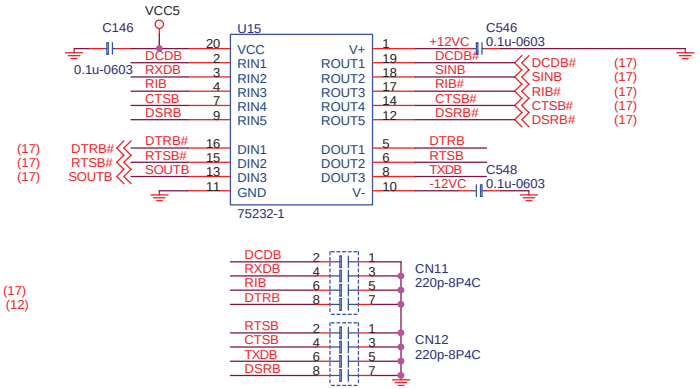




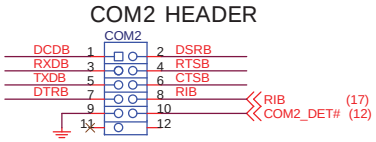
SERIAL PORT 1

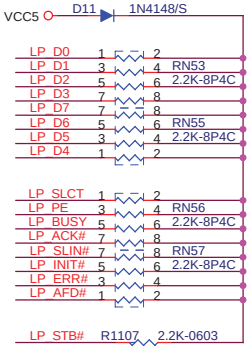


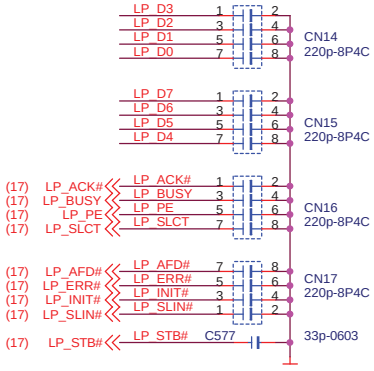
SERIAL PORT 2

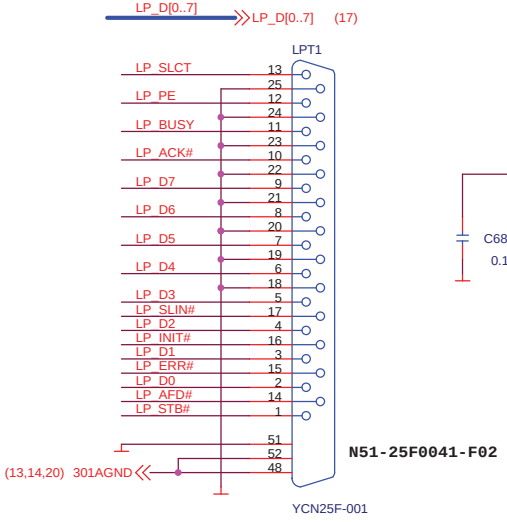


COM2 HEADER

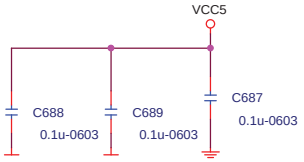


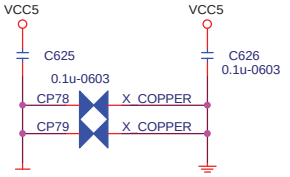






PARALLAL PORT





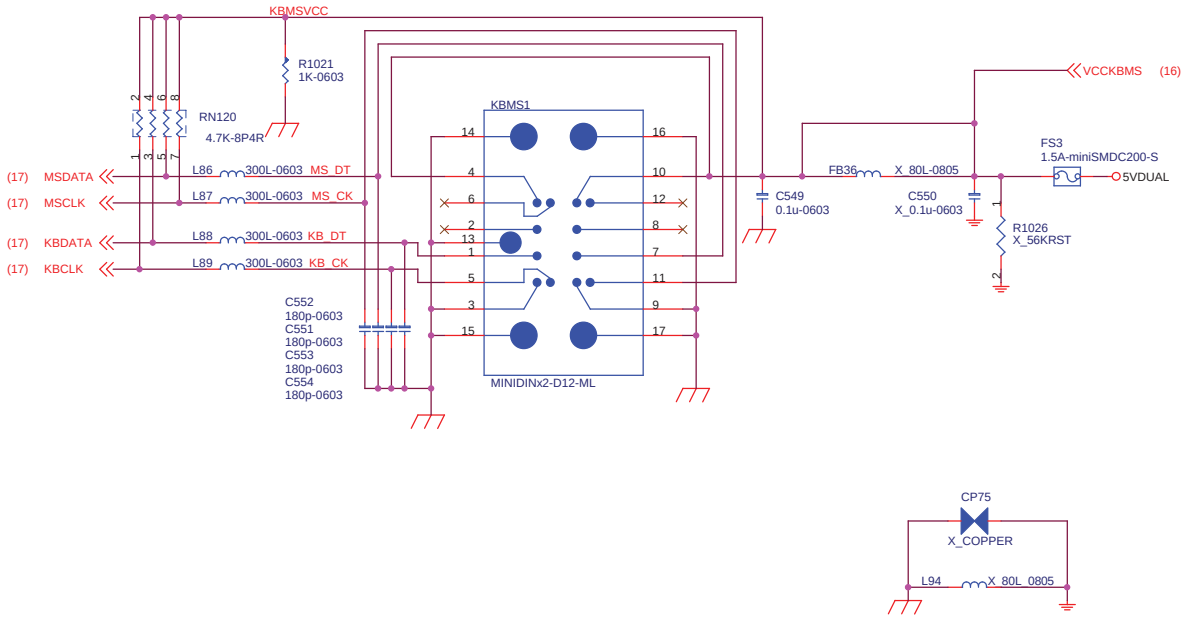
MICRO-STAR INT'L CO.,LTD.

Title: LPC I/O(W83627HF) / COM / PARALLEL/FDD

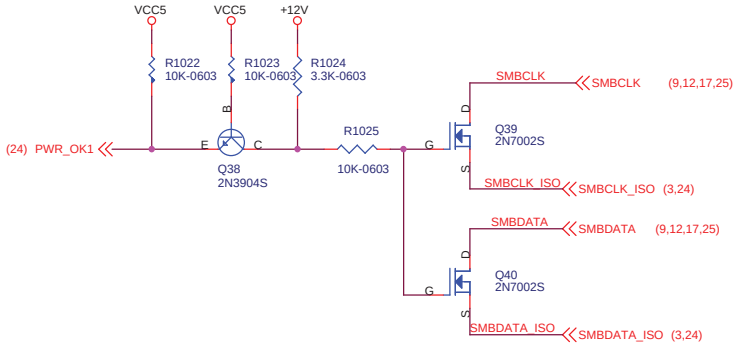
Size: Custom | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 18 of 34

PS2 KEYBOARD & MOUSE CONNECTOR

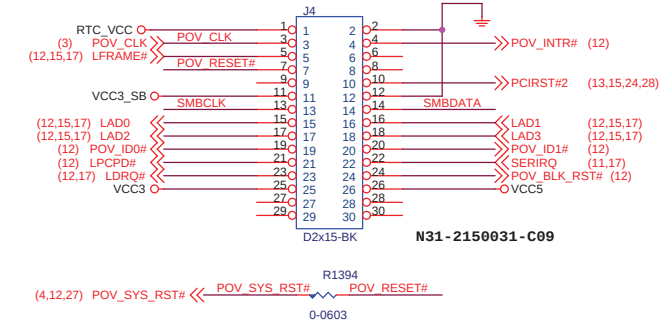


SMBus Isolation

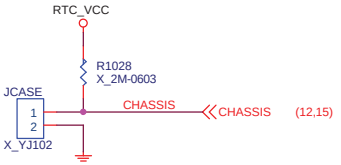


NEW ADD POV3 CONNECTOR

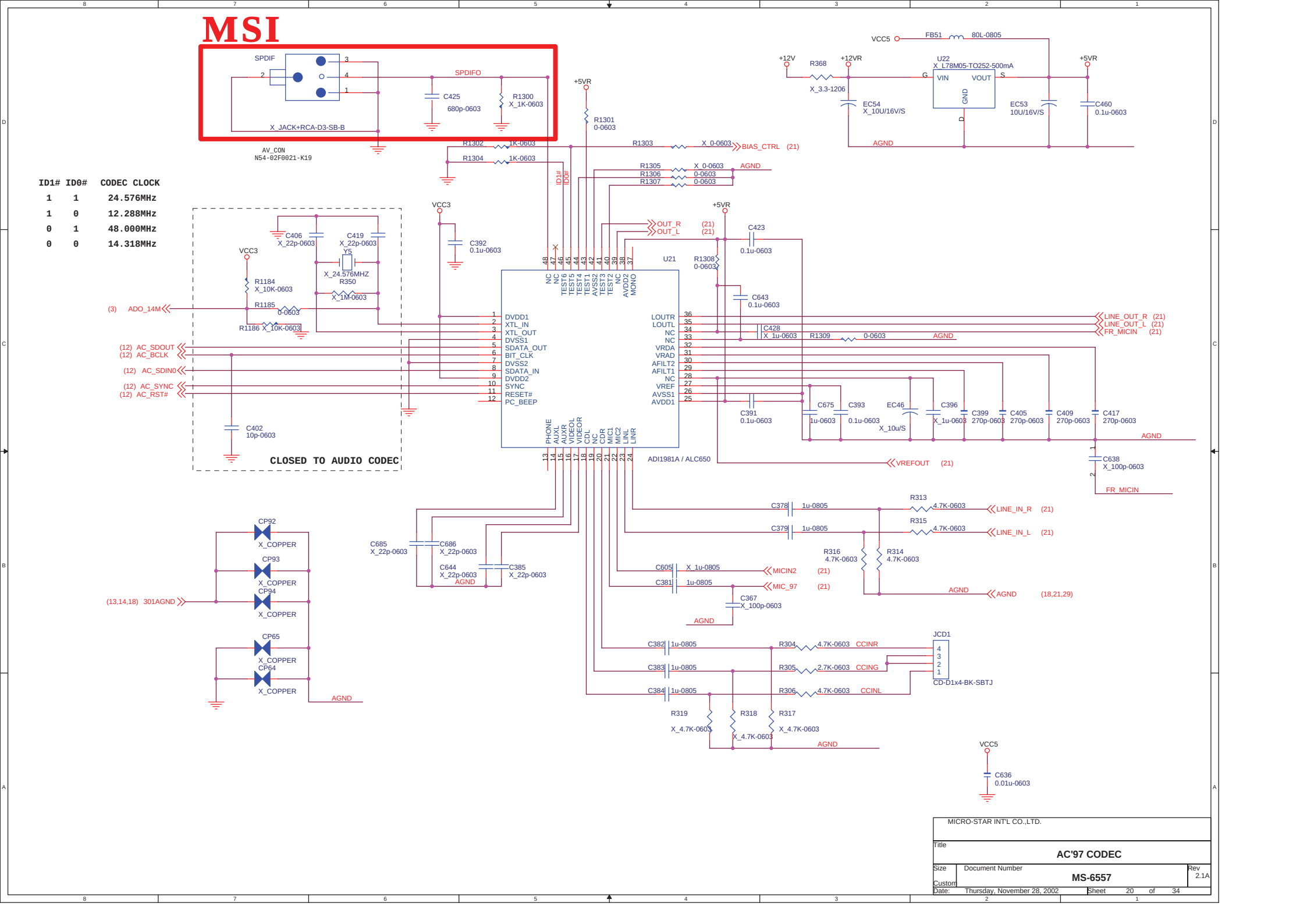
POV3 connector



Chasiss Intrusion Header



MICRO-STAR INT'L CO.,LTD.		
Title: KB/MS CONNECTOR /WAKE UP		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 19 of 34	


MSI
SPDIF
SPDIFO
C425
680p-0603
R1300
X_1K-0603
X_JACK+RCA-D3-SB-B
AV_CON
N54-02F0021-K19
+5VR
R1301
0-0603
R1302
1K-0603
R1303
X_0-0603
BIAS_CTRL (21)
R1304
1K-0603
R1305
X_0-0603
R1306
0-0603
R1307
0-0603
AGND
VCC5
FB51
80L-0805
+12V
R368
X_3.3-1206
U22
X_L78M05-TO252-500mA
VIN
VOUT
GND
EC54
X_10U/16V/S
EC53
10U/16V/S
C460
0.1u-0603
ID1#
ID0#
ID1# ID0# CODEC CLOCK
1 1 24.576MHz
1 0 12.288MHz
0 1 48.000MHz
0 0 14.318MHz
VCC3
C406
X_22p-0603
C419
X_22p-0603
Y5
X_24.576MHZ
R350
X_1M-0603
R1184
X_10K-0603
R1185
0-0603
R1186 X_10K-0603
(3) ADO_14M
C392
0.1u-0603
C402
10p-0603
CLOSED TO AUDIO CODEC
U21
ADI1981A / ALC650
DVDD1
XTL_IN
XTL_OUT
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PC_BEEP
NC
NC
TEST6
TEST5
TEST4
TEST1
AVSS2
TEST3
NC
AVDD2
MONO
PHONE
AUXL
AUXR
VIDEOL
VIDEOR
CDL
NC
CDR
MIC1
MIC2
LINL
LINR
LOUTR
LOUTL
NC
NC
VRDA
VRAD
AFILT2
AFILT1
NC
VREF
AVSS1
AVDD1
OUT_R (21)
OUT_L (21)
C423
0.1u-0603
R1308
0-0603
C643
0.1u-0603
C428
X_1u-0603
R1309
0-0603
C675
1u-0603
C393
0.1u-0603
C391
0.1u-0603
EC46
X_10u/S
C396
X_1u-0603
C399
270p-0603
C405
270p-0603
C409
270p-0603
C417
270p-0603
C638
X_100p-0603
LINE_OUT_R (21)
LINE_OUT_L (21)
FR_MICIN (21)
FR_MICIN
VREFOUT (21)
(12) AC_SDOUT
(12) AC_BCLK
(12) AC_SDIN0
(12) AC_SYNC
(12) AC_RST#
CP92
X_COPPER
CP93
X_COPPER
CP94
X_COPPER
CP65
X_COPPER
CP64
X_COPPER
(13,14,18) 301AGND
C685
X_22p-0603
C686
X_22p-0603
C644
X_22p-0603
C385
X_22p-0603
C378
1u-0805
C379
1u-0805
R313
4.7K-0603
R315
4.7K-0603
LINE_IN_R (21)
LINE_IN_L (21)
R316
4.7K-0603
R314
4.7K-0603
C605
X_1u-0805
C381
1u-0805
MICIN2 (21)
MIC_97 (21)
C367
X_100p-0603
AGND (18,21,29)
C382
1u-0805
C383
1u-0805
C384
1u-0805
R304
4.7K-0603
CCINR
R305
2.7K-0603
CCING
R306
4.7K-0603
CCINL
JCD1
CD-D1x4-BK-SBTJ
R319
X_4.7K-0603
R318
X_4.7K-0603
R317
X_4.7K-0603
C636
0.01u-0603
MICRO-STAR INT'L CO.,LTD.
Title
AC'97 CODEC
Size
Document Number
MS-6557
Rev
2.1A
Custom
Date: Thursday, November 28, 2002
Sheet 20 of 34

VALUE	AD1981A	AD1981B	ALC650
C605	NO POP	POP	POP
R1176	NO POP	POP	POP
R1187	POP	POP	NO POP
R1311	NO POP	NO POP	NO POP
R1401	NO POP	POP	NO POP
R1310	POP	POP	NO POP
R1402	POP	POP	NO POP
R1403	NO POP	NO POP	POP
R1174	NO POP	NO POP	POP
R1175	POP	POP	NO POP
R1404	POP	POP	NO POP
D60	NO POP	NO POP	POP
Q65	NO POP	NO POP	POP
R1255	NO POP	NO POP	POP
R1178	NO POP	NO POP	POP
C64	NO POP	NO POP	POP
C428	NO POP	NO POP	POP

NEAR FRONT CONN

TO FRONT AUDIO

updated circuitry

Internal Speaker

updated circuitry

updated circuitry

For ALC650

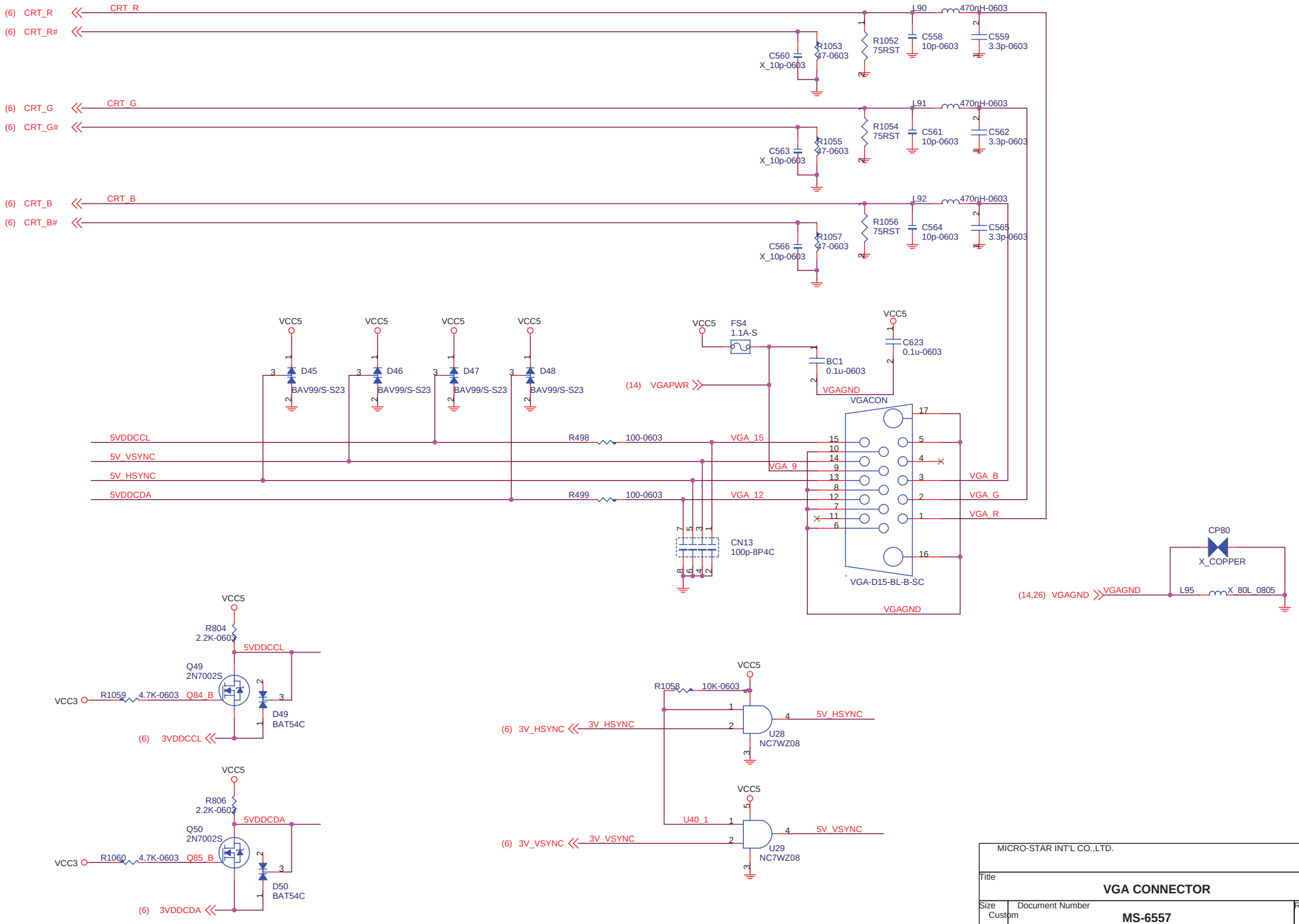
RESERVED FOR MIC BIAS (5V)

For EMI

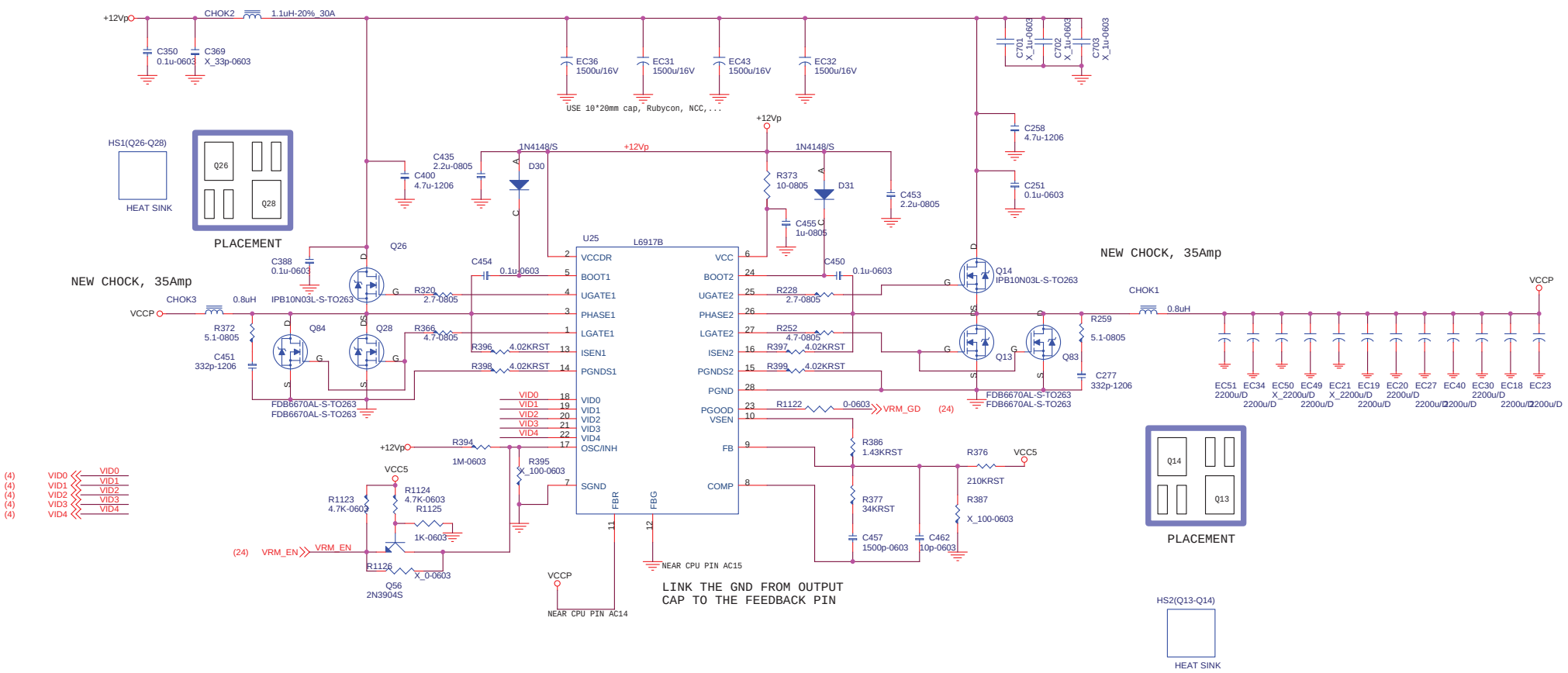
FRONT AUDIO

MICRO-STAR INT'L CO.,LTD.			
Title: AUDIO CONNECTOR			
Size: Custom	Document Number: MS-6557		Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 21 of 34		

Video Connector



MICRO-STAR INT'L CO.,LTD.		
Title	VGA CONNECTOR	
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 22 of 34	



MICRO-STAR INT'L CO.,LTD.

Title	VRM 9.0	
Size	Document Number MS-6557	Rev 2.1A
Date: Thursday, November 28, 2002	Sheet 23 of 34	

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

5VUSB USE 2 MOSFET

**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)

Q18/Q23 can use :
Philips P/N : D03-45N030B-P03 &
Niko P/N : D03-45N020B-N03

Low RDS ON MOSFET

Q31,Q29 is single source of
Niko--P3055LD :
D03-3055LDB-N03

VREF1_25 CHARGE PUMP VOLTAGE OUTPUT

Reserved

THIS PIN IS OPEN DRAIN OUTPUT

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

FOR 3VDUAL
SETTING BY SEL1

** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

Q18/Q23 can use :
Philips P/N : D03-45N030B-P03 &
Niko P/N : D03-45N020B-N03

Place these two cap at the
opposite side to EC45

Q22/Q17 can use
Niko P/N : D03-3055LSB-N03 &
Vishay P/N : D03-45N031B-V02 &
Niko P/N : D03-45N021B-N03

Power-Well Isolation Control

2.1V POWER TRANSLATOR

To DDR Clock Buffer

1.5VSBY POWER TRANSLATOR

I = 4Amp

MICRO-STAR INT'L CO.,LTD.

Title: ACPI (MS5) CONTROL

Size | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 24 of 34

B06-562EZ05-I06
Controller,LAN,INTEL/Kinnereth-R,BGA-196pin, 10/100 MBPS Ethernet Controller

B06-8254005-I06
CHIP,LAN,INTEL/82540EM,BGA-196,5V/3.3V, 10/100/1000 MBPS Gigabit Ethernet Controller

LAN KINNERETH-R/KENAI32

1.5V RAIL ONLY REQUIRED WITH KENAI CONTROLLER

FOR Kinnereth-R

FOR KENAI

2.5V RAIL ONLY REQUIRED WITH KENAI CONTROLLER. NOT CONNECTED WITH LAVON

KENAI/KINNERETH VCC3.3VDECOUPLING CAPS

updated circuitry

FOR KENAI32 pull down 3.3K.

FOR IEEE jitter testing

R1321=549 ohm for KINNERETH, 2.49K ohm for KENAI.

R1322= 619 ohm 1% for Kinnereth-R ,KENAI no mount

TCK= "1" to Disable Kinnerth LAN

Company	MICRO-STAR INT'L CO., LTD.
Title	LAN CONTROLLER
Size	Document Number: MS-6557
Rev	2.1A
Date	Thursday, November 28, 2002
Sheet	25 of 34

L05-0500080-P21

U43

H5007/X_H1267

FOR KENAI

FOR KENAI.

FOR KENAI

FOR KENAI/KINNERETH-R

R1344/R1345 49.9 ohm FOR KENAI.

STUFF 60.4 ohm FOR Kinnereth-R

Reserved larger plane.

LAN_GND is a separated GND below connector and transformer.

MSI new part number = N58-20F0041-A10

AMP part number 1277852-4

LEFT 1G=AMBER 100=GREEN

RIGHT ACTIVE =YELLOW

Dual LED pin definition

17 Green Amber 18

N58-20F0091-A10

7/9 modify

FOR KENAI.

Q79 Philips BCP69-16 only.

INSTALL POWER TRANSISTOR Q79 & Q80 AND SUPPORT COMPONENTS ONLY WHEN USING KENAI32 CONTROLLER

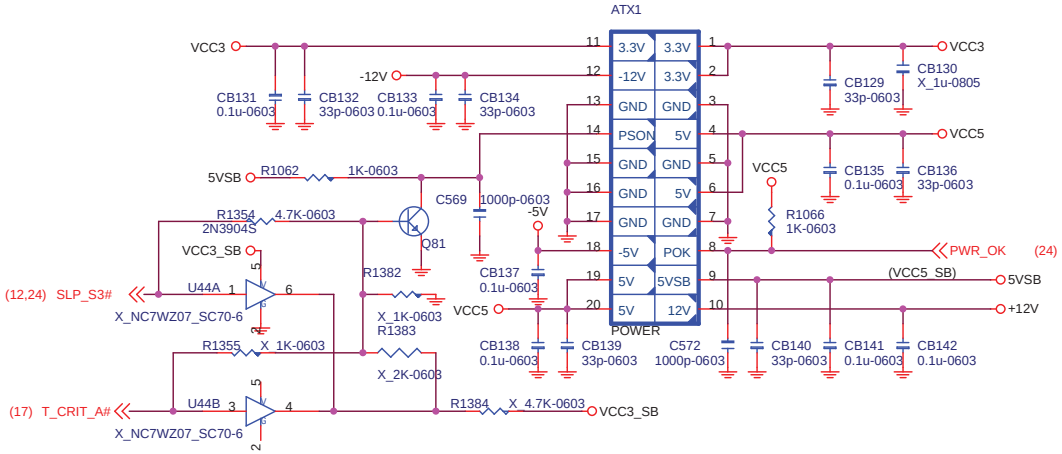
THESE THREE CAPACITORS ACROSS THE CHASSIS GND TO GND SPLIT, ARE LOCATED ABOVE THE MAGNETICS MODULE. PLACE AS CLOSE AS POSSIBLE TO THE MAGNETICS MODULE.

LAN Crystal

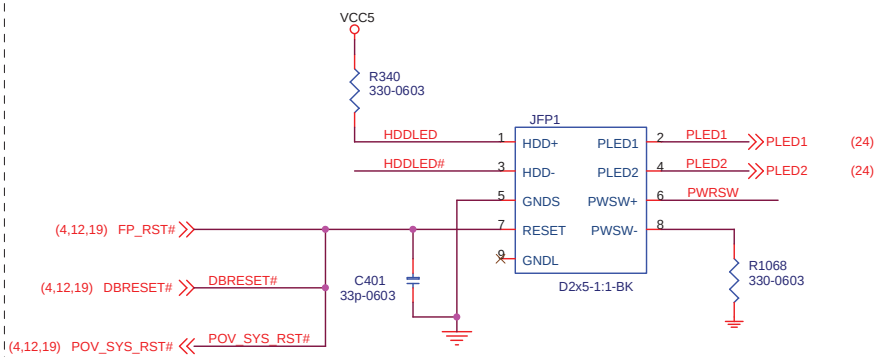
THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.

<OrgAddr1>	MICRO-STAR INT'L CO., LTD.
Title	LAN CONTROLLER
Size	Document Number: MS-6557
Rev	2.1A
Date:	Thursday, November 28, 2002
Sheet	26 of 34

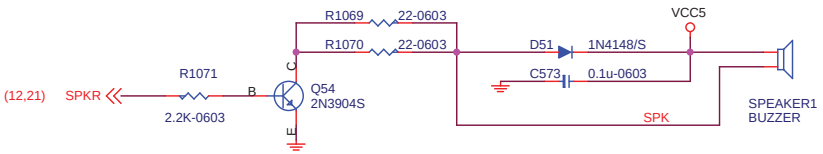
ATX CONNECTOR



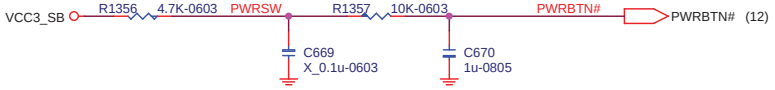
POWER BUTTON



SPEAKER



POWER BUTTON



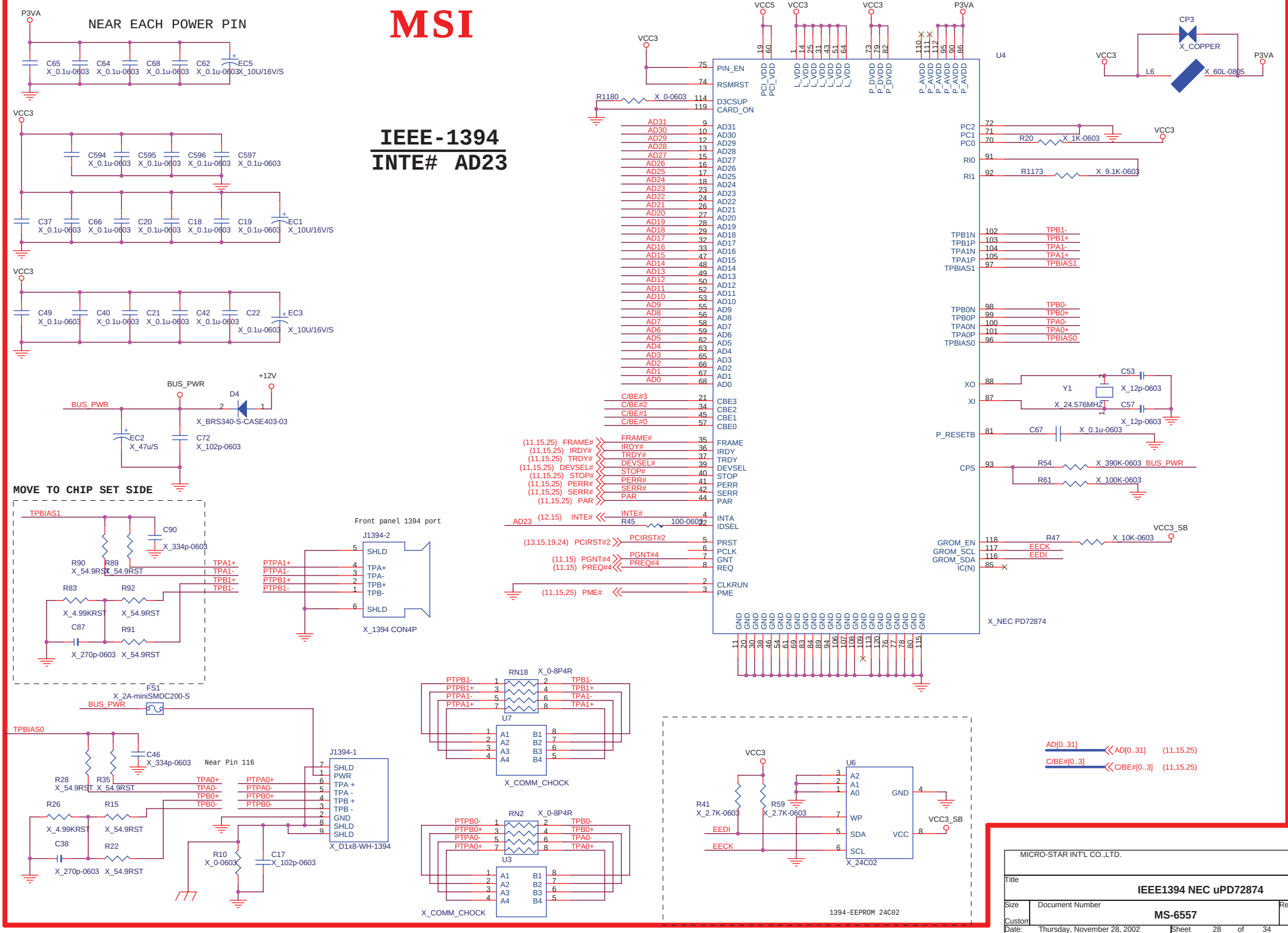
MICRO-STAR INT'L CO.,LTD.		
Title: ATX Power Conn. & VGA Conn.		
Size: B	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 27 of 34	

MSI

IEEE-1394
INTE# AD23

NEAR EACH POWER PIN

MOVE TO CHIP SET SIDE



PCB OTHER COMPONENT

BS1_X1 BS2_X1 BS3_X1 BS4_X1 BS5_X1

MH2 MH3 MH1 MH4

94GND AGND (18,20,21)

J2 X_PIN1*2 CPU

J1 VCC5 X_PIN1*2 AGP

System Decoupling Capacitors

+12V: EC11 10U/16V/S, C99 0.1u-0603, C43 0.1u-0603

VCC5: EC13 10U/16V/S, C117 0.1u-0603, C456 0.1u-0603, C13 0.1u-0603, C464 0.1u-0603

5VSB: C323 0.1u-0603, C373 0.1u-0603

-12V: EC8 10U/16V/S, C123 0.1u-0603, C125 0.1u-0603

VCC3: EC10 10U/16V/S, C162 0.1u-0603, C205 0.1u-0603, C189 0.1u-0603, C274 0.1u-0603, C246 0.1u-0603

VCC3_SB: C39 0.1u-0603, C28 0.1u-0603

VCC3: C70 0.1u-0603, C253 0.1u-0603, C71 0.1u-0603

VCC_AGP: C610 X_0.1u-0603, VCCP; VCC5: C611 0.1u-0603, VCCP

VCC5: C613 0.1u-0603, C614 0.1u-0603, C615 0.1u-0603, C616 0.1u-0603, C617 0.1u-0603, VCC3

NB SOLD SIDE

HUB LINK GND & VCC_AGP

VCC_AGP: C618 X_0.1u-0603, C619 X_0.1u-0603, C620 X_0.1u-0603

VCC_AGP MEM_STR: C621 X_0.1u-0603, C622 X_0.1u-0603, VCCP

High Freq. return current decoupling

VCC5 C342 1000p-0603 VCC3

C44 1000p-0603

MF5 MF12 MF2 MF8

MF4 MF13 MF3 MF9

MF7 MF11 MF1 MF10

MF6 MF14

sponge1 Sponge

Barcode1 Barcode

PCB1 6557 2.1A

FM9 FM3 FM1 FM2 FM4 FM7 FM5 FM6 FM8

At solder side

MICRO-STAR INT'L CO.,LTD.

Title: DECOUPLING CAPACITOR

Size: B | Document Number: MS-6557 | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 29 of 34

	PIN NAME	POWER WELL	USAGE	DURING RESET	S3/ S4/S5	NOTES
ICH4	GPI0	CORE	PD_DET			DETECT CABLE TYPE ATTACHED TO PRIMARY IDE CONNECTOR
	GPI1	CORE	SD_DET			DETECT CABLE TYPE ATTACHED TO SECONDARY IDE CONNECTOR
	GPI2	CORE	INTE#			
	GPI3	CORE	INTF#			
	GPI4	CORE	INTG#			
	GPI5	CORE	INTH#			
	GPI6	CORE	POV_ID0#			FOR POV3 connector POV_ID0#
	GPI7	CORE	POV_ID1#			FOR POV3 connector POV_ID1#
	GPI8	RESUME	SIO_PME#			FROM SIO
	GPI11	RESUME	LM86_THERM_N			FROM LM86
	GPI12	RESUME	NONE			PULLDOWN WITH 10K OHM RESISTOR
	GPI13	RESUME	NONE			PULLUP
	GPO16	CORE	UNUSED	HIGH	OFF	
	GPO17	CORE	UNUSED	HIGH	OFF	
	GPO18	CORE	UNUSED	HIGH	OFF	
	GPO19	CORE	UNUSED	HIGH	OFF	
	GPO20	CORE	C2_BLK_RESET#	HIGH	OFF	CONNECT TO FLASH WRITE-PROTECT LATCH
	GPO21	CORE	C2_BLK_SET#	HIGH	OFF	CONNECT TO FLASH WRITE-PROTECT LATCH
	GPO22	CORE	NONE	HIGH-Z	OFF	CONNECT TO ONE END OF NOPOPED RESISTOR
	GPO23	CORE	NONE	LOW	OFF	CONNECT TO ONE END OF NOPOPED RESISTOR
	GPO24	RESUME	GPI24	LOW	DEFINED	For HSMI# , Second signal for BIOS
	GPO25	RESUME	ENET_DIS	HIGH	DEFINED	HARDWARE CONTROL OF 10/100 OR GbE DEVICE
	GPO27	RESUME	POV_BLK_RST#	HIGH	DEFINED	FOR POV3 connector POV_BLACK_RESET#
	GPO28	RESUME	GPI28	HIGH	DEFINED	Power LED from MS5 , The GPIO pull up .
	GPI32	CORE	GPI32	HIGH	OFF	ATTACHTO PIN 2 OF 3-PIN HEADER AND PULL UP. PIN 3 IS GND / CLEAR_CMOS#
	GPI33	CORE	NONE	HIGH	OFF	NO CONNECT
	GPI34	CORE	NONE	HIGH	OFF	NO CONNECT
	GPI35	CORE	COM2_DET#	HIGH	OFF	LOW(ASSERTED) IF 2ND SERIAL PORT CABLE IS INSTALLED
	GPI36	CORE	GPI36	HIGH	OFF	PULLUP
	GPI37	CORE	GPI37	HIGH	OFF	PULLUP
	GPI38	CORE	GPI38	HIGH	OFF	PULLUP
	GPI39	CORE	GPI39	HIGH	OFF	PULLUP
	GPI40	CORE	GPI40	HIGH	OFF	PULLUP
	GPIO41	CORE	UNUSED	HIGH	OFF	
	GPIO42	CORE	UNUSED	HIGH	OFF	
	GPIO43	CORE	UNUSED	HIGH	OFF	
	RI*	RESUME	RING#			FOR COM PORT RING WALK UP
	THERM*	CORE	THRM#			
FWH	GPI0		PERS0	INPUT	DEFINED	Jedda - Pull-Down
	GPI1		PERS1	INPUT	DEFINED	Jedda - PULLUP
	GPI2		PERS2	INPUT	DEFINED	Jedda - Pull-Down
	GPI3		PERS3	INPUT	DEFINED	Jedda - Pull-Down
	GPI4		PERS4	INPUT	DEFINED	Pull-Up if 10/100 ethernet,pulldown if gigabit ethernet.
SIO	GP10		SIO_LOCK_SET#	INPUT	DEFINED	CONNECT TO SIO DDRC CONTROL LATCH
	GP27		IO_SMI#	INPUT	DEFINED	USED FOR IO_SMI# FUNCTION,CONNECT TO SYSTEM SMI SIGNAL
	GP30		CPU_FAN1	INPUT	DEFINED	USED FOR FAN TACH1 FUNCTION,CONNECT TO CPU FAN TACH
	GP31		SYS_FAN1	INPUT	DEFINED	USED FOR FAN TACH2 FUNCTION,CONNECT TO REAR FAN TACH
	GP32		PWM_CPU	OUTPUT	DEFINED	USED FOR FAN1 PWM FUNCTION,CONNECT TO FAN CONTROL
	GP33		PWM_SYS	OUTPUT	DEFINED	USED FOR FAN2 PWM FUNCTION,CONNECT TO FAN CONTROL
	GP42		SIO_PME#	INPUT	DEFINED	USED FOR IO_PME# FUNCTION,CONNECT TO ICH GPI8
	GP43		DDRC_LOCK_DIS	INPUT	DEFINED	USED FOR DDRC FUNCTION,CONNECT TO DDRC LATCH

PCI DEVICE ROUTING TABLE

DEVICE	INT pin	REQ/GNT	IDSEL
VGA	INTA#		
PCI SLOT	INTB# INTC# INTD# INTA#	0 1	AD17
1394	INTE#	4	AD23
LAN	INTA#	3	AD27

PCI RISER

DEVICE	INT pin	REQ/GNT	IDSEL
PCI #1	INTB# INTC# INTD# INTA#	0	AD17
PCI #2	INTC# INTD# INTA# INTB#	1	AD18

MICRO-STAR INT'L CO.,LTD.

Title: **GPIO SETTING**

Size: Custom | Document Number: **MS-6557** | Rev: 2.1A

Date: Thursday, November 28, 2002 | Sheet 30 of 34

MS-6557 2.0 (Modify from MS-6557 1.0)

PAGE	Description
	05/24/2002
	Modify from MS6557 1.0 , Change specifications for customer
	05/25/2002
	Modify from MS6557 2.0 , Change specifications for customer and delete OPTION A (MSI SPEC).
Page-03:	For Customer request PCI slot clock definition
	1. R822 link to LAN_PCLK 2. R823 link to PCICLK1 3. R1363 link to PCICLK2
	4. RN76 link to FWH_PCLK , ICH_PCLK , SIO_PCLK
	5. R824 link to CARD_CLK , R824 not mount (OPTION A)
	6. R825 link to 1394_PCLK , R825 not mount (OPTION A)
	7. R826 link to MS_CLK , R826 not mount (OPTION A)
	8. R832 not mount (OPTION A)
	9. OPTION A block not mount all parts.
	10. New add R1358 link to ICH14 , R1359 link to SIO_14,R1374 link to ADO_14M
	11. CN3 and CN4 swap for layout.
	12. C482 net name error ,change to SIO_14
	13. Not mount C485,C486,C627
Page-06:	1. Delete R864 ,Pin AJ31 directly to PCIRST#1
	2. Delete 3VDDCDA and 3VDDCCL link point , it's circuit error.
Page-11:	1. Delete R923,R925,R928,R930,R932,R933,R934,R936
	2. Delete PD_DET and SD_DET pull down resistors R929 and R931.
Page-12:	1. Delete R1041 for GPIO8 , It's link to SIO_PME#
Page-13:	1. Delet U30 and R1101.
	2. Delete RN127, Add R1361 for DDCDATA and R1362 for DDCCLK
	3. Delete EC37 for layout.
Page-14:	1. OPTION A block not mount all parts
Page-17:	1. Delete CB149
	2. Delete R1298 , U38 pin 17 directly link SIO_PME#
	3. Change U39 part name from CY2305sc-1H to LM86
Page-20:	Mount ADI1981A update parts
	1. Not mount: C406 C419 Y5 R350 R1303 R1305 C428 C396 R1187
	2 Mount: R1185 R1302 R1304 R1301 R1306 R1307 R1308 C643
	3. Delete C418
Page-21:	Mount ADI1981A update parts
	1. Mount : R355 R354 R1175 C624
	2. Not mount: R1255 R1178 C640 Q65 R1174 D60
	3. New add R1375 R1376 but not mount
	4. Delete C433 C432
	5. Change parts value : C404 C397 C398 C420 from 180 pf to 1000pf
	6. Change parts value : R1176 from 4.7k to 2.2k
	7. Circuit modify: R1311 directly link to +5VR
	05/26/2002 ***Page 25 26 LAN circuit review and modify***
Page-25 26 :	For Kenai 32
	1. Mount : RN130 R1312 R1328 RN131
	2. Not mount : R1326 R1332 R1322 R1316
	3. Change part value : R1321=2.49K1% U41=512KX8
Page-28 :	1. OPTION A block not mount all parts.
Page-29 :	1. OPTION A block not mount all parts.
Page-30 :	1. OPTION A block not mount all parts.
Page-31 :	1. OPTION A block not mount all parts.

PAGE	Description
	05/27/2002
	Follow common BIOS Hardware Definition of customer
Page-15:	1. Will PCI slot 1 INT# change to INT#F INT#G INT#H INT#E.
	2. Will PCI slot 1 IDESL change to AD25
	3. Will PCI slot 1 REQ/GNT change to 4 and riser card slot 2 change to 0
	4. Add R1364 R1365 R1366 for customer requeet , they are select project ID , Jedda it's 0010 ,so mount R1364 R1288 R991 R992 , not mount R1287 R1365 R1366 R1289
	4. Delete U37 FWH SMT socket.
Page-17:	1. Will FAN control PWM separated to PWM_CPU and PWM_SYS for customer request.
	MSI modify
Page-18 :	1. Layout request : swap CN14 CN15 CN17 RN53 RN55 RN57.
Page-22 :	1. Delete R1253 and R1254
Page-28 :	1. Change PCMCIA IDSEL to 24 and REQ/GNT to 2
Page-31 :	1. Change IEEE1394 REQ/GNT to 1
Page-33 :	1. Change PCI Device Routing Table:
	05/29/2002
Page-12:	Follow customer request will GPI34 pull down , new add R1377 10Kohm .
Page-26:	Follow INTEL TA-147 Version 1 notes , add R1360 30K resistor from the base to the collector of Q79.
	05/30/2002
	For customer feback email circuit issues on 5/30
Page-25 26 :	For Kenai 32
	1. Will LILED# connect to the cathode of a yellow Led on the RJ-45 connector
	2. Will ACTLED# connect to a 330 ohm resistor , then to the anode of a yellow Led on the RJ-45 connector
	3. Will 100_LED# connect to a 330 ohm resistor , then to a green/amber Led on the RJ-45 connector
	4. Will 1000_LED# connect to the a green/amber Led on the RJ-45 connector
	5. R529 and r525 not mount
	6. Will R1314 connector a 10Kohm pull up resistor from pin4 of U41 to VCC3_SB
	7. Connect pin 6 of U41 to VCC3_SB
	8. Pin M8 should be connector to a 2 pin header connector for IEEEjitter testing.
	9. Delete R1349 and R1350
	10. Delete R1327 R1330 U42 ,will AD27 directly to IDSEL.
	11. R1331 change to 10K and connected to VCC3_SB
	12. Delete R1351 and R1352 ,will X1_KENAI and X2_KENAI connected directly to the crysatl.
	13. Add LAN power good circuit , not mount R1323 , add R1368 R1369 R1370 Q82 C674
	14. Change value R1328 from 0 ohm to 10Kohm
	15. Delete R1325
	16. Add VCC3_SB cap , CB169 CB170 CB171 CB172
	17. Add VCCL1.5 bypass cap : CT20 CB165 CB166 CB167 CB168
	18. Add VCCL2.5 bypass cap : CB173 CB174 CB175
	19. Change C648 value FROM 0.01uF TO 1500pf
	20 . Change R1343 value from 1ohmTO 2ohm,and add another 2 ohm 1206 package resistor in parallel with R1343
	21. Not mount R1346

Title	HISTORY	
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 31 of 34	

MS-6557 2.0 (Modify from MS-6557 1.0)

PAGE	Description
	05/31/2002
Page-25:	1. For Layout swap RN132.
	2. Delete CB172 ,CT18 CT19
	3. Mark RN132 for KENAI32.
Page-26:	1. For Layout delete C665 C655
Page-27:	1. New add U44 for SLP_S3# and T_CRIT_A# control power on function.
	2. Delete R1063 C571 C570, change JFP1 pin 8 signal not PWRSW, change R1068 from 10K ohm TO 330ohm
	06/02/2002 Follow common BIOS Hardware Definition of customer
Page-15:	1. Will PCI slot 1 INT# change to INT#B INT#C INT#D INT#A.
	2. Will PCI slot 1 IDESL change to AD17
	3. Will PCI slot 1 REQ/GNT change to 0 and riser card slot 2 change to 1
Page-31 :	1. Change IEEE1394 REQ/GNT to 4
	06/03/2002
Page-26 :	1. R529 change connect to USB1B pin19
MS-6557 2.0A	***06/10/2002***
Page-3:	1. R812 R813 and R807 change connect to VDDA3V
Page-12 :	1.will INTRUDER# signal connector to page 19 CHASSIS signal and not mount R1028
Page-21 :	1.Delete CP66 for audio precision.
Page-25 :	1.Will ENET_DIS signal connect to ICH4 ENET_DIS.
Page-27 :	1.Not mount R1382 , R1383 R1384,R1355 and U44 , MOUNT R1354
	06/12/2002
Page-25 26 :	For Kinnereth-R
	1.Mount RN130 R1315
	2.Not mount Q80 R1353 C667 CB163 C673 CB164
	3.Change U9 from L05-0100020-B09 to L05-0100040-B09
	4. U9 pin 10 pin15 NC not connect anything.
Page-25:	For Kenai -32
	1.not mount RN130
Page-20:	1.pop C425 is 680pf for EMC solution.
Customer change request 06/21/2002	
Page-3 :	1. Mount U35 C642 C671 R1182 R837 R1259 to provide 14Mhz clock.
	2. Not mount R1358 R1359 R1374
	3. Add R1386 R1388 R1385 R1387 for ITP clock.
Page-4 :	1. Connect ITPCLK ,ITPCLK#,DBRESET# to CPU skt to support ITP
Page-20:	1.For cost down ,no mount Jaux1 JMD1 C365 C366 C386 C422 R294 R295 R301 R362
	2. Change U22 parts to 78M05 package is TO252 , no mount U22 EC54 R368
	3. Add FB51 for audio power use filtered digital 5V instead
	4. change EC44 from 10uF to 1uF.
	5. Change C399 C405 C409 and C417 to 270pf X7R
	6. Change R304 R306 to 4.7K,R305 to 2.7K, R313 R314 R315 R316 to 4.7K and pop.
Page-21:	1.Change EC48 and EC52 from 10uF to 100uF
	2. Change R351 and R352 from 75 Ohm to 0Ohm.
	3. New add function : rear audio output port should be disable when front headphone port is plugged.
Page-25 26:	1. The polarity of the green LED that connects LILED# and ACTLED# is reversed.
	2. Add R1389 R1390 for SMbus siganl isolation purposes.
	3. Will R525 connected to 1000LED# and should be pop'd for Kinnereth-R design.
	4. Will R1371 moved from 100LED# to the 1000LED# line , pop only for KENAI32
	5.C645 should be 0.01uF.
	6. De-pop R1324 for Kinnereth-R and KENAI-32

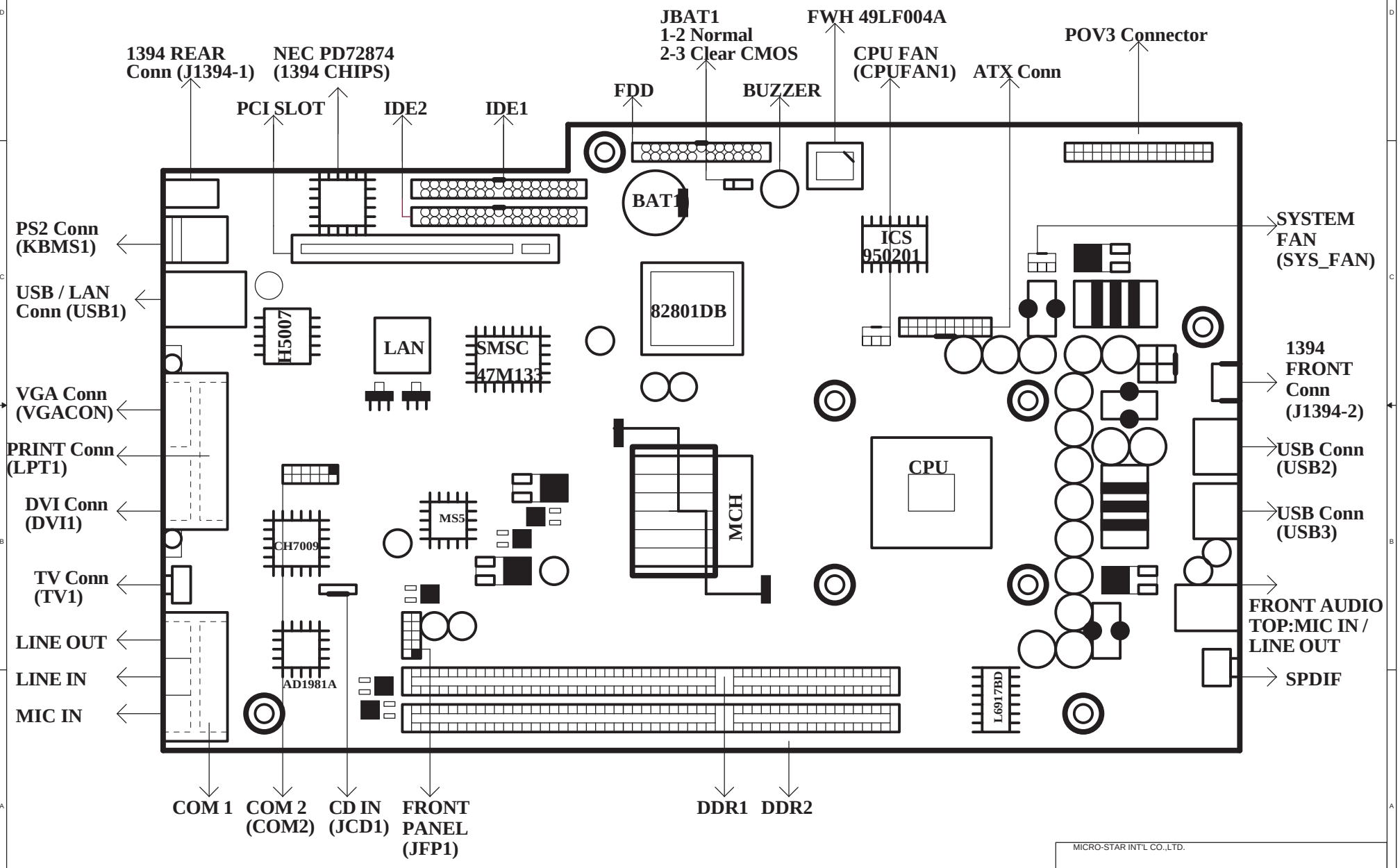
	Customer change request 06/26/2002
Page-3:	New add POV3 connector.CLK-gen circuit modify.
	1. New POV3 connector , will U34 PIN 10 for POV_CLK, throuth R824 and link to CN3 PIN 5
	2. U34 and RN76 pin out renew link .
Page-12:	1. will U8 pin AB3 link to POV3 for LPCPD# and R1114
	2. U8 pin R2 link to POV_ID0# and R972
	3. U8 pin W1 link to POV_BLK_RST# AND R1269
	4. U8 pin R3 link to POV_ID1# and R974
	5. Add R1392 and R1393 for chassis intruder and POV_INTR# to connector.
Page-15:	1. modify FWH Write protect circuit by Customer circuit.
Page-17:	1. modify FDD Write protect latch circuit by Customer circuit.
	2. Add R1395 for LM86 T_CRIT_A# isolation purposes.
Page-19:	New add POV3 connector.
Page-27:	will FP_RST# DBRESET# and POV_SYS_RST# connect together.
Page-30:	GPIO setting :
	1. GPI6 for POV_ID0# GPI7 for POV_ID1# GPI27 for POV_BLK_RST#
	Change SPEC 06/28/2002
	Delete PCMCIA and MEMORY STICK circuit and NOT support DVI functions.
Page-3:	1. Delete C483 and CN3 pin 1 not connect.
	2. Will POV_CLK resistor change to R824
	3. Will R826 link to REF_14
Page-7:	1. Not mount R1075 R1076 R1077 R1078 R1079 R1081 R1082 R1091R1080.
Page-12:	1.Modify U8 pin W3 and R1274 from CARD_RI# to GPI13
Page-13:	all parts not mount for SPEC. BUT R1102 R1103 AND C294 need mount for 845G.
Page-14:	all parts not mount for SPEC.
Page-24:	Change R245 from 200Ohm to 150 Ohm. will AGP1 change to 2.1V
Page-27:	Delete R1072 for new SPEC
Page-28 29 30:	Delete page.
Page-33:	GPIO SETTING
	1. Delete PCMCIA routing table.
	2. GPI13 not connect
	Circuit modify 07/02/2002
Page-3:	1. change parts valus R849 R850 to 10K, C487 and C489 no-pop.
Page-11:	1.delete signal FINIT# change to HINIT#
Page-12:	1. Change D38 from BAT54A to 1n5817/S,will VBAT signal change to RTC_VCC
Page-15:	1.change signal FINIT# to HINIT# , and R1117 no-pop
Page-17:	1.add C678 for temperature sensor issue.
	Circuit modify 07/09/2002
Page-3:	1. change parts valus C478 C481 to 22p
	2. Layout request swap PCI-clock signals (delete R822 R823 R1363 R824 R825 add RN135 , swap CN3 CN4 pin)
Page-4:	1. add VCC_VID circuit for layout issue. (add R1397 R1398R1399 R1400 VR1)
Page-12:	1.Follow ADV team change SLP_S5# to SLP_S4# , control MS5 suspend status .
Page-20 :	delete R400 R312 for MIC
Page-21 :	1.Change rear/front audio MIC circuit for codec vendor
	2.add pop/no-pop table for codec.
Page-22:	1.change L90 L91 L92 from 120 L to 0.082uH,C558 C561 C564 from 3.3p TO 10pF for video signal quality issue.

Title	HISTORY	
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 32 of 34	

PAGE	Description
Page-23:	1.Each phas add low side mosfet ,add Q83 Q84.
	2.Change R252 R366 from 2.7Ohm to 0Ohm
	3.Change EC36 EC31 EC32 EC43 Pcb footprint for layout.
	4. no-pop EC50 EC21 for cost down
Page-24:	1.MS5 VCC_VID no link to cpu.
	2.U20 pin 38 signal change from SLP_S5# to SLP_S4# for ACPI issue(S4 memory power off)
Page-25:	1. Add R1405 for ENET_DIS signal pull down.
	2.no-pop R1318 for customer request
	2.Delete R1316 for customer request.
Page-26:	1. Swap signal for U43 and delete U9.
	2.Add C691 for EMI solution
	3. add R1337 and R1396 for 10/100 LAN.
	4. delete C658 , add R1406 0ohm for EMC solution
MS-6557 2.0B 07/27/2002	
Page-3:	1. Change R849,R850 from 15K to 10K, del C487,C489 for IDE control signal.
	2. Change C478,C481 from 10P to 22P for crystal accuracy of clock generator.
Page-5:	1. Add 10uF on C296,C346 for 33MHz harmonic.
Page-12:	1. Change CB112 to 0.1u/X7R for RTCRST reliability.
	2. Add 4.7K on R976 for IDE autoreset issue.
Page-18:	1. Change the placement of sys fan connector and related component.
	2. Reserve C693 for EMI reducing.
Page-21:	1. Add four bridges CP95,CP96,CP97,CP98 and two reserved capacitors C694,C695 between audio GND and system GND.
Page-23:	1. Change R252,R366 of PWM power mosfet gate pin resistor from 2.7ohm to 0 Ohm.
Page-25:	1. Del CB168,CB156 for 25MHz.
Page-26:	1. Change C650 to 330PF for 25MHz harmonic.
	2. Add 0.1uF on C651,C652,CB163 and 0.01uF on C673 for 25MHz harmonic.
Page-27:	1.Add 33pF on C401 for 33 MHz.
MS-6557 2.0C 08/8/2002	
Page-12:	1.Add 0.1uF on CB176 to reduce noise on signal of rear USB over current protection.
Page-16:	1.Replace CP69,70,71 with wide trace.
Page-17:	1.Change LM86 power well from 3Vstandby to Vcc3 and add C696 for bypass capacitor
Page-19:	1.Change the part number of FS3 to reach 1.5A specification.
Page-20:	1.Replace R341,R338 by trace for cost down purpose, add 0 ohm on R1309.
Page-21:	1.Add R1411,R1412 del CP96 change R339,R348 from 75 to 22 ohm for reducing audio noise.
	2.Move the placement of C684 to audio connector side.
Page-22:	1.Change L90,91,92 from 0.082uH to 0.047uH, change C558,C561,C564 from 10P to 3.3P,C562,C565,C559 from 10P to 15P for EMI issue.
Page-23:	1.Change R252,R366 of PWM power mosfet gate pin resistor from 0 ohm to 2.7 Ohm.
	2.Change part number of HS1,HS2.
Page-24:	1.Del R1242,R1243,R1244,R1245,R1249,R1248,R1250,C637,Q70,Q72,Q69,Q71 add R1247 for resume reset circuitry to prevent low temperature power on fail.
	2.Reserve C697 to reduce noise on MSVC_VID.
Page-25:	1.Del reserved R1368, R1369,C674,R1370,Q82.
Page-26:	1.Change the part number of C648 to reach high voltage specification.
	2.Add 470pF on C691.
	3.Change USB1 to correct part number for IBM LED light requirement.
Page-27:	1.Change R1069,1070 from 220 to 22 ohm.
	2.Del useless R1384.
MS-6557 2.0C 08/13/2002	
Page-20:	1.Pop R1309 for AD1981A's REFERENCE CIRCUIT.
Page-21:	1. Delete CP95 CP97 CP98 for audio perciation
Page-23:	1.Change R252,R366 of PWM power mosfet gate pin resistor from 2.7 ohm to 4.7 Ohm.
MS-6557 2.0C 08/22/2002	
Page-23:	1. change HS1 HS2 heat sink for DFM request.
Page 26:	1.Change USB1 to correct part number for IBM LED light requirement.
MS-6557 2.0C 08/27/2002	
Page 15:	1.U37 no-pop FWH socket , delete PLCC32-SMT socket.
Change parts vendor , CT1,EC48,EC52 for factory production	
MS-6557 2.0C 08/30/2002	
Page 21:	1.Add C694 , C695, FB53 to 1uF for front audio noise,EMI issues.
Page 22:	1.C565, C562, C559 change to 3.3pF for video noise ,EMI issues.
	2.C558, C561, C564 change to 10 pF for video noise ,EMI issues.
Page 21:	1.change R339,R348 from 22Ohm to 10 Ohm for customer requset .
	2. No-pop R1402 for customer request
	3. change R1310,R1176 from 2.2kOhm to 2.4kOhm for customer request
MS-6557 2.1 11/4/2002	
Page 11:	1.Change R922 from 62 ohm to 330 ohm.
Page 17:	1.Reserve R1425 for GP17/20 pull up resistor.
	2. LM86's T-CRIT wire or with CPU's thermal trip and LM86 use 3V_stby power well
Page 18:	1.Reserve R1415,R1416,R1418,R1417,Q86 and Q87 for fan automatic turn on function.
Page21:	1.Add R1419,R1420,R1421,R1423,R1422,R1424,C708,C709,C710,C711,C714,C713,CT21,U41 and CON1 for internal speaker function.
	2.Reserve C715,C716 for EMI concern.
	3.Change FB53 from 1uF/0805 to 0.1uF/0603.
Page 25:	1.Reserve R1413 and add U46,R1414 for gigabit lan disable function.

Title	HISTORY	
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 33 of 34	

MS6557 2.0C Jumper Diagram



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Title: System Block Diagram		
Size: Custom	Document Number: MS-6557	Rev: 2.1A
Date: Thursday, November 28, 2002	Sheet 34 of 34	