MS-6555

Version 40a FSB533

INTEL (R) Brookdale - GV Chipset

Northwood / Presott 478pin mPGA-B Processor Schematics

CPU : Northwood / Presott mPGA-478B Processor

System Brookdale - G / GL / GV / GE Chipset : INTEL GMCH + ICH4

On Board Chipset:

- **BIOS -- FWH**
- **LPC Super I/O -- W83627THF-AW**
- **Clock Generator -- CY28349B**
- **AC'97 Codec -- RealTek ALC655 / AD1888**
- **Onboard Lan Chipset-- RealTek RTL8100C**

Expansion Slots:

- **AGP2.0 Slot * 0**
- **PCI2.2 Slot * 3**
- **CNR Slot * 0**

Platform : Micro ATX (244 mm * 200 mm ; 9.61 inch * 8.03 inch)

MODEL Config.	ORCAD Config.	Function	Option	ERP Number
MS6555GV STD (6555L2-40a-STD)	Cfg6555GV-ALC655	GV STD (ALC655)	STD	601-6555-19S
MS6555GV option: A (6555L2-40a-A)	Cfg6555GV-AD1888	GV STD + AD1888	A	601-6555-20S
MS6555GL STD	Cfg6555GL-ALC655	GL STD (ALC655)	GL	
MS6555GL option: A	Cfg6555GL-AD1888	GL STD + AD1888	GLA	

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Title: COVER SHEET

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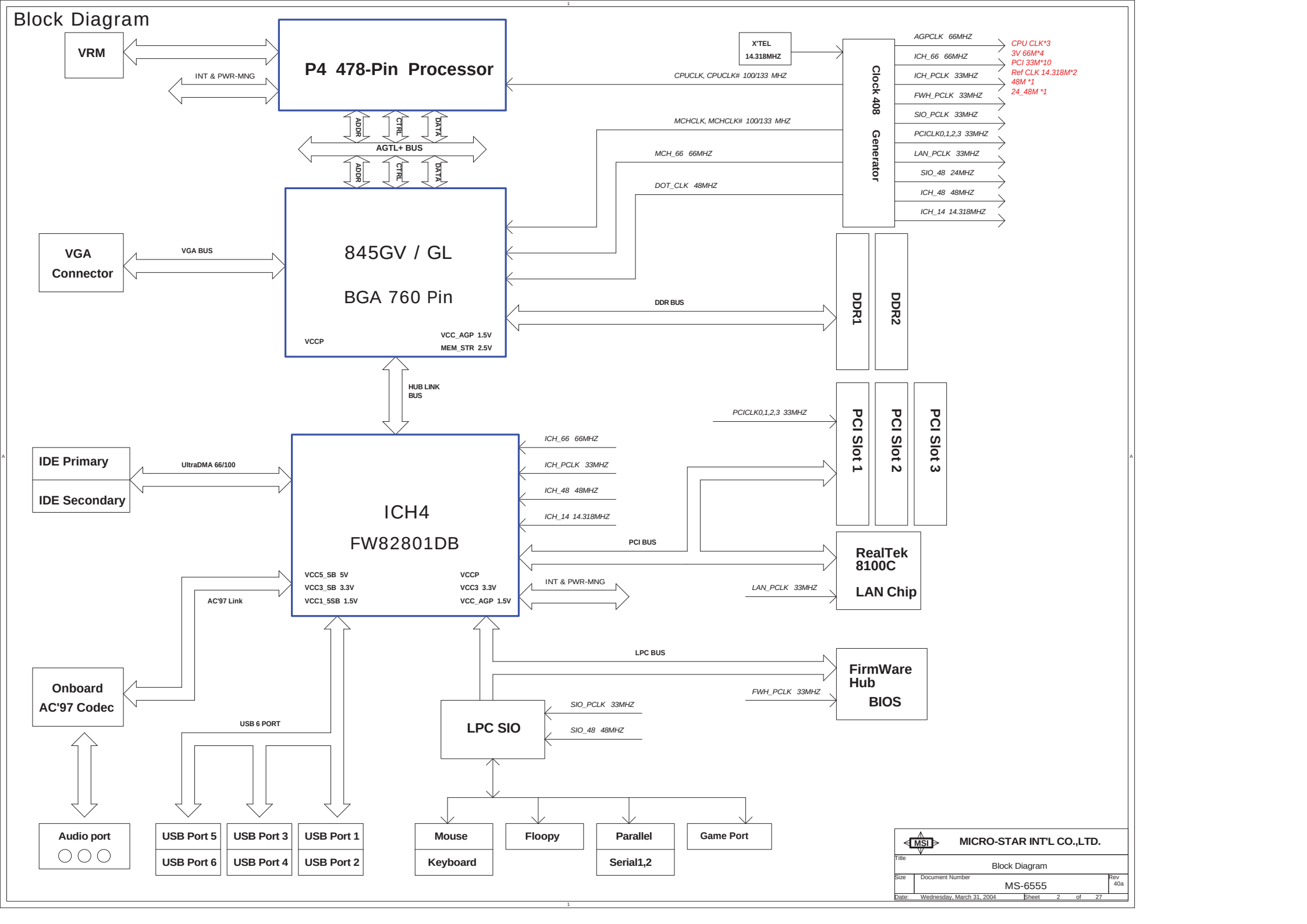
Block Diagram



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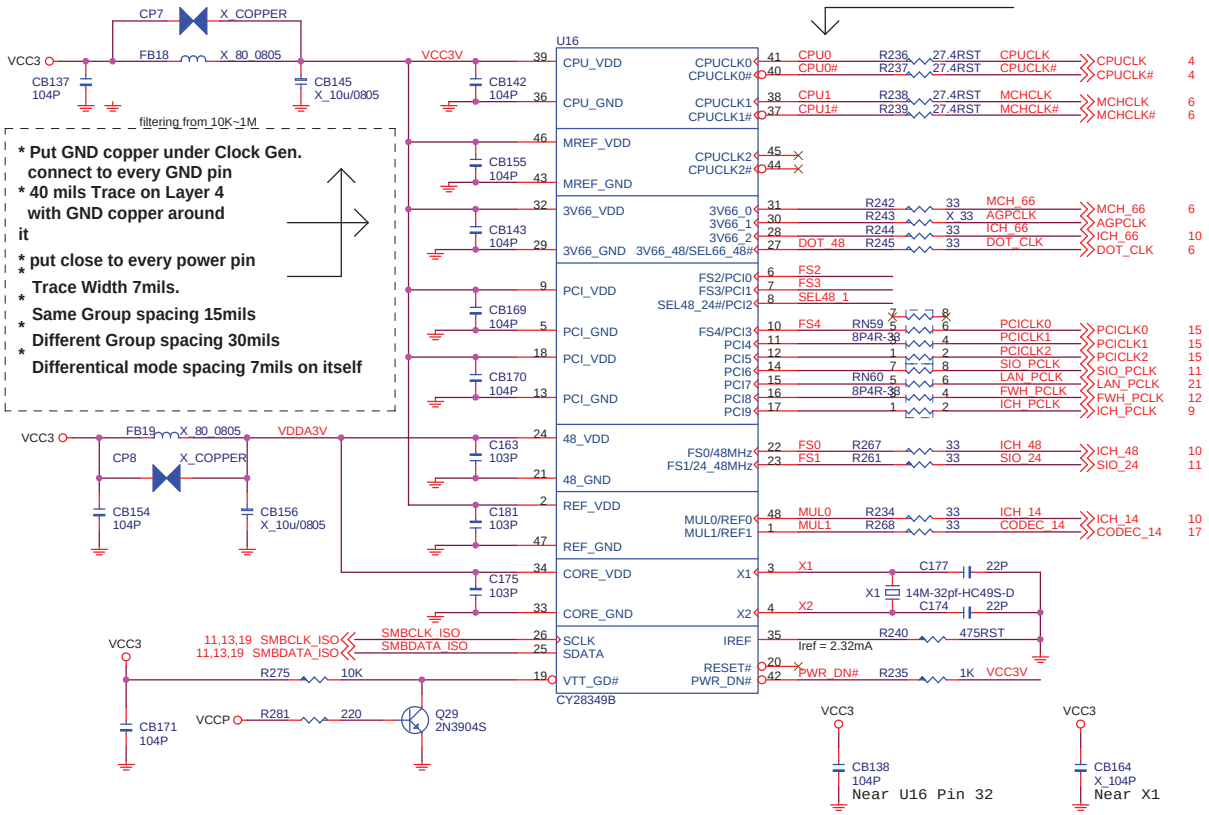
CLOCK GENERATOR BLOCK

*Trace < 0.5"



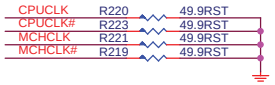
filtering from 10K~1M

* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differentical mode spacing 7mils on itself

Near U16 Pin 32

Near X1

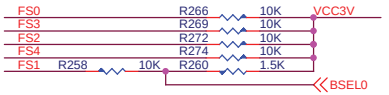
Shut Source Termination Resistors



Trace less 0.2"

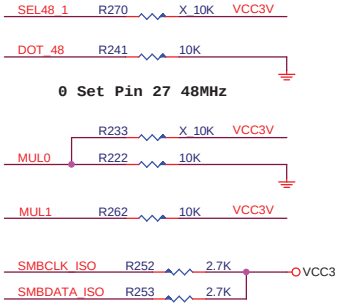
49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



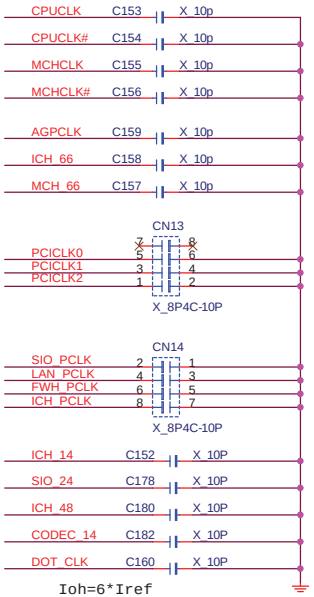
BSEL0 0 100 ; 1 133

FS4	FS3	FS2	FS1	FS0	FSB (MHz)
1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz



MUL 1:0	
0 0	4X
0 1	5X
1 0	6X
1 1	7X

Pull-Down Capacitors

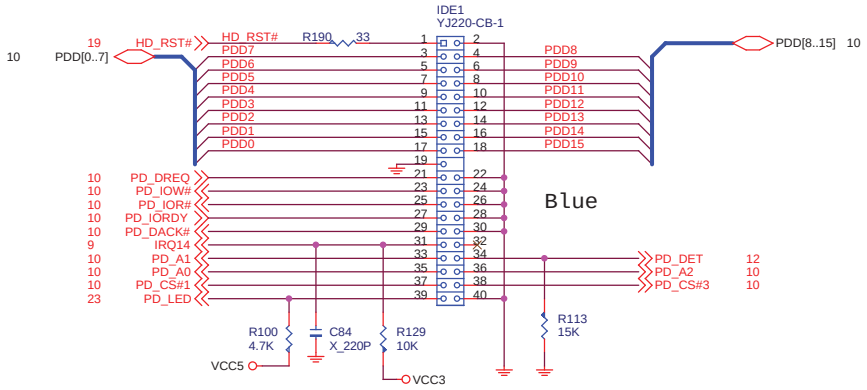


Ioh=6*Iref
Voh=0.71V

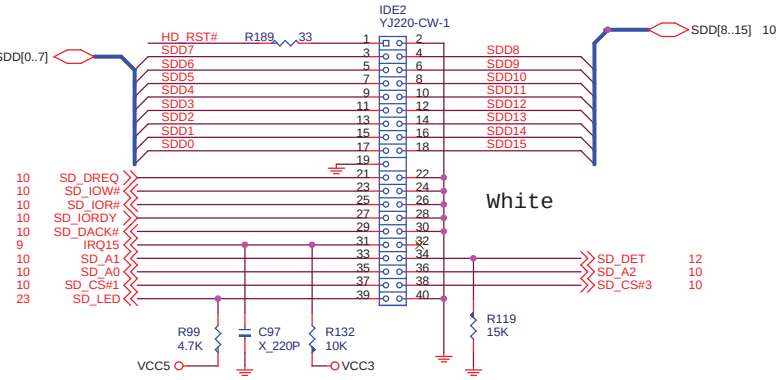
used only for EMI issue

Trace less 0.2"

PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



ATA100 IDE CONNECTORS

DIOR-:HDMARDY-(Host Strobe)
IORDY:DDMARDY-(Device Strobe)
DIOW-:STOP
PDIAG-:CBLID-

Trace Width : 5mils
Trace Spacing : 7mils
Trace Length less than 5"
Strobe Equal
Length(longest)-Length(shortest)<0.5"

MICRO-STAR

Title	CLOCK GEN & ATA100 IDE	
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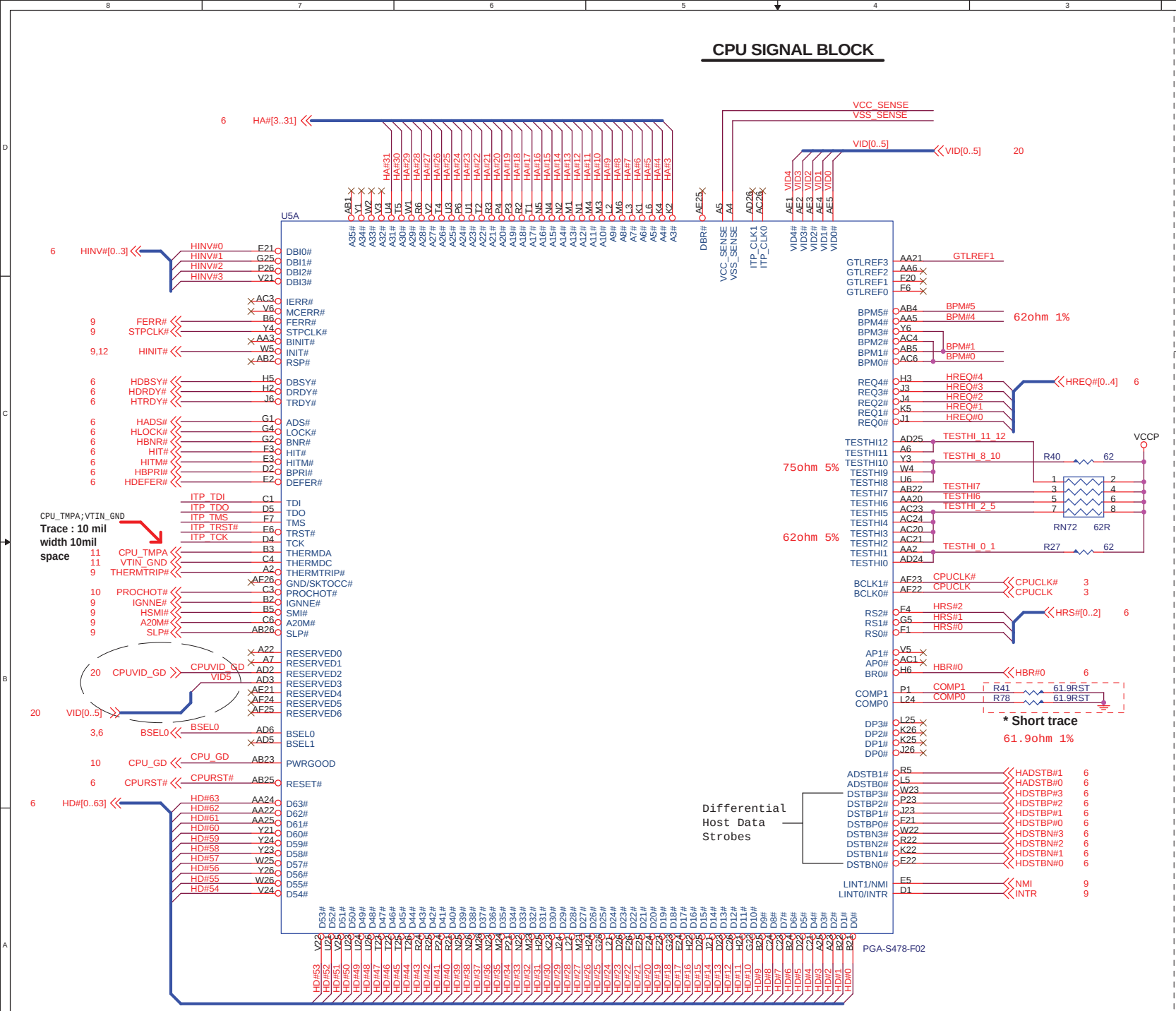
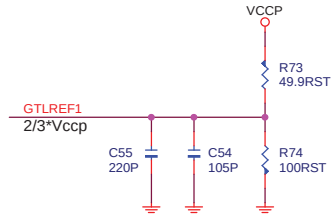
CPU SIGNAL BLOCK

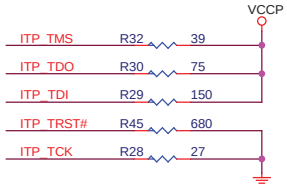


CPU GTL REFERNCE VOLTAGE BLOCK



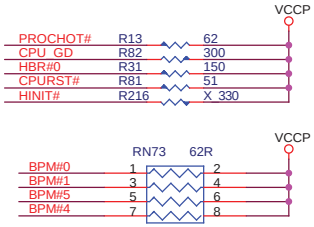
Every pin put one 220pF cap near it.
Trace Width 10mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



ALL COMPONENTS CLOSE TO CPU

CPU STRAPPING RESISTORS



Pin Definition Change	
AD1 : BOOTSELECT	Input
AD2 : VIDPWRGD	Input
AD3 : VID5	Output
AE26: OPTIMZED/COMPAT*	Input
AF3 : VCCVIDLB	Input

The OPTIMZED/COMPAT*(AE26) and RSP#(AB2) pins on the CPU socket should be left as a no connect(NC).

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Title: INTEL mPG478 CPU1

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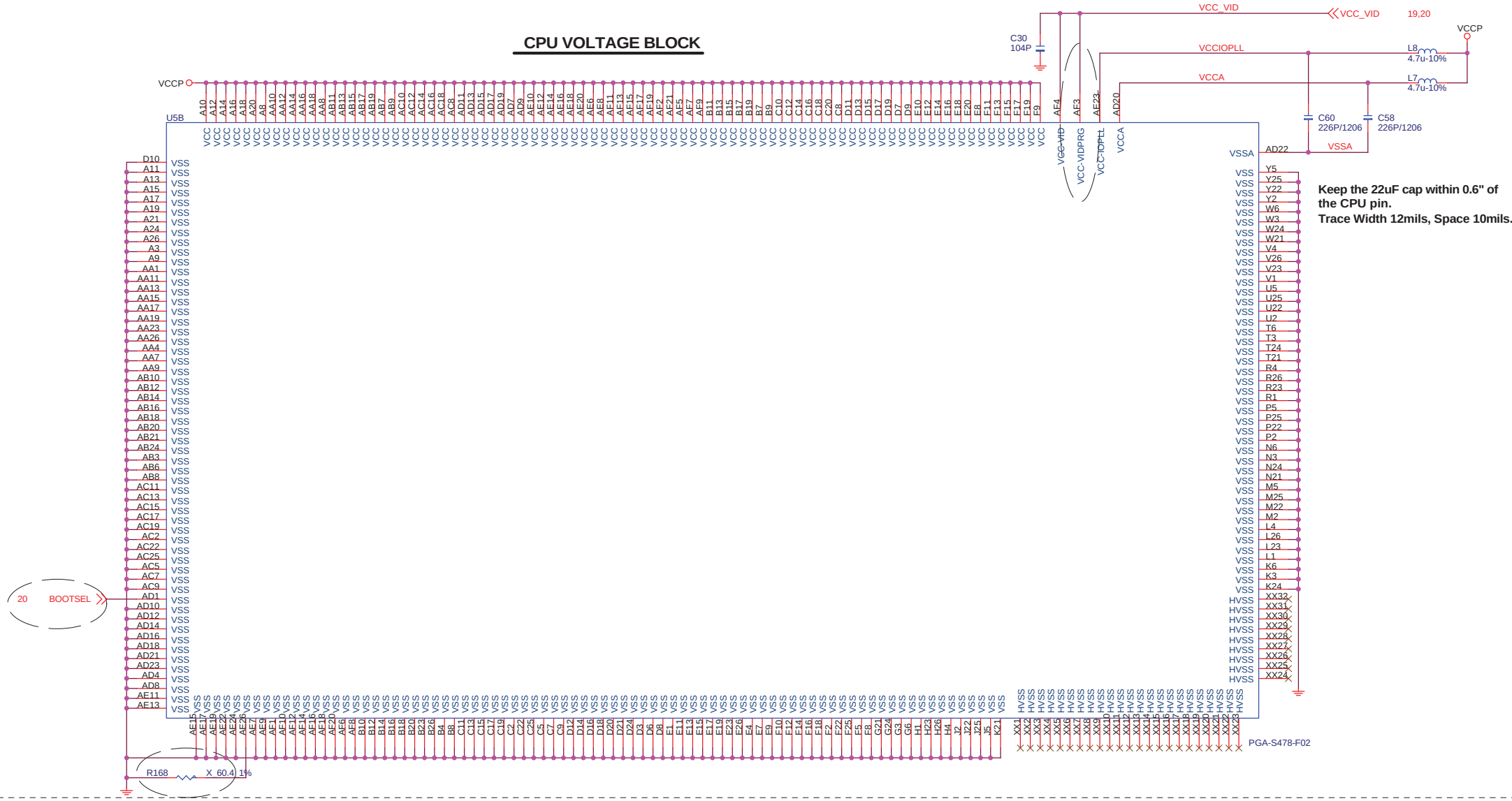
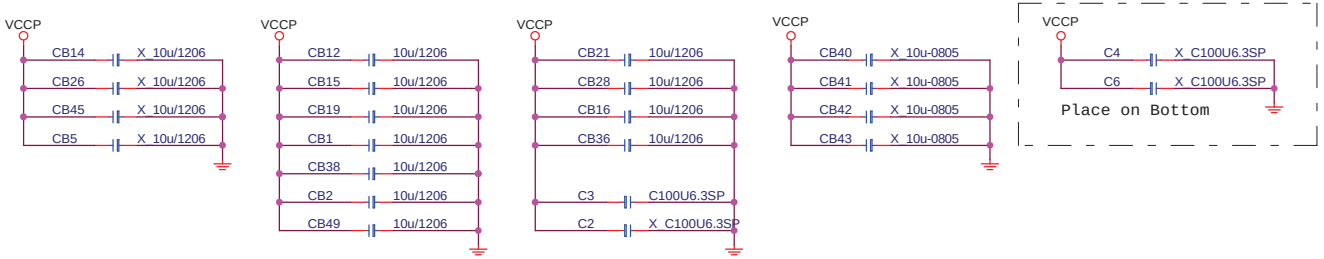
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



MLCC(10uF / Y5V / 1206)
Taiyo

MLCC(10uF / Y5V / 0805)
Walsin

SP-CAP(100uF)
Ripplecur = 2000mA
Impedance = 20mΩ
Panasonic

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Title: INTEL mPGA478-B CPU2

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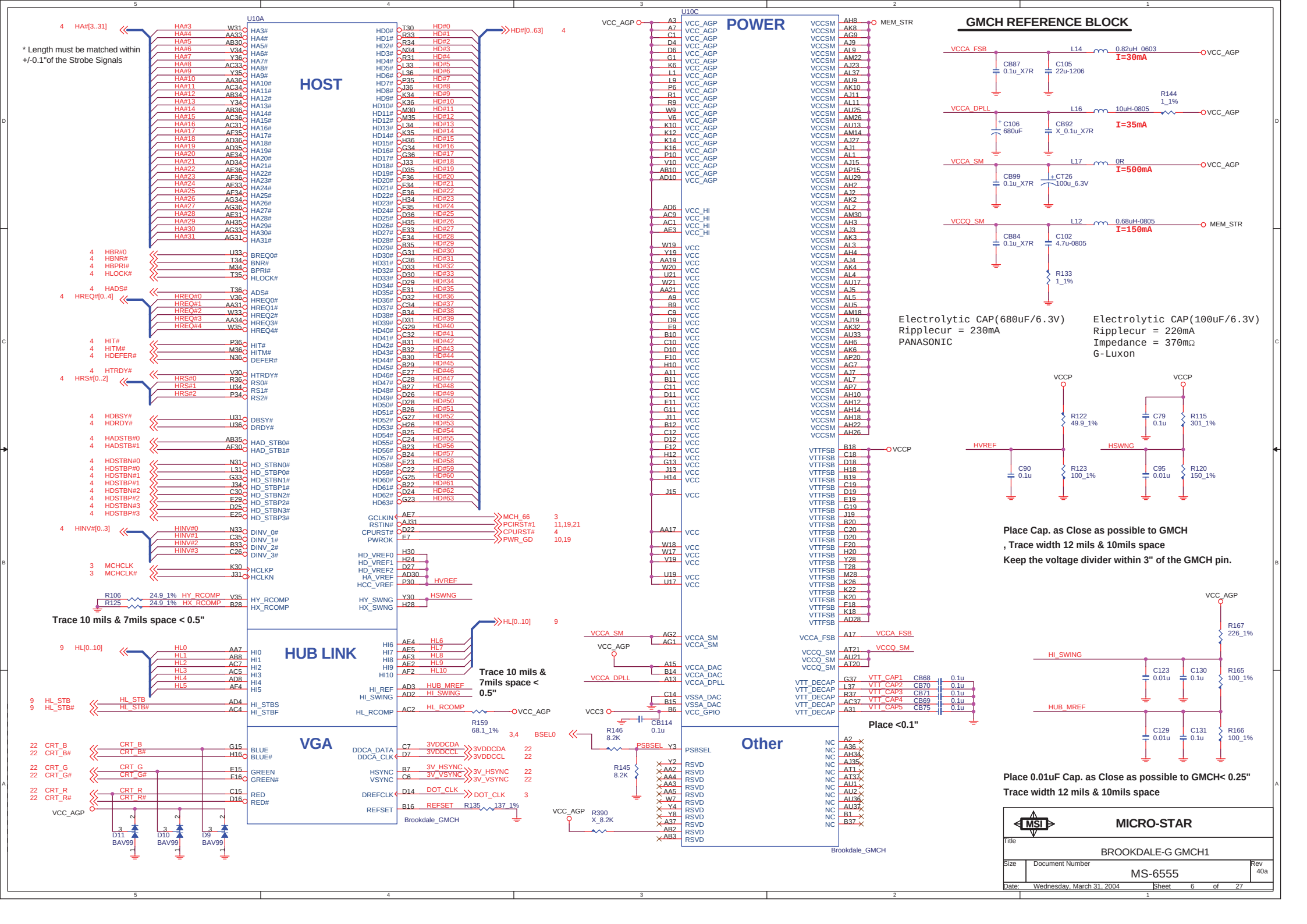
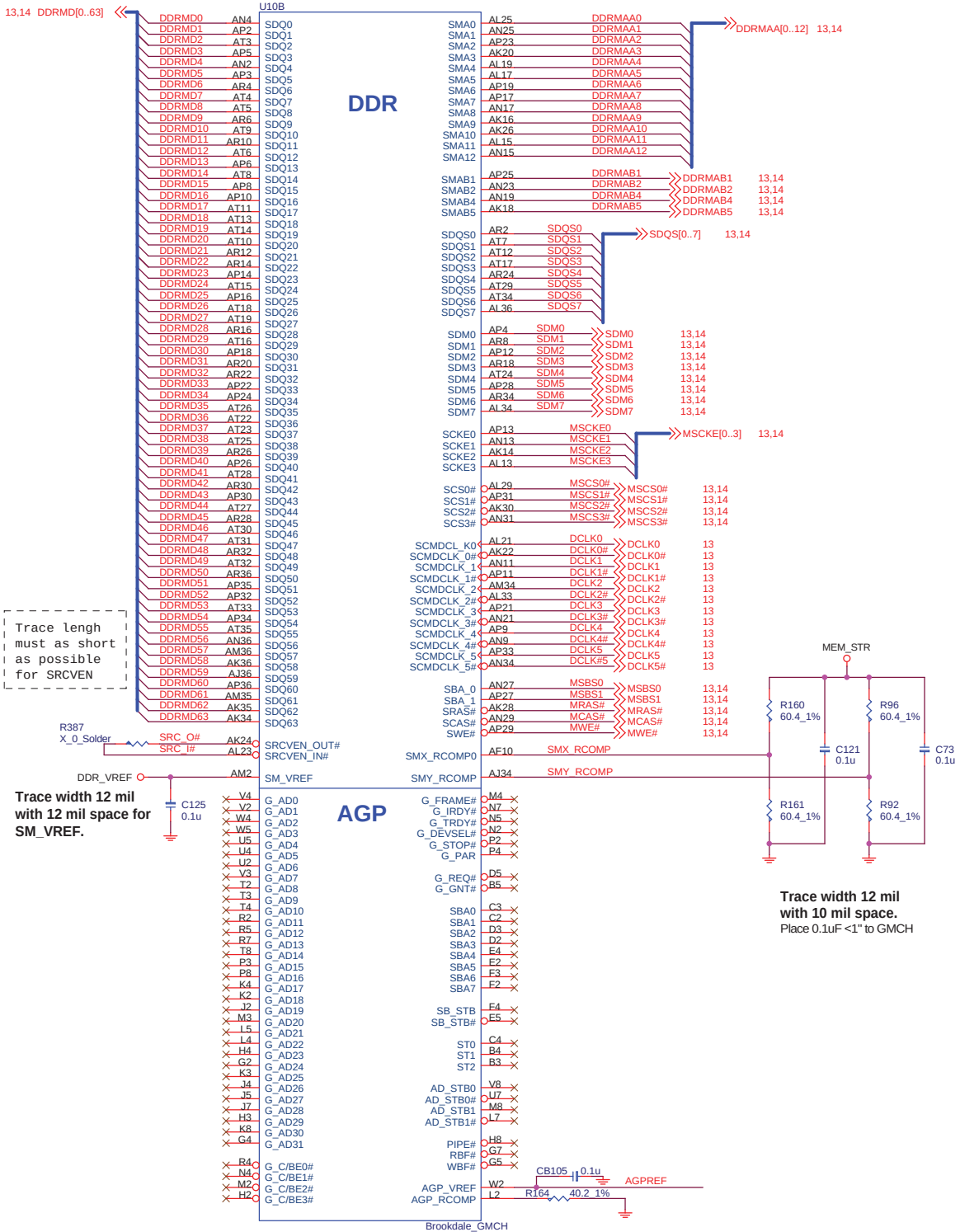
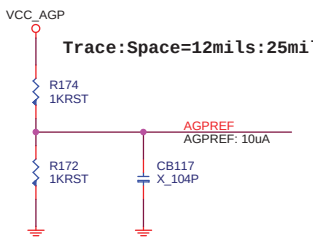

HOST
HUB LINK
VGA
POWER
Other
U10A
U10C
* Length must be matched within +/-0.1"of the Strobe Signals
Trace 10 mils & 7mils space < 0.5"
Trace 10 mils & 7mils space < 0.5"
Place <0.1"
GMCH REFERENCE BLOCK
VCCA_FSB
VCCA_DPLL
VCCA_SM
VCCQ_SM
MEM_STR
VCC_AGP
I=30mA
I=35mA
I=500mA
I=150mA
Electrolytic CAP(680uF/6.3V)
Ripplecur = 230mA
PANASONIC
Electrolytic CAP(100uF/6.3V)
Ripplecur = 220mA
Impedance = 370mΩ
G-Luxon
VCCP
HVREF
HSWNG
Place Cap. as Close as possible to GMCH
, Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the GMCH pin.
HI_SWING
HUB_MREF
Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space
Brookdale_GMCH
MICRO-STAR
BROOKDALE-G GMCH1
MS-6555
Wednesday, March 31, 2004



DDR SERIAL RESISTORS

AGP SLOT DECOUPLING CAPACITORS

AGP SIGNAL REFERENCE CIRCUIT



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Title	BROOKDALE-G GMCH2	
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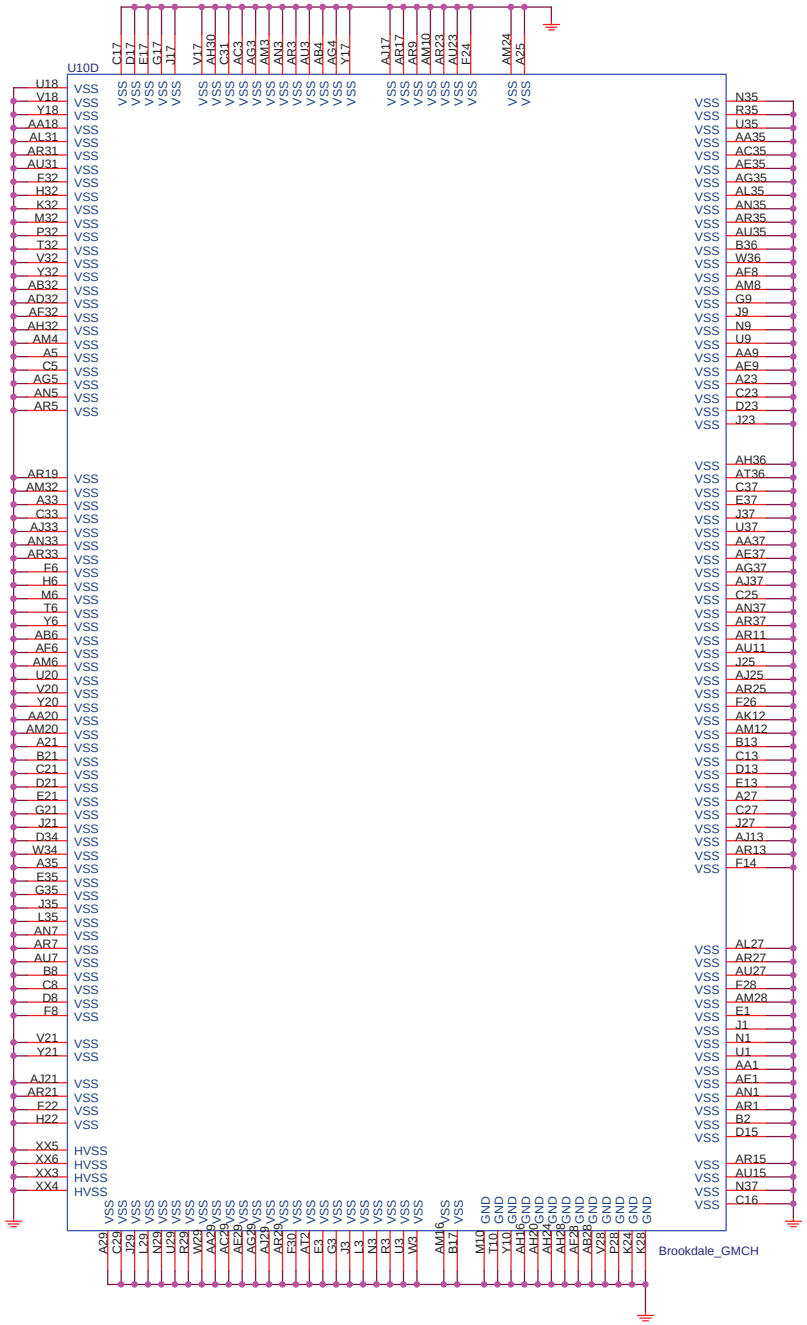
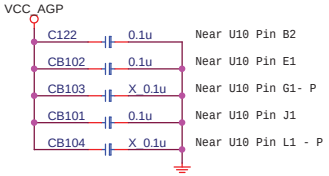
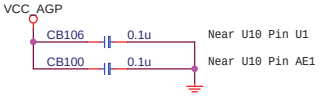


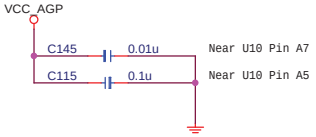
GMCH DECOUPLING CAPACITOR



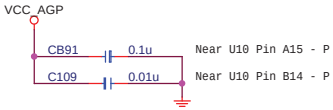
Place decoupling cap close to GMCH AGP Interface < 0.1"



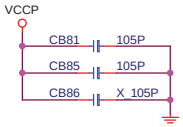
Place decoupling cap close to GMCH Hub-Link Interface< 0.1"



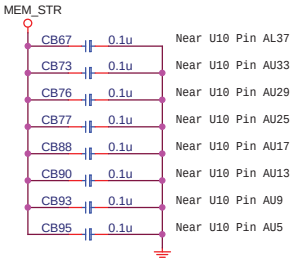
Place decoupling cap close to GMCH DAC Interface< 0.1"



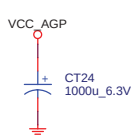
Place decoupling cap close to GMCH Core Logic Interface < 0.1"

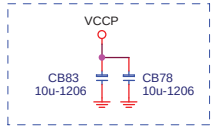


Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor

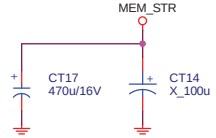


Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width





Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot

Electrolytic CAP(470uF/16V)
Ripplecur = 310mA
Panasonic

Electrolytic CAP(1000uF/6.3V)
Ripplecur = 1050mA
Impedance = 50mΩ
Panasonic

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Title: Broodale-G GMCH3		
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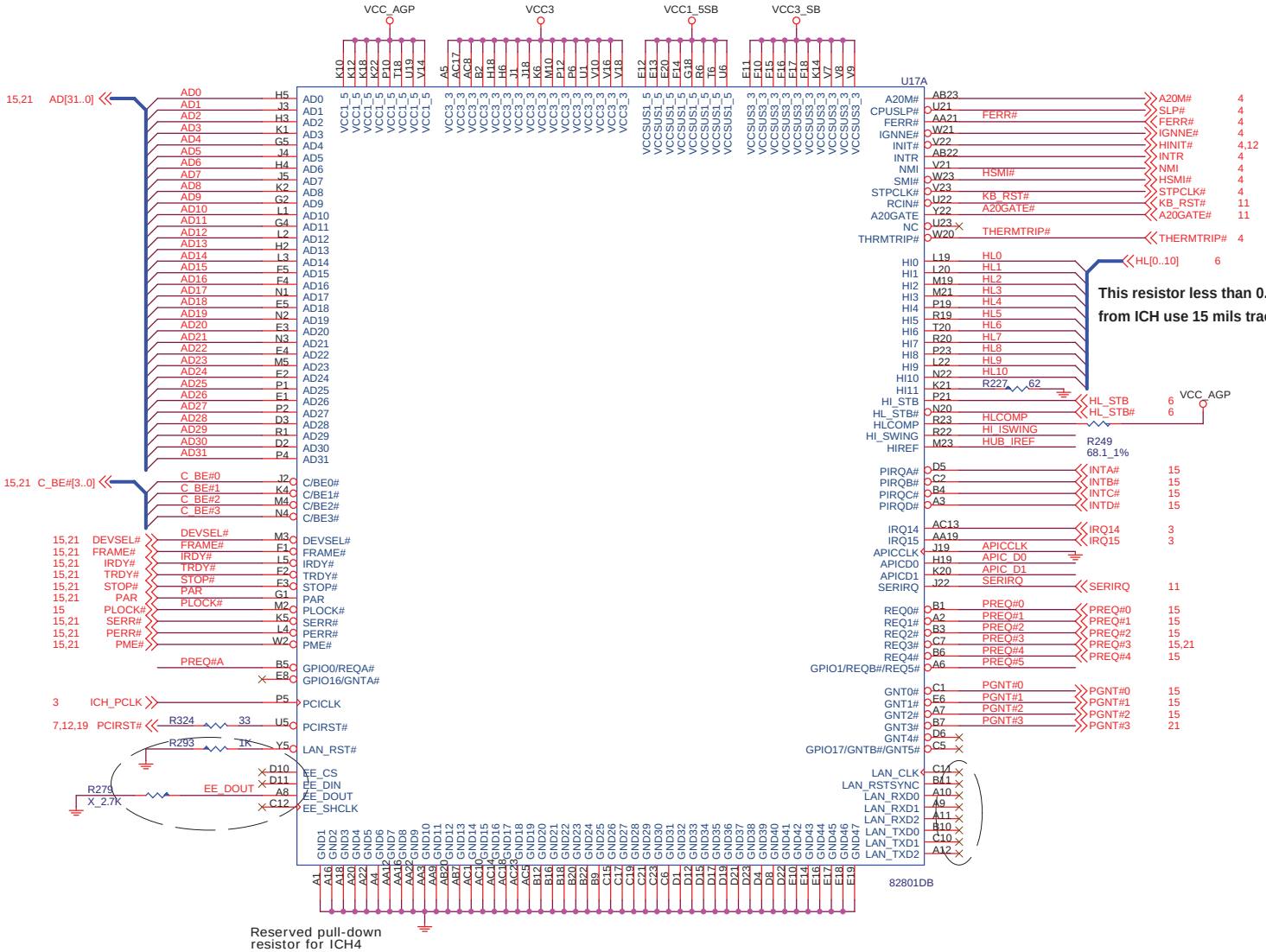
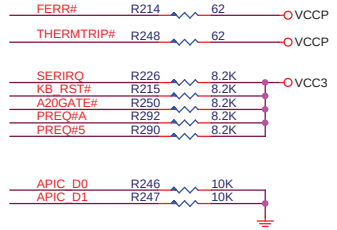
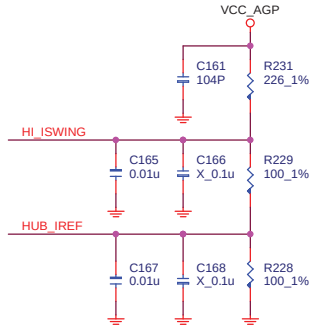
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



ICH4 PULL-UP/DOWN RESISTORS

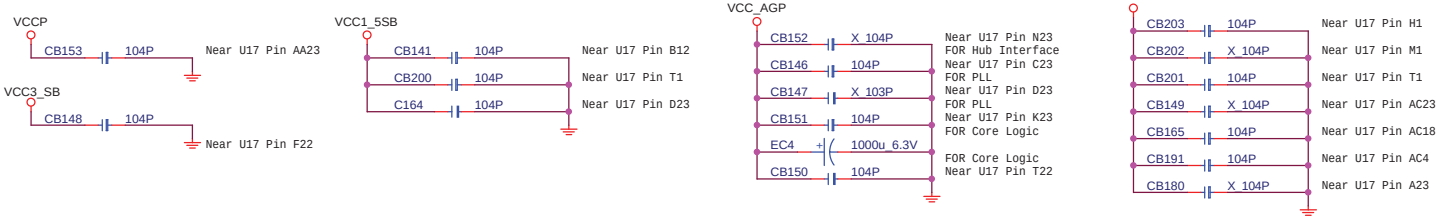


ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS



Place one 0.1u close to ICH4 <100 mil

MICRO-STAR

Title: ICH4 PCI/HI/LAN

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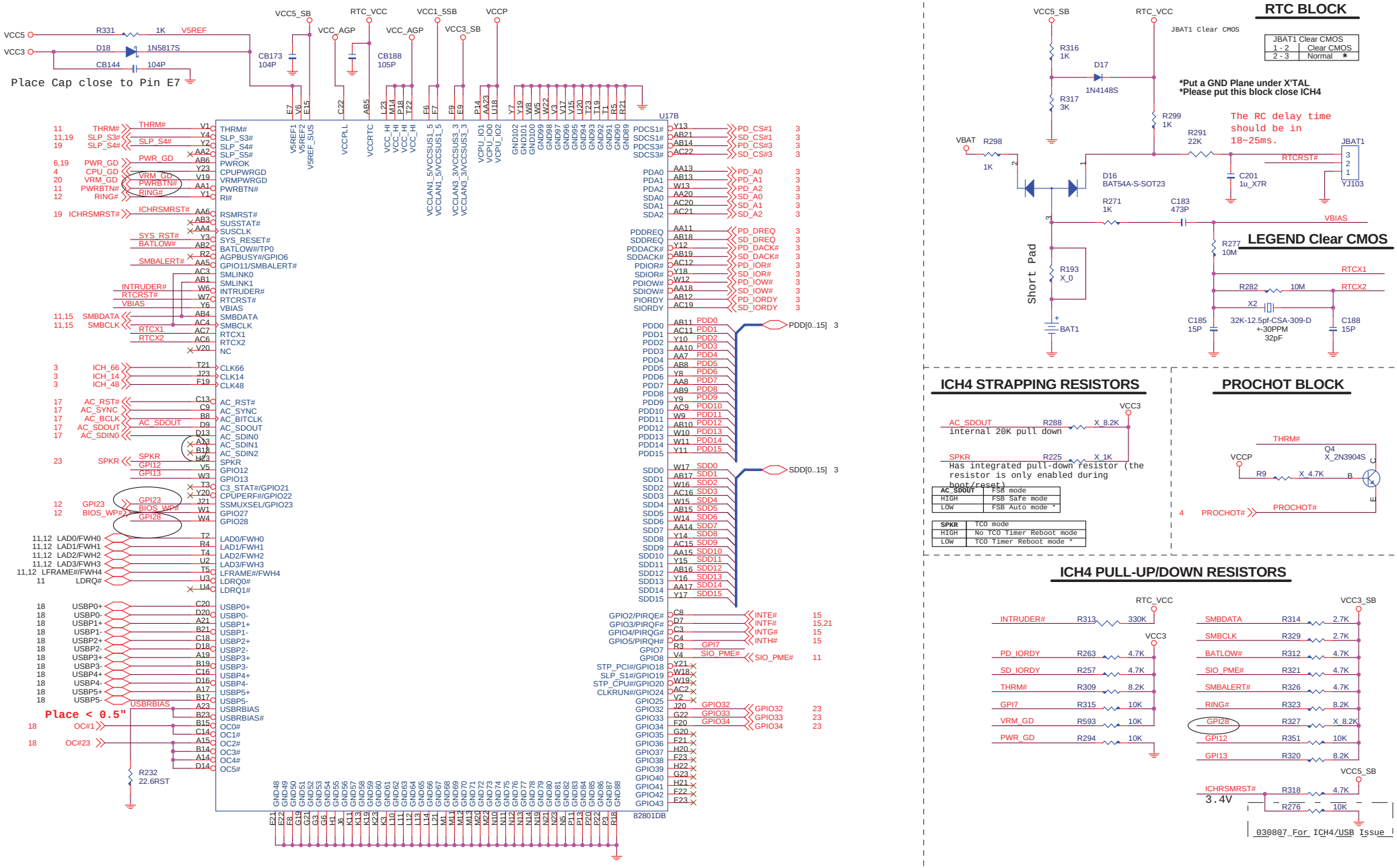

RTC BLOCK

LEGEND Clear CMOS

ICH4 STRAPPING RESISTORS

AC_SDOUT	FSB mode
HIGH	FSB Safe mode
LOW	FSB Auto mode *

SPKR	TCO mode
HIGH	No TCO Timer Reboot mode
LOW	TCO Timer Reboot mode *

PROCHOT BLOCK

ICH4 PULL-UP/DOWN RESISTORS

ICH4 DECOUPLING CAPACITOR

Place one 0.1u close to ICH4 <100 mil

SYSTEM RESET

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Title: ICH4 OTHER

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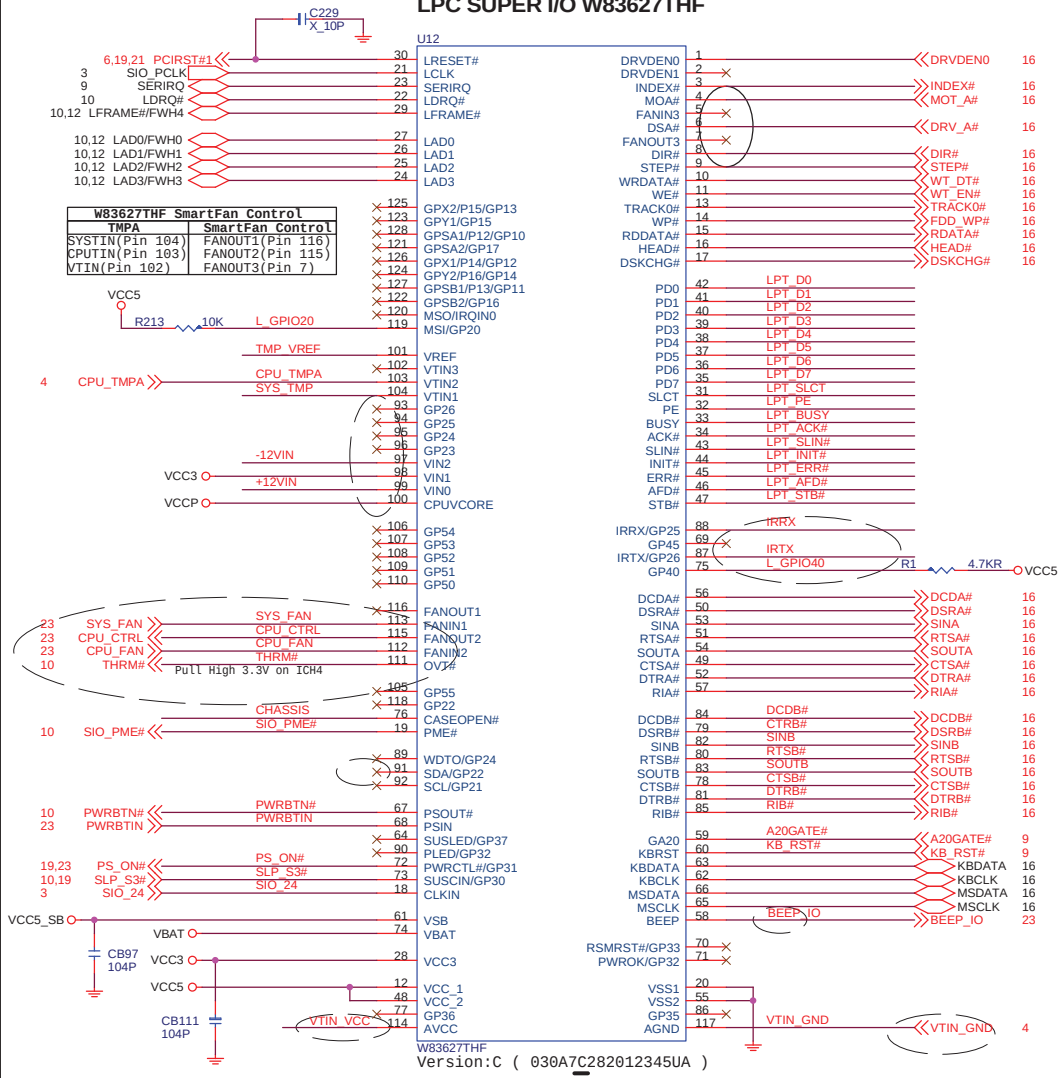
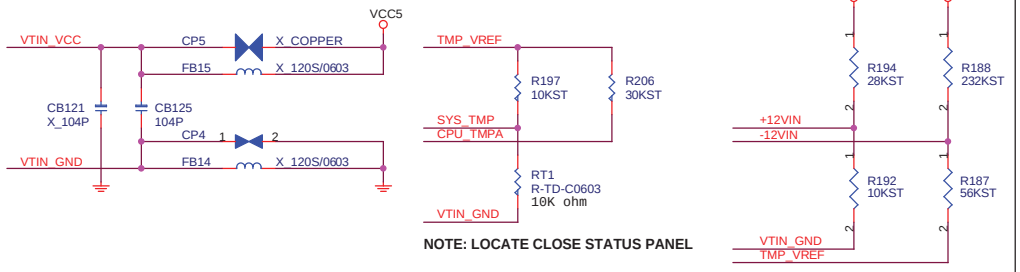
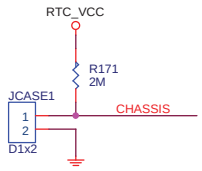
LPC SUPER I/O W83627THF



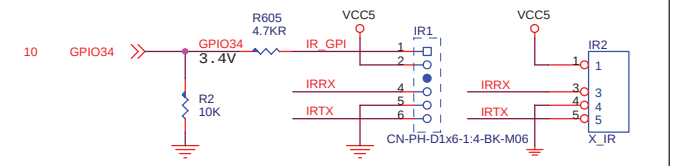
THERMAL RESISTOR BLOCK



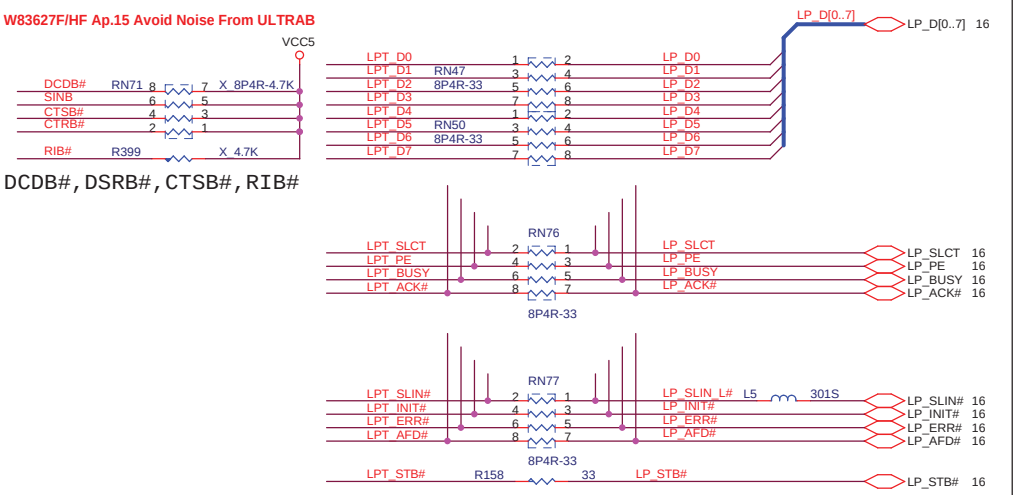
Chasiss Intrusion Header



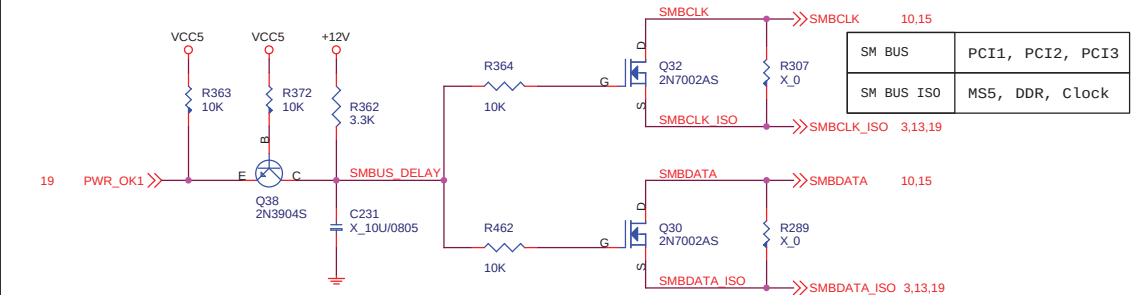
Legend Front IR Header



W83627F/HF Ap.15 Avoid Noise From ULTRAB

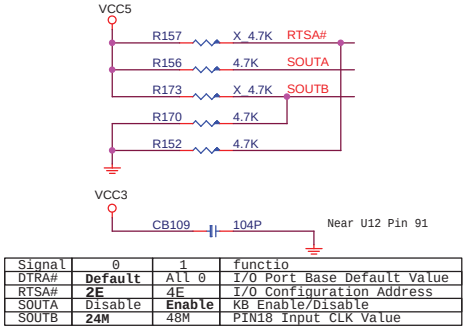


SMBus Isolation



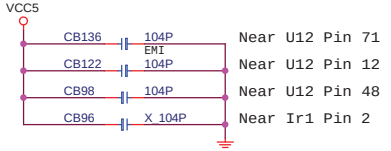
SM BUS	PCI1, PCI2, PCI3
SM BUS ISO	MS5, DDR, Clock

SUPER I/O STRAPPING RESISTOR



Signal	0	1	functio
DTRA#	**Default**	All 0	I/O Port Base Default Value
RTSA#	**2E**	4E	I/O Configuration Address
SOUTA	Disable	**Enable**	KB Enable/Disable
SOUTB	**24M**	48M	PIN18 Input CLK Value

LPC I/O DECOUPLING CAPACITORS



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Title: LPC SUPER I/O

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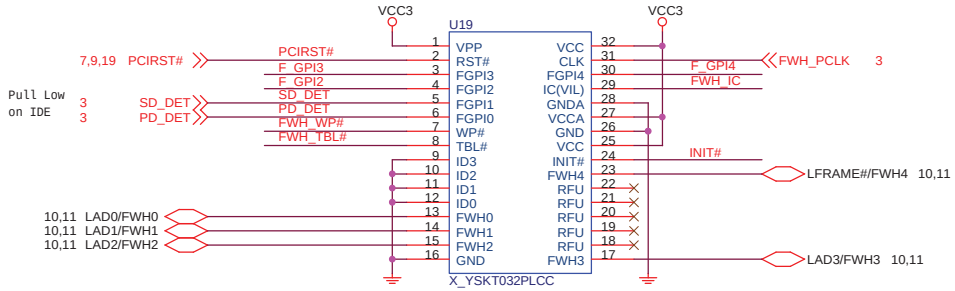
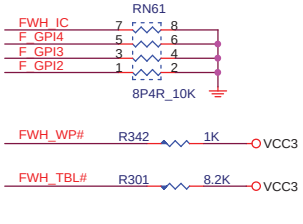
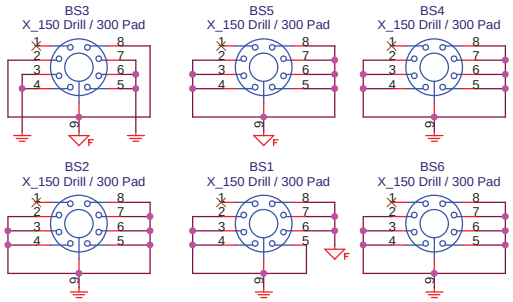
Firware Hub (FWH)



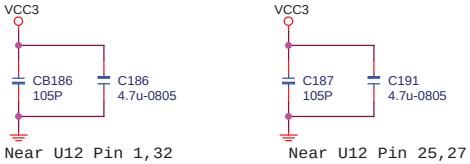
FWH RESISTORS



PCB Mounting Holes

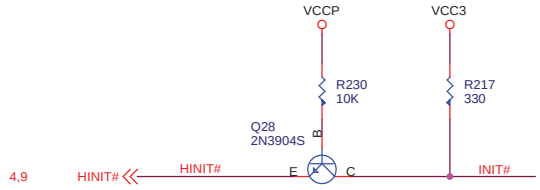


FWH DECOUPLING CAPACITORS

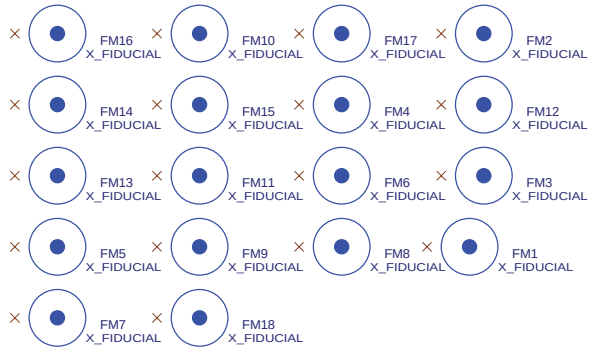


Place Cap. as Close to FWH< 350 mil

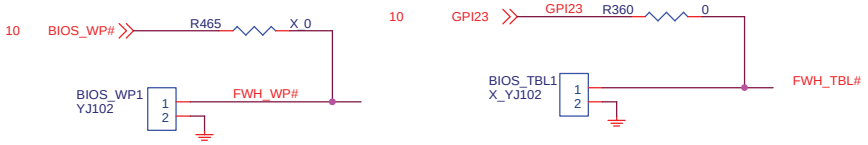
FWH INIT Signal Voltage Translation Block



PCB Fiducials



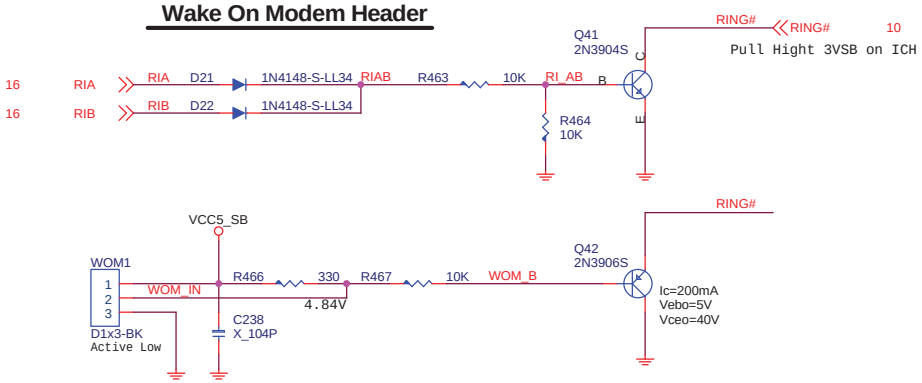
FWH write protect

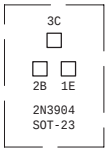


BIOS_WP	BIOS_WP1
Flash Write Enable	OPEN (Default)
Flash Write Disable	SHORT

SIMULATION TRACE

Wake On Modem Header





MSI **MICRO-STAR**

Title: FWH

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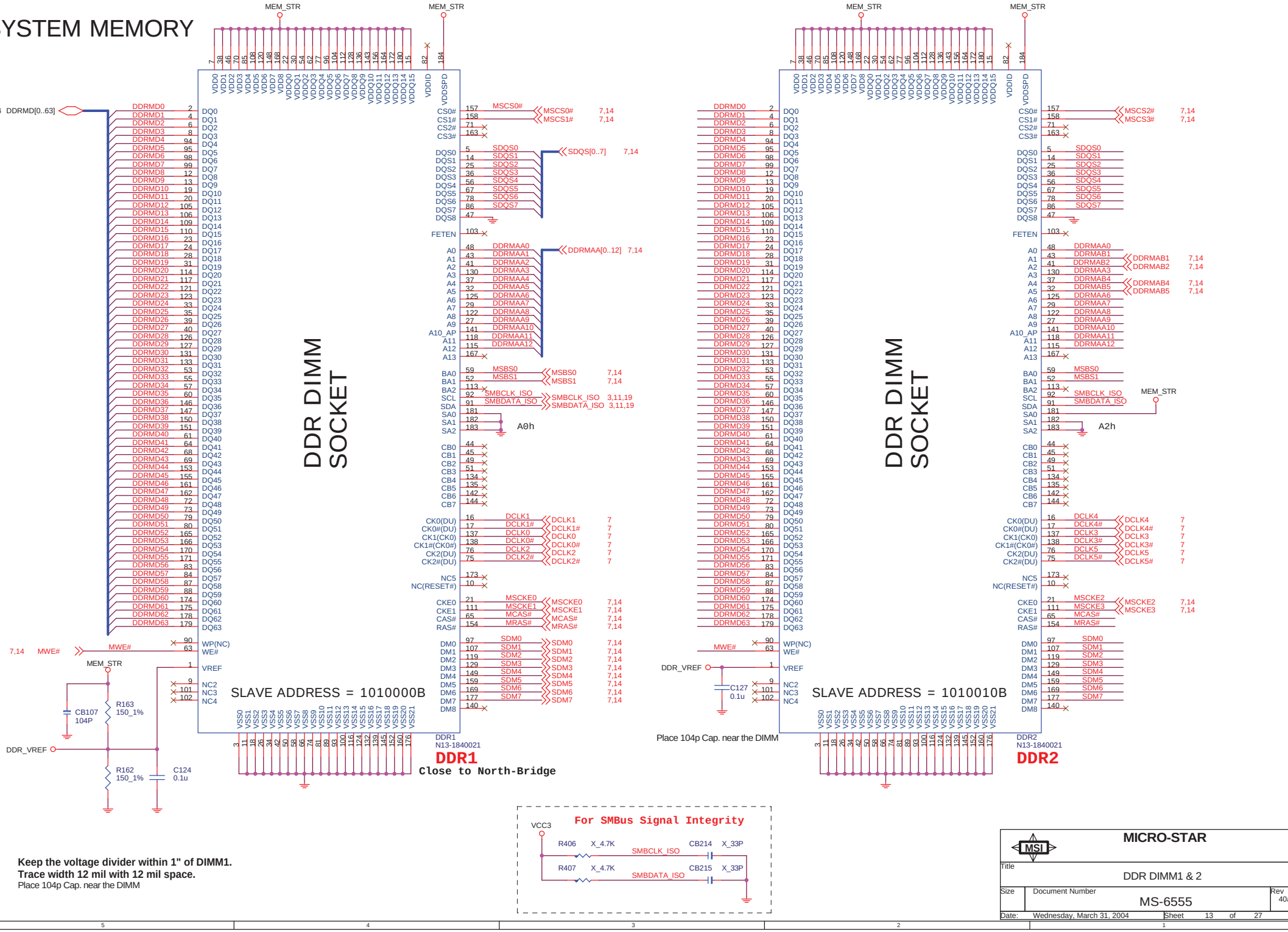
Date: Wednesday, March 31, 2004 Sheet 12 of 27

SYSTEM MEMORY



Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DIMM

MICRO-STAR

Title	DDR DIMM1 & 2	
Size	Document Number MS-6555	Rev 40a
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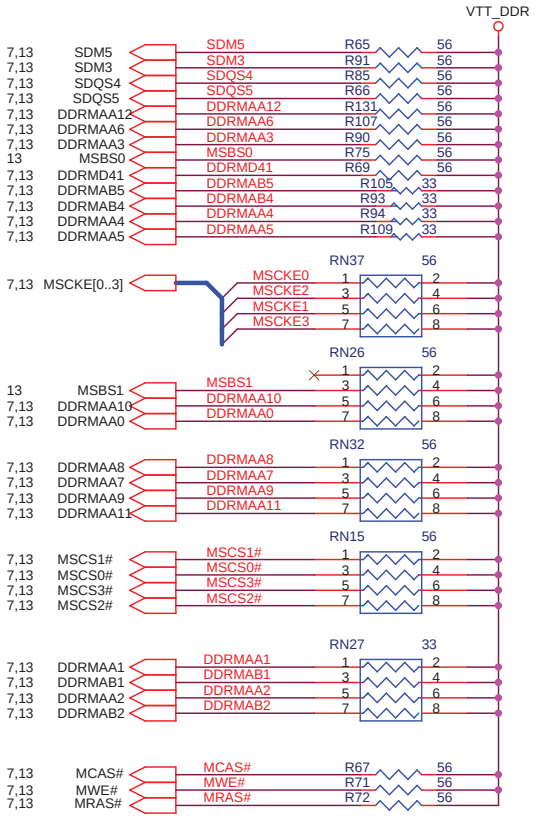
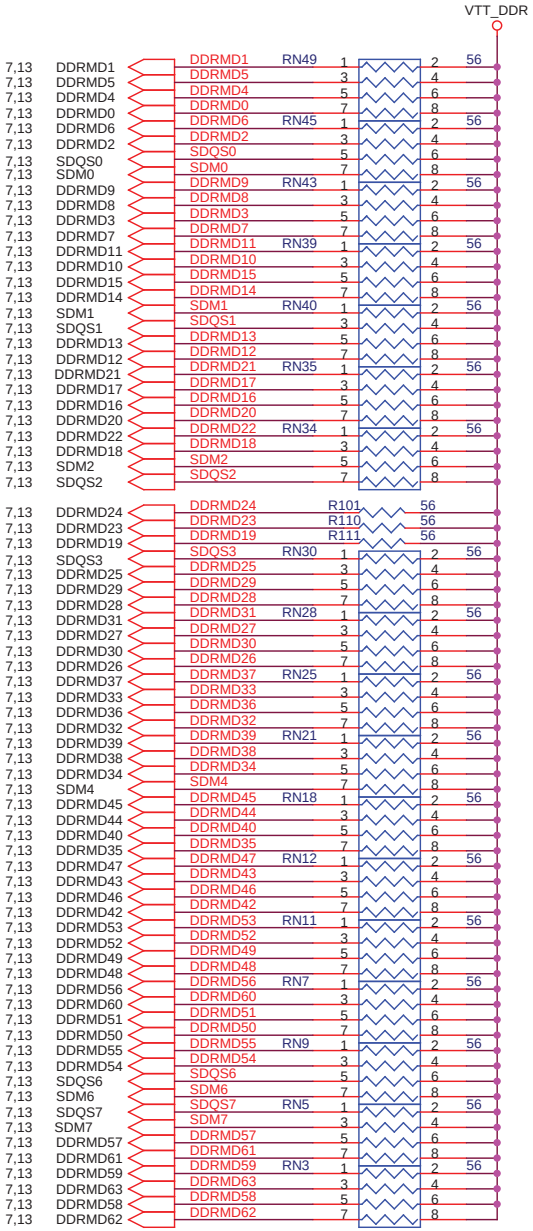
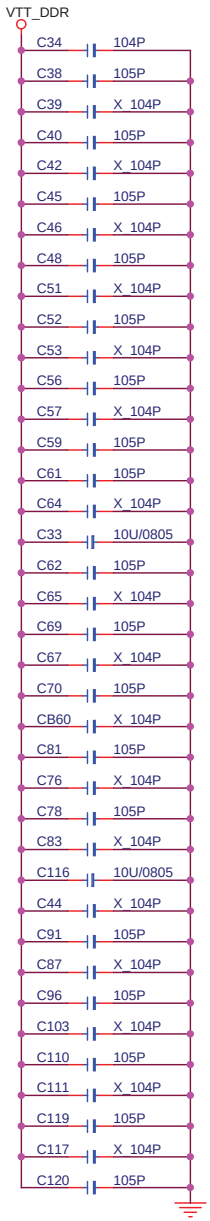
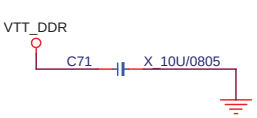
DDR TERMINATORS

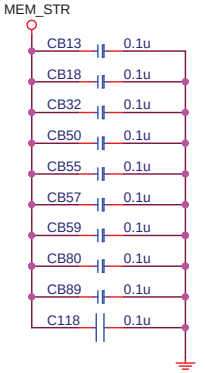


TERMINATION DECOUPLING









9Pcs doupling caps place between DDR1 and DDR2

MSI MICRO-STAR

Title: DDR DAMPING

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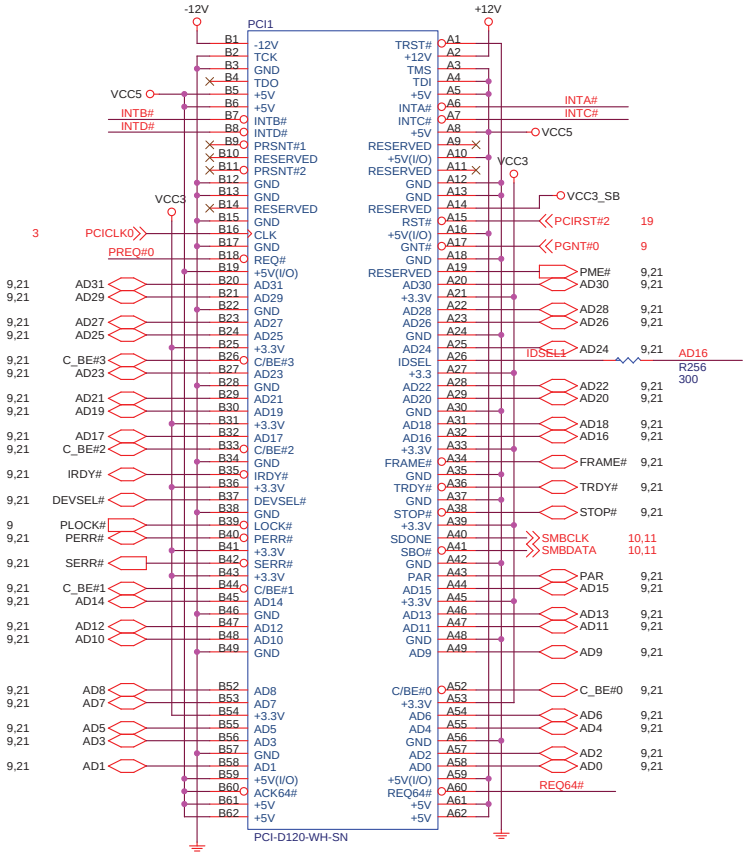
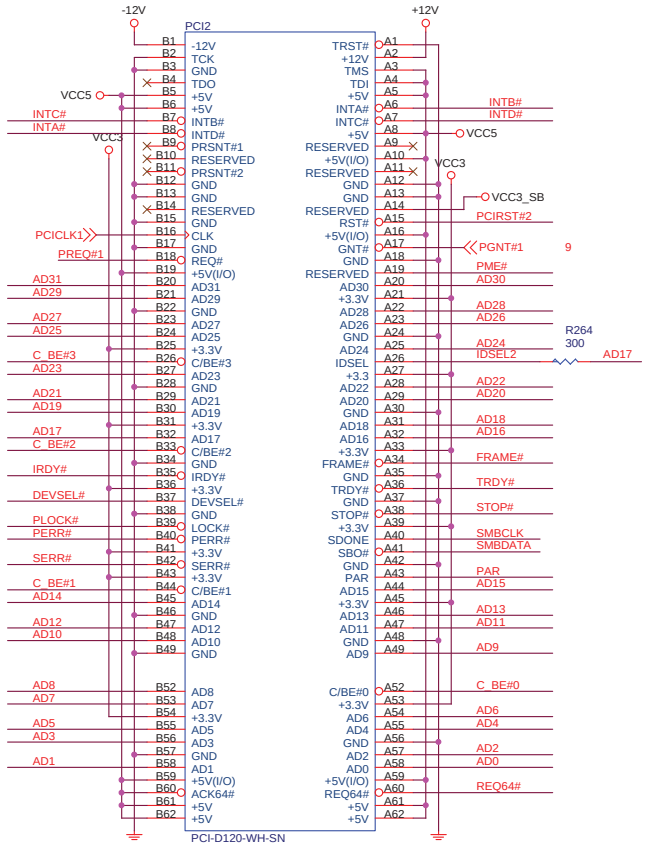
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



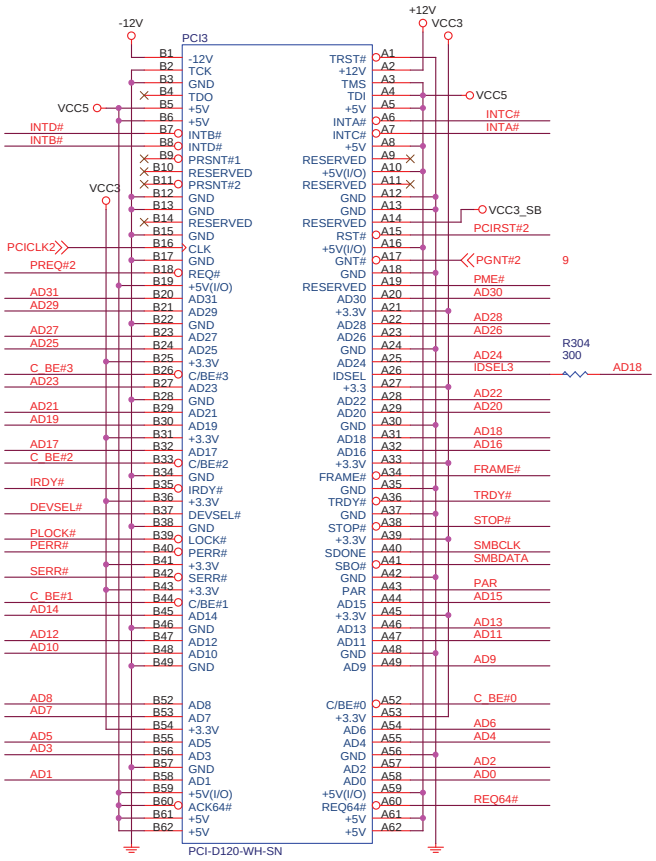
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



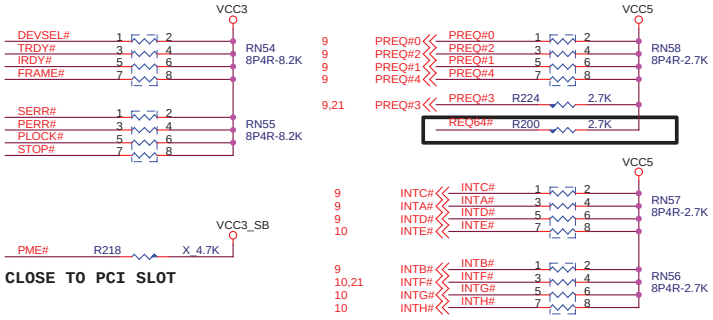
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

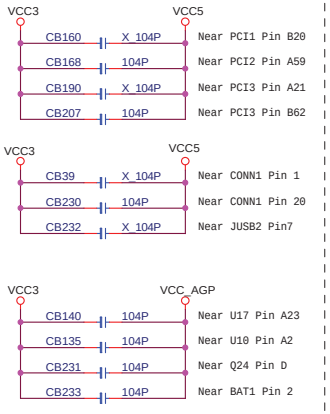


IDSEL = AD18
MASTER = PREQ2
INTC#

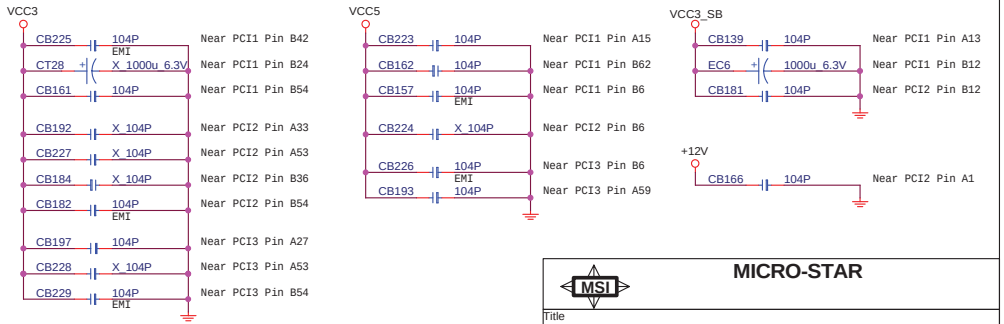
PCI PULL-UP / DOWN RESISTORS



CLOSE TO PCI SLOT



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR

Title: PCI SLOT 1,2,3

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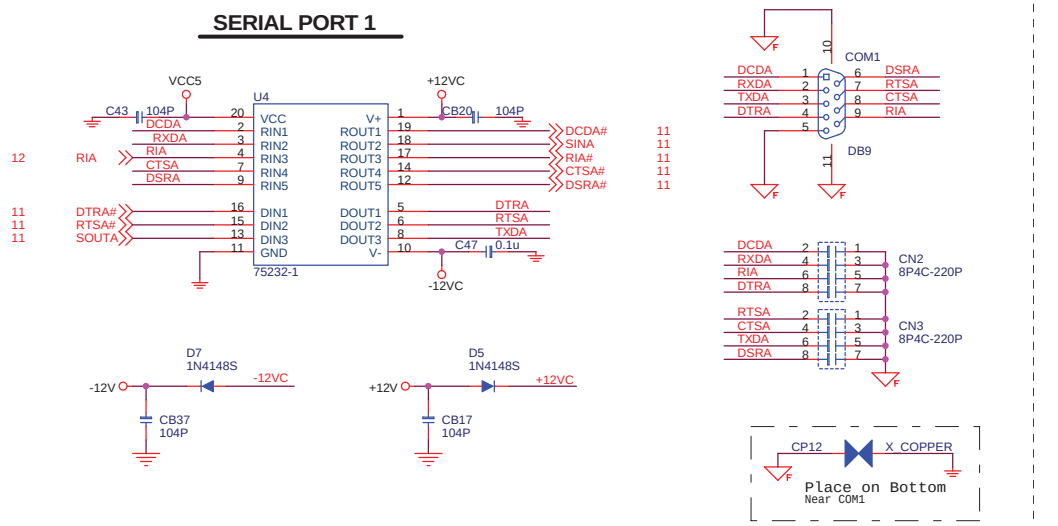
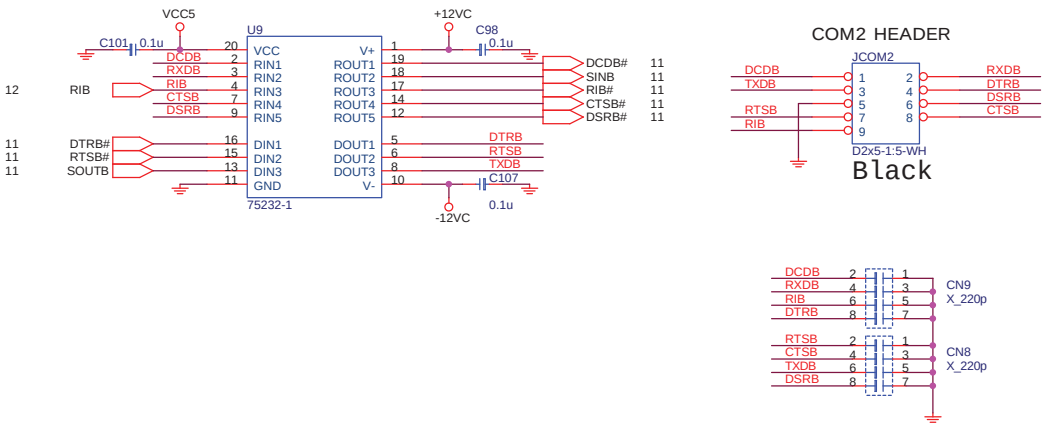
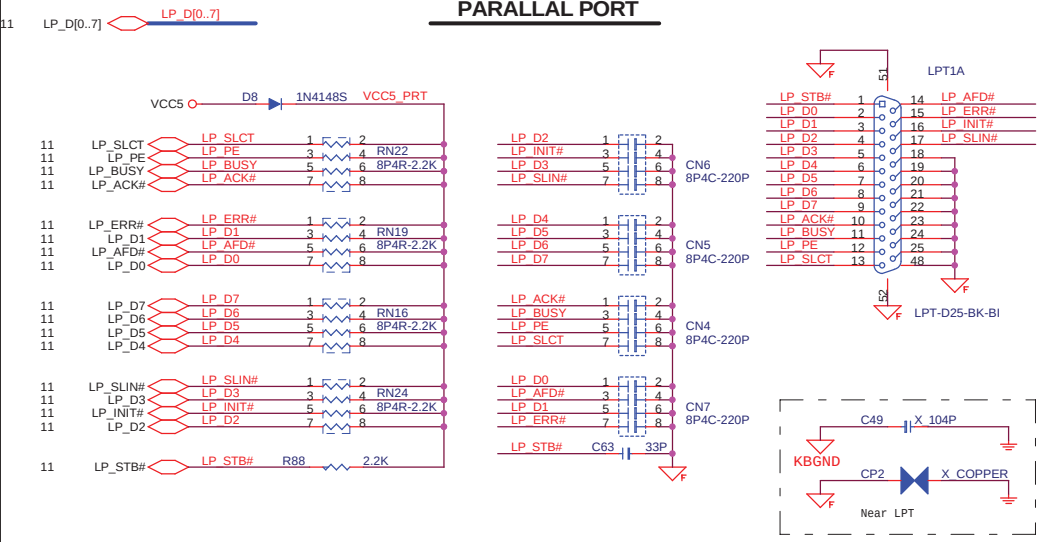
SERIAL PORT 1



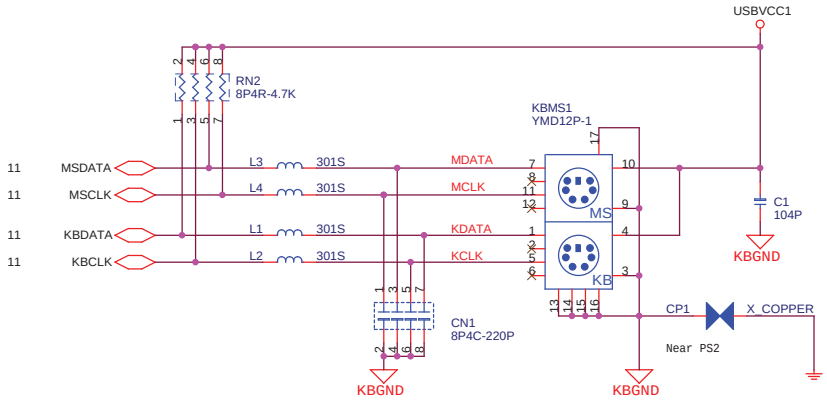
SERIAL PORT 2



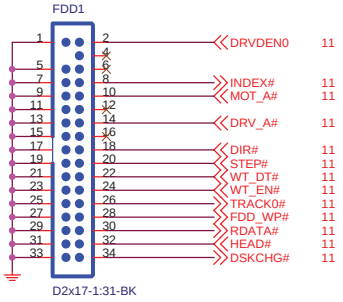
PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR



FLOPPY CONNECTOR



MSI MICRO-STAR

Title: I/O CONNECTORS

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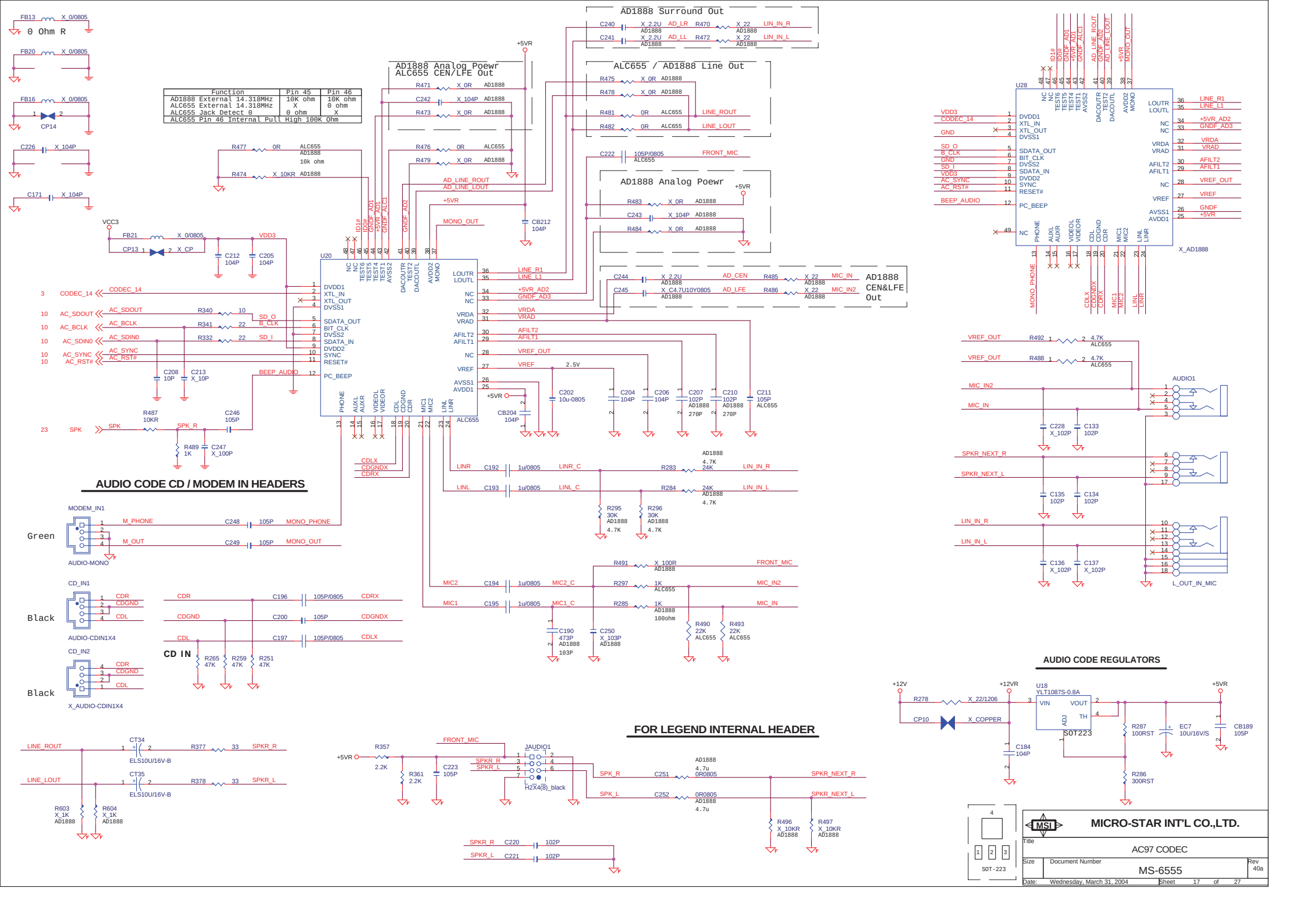
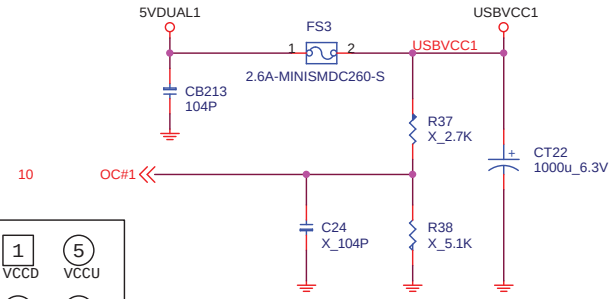
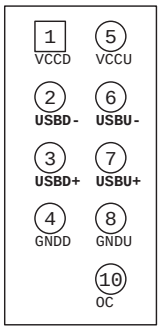

AD1888 Surround Out
ALC655 / AD1888 Line Out
AD1888 Analog Poewr
ALC655 CEN/LFE Out
AD1888 Analog Poewr
ALC655 CEN/LFE Out
AUDIO CODE CD / MODEM IN HEADERS
AUDIO CODE REGULATORS
FOR LEGEND INTERNAL HEADER
CD IN
Green
Black
Black
U20
U28
ALC655
AD1888
MICRO-STAR INT'L CO.,LTD.
AC97 CODEC
MS-6555

POWER CIRCUIT FOR USB PORT 0,1

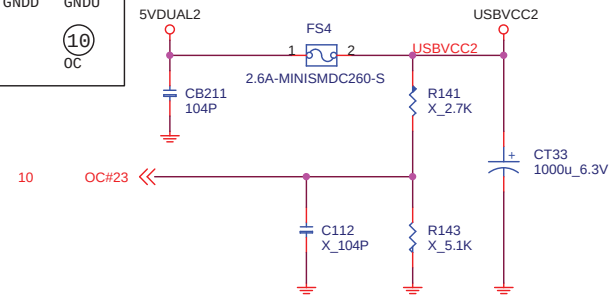
POWER CIRCUIT FOR USB PORT 2,3





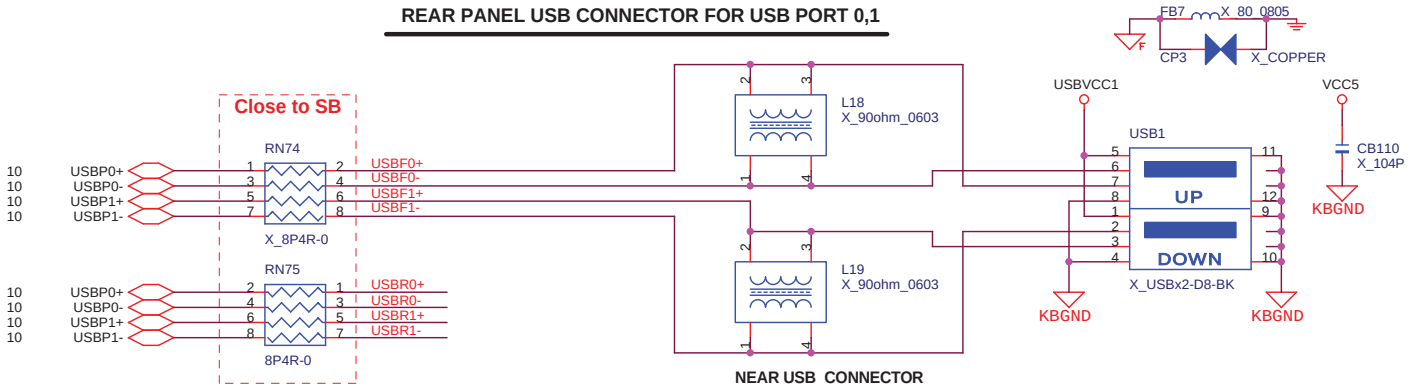
POWER CIRCUIT FOR USB PORT 0,1

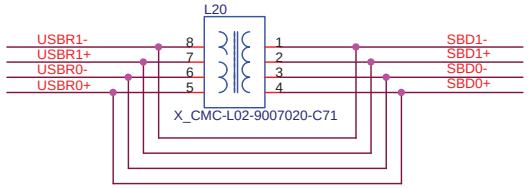
POWER CIRCUIT FOR USB PORT 4,5

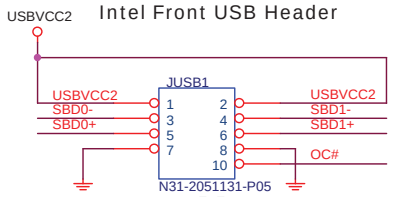


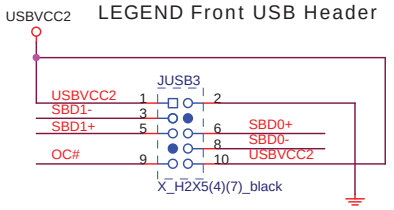
* USB Trace width : 7.5 mils
* USB Trace Spacing : 20 mils
* Differential USB Signlas Trace, Spacing : 7.5 mils
* USB Power Trace must be 50mils width

REAR PANEL USB CONNECTOR FOR USB PORT 0,1



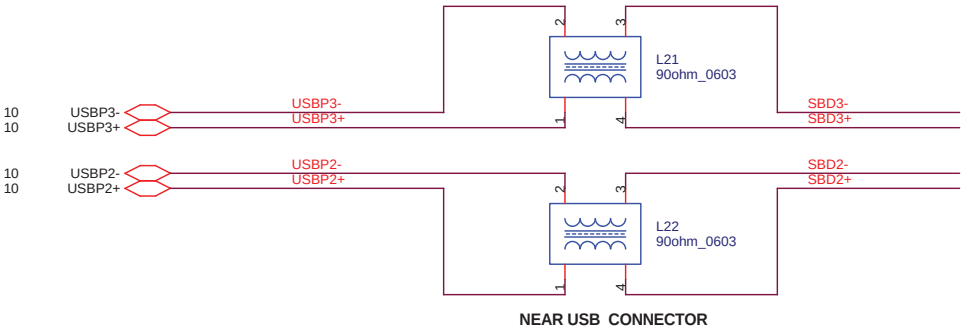


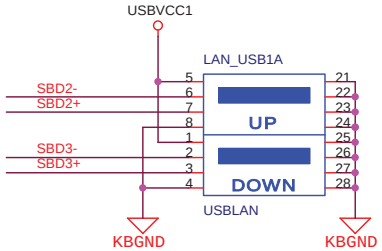




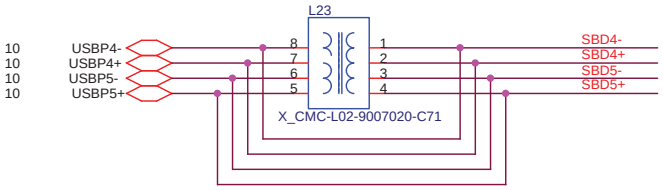
BLACK

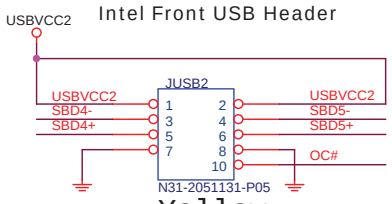
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

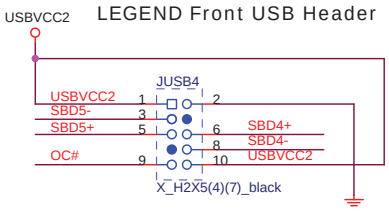


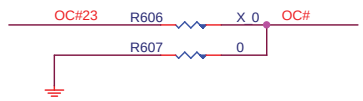


FRONT PANEL USB CONNECTOR FOR USB PORT 4,5









MSI **MICRO-STAR**

Title: USB CONNECTORS

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SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

to Solve MS-5 Can't Power Down(ATX Power-OK issue)

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE OUTPUT 1 AND 2 FOR GPIO FUNCTION

Place close W83302D

I2C ADD = 0x5Eh

PCIRST#1	GMCH, LPC, LAN
PCIRST#2	PCI1, PCI2, PCI3

5V DUAL Power

to Control the slew rate of soft-start

Rear USB ports

Front USB ports

to Solve MS-5 Charge issue

Place near CPU

DDR 2.5V Power

2.5V/2.8A+5.92A

DDR VTT Power

1.25V / 2.1A

AGP 2.5V POWER TRANSLATOR

1.5V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)

For 3VSB OR 3VSTR Setting by SEL1
** Setting 3VSTR then VRAM_2.5 become to 1.25 VREF

SEL1	VRAM	VRAM_2.5_SEN
Hi	3.3VDUAL	2.5V
Tri-State	3.3VSB	2.5V
Lo	3.3VSTR	1.25V
Hi	3VSTR > 2.8V RSMRST# Delay 80ms	

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_USB	Main	Standby	0V
MEM_STR	Main	Standby	0V

MOS	RDS(ON)	Vdss	Vgs	Id	Package	Qg
PHKD6N02LT	20.0m	20V	12V	6A	SO-8	20
P3055LD	90.0m	25V	20V	12A	TO-252	20
P45N02LD	28.0m	25V	20V	45A	TO-252	30
2N7002	7.5	60V	20V	115mA	SOT-23	

MICRO-STAR

Title: ACPI CONTROLLER

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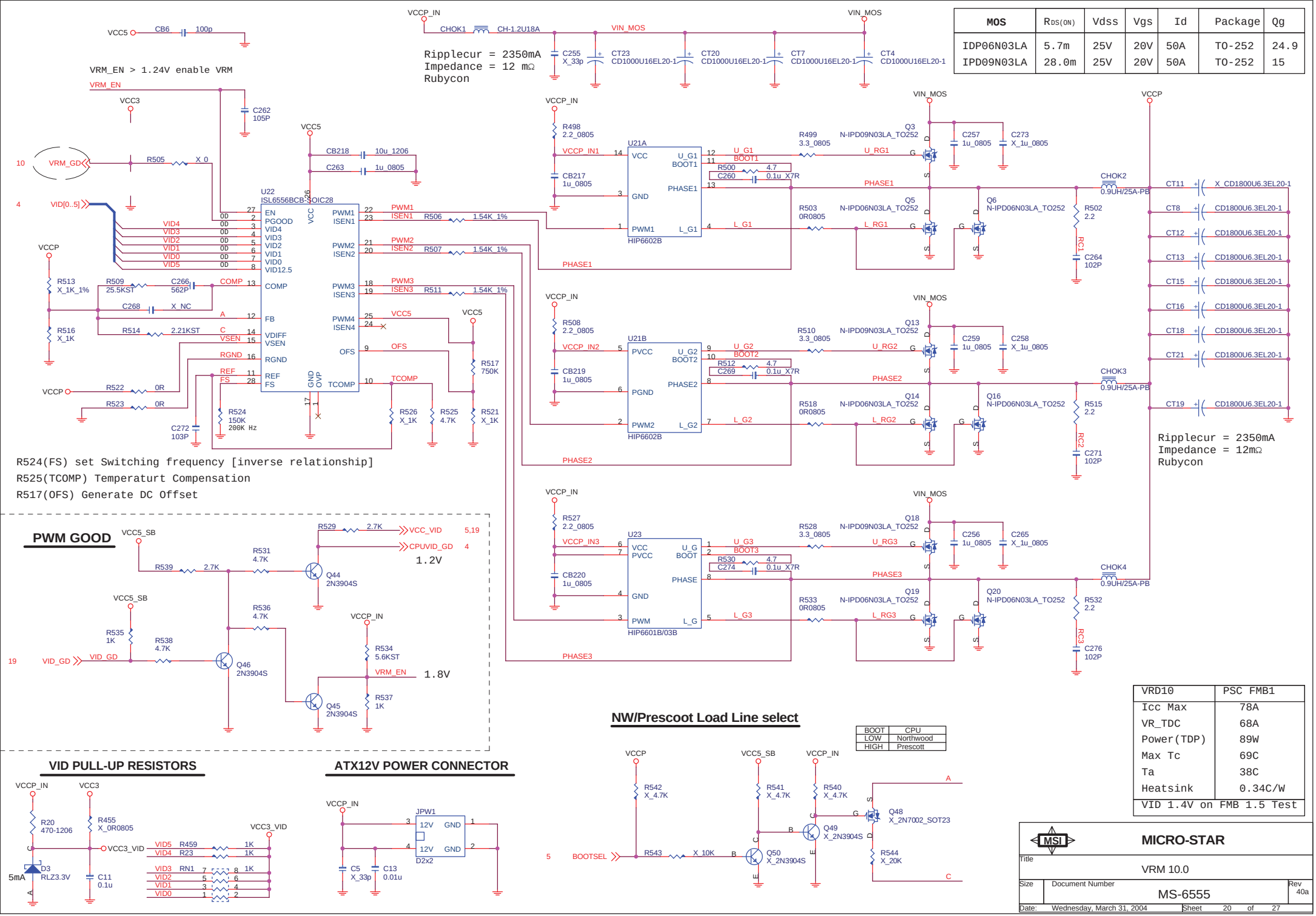

MOS	RDS(ON)	Vdss	Vgs	Id	Package	Qg
IDP06N03LA	5.7m	25V	20V	50A	TO-252	24.9
IPD09N03LA	28.0m	25V	20V	50A	TO-252	15

VRD10	PSC FMB1
Icc Max	78A
VR_TDC	68A
Power(TDP)	89W
Max Tc	69C
Ta	38C
Heatsink	0.34C/W
VID 1.4V on FMB 1.5 Test	

MSI MICRO-STAR

Title: VRM 10.0

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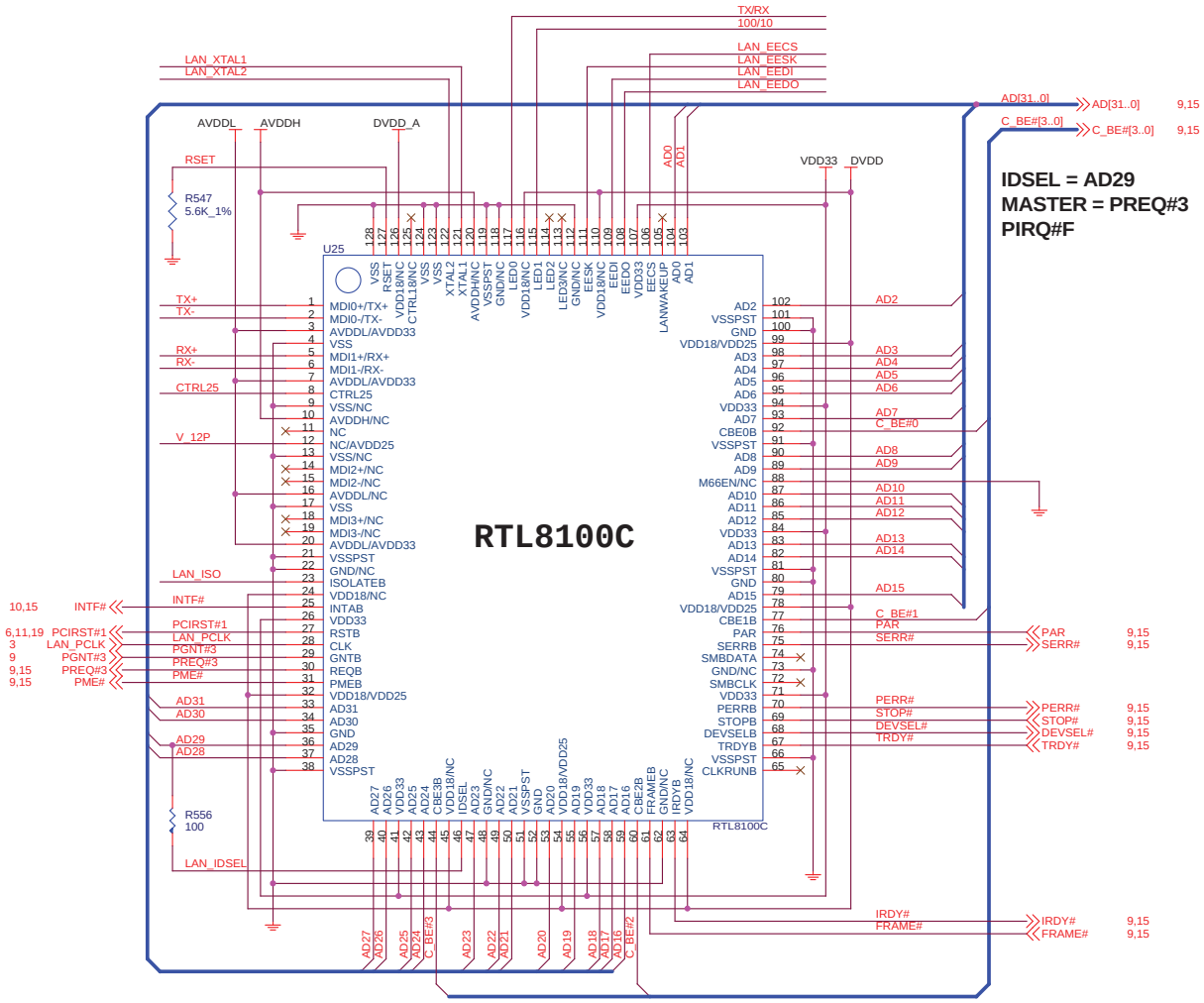
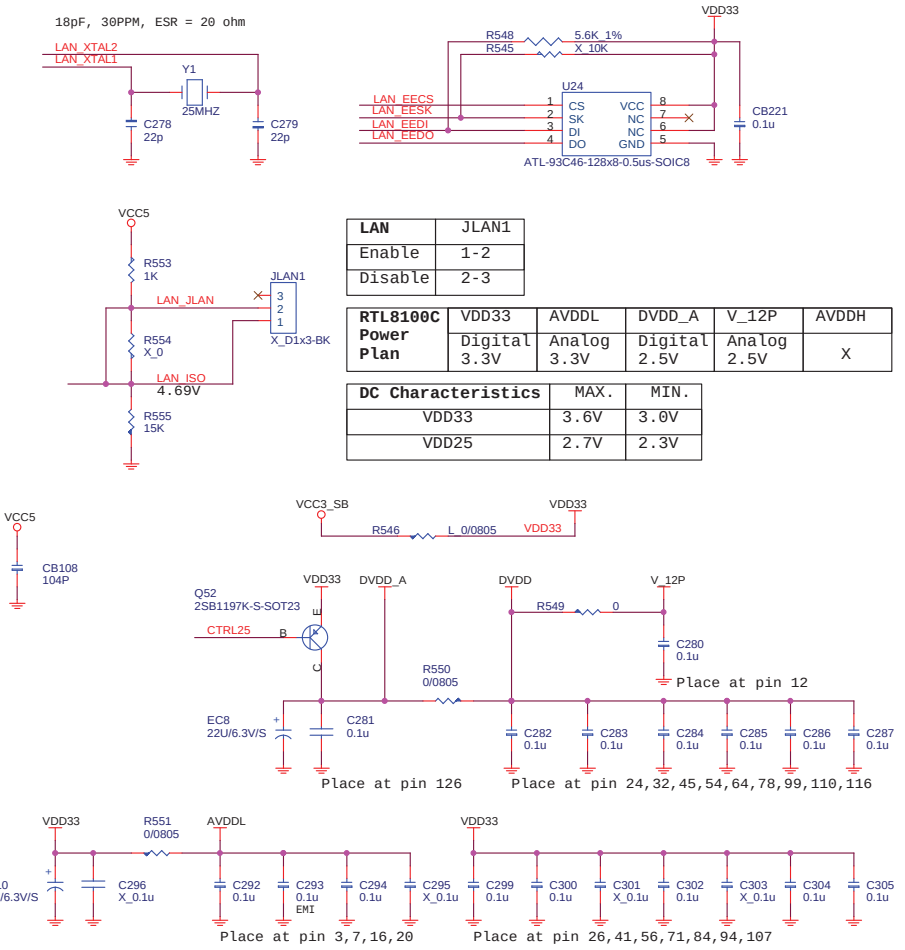


LAN EEPROM



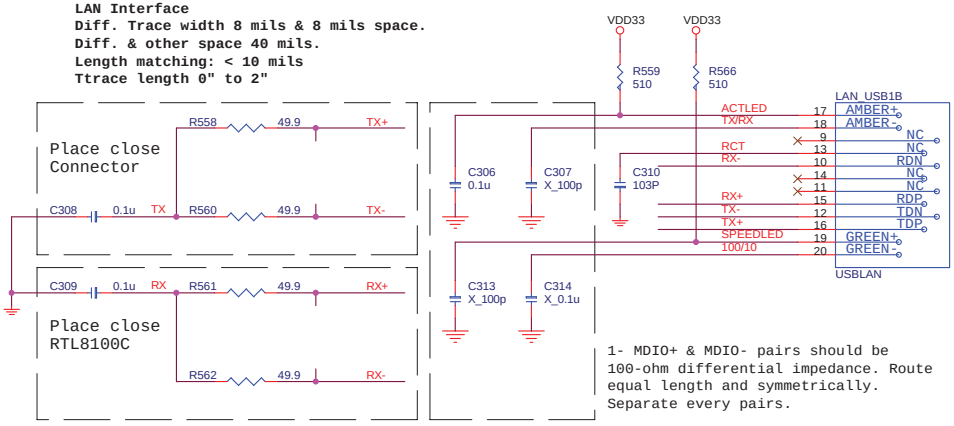
LAN	JLAN1
Enable	1-2
Disable	2-3

RTL8100C Power Plan	VDD33	AVDDL	DVDD_A	V_12P	AVDDH
	Digital 3.3V	Analog 3.3V	Digital 2.5V	Analog 2.5V	X

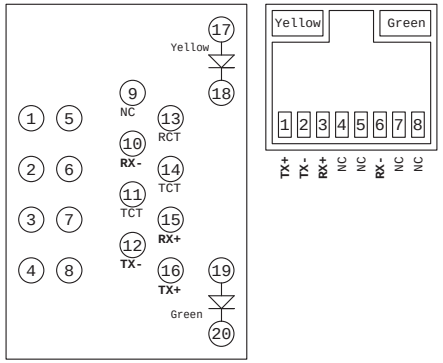
DC Characteristics	MAX.	MIN.
VDD33	3.6V	3.0V
VDD25	2.7V	2.3V

RJ45 Connector (with transformer)

LAN Interface
Diff. Trace width 8 mils & 8 mils space.
Diff. & other space 40 mils.
Length matching: < 10 mils
Ttrace length 0" to 2"

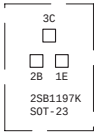


1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.



BJT	hFE	Vce	Vce(sat)	Id	Package
2SB1197K	120	-32V	-0.5V	-0.8A	SOT-23

Part Recommendations
BJT : Ic > 150 mA , hFE > 150 Bead : 100 ohm @ 100Mhz , 300mA Crystal : 50 PPM Magnetic : 350nH @ 8mA



MSI **MICRO-STAR**

Title	LAN REALTEK 8100C	
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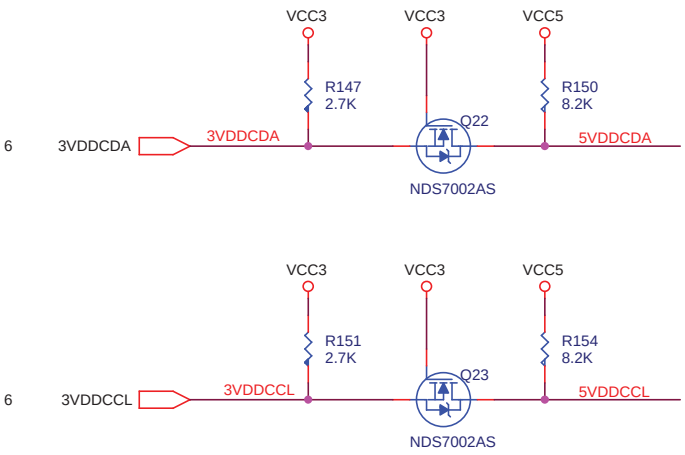
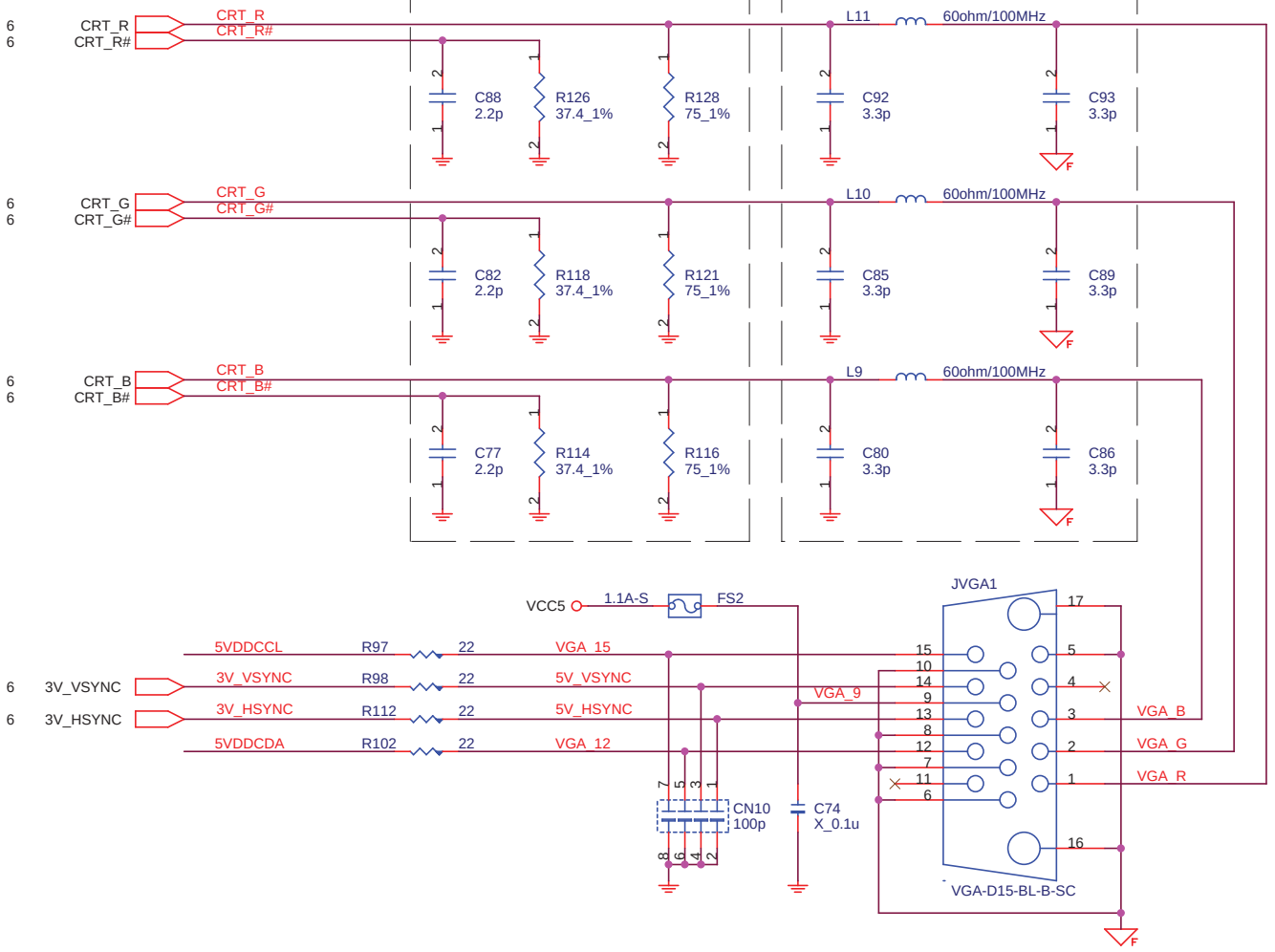
Place termination resistor as close as possible pi-filter

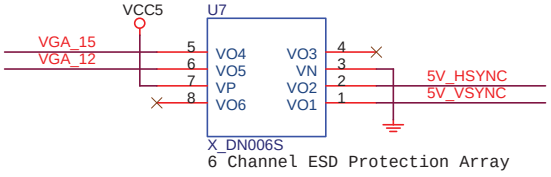
Place CLC Pi-Filter near VGA Connector

Level-Shifting





ESD Protection



MICRO-STAR

Title	VGA CONNECTOR	
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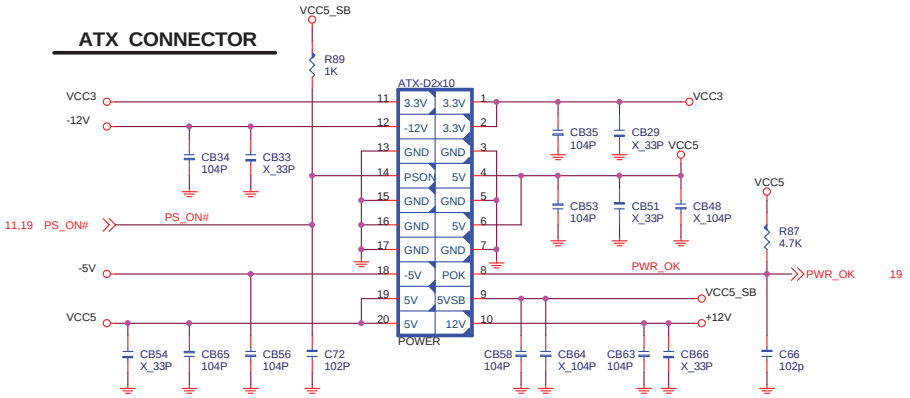
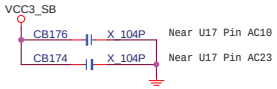
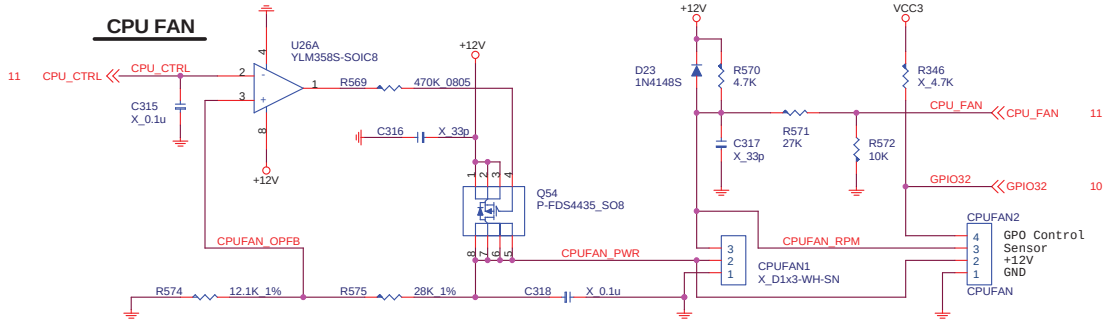
ATX CONNECTOR



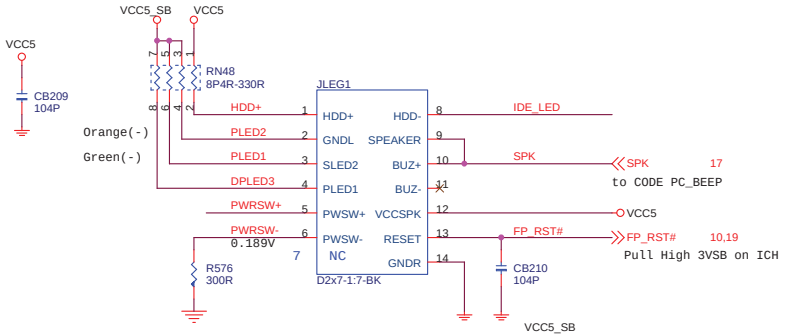
REGULATORS OUTPUT DECOUPLING CAPACITORS



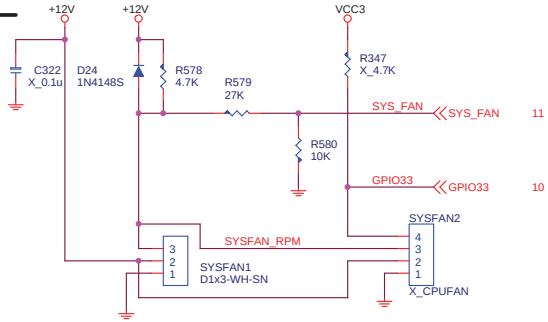
CPU FAN



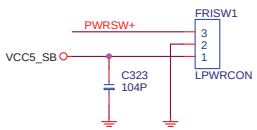
LEGEND FRONT PANEL-M

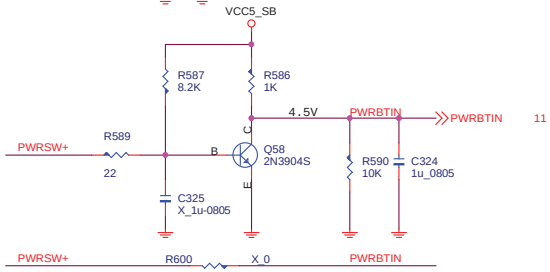


SYSTEM FAN

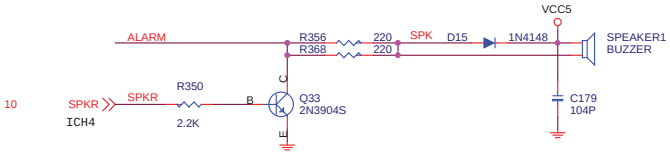


LEGEND POWER SWITCH
Independent Power Switch Header

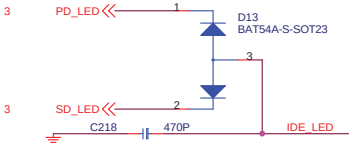


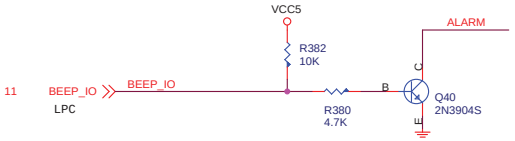


BUZZER

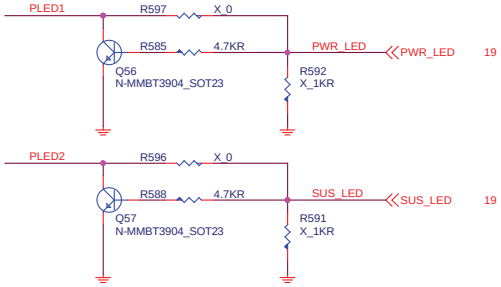


IDE LED





POWER LED



MSI **MICRO-STAR**

Title	Front Panel & ATX Connector & FAN	
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BOM:

A.Audio---
1.DEL JAUDIO1(3-4), JAUDIO1(5-6)
2.ADD JAUDIO1(3-6)
3.DEL FB13
4.ADD C211(ALC655)
5.ADD R357, R361, C223

B.LAN---
1.DEL JLAN1, JLAN1(1-2)

C.I/O---
1.ADD RN76, RN77, R157
2.ADD CB94, CB136

D.PS/2---
1.ADD L1, L2, L3, L4

E.USB---
1.ADD L21, L22
2.DEL CB232

F.LAN---
1.ADD C293

G.PCI---
1.ADD CB157, CB226, CB182, CB225, CB229

H.PWM---
1.Change C264, C271,C276
2.DEL C2
3.ADD C3

I.APIC---
1.Change R184

J.FWN---
1.DEL U19

K.DDR VTT---
1.DEL C71, C53
3.ADD C56

Design:

A.USB---
1.ADD USB Header for Legend

B.S/B---
1.Change GPI 21 to GPIO 34

C.Audio---
1.DEL C217, R358, R359
2.DEL CP11
3.Change CT32(EL) to C202(MLCC)
4.Change C243 Power Pin

D.PCI---
1.ADD R200

E.PWM---
1.DEL R519, R520
2.ADD R538

F.COM2---
1.ADD RN71, R399

G.I/O---
1.ADD L5, R152, CB96

H.FWH---
1.ADD R360, BIOS_TBL1

Layout:

A.USB---
1.Change USB1 USB2 PCB Footprint

B.COM Port---
1.Change COM2 PCB Footprint

C.AUDIO ---
1.ADD AD1888(U28) PCB Footprint

MICRO-STAR		
Title: DIAG LED		
Size: Custom	Document Number: MS-6555	Rev: 40a
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