ZZTOP (MS-6553)

Version 0B
10/16/2001 Update

Nvidia (R) Crush11(nForce IGP 64) + MCP Chipset
AMD Althon/Duron/Palomino Socket 462 Processor

CPU:

AMD Althon/Duron/Palomino Socket 462 Processor

System Chipset:

Nvidia nForce IGP 64 (North Bridge)
MCP Wep (South Bridge)

On Board Chipset:

BIOS -- LPC EEPROM
AC'97 Codec -- AD1885
LPC Super I/O -- LPC47B367
LAN -- ICS1893AF

Expansion Slots:

AGP2.0 SLOT (1.5V) * 1
PCI2.2 SLOT * 3

Intersil PWM:

Controller: HIP6301
Driver: HIP6601 + HIP6602

Regulators

System : SC1544
DDR VTT: CM8500
LDT : IRU3037

MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	COVER SHEET	
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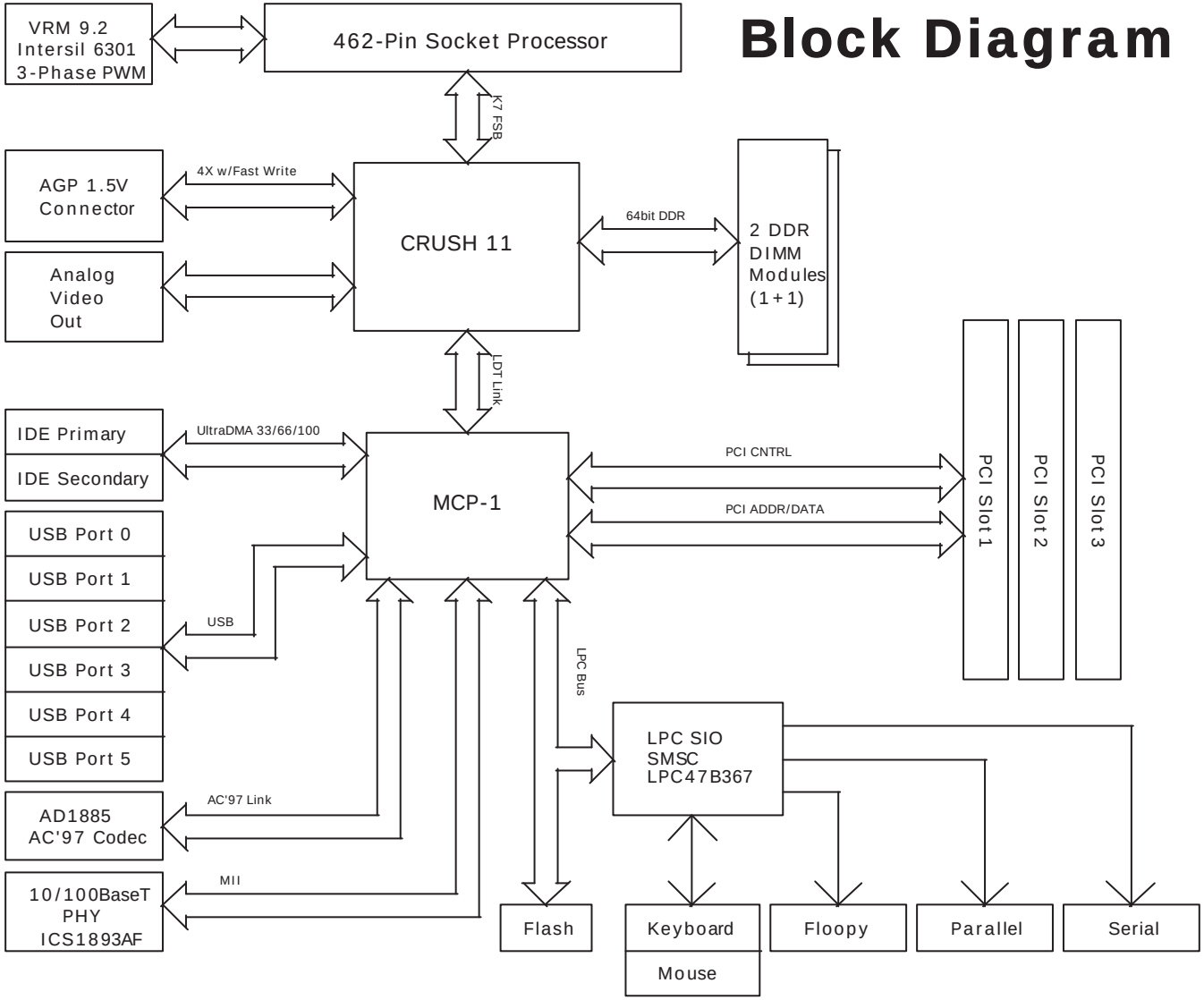
Block Diagram



MSI	MICRO-STAR INt'L CO., LTD.	
	H/W Project Leader : Andy Chen	
	H/W Project Engineer : Prudence Wang	
Title	BLOCK DIAGRAM	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
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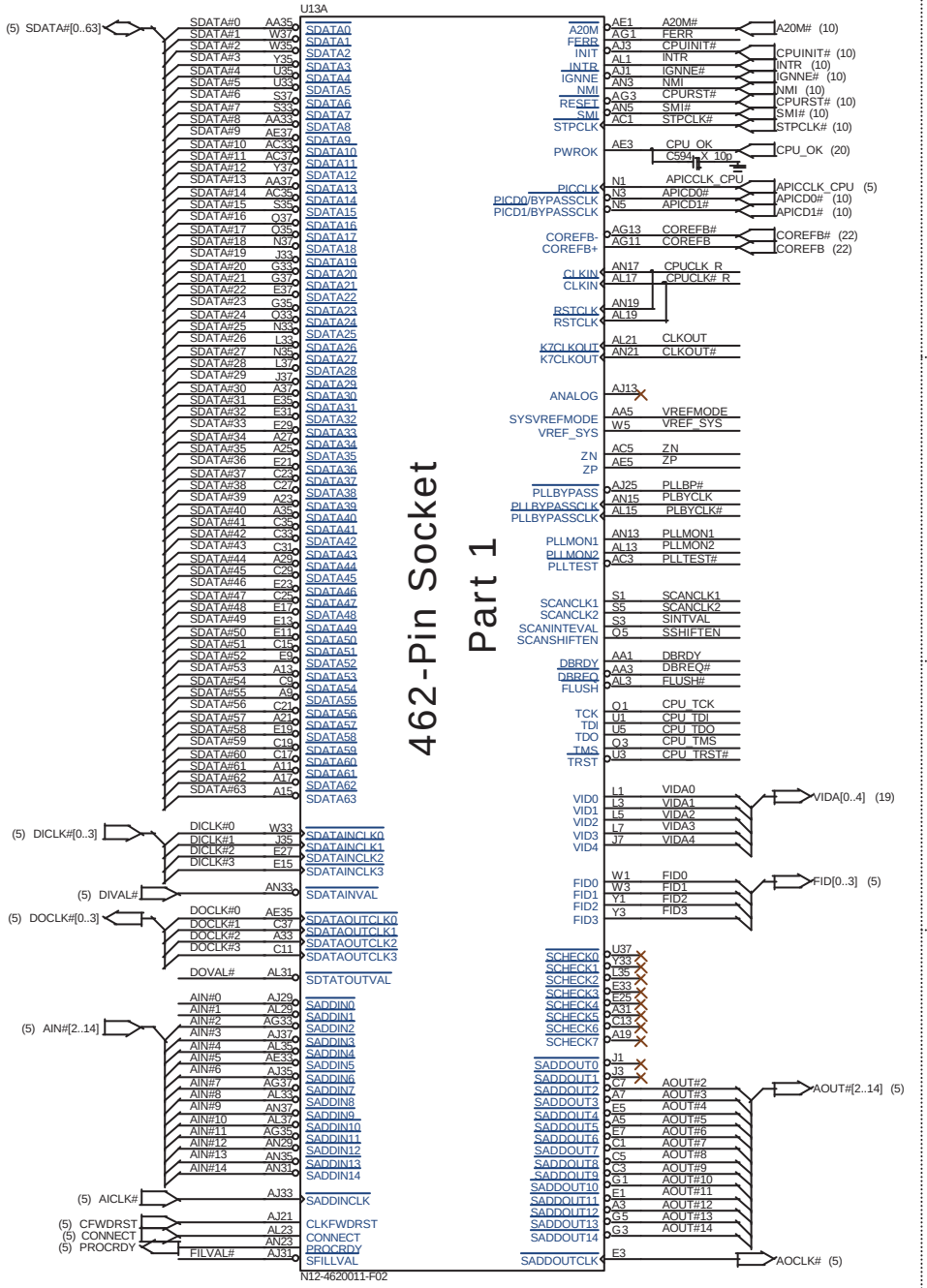
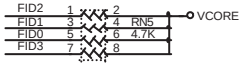
CPU SIGNAL BLOCK



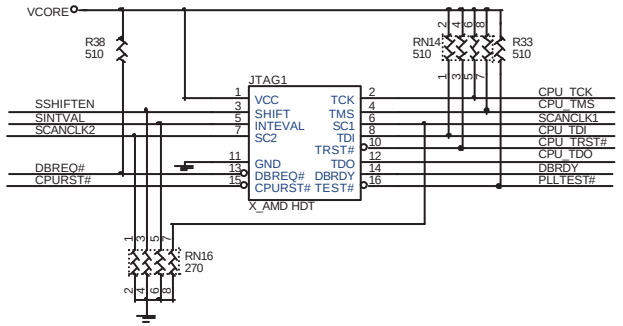
****All CPU interface are 2.5V tolerant****

CPU Clock Multiplier

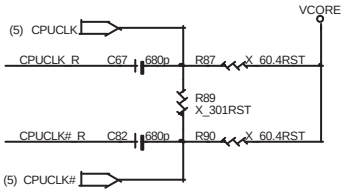


CFID[3:0] => CPU Clock Multiplier

AMD HDT Debug Port

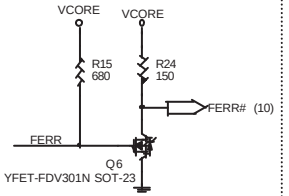


CPU SYSCLK BLOCK



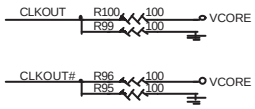
CLOSE SOCKET462

CPU FERR BLOCK



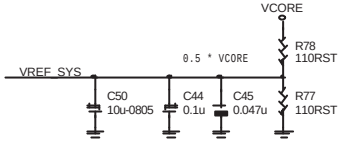
Measure FERR# & IGNNE Delay Time

CPU K7CLKOUT BLOCK



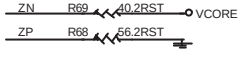
**** Trace lengths of CLKOUT and CLKOUT# are between 2" and 3"***

CPU SYSCLK REFERNCE BLOCK



CLOSE SOCKET462

CPU ZN / ZP BLOCK

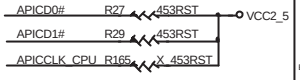


CLOSE SOCKET462

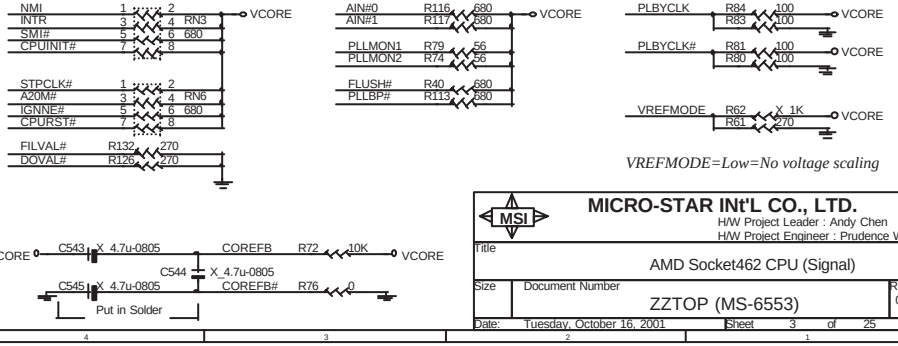
match the transmission line

Push-pull compensation circuit

CPU APIC BLOCK



CPU PULL-UP / DOWN BLOCK



VREFMODE=Low=No voltage scaling

MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title	AMD Socket462 CPU (Signal)	
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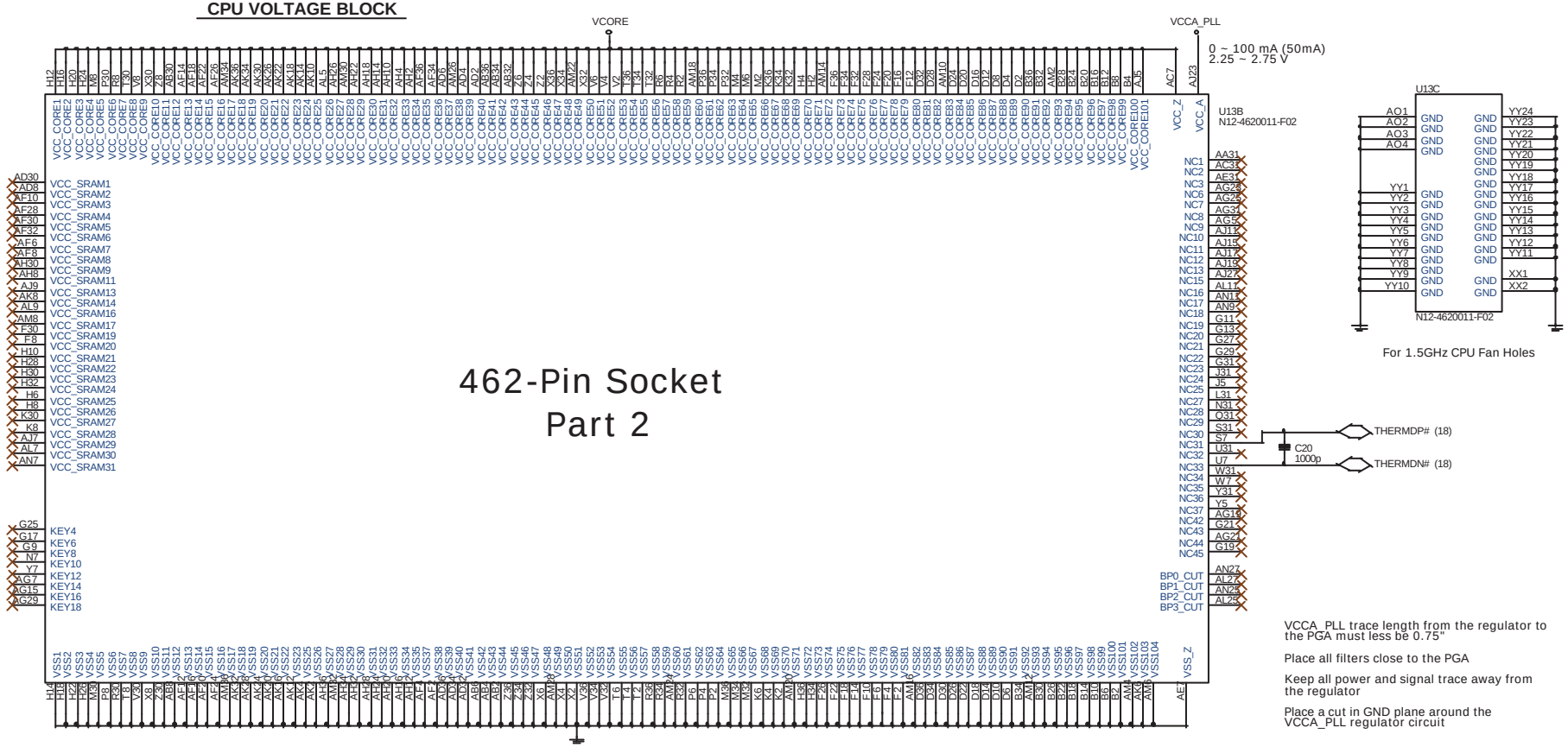
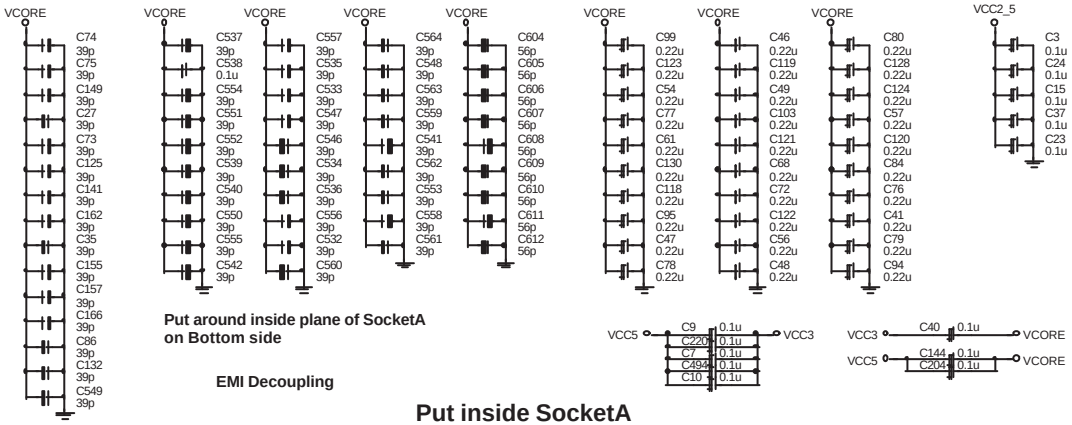
CPU VOLTAGE BLOCK

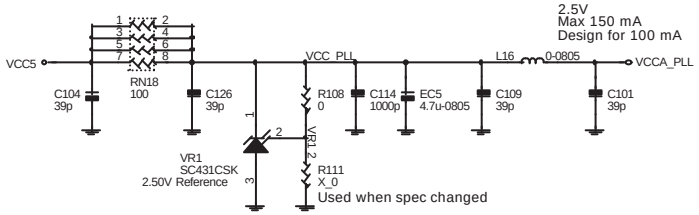


CPU DECOUPLING CAPACITORS



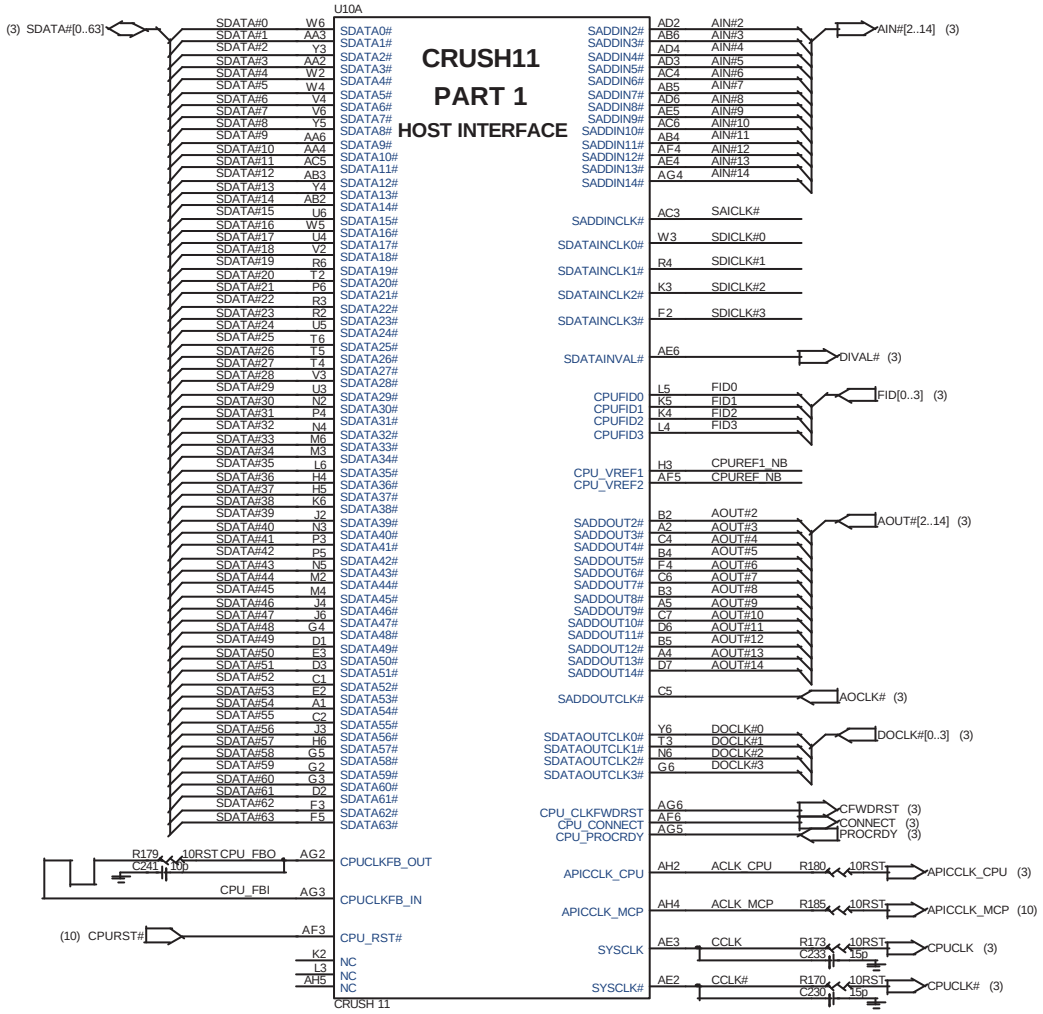
CPU PLL VOLTAGE BLOCK

(40mils trace / 60 mils space)

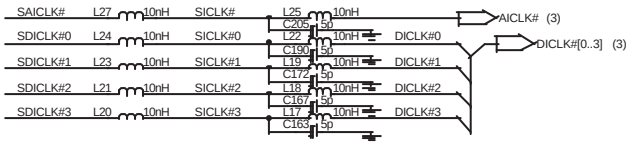


MSI	MICRO-STAR INt'L CO., LTD.
	H/W Project Leader : Andy Chen
	H/W Project Engineer : Prudence Wang
Title	AMD Socket462 CPU (Power)
Size	Document Number: ZZTOP (MS-6553) Rev: 0B
Date: Tuesday, October 16, 2001	Sheet 4 of 25

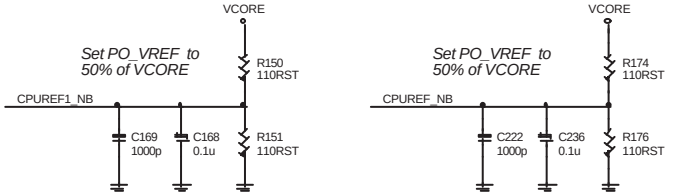
CRUSH 11 HOST SIGNALS



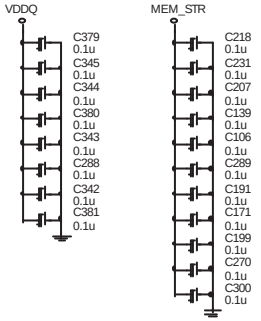
SYSTEM DATA-IN-CLK NOISE L/C BLOCK



REFERNCE VOLTAGE BLOCK



Crush 11 Decoupling Capacitors



BELONG TO CLKFWD GROUP[SADDIN] MATCH W/IN +/-10MILS OF GROUP 5/15, CLK:10/30

BELONG TO CLKFWD GROUP[SADDOUT] MATCH W/IN +/-10MILS OF GROUP 5/15, CLK:10/30

BELONG TO CLKFWD GROUP;MATCHED TO INDIVIDUAL CLKFWD GROUP

RESPECTIVELY.[SDATA0], [SDATA1], [SDATA2],[SDATA3] W/IN+/-10MILS OF GROUP

MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: Crush11 Host Signals

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CRUSH 11 MEMORY SIGNALS

CRUSH11

PART 2

SYSTEM MEMORY

U10B
CRUSH 11

DDR Terminational Resisitors

VTT_DDR2

DDR Dampping Resisitors

DDR REFENCE VOLTAGE

MEM_STR
R43 110RST
R42 110RST
DDR2_VREF
DDR2_VREF (14)

Put near DIMM

30mils Trace/45mils Space

(14) MA_B[0..12]

(14) MA_A[0..12]

MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title: Crush11 Memory Signals

Size | Document Number: ZZTOP (MS-6553) | Rev: 0B

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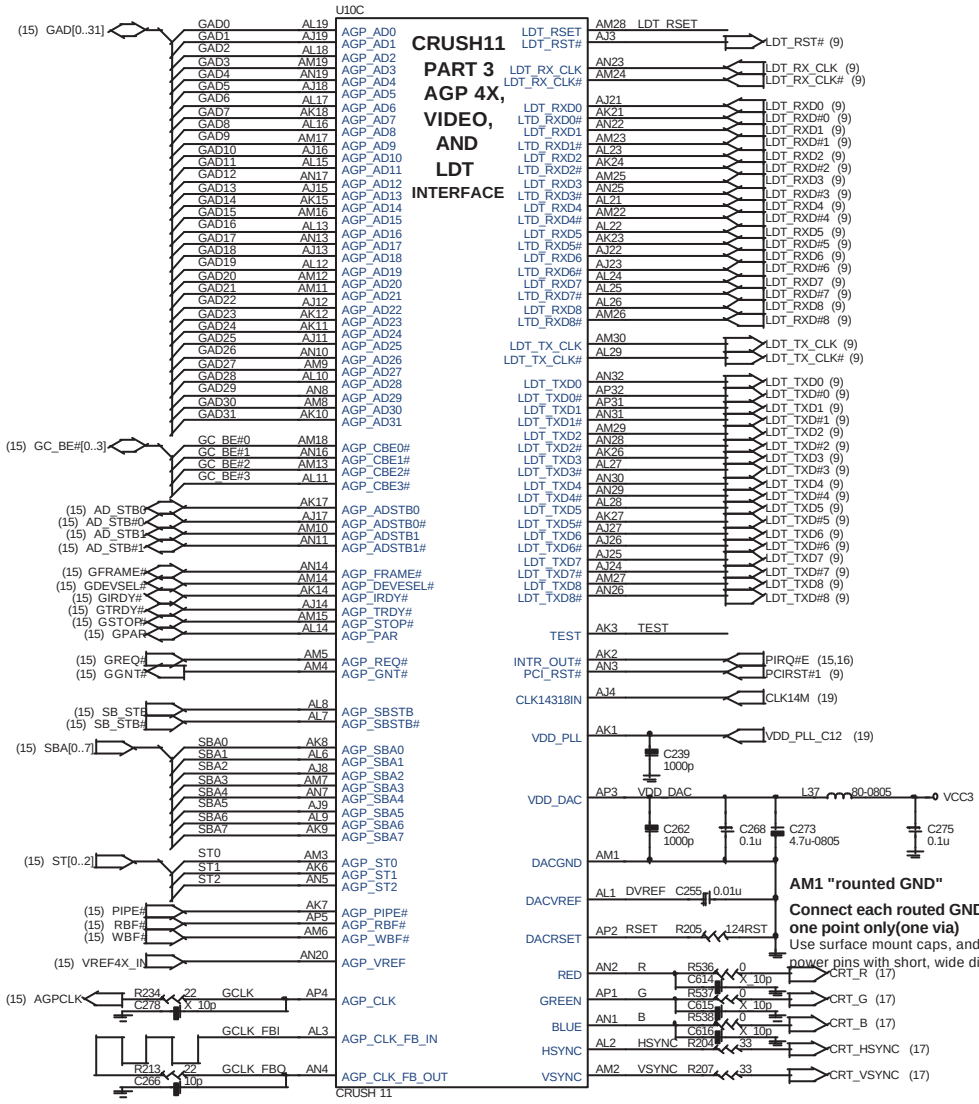
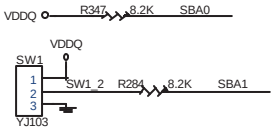
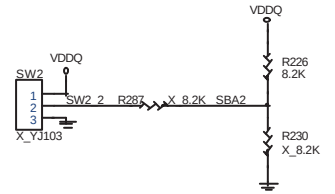
CRUSH 11 AGP & LDT SIGNALS



CRUSH 11 Strapping Resistors

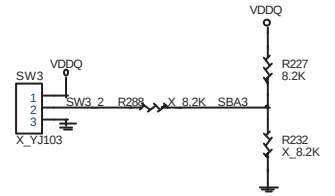


Host Freq.	SBA1	SBA0
100MHz	0	1
133MHz	1	1



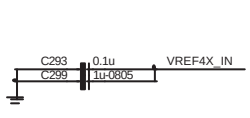
0 = Use values stored in ROM tables.
1 = AUTO detect by reading SBA[1:0]

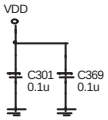
FSB Set.	SBA2
ROM	0
AUTO	1



0 = "SAFE" mode table
1 = USER defined table

FSB Mode	SBA3
SAFE	0
AUTO	1





MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: Crush11 AGP & LDT Signals

Size | Document Number: ZZTOP (MS-6553) | Rev: 0B

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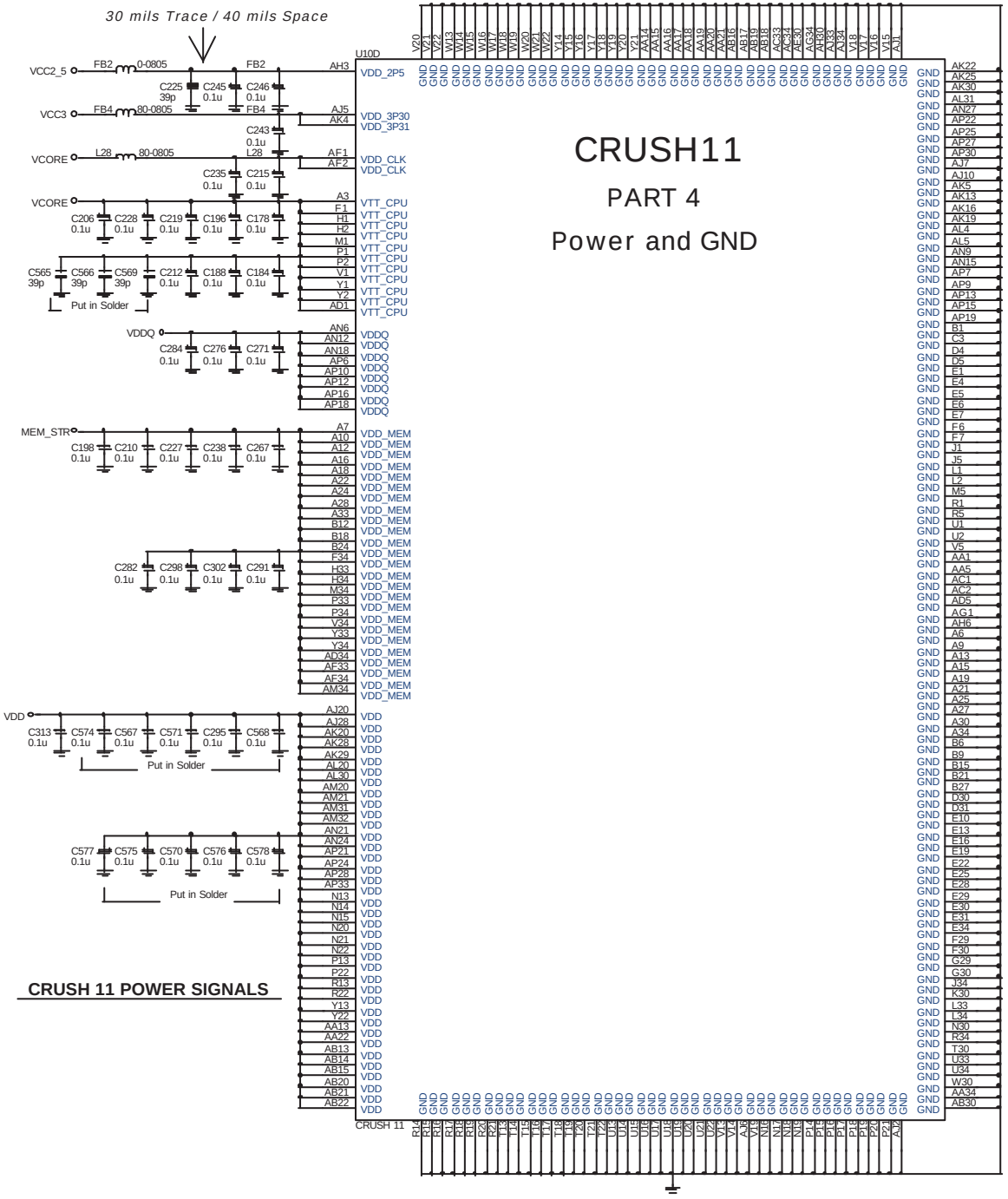
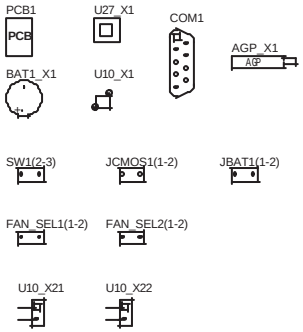
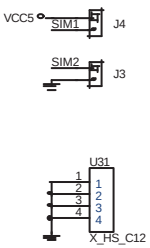


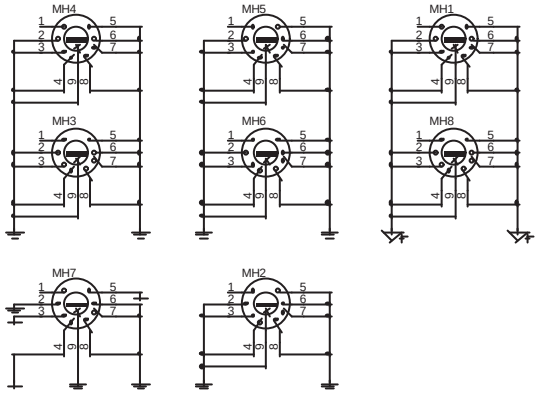
Auto-BOM Manual Parts



Simulation



Mounting Holes



MSI	MICRO-STAR INt'L CO., LTD.	
	H/W Project Leader : Andy Chen	
	H/W Project Engineer : Prudence Wang	
Title	Crush11 Power Signals	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
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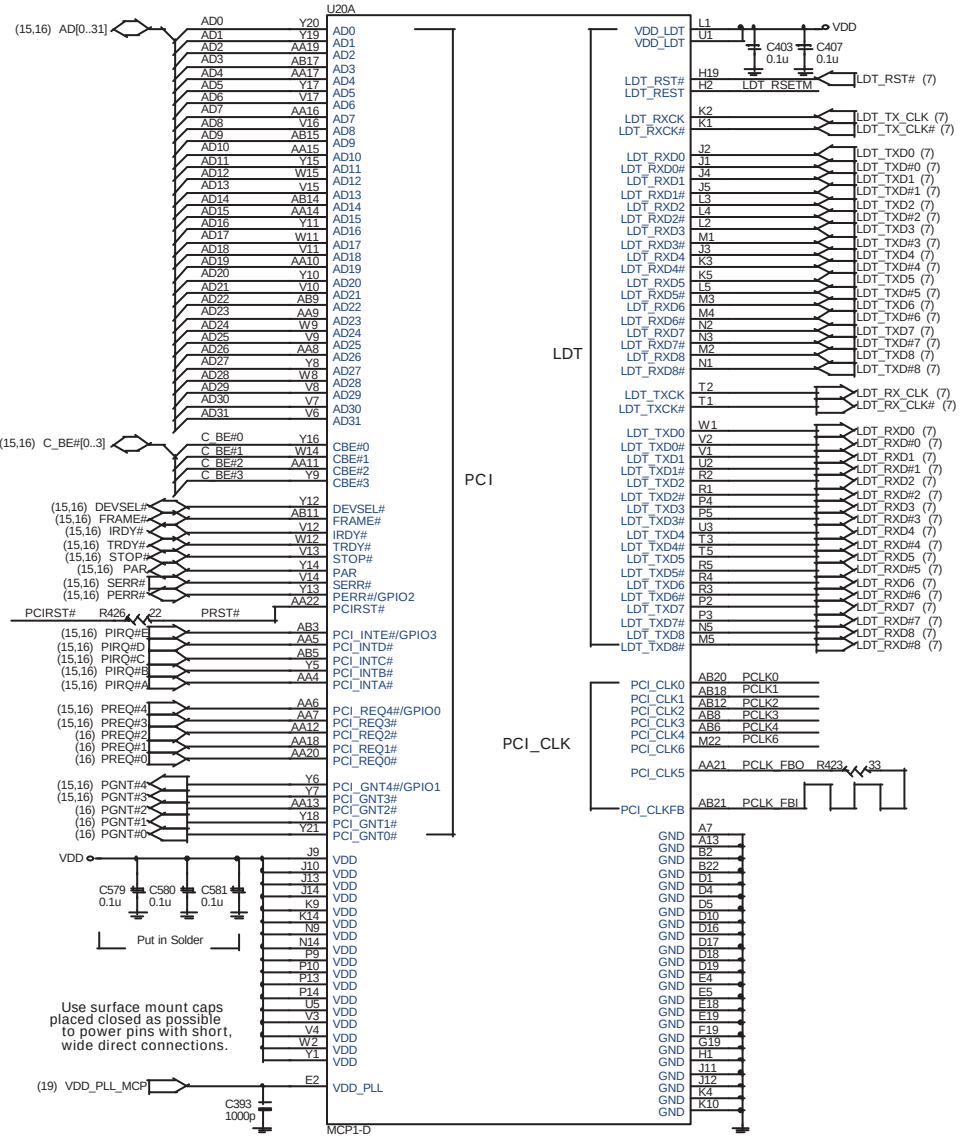
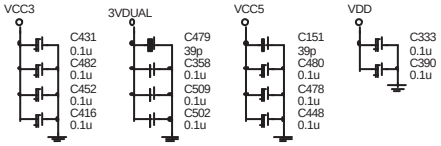
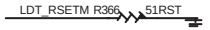
MCP PCI & LDT SIGNALS



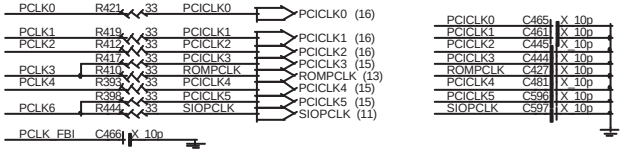
MCP Decoupling Capacitors



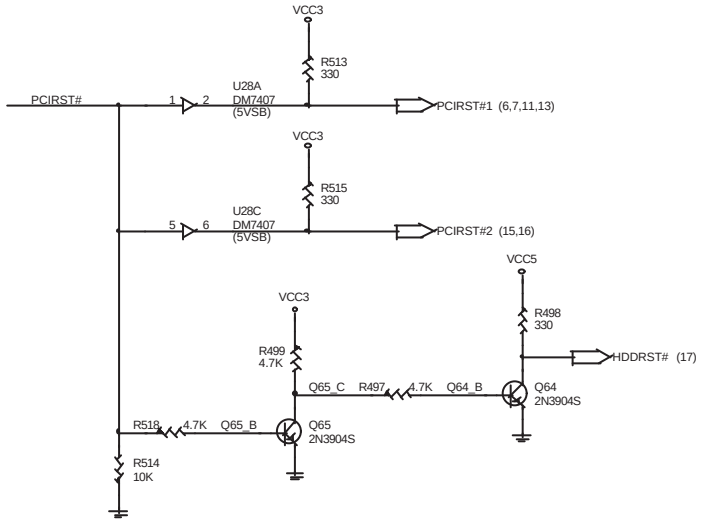
MCP LDT SET Resistors



MCP PCI Clock Dampping Resistors & Capacitors



PCI RESET LOGIC



MICRO-STAR INt'L CO., LTD.		
H/W Project Leader : Andy Chen		
H/W Project Engineer : Prudence Wang		
Title: MCP PCI & LDT Signals		
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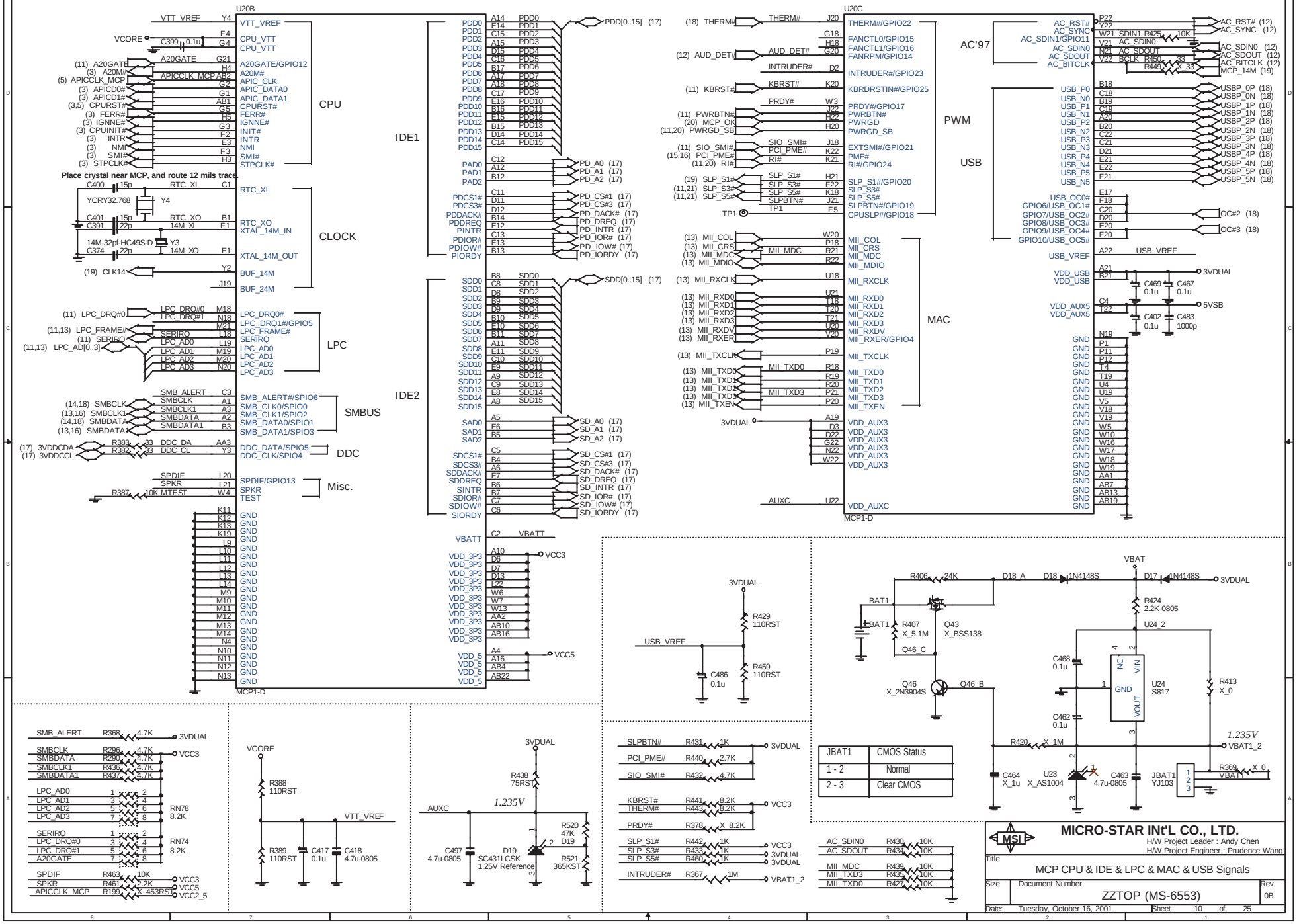
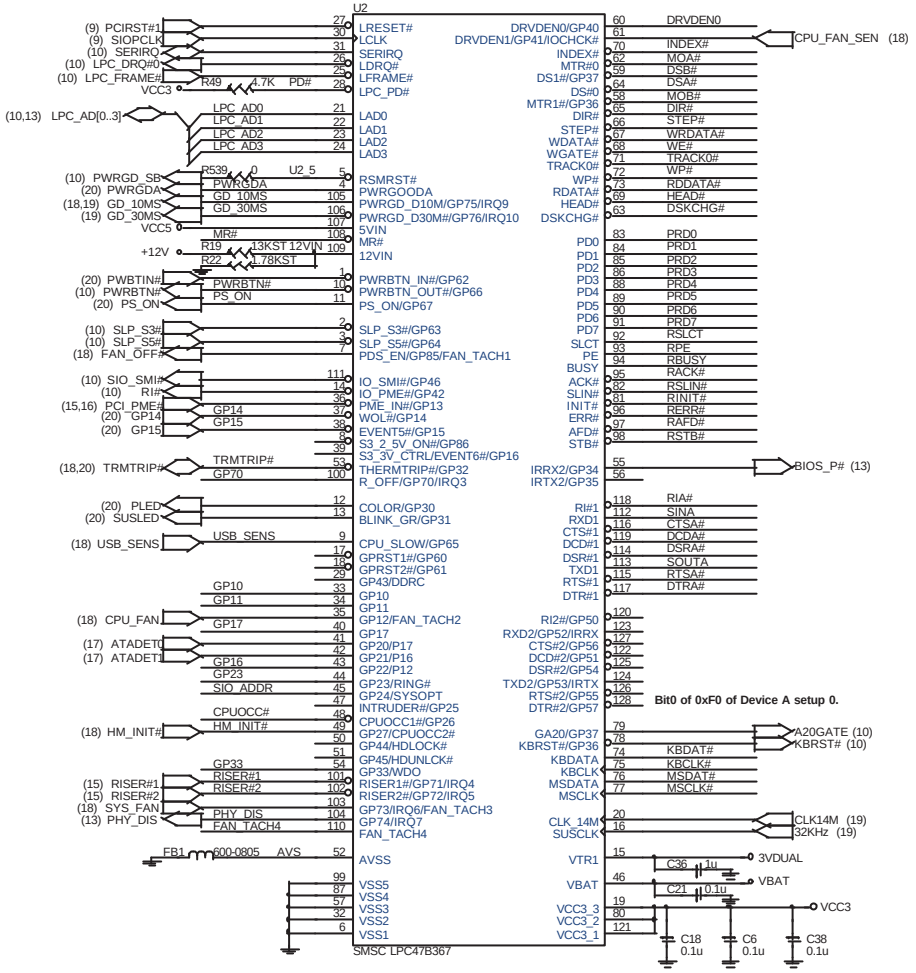
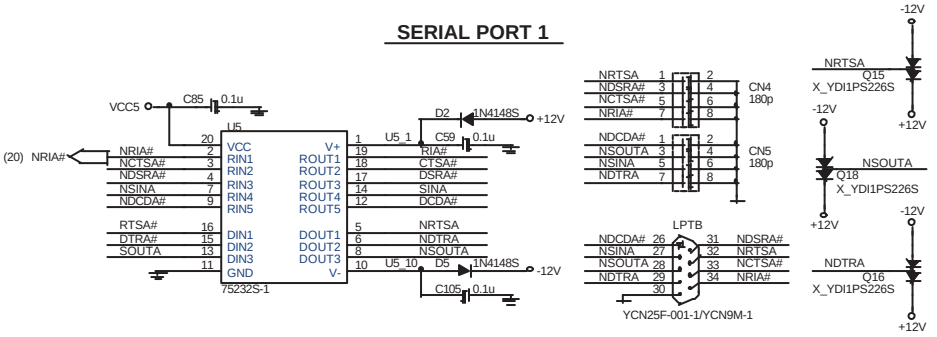
MCP PCI & LDT SIGNALS



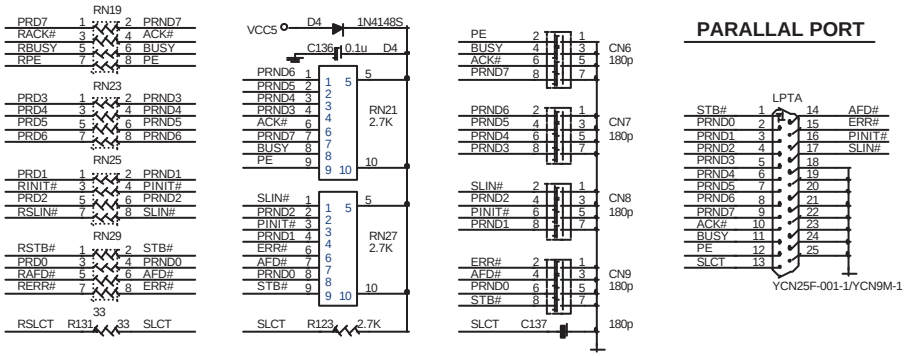
LPC SUPER I/O LPC47B367



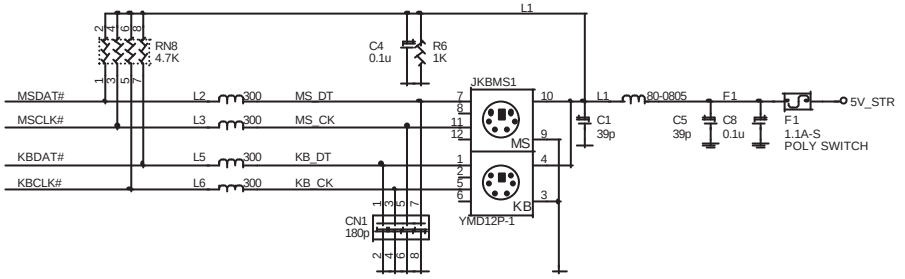
SERIAL PORT 1



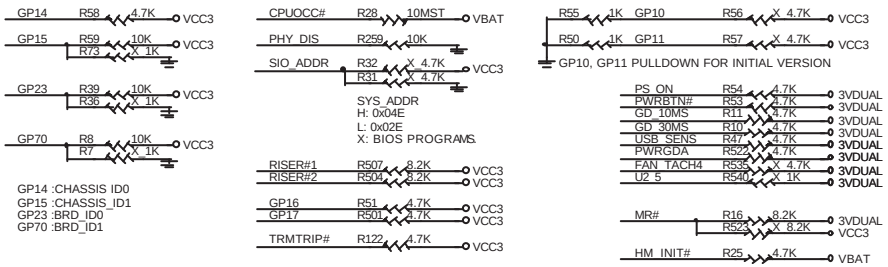
PARALLAL PORT



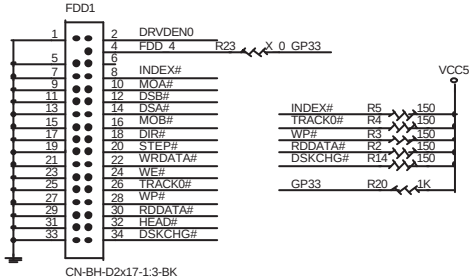
PS2 KEYBOARD & MOUSE CONNECTOR



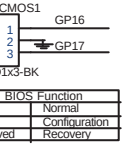
LPC I/O STRAPPING RESISTOR



FLOPPY CONNECTOR

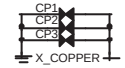


CMOS CLEAR



BIOS Function	
1-2	Normal
2-3	Configuration
Removed	Recovery

COPPER



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: LPC SUPER I/O & CONNECTORS

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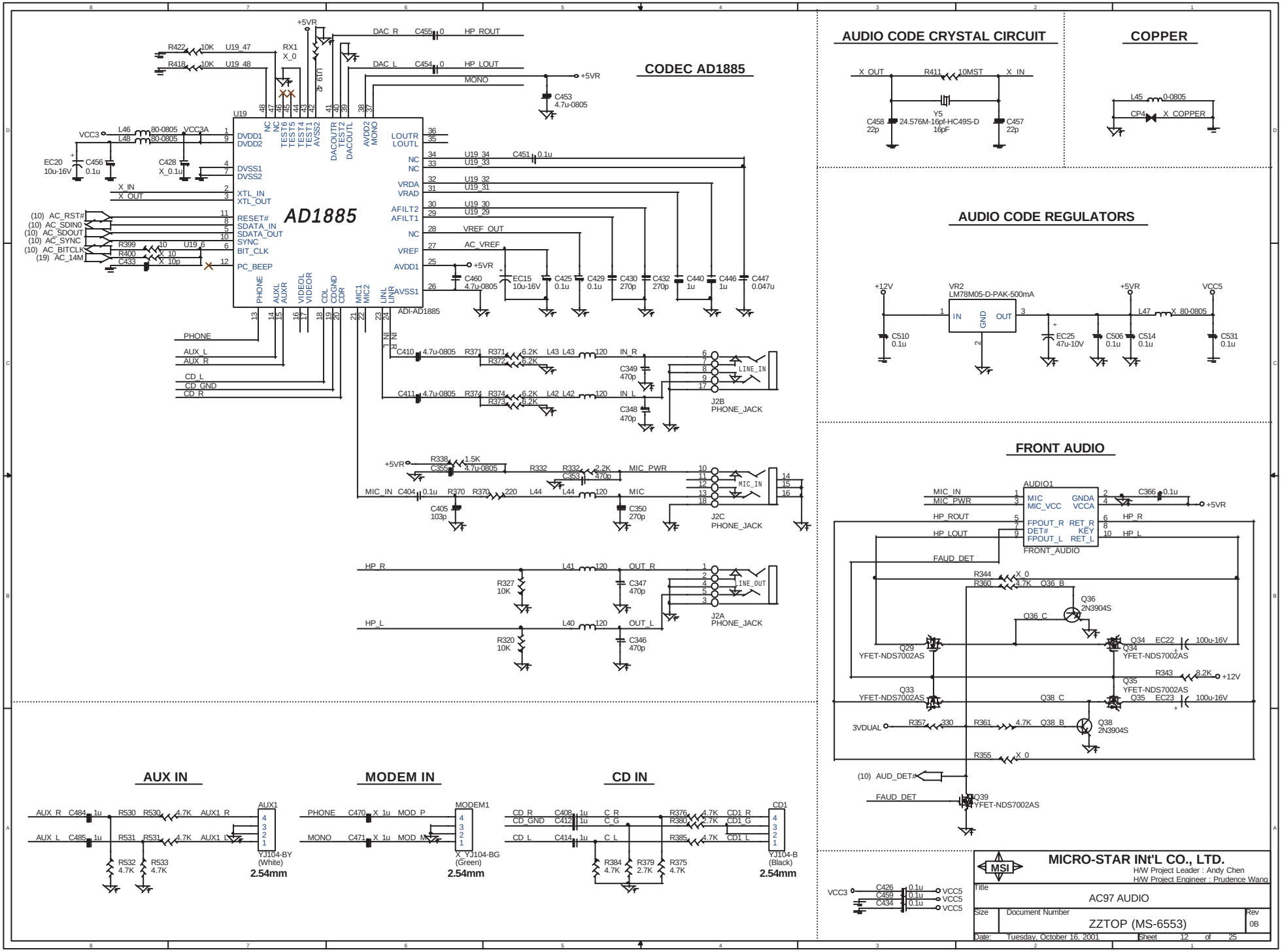
CODEC AD1885
AD1885
ADI-AD1885
AUDIO CODE CRYSTAL CIRCUIT
COPPER
AUDIO CODE REGULATORS
FRONT AUDIO
AUX IN
MODEM IN
CD IN
MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
AC97 AUDIO
ZZTOP (MS-6553)
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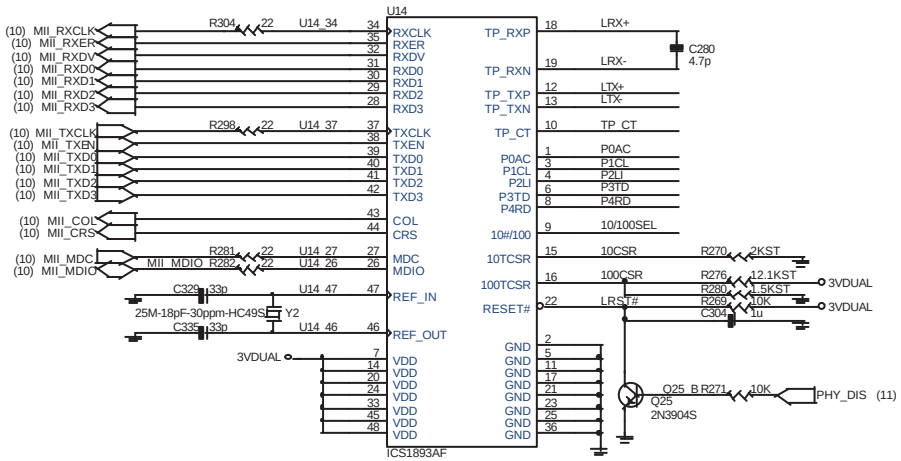
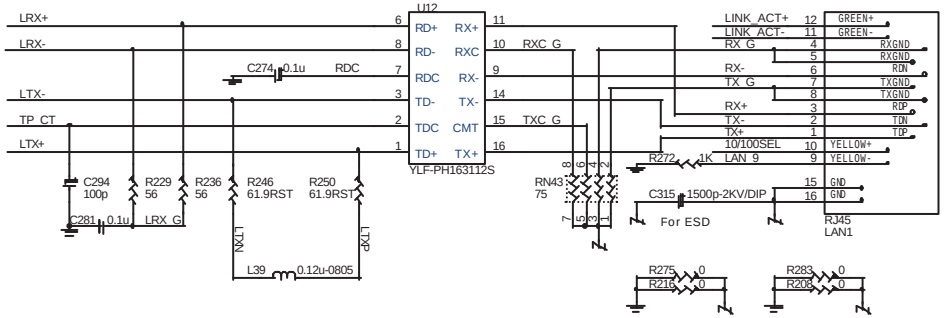
LAN ICS1893AF

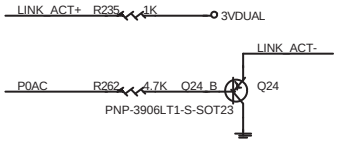


RJ45 Connector

Trace from RJ45 to Transformer must less than 1 inch.

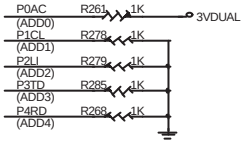


Active LED Block



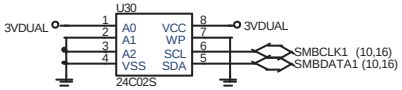
MDIO Strapping

PHY Adress Starpping

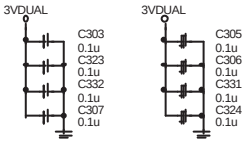


PHY Address = 00001

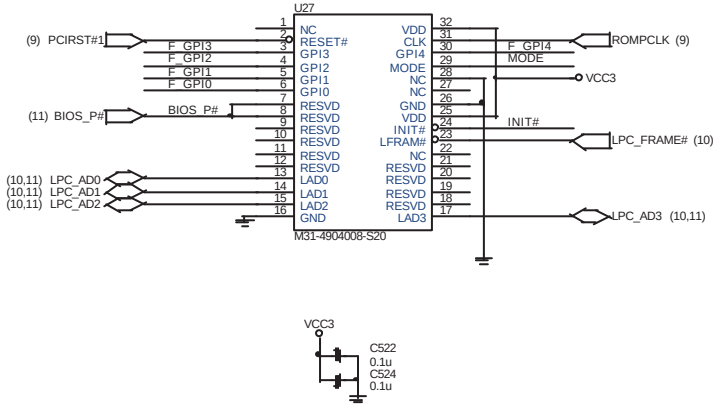
LAN EEPROM



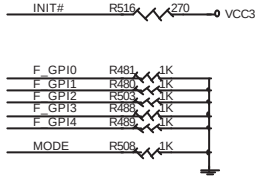
LAN Decoupling Capacitors



LPC Flash EEPROM

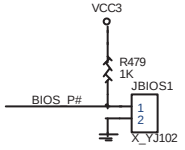


EEPROM Strapping Resistors



Interface MODE Selection		
HIGH	Programmer mode	
LOW	LPC mode	Default

BIOS PROTECT BLOCK



BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

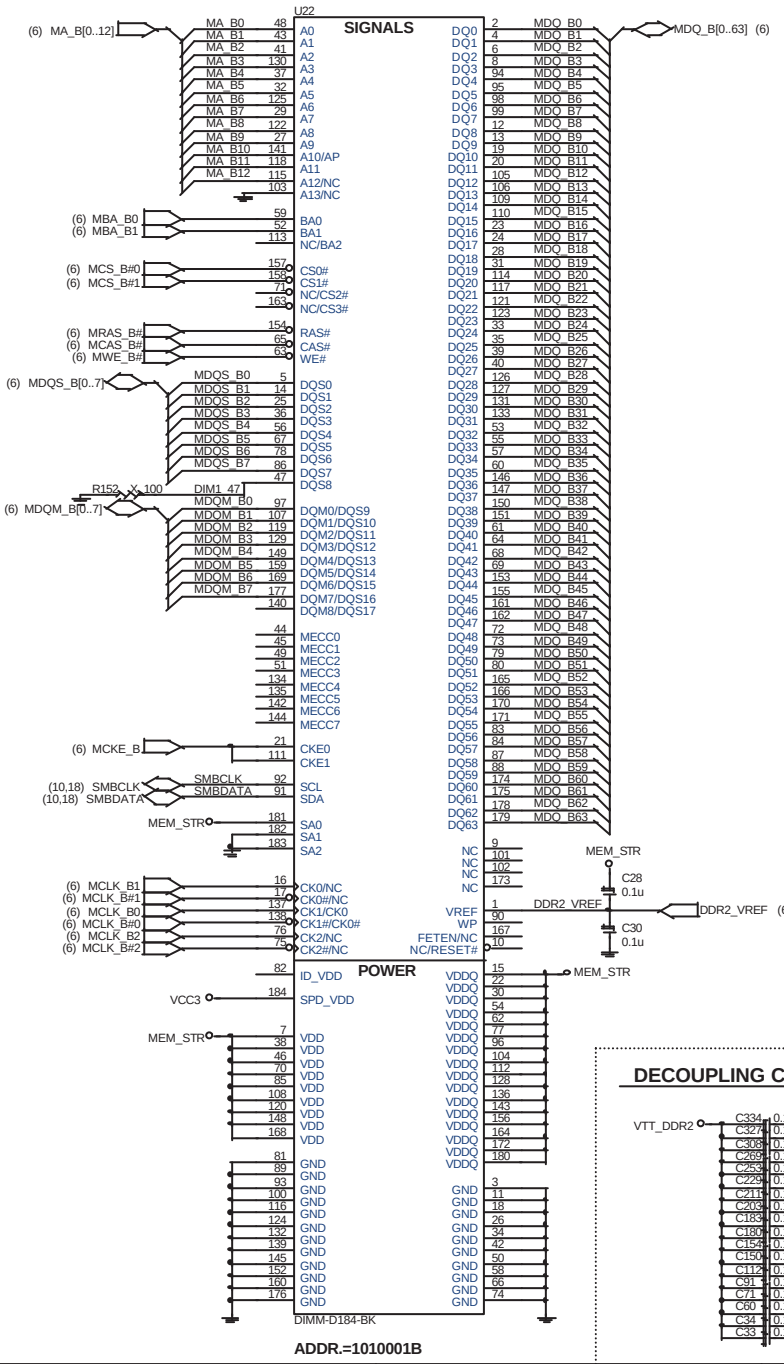
H/W Project Engineer : Prudence Wang

Title: LAN ICS1893AF & LPC Flash EEPROM

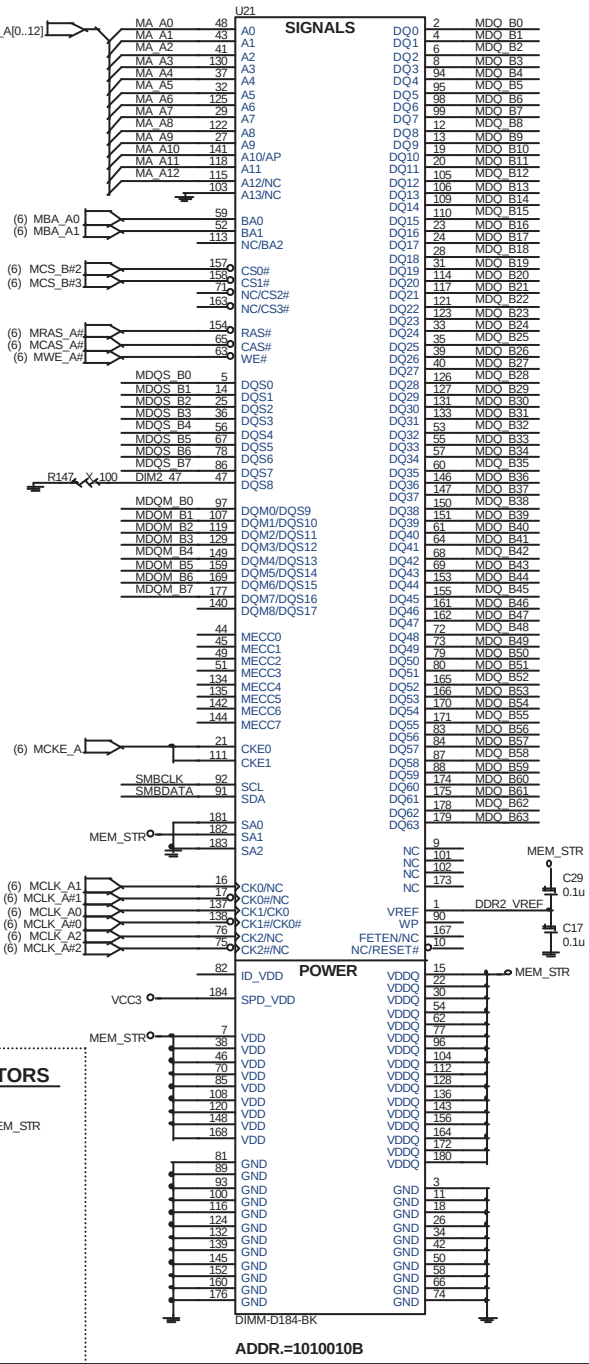
Size | Document Number: ZZTOP (MS-6553) | Rev: 0B

Date: Tuesday, October 16, 2001 | Sheet 13 of 25

DDR DIMM1

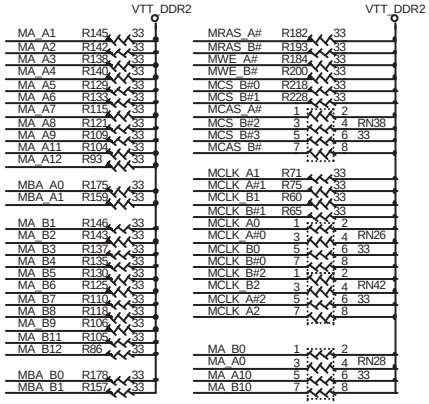


DDR DIMM2

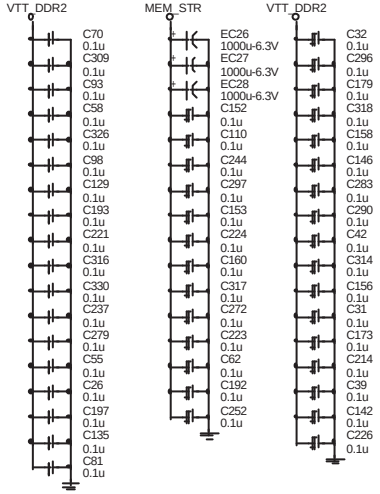


DECOUPLING CAPACITORS

DDR Terminational Resisitors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.

One decoupling capacitor for each R-pack.

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

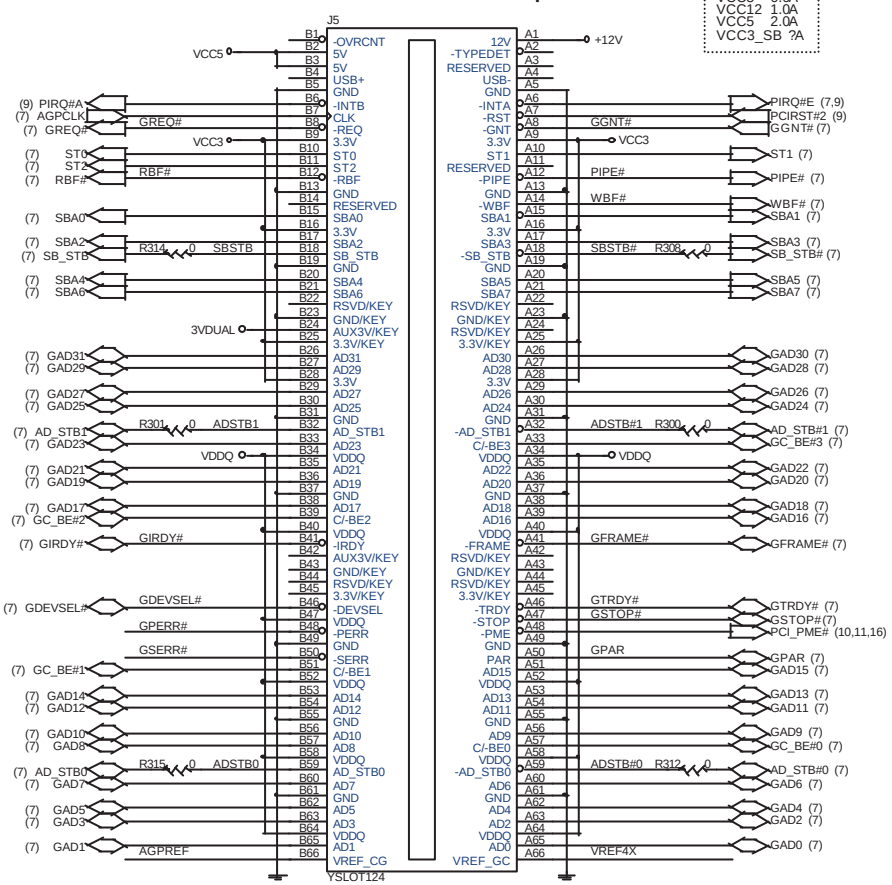
Title	DDR DIMM 1 & 2	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
Date: Tuesday, October 16, 2001	Sheet 14 of 25	

AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

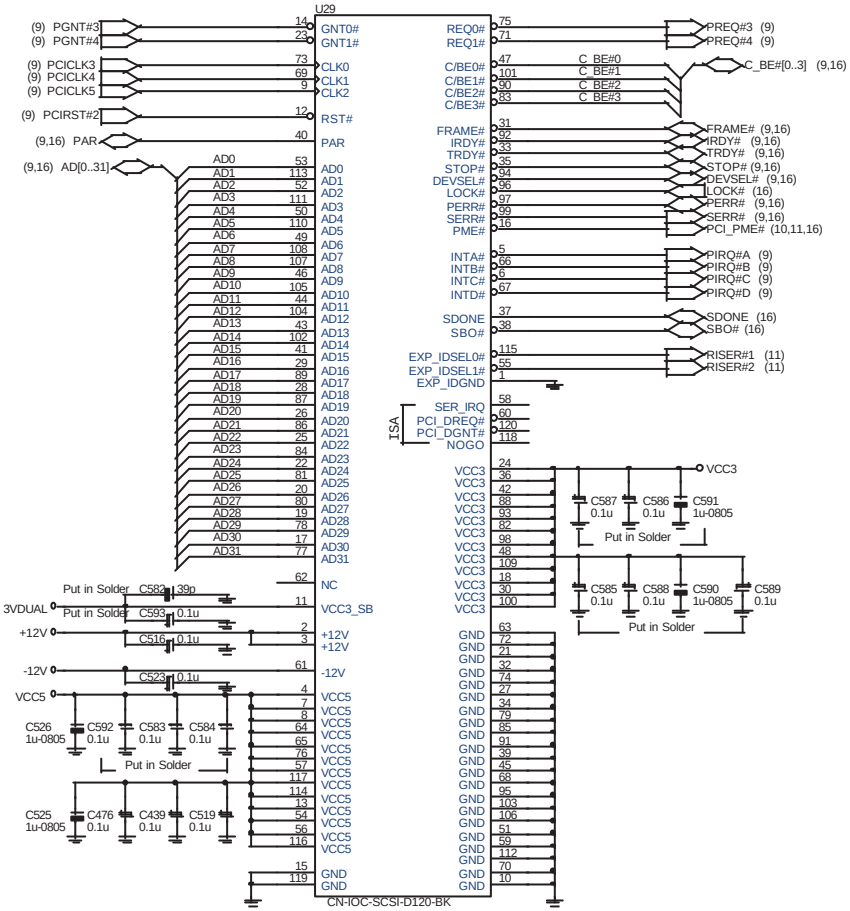
AGP Slot Imax

VCCg	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	?A

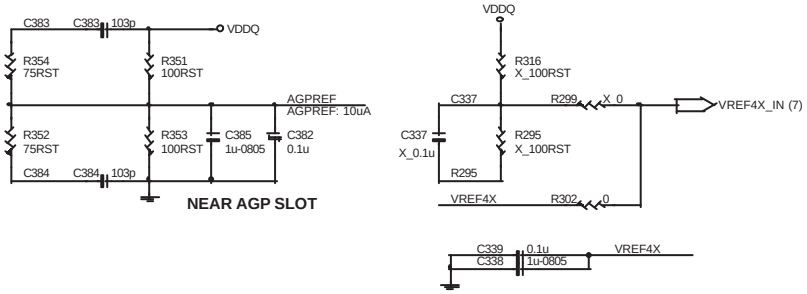


PIRQ#A / PIRQ#B

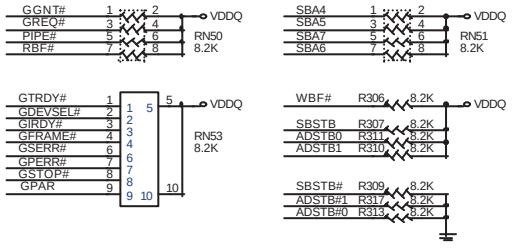
PCI EXPANSION RISER (PCI VER:2.2 COMPLY)



AGP SIGNAL REFERENCE CIRCUIT



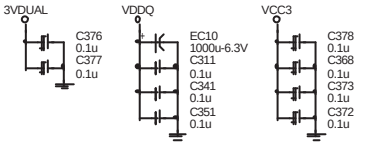
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



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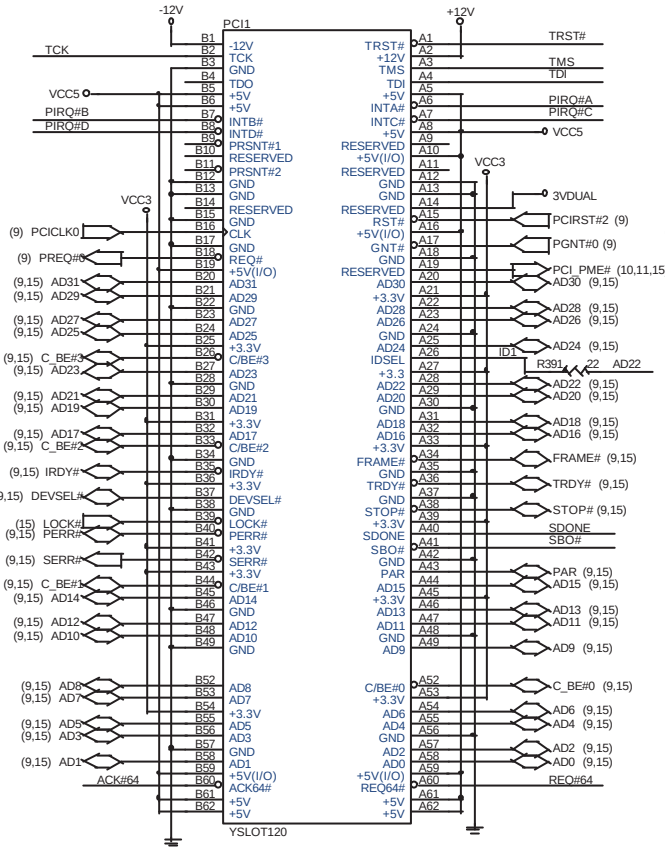
MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

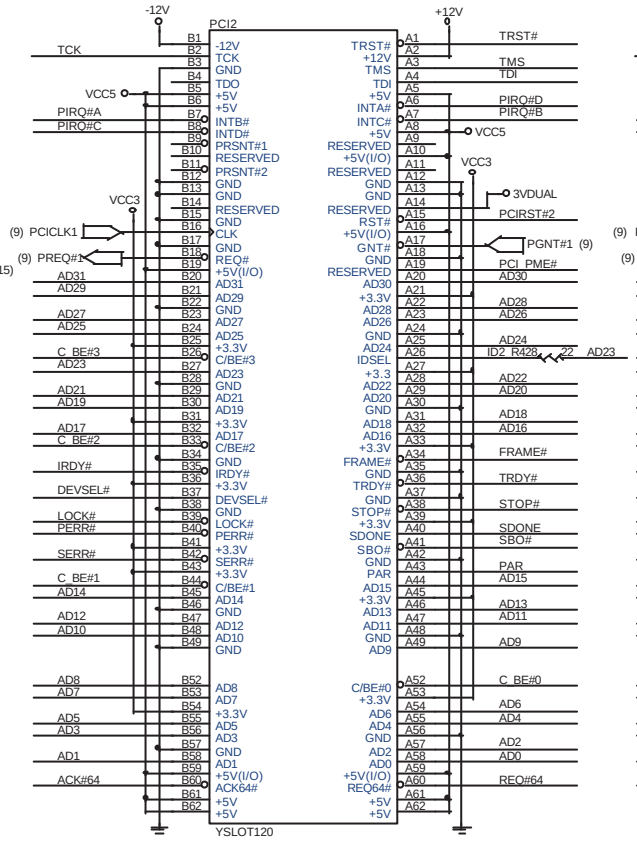
Title	AGP 1.5V SLOT & PCI RISER	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
Date: Tuesday, October 16, 2001	Sheet 15 of 25	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



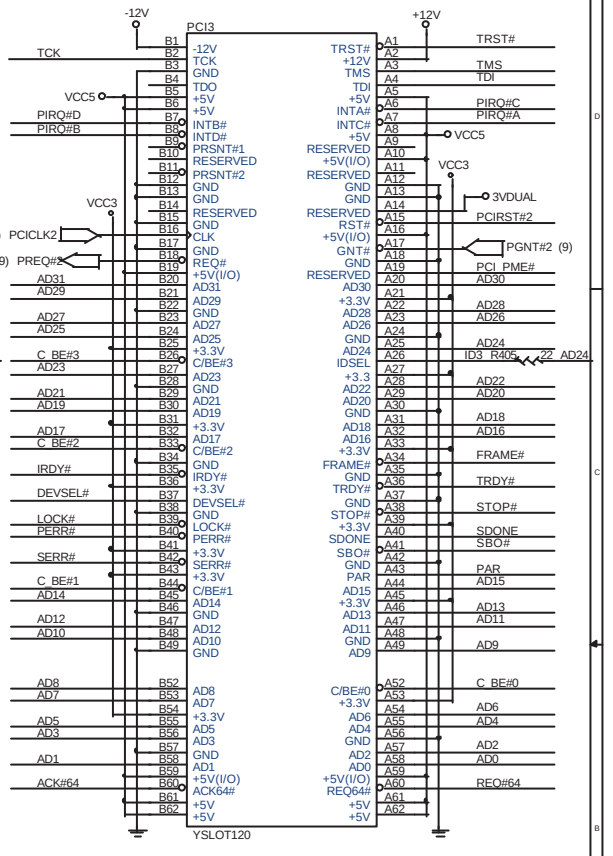
IDSEL = AD22
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



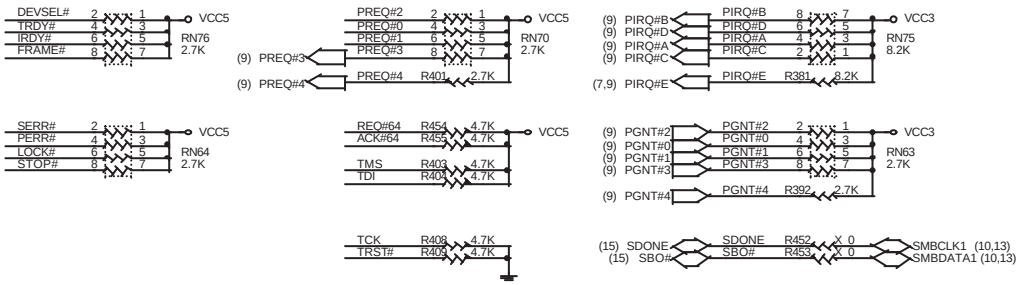
IDSEL = AD23
MASTER = PREQ#1
PIRQ#D

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

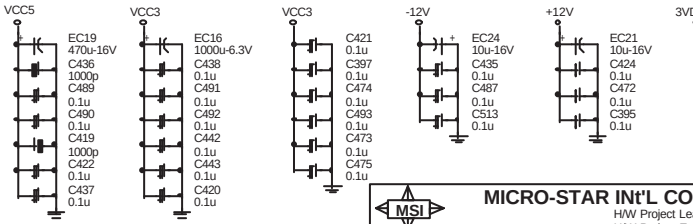


IDSEL = AD24
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

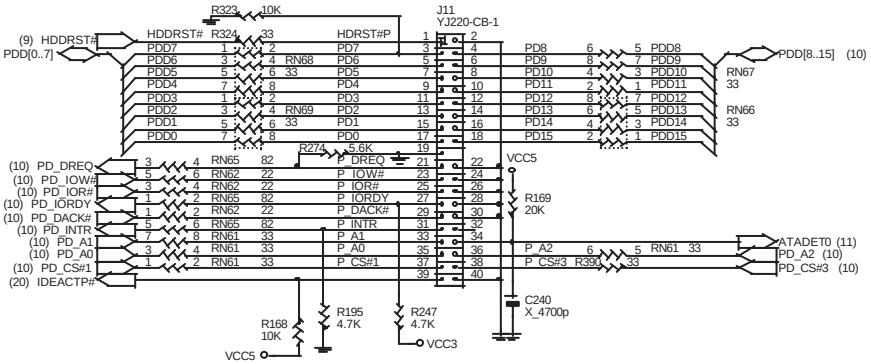


MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

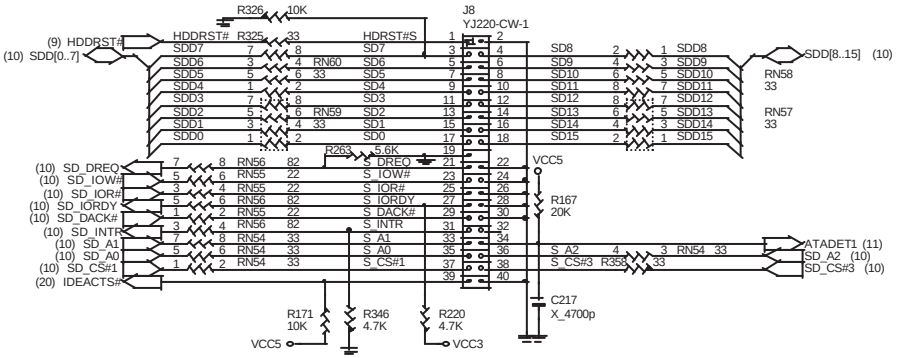
Title	PCI 1& 2 & 3 Slots	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
Date: Tuesday, October 16, 2001	Sheet 16 of 25	

ATA 33/66/100 IDE Connectors

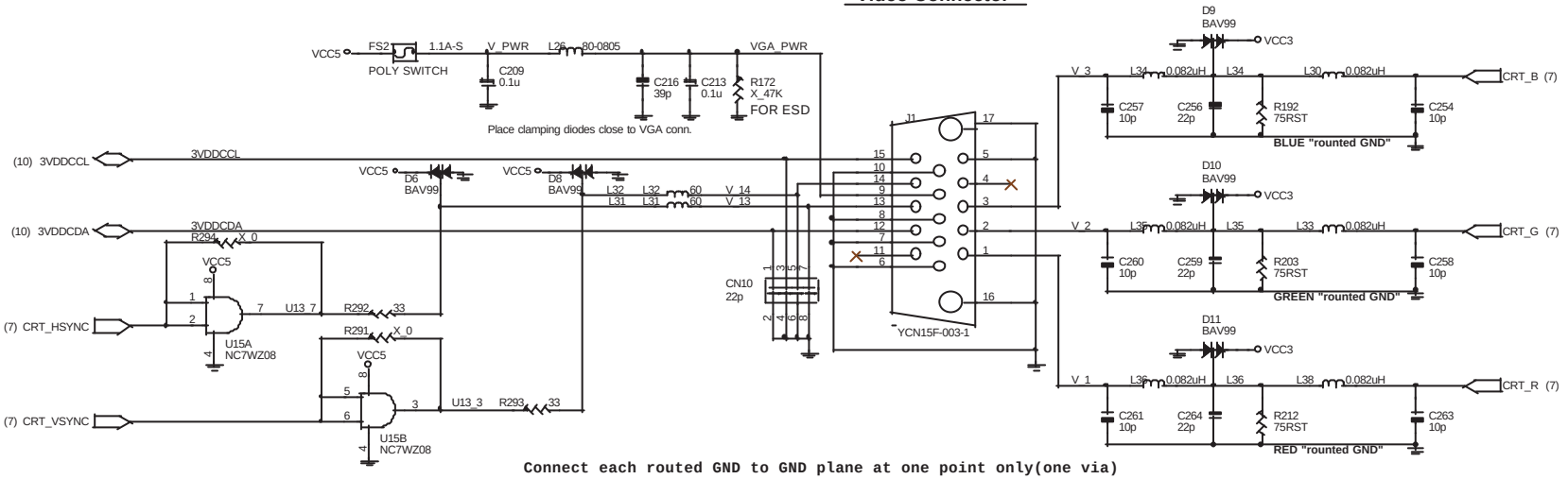
PRIMARY IDE BLOCK



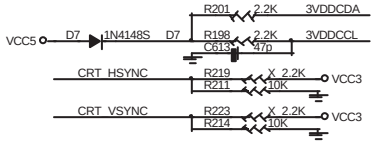
SECONDARY IDE BLOCK



Video Connector



Connect each routed GND to GND plane at one point only(one via)



Function		LDT internal terminations		CPU Type strapping	
		Enable	Disable	Intel	AMD
HSYNC	Buffered	0	1	X	X
	Non-Buffered	0*	1	X	X
VSYNC	Buffered	X	X	1	0
	Non-Buffered	X	X	1	0*

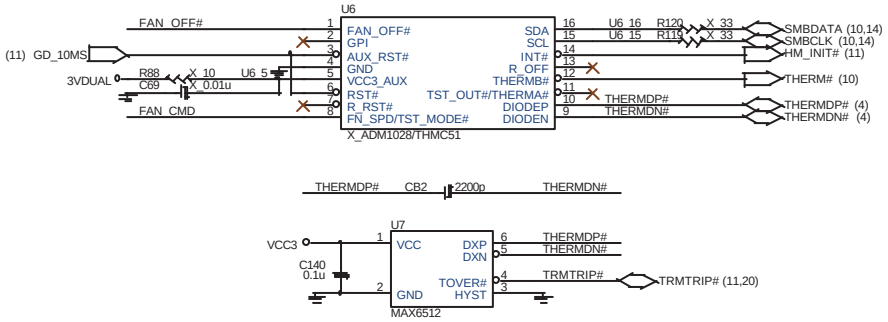
Use 10K pu/pd if VSYNC/HSYNC are buffered;
use 2.2K if VSYNC/HSYNC are un-buffered.
* Default

MSI **MICRO-STAR INt'L CO., LTD.**

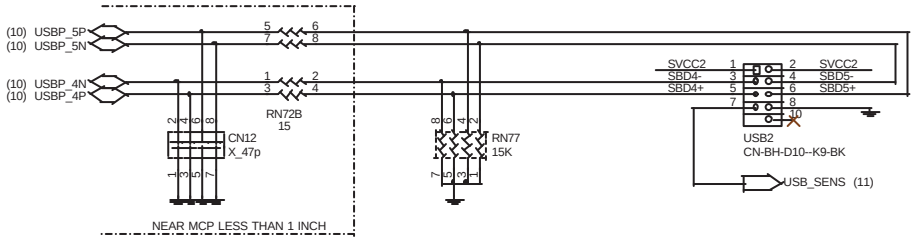
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title	ATA33/66/100 IDE & VIDEO Connectors	
Size	Document Number: ZZTOP (MS-6553)	Rev: 0B
Date: Tuesday, October 16, 2001	Sheet 17 of 25	

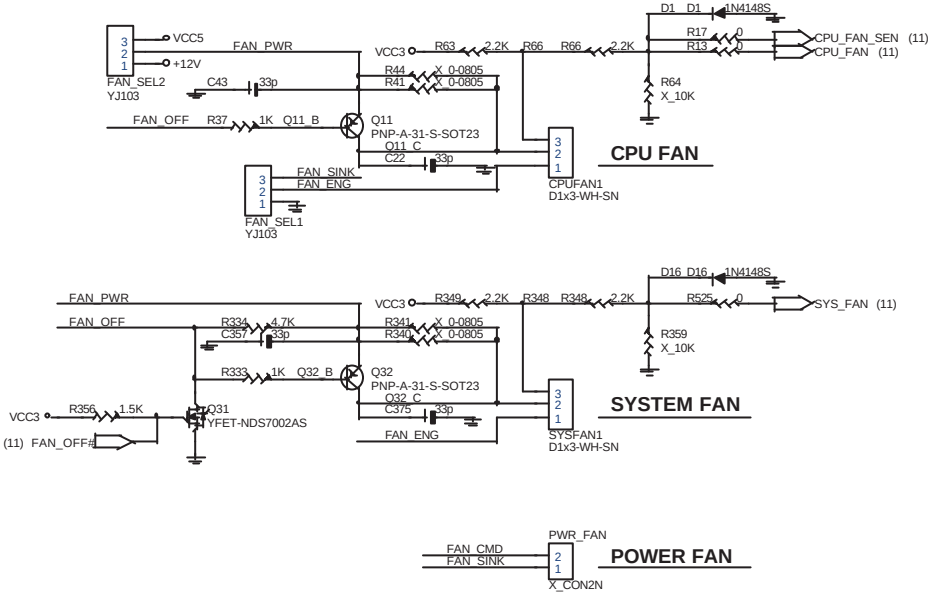
H/W MONITOR - ADM1028 & MAX6512



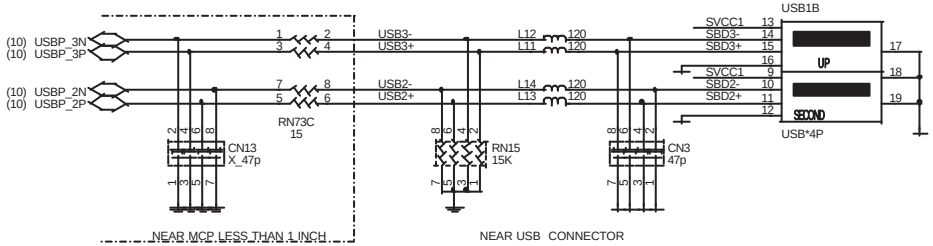
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



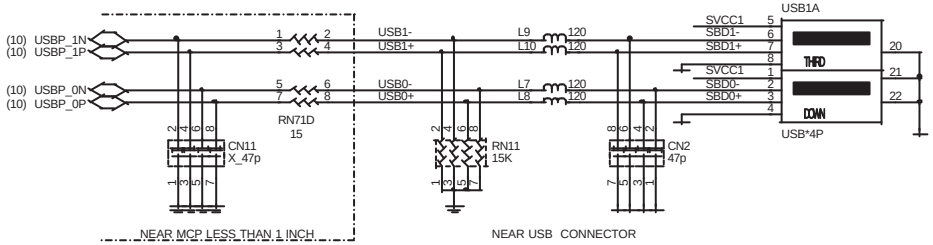
FAN CONTROLLER



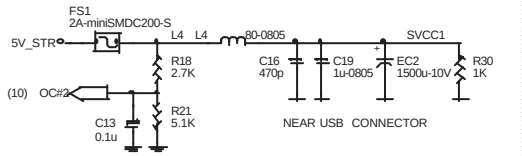
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



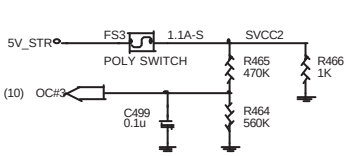
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

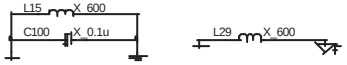


POWER CIRCUIT FOR USB PORT 0,1,2,3



POWER CIRCUIT FOR USB PORT 4,5





MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

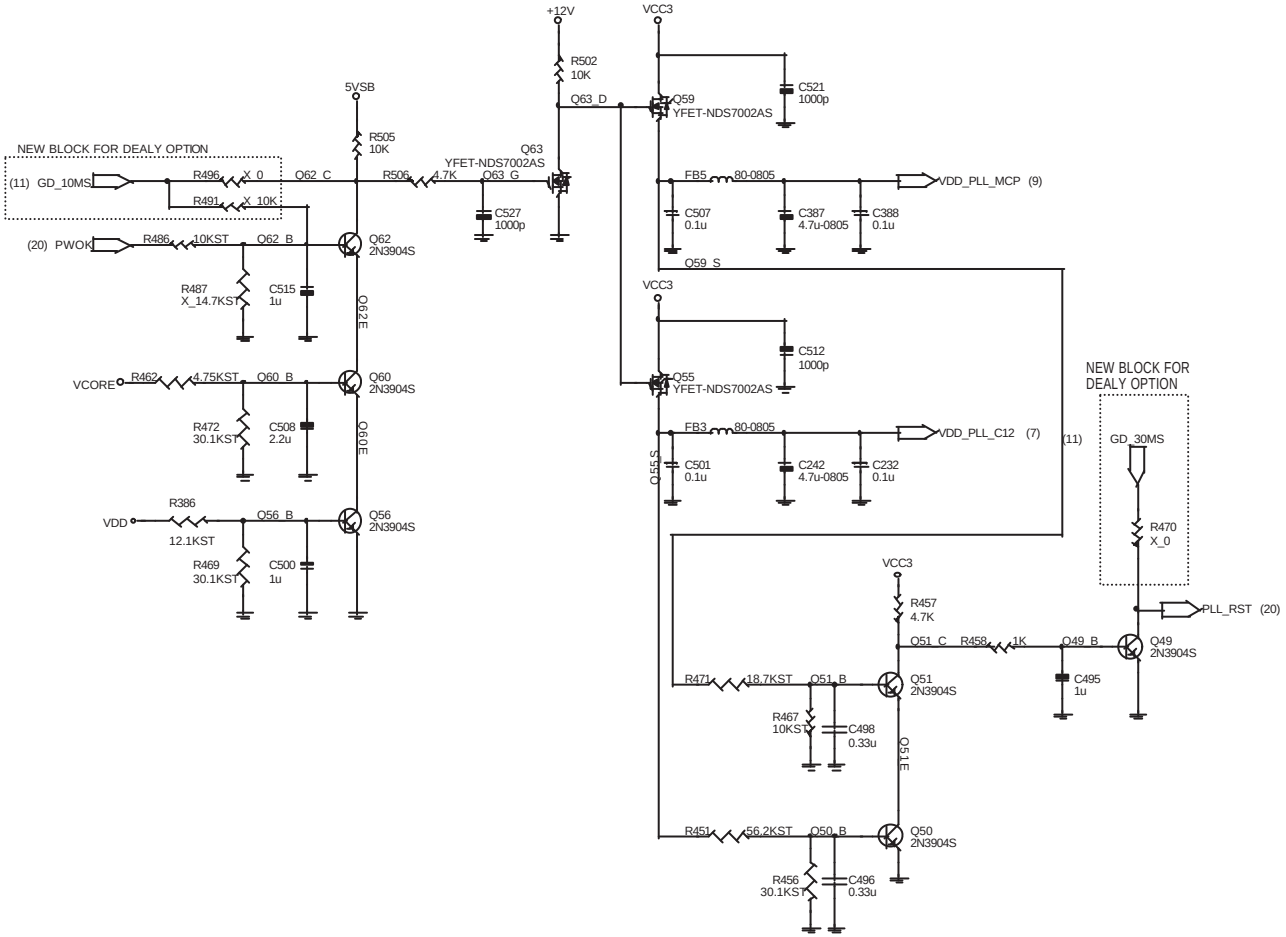
H/W Project Engineer : Prudence Wang

Title: H/W Monitor & FAN & USB Connectors

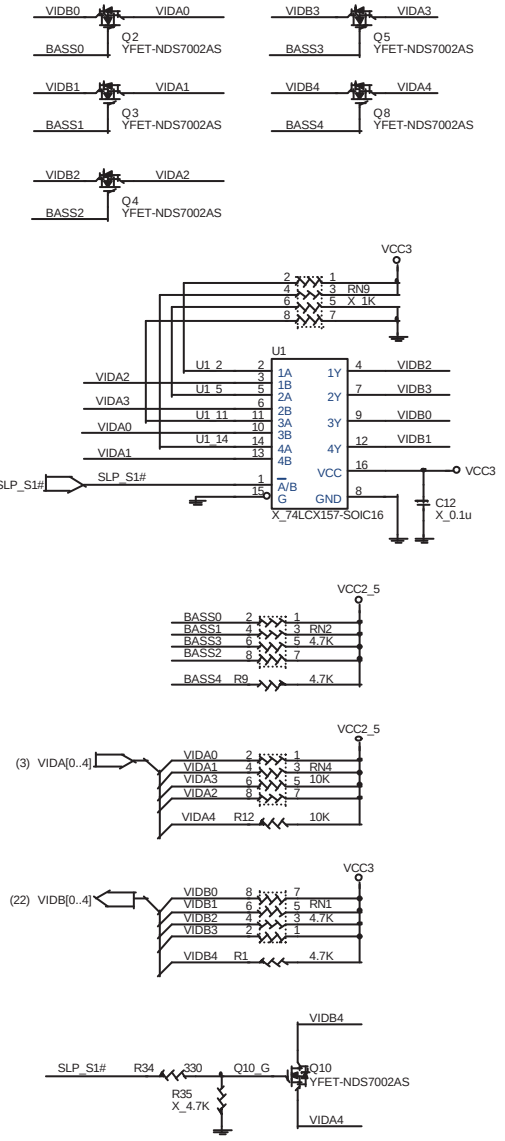
Size | Document Number: ZZTOP (MS-6553) | Rev: 0B

Date: Tuesday, October 16, 2001 | Sheet 18 of 25

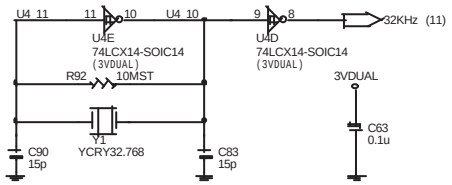
PLL Delay Block



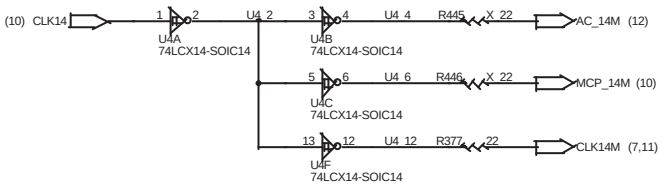
VID Selector Block



32.768KHz Clock Block



14.318MHz Clock Block



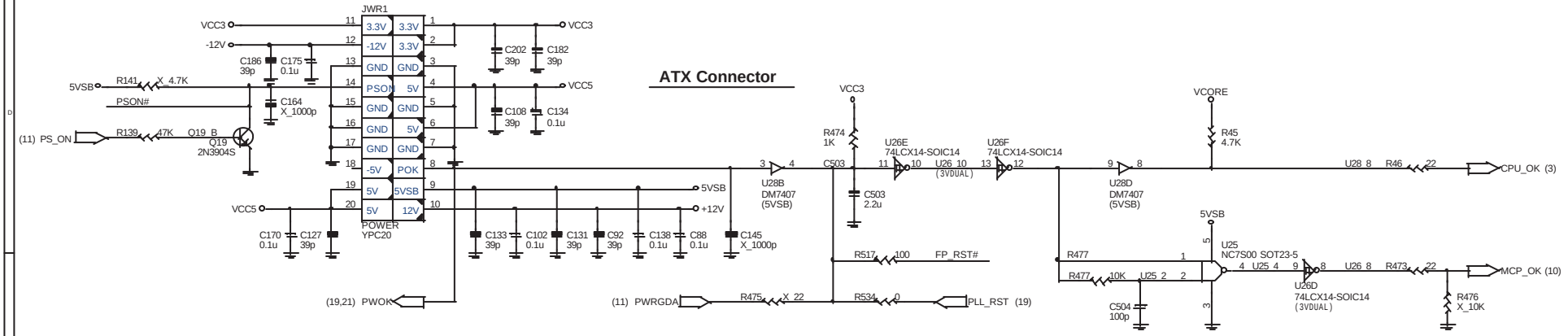
MSI

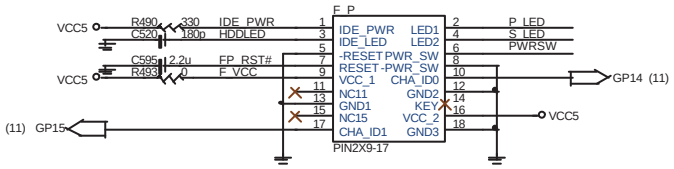
MICRO-STAR INt'L CO., LTD.

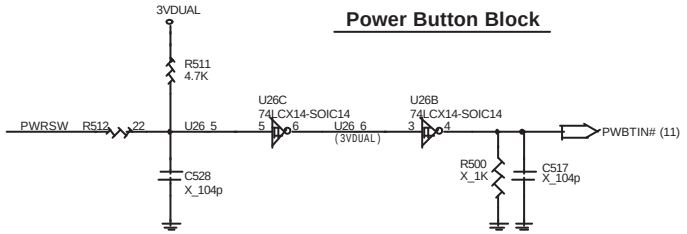
H/W Project Leader : Andy Chen

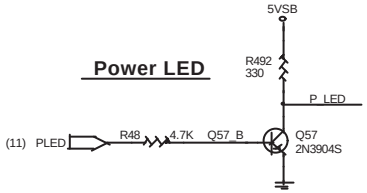
H/W Project Engineer : Prudence Wang

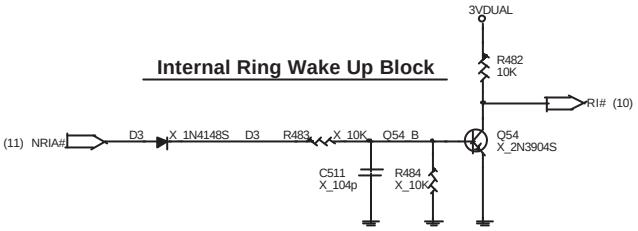
Title	PLL Delay & VID Selector	
Size	Document Number: ZZTOP (MS-6553)	Rev 0B
Date: Tuesday, October 16, 2001	Sheet 19 of 25	

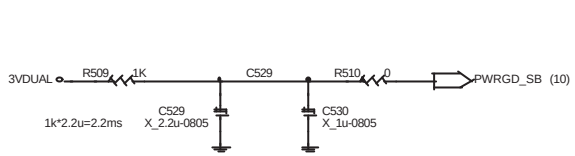


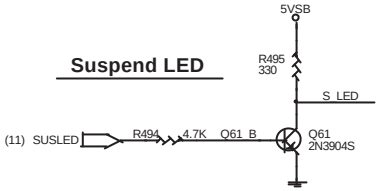


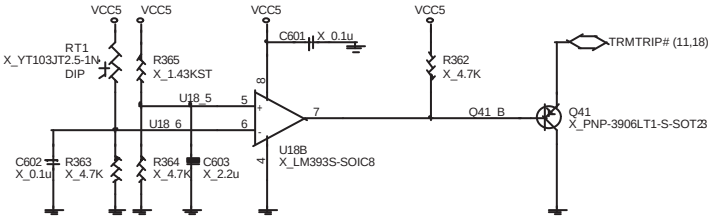


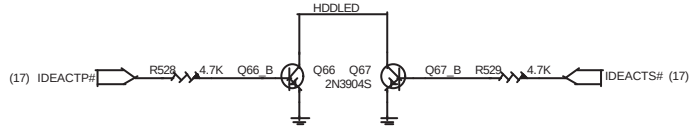












STATE	S0	S1	S3	S4/S5
P_LED	Green	Red	Red	DARK
S_LED (Yellow)	DARK	BRIGHT	BRIGHT	DARK

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

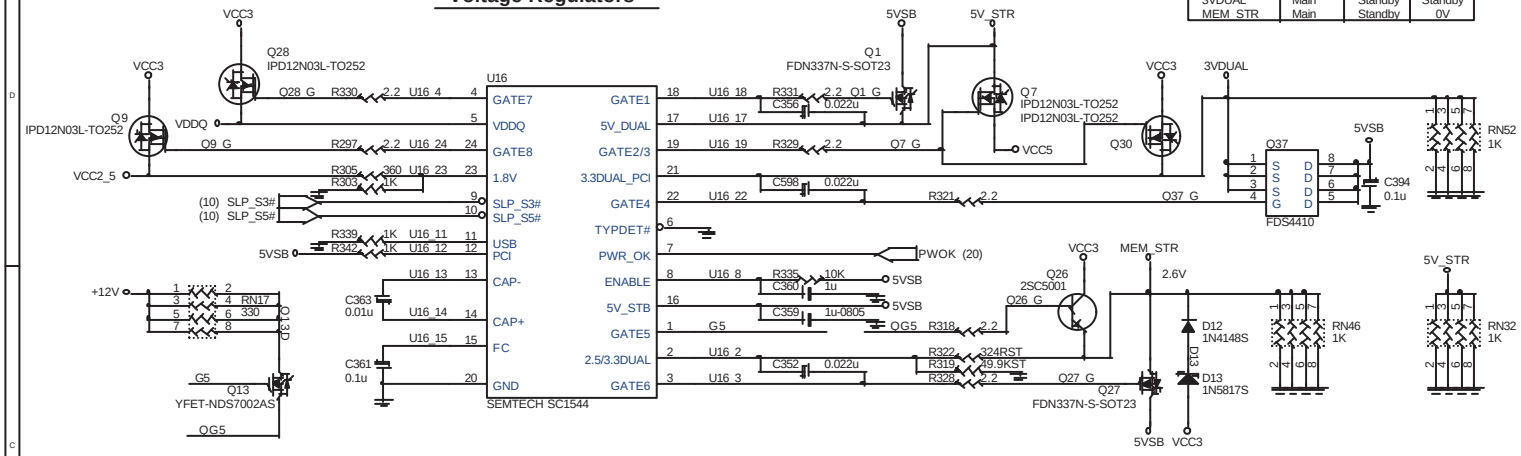
Title: ATX Connector & Front Panel

Size | Document Number: ZZTOP (MS-6553) | Rev: 0B

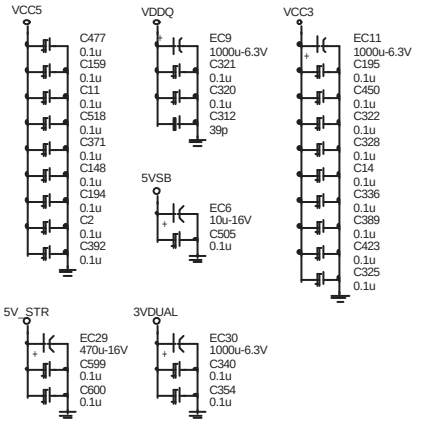
Date: Tuesday, October 16, 2001 | Sheet 20 of 25

Voltage Regulators

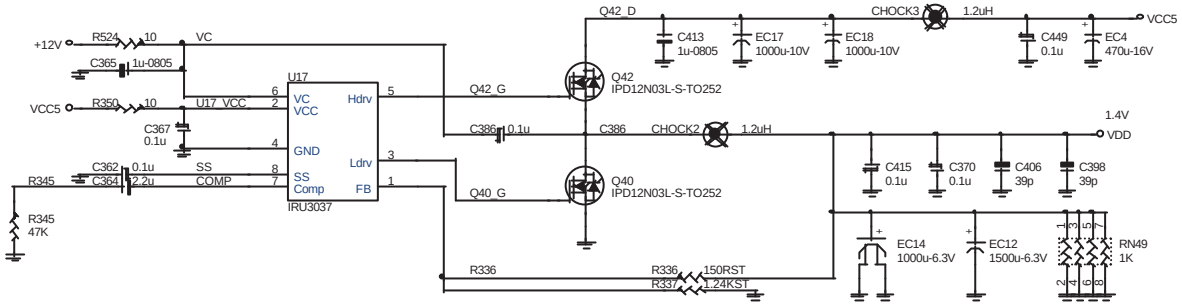
Power	S0	S3	S5
5V_STR	Main	Standby	0V
3VDUAL	Main	Standby	Standby
MEM_STR	Main	Standby	0V



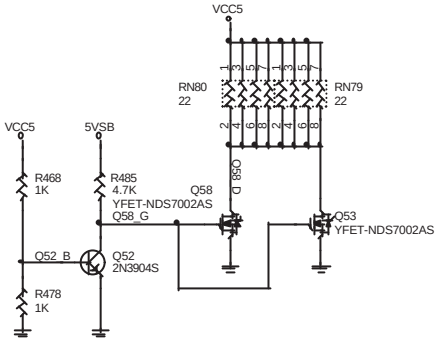
System Decoupling Capacitors



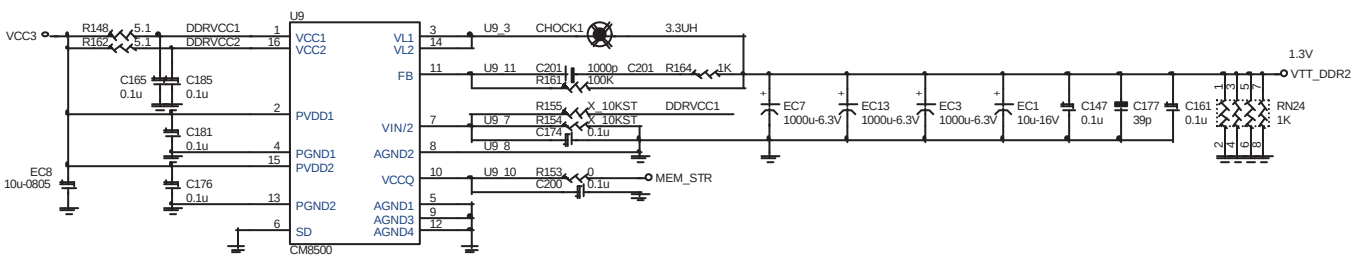
LDT Voltage Regulator



VCC5 Discharge Residual Voltage



DDR VTT Voltage Regulators



MSI	MICRO-STAR INt'L CO., LTD.		
	H/W Project Leader : Andy Chen		
	H/W Project Engineer : Prudence Wang		
Title	System & DDR Regulators		
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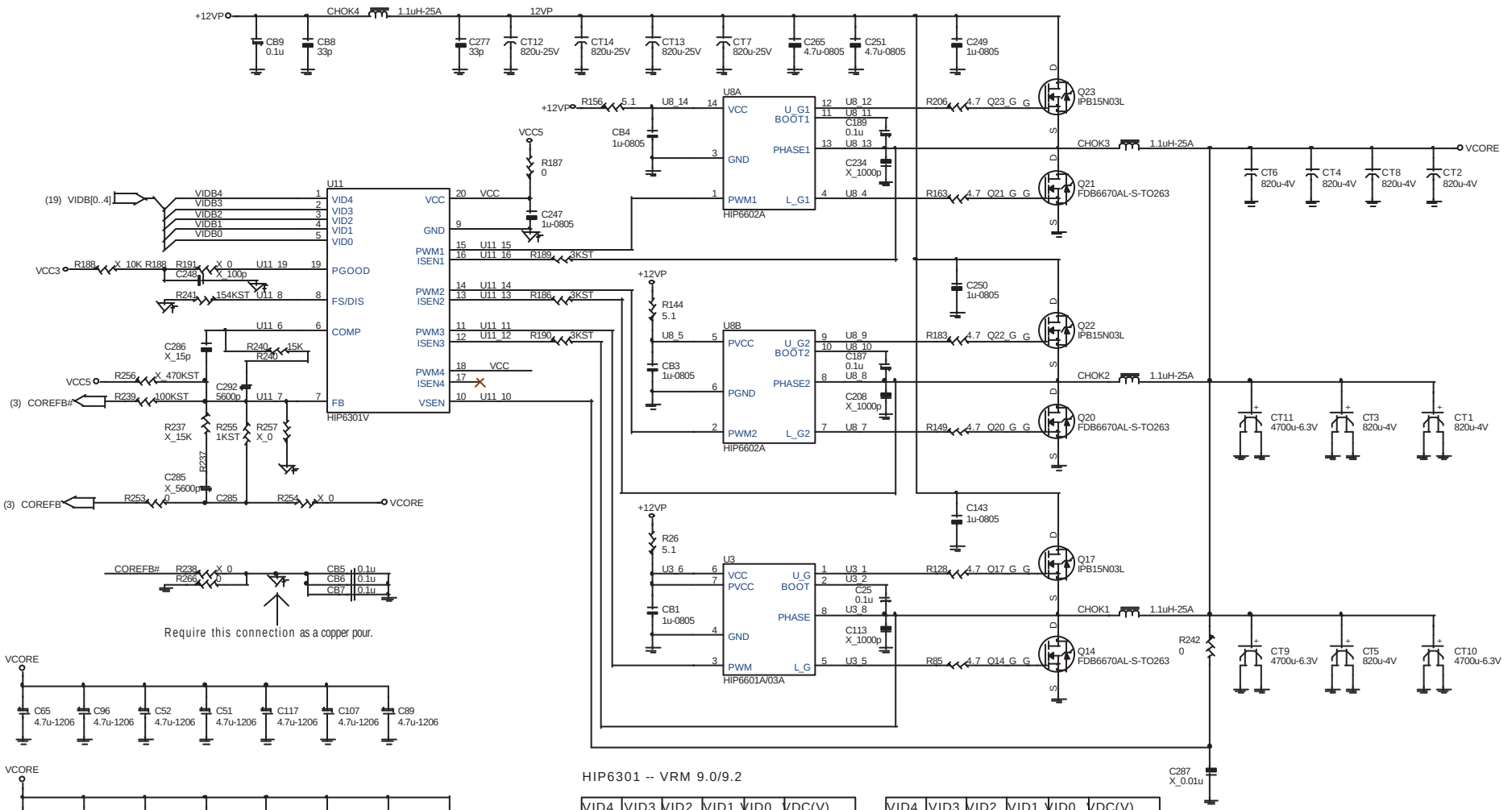
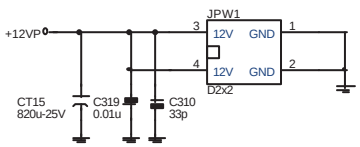


HIP6301 -- VRM 9.0/9.2

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

ATX12V POWER CONNECTOR



MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title: VRM 9.2 - Intersil 6301

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MCP

GPIO Pin	Type	Function
GPIO 0	I	PCI_REQ#4 (multifunction pin)
GPIO 1	O	PCI_GNT#4 (multifunction pin)
GPIO 2	I/O	PCI_PERR# (multifunction pin)
GPIO 3	I	PCI_IRQ#E (multifunction pin)
GPIO 4	I	MII_RXER (multifunction pin)
GPIO 5	I	Pull up through 8.2K ohms (LPC_DRQ#1)
GPIO 6	I	USB_OC2# (multifunction pin)
GPIO 7	I	USB_OC2# (multifunction pin)
GPIO 8	I	USB_OC2# (multifunction pin)
GPIO 9	I	USB_OC3# (multifunction pin)
GPIO 10	I	USB_OC3# (multifunction pin)
GPIO 11	I	AC_SDIN1 (multifuntion pin)
GPIO 12	I	A20GATE (multifuntion pin)
GPIO 13	I	Pull up through 10K ohms (SPDIF)
GPIO 14	I	AUD_DET# (multifunction pin)
GPIO 15	I/O	Unused
GPIO 16	I/O	Unused
GPIO 17	I	Pull up through 8.2K ohms (PRDY#)
GPIO 18	I/O	Unused
GPIO 19	I/O	Unused
GPIO 20	O	SLP_S1# (multifunction pin)
GPIO 21	I	SIO_SMI# (multifunction pin)
GPIO 22	I	THERM# (multifuntion pin)
GPIO 23	I	INTRUDER#
GPIO 24	I/O	RI# (multifuntion pin)
GPIO 25	I/O	KBRST# (multifuntion pin)
SPIO 0	I/O	SM_CLK0 (multifuntion pin)
SPIO 1	I/O	SM_DATA0 (multifuntion pin)
SPIO 2	I/O	SM_CLK1 (multifuntion pin)
SPIO 3	I/O	SM_DATA1 (multifuntion pin)
SPIO 4	I/O	DDC_CLK (multifuntion pin)
SPIO 5	I/O	DDC_DATA (multifuntion pin)
SPIO 6	I	Pull up through 4.7K ohms (SMB_ALERT#)

Flash ROM

GPIO Pin	Type	Function
GPI 0	I	Pull down through 1K ohms (unused)
GPI 1	I	Pull down through 1K ohms (unused)
GPI 2	I	Pull down through 1K ohms (unused)
GPI 3	I	Pull down through 1K ohms (unused)
GPI 4	I	Pull down through 1K ohms (unused)

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2	1010010B	MCLK_A0/MCLK_A0#
		MCLK_A1/MCLK_A1#
		MCLK_A2/MCLK_A2#
DIMM 1	1010001B	MCLK_B0/MCLK_B0#
		MCLK_B1/MCLK_B1#
		MCLK_B2/MCLK_B2#

BIOS Protect Config.	
BIOS Un_Protected	1
BIOS Protected	0

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA#	PCI_REQ#0	AD22	PCICLK0	MCP/AB20 (PCI_CLK0)
	INTB#	PCI_GNT#0			
	INTC#				
	INTD#				
PCI Slot 2	INTD#	PCI_REQ#1	AD23	PCICLK1	MCP/AB18 (PCI_CLK1)
	INTA#	PCI_GNT#1			
	INTB#				
	INTC#				
PCI Slot 3	INTC#	PCI_REQ#2	AD24	PCICLK2	MCP/AB12 (PCI_CLK2)
	INTD#	PCI_GNT#2			
	INTA#				
	INTB#				

LPC Super I/O

GPIO Pin	Type	Function
GPIO 14	I	CHASSIS_ID0
GPIO 15	I	CHASSIS_ID1
GPIO 86	I/O	Unused
GPIO 16	I/O	Unused
GPIO 23	I	BOARD_ID0
GPIO 70	I	BOARD_ID1
GPIO 65	I	USB_SENS
GPIO 60	I/O	Unused
GPIO 61	I/O	Unused
GPIO 43	I/O	Unused
GPIO 10	I	VERSION_ID0
GPIO 11	I	VERSION_ID1
GPIO 12	I	CPU_FAN
GPIO 27	I	HM_INIT#
GPIO 16	I/O	Unused
GPIO 17	I/O	Unused
GPIO 24	I/O	SIO_ADDR
GPIO 20	I/O	Primary IDE ATA66/100 detection (ATADET0)
GPIO 21	I/O	Secondary IDE ATA66/100 detection (ATADET1)
GPIO 44	I/O	Unused
GPIO 45	I/O	Unused
GPIO 33	I/O	FDD_DET
GPIO 74	I/O	PHY Disable
GPIO 50	I/O	Unused
GPIO 51	I/O	Unused
GPIO 52	I/O	Unused
GPIO 53	I/O	Unused
GPIO 54	I/O	Unused
GPIO 55	I/O	Unused
GPIO 56	I/O	Unused
GPIO 57	I/O	Unused
GPIO 35	I/O	Unused
GPIO 34	O	BIOS Protect
FAN_TACH4	I	Unused

MICRO-STAR INt'L CO., LTD.
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
Title: General Purpose Spec
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Revision Initial ver: 0AE0 on 09/10/01

Schematic Initial Revision 0AE0.

Revision change list from ver: 0AE0 to ver: 0AE1 on 09/12/2001

Sheet 3: Change R135 and R136 from 10Kohm to 0ohm.

Sheet 9: Change R592 and R595 power from 3vdual to vcc3.

Sheet 12: Modify audio of front panel block.

Sheet 18: Modify some block for customer request, detail list on below:

(1) Add max6512.

(2) Modify FAN block.

Sheet 16: Modify some block for customer request, detail list on below:

(1) Modify IDSEL same as nVidia.

(2) Modify int routing same as nVidia.

Sheet 19: Add 32KHz block for support S3 state of LPC I/O.

Revision change list from ver: 0AE1 to ver: 0AE2 on 09/13/2001

Sheet 1: Modify some description.

Sheet 3: Delete clock multiplier table.

Sheet 16: Update PCI device note.

Sheet 18: Add clamp diode on fan.

Sheet 20: Add CPU therm meter block.

Sheet 21: Change RN114, RN130, RN131, RN132 and RN133 value from 100ohm to 1Kohm.

Sheet 22: Modify DDR VTT block for support 1.3V.

Revision change list from ver: 0AE2 to ver: 0AE3 on 09/19/2001

Sheet 3: Add a pull high resistor on APICCLK_CPU.

Sheet 10: Modify some block for customer request, detail list on below:

(1) Change LDT_2NB_1 to LDT_TXD1.

(2) Swap PERR# and SERR#.

Sheet 10: Modify some block for customer request, detail list on below:

(1) Add a pull high resistor on APICCLK_MCP.

(2) Delete R184.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Change Q152 from 2N3904S to 2N7002.

(2) Delete L77,L78,C718,C719.

(3) AUX install.

Sheet 15: Change VCC_AGP to VDDQ.

Revision change list from ver: 0AE3 to ver: 0AE4 on 09/20/2001

Sheet 12: Modify some block for customer request, detail list on below:

(1) Delete amplifier and relational components.

(2) Delete L77,L78,C718,C719.

(3) Change C31 and C36 from 0.1uF to 4.7uF/0805.

(4) Delete R1021 and change Q152 from 2N3904 to NDS7002AS.

(5) Add a ferrite bead to connect VCC5 and +5VR, but no stufff.

(6) Change from analog gnd to digital gnd on R463,R618,Q146,Q151, and Q152.

Sheet 15: Delete C825 and C830.

Sheet 18: Modify some block for customer request, detail list on below:

(1) Delete L30,L31,L34,L35, and CN17.

(2) Delete FB5,C493,C617, and EC44.

Sheet 21: Change Q124 from FDN337N to FDS4410.

Revision change list from ver: 0AE4 to ver: 0AE5 on 09/21/2001

Rename all components.

Sheet 3: Add a capacitor on CPU_OK.

Sheet 10: Change U33 from RT9169 to S817.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Change value from 4.7Kohm to 6.2Kohm on R14, R621, R9, and R622.

(2) Change from XTAL output on audio.

(3) Add two pull down resistors near C607 and C609.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Add a resistor between U26D and U26E.

(2) Delete invert logic on RESUME Block.

(3) Add a invert logic on PWRBTN Block.

Revision change list from ver: 0AE5 to ver: 0A on 09/22/2001

Release final ver:0A schematic.

Sheet 23: Modify GPIO port.

Revision change list from ver: 0A to ver: 0AE6 on 09/26/2001

Sheet 17: Modify some block for customer request, detail list on below:

(1) Add BAV99 components of BOM on D6, D8 to D11.

(2) Change from 60ohm to 0.082uH on L30, L33 to L36, and L38.

Sheet 18: Add a component of BOM on U7.

Sheet 22: Change from 1500uF-16V to 820uF-25V on CT7, CT12 to CT15.

Revision change list from ver: 0AE6 to ver: 0AE7 on 09/27/2001

Sheet 18: Modify some block for customer request, detail list on below:

(1) Change U6,R88,C69,R119,and R120 to not installed.

(2) Change R63,R66,R64,D1,R13,Q11,and R37 to not installed.

(3) Change R349,R348,R359,D16,R334,Q32,and R333 to not installed.

(4) Change Q31,Q12,R356,R52,and R67 to not installed.

(5) Change PWR_FAN to not installed.

Revision change list from ver: 0AE7 to ver: 0AE8 on 10/08/2001

All no label made label.

Sheet 10: Modify some block for customer request, detail list on below:

(1) Add R520, and R521 for next version.

(2) Delete R431 for duplicate components on AUD_DET# signal..

(3) Change package to SC82AB on S817.

(4) Change R407,Q43,Q46,R420,C464,U23, and R413 to no stuff.

(5) Change U24 to stuff.

(6) CLK14 through buffer drive in sheet19.

Sheet 11: Modify some block for customer request, detail list on below:

(1) Add one pull 3VDUAL resistor on PWRGDA signal.

(2) Add one pull VCC3 resistor on MR# signal, and no stuff.

Sheet 13: Add 24C02 eeprom.

Sheet 14: Add three bulk capacitors on MEM_STR.

Sheet 18: Fan system change to same as MS-6525.

Sheet 19: Add 14.318M clock block.

Sheet 20: Delete Over TEMP. shutdown circit block.

Sheet 21: Modify some block for customer request, detail list on below:

(1) Add one bulk capacitor on 5V_STR signal.

(2) Add one bulk capacitor on 3VDUAL signal.

(3) Change CHOCK2 from 8uH to 1.2uH.

(4) Change pin2 of U17 from +12V to Vcc5.

(5) Swap pin D and pin S on Q26.

Sheet 22: Change from +12V to +12VP on R26, R144, and R156.

Revision change list from ver: 0AE8 to ver: 0AE9 on 10/11/2001

Sheet 10: Modify some block for customer request, detail list on below:

(1) Change AUD_DET# signal from pin J21 to pin G20 on MCP.

(2) Restore R431 to pin J21, and change label to SLPBTN#.

Sheet 11: Modify some block for customer request, detail list on below:

(1) Change CPU_FAN signal from pin 110 to pin 35 on Super I/O.

(2) Add one pull 3VDUAL resistor on pin110 on Super I/O.

Sheet 12: Modify some block for customer request, detail list on below:

(1) Delete R447 and R448.

(2) Move R327 and R320 to the other side of L41 and L40.

(3) Neighbor EC22 and EC23 with Q34 and Q35 individual.

(4) Use two 4.7Kohm resistors to divide voltage of right and let signals on AUX IN connector.

(5) Change value and type from 1uF 0603 to 4.7uF 0805 on C355.

(6) Change from GND to audio GND on Q36, Q38, and Q39.

(7) Change value and type from 47uF to 100uF on EC22 and EC23.

(8) Change R343 power from +12VR to +12V.

Sheet 13: Change Q24 from 2N3904S to 2N3906.

Sheet 17: Modify some block for customer request, detail list on below:

(1) Delete R209 and R231, tired to GND on pin28.

(2) Delete R177 and R166; C240 and C217 no stuff.

(3) Change R167 and R169 from GND to VCC5.

Sheet 18: Install R17.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Delete a resistor between U26D and U26E.

(2) Delete D14 and D15; add two 2N3904S to IDEACTP# and IDEACTS# signals.

(3) Change R365 value from 10Kohm to 1.43Kohm.

Sheet 21: Modify some block for customer request, detail list on below:

(1) Change part from SPD09N05 to IPD12N03L on Q7, Q9, Q28 and Q30.

(2) Add a capacitor between pin21 and pin22 on U16.

(3) Add some capacitors on 5V_STR signal.

Sheet 22: Change value from 0ohm to 2.7ohm on R85, R128, R149, R183, R163, and R206.

Sheet 23: Modify some block for customer request, detail list on below:

(1) Modify GPIO14 and GPIO19 on MCP.

(2) Modify GP12 and add FAN_TACH4 on Super I/O.

Revision change list from ver: 0AE9 to ver: 0AEA on 10/12/2001

Sheet 12: Removed audio GND from pin12 of J2C.

Sheet 20: Modify some block for customer request, detail list on below:

(1) Change part from LM358 to LM393 on U18.

(2) Change powr from +12V to VCC5 on pin8 on U18, and add a capacitor to this.

(3) Change R363 and R364 from 10Kohm to 4.7Kohm.

(4) Swap relational components on pin5 and pin6 of U18, and add two capacitors on these.

(5) Change R362 to pull VCC5 between Q41 and pin7 of U18.

(6) Change R362 value from 1Kohm to 4.7Kohm.

MSI

MICRO-STAR INt'L CO., LTD.

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title	REVISION HISTORY - 1	
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Revision change list from ver: 0AEA to ver: 0AEB on 10/15/2001

Sheet 1: Add sheet25.

Sheet 4: Add nine 56pF capacitors on VCORE for EMI.

Sheet 7: Add RC on RGB singals and put near chipset for EMI.

Sheet 12: Add a bead on pin9 on U19 for EMI.

Sheet 17: Add a 47pF capacitor on 3VDDCCL signal for EMI.

Sheet 19: Swap pin 12 and pin4 on U4 for simple layout.

Sheet 22: Change value from 2.7ohm to 4.7ohm on R85, R128, R149, R183, R163, and R206 for EMI.

Sheet 25: Add new sheet for revision history 2.

Revision change list from ver: 0AEB to ver: 0B on 10/16/2001

Sheet 5: Modify some block for customer request, detail list on below:

(1) Change R185, R179 and R180 from 0ohm to 10ohm for EMI.

(2) Change C241 from no stuff to 10pF for EMI.

Sheet 10: Change SMBBUS signals power from 3VDUAL to VCC3.

Sheet 11: Add R539 and R540 on pin5 of U2.

Sheet 12: Move EC20 to another side on L48 for EMI.

We move audio connector same as Styx position.

Gerber release on this version.

MSI	**MICRO-STAR INt'L CO., LTD.** H/W Project Leader : Andy Chen H/W Project Engineer : Prudence Wang	
Title	REVISION HISTORY - 2	
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