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MS-6552 (LEGEND)

Version 0A

1002

INTEL (R) Brookdale Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generation -- ICS94208

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 3
CNR SLOT * 1

Micro-Star	Title: *MS-6552*	Rev: *0A*
Document Number: Cover Sheet		
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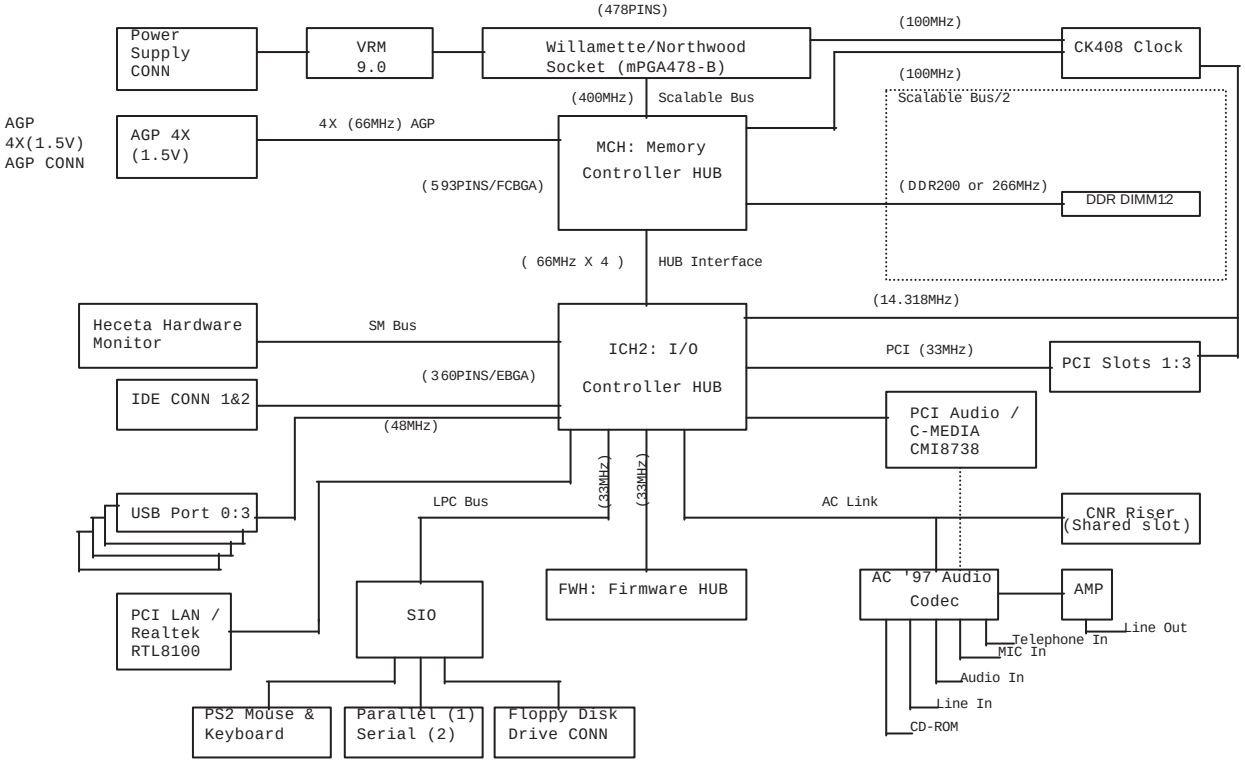

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Block Diagram		
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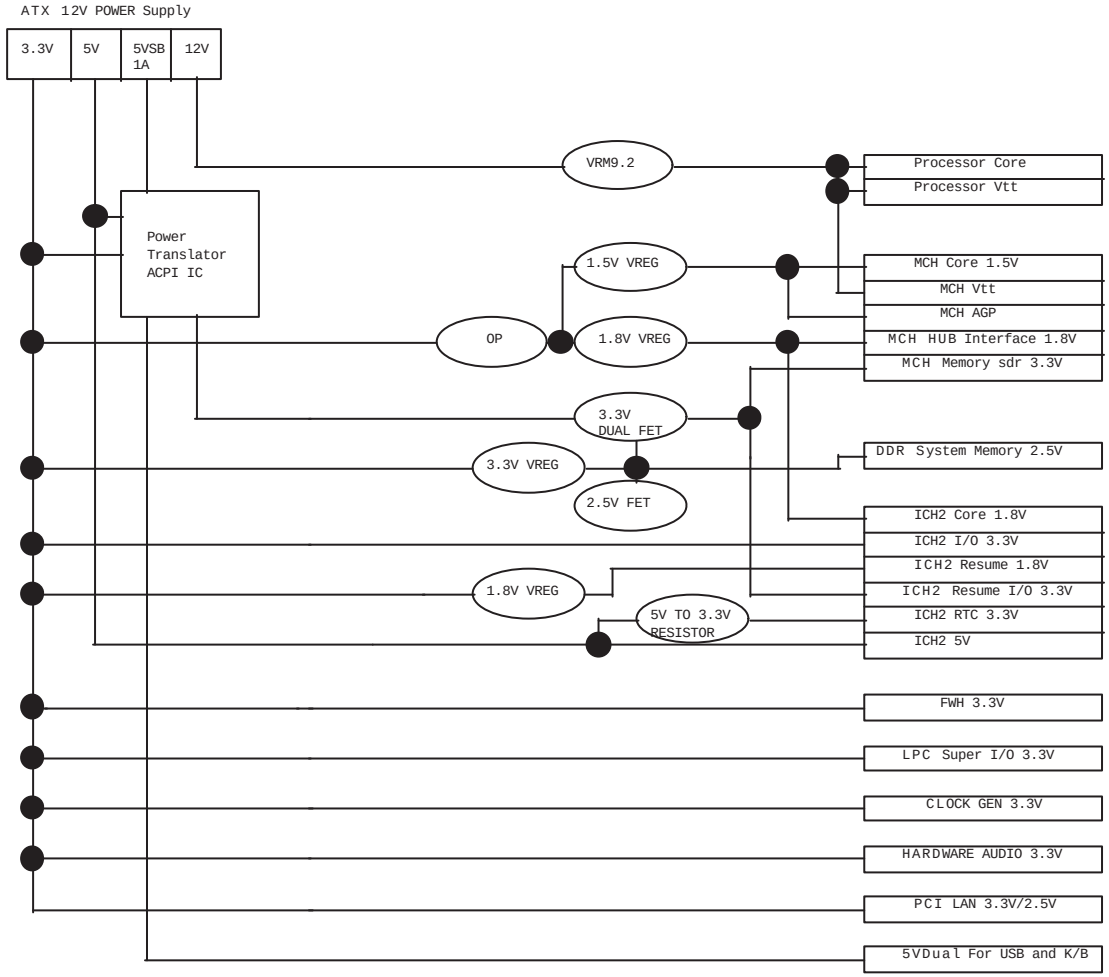
Power Delivery Map



Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Power Delivery Map		
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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Not Implemented
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	Non
GPIO 29~31	I/O	Not Implemented

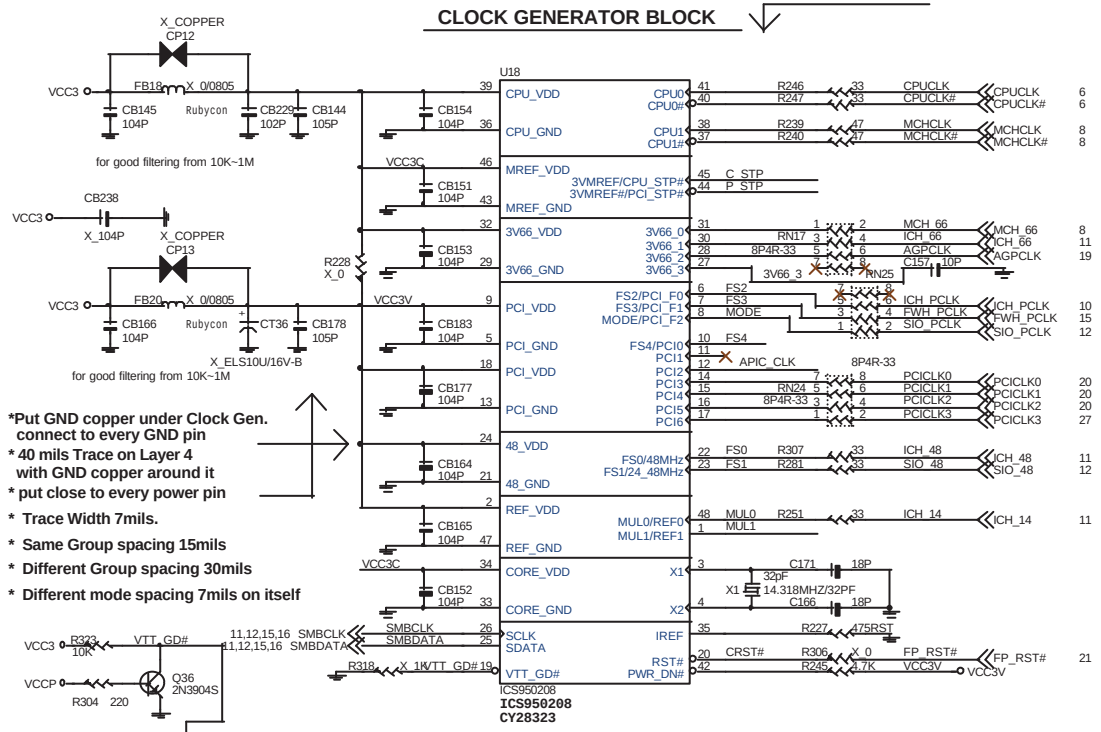
FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

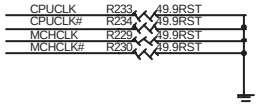
DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Audio	INTD#/INTE# INTA# INTB# INTC#	AD23
PCI Lan	INTC#/INTF# INTD# INTA# INTB#	AD22

*Trace less 0.5"

CLOCK GENERATOR BLOCK

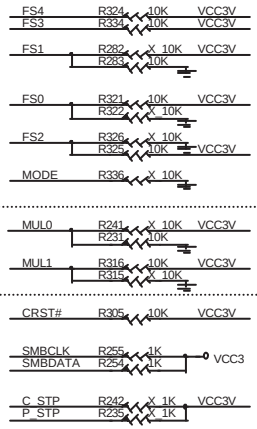


Shut Source Termination Resistors

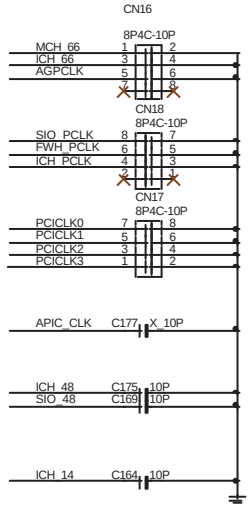


Trace less 0.2"
49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



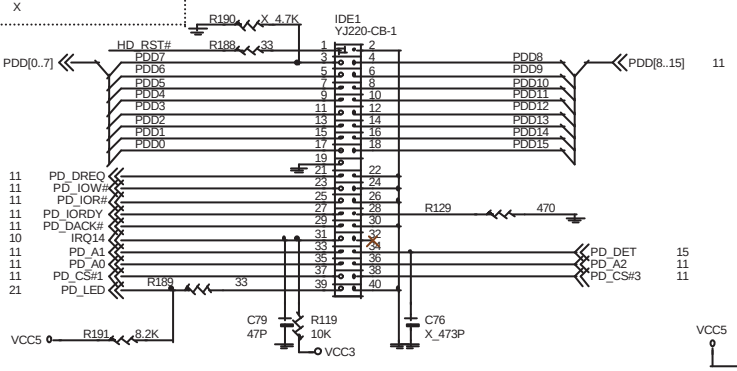
Pull-Down Capacitors



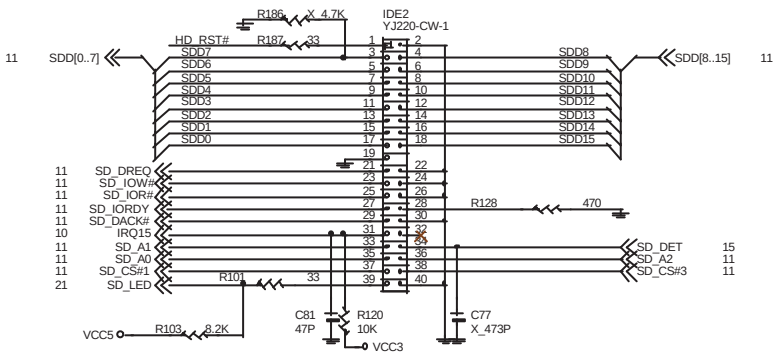
used only for EMI issue
Trace less 0.2"

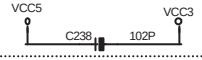
ATA100 IDE CONNECTORS

PRIMARY IDE BLOCK

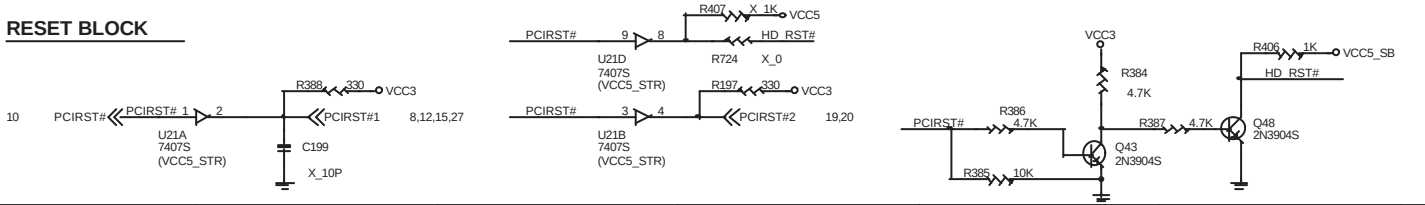


SECONDARY IDE BLOCK





RESET BLOCK



Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Clock CY28323/4 & ATA100 IDE		
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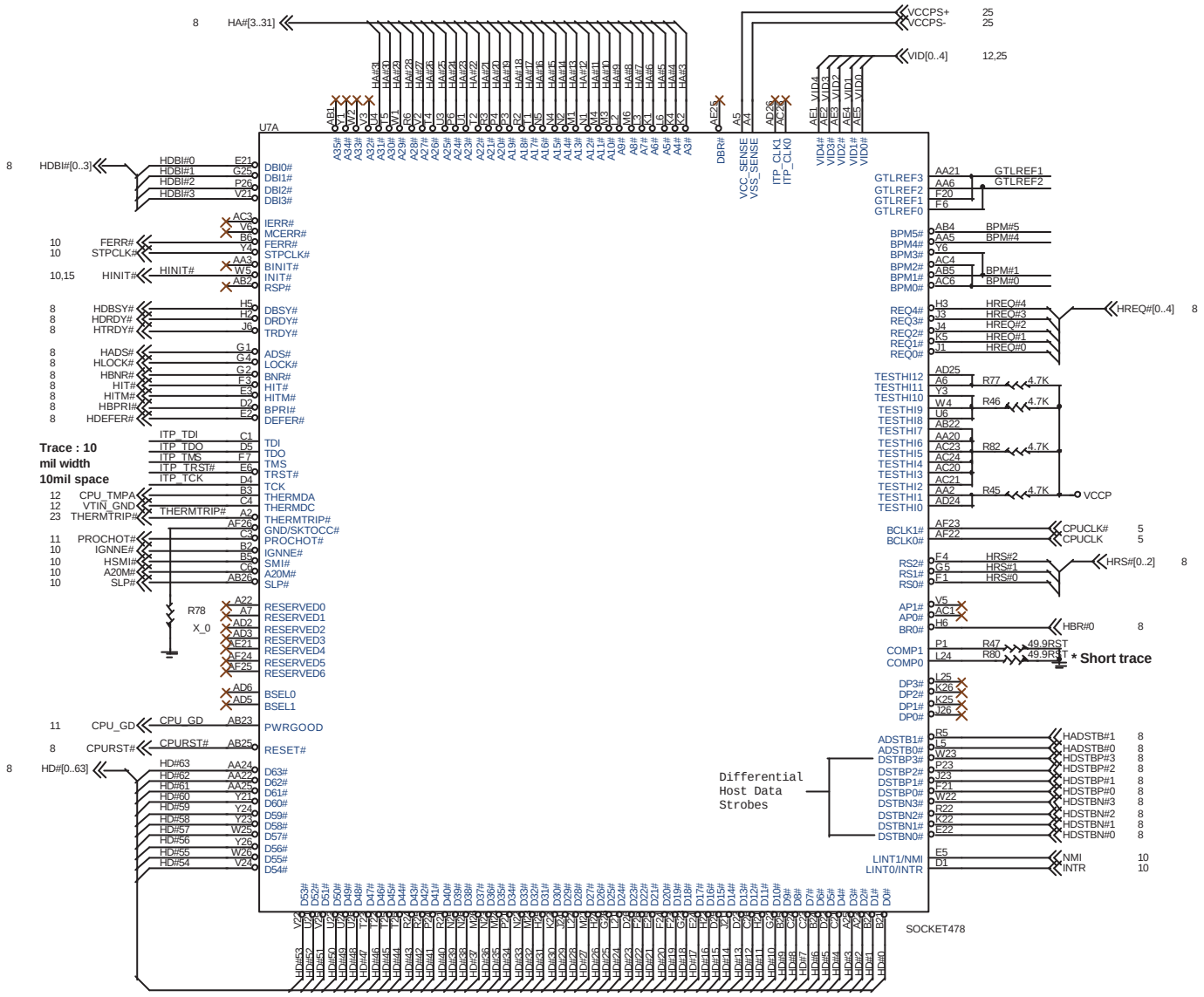
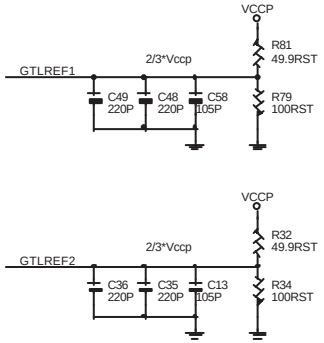
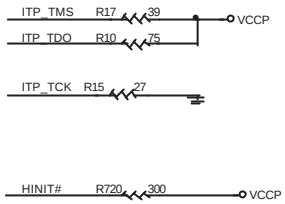
CPU SIGNAL BLOCK



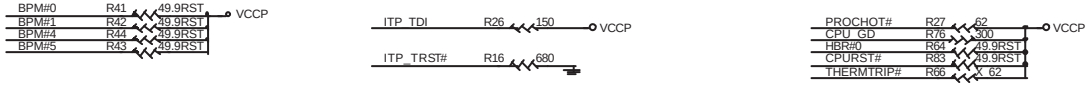
CPU GTL REFERNCE VOLTAGE BLOCK



Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin



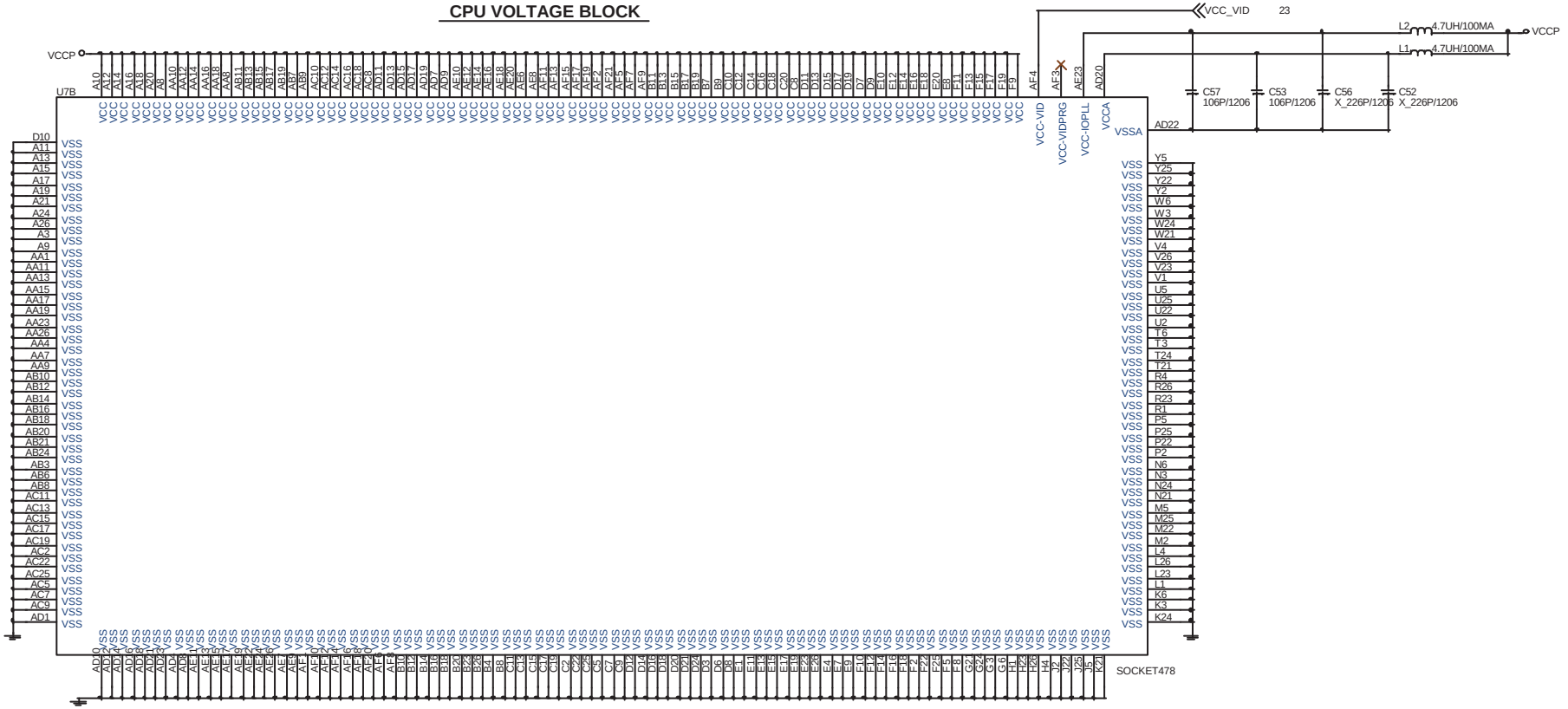
CPU STRAPPING RESISTORS



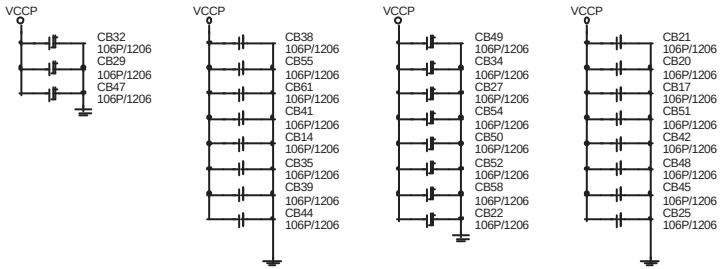
ALL COMPONENTS CLOSE TO CPU

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: INTEL mPGA478-B CPU1		
Last Revision Date: Wednesday, September 19,2001	Sheet 6 of 35	

CPU VOLTAGE BLOCK

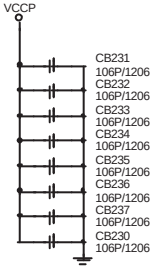


CPU DECOUPLING CAPACITORS



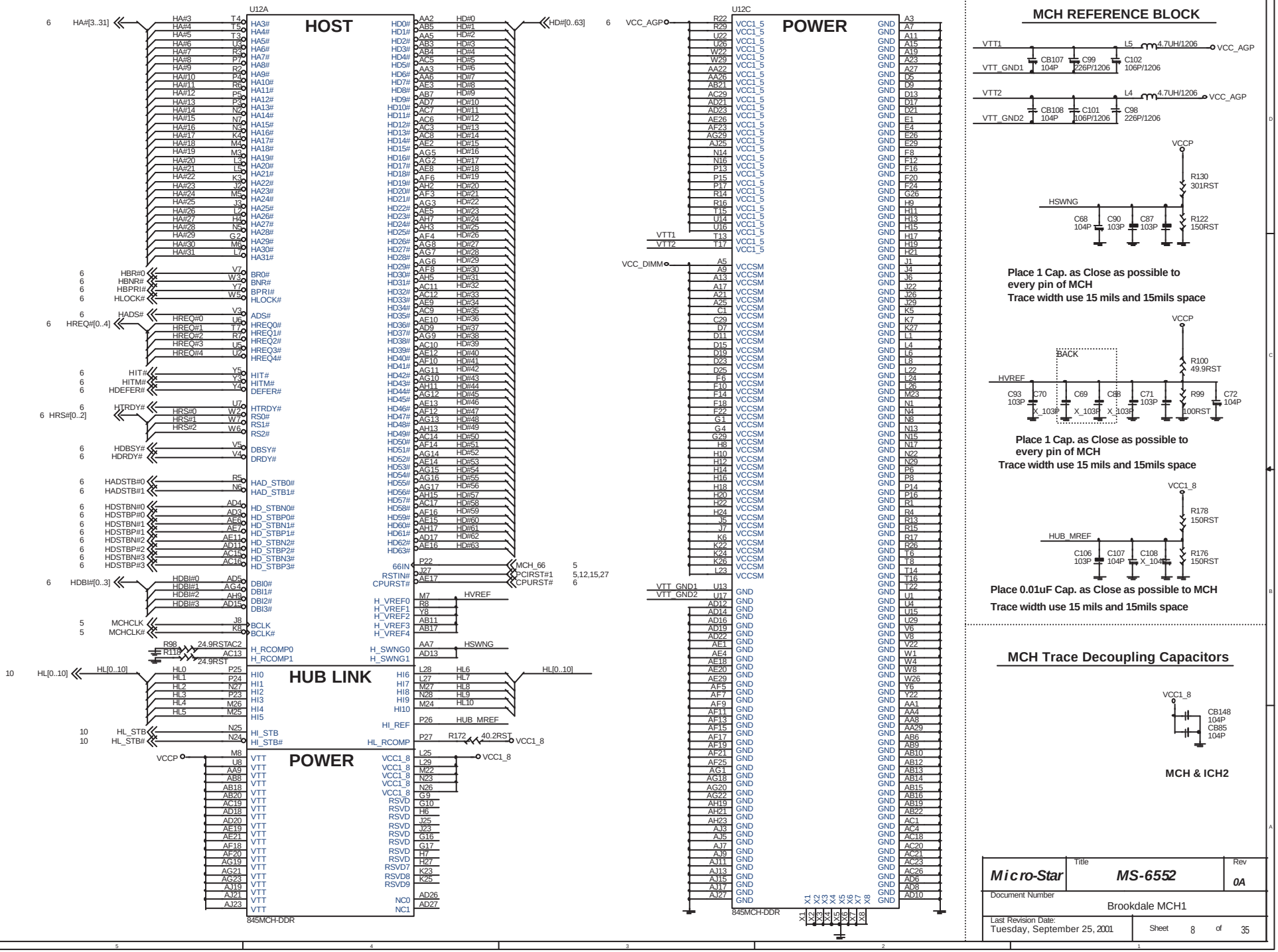
PLACE CAPS WITHIN CPU CAVITY

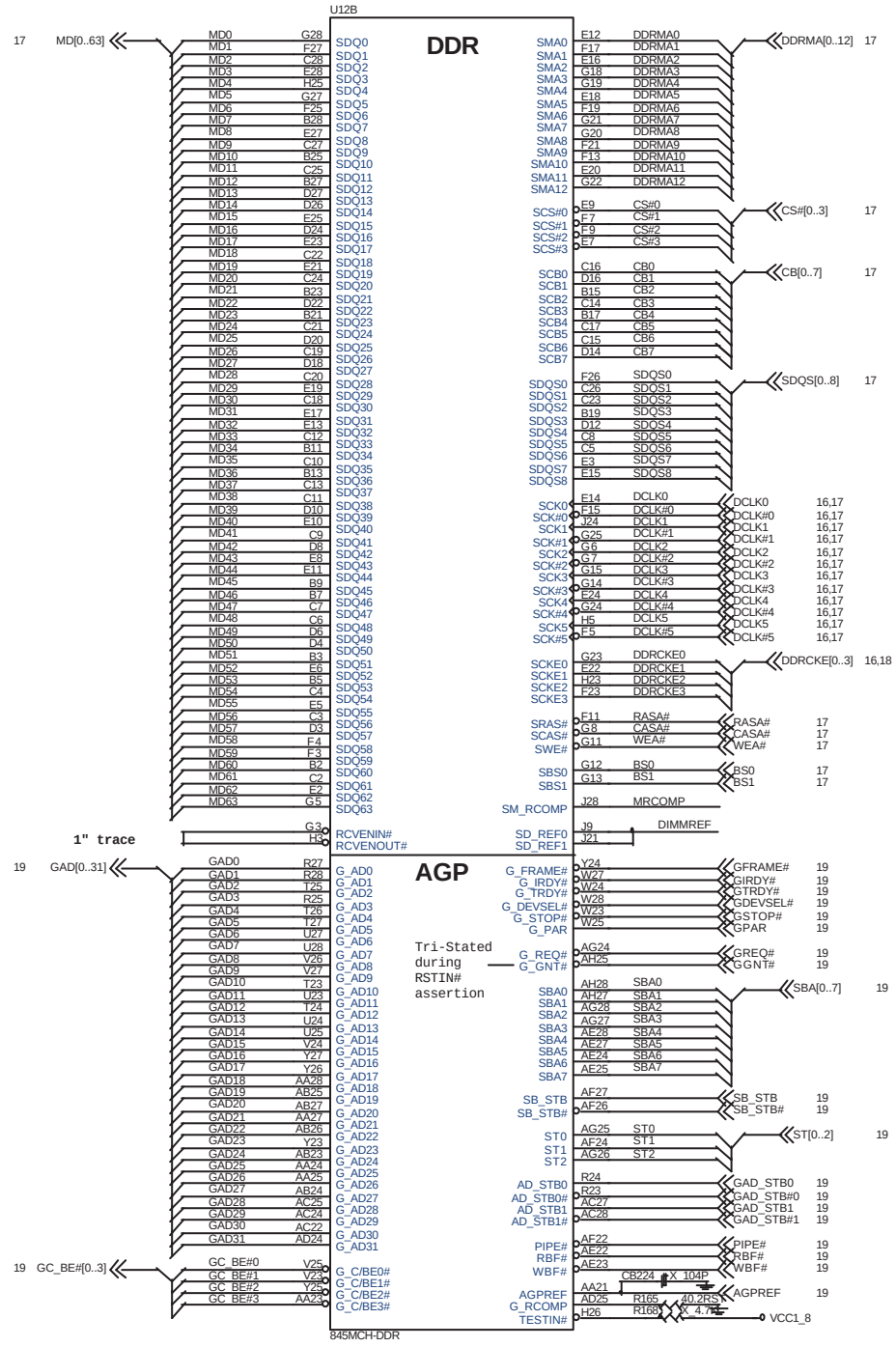
CPU DECOUPLING CAPACITORS



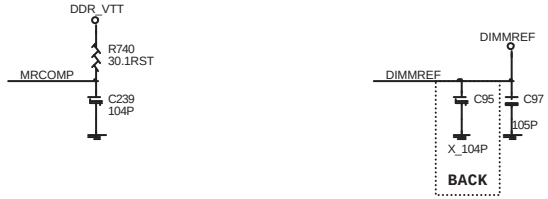
PLACE CAPS WITHIN CPU CAVITY SOLDER

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: INTEL mPGA478-B CPU2		
Last Revision Date: Wednesday, September 19,2001	Sheet 7 of 35	

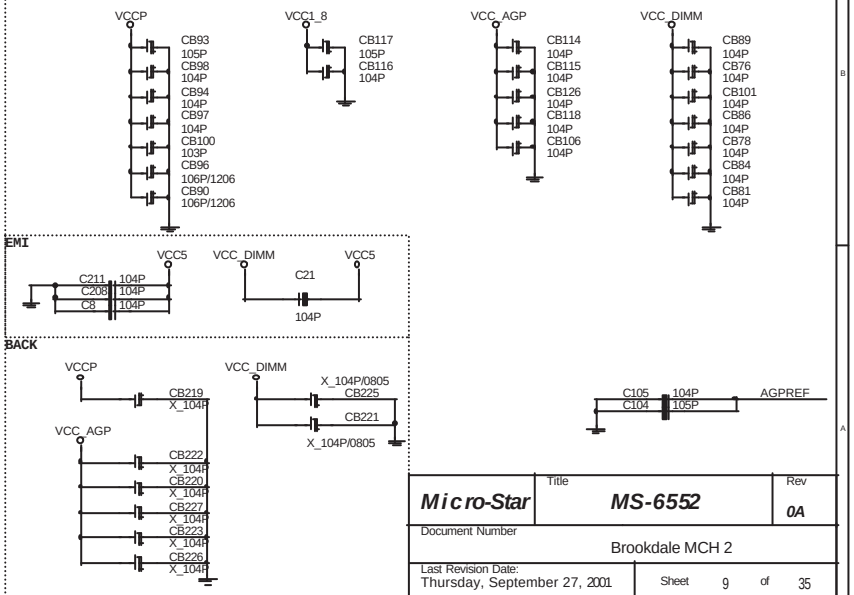

U12A
HOST
HA#[3..31]
HD#[0..63]
HBR#0
HBNR#
HBPRI#
HLOCK#
HADS#
HREQ#[0..4]
HIT#
HITM#
HDEFER#
HTRDY#
HRS#[0..2]
HDBSY#
HDRDY#
HADSTB#0
HADSTB#1
HDSTBN#0
HDSTBP#0
HDSTBN#1
HDSTBP#1
HDSTBN#2
HDSTBP#2
HDSTBN#3
HDSTBP#3
HDBI#[0..3]
MCHCLK
MCHCLK#
R98 24.9RSTAC2
R118 24.9RST
HL[0..10]
HL_STB
HL_STB#
VCCP
HUB LINK
HL[0..10]
HUB_MREF
R172 40.2RST
VCC1_8
POWER
845MCH-DDR
U12C
POWER
VCC_AGP
VCC_DIMM
VTT1
VTT2
VTT_GND1
VTT_GND2
845MCH-DDR
MCH REFERENCE BLOCK
VTT1
VTT_GND1
CB107 104P
C99 226P/1206
C102 106P/1206
L5 4.7UH/1206
VCC_AGP
VTT2
VTT_GND2
CB108 104P
C101 106P/1206
C98 226P/1206
L4 4.7UH/1206
VCCP
R130 301RST
HSWNG
C68 104P
C90 103P
C87 103P
R122 150RST
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
BACK
HVREF
R100 49.9RST
C93 103P
C70 X_103P
C69 X_103P
C88 X_103P
C71 103P
R99 100RST
C72 104P
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCC1_8
R178 150RST
HUB_MREF
C106 103P
C107 104P
C108 X_104P
R176 150RST
Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space
MCH Trace Decoupling Capacitors
VCC1_8
CB148 104P
CB85 104P
MCH & ICH2
Micro-Star
Title
MS-6552
Rev
0A
Document Number
Brookdale MCH1
Last Revision Date:
Tuesday, September 25, 2001
Sheet 8 of 35



MCH REFERENCE VOLTAGE

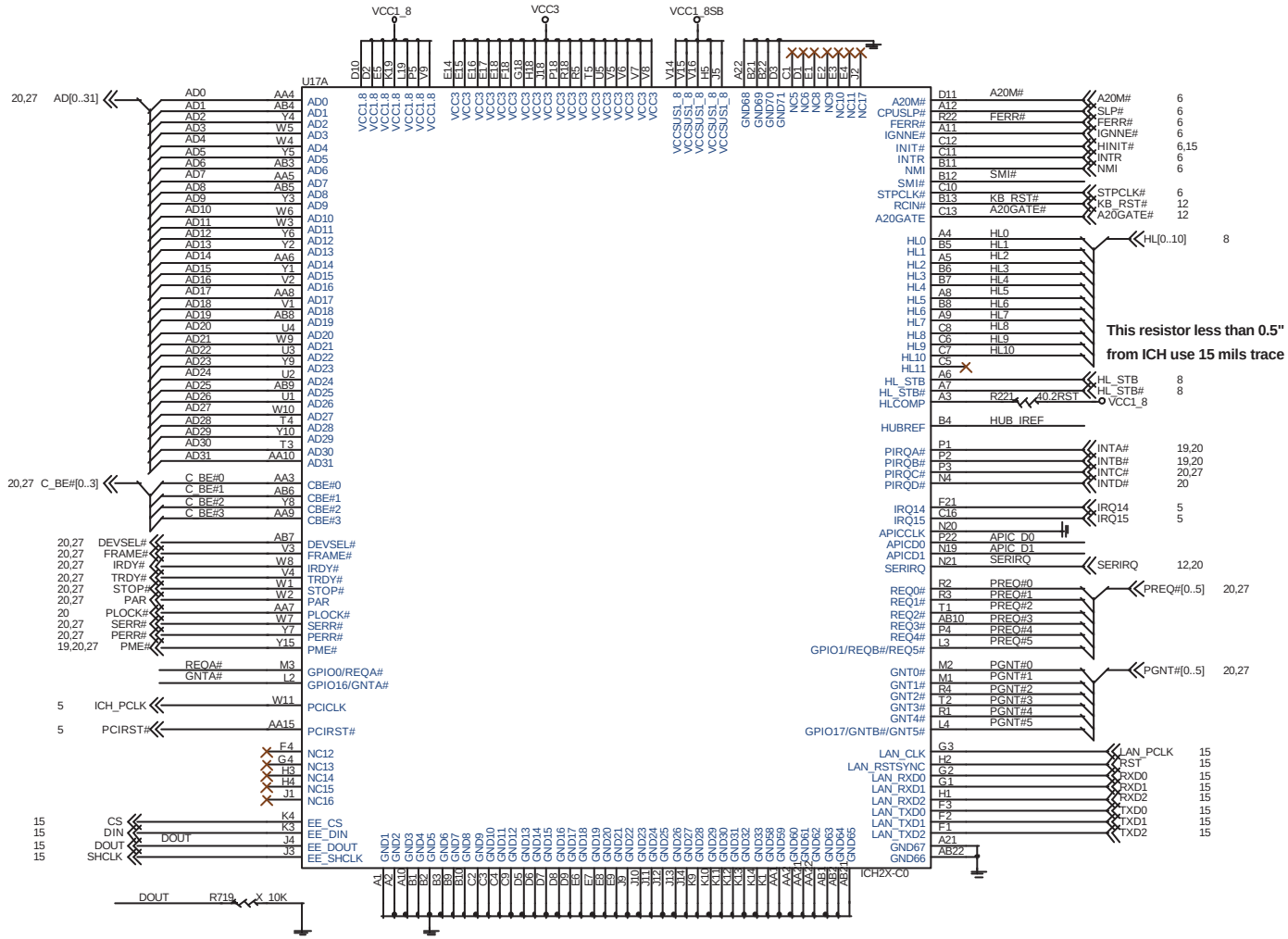


MCH DECOUPLING CAPACITOR

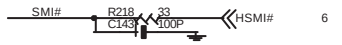


Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Brookdale MCH 2		
Last Revision Date: Thursday, September 27, 2001	Sheet 9 of 35	

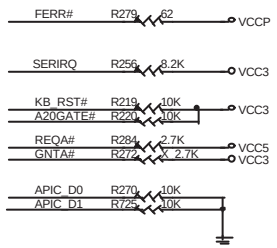
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



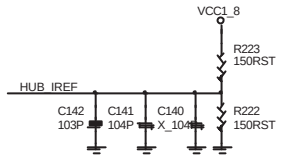
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

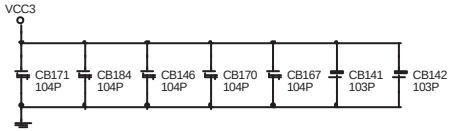


ICH2 REFERENCE VOLTAGE

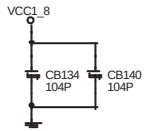


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

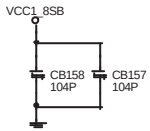
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



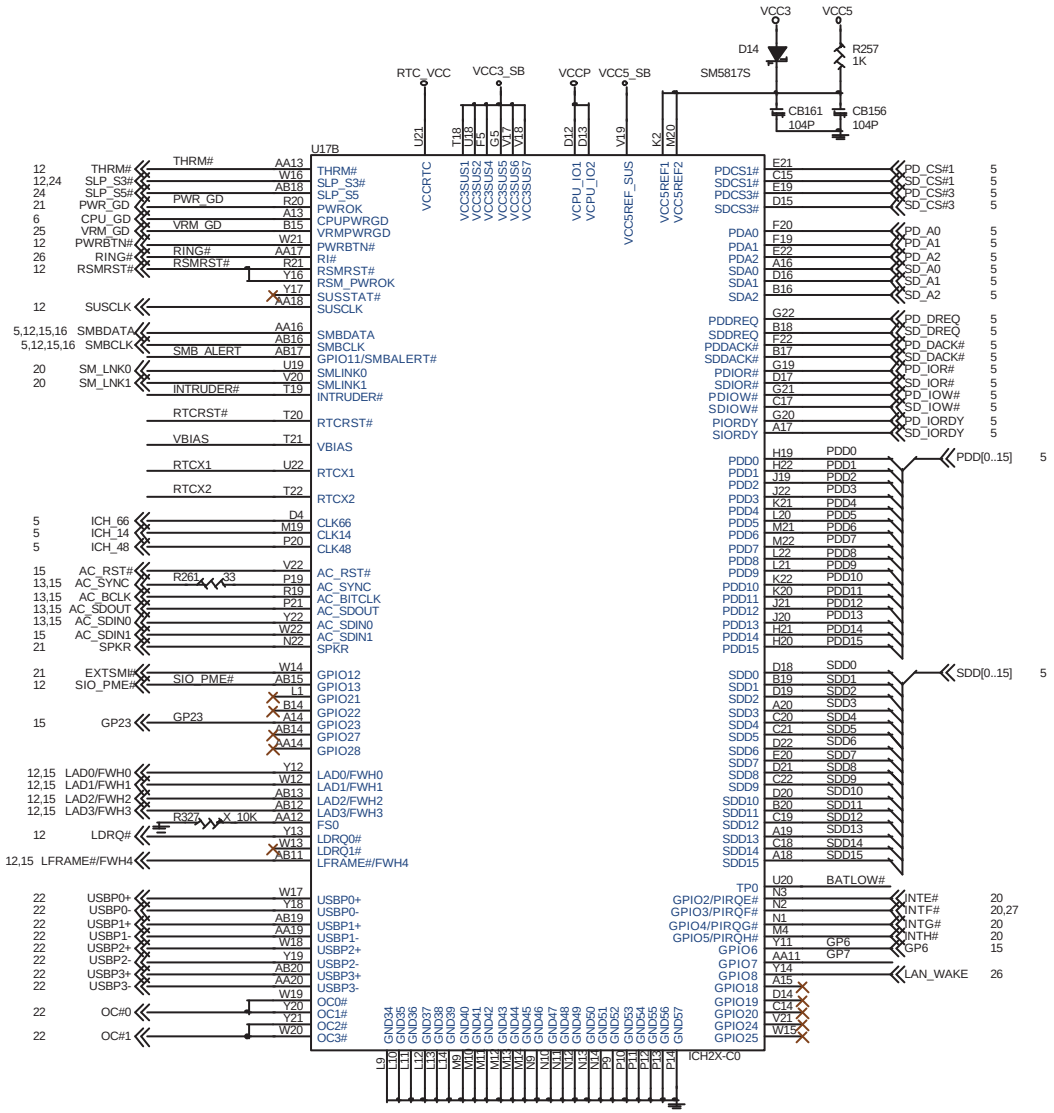
Distribute near the 1.8V power pin of the ICH2



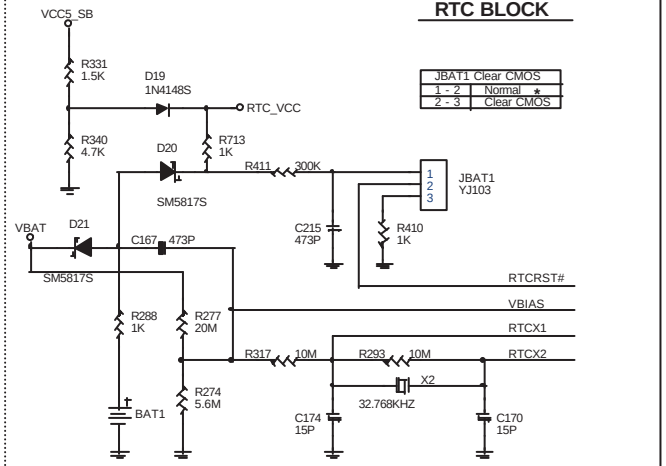
Distribute near the VCC1_8SB Power pin of the ICH2

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Brookdale ICH2 PCI		
Last Revision Date: Wednesday, September 12, 2001	Sheet 10 of 35	

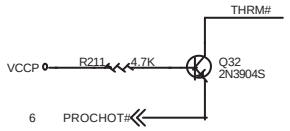
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

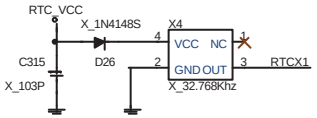


RTC BLOCK

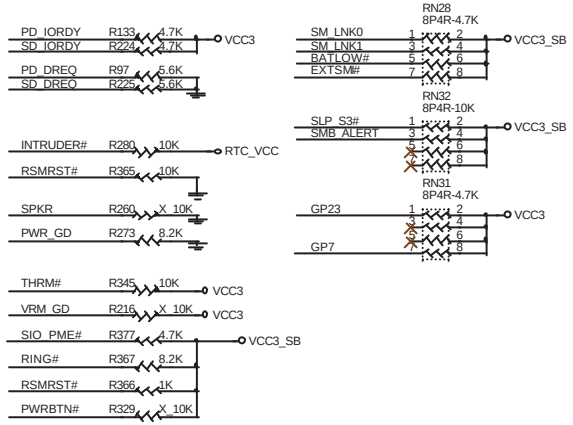


PROCHOT BLOCK

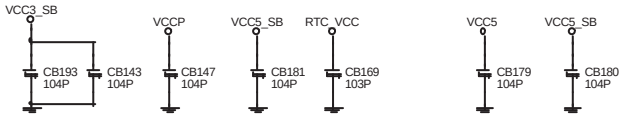




ICH2 STRAPPING RESISTORS



ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Brookdale ICH2 Other		
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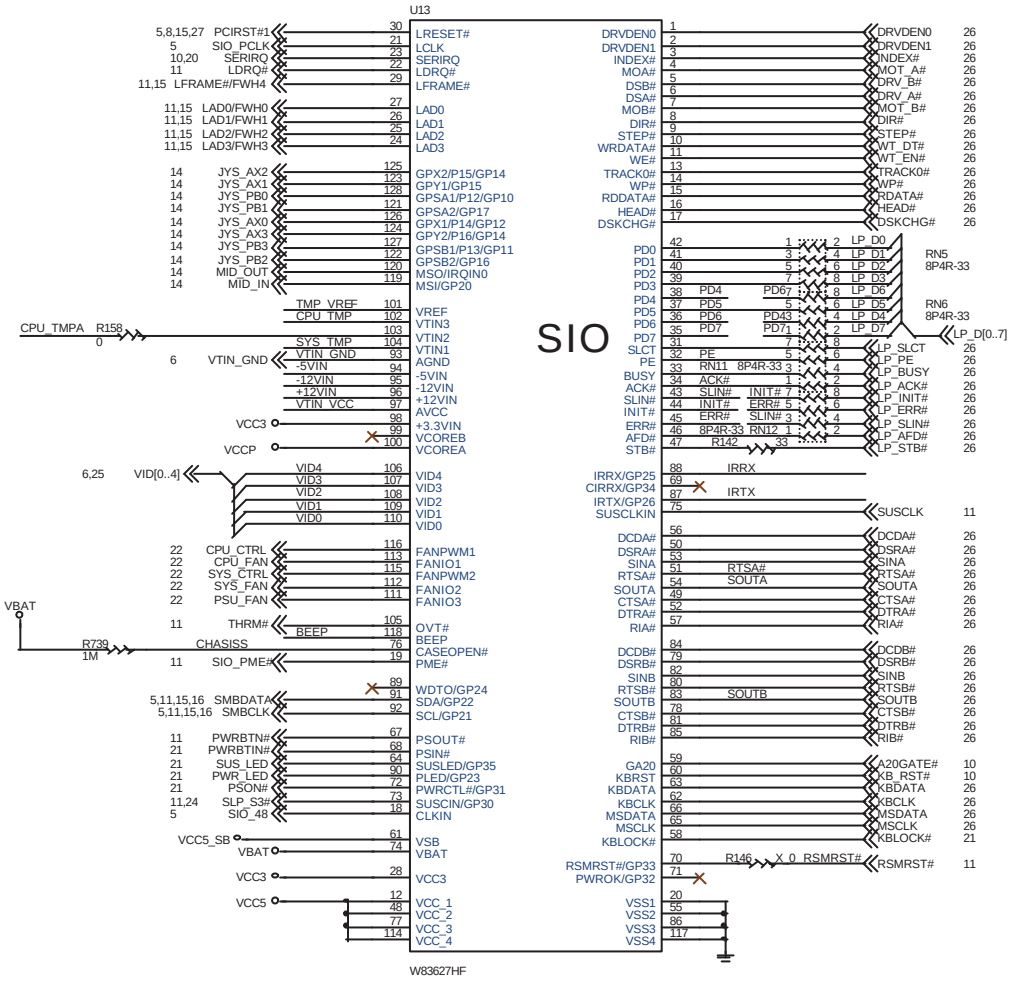
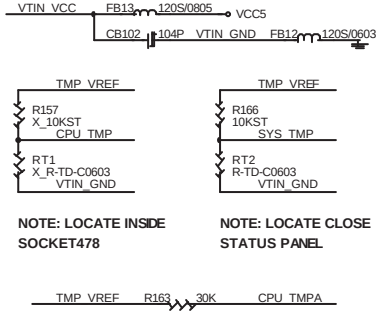
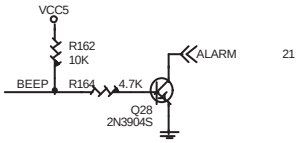
LPC SUPER I/O W83627HF



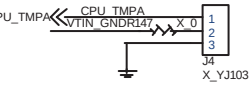
THERMAL RESISTOR BLOCK



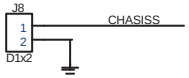
SPEAKER BLOCK



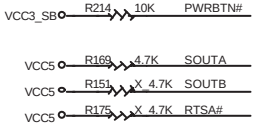
CPU Temperature Read



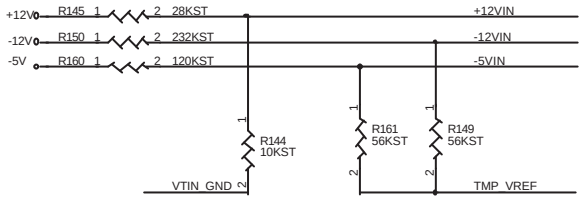
CHASISS INTRUSION HEADER



SUPER I/O STRAPPING RESISTOR

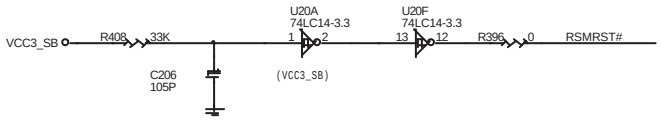


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

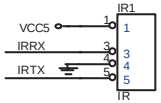


RESUME RESET CIRCUIT BLOCK

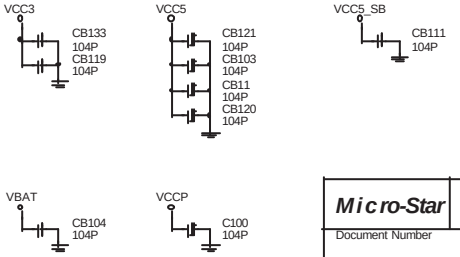
Stuff all for D Version bug



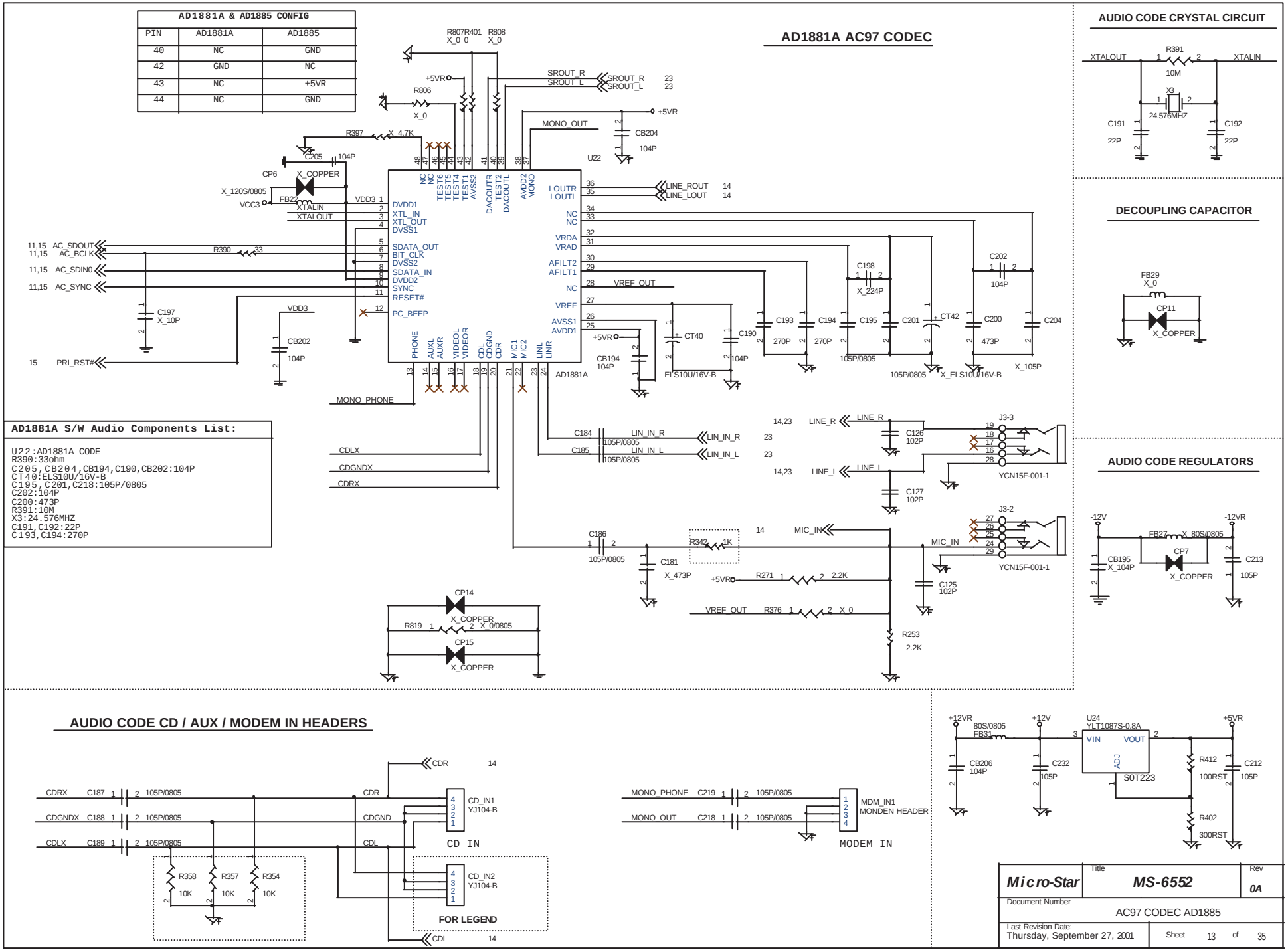
IR HEADER



DECOUPLING CAPACITOR



Micro-Star	Title: MS-6552		Rev: 0A
Document Number: LPC I/O W83627HF			
Last Revision Date: Wednesday, September 12, 2001		Sheet 12 of 35	


AD1881A & AD1885 CONFIG
PIN | AD1881A | AD1885
40 | NC | GND
42 | GND | NC
43 | NC | +5VR
44 | NC | GND
AD1881A AC97 CODEC
AUDIO CODE CRYSTAL CIRCUIT
XTALOUT
XTALIN
R391
10M
X3
24.576MHZ
C191
22P
C192
22P
DECOUPLING CAPACITOR
FB29
X_0
CP11
X_COPPER
AUDIO CODE REGULATORS
-12V
-12VR
FB27
X_80S/0805
CP7
X_COPPER
CB195
X_104P
C213
105P
AD1881A S/W Audio Components List:
U22:AD1881A CODE
R390:33ohm
C205,CB204,CB194,C190,CB202:104P
CT40:ELS10U/16V-B
C195,C201,C218:105P/0805
C202:104P
C200:473P
R391:10M
X3:24.576MHZ
C191,C192:22P
C193,C194:270P
AUDIO CODE CD / AUX / MODEM IN HEADERS
CD IN
CD_IN1
YJ104-B
CD_IN2
YJ104-B
MODEM IN
MDM_IN1
MONDEN HEADER
FOR LEGEND
U24
YLT1087S-0.8A
VIN
VOUT
ADJ
SOT223
+12VR
+12V
+5VR
Micro-Star
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MS-6552
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0A
Document Number
AC97 CODEC AD1885
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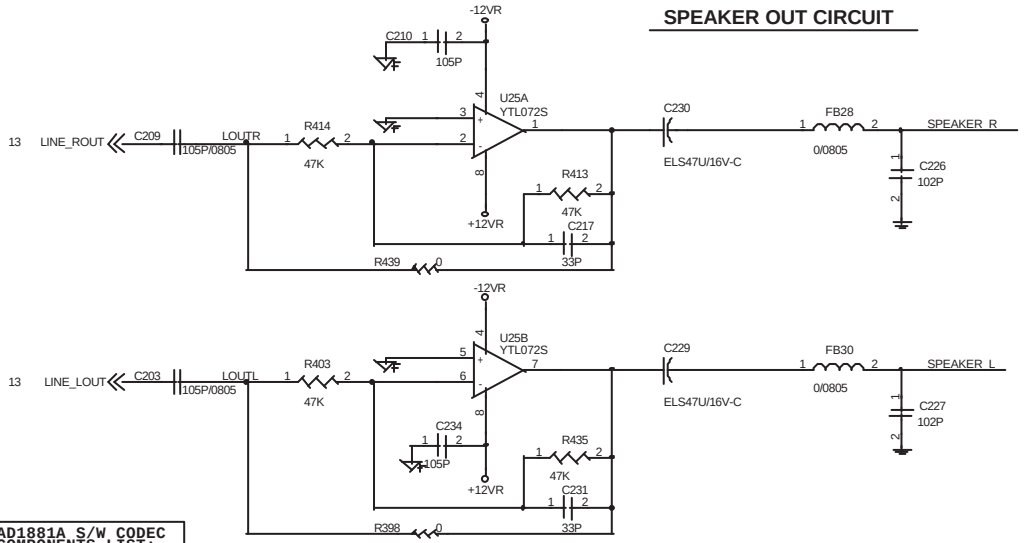
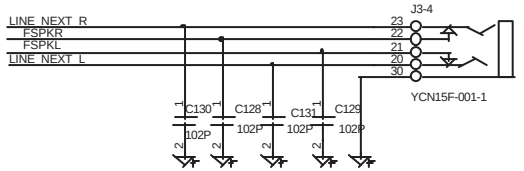
Thursday, September 27, 2001
Sheet 13 of 35

SPEAKER OUT CIRCUIT



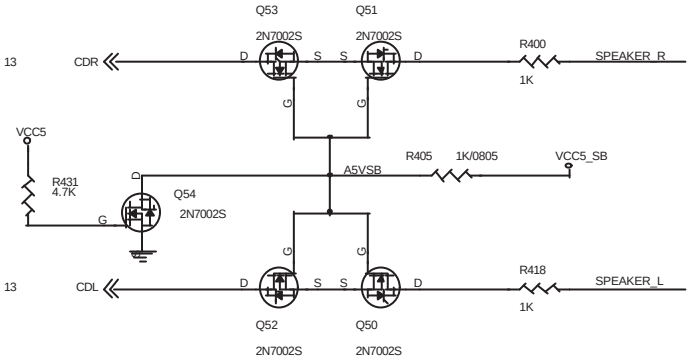
SPEAKER OUT JACK



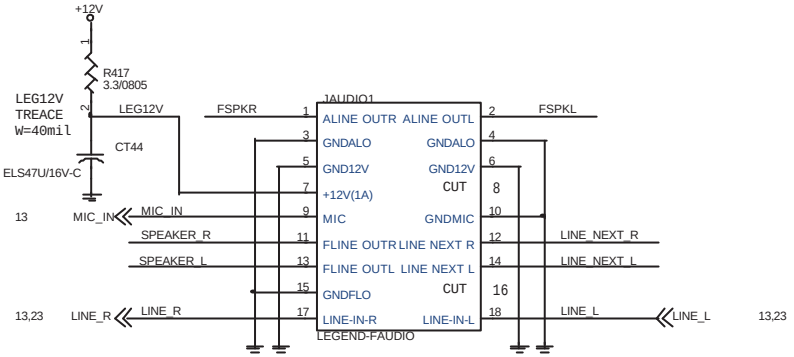
AD1881A S/W CODEC COMPONENTS LIST:

C210,C234:105P
R414,R435,R413,R403:47K
C217,C231:33P
R439,R398:NC

CD PANEL PLAY WITHOUT PC POWER_ON

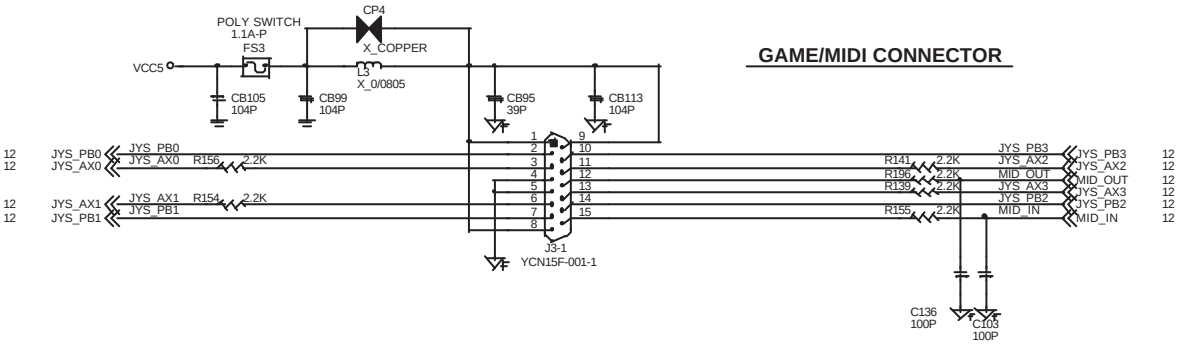


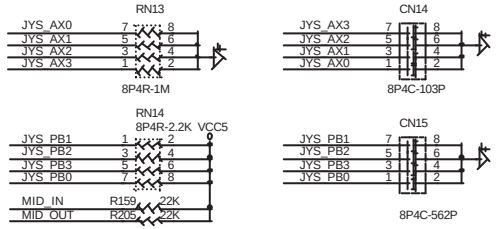
FOR MSI INTERNAL HEADER



FOR LEGEND

GAME/MIDI CONNECTOR





Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Audio Amp TL072 & GAME		
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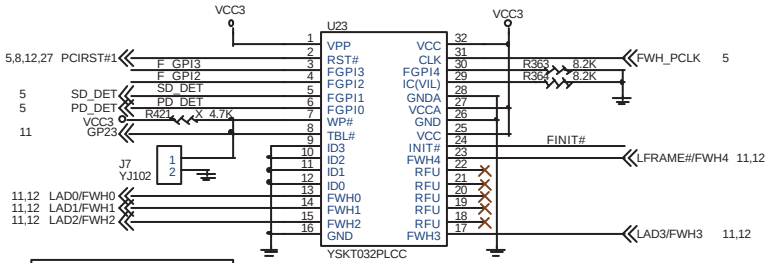
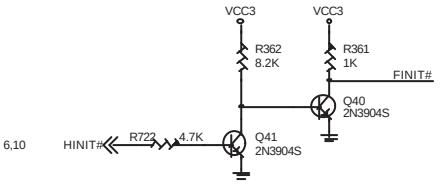
Firware Hub (FWH)

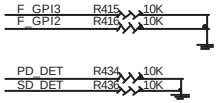


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

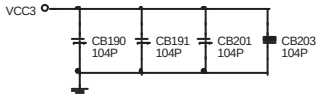
FWH INIT Signal Voltage Translation Block



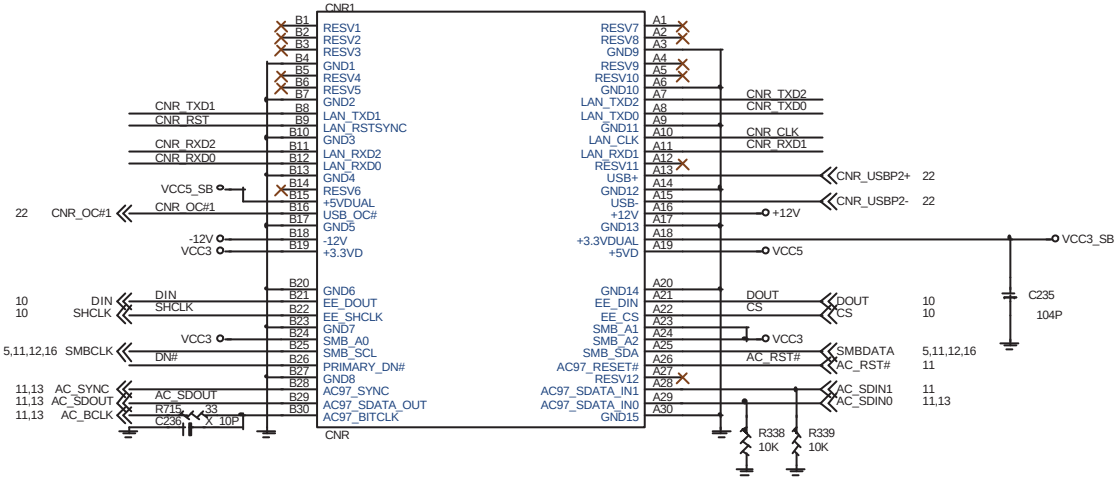
FWH RESISTORS



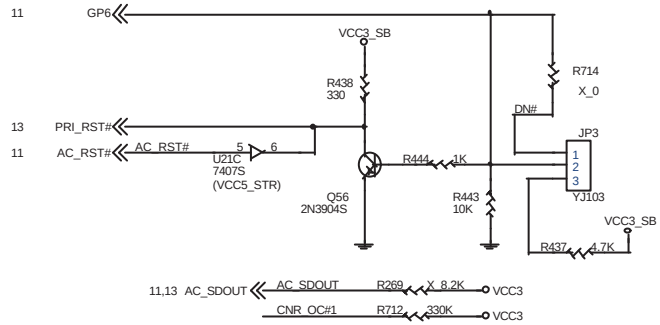
FWH DECOUPLING CAPACITORS



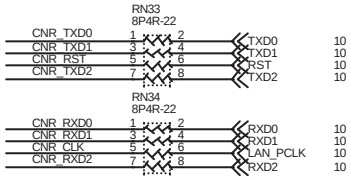
CNR RISER



JP3	AUDIO DOWN
1 - 2	Auto mode
2 - 3	Disabled onboard audio codec



NEAR ICH2



2.5"<L<9"

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: FWH & CNR		
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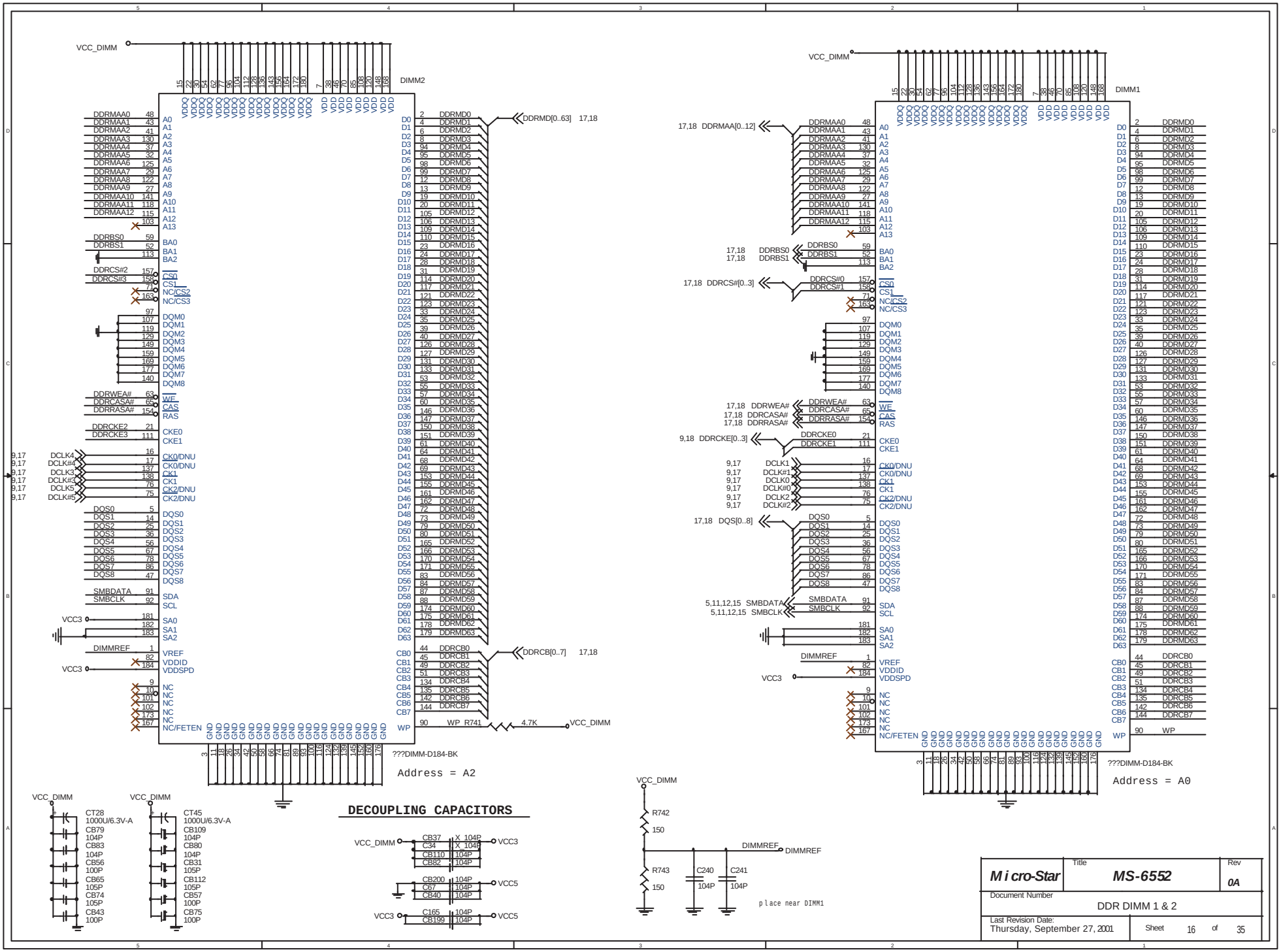

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Document Number: DDR DIMM 1 & 2		
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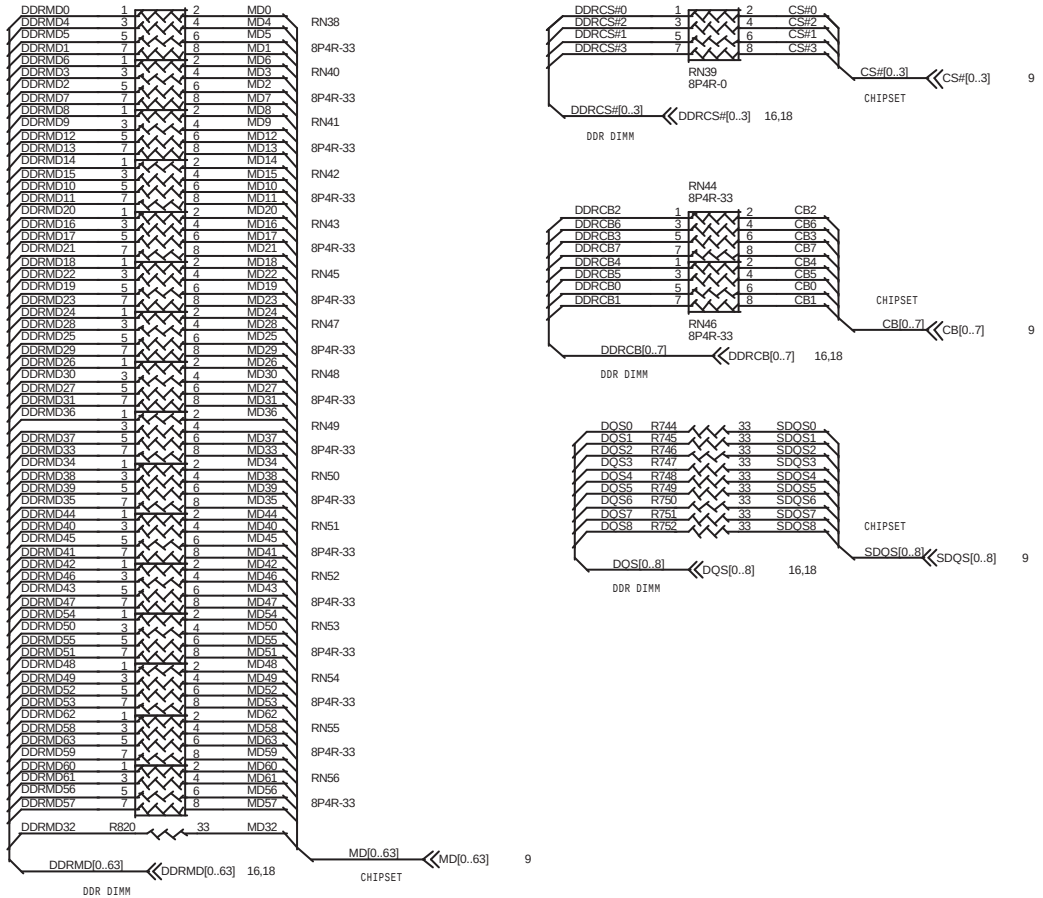
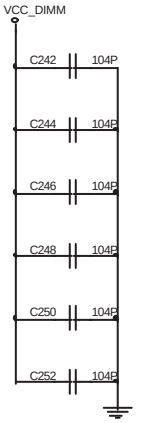
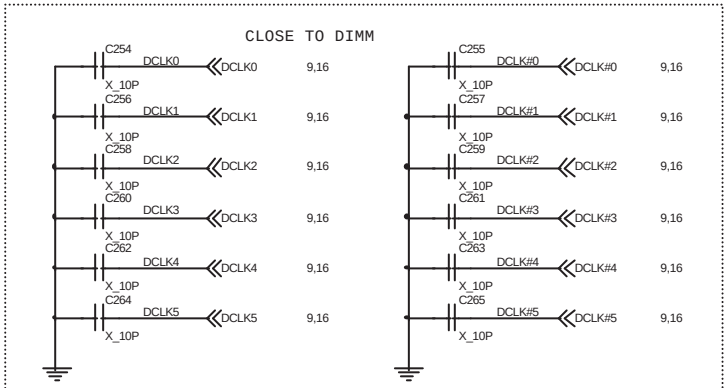
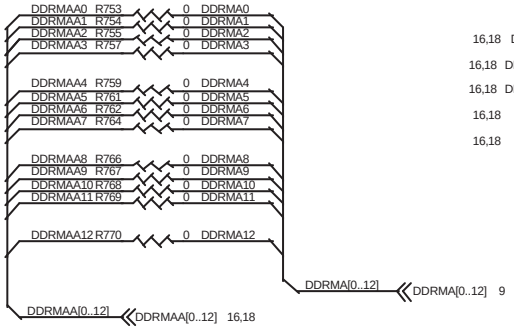
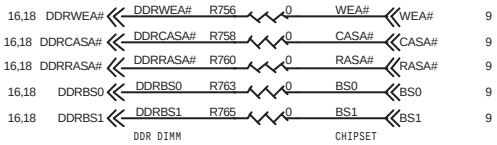
DDR DAMPING











Micro-Star	Title: MS-6552		Rev: 0A
Document Number: DDR DAMPING			
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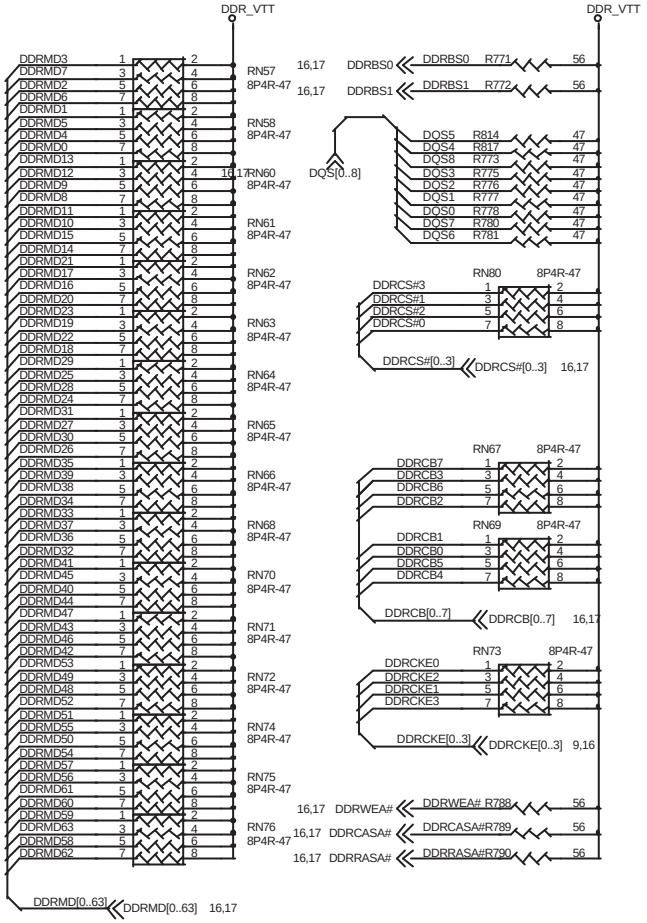
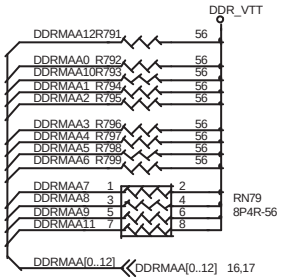
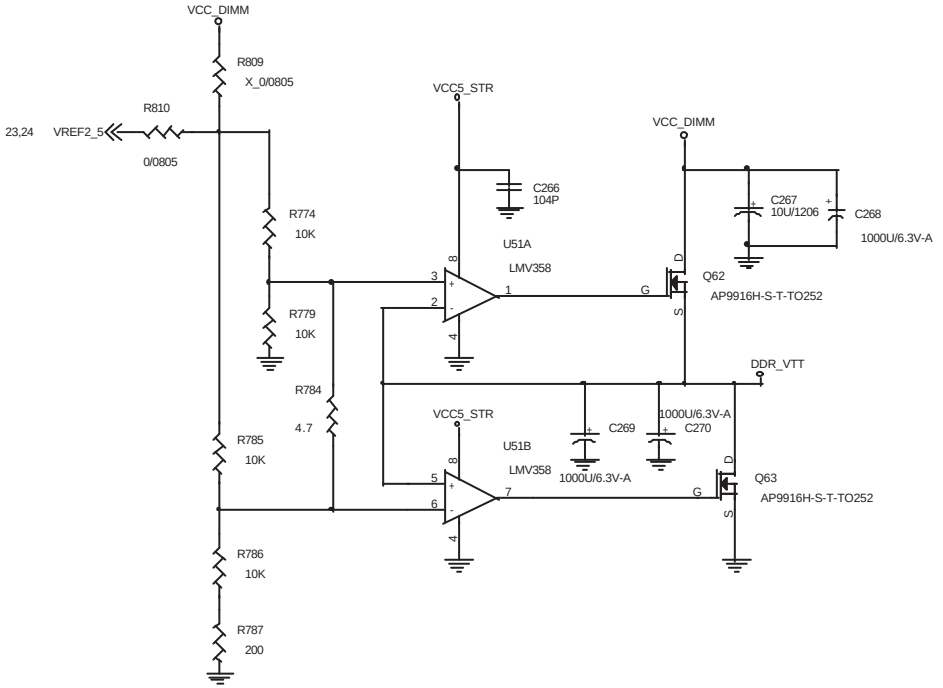
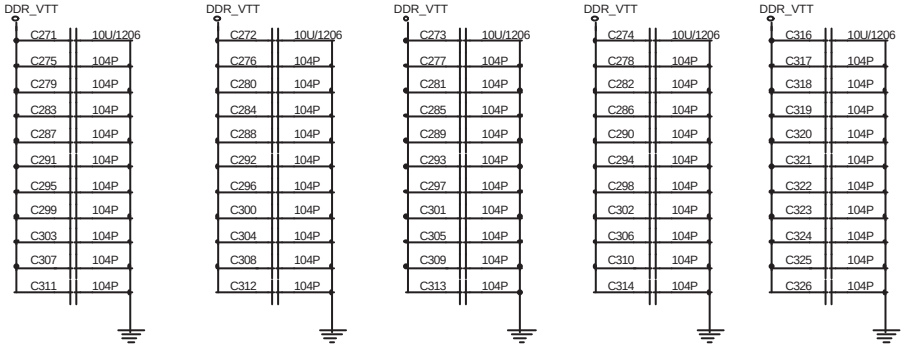
DDR TERMINATION





DDR POWER





Micro-Star	Title: MS-6552	Rev: 0A
Document Number: DDR TERMINATION & POWER		
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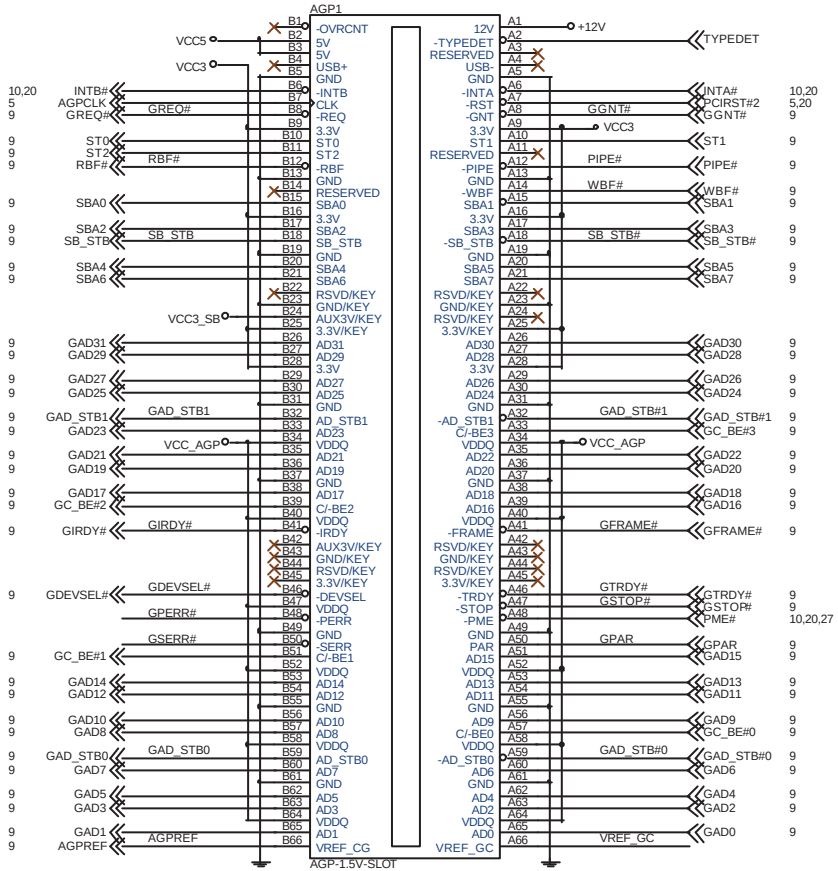
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

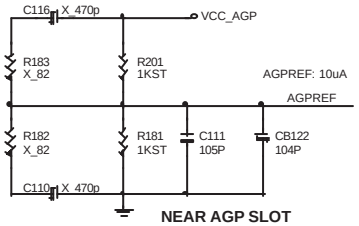
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

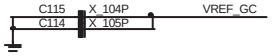
VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#

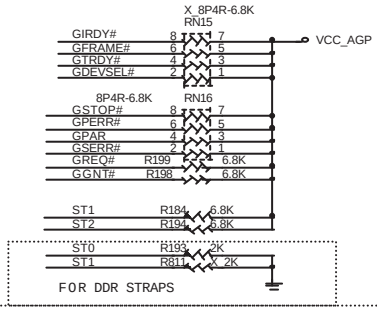
AGP SIGNAL REFERENCE CIRCUIT

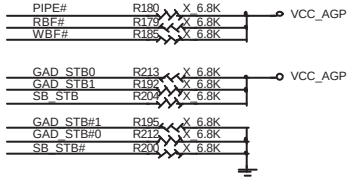


NEAR AGP SLOT



AGP TERMINATION RESISTORS

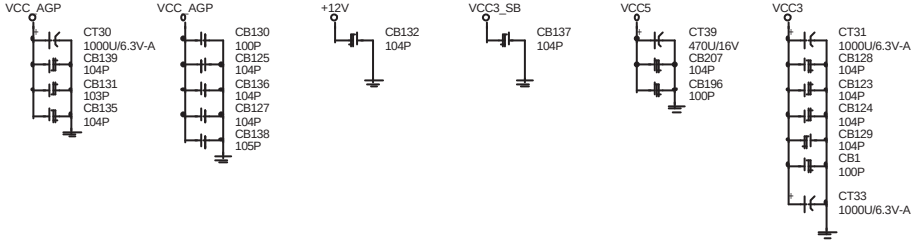




LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6552	Rev: 0A
Document Number: AGP Slot		
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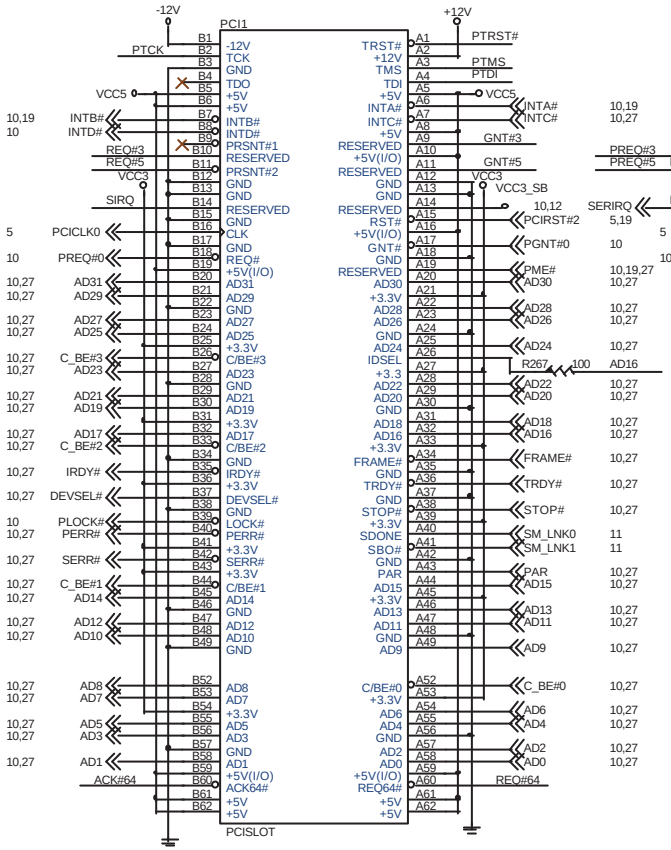
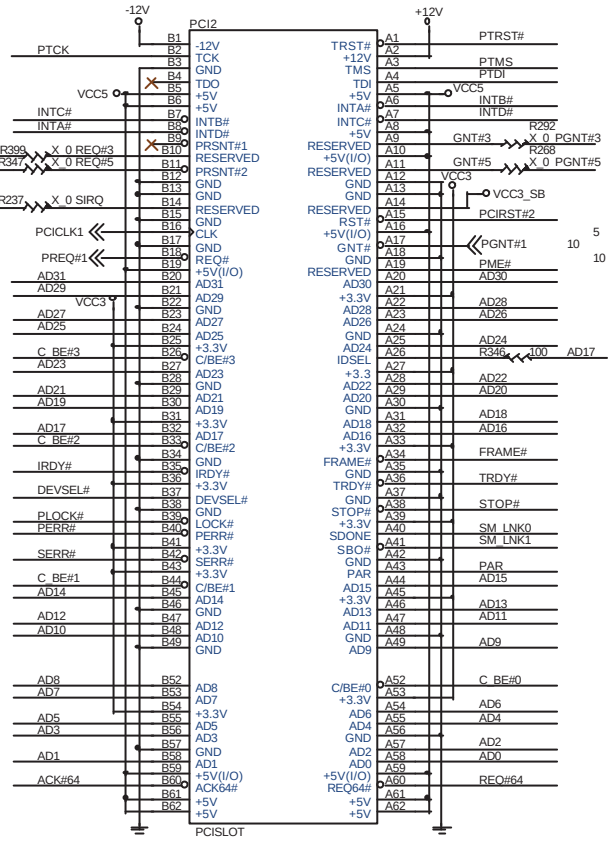
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



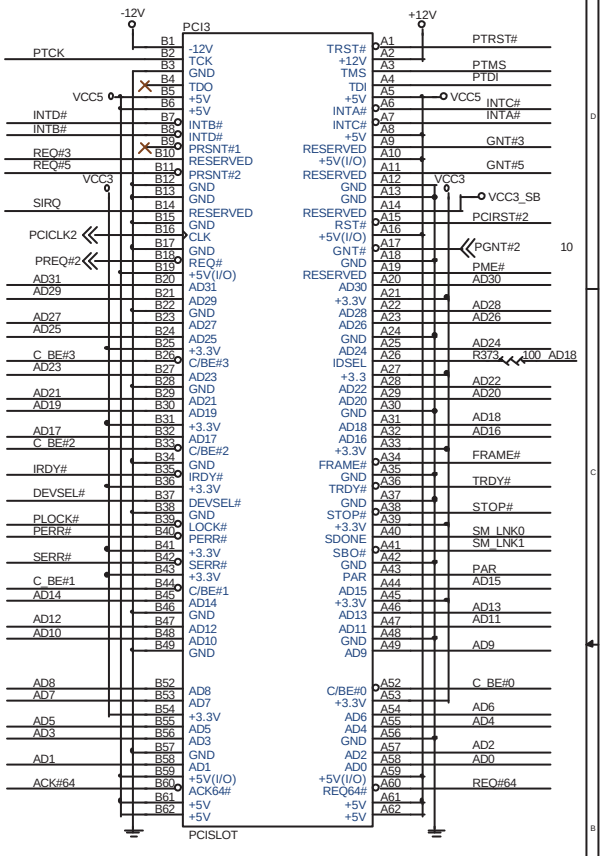
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



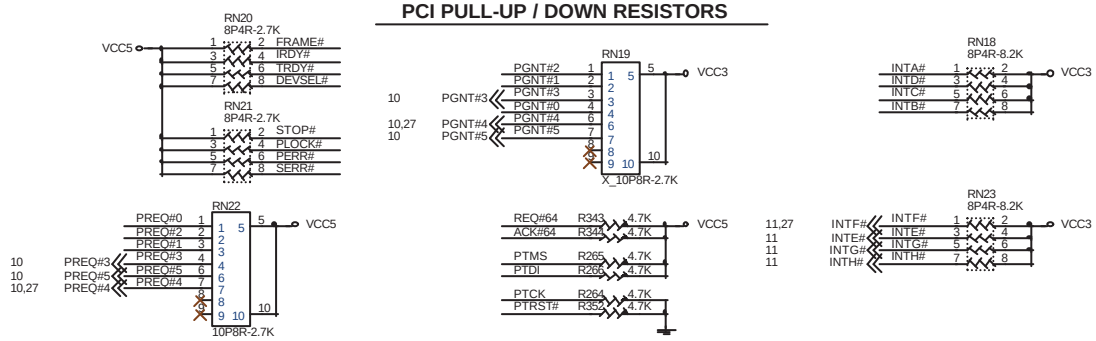
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

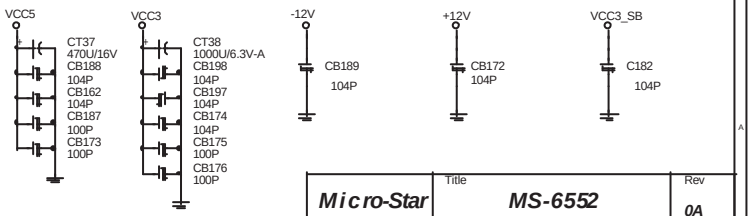


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6552	Rev: 0A
Document Number: PCI Slot 1 & 2 & 3		
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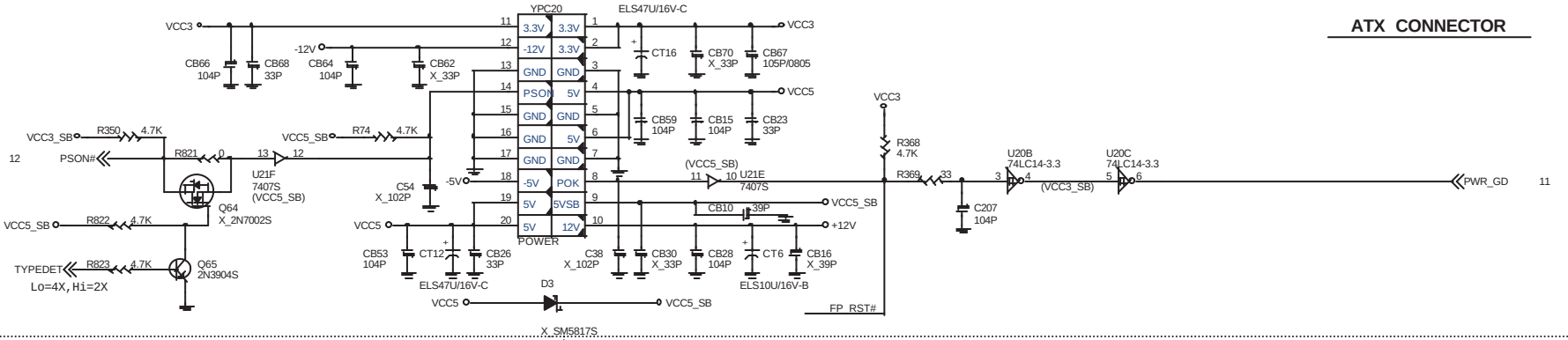
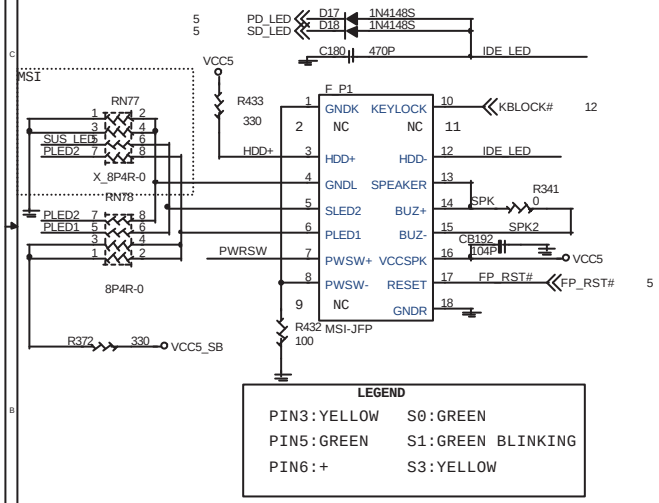
ATX CONNECTOR



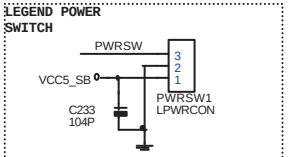
Brookdale FRONT PANEL-M

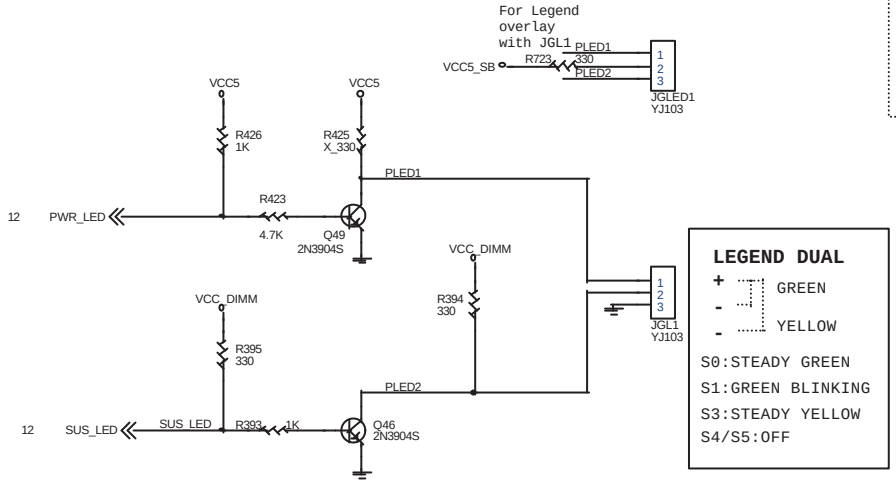


LEGEND

PIN3:YELLOW	S0:GREEN
PIN5:GREEN	S1:GREEN BLINKING
PIN6:+	S3:YELLOW

LEGEND POWER SWITCH

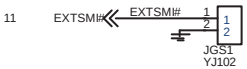




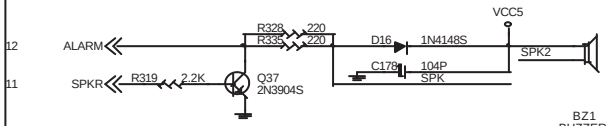
LEGEND DUAL

+	GREEN
-	YELLOW
-	

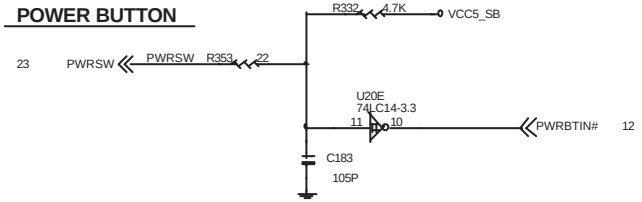
S0:STEADY GREEN
S1:GREEN BLINKING
S3:STEADY YELLOW
S4/S5:OFF



SPEAKER



POWER BUTTON



Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Front Panel & Connector		
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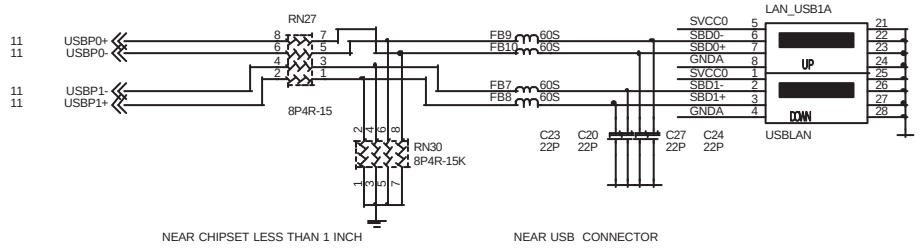
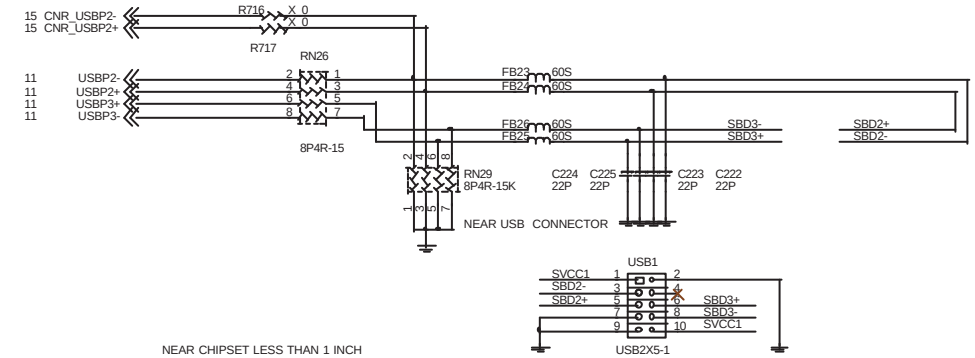
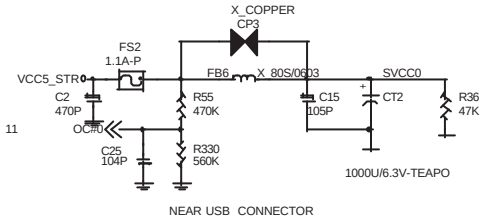
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



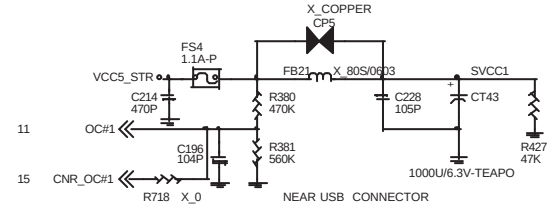
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



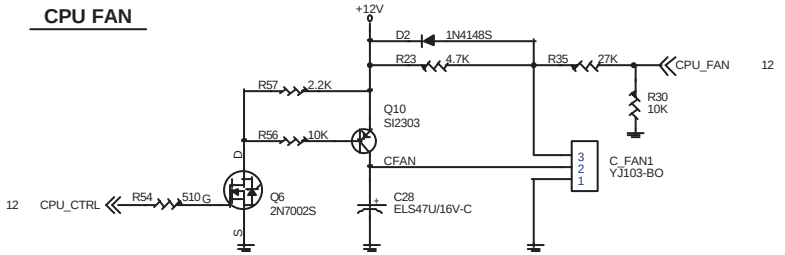
POWER CIRCUIT FOR USB PORT 0,1



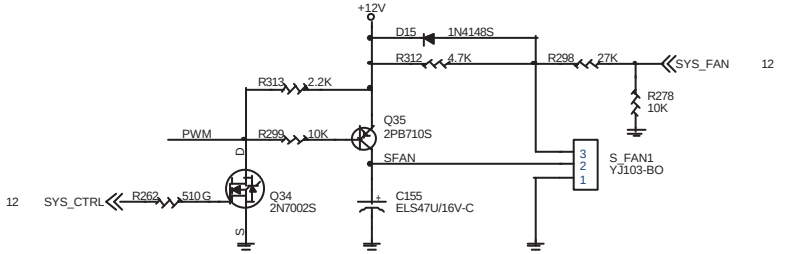
POWER CIRCUIT FOR USB PORT 2, 3



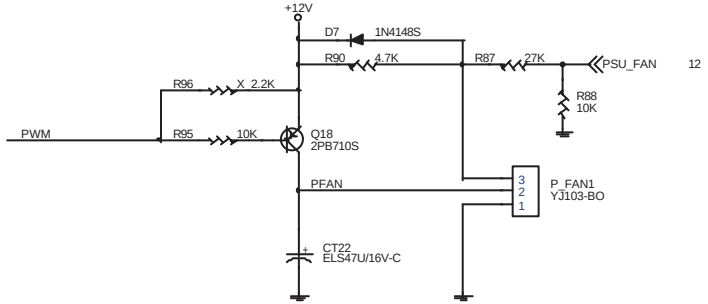
CPU FAN



SYSTEM FAN



ATX PSU FAN ON/OFF CONTROL

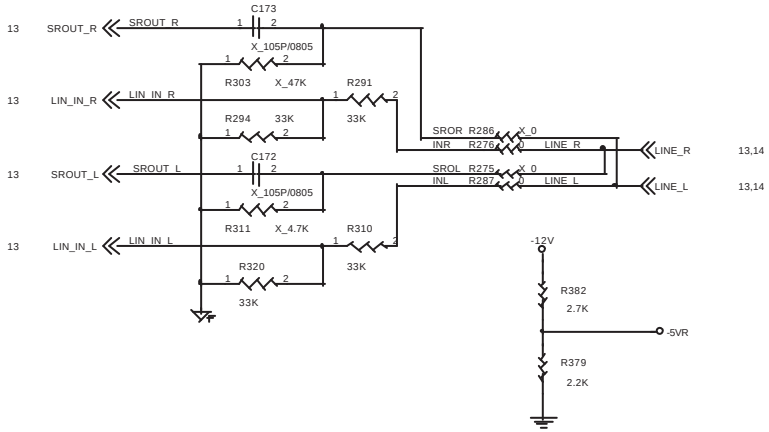


Micro-Star	Title: MS-6552	Rev: 0A
Document Number: USB & FAN Connectors		
Last Revision Date: Wednesday, September 12, 2001	Sheet 22 of 35	

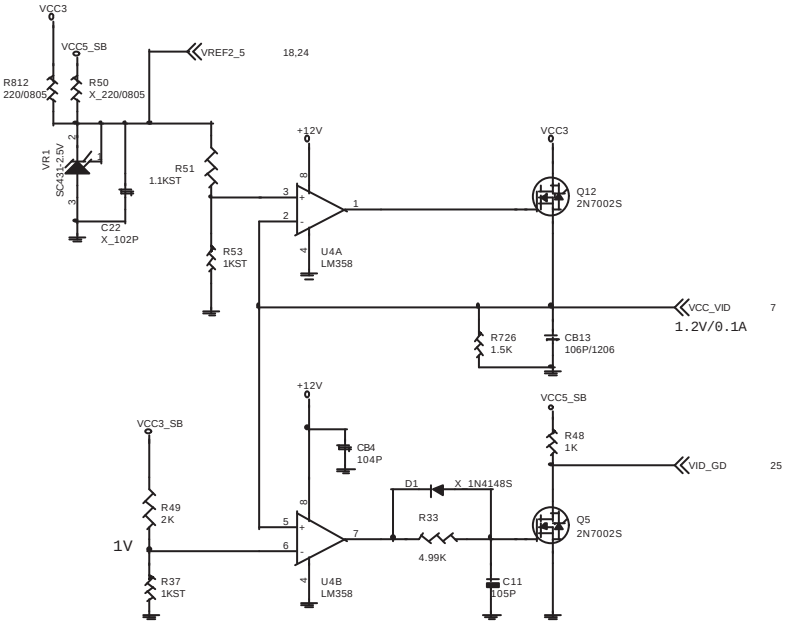
6 CHANNEL CONTROLLER

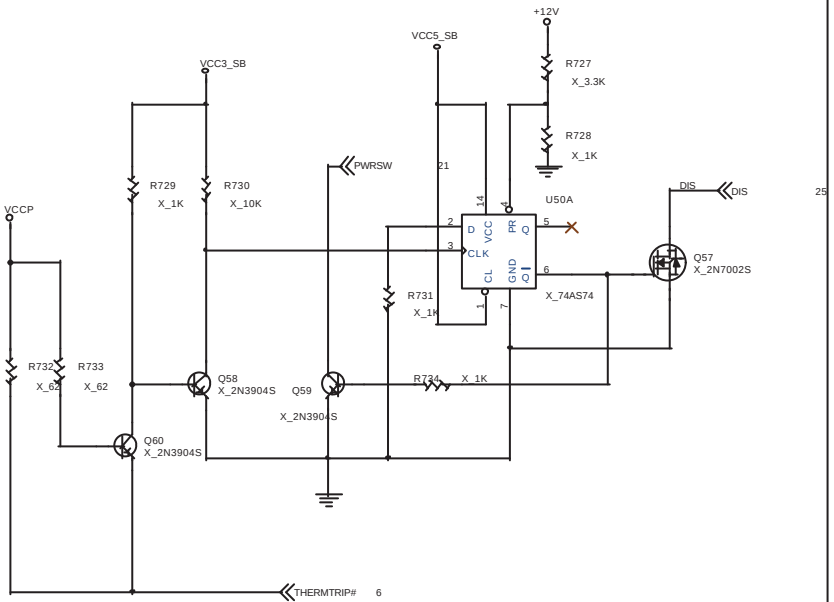
AD1881A S/W CODEC COMPONENTS LIST:

R217:0ohm
C160,R238,C163,R249,U16,C133,R382,R379:X



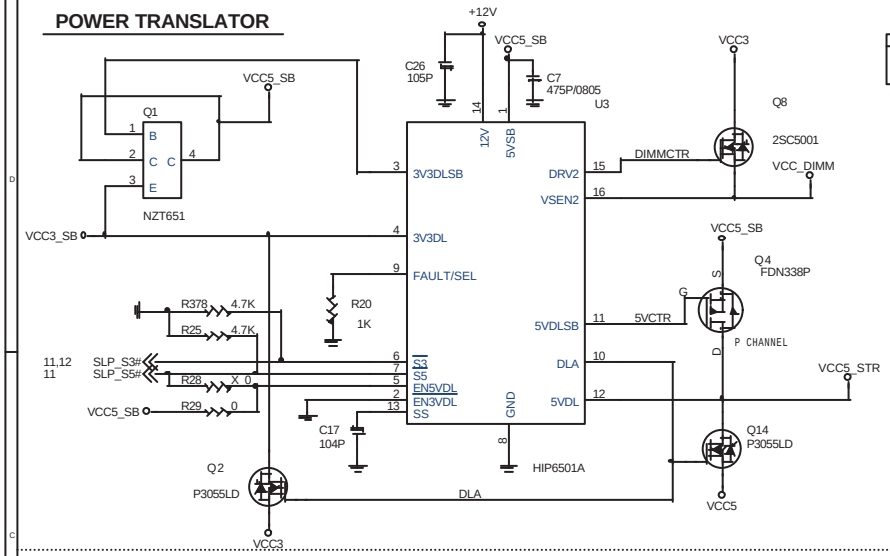
VCC_VID / VID_GOOD





Micro-Star	Title: MS-6552	Rev: 0A
Document Number: VID & 6 CHANNEL CONTROL		
Last Revision Date: Wednesday, September 12,2001	Sheet 23 of 35	

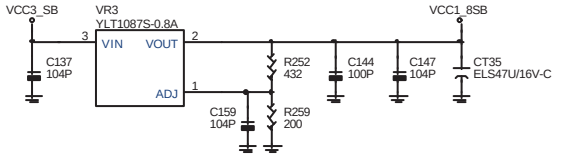
POWER TRANSLATOR



Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V

1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

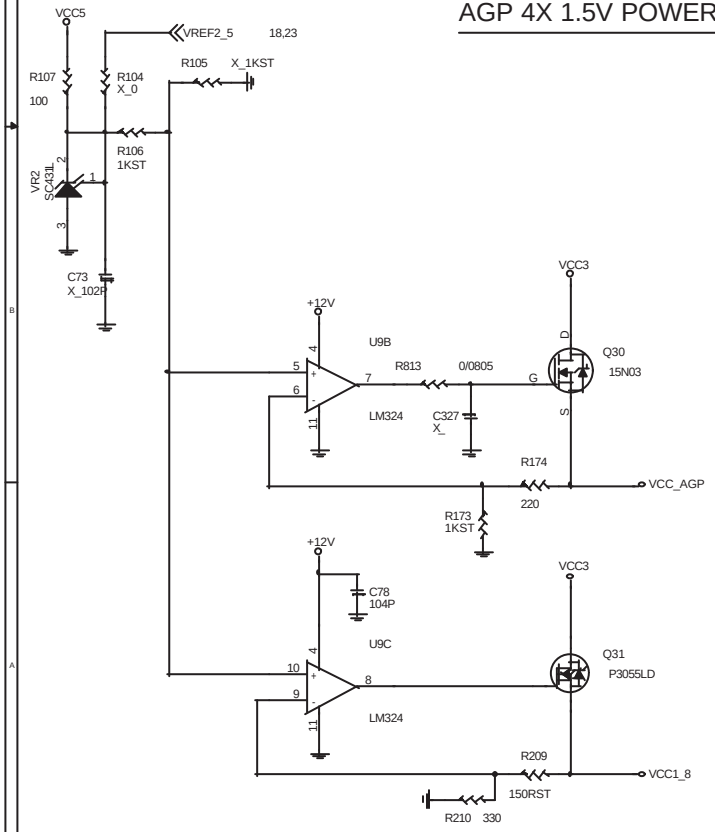
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

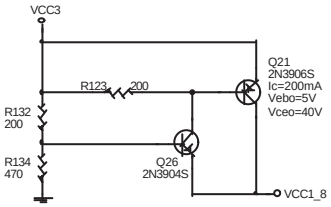
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

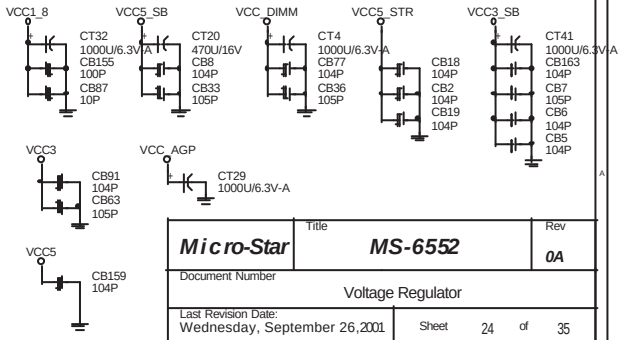
AGP 4X 1.5V POWER TRANSLATOR



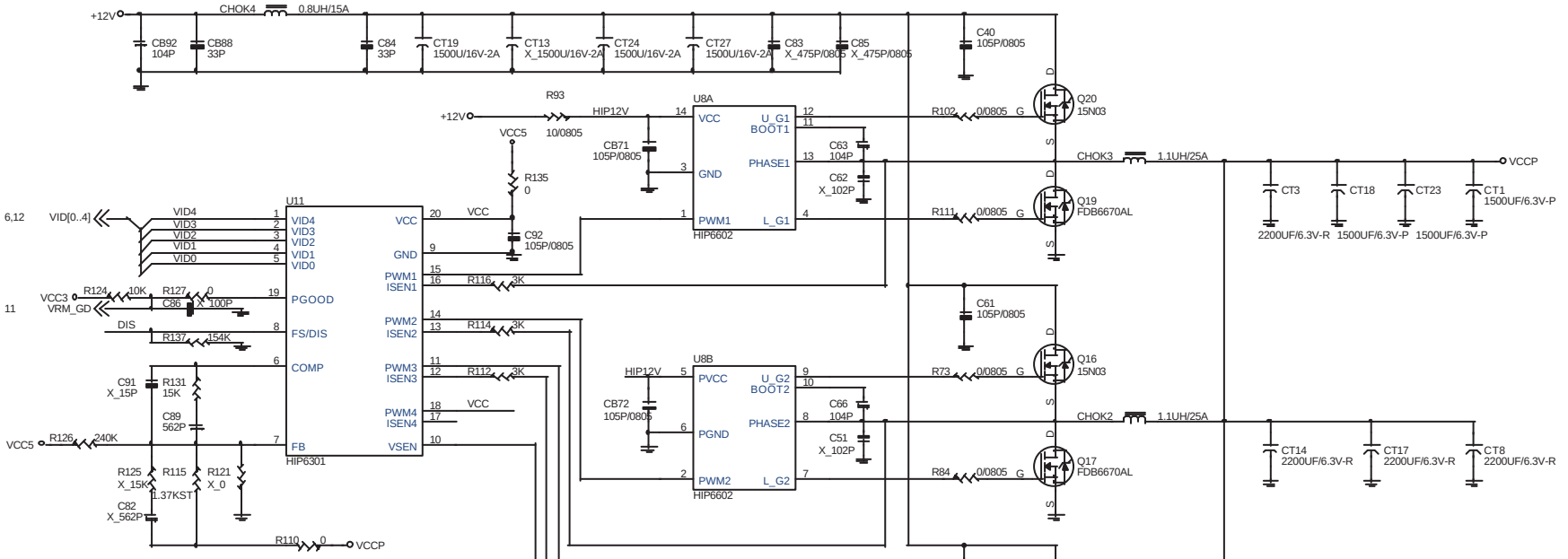
1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6552	Rev: 0A
	Document Number: Voltage Regulator	
	Last Revision Date: Wednesday, September 26,2001	Sheet 24 of 35

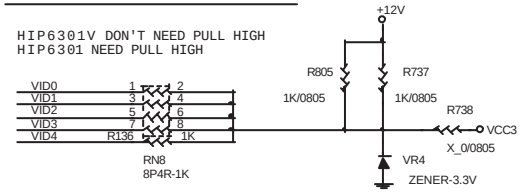


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

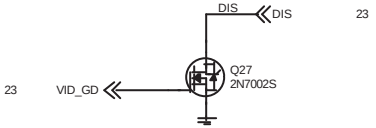
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

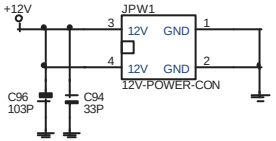
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWM GOOD

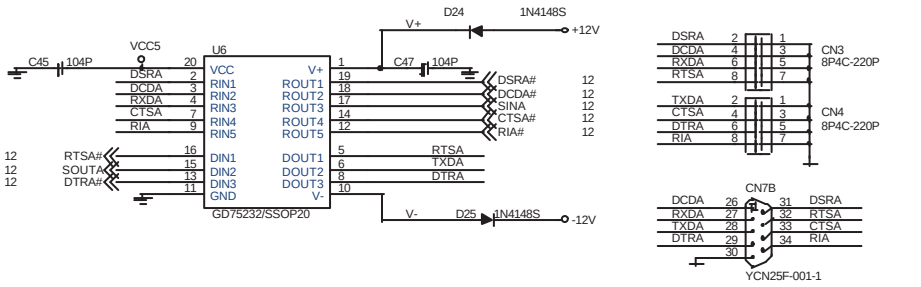


ATX12V POWER CONNECTOR

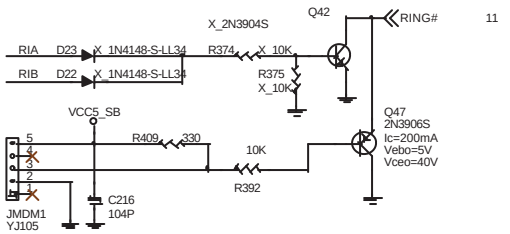


Micro-Star	Title: MS-6552	Rev: 0A
Document Number: VRM 9.0		
Last Revision Date: Monday, October 01, 2001	Sheet 25 of 35	

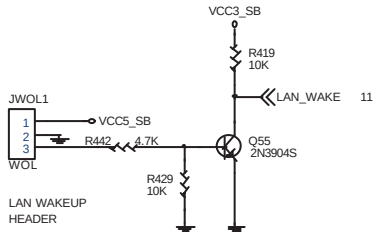
SERIAL PORT 1



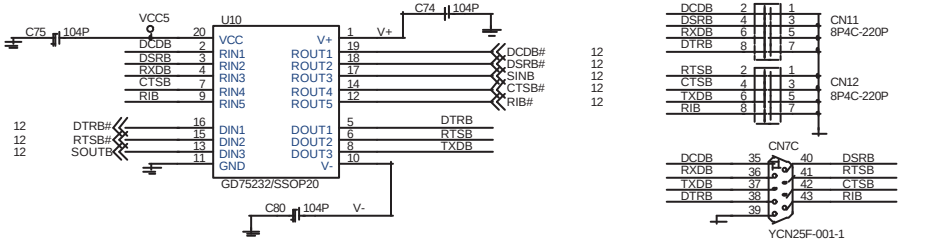
MODEM RING BLOCK



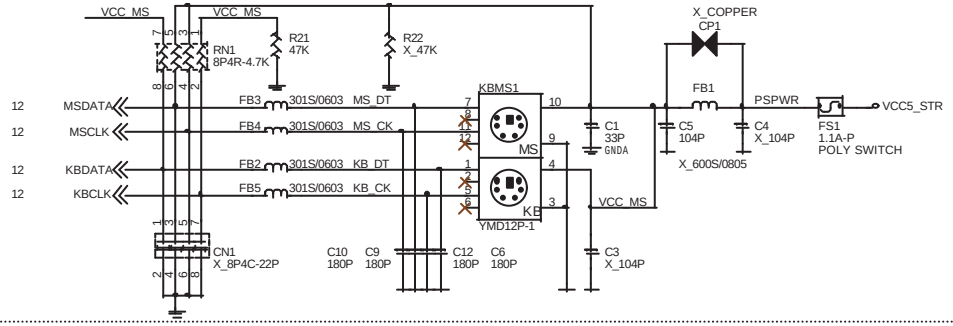
LAN WAKEUP BLOCK



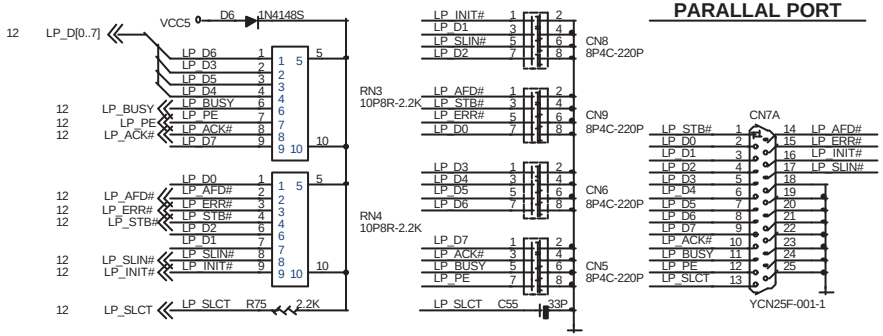
SERIAL PORT 2



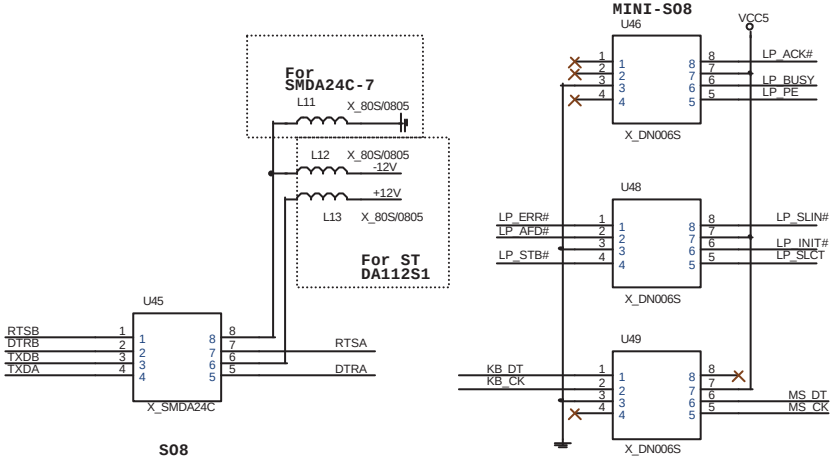
PS2 KEYBOARD & MOUSE CONNECTOR



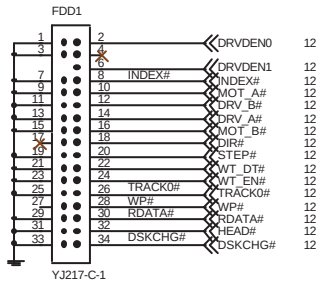
PARALLAL PORT



ESD

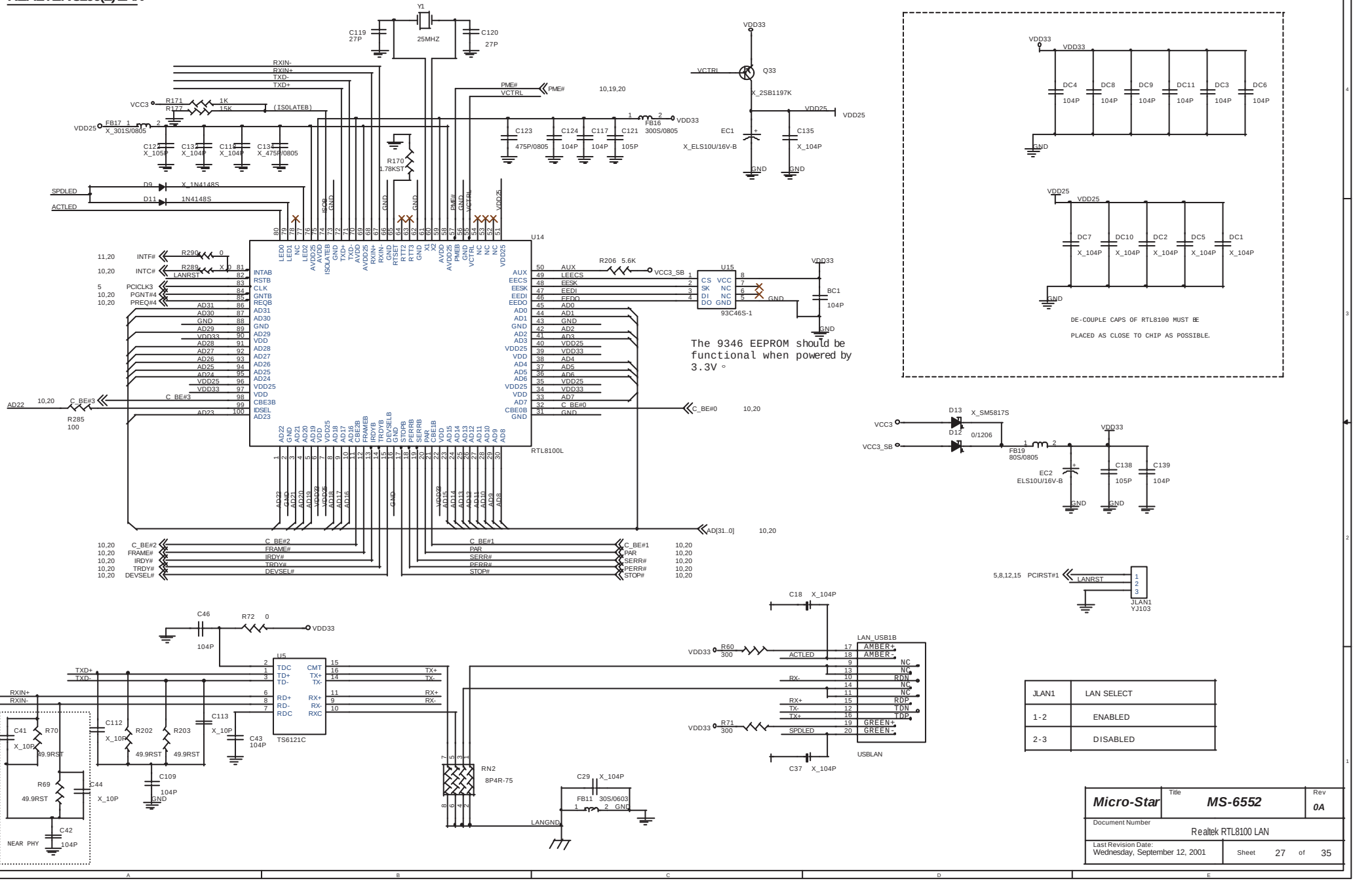


FLOPPY CONNECTOR



Micro-Star	Title: MS-6552		Rev: 0A
Document Number: IO Connector / ESD			
Last Revision Date: Wednesday, September 12, 2001		Sheet 26 of 35	

REALTEK 8100(L) LAN



JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

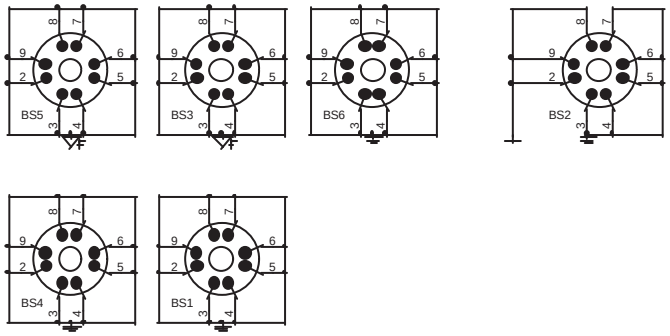
Micro-Star	Title: MS-6552	Rev: 0A
Document Number: Realtek RTL8100 LAN		
Last Revision Date: Wednesday, September 12, 2001	Sheet 27 of 35	

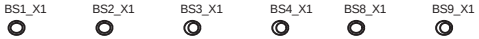
Jumper Setting

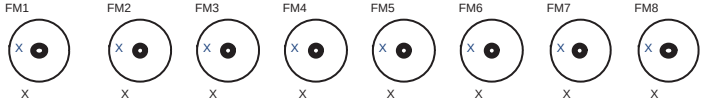
Jumper	Description	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
IR1	IR HEADER	
CD_IN1	CDROM HEADER (ATAPI)	
MDM_IN1	TELEPHONY HEADER (ATAPI)	
JP1	CNR RISER CODEC SELECT HEADER	
1-2	AUTO MODE	(Default)
2-3	PRIMARY AUDIO CODEC ONBOARD	

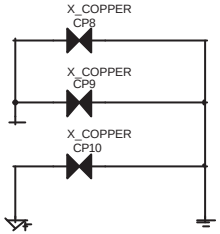
Micro-Star	Title: MS-6552	Rev: 0A
Document Number: JUMPER SETTING		
Last Revision Date: Wednesday, September 12,2001	Sheet 28 of 35	

PCB OTHER COMPONENT









SIMULATION TRACE

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: MANUAL		
Last Revision Date: Wednesday, September 26,2001	Sheet 29 of 35	

Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

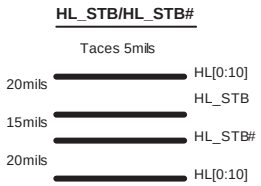
Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

***** Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space

Miscellaneous Signals

HL_STB/HL_STB#

Taces 5mils



* Max Length : 8"
* STB and STB# Length must be equal

HL[10..0]

* Max Length : 8"
* Length must be matched within +/- 0." of the Strobe Signals

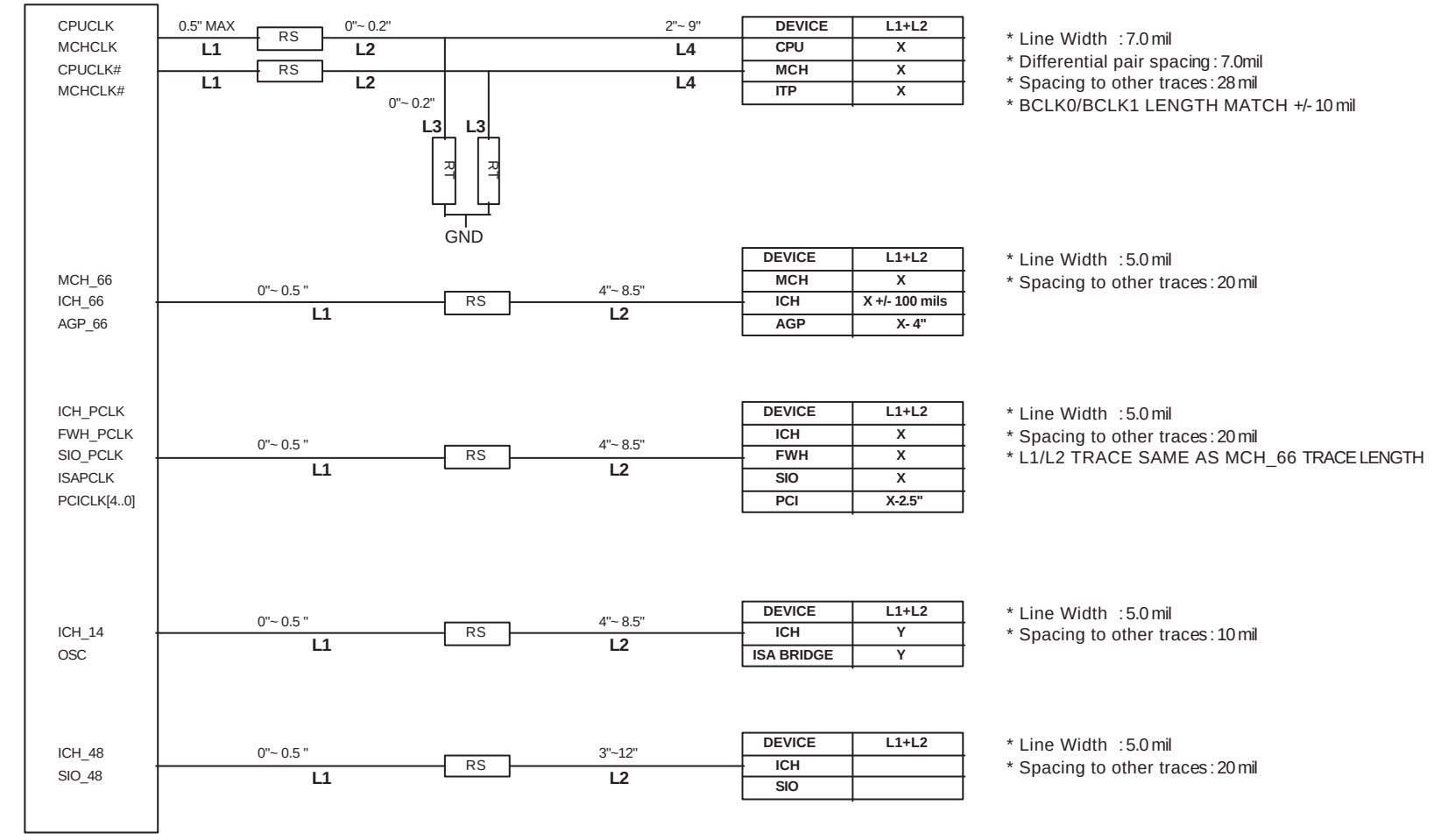
USB

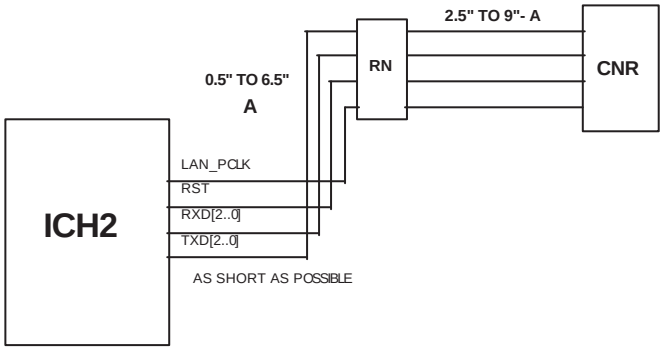
*** USB Trace width : 9 mils**
*** USB Trace Spacing : 25 mils**
*** Differential USB Signlas Trace Spacing : 18 mils**
*** USB Power Trace must be 40mils width**

AGP

1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#





* Line Width : 7.0 mil
* Differential signls space : 14mils
* Differential signls length mismatch +/- 7mil

Micro-Star	Title: MS-6552	Rev: 0A
Document Number: CK-408 and LAN Design Guide		
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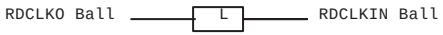
SDRAM Routing Guidelines

5.Feedback - RDCLKO,RDCLKIN routing rule

2 or 3 DIMM feedback layout guideline

Signal	Length	Width	Trace Spacing
Trace L	50 mils	7 mil	5 mil



DDR-SDRAM Routing Guidelines

1.DDR bus reference plane stack-up

PCB Layer	Description
Layer 1	Signal
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Power / Signal

***All the memory bus signals must be referenced to GND**

2.DDR signal groups

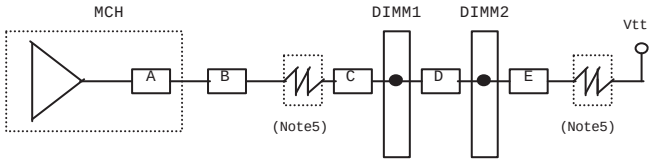
Group	Signals
Data	SDQ[63:0],SCB[7:0],SDQS[8:0]
Command	SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE#
Control	SCKE[3:0],SCS#[3:0]
Clock	SCK[5:0],SCK#[5:0]
Feedback	RCVENOUT#,RCVENIN#

3.SDQ[63:0],SCB[7:0],SDQS[8:],SCK/SCK#[5:0]routing rule

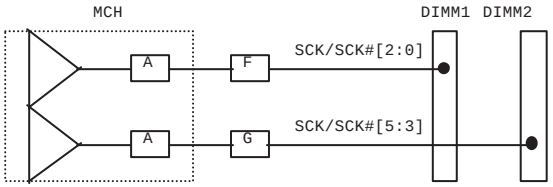
Signal	Length A	Length B	Length C	Length D	Length E	Width	Spacing	Routing Layer
SDQ[63:0] SCB[7:0] SQDS[8:0]	Package length	2.0" - 5.0"	Max = 0.5"	0.3' - 0.5"	0.1" - 0.8"	5 mil	(Note2)	Top
(Note1)	DIMM 1 = A + B + C = X DIMM 2 = A + B + C + D = X + D							
SCK/SCK#[2:0]	Package length	B+C+2"<= Length F <= B+C+1" 2.0" - 6.5"		None	None	5 mil	(Note4)	Bottom
	DIMM 1 = A + F = X + 1" to X + 2"							
SCK/SCK#[5:3] (Note3)	Package length	B+C+D+2"<= Length G <= B+C+D+1" 2.5" - 7.0"				5 mil	(Note4)	Bottom
	DIMM 2 = A + G = X + D + 1" to X + D + 2"							

*** Package length see Table - 4**

SDQ[63:0],SCB[7:0],SDQS[8:] layout guideline



SCK[5:0] layout guideline



Note1:Each data and strobe signal group must be length matching +/- 25 mils

SDQS[X] = +/- 25 mils SDQ[X]/SCB[X] group length

Signals	Associated Strobe
SDQ[7:0]	SDQ0
SDQ[15:8]	SDQ1
SDQ[23:16]	SDQ2
SDQ[31:17]	SDQ3
SDQ[39:32]	SDQ4
SDQ[47:40]	SDQ5
SDQ[55:48]	SDQ6
SDQ[63:56]	SDQ7
SCB[7:0]	SDQ8

Note2:Trace spacing normally = 12 mils and through between DIMM 2 pin = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils

Note3:

- * SCK[X] length = SCK#[X] length
- * SCK/SCK#[2:0] routed to DIMM 0 are equal in length, and SCK/SCK#[5:3] routed to DIMM 1 are equal in 1ength

Note4:

- * Between the pair differential clock 2 signal trace spacing = 7 mils
- * Differential Trace with 2.5V copper flood spacing = 10 mils minimum
- * Serpentine spacing = 20 mils minimum
- * Differential signals breakout form MCH = 5 mil width with 7 mil differential spacing and 7 mil isolation spacing from another signal for a max of 350 mils

Note5:Data group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the command or control group signal

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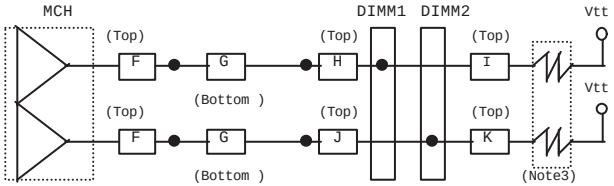
DDR-SDRAM Routing Guidelines

4.SCKE[3:0],SCS#[3:0] routing rule

DIMM 0					
Signal	Length F	Length G	Length H	Length I	Width
SCS#[1:0] SCKE[1:0] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils (Note2)	0.4" - 1.3"	5 mils
Total lenght	DIMM0 SCK/SCK#[2:0] length = X" DIMM0 SCS#/SCKE length = F + G + H = X"- 1"				
DIMM 1					
Signal	Length F	Length G	Length J	Length K	Width
SCS#[3:2] SCKE[3:2] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 1" (Note2)	0.1" - 0.8"	5 mils
Total lenght	DIMM1 SCK/SCK#[5:3] length = Y" DIMM1 SCS#/SCKE length = F + G + J = Y"- 1"				



Note1:

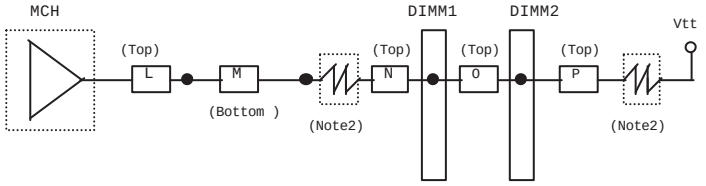
- *Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
- *Trace with 2.5V copper flood spacing = 7 mils minimum
- *Isolation spacing form another group signal spacing = 20 mils minimum
- *Control signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:This purpose prevent break form DIMM0 bottom size 2.5V copper flood to MCH power plane

Note3:Control group signal can NOT placed within the same parallel resistor packs as the command or data group signal

5.SMA[12:0],SBS[1:0],SRAS#,SCAS# routing rule

Signal	Length L	Length M	Length N	Length O	Length P	Width
SMA[12:0] SBS[1:0] SRAS# SCAS# (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils	0.3" - 0.5"	0.1" - 0.8"	5 mils
DIMM 0 Total lenght	DIMM0 SCK/SCK#[2:0] length = X" Command signal length = L + M + N = X" - 1"					
DIMM 1 Total lenght	DIMM0 SCK/SCK#[5:3] length = Y" Command signal length = L + M + N + O = Y" - 1"					



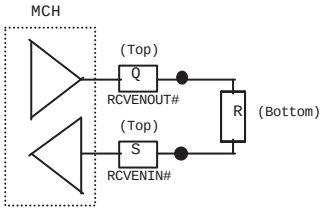
Note1:

- *Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
- *Trace with 2.5V copper flood spacing = 7 mils minimum
- *Isolation spacing form another group signal spacing = 20 mils minimum
- *Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:Command group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the data or control group signal

5.Feedback - RCVENOUT#,RCVENIN# routing rule

Signal	Length Q	Length R	Length S	Width
RCVENOUT# RCVENIN# (Note1)	40 mils	Equal 1"	40 mils	5 milS
Total Length	Q + R + S = 1080 mils			



Note1:

- *Trace spacing = 12 mils
- *Trace with 2.5V copper flood spacing = 7 mils minimum
- *Isolation spacing form another group signal spacing = 10 mils minimum
- *Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

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Table - 4

DDR Data Signals(1)		
Signal	MCH ball	Package length(")
SDQ0	G28	0.716
SDQ1	F27	0.699
SDQ2	C28	0.874
SDQ3	E28	0.754
SDQ4	H25	0.532
SDQ5	G27	0.666
SDQ6	F25	0.592
SDQ7	B28	0.892
SDQ8	E27	0.797
SDQ9	C27	0.833
SDQ10	B25	0.812
SDQ11	C25	0.753
SDQ12	B27	0.886
SDQ13	D27	0.867
SDQ14	D26	0.773
SDQ15	E25	0.645
SDQ16	D24	0.722
SDQ17	E23	0.602
SDQ18	C22	0.699
SDQ19	E21	0.566
SDQ20	C24	0.785
SDQ21	B23	0.781
SDQ22	D22	0.640
SDQ23	B21	0.711
SDQ24	C21	0.627
SDQ25	D20	0.555
SDQ26	C19	0.587
SDQ27	D18	0.522
SDQ28	C20	0.615
SDQ29	E19	0.487
SDQ30	C18	0.579
SDQ31	E17	0.521

DDR Data Signals(2)		
Signal	MCH ball	Package length(")
SDQ32	E13	0.432
SDQ33	C12	0.543
SDQ34	B11	0.596
SDQ35	C10	0.590
SDQ36	B13	0.639
SDQ37	C13	0.552
SDQ38	C11	0.588
SDQ39	D10	0.626
SDQ40	E10	0.533
SDQ41	C9	0.605
SDQ42	D8	0.587
SDQ43	E8	0.522
SDQ44	E11	0.523
SDQ45	B9	0.715
SDQ46	B7	0.706
SDQ47	C7	0.643
SDQ48	C6	0.700
SDQ49	D6	0.664
SDQ50	D4	0.760
SDQ51	B3	0.922
SDQ52	E6	0.640
SDQ53	B5	0.846
SDQ54	C4	0.810
SDQ55	E5	0.670
SDQ56	C3	0.859
SDQ57	D3	0.811
SDQ58	F4	0.723
SDQ59	F3	0.814
SDQ60	B2	0.949
SDQ61	C2	0.893
SDQ62	E2	0.865
SDQ63	G5	0.689

DDR ECC Signals		
Signal	MCH ball	Package length(")
SCB0	C16	0.570
SCB1	D16	0.526
SCB2	B15	0.623
SCB3	C14	0.533
SCB4	B17	0.621
SCB5	C17	0.583
SCB6	C15	0.540
SCB7	D14	0.503

DDR Data Strobe Signals		
Signal	MCH ball	Package length(")
SDQS0	F26	0.651
SDQS1	C26	0.775
SDQS2	C23	0.738
SDQS3	B19	0.636
SDQS4	D12	0.493
SDQS5	C8	0.596
SDQS6	C5	0.776
SDQS7	E3	0.821
SDQS8	E15	0.520

DDR Clock Signals		
Signal	MCH ball	Package length(")
SCK0	E14	0.453
SCK#0	F15	0.432
SCK1	J24	0.454
SCK#1	G25	0.587
SCK2	G6	0.551
SCK#2	G7	0.543
SCK3	G15	0.371
SCK#3	G14	0.349
SCK4	E24	0.610
SCK#4	G24	0.548
SCK5	H5	0.589
SCK#5	F5	0.693

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JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

JBAT1(1-2)
YJUMPER-MG

LEGEND AUDIO

KKK
JC-D2x2-GN

BAT SOCKET

BAT1[A]
YSKTBT

JP2 H/W AUDIO	
1 - 2	DISABLE
2 - 3	ENABLE *

JP2(2-3)
YJUMPER-MG

J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

J7(1)
YJUMPER-MG

BIOS

U23(1)

1	VPP	VCC	32
2	RST#	CLK	31
3	FGPI3	FGPI4	30
4	FGPI2	IC(VIL)	29
5	FGPI1	GNDA	28
6	FGPI0	VCCA	27
7	WP#	GND	26
8	TBL#	VCC	25
9	ID3	INIT#	24
10	ID2	FWH4	23
11	ID1	RFU	22
12	ID0	RFU	21
13	FWH0	RFU	20
14	FWH1	RFU	19
15	FWH2	RFU	18
16	GND	FWH3	17

SST49LF002A

FRONT PANNEL BUZZER

F_P114-15
X_YJUMPER-MG

JP3	AUDIO DOWN
1-2	Auto mode
2-3	Disabled onboard audio codec

JP3(1-2)
YJUMPER-MG

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

JLAN1(1-2)
YJUMPER-MG

MS6552 PCB

PCB
MS-6552-00A

COM1
YCN9M-1

COM2
YCN9M-1

X_U12-A
845-MCH-PIN

X_U12-B
845-MCH-PIN

X_U12-C
845-MCH-PIN

X_U12-D
845-MCH-PIN

X_U12
845-MCH-H

X_AGP1
AGP-R

LAN_USB2
USB2
USB1
YUSB-D1

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