MS-6551

Version 10

10/15/2001 Update

INTEL (R) Brookdale Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:

BIOS -- FWH
AC'97 Codec -- AD1881
LPC Super I/O -- W83627HF
Clock Generation -- ICS 950208
LAN -- INTEL 82562EM/ET

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 5
CNR SLOT * 1
ISA SLOT * 1 (Share PCI5)

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Document Number: Cover Sheet		
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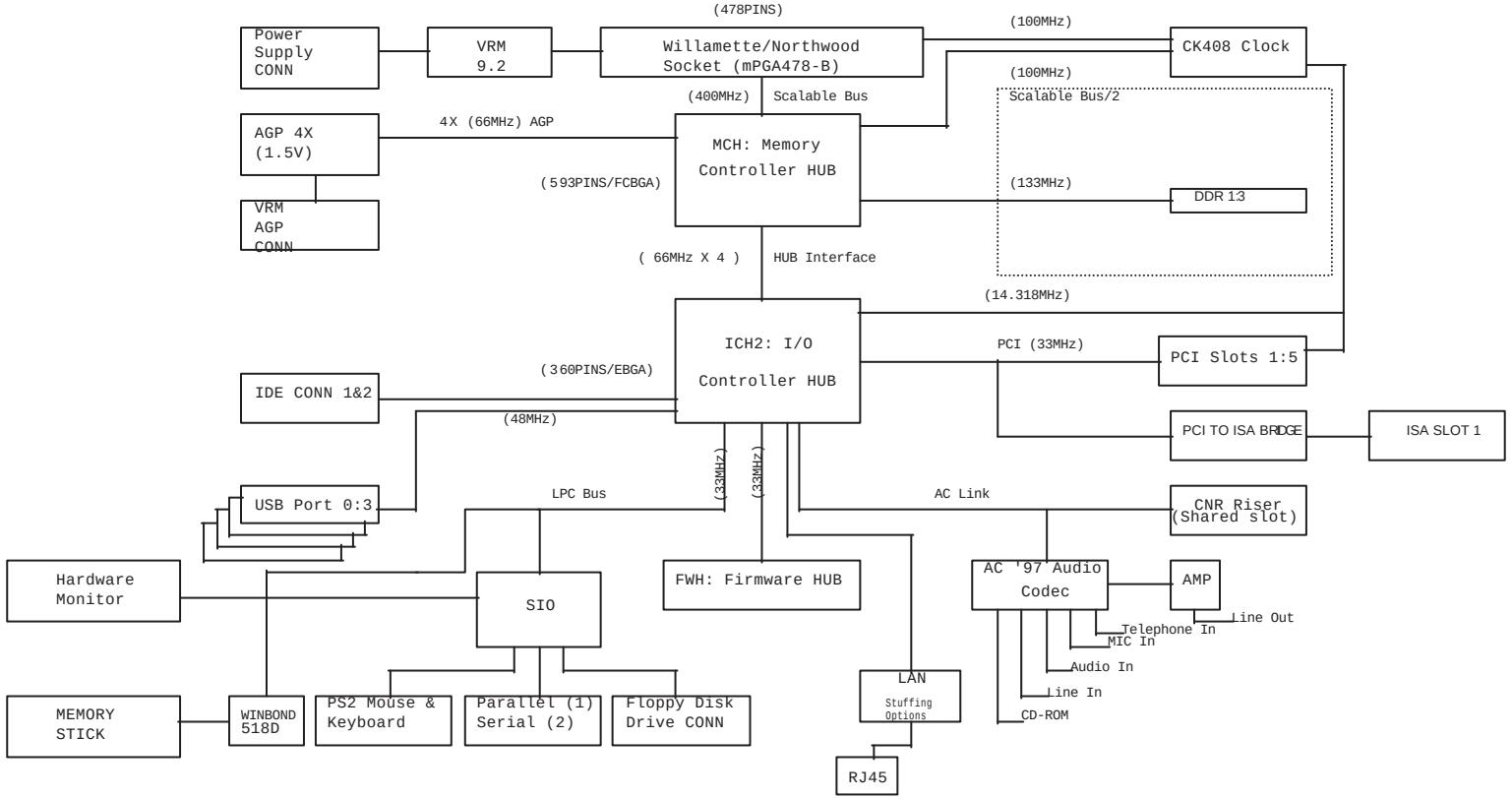
AGP
4X(1.5V)
AGP CONN



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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	PCI TO ISA REQA#
GPIO 1	I	Non Connect (PREQ#5)
GPIO 2	I	INTE#
GPIO 3	I	INTF#
GPIO 4	I	INTG#
GPIO 5	I	INTH#
GPIO 6	I	CNR Detect
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	PCI TO ISA GNTA#
GPIO 17	O	Non Connect (PGNT#5)
GPIO 18	O	Not Implemented
GPIO 19	O	Non Connect
GPIO 20	O	Non Connect
GPIO 21	O	PCI TO ISA NOGO
GPIO 22	OD	Audio 4 channel control
GPIO 23	O	BIOS Locked/Unlocked
GPIO 24	O	Non Connect
GPIO 25	O	Lan Status Input
GPIO 26	O	Non Connect
GPIO 27	I/O	Non Connect
GPIO 28	I/O	LAN ENABLE/DISABLE
GPIO 29~31	I/O	Not Implemented

FWH

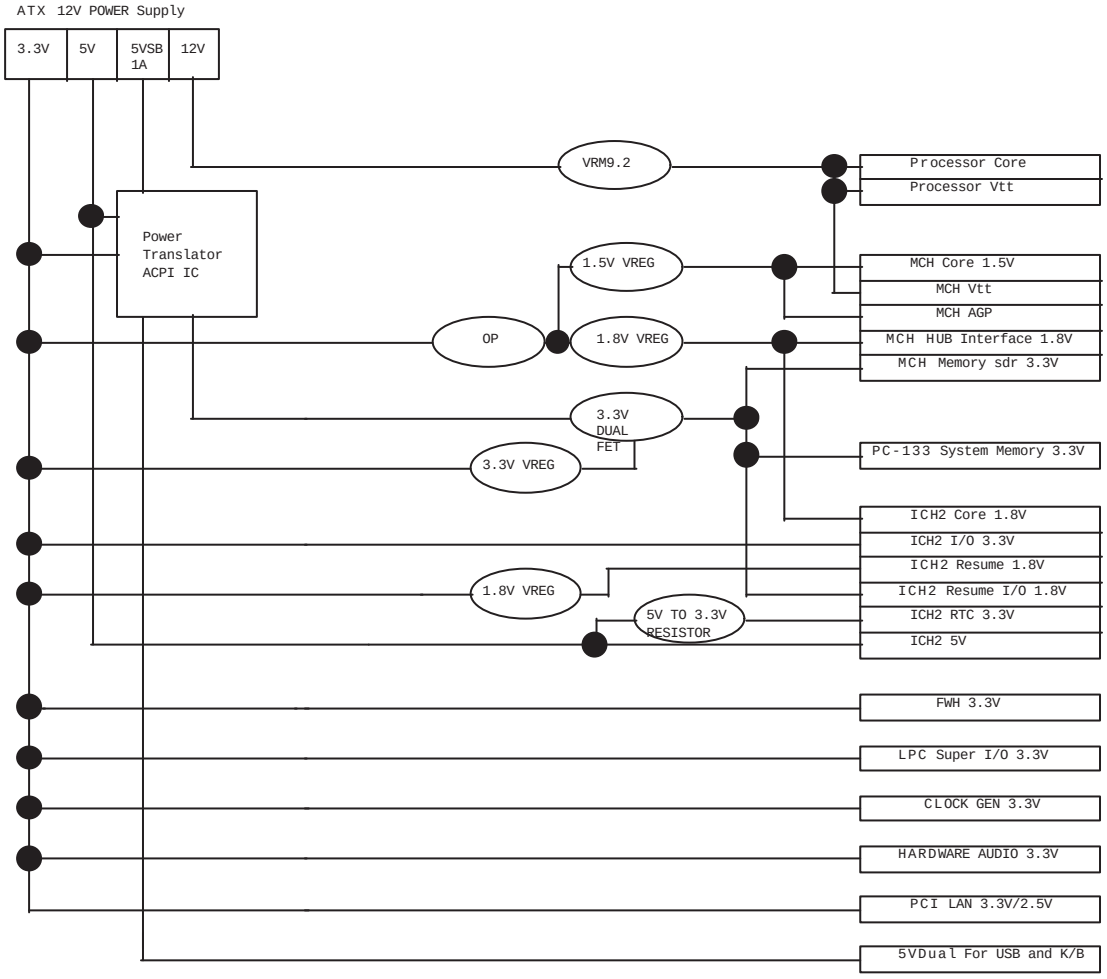
GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DLED

GPIO Pin	Type	Function
GP32	I/OD	DLED1
GP24	I/OD	DLED2
GP34	I/OD	DLED3
GP33	I/OD	DLED4

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19
PCI Slot 5	INTB# INTC# INTD# INTA#	AD21

Power Delivery Map



Micro-Star	Title: MS-6551	Rev: 10
Document Number: Power Delivery Map		
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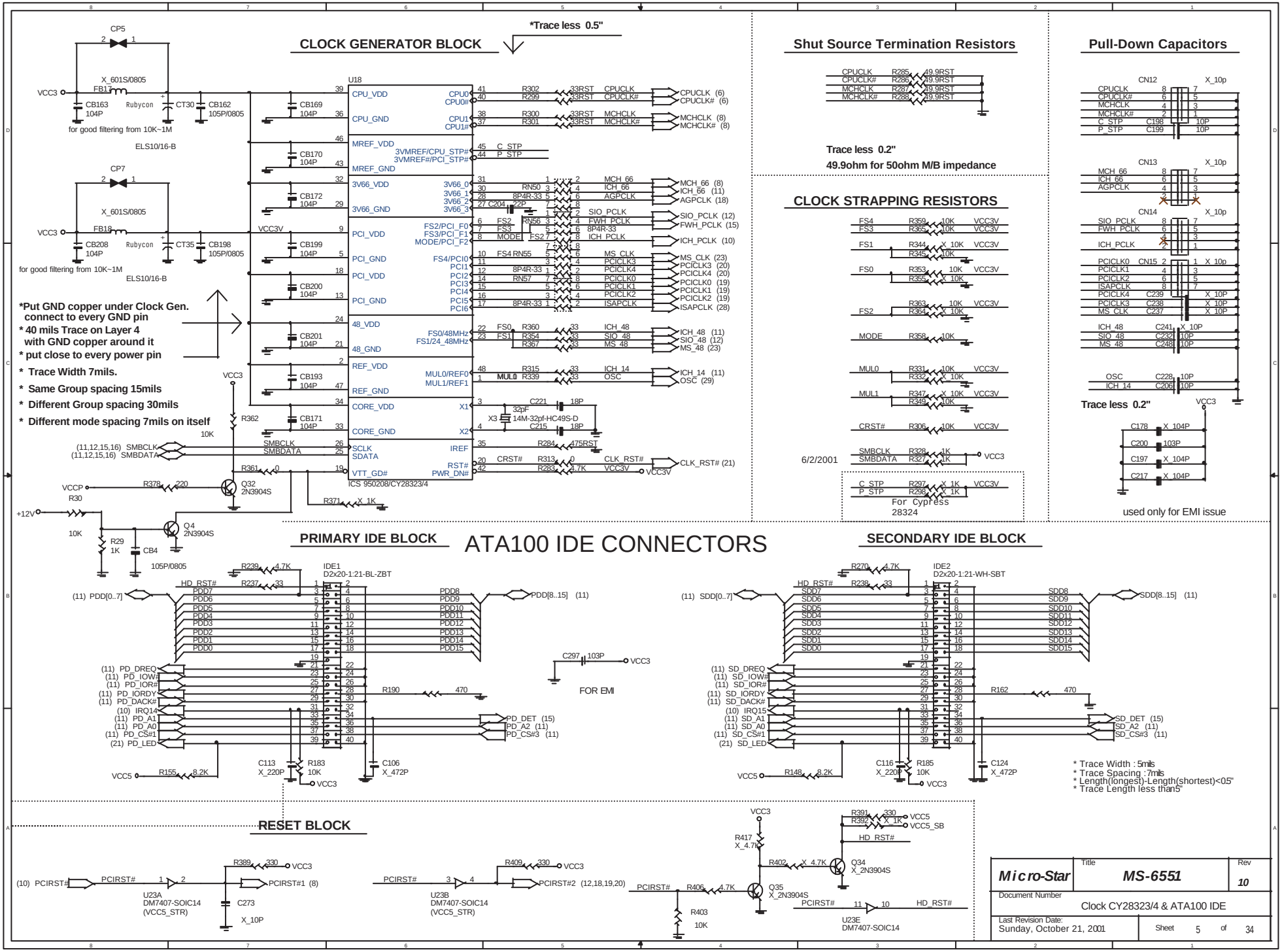
CLOCK GENERATOR BLOCK
*Trace less 0.5"
U18
CPU_VDD
CPU_GND
MREF_VDD
MREF_GND
3V66_VDD
3V66_GND
PCI_VDD
PCI_GND
48_VDD
48_GND
REF_VDD
REF_GND
CORE_VDD
CORE_GND
ICS 950208/CY28323/4
*Put GND copper under Clock Gen.
connect to every GND pin
* 40 mils Trace on Layer 4
with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Different mode spacing 7mils on itself
Shut Source Termination Resistors
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
6/2/2001
For Cypress
28324
Pull-Down Capacitors
Trace less 0.2"
used only for EMI issue
ATA100 IDE CONNECTORS
PRIMARY IDE BLOCK
SECONDARY IDE BLOCK
IDE1
D2x20-1:21-BL-ZBT
IDE2
D2x20-1:21-WH-SBT
FOR EMI
* Trace Width : 5mils
* Trace Spacing :7mils
* Length(longest)-Length(shortest)<05"
* Trace Length less than5"
RESET BLOCK
Micro-Star
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Clock CY28323/4 & ATA100 IDE
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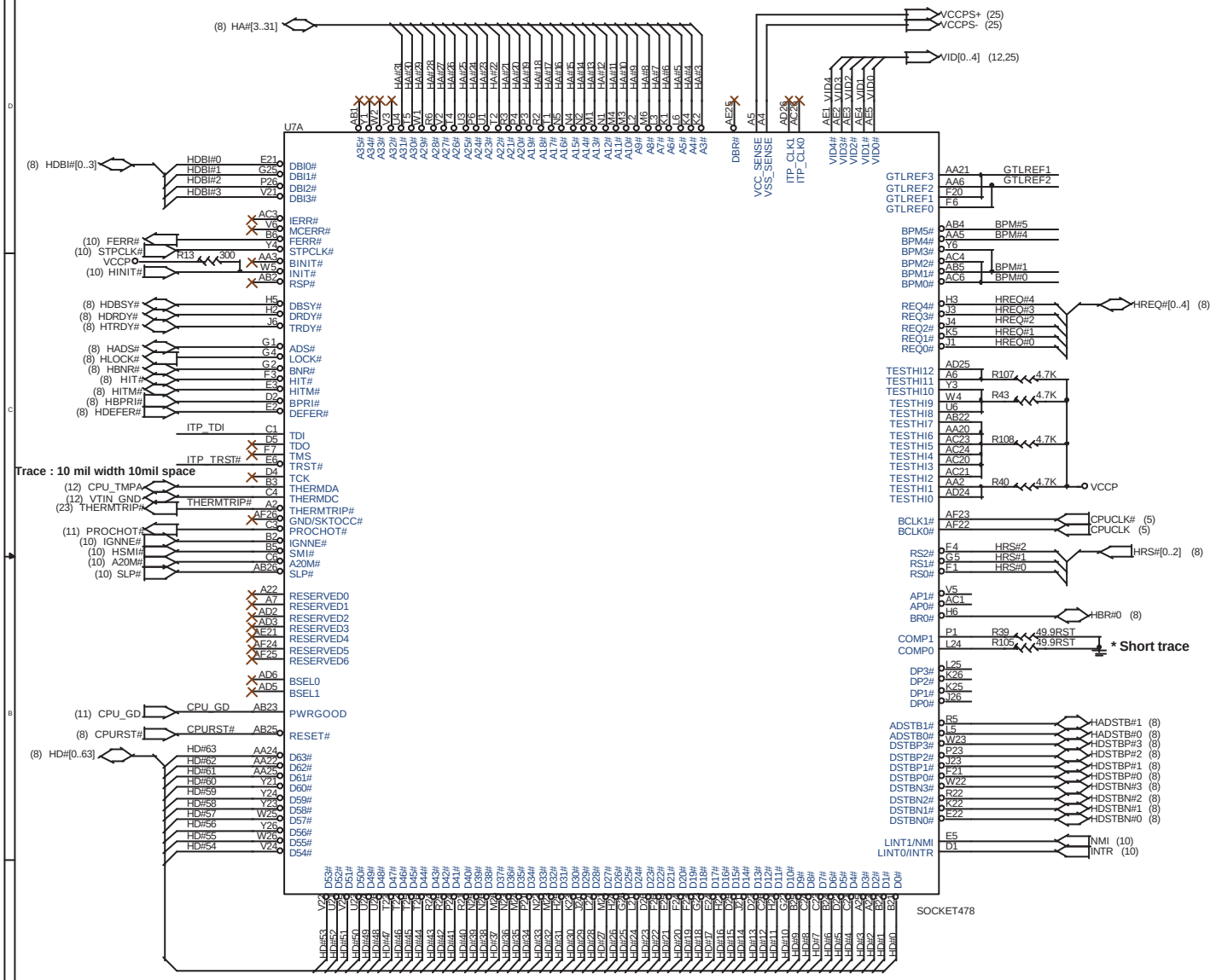
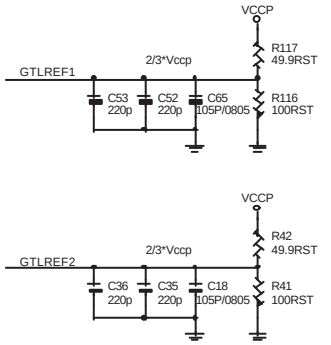
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK



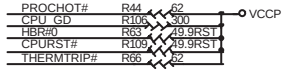
Every pin put one 220pF cap near it.

Trace Width 15mils, Space 15mils.

Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



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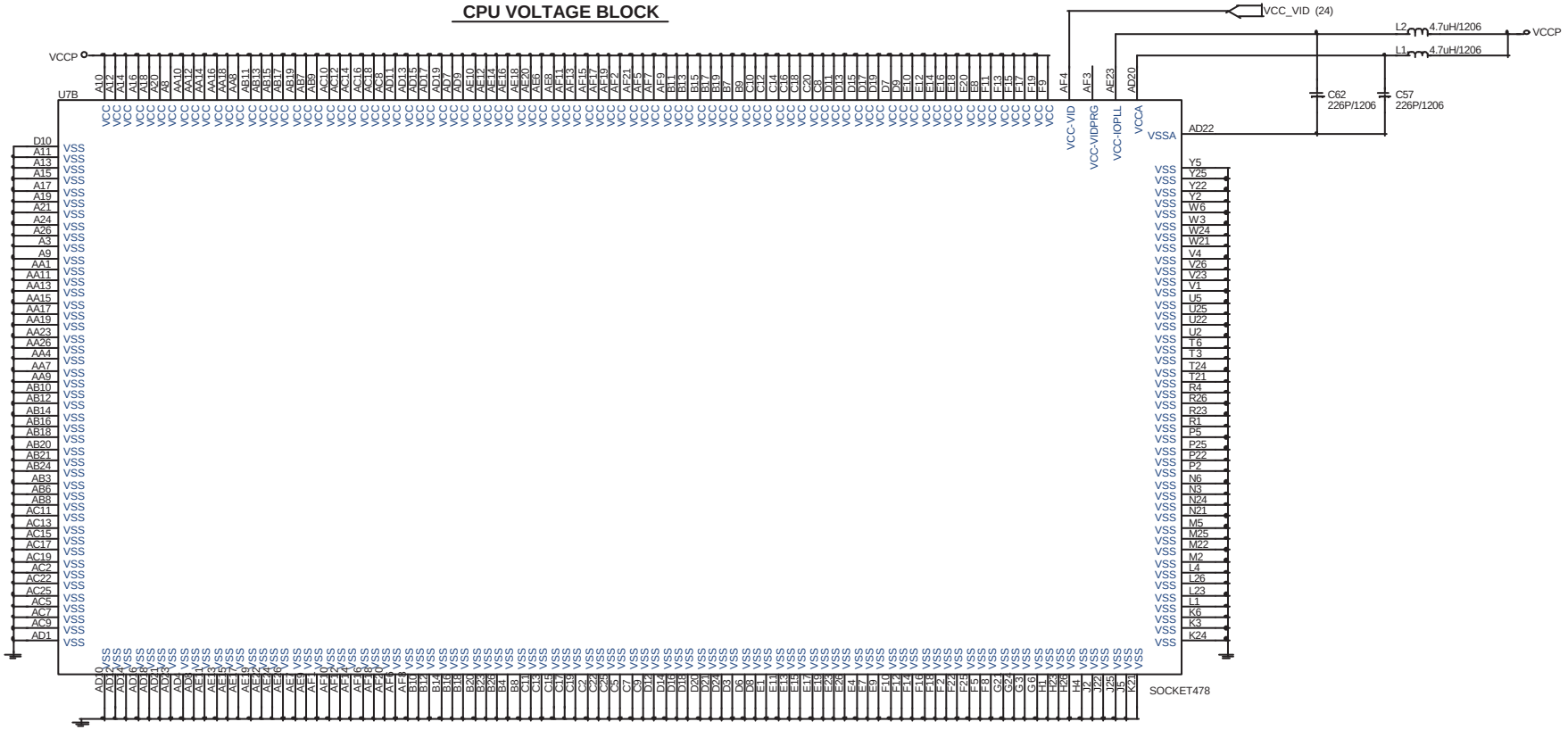
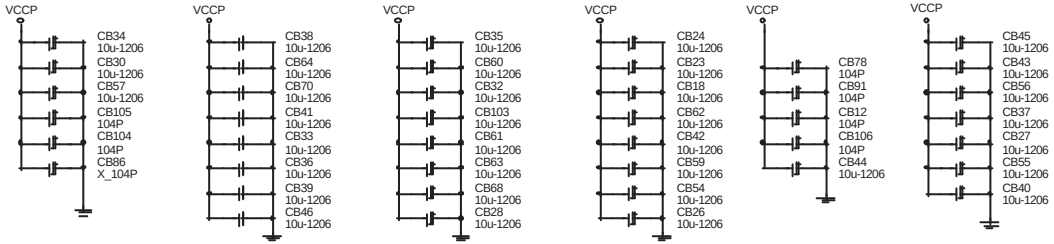
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITOR



PLACE CAPS WITHIN CPU CAVITY

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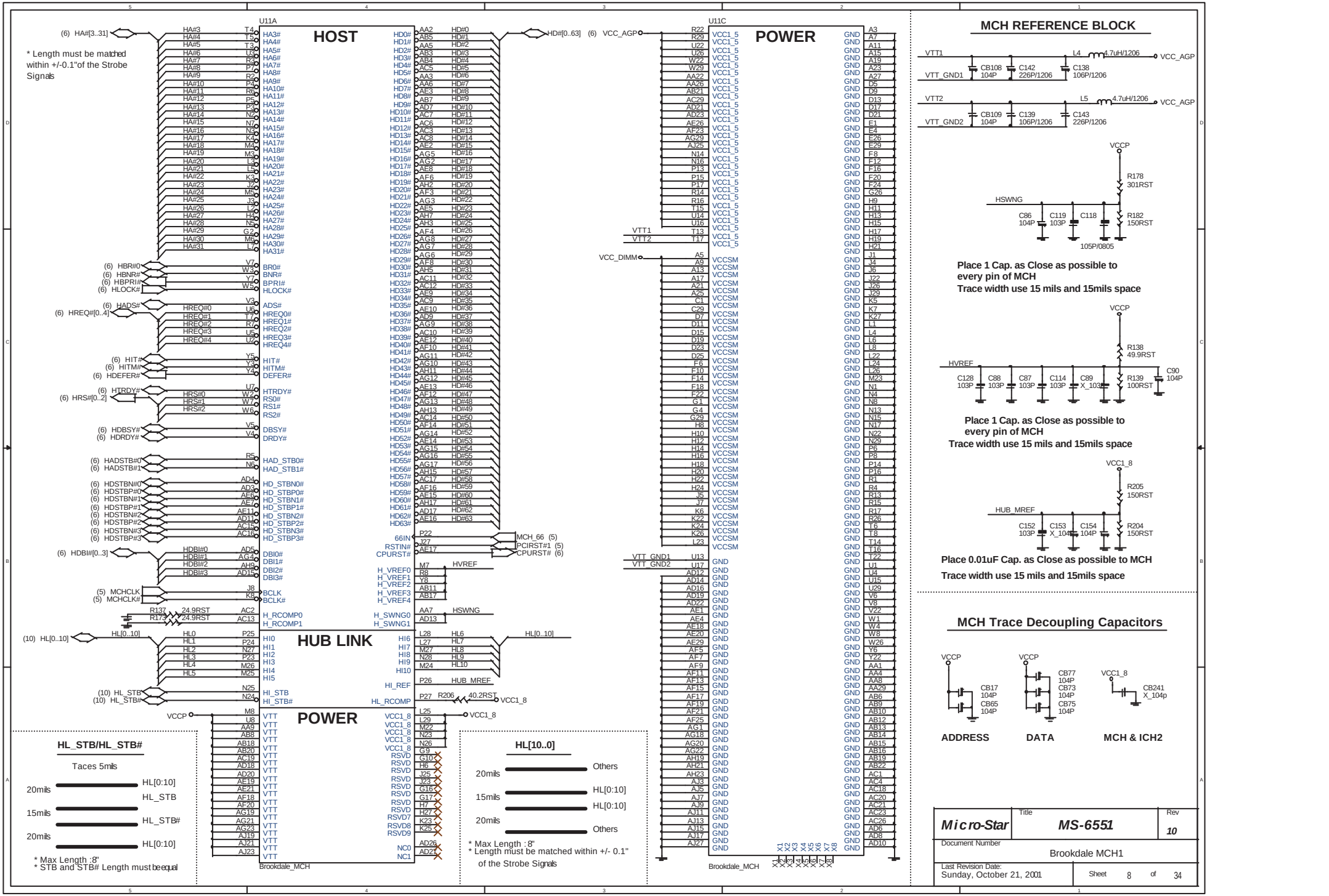
HOST
HUB LINK
POWER
POWER
U11A
U11C
Brookdale_MCH
Brookdale_MCH
* Length must be matched within +/-0.1"of the Strobe Signals
HL_STB/HL_STB#
Taces 5mils
20mils
HL[0:10]
HL_STB
15mils
HL_STB#
20mils
HL[0:10]
* Max Length :8"
* STB and STB# Length must be equal
HL[10..0]
20mils
Others
15mils
HL[0:10]
HL[0:10]
20mils
Others
* Max Length : 8"
* Length must be matched within +/- 0.1" of the Strobe Signals
MCH REFERENCE BLOCK
VTT1
VTT_GND1
CB108 104P
C142 226P/1206
C138 106P/1206
L4 4.7uH/1206
VCC_AGP
VTT2
VTT_GND2
CB109 104P
C139 106P/1206
C143 226P/1206
L5 4.7uH/1206
VCC_AGP
VCCP
R178 301RST
HSWNG
C86 104P
C119 103P
C118
R182 150RST
105P/0805
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCCP
R138 49.9RST
HVREF
C128 103P
C88 103P
C87 103P
C114 103P
C89 X_103p
R139 100RST
C90 104P
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCC1_8
R205 150RST
HUB_MREF
C152 103P
C153 X_104p
C154 104P
R204 150RST
Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space
MCH Trace Decoupling Capacitors
VCCP
CB17 104P
CB65 104P
ADDRESS
VCCP
CB77 104P
CB73 104P
CB75 104P
DATA
VCC1_8
CB241 X_104p
MCH & ICH2
Micro-Star
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10
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Brookdale MCH1
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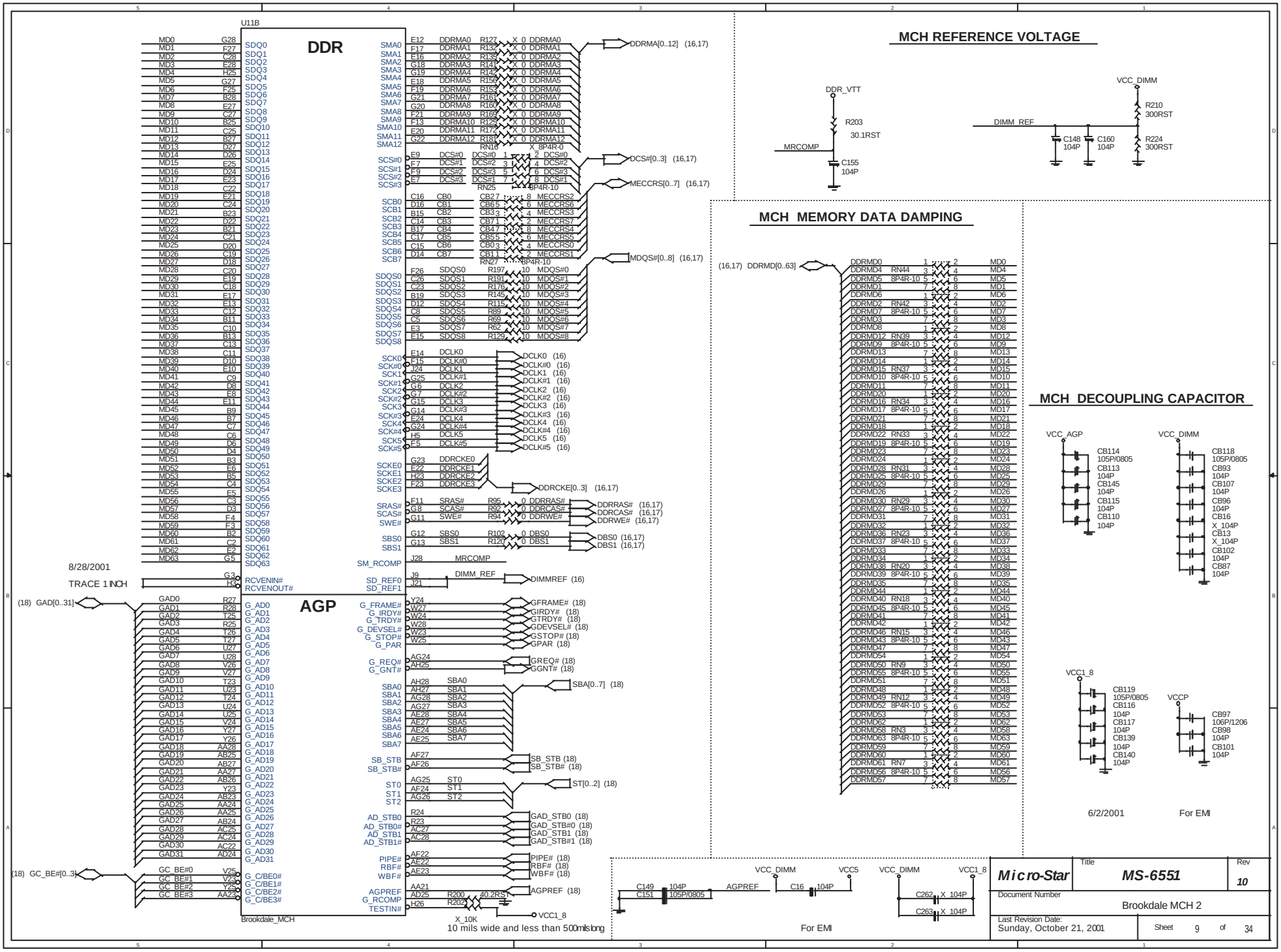
U11B
DDR
AGP
Brookdale_MCH
MCH REFERENCE VOLTAGE
MCH MEMORY DATA DAMPING
MCH DECOUPLING CAPACITOR
8/28/2001
TRACE 1 INCH
10 mils wide and less than 500mils long
For EMI
6/2/2001
For EMI
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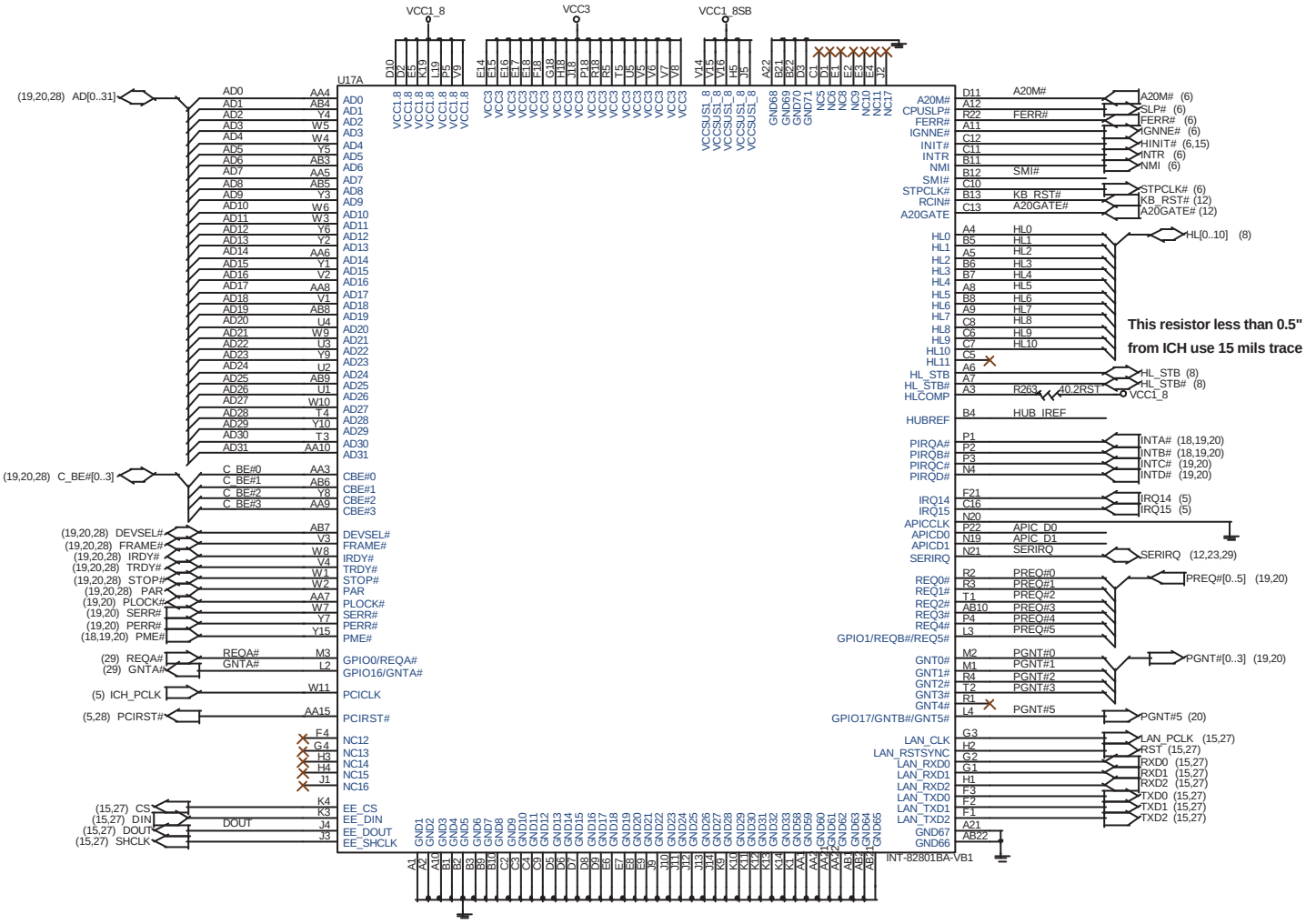
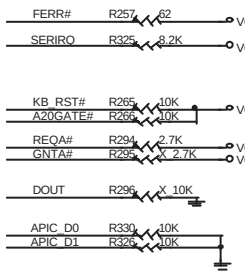
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



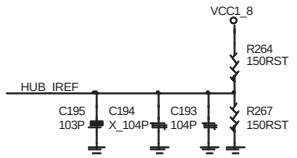
This resistor less than 0.5" from ICH use 15 mils trace

ICH2 SMI# SIGNAL

ICH2 STRAPPING RESISTORS

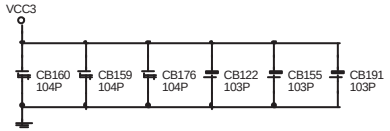


ICH2 REFERENCE VOLTAGE

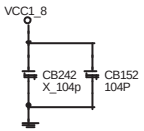


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

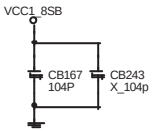
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



Distribute near the 1.8V power pin of the ICH2



Distribute near the VCC1_8SB Power pin of the ICH2

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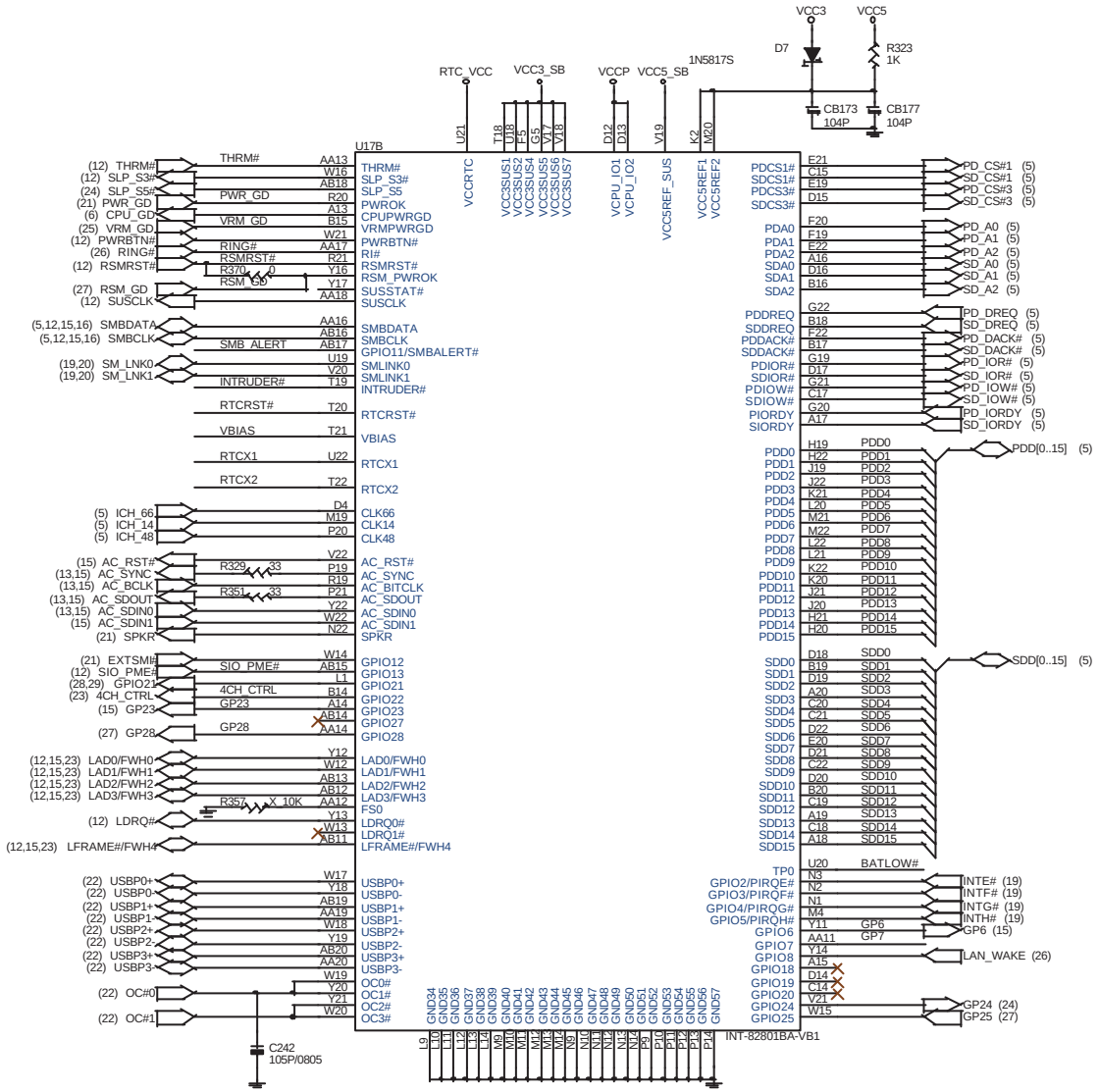
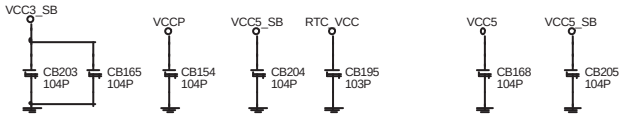
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

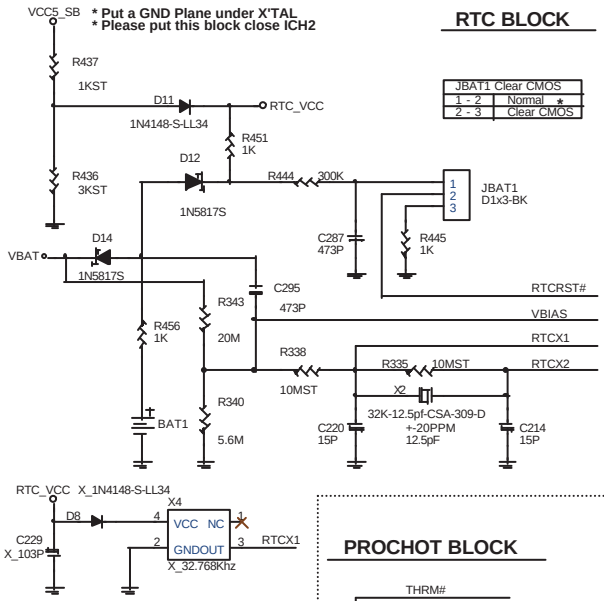


ICH2 DECOUPLING CAPACITOR

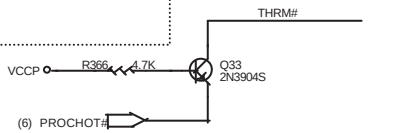


Distribute near the VCC3_SB power pin of the ICH

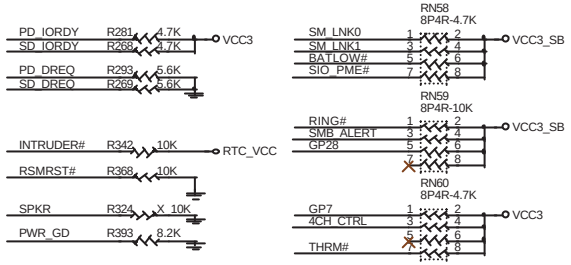
RTC BLOCK



PROCHOT BLOCK



ICH2 STRAPPING RESISTORS



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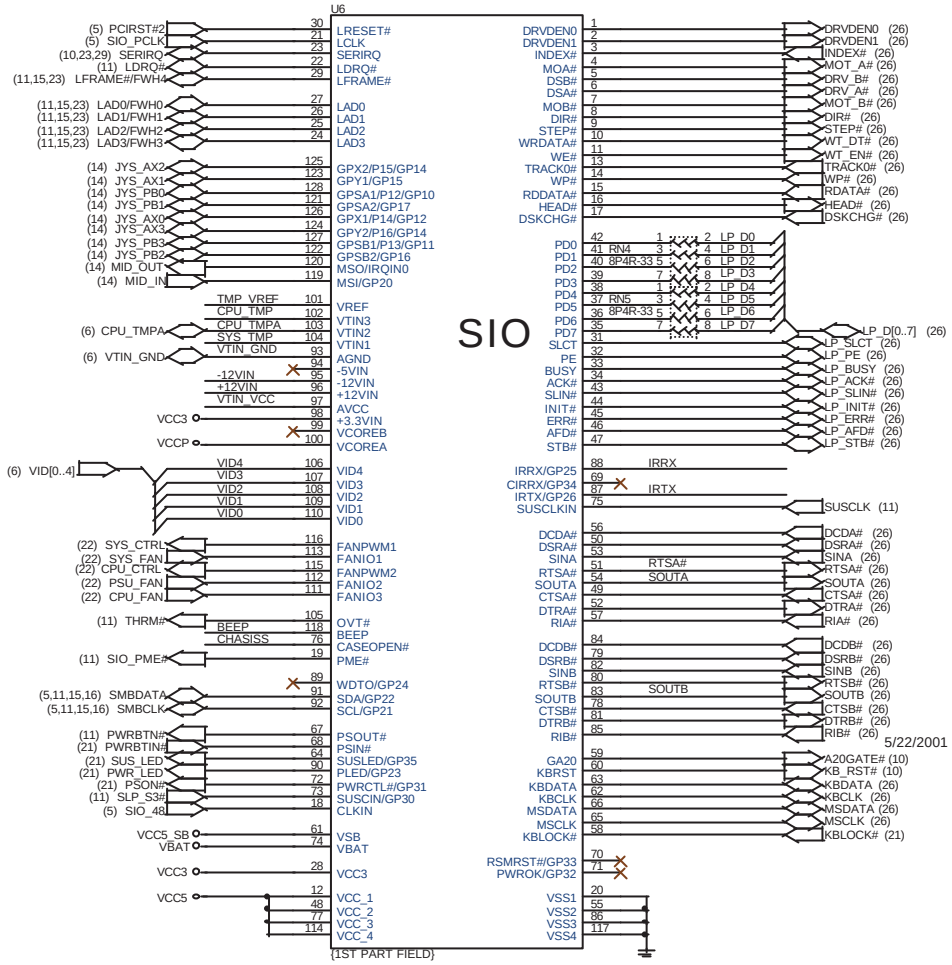
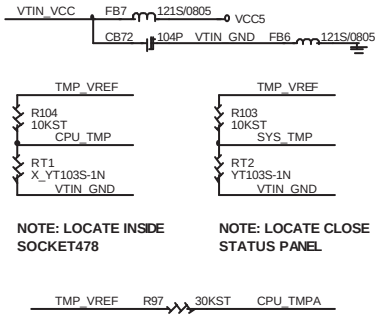
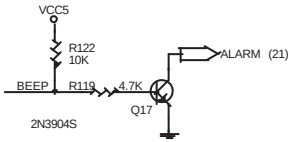
LPC SUPER I/O W83627HF



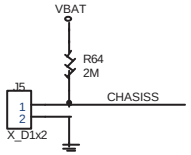
THERMAL RESISTOR BLOCK



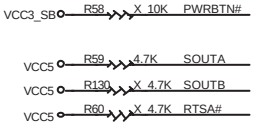
SPEAKER BLOCK



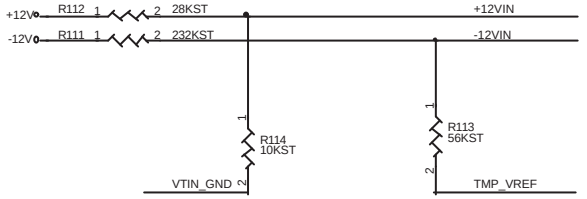
CHASISS INTRUSION HEADER



SUPER I/O STRAPPING RESISTOR

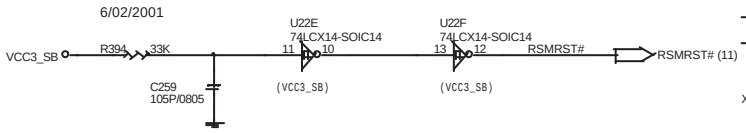


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

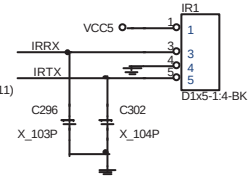


RESUME RESET CIRCUIT BLOCK

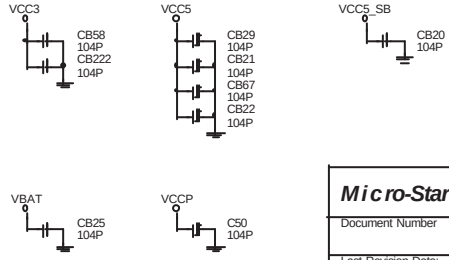
Stuff all for D Version bug



IR HEADER



DECOUPLING CAPACITOR



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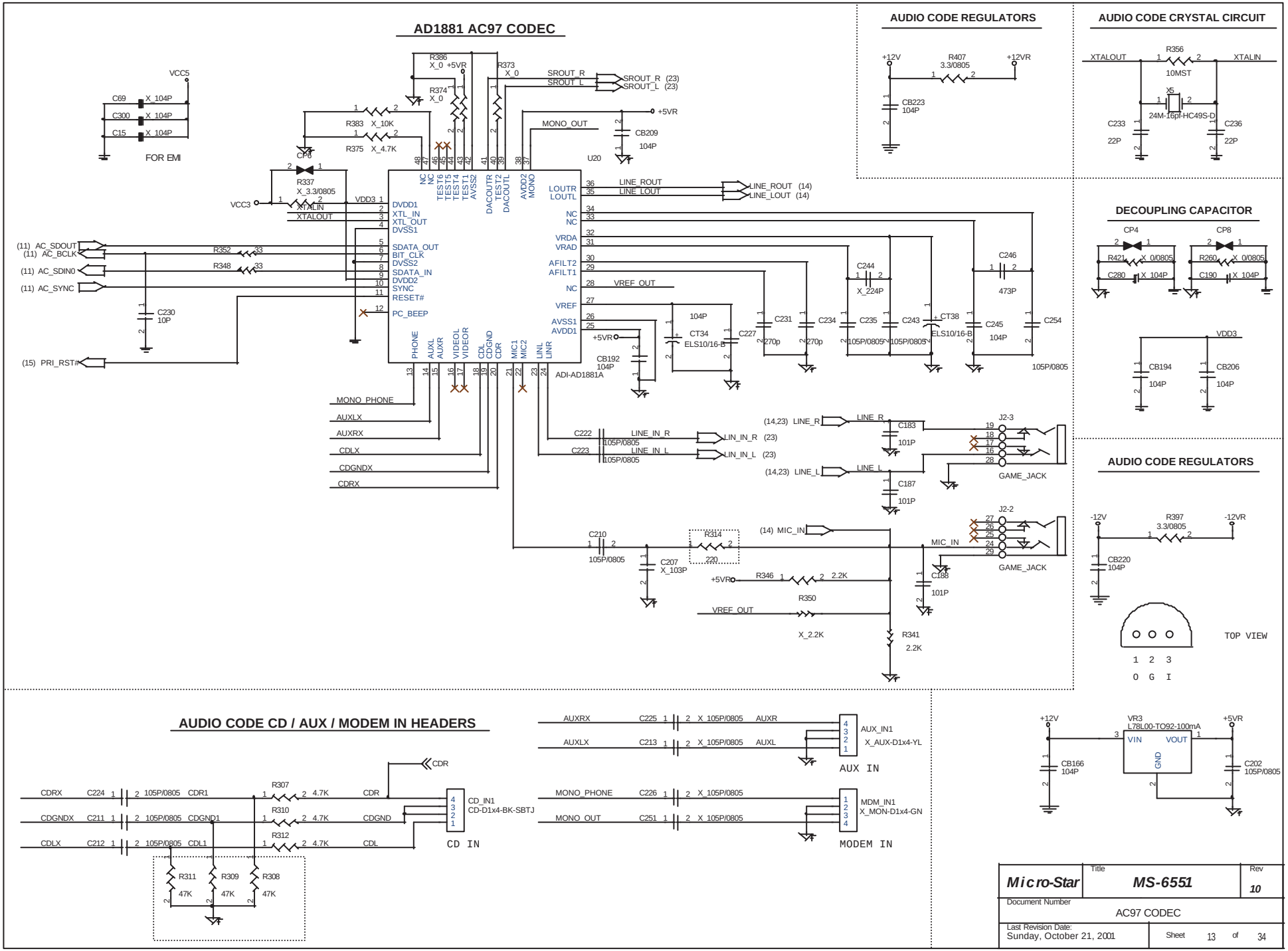
AD1881 AC97 CODEC
AUDIO CODE REGULATORS
AUDIO CODE CRYSTAL CIRCUIT
DECOUPLING CAPACITOR
AUDIO CODE REGULATORS
AUDIO CODE CD / AUX / MODEM IN HEADERS
ADI-AD1881A
FOR EMI
GAME_JACK
GAME_JACK
AUX IN
CD IN
MODEM IN
TOP VIEW
1 2 3
O G I
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AC97 CODEC
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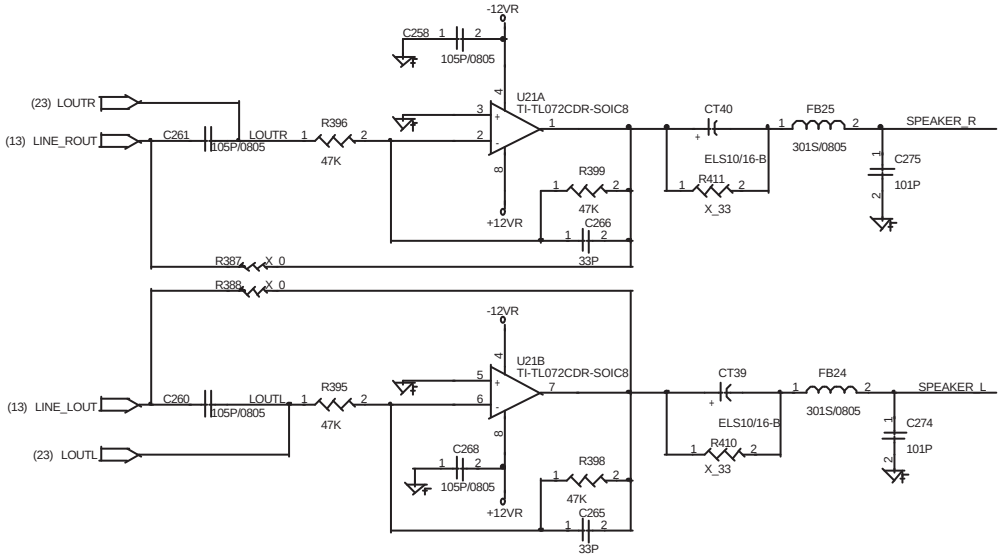
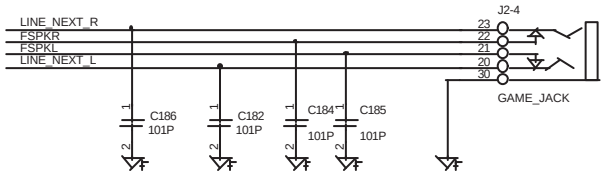
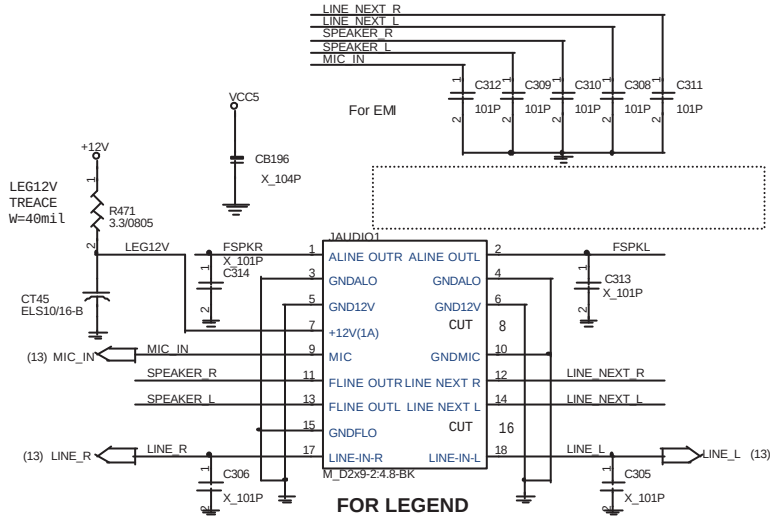
SPEAKER OUT CIRCUIT



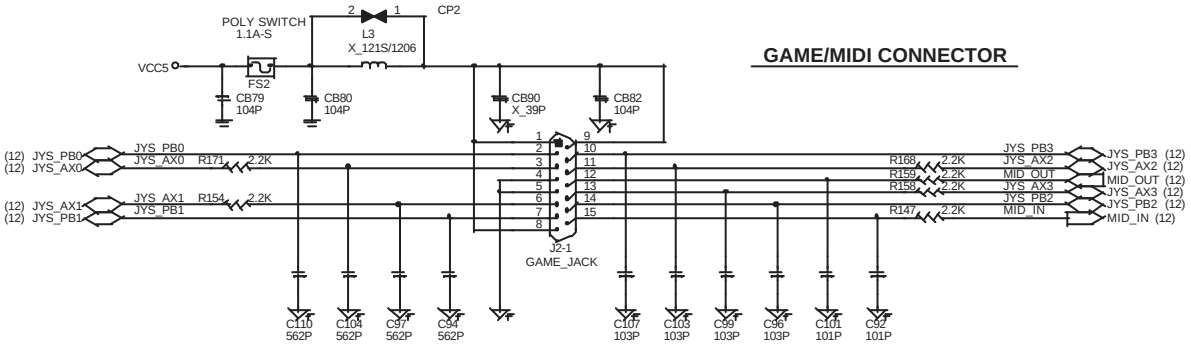
SPEAKER OUT JACK

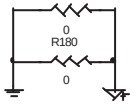


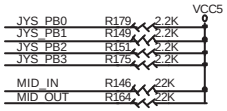
FOR MSI INTERNAL HEADER



GAME/MIDI CONNECTOR







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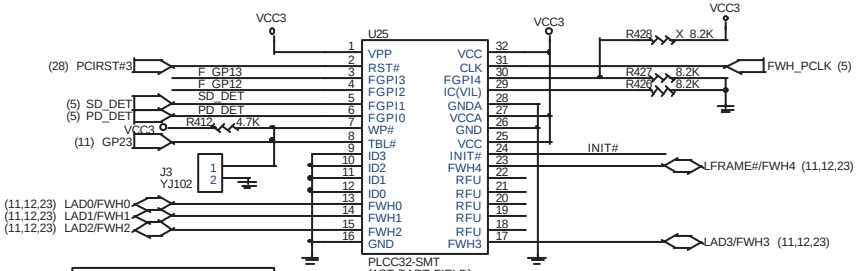
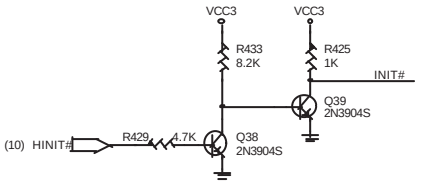
Firware Hub (FWH)

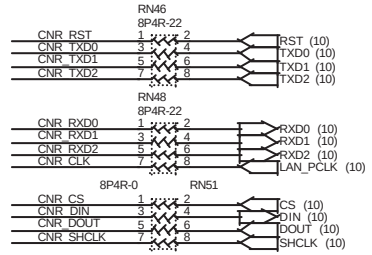


J3 BIOS Update	
SHORT	Locked
* OPEN	Unlocked

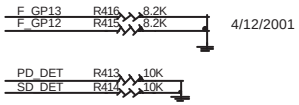
FWH INIT Signal Voltage Translation Block



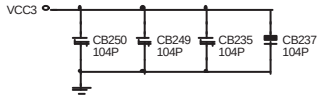
CNR Damping Resistor Net



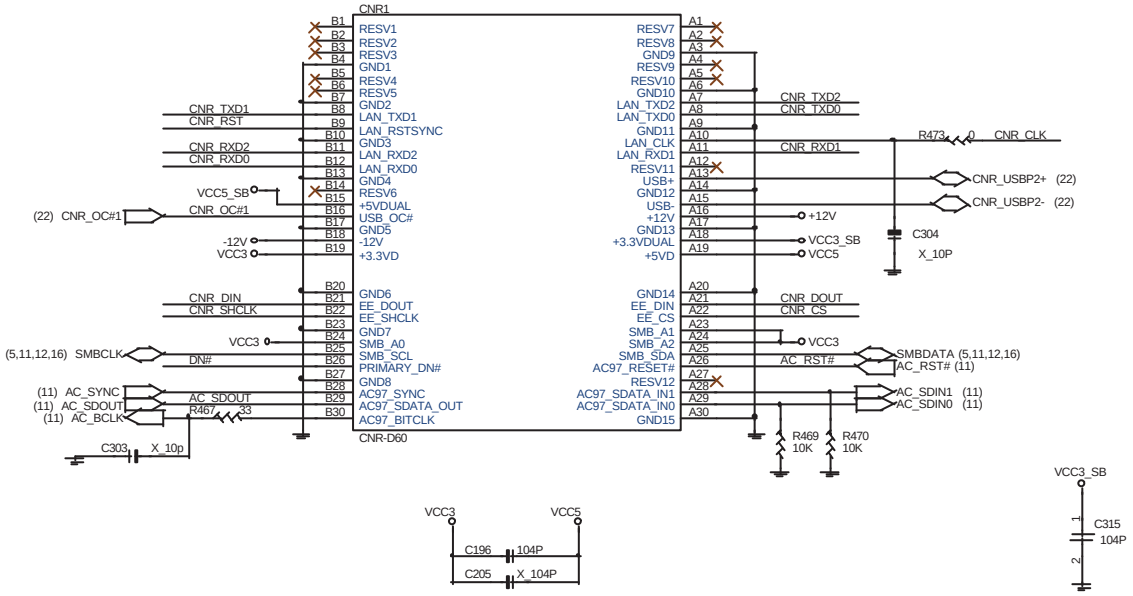
FWH RESISTORS



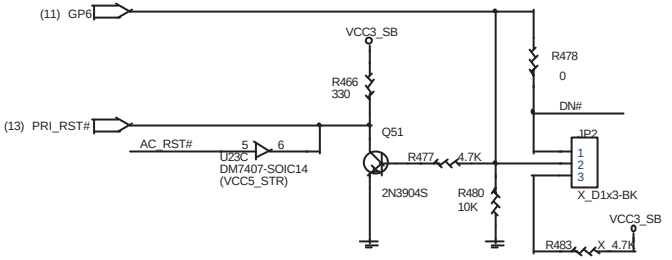
FWH DECOUPLING CAPACITORS



CNR RISER

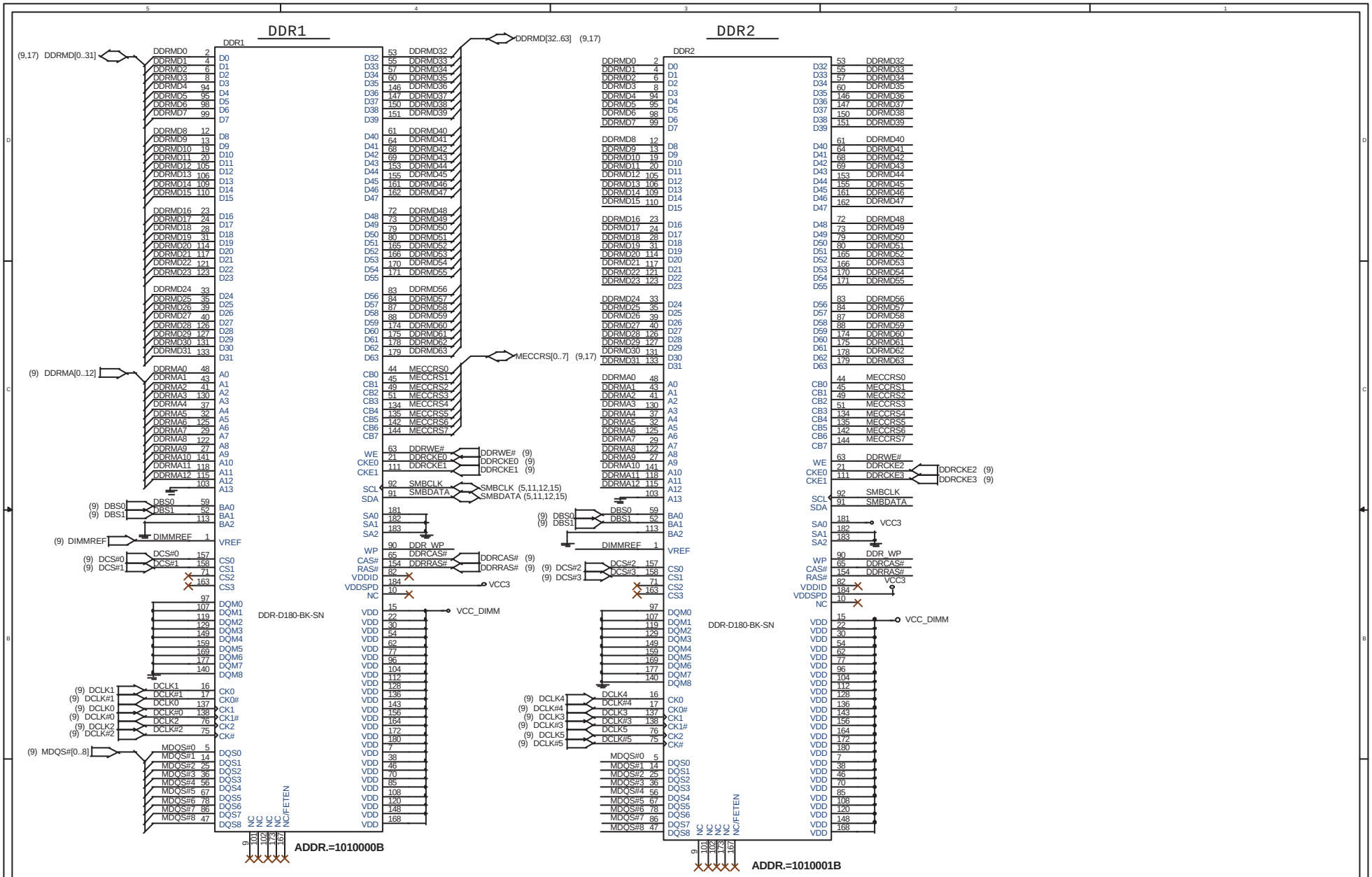


FOR EMI



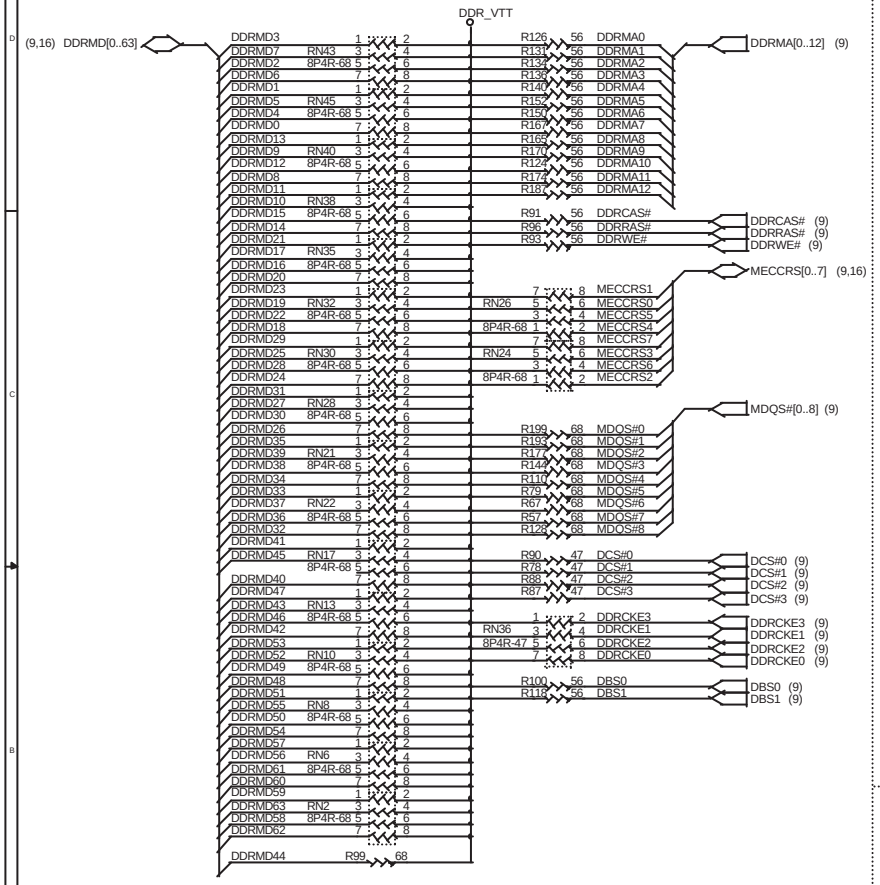
JP2	AUDIO DOWN
1 - 2	Auto mode
2 - 3	Disabled onboard audio codec

Micro-Star	Title: MS-6551	Rev: 10
Document Number: FWH & CNR RISER		
Last Revision Date: Sunday, October 21, 2001	Sheet 15 of 34	

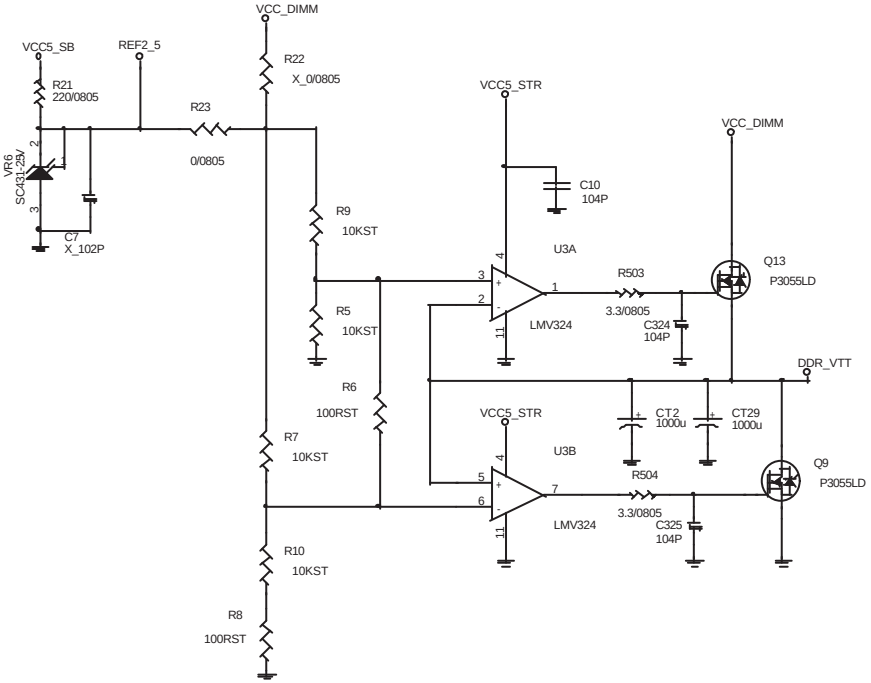


Micro-Star	Title: MS-6551		Rev: 10
Document Number: DDR 1 & 2			
Last Revision Date: Sunday, October 21, 2001		Sheet 16 of 34	

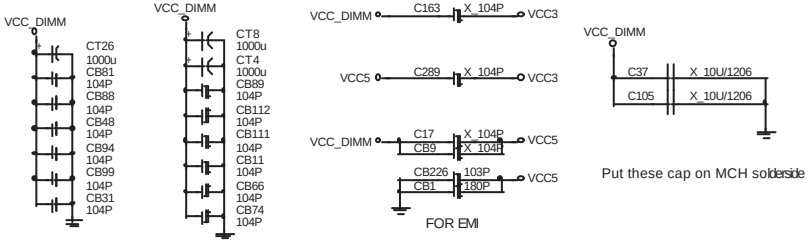
DDR TERMINATION

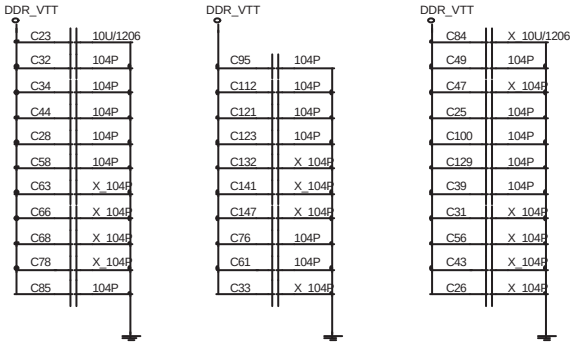


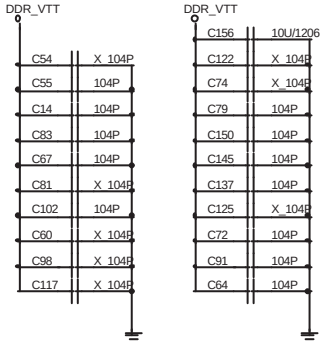
DDR POWER



DECOUPLING CAPACITORS







Micro-Star	Title: MS-6551	Rev: 10
Document Number: DDR_VTT & TERMINATION		
Last Revision Date: Monday, October 22, 2001	Sheet 17 of 34	

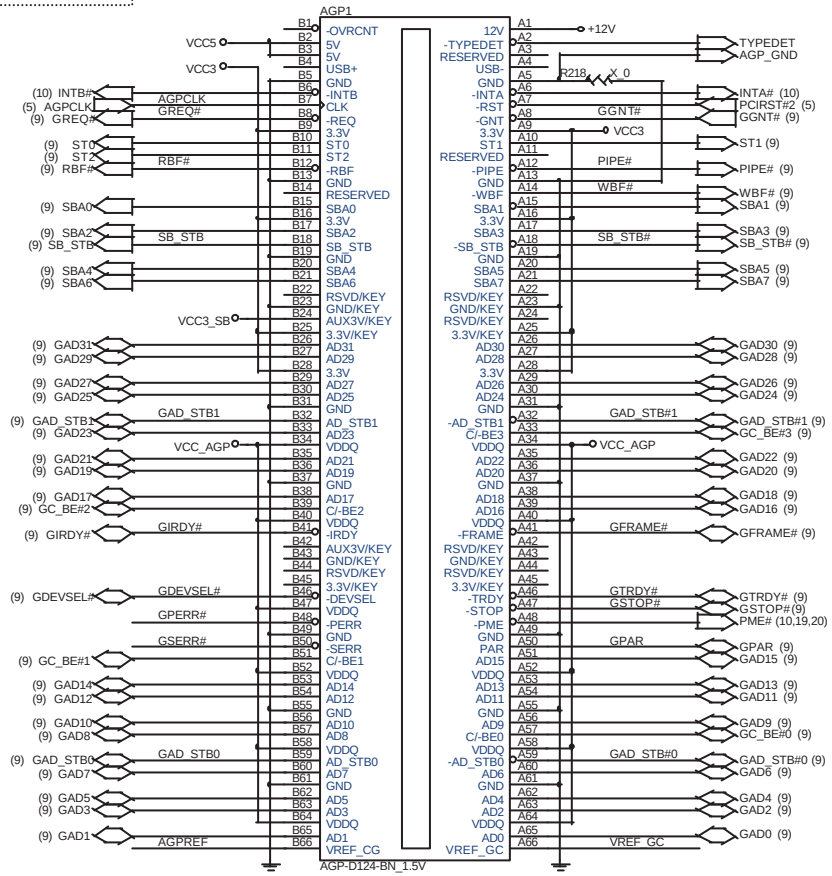
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

AGP Slot Imax

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

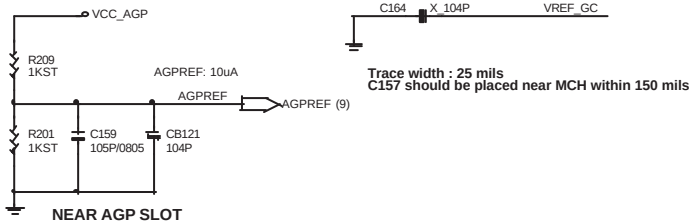
INTA#
INTB#



1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

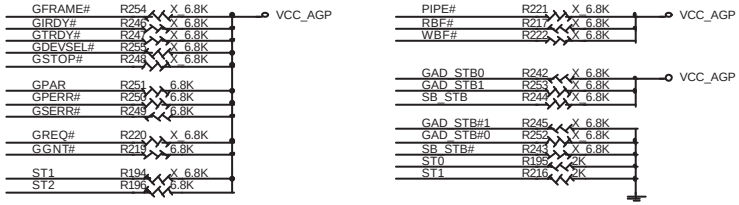
SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

AGP SIGNAL REFERENCE CIRCUIT



Trace width : 25 mils
C157 should be placed near MCH within 150 mils

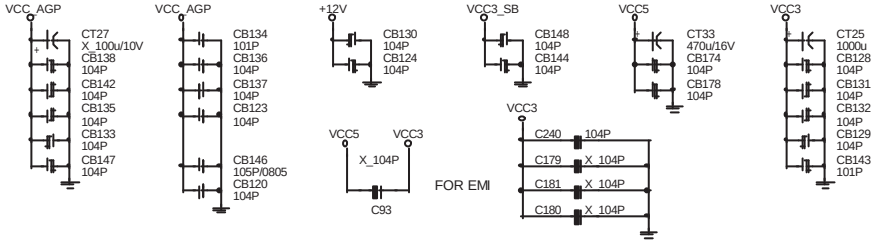
AGP TERMINATION RESISTORS

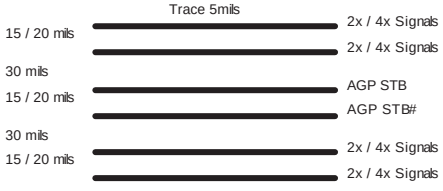


LESS 100MILS STUB TRACE LENGTHMUSTBE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS





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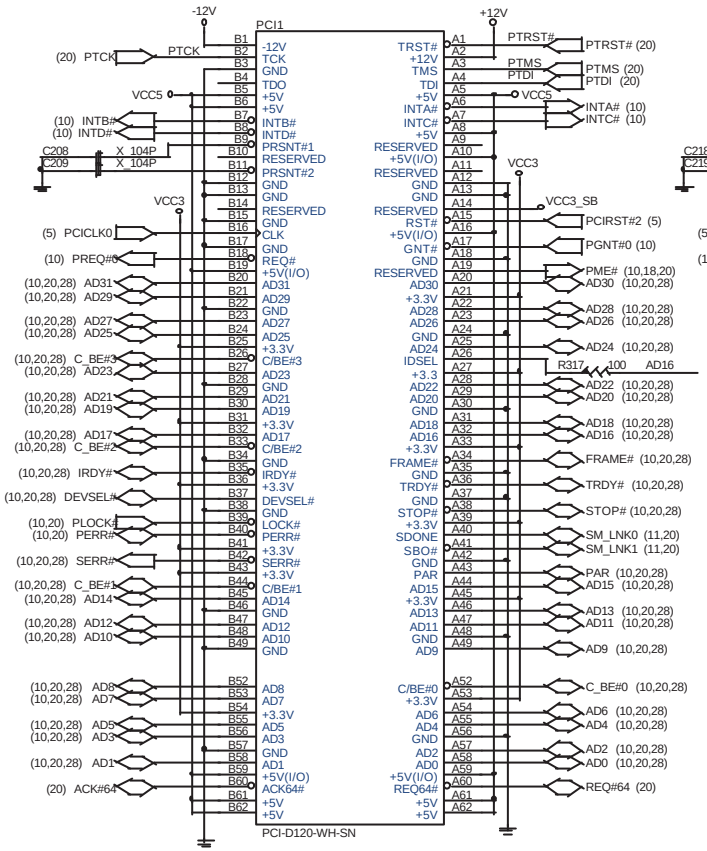
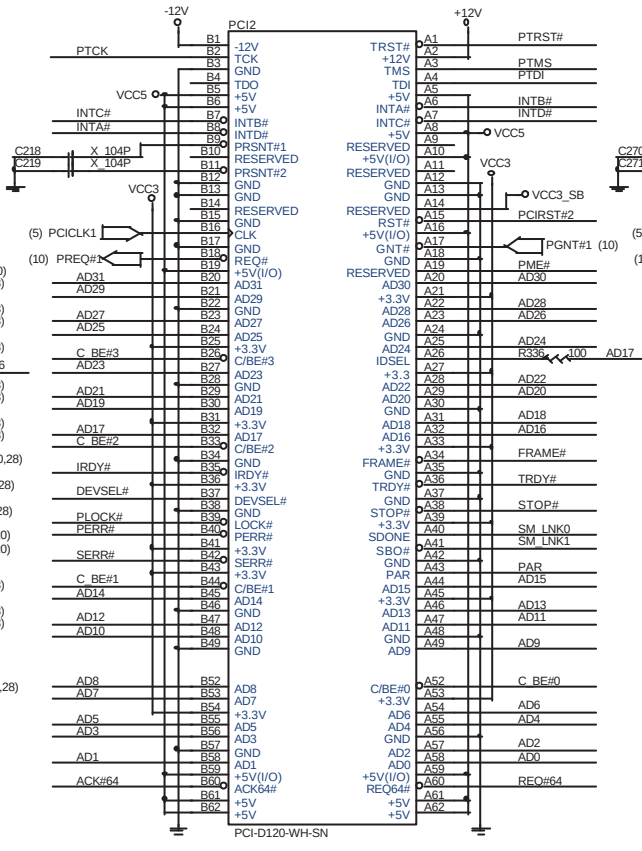
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



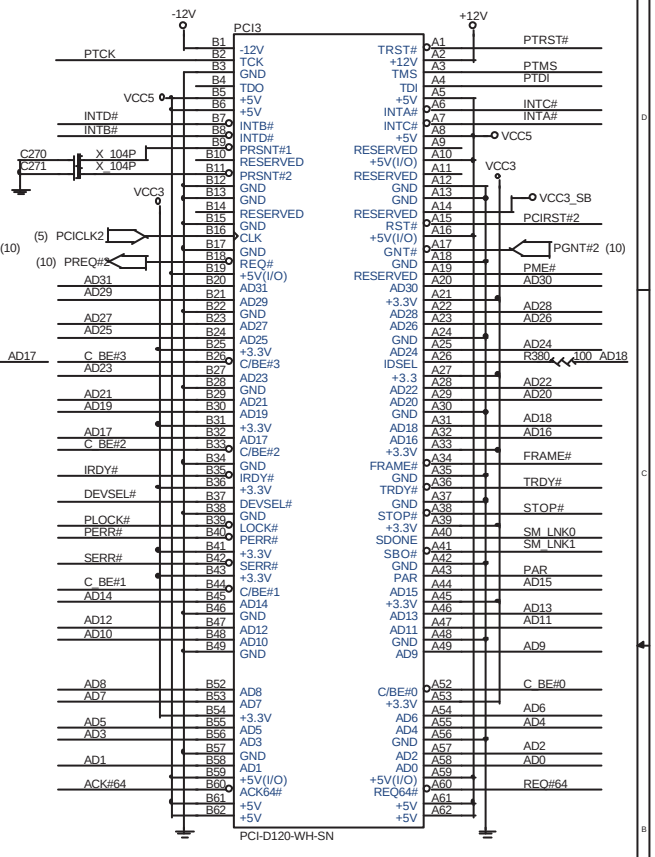
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



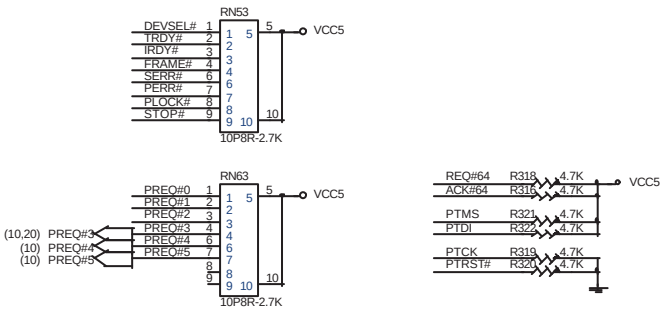
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

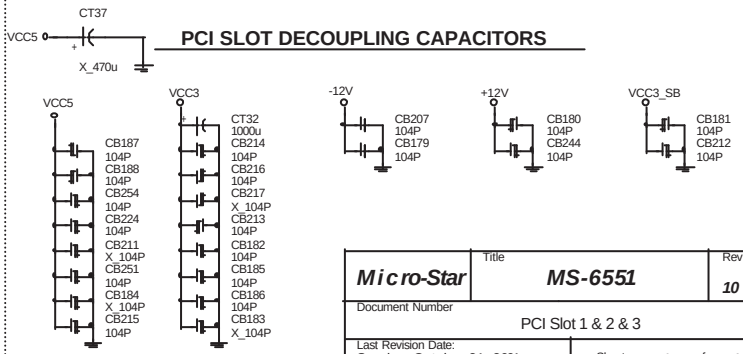


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6551	Rev: 10
Document Number: PCI Slot 1 & 2 & 3		
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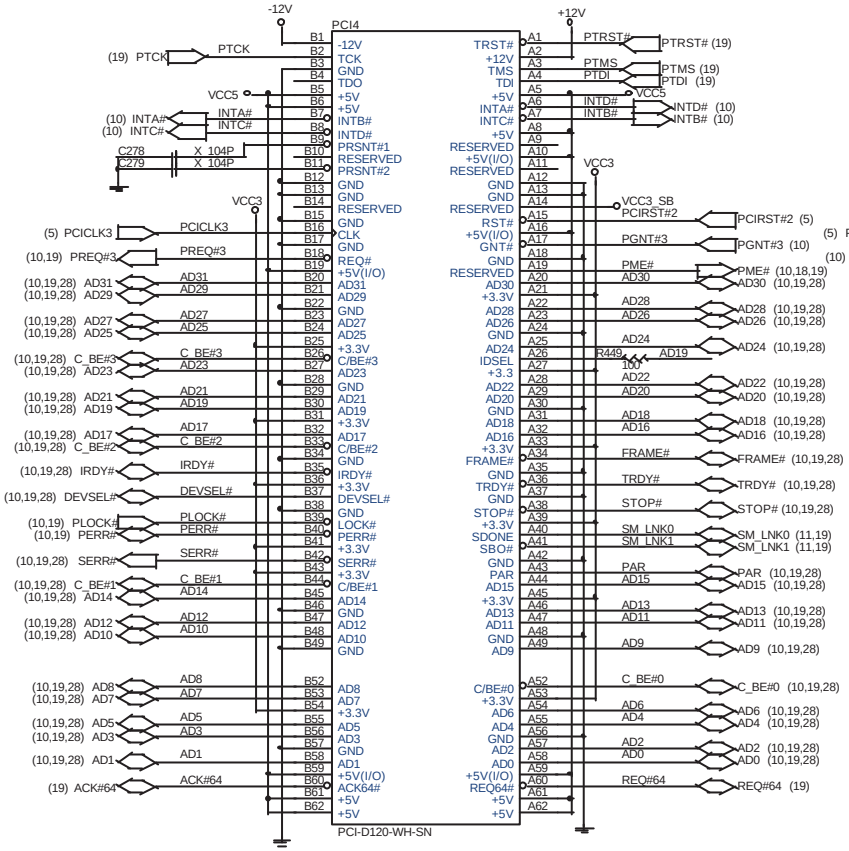
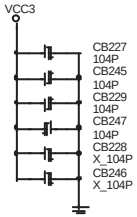
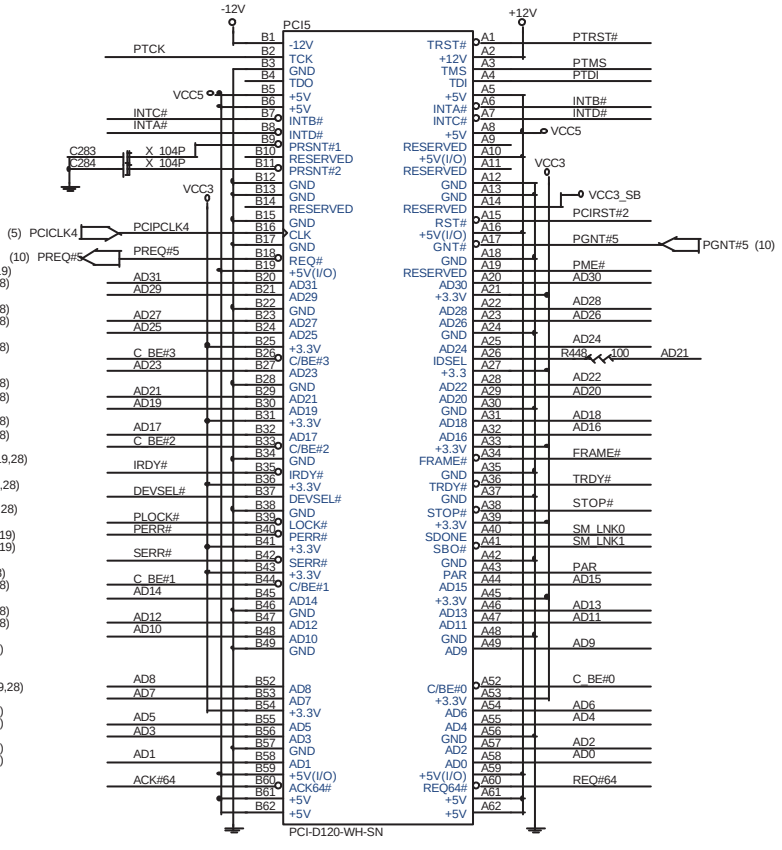
PCI SLOT 4 (PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER = PREQ3
INTD#



PCI SLOT 5 (PCI VER: 2.2 COMPLY)



IDSEL = AD21
MASTER = PREQ5
INTB#

Micro-Star	Title: MS-6551	Rev: 10
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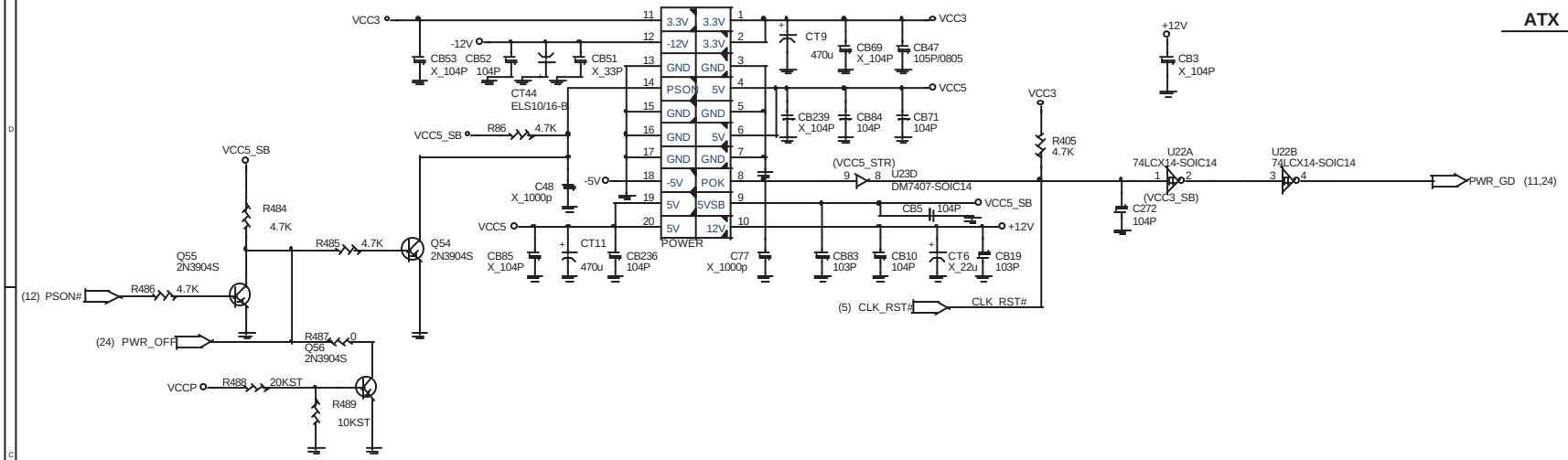
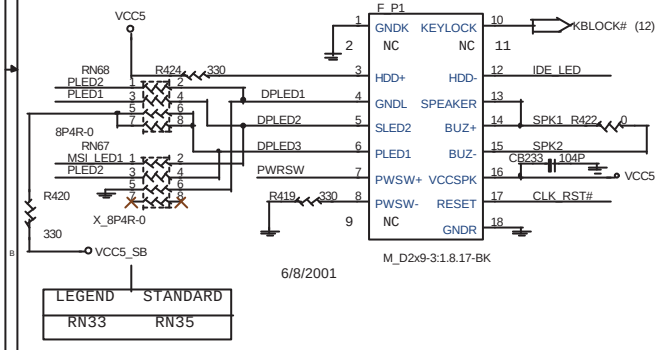
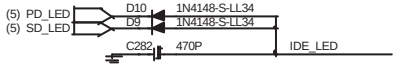
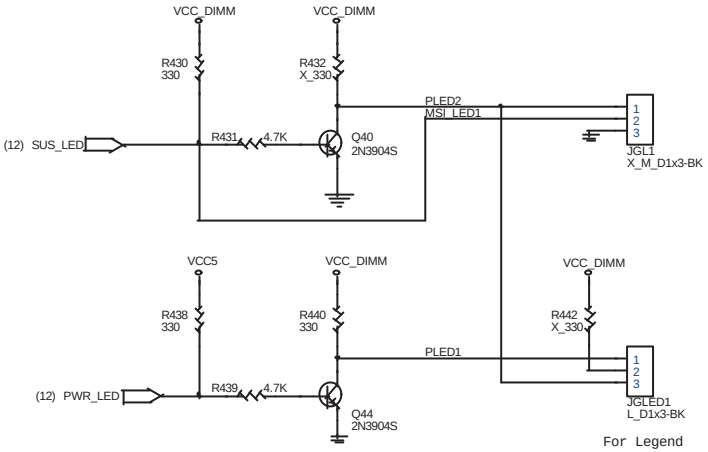


Brookdale FRONT PANEL-M



LEGEND	STANDARD
RN33	RN35

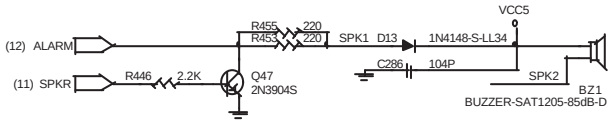




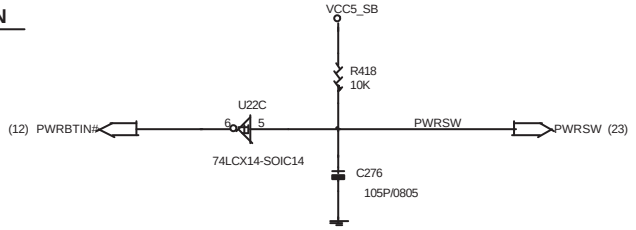
Front Panel LED Circuit component selection

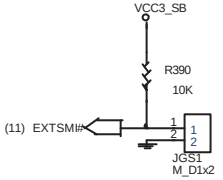
	LEGEND	MSI
R420	ON	OFF
R439	ON	OFF
R440	ON	OFF
R438	ON	OFF
R442	ON	OFF
R432	OFF	ON
R431	ON	ON
R430	4.7K	330
RN68	ON	OFF
RN67	OFF	ON
Q40	ON	ON
Q44	ON	OFF
JGL1	OFF	ON
JGLED1	ON	OFF

SPEAKER



POWER BUTTON





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Document Number: Front Panel & Connector		
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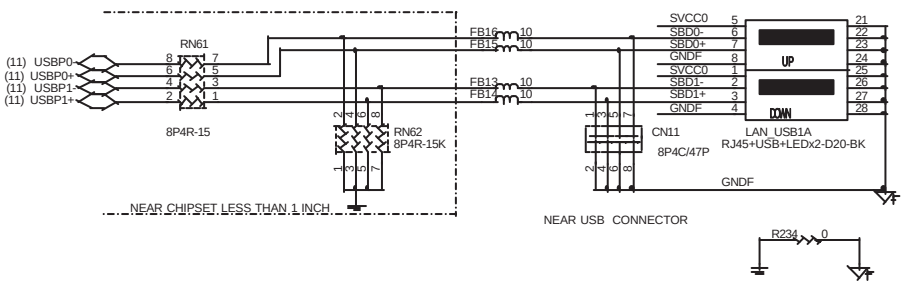
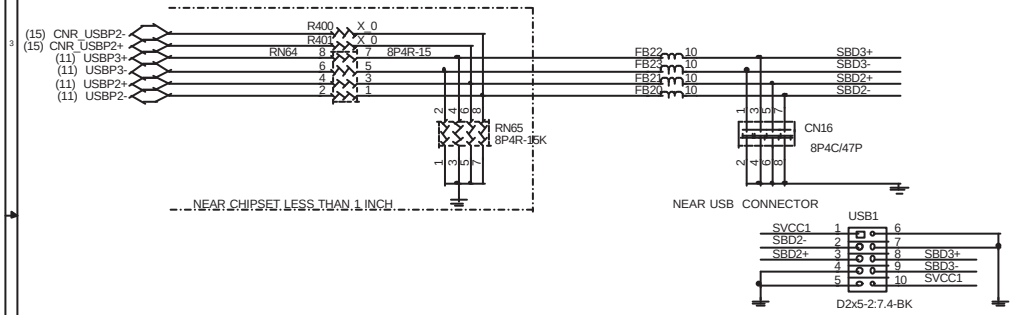
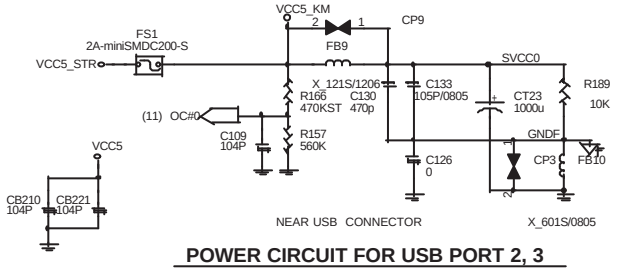
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



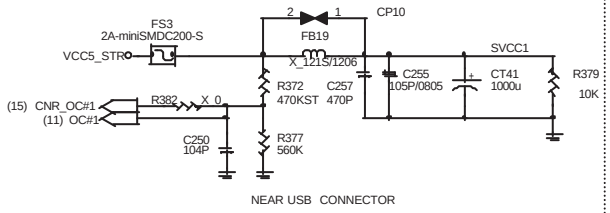
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



POWER CIRCUIT FOR USB PORT 2, 3



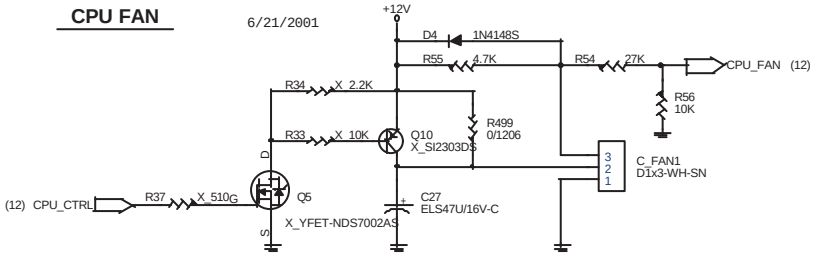
*** USB Trace width : 9 mils**

*** USB Trace Spacing : 25 mils**

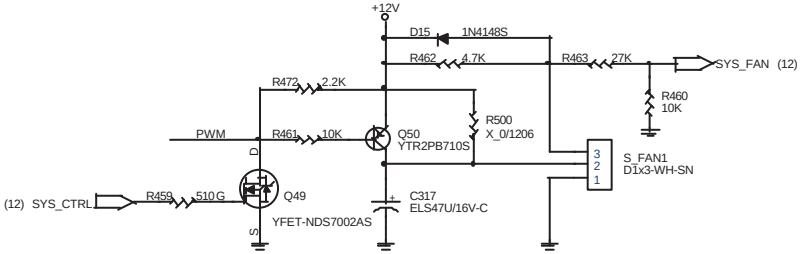
*** Differential USB Signlas Trace Spacing : 18 mils**

*** USB Power Trace must be 40mils width**

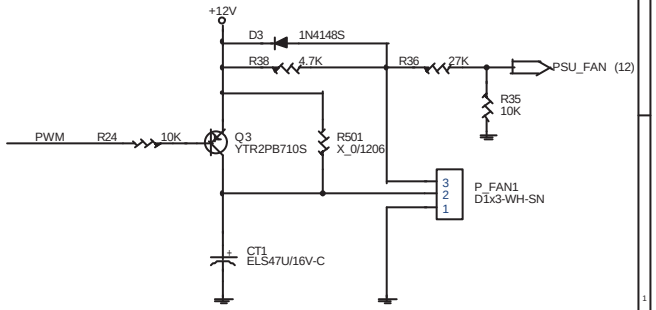
CPU FAN



SYSTEM FAN



ATX PSU FAN ON/OFF CONTROL



Micro-Star	Title: MS-6551	Rev: 10
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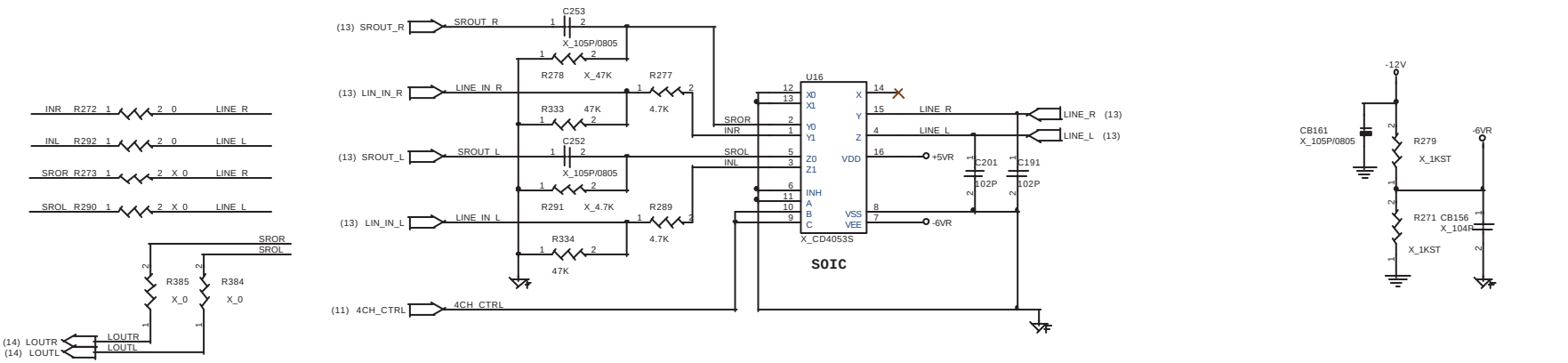
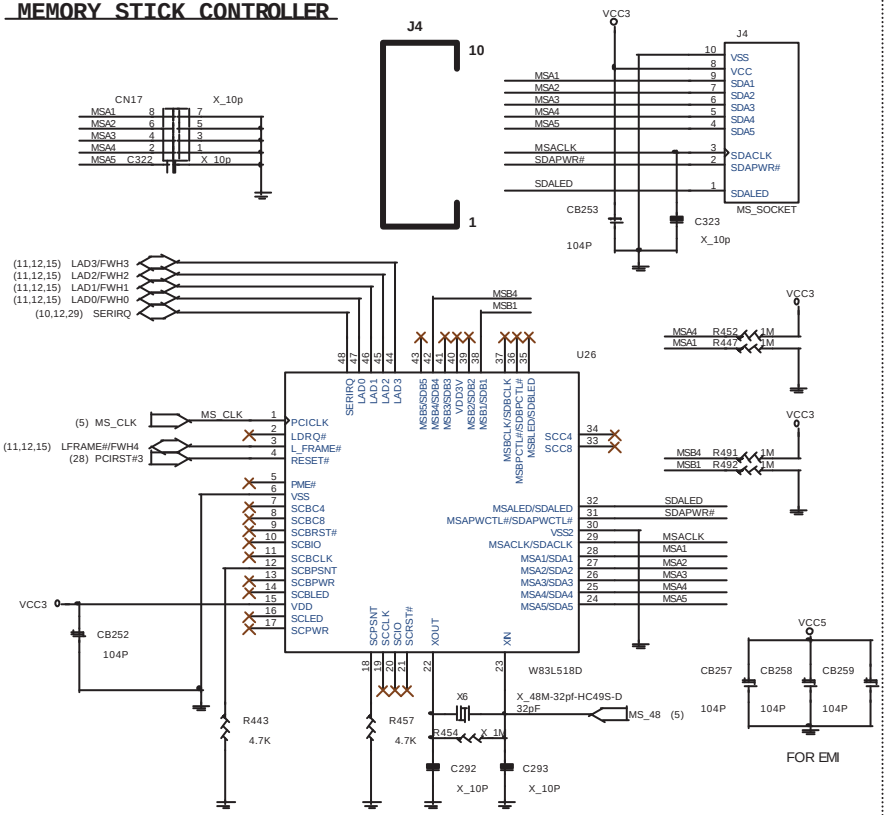
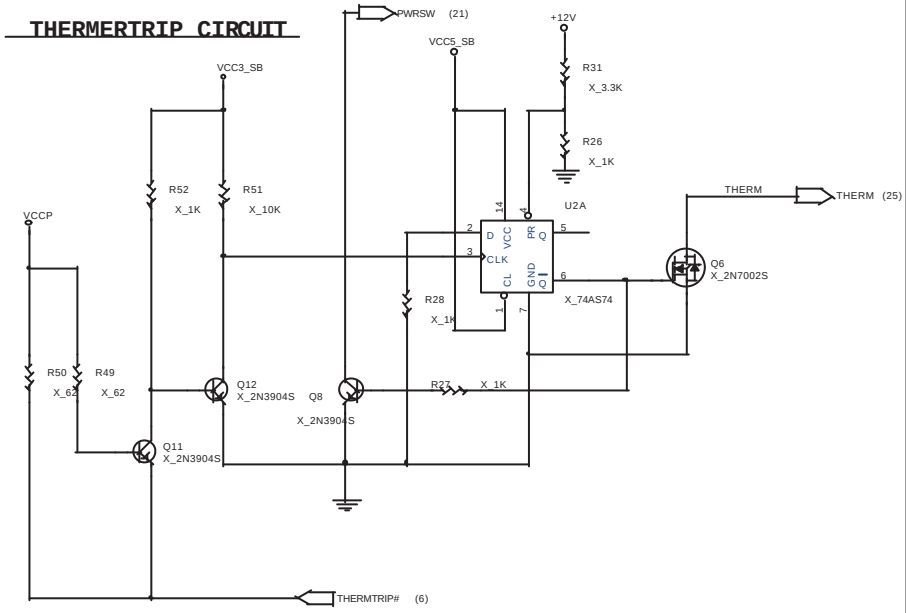
4 CHANNEL CONTROLLER



MEMORY STICK CONTROLLER



THERMERTRIP CIRCUIT



Micro-Star	Title: MS-6551		Rev: 10
Document Number: 4 CHANNEL CONTROL			
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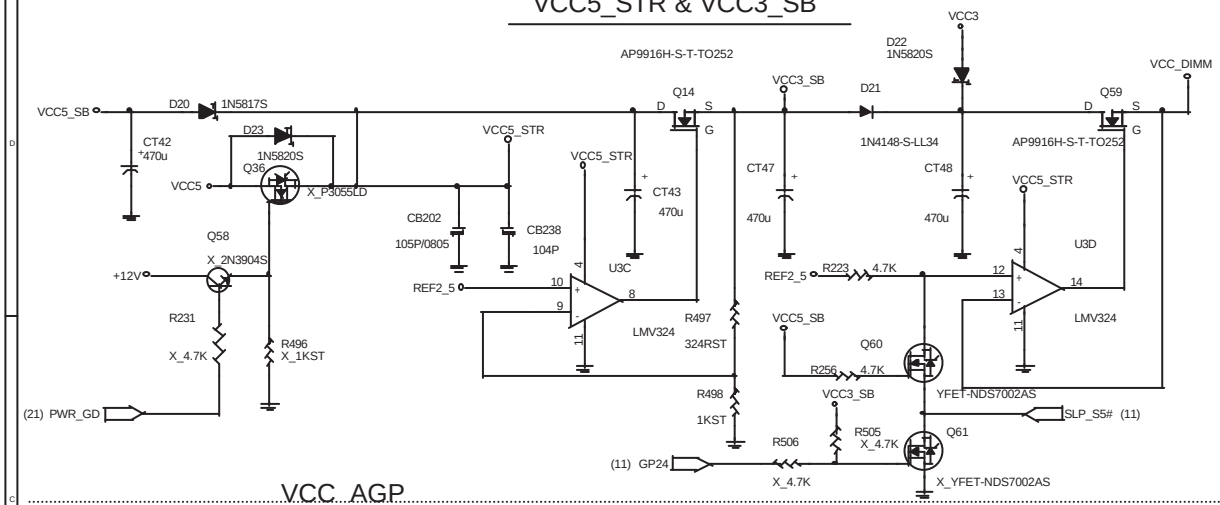
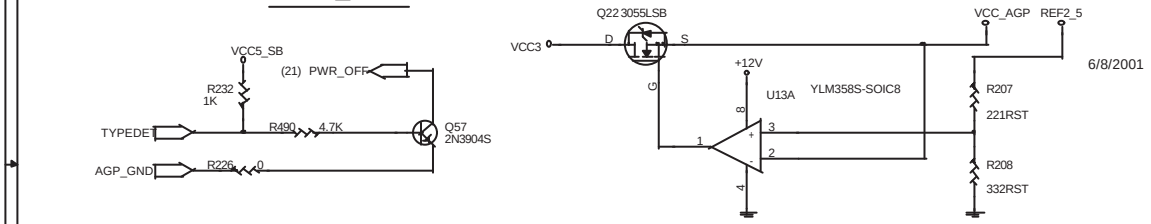
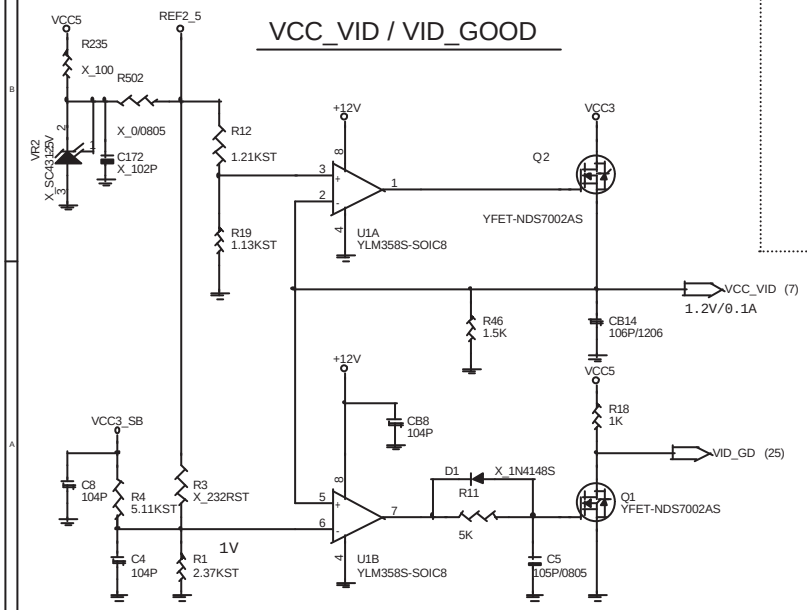
VCC5_STR & VCC3_SB

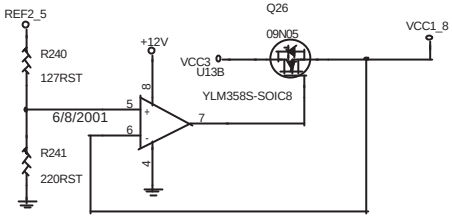


VCC_AGP



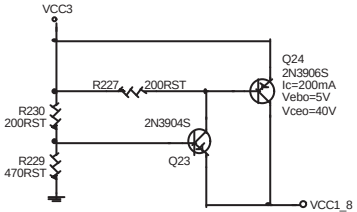
VCC_VID / VID_GOOD





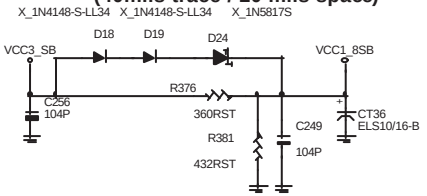
VCC1_8

1.8V/3.3V SEQUENCE CIRCUIT



1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1881A	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

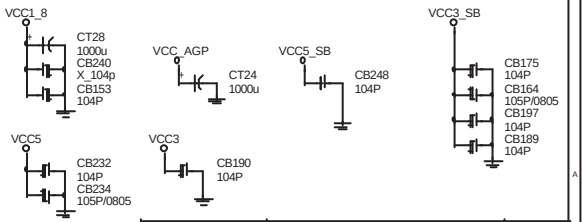
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

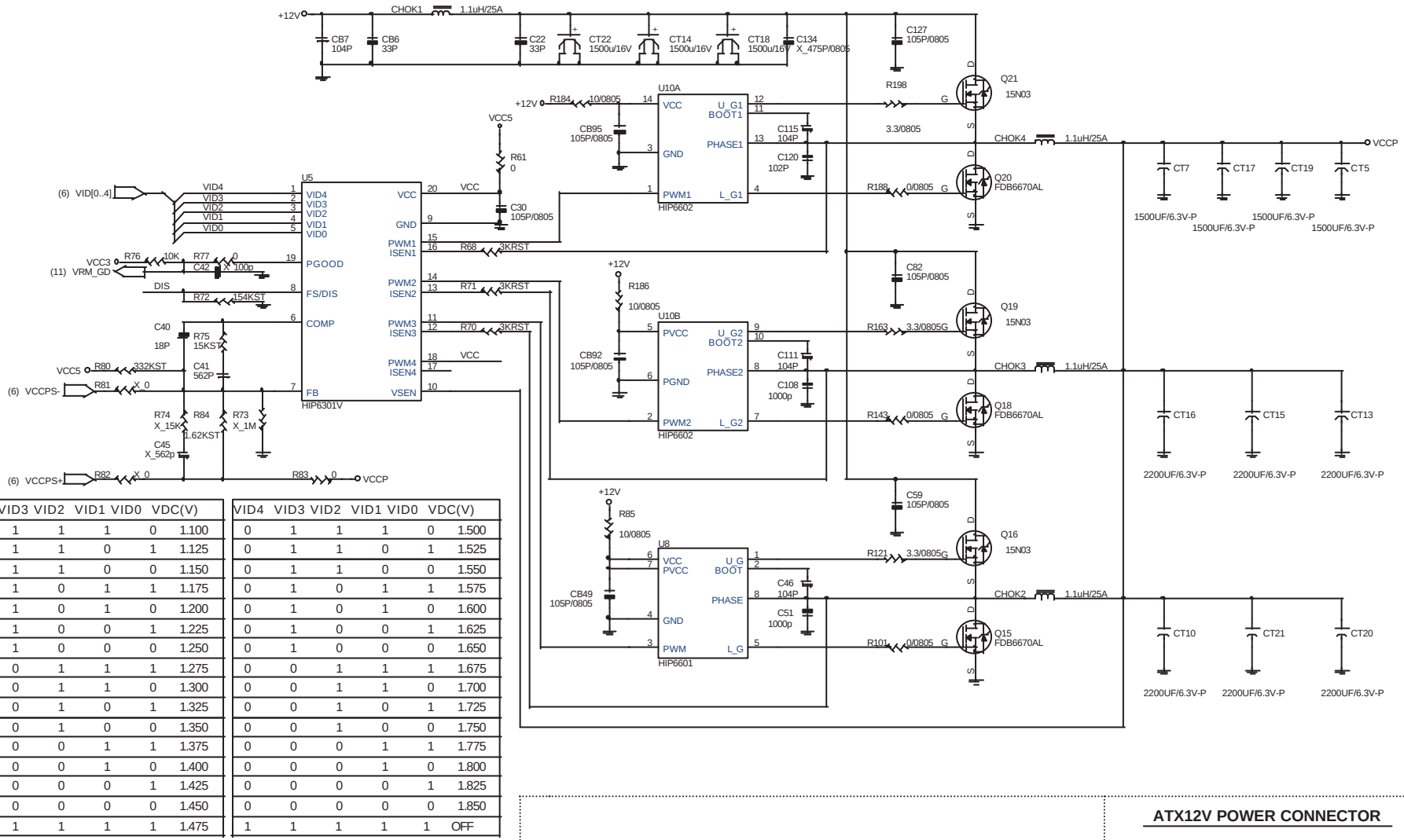
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

REGULATORS OUTPUT DECOUPLING CAPACITORS



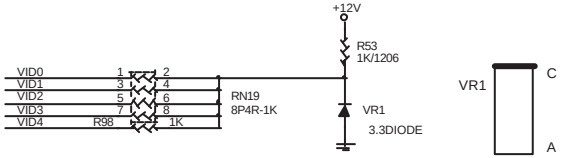
Micro-Star	Title: MS-6551	Rev: 10
Document Number: Voltage Regulator		
Last Revision Date: Sunday, October 21, 2001	Sheet 24 of 34	



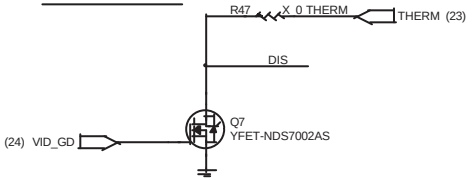
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

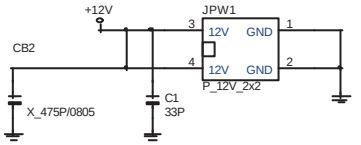
VID PULL-UP RESISTORS



PWM GOOD

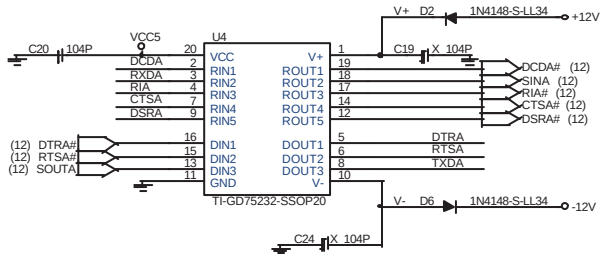


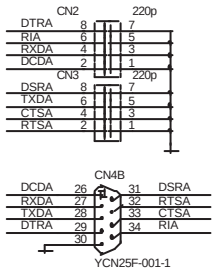
ATX12V POWER CONNECTOR



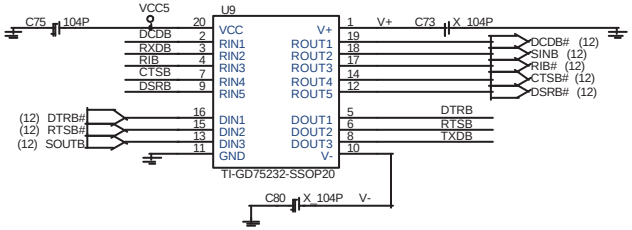
Micro-Star	Title: MS-6551	Rev: 10
Document Number: VRM 9.2		
Last Revision Date: Sunday, October 21, 2001	Sheet 25 of 34	

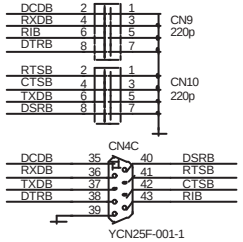
SERIAL PORT 1



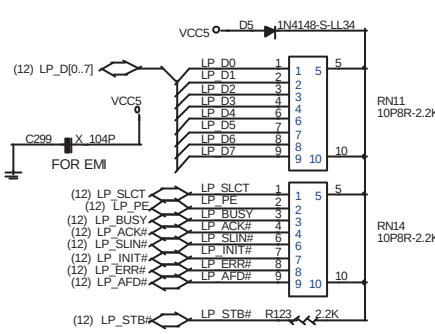


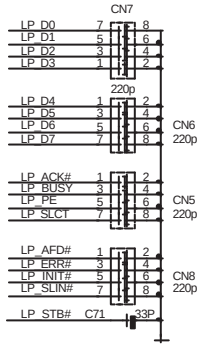
SERIAL PORT 2

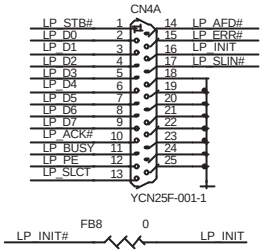




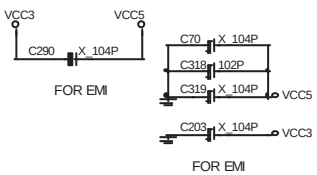
PARALLAL PORT

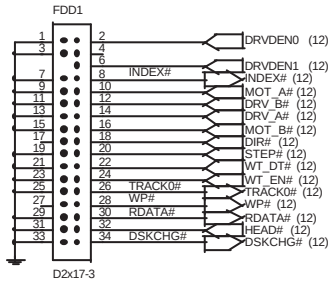




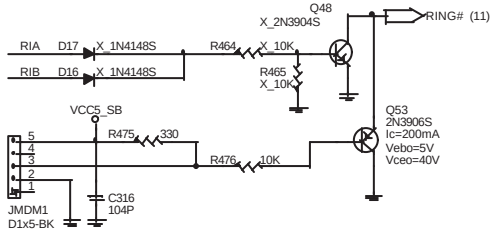


FLOPPY CONNECTOR

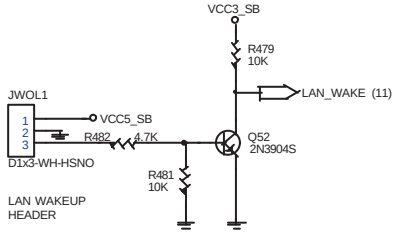




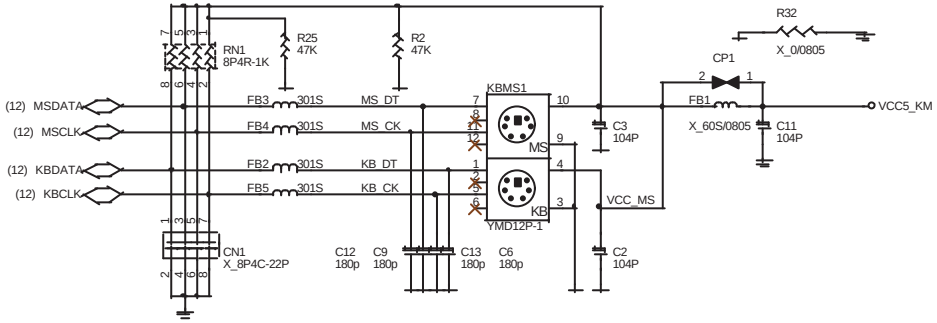
MODEM RING BLOCK

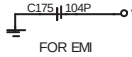


LAN WAKEUP BLOCK



PS2 KEYBOARD & MOUSE CONNECTOR





Micro-Star	Title: MS-6551	Rev: 10
Document Number: IO Connector		
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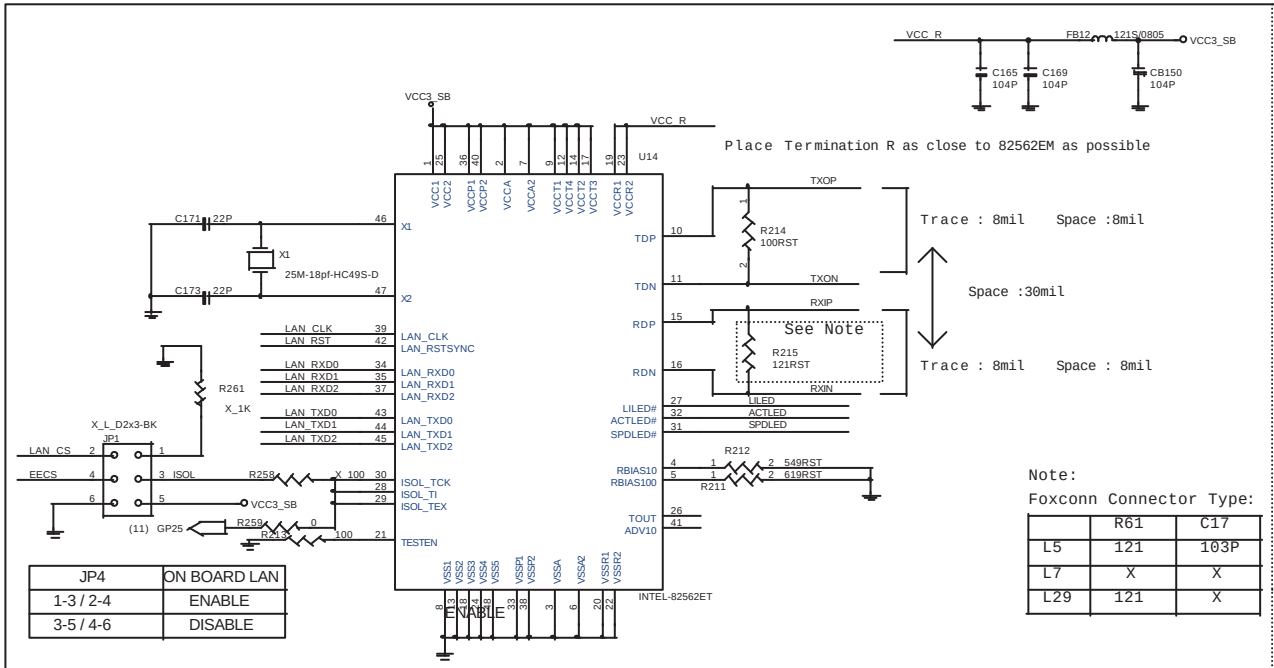
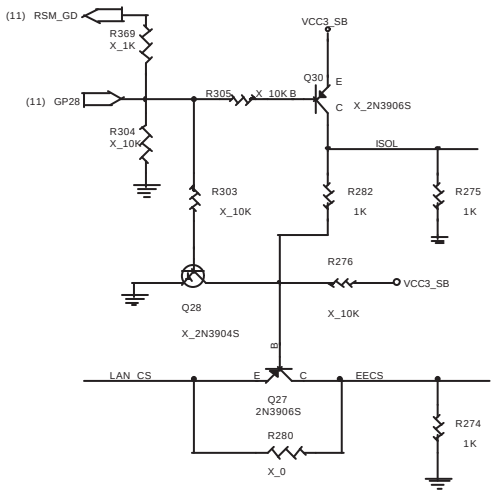
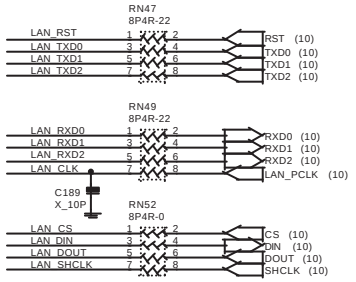


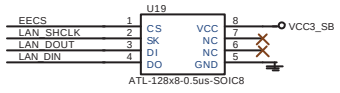
LAN DISABLE



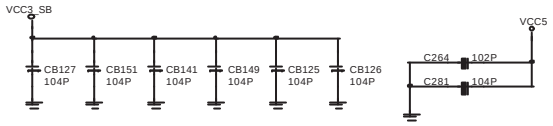
LAN OPTION RESISTORS

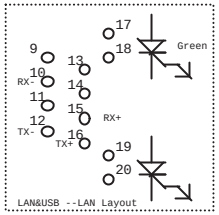


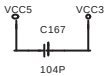
LAN EEPROM

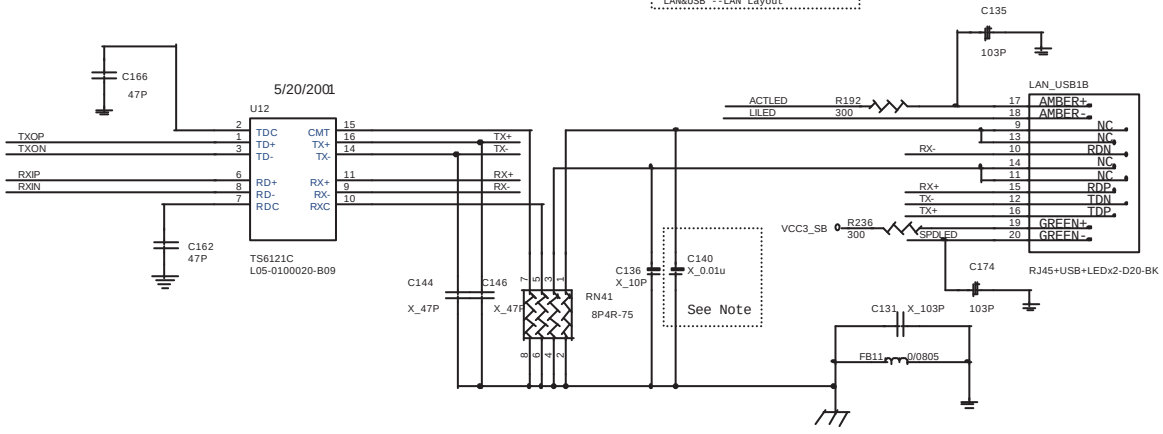


5/20/2001





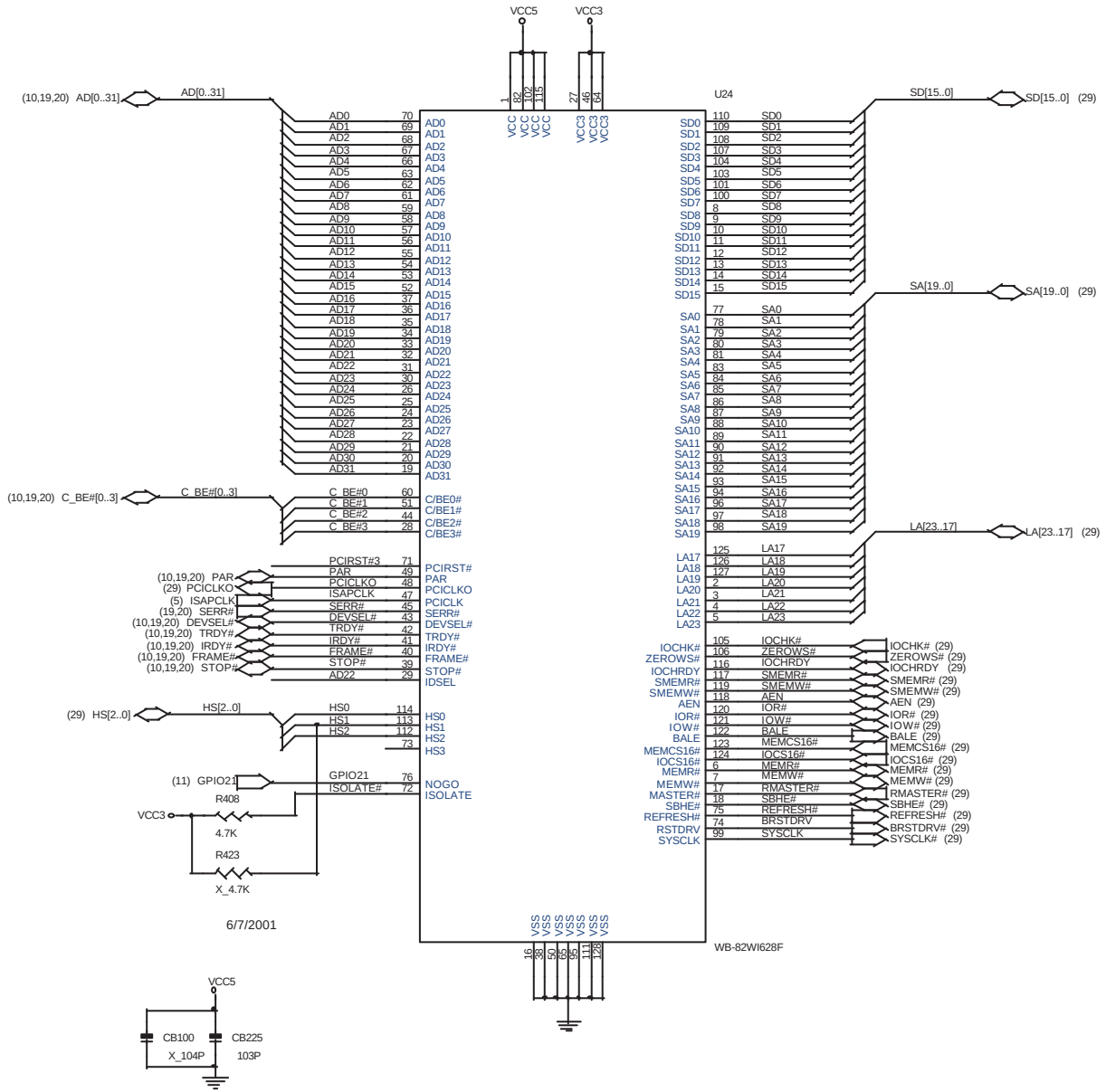




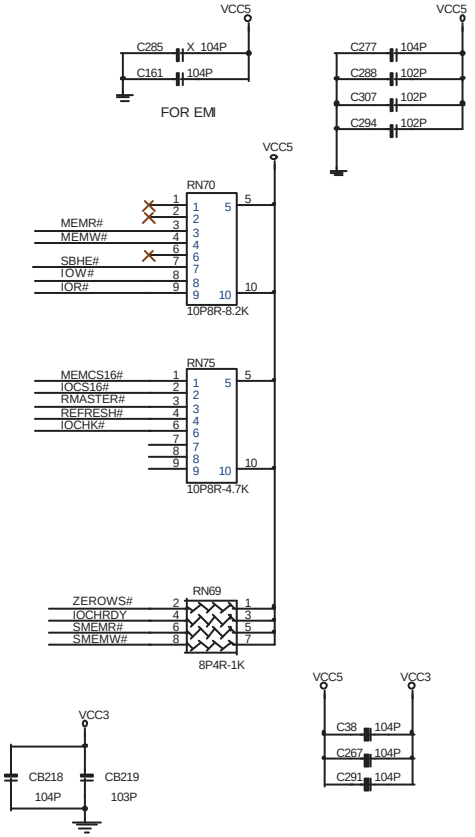
Remark:
82562EM with 93C66:M33-26N0103-A26
82562ET with 93C46:M33-15O0203-A26 *

Micro-Star	Title: MS-6551	Rev: 10
	Document Number: LAN INTEL 82562EM/ET	
	Last Revision Date: Monday, October 22,2001	Sheet 27 of 34

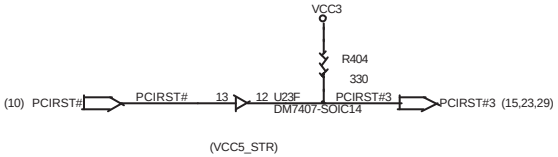
PCI To ISA Bridge, Part 1



PCI to ISA Bridge Pull Up / Low

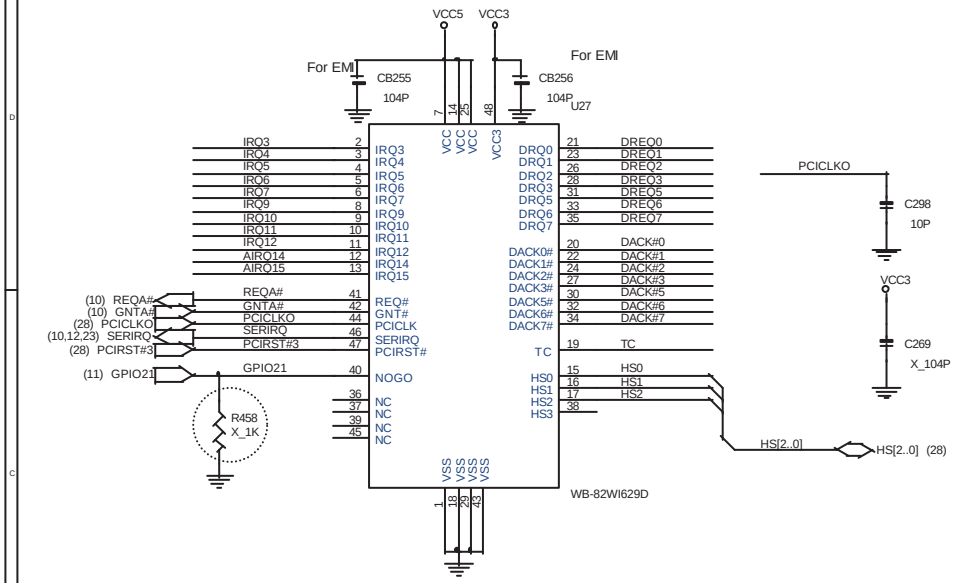


PCI to ISA Bridge Reset

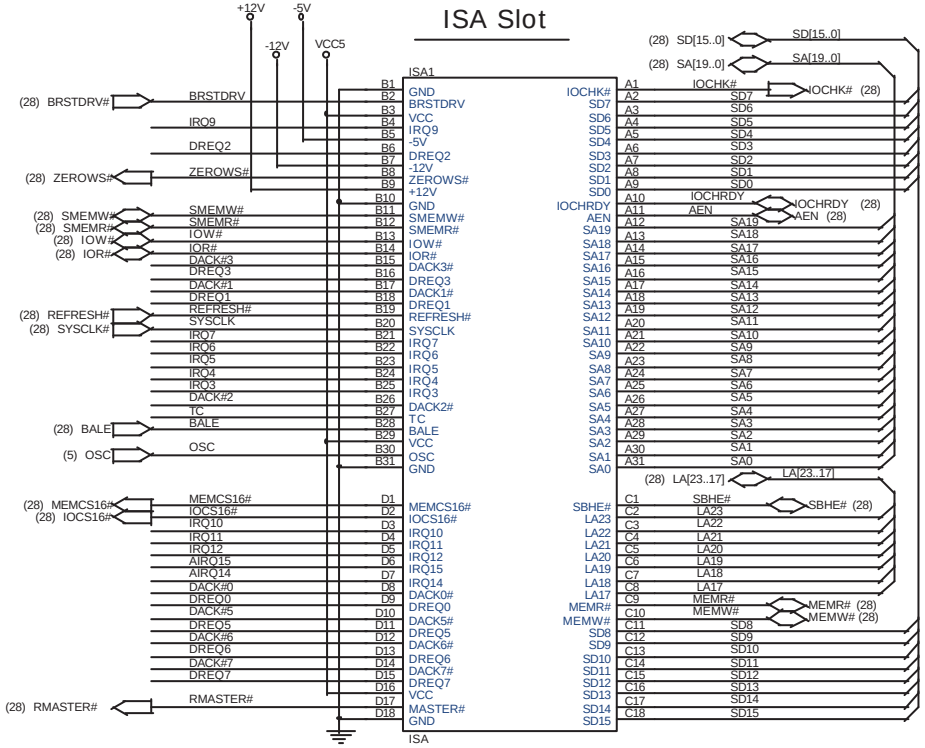


Micro-Star	Title: MS-6551	Rev: 10
Document Number: ISA Bridge Part 1		
Last Revision Date: Sunday, October 21, 2001	Sheet 28 of 34	

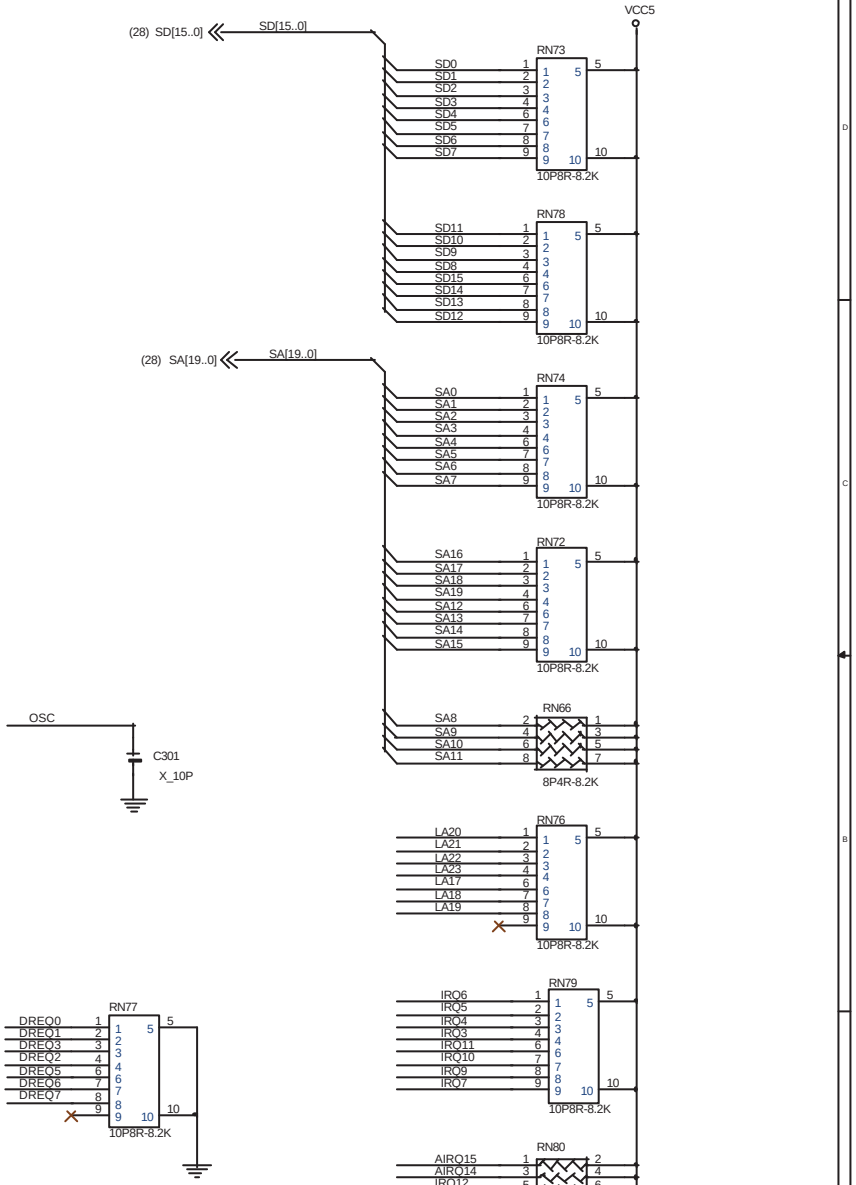
PCI To ISA Bridge, Part 2



ISA Slot



PCI to ISA Bridge Pull Up / Low



Micro-Star	Title: MS-6551	Rev: 10
Document Number: ISA Bridge Part 2 / ISA SLOT		
Last Revision Date: Sunday, October 21, 2001	Sheet 29 of 34	

Jumper Setting & Connector Setting

Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
DIM3	SDRAM DIMM3
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
PCI4	PCI Slot4
PCI5	PCI Slot5
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
USB1	USB REAR CONNECTOR
USB2	USB INTERNAL HEADER
POWER	ATX Power
F_P1	Front Panel
C_FAN1	CPU FAN HEADER
S_FAN1	SYS FAN HEADER
P_FAN1	ATX FAN HEADER
JAUDIO1	AUDIO HEADER FOR LEGEND
CD_IN1	CD IN HEADER
CD_IN2 / JSCD1	CD-IN HEADER FOR LEGEND
AUX_IN1	AUX_IN HEADER
MDM_IN1	MODEM_IN HEADER
IR1	IR HEADER
JPW1	ATX12V Power

Micro-Star	Title: MS-6551	Rev: 10
Document Number: JUMPER SETTING		
Last Revision Date: Thursday, October 11, 2001	Sheet 30 of 34	

JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

JBAT1(1-2)
YJUMPER-MG

LEGEND AUDIO

J(KKK)
JC-D2x2-GN

BAT SOCKET

BAT1[A]
YSKTBT

J3 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

J3(2)
YJUMPER-MG

JP2	AUDIO DOWN
OPEN	Auto mode
SHORT	Disabled onboard audio codec

JP2(1-2)
YJUMPER-MG

JP1	ON BOARD LAN
1-3 / 2-4	ENABLE
3-5 / 4-6	DISABLE

JP1(13/24)
X_JC-D2x2-GN

MS6551 PCB

PCB
MS-6551-10

COM1
YCN9M-1

COM2
YCN9M-1

U11_X-A-1
845-MCH-PIN

U11_X-B-1
845-MCH-PIN

U11_X-C-1
845-MCH-PIN

U11_X-D-1
845-MCH-PIN

U11_X
845-MCH-H

USB
UP
DOWN
USBA

U25_1

1	VPP	VCC	32
2	RST#	CLK	31
3	FGPI3	FGPI4	30
4	FGPI2	IC(VIL)	29
5	FGPI1	GNDA	28
6	FGPI0	VCCA	27
7	WP#	GND	26
8	TBL#	VCC	25
9	ID3	INIT#	24
10	ID2	FWH4	23
11	ID1	RFU	22
12	ID0	RFU	21
13	FWH0	RFU	20
14	FWH1	RFU	19
15	FWH2	RFU	18
16	GND	FWH3	17

SST49LF002A

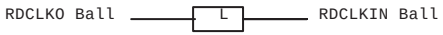
Micro-Star	Title: MS-6551	Rev: 10
Document Number: MANUAL		
Last Revision Date: Monday, October 22, 2001	Sheet 31 of 34	

SDRAM Routing Guidelines

5.Feedback - RDCLKO,RDCLKIN routing rule

2 or 3 DIMM feedback layout guideline

Signal	Length	Width	Trace Spacing
Trace L	1 inch	7 mil	5 mil



DDR-SDRAM Routing Guidelines

1.DDR bus reference plane stack-up

PCB Layer	Description
Layer 1	Signal
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Power / Signal

***All the memory bus signals must be referenced to GND**

2.DDR signal groups

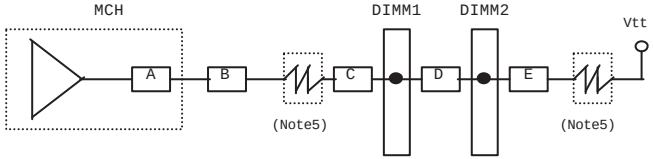
Group	Signals
Data	SDQ[63:0],SCB[7:0],SDQS[8:0]
Command	SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE#
Control	SCKE[3:0],SCS#[3:0]
Clock	SCK[5:0],SCK#[5:0]
Feedback	RCVENOUT#,RCVENIN#

3.SDQ[63:0],SCB[7:0],SDQS[8:],SCK/SCK#[5:0]routing rule

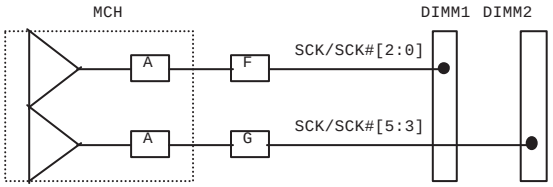
Signal	Length A	Length B	Length C	Length D	Length E	Width	Spacing	Routing Layer
SDQ[63:0] SCB[7:0] SQDS[8:0]	Package length	2.0" - 5.0"	Max = 0.5"	0.3' - 0.5"	0.1" - 0.8"	5 mil	(Note2)	Top
(Note1)	DIMM 1 = A + B + C = X DIMM 2 = A + B + C + D = X + D							
SCK/SCK#[2:0]	Package length	B+C+2"<= Length F <= B+C+1" 2.0" - 6.5"		None	None	5 mil	(Note4)	Bottom
	DIMM 1 = A + F = X + 1" to X + 2"							
SCK/SCK#[5:3] (Note3)	Package length	B+C+D+2"<= Length G <= B+C+D+1" 2.5" - 7.0"				5 mil	(Note4)	Bottom
	DIMM 2 = A + G = X + D + 1" to X + D + 2"							

*** Package length see Table - 4**

SDQ[63:0],SCB[7:0],SDQS[8:] layout guideline



SCK[5:0] layout guideline



Note1:Each data and strobe signal group must be length matching +/- 25 mils

SDQS[X] = +/- 25 mils SDQ[X]/SCB[X] group length

Signals	Associated Strobe
SDQ[7:0]	SDQS0
SDQ[15:8]	SDQS1
SDQ[23:16]	SDQS2
SDQ[31:17]	SDQS3
SDQ[39:32]	SDQS4
SDQ[47:40]	SDQS5
SDQ[55:48]	SDQS6
SDQ[63:56]	SDQS7
SCB[7:0]	SDQS8

Note2:Trace spacing normally = 12 mils and through between DIMM 2 pin = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils

Note3:

- * SCK[X] length = SCK#[X] length
- * SCK/SCK#[2:0] routed to DIMM 0 are equal in length, and SCK/SCK#[5:3] routed to DIMM 1 are equal in 1ength

Note4:

- * Between the pair differential clock 2 signal trace spacing = 7 mils
- * Differential Trace with 2.5V copper flood spacing = 10 mils minimum
- * Serpentine spacing = 20 mils minimum
- * Differential signals breakout form MCH = 5 mil width with 7 mil differential spacing and 7 mil isolation spacing from another signal for a max of 350 mils

Note5:Data group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the command or control group signal

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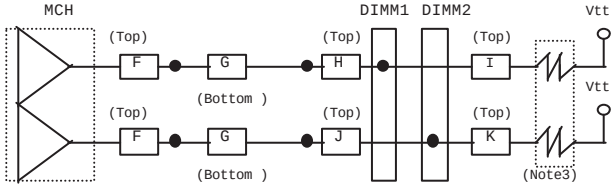
4.SCKE[3:0],SCS#[3:0] routing rule

DIMM 0					
Signal	Length F	Length G	Length H	Length I	Width
SCS#[1:0] SCKE[1:0] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils (Note2)	0.4" - 1.3"	5 mils
Total lenght	DIMM0 SCK/SCK#[2:0] length = X" DIMM0 SCS#/SCKE length = F + G + H = X"- 1"				
DIMM 1					
Signal	Length F	Length G	Length J	Length K	Width
SCS#[3:2] SCKE[3:2] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 1" (Note2)	0.1" - 0.8"	5 mils
Total lenght	DIMM1 SCK/SCK#[5:3] length = Y" DIMM1 SCS#/SCKE length = F + G + J = Y"- 1"				



Note1:

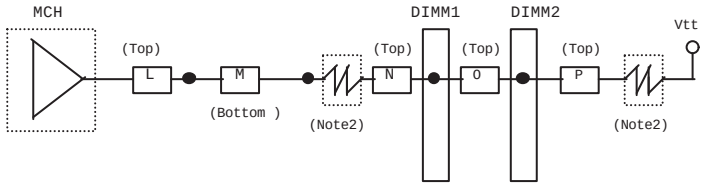
* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Control signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:This purpose prevent break form DIMM0 bottom size 2.5V copper flood to MCH power plane

Note3:Control group signal can NOT placed within the same parallel resistor packs as the command or data group signal

5.SMA[12:0],SBS[1:0],SRAS#,SCAS# routing rule

Signal	Length L	Length M	Length N	Length O	Length P	Width
SMA[12:0] SBS[1:0] SRAS# SCAS# (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils	0.3" - 0.5"	0.1" - 0.8"	5 mils
DIMM 0 Total lenght	DIMM0 SCK/SCK#[2:0] length = X" Command signal length = L + M + N = X" - 1"					
DIMM 1 Total lenght	DIMM0 SCK/SCK#[5:3] length = Y" Command signal length = L + M + N + O = Y" - 1"					



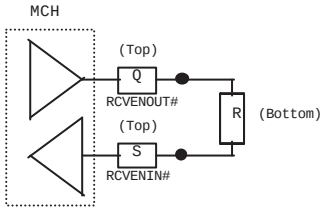
Note1:

* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:Command group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the data or control group signal

5.Feedback - RCVENOUT#,RCVENIN# routing rule

Signal	Length Q	Length R	Length S	Width
RCVENOUT# RCVENIN# (Note1)	40 mils	Equal 1"	40 mils	5 milS
Total Length	Q + R + S = 1080 mils			



Note1:

* Trace spacing = 12 mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 10 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

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DDR Data Signals(1)		
Signal	MCH ball	Package length(")
SDQ0	G28	0.716
SDQ1	F27	0.699
SDQ2	C28	0.874
SDQ3	E28	0.754
SDQ4	H25	0.532
SDQ5	G27	0.666
SDQ6	F25	0.592
SDQ7	B28	0.892
SDQ8	E27	0.797
SDQ9	C27	0.833
SDQ10	B25	0.812
SDQ11	C25	0.753
SDQ12	B27	0.886
SDQ13	D27	0.867
SDQ14	D26	0.773
SDQ15	E25	0.645
SDQ16	D24	0.722
SDQ17	E23	0.602
SDQ18	C22	0.699
SDQ19	E21	0.566
SDQ20	C24	0.785
SDQ21	B23	0.781
SDQ22	D22	0.640
SDQ23	B21	0.711
SDQ24	C21	0.627
SDQ25	D20	0.555
SDQ26	C19	0.587
SDQ27	D18	0.522
SDQ28	C20	0.615
SDQ29	E19	0.487
SDQ30	C18	0.579
SDQ31	E17	0.521

DDR Data Signals(2)		
Signal	MCH ball	Package length(")
SDQ32	E13	0.432
SDQ33	C12	0.543
SDQ34	B11	0.596
SDQ35	C10	0.590
SDQ36	B13	0.639
SDQ37	C13	0.552
SDQ38	C11	0.588
SDQ39	D10	0.626
SDQ40	E10	0.533
SDQ41	C9	0.605
SDQ42	D8	0.587
SDQ43	E8	0.522
SDQ44	E11	0.523
SDQ45	B9	0.715
SDQ46	B7	0.706
SDQ47	C7	0.643
SDQ48	C6	0.700
SDQ49	D6	0.664
SDQ50	D4	0.760
SDQ51	B3	0.922
SDQ52	E6	0.640
SDQ53	B5	0.846
SDQ54	C4	0.810
SDQ55	E5	0.670
SDQ56	C3	0.859
SDQ57	D3	0.811
SDQ58	F4	0.723
SDQ59	F3	0.814
SDQ60	B2	0.949
SDQ61	C2	0.893
SDQ62	E2	0.865
SDQ63	G5	0.689

DDR ECC Signals		
Signal	MCH ball	Package length(")
SCB0	C16	0.570
SCB1	D16	0.526
SCB2	B15	0.623
SCB3	C14	0.533
SCB4	B17	0.621
SCB5	C17	0.583
SCB6	C15	0.540
SCB7	D14	0.503

DDR Data Strobe Signals		
Signal	MCH ball	Package length(")
SDQS0	F26	0.651
SDQS1	C26	0.775
SDQS2	C23	0.738
SDQS3	B19	0.636
SDQS4	D12	0.493
SDQS5	C8	0.596
SDQS6	C5	0.776
SDQS7	E3	0.821
SDQS8	E15	0.520

DDR Clock Signals		
Signal	MCH ball	Package length(")
SCK0	E14	0.453
SCK#0	F15	0.432
SCK1	J24	0.454
SCK#1	G25	0.587
SCK2	G6	0.551
SCK#2	G7	0.543
SCK3	G15	0.371
SCK#3	G14	0.349
SCK4	E24	0.610
SCK#4	G24	0.548
SCK5	H5	0.589
SCK#5	F5	0.693

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