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MS-6550

Version : 1.0A 06/11/2002 Update

INTEL (R) Brookdale Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

**INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)**

On Board Chipset:

BIOS -- FWH
AC'97 Codec -- AD1881/1885
LPC Super I/O -- W83627HF
Clock Generation -- CY28324 //ICS950208
LAN -- INTEL 82562ET/EM

Expansion Slots:

DDR DIMM SLOT * 2
AGP2.0 SLOT * 1
PCI2.2 SLOT *3
ISA SLOT * 1 (Share PCI3)

Note :

Standard -> WO/ISA ;WO/LAN ;W/ADI1881
A -> With Intel LAN (82562ET + 93C46)
B -> With ISA (W83628 + W83629)
C -> Support Audio Codec ADI1885
D -> Support Intel LAN (82562EM + 93C66)
T -> With CPU Thermstrip Function

MS6550/VER: 10A BOM :

MS6550L2_Option : L -> Note -> A + C => 6550-010 (MP BOM)

MS6550L2_Option : I + L -> Note -> A + B +C => 6550-020 (MP BOM)

MS6550L2_Standard -> Note -> C =>6550-020 (MP BOM) -> 6550-030 (MP BOM) 7/June

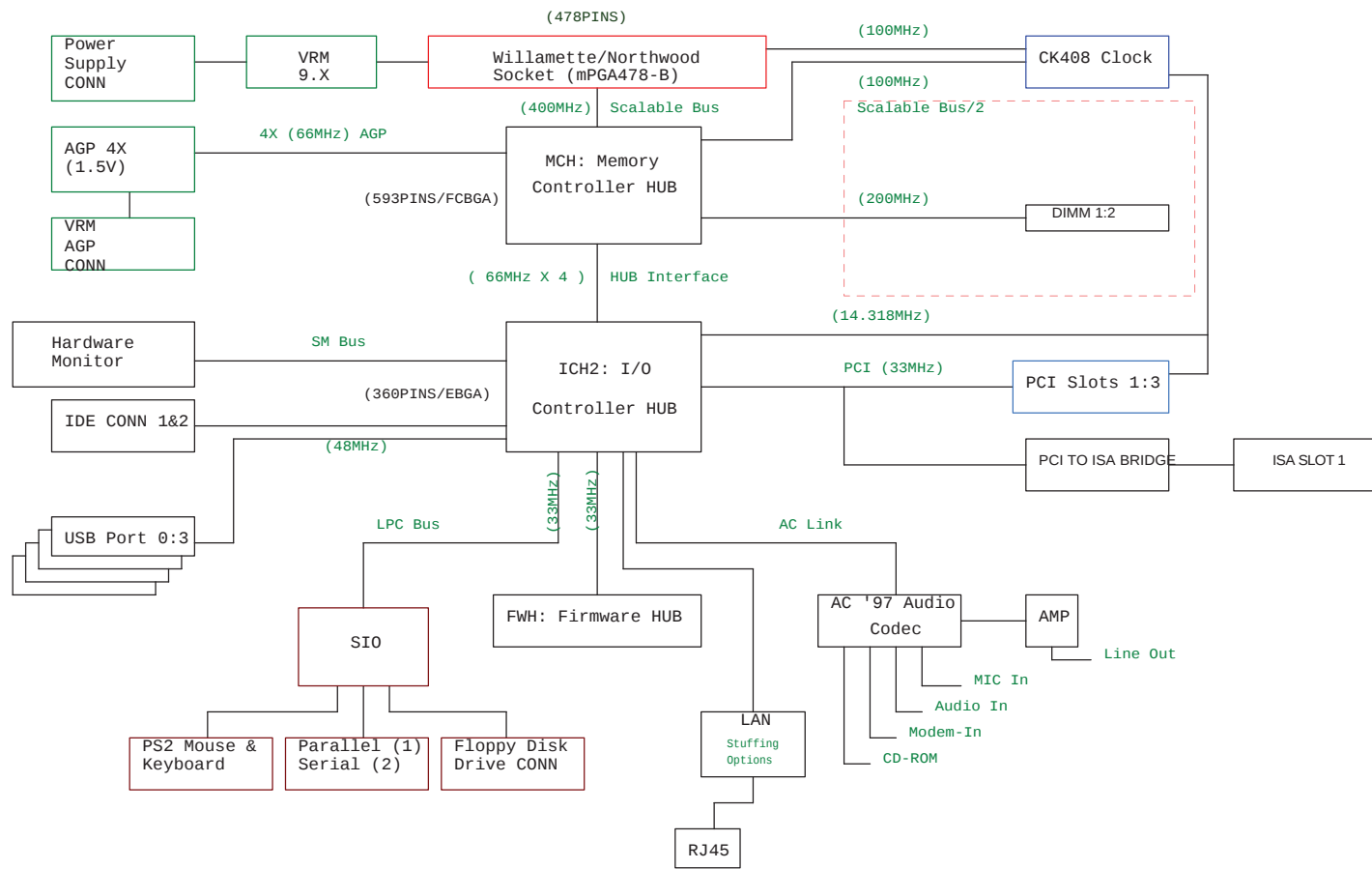
MS6550L2_Option : I -> Note -> B + C =>6550-020 (MP BOM) -> 6550-040 (MP BOM) 7/June

1.Release ECR for L2 P.S. compatibility and Q51/MOSFET too hot issue. 2002/06/07
2.Creat 2 New-BOM from 6550L2/OPT:I+L (6550-020) to 6550L2/OPT:I & Stand for PM requested 2002/06/11
3.Modify ICH2 "RTC" issue . (Reference to MS6551)

XXX MS6550L2_Option : L -> Note -> A + B + C => 6550-03S (ES BOM)

XXX MS6550_Option : L -> Note -> A + C => 6550-04S (ES BOM)

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General Purpose I/O Spec.

ICH2

GPIO Pin	PIN #	Type	Function
GPIO 0	M3	I	PCI TO ISA REQA#
GPIO 1	L3	I	Not Using (PREQ#5)
GPIO 2	N3	I	Not Using (INTE#)
GPIO 3	N2	I	Not Using (INTF#)
GPIO 4	N1	I	Not Using (INTG#)
GPIO 5	M4	I	Not Using (INTH#)
GPIO 6	Y11	I	Reserved for futuer
GPIO 7	AA11	I	Non Connect
GPIO 8	Y14	I	LAN Wake Up
GPIO 9	Y22	I	AC'97 Serial Data In 0
GPIO 10		I	Non Connect
GPIO 11	AB17	I	Not Using (SMB_ALERT)
GPIO 12	W14	I	External SMI
GPIO 13	AB15	I	LPC PME
GPIO 14~15		I	Not Implemented
GPIO 16	L2	O	PCI TO ISA GNTA#
GPIO 17	L4	O	Non Connect
GPIO 18	A15	O	Non Connect
GPIO 19	D14	O	Non Connect
GPIO 20	C14	O	Non Connect
GPIO 21	L1	O	PCI TO ISA NOGO
GPIO 22	B14	OD	Non Connect
GPIO 23	A14	O	BIOS Locked/Unlocked
*** GPIO 24	V21	O	Power-On Loss Control (Set Low after Power-On)
GPIO 25	W15	O	LAN ENABLE/DISABLE
GPIO 26		O	Non Connect
GPIO 27	AB14	I/O	LAN Enable/Disable Detected
GPIO 28	AA14	I/O	Reserved (for LAN ENABLE/DISABLE)
GPIO 29~31		I/O	Not Implemented

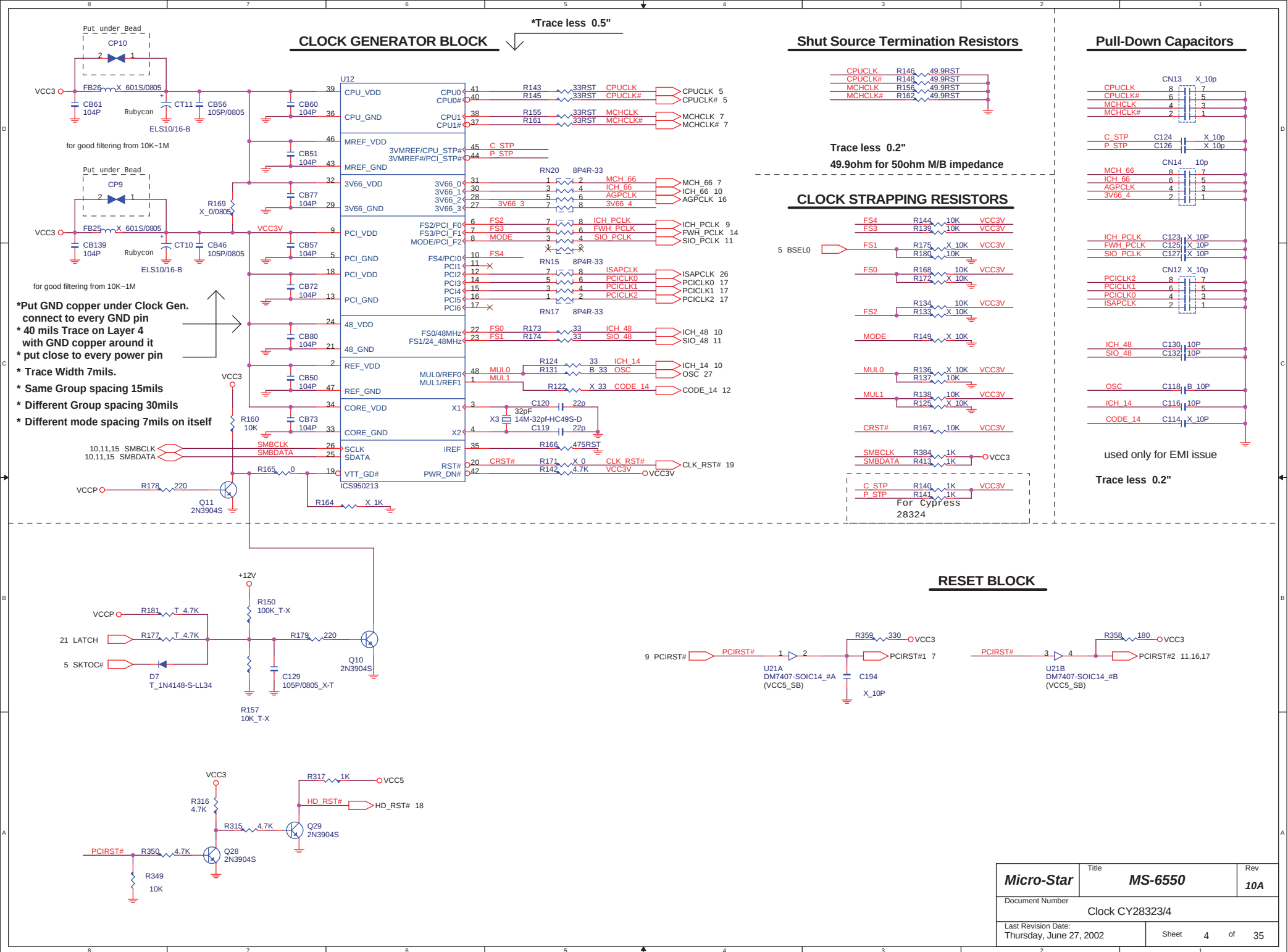
FWH

GPIO Pin	PIN #	Type	Function
GPI 0	6	I	ATA IDE 1 Detect
GPI 1	5	I	ATA IDE 2 Detect
GPI 2	4	I	Not Using
GPI 3	3	I	Not Using

SIO

GPIO Pin	PIN #	Type	Function
GP32	71	I/OD	Non Connect
GP24	89	I/OD	Non Connect
GP34	69	I/OD	Non Connect
GP33	70	I/OD	Non Connect

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
ISA SLOT		AD22



[illegible]

Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

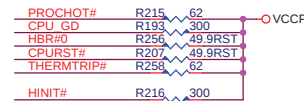
BPM#0 R212 49.9RST

BPM#1 R210 49.9RST

BPM#4 R214 49.9RST

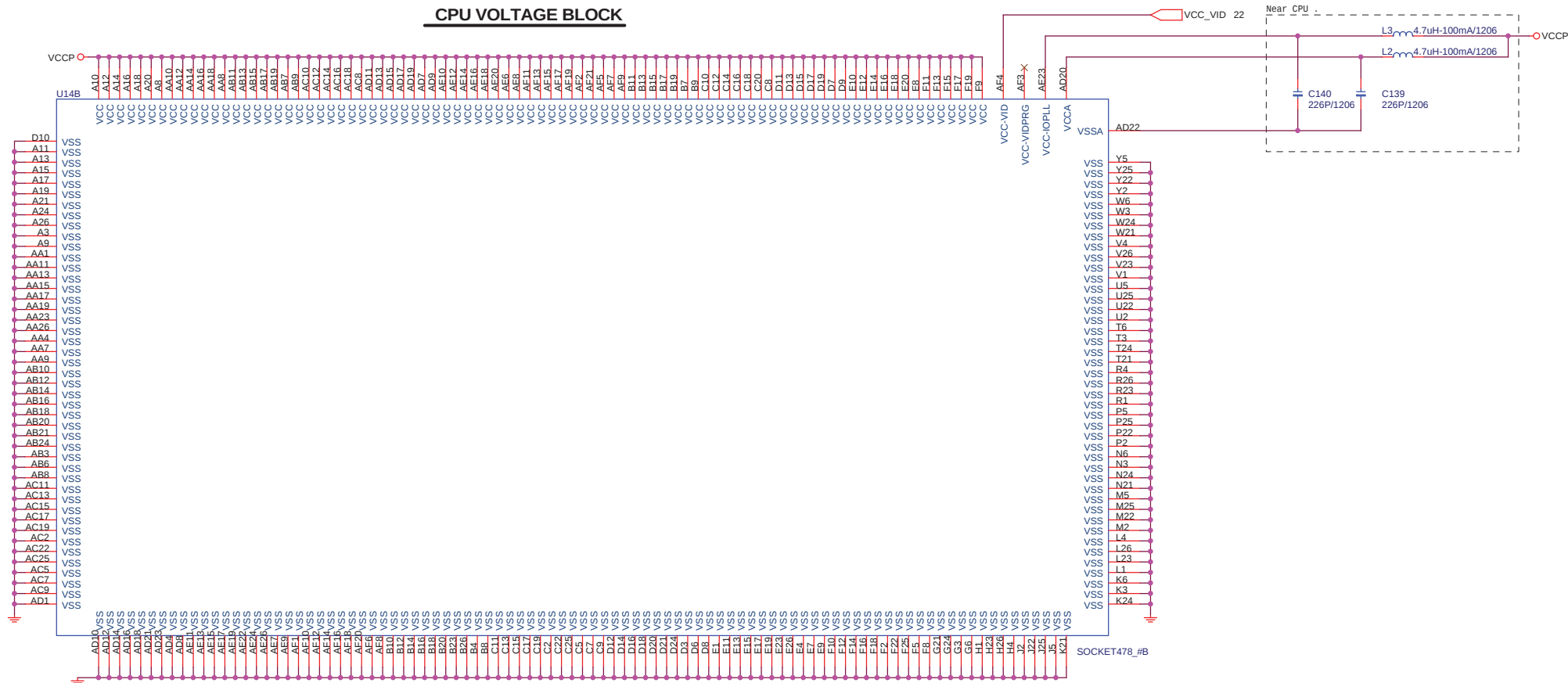
BPM#5 R208 49.9RST

VCCP

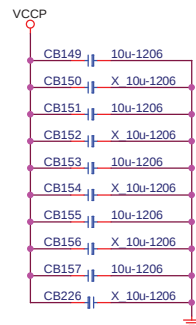


<i>Micro-Star</i>	Title	Rev
	<i>MS-6550</i>	<i>10A</i>
Document Number		
INTEL mPGA478-B CPU1		
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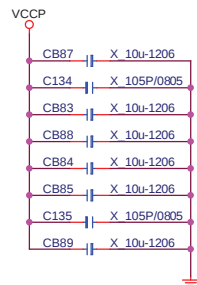
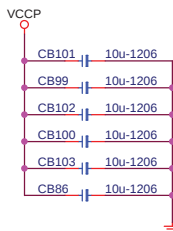
CPU VOLTAGE BLOCK



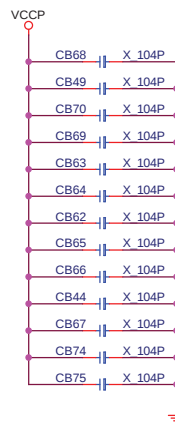
PLACE CAPS WITHIN CPU CAVITY



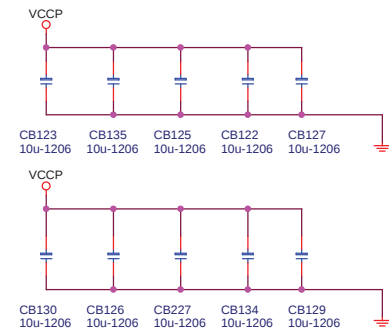
CPU DECOUPLING CAPACITOR



CPU DECOUPLING CAPACITOR

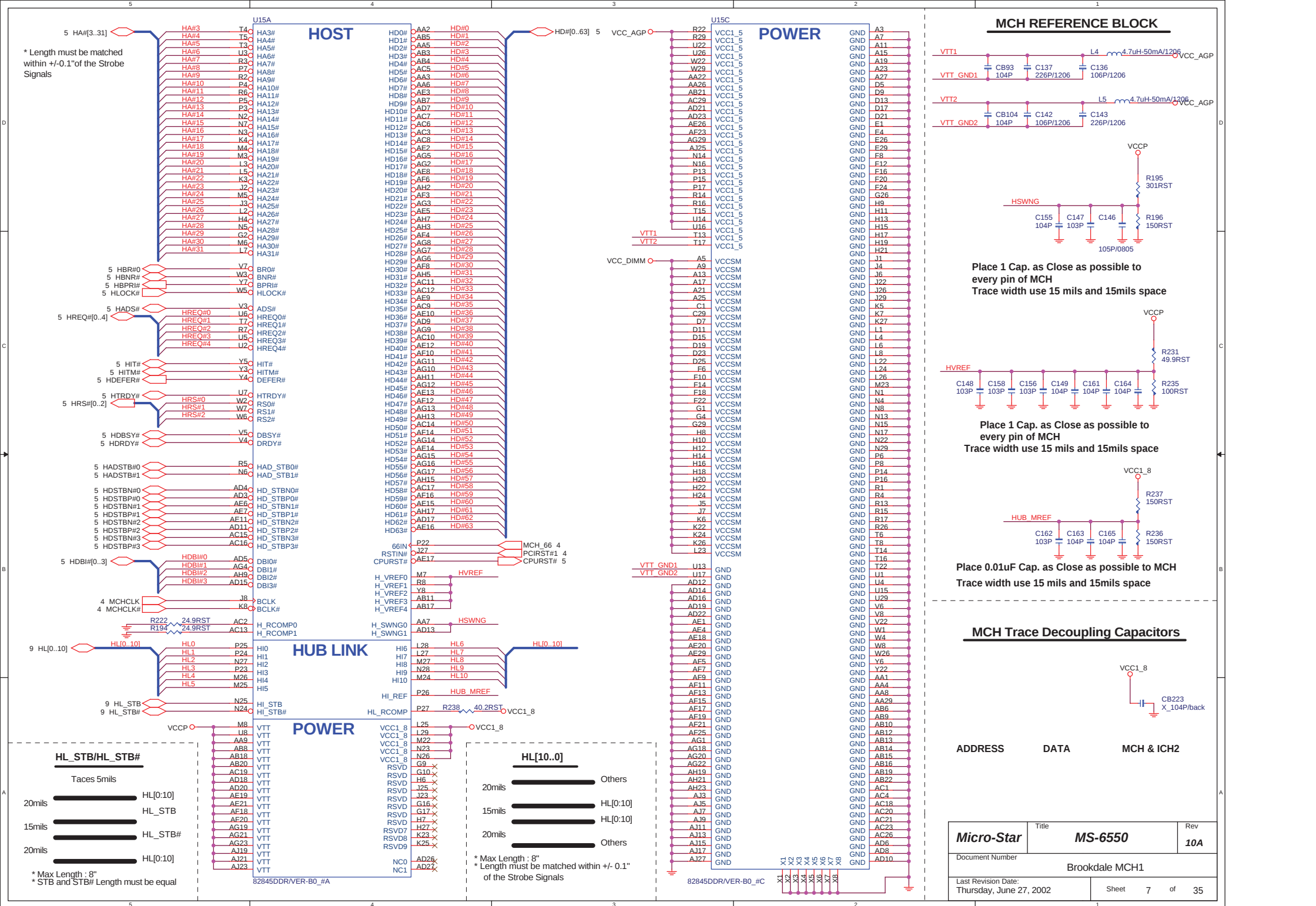


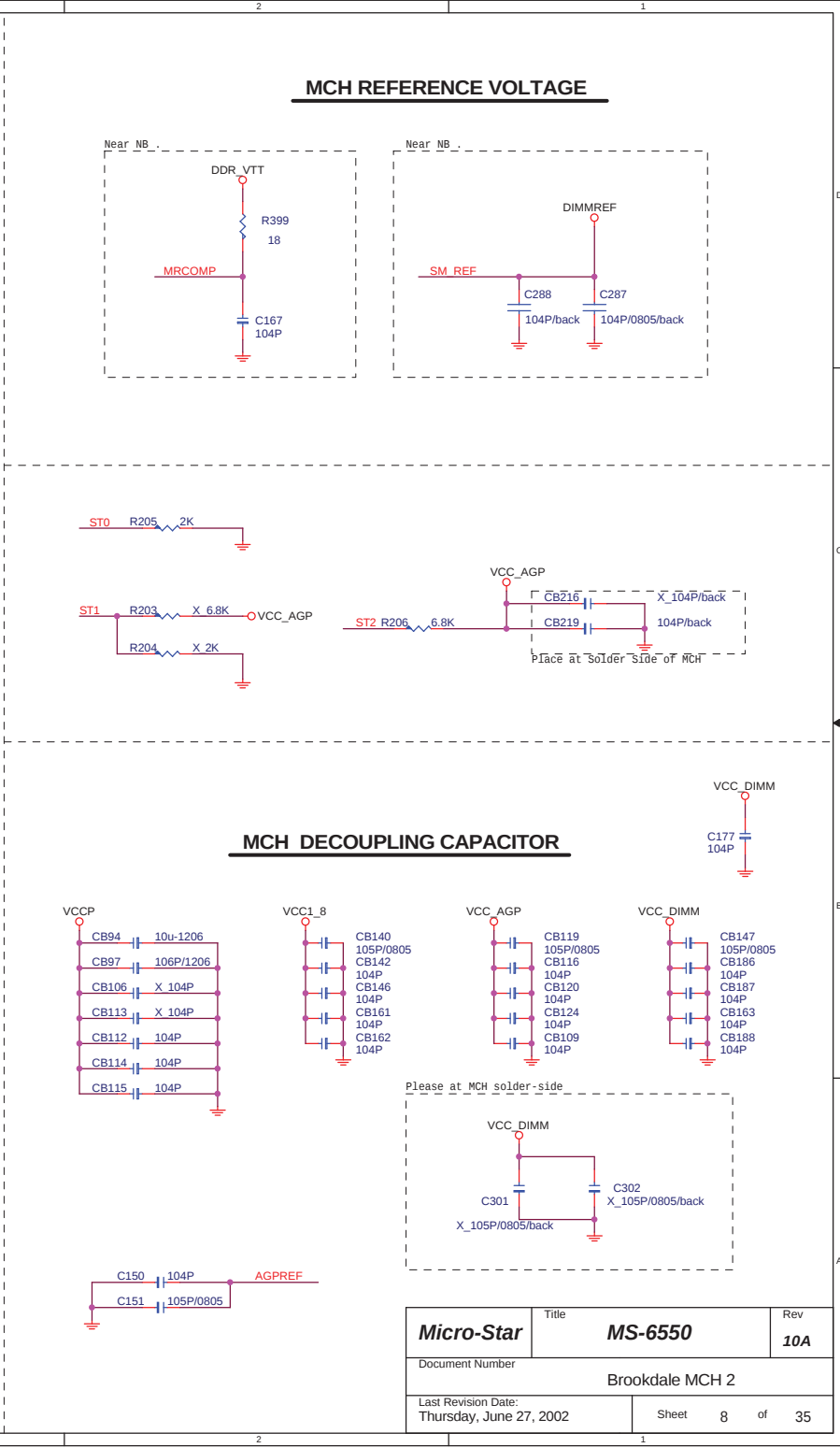
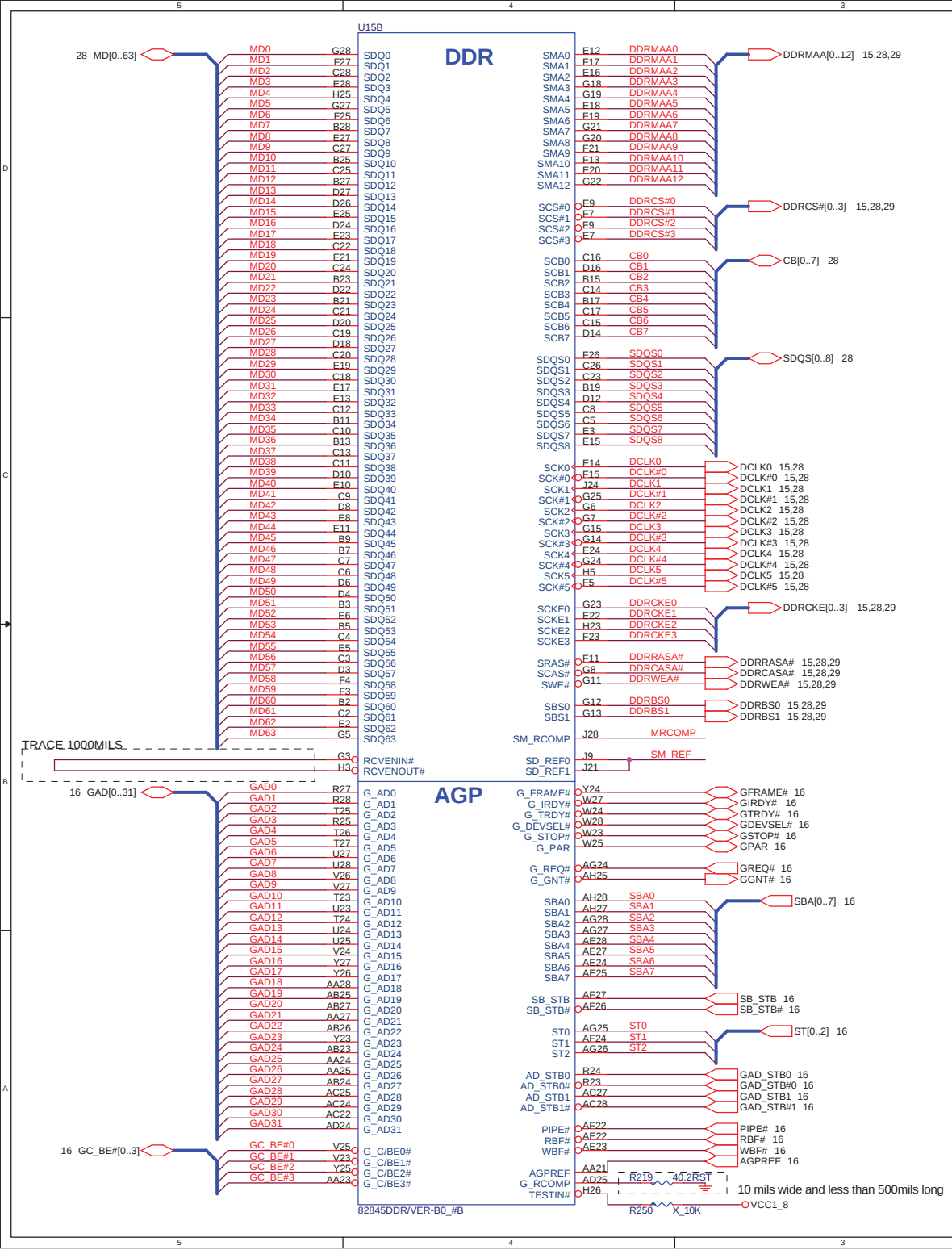
CPU DECOUPLING CAPACITORS UNDER SOCKET-478



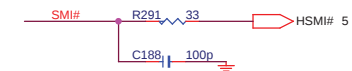
PLACE CAPS WITHIN CPU CAVITY SOLDER

Micro-Star	Title	MS-6550	Rev	10A
Document Number				
INTEL mPGA478-B CPU2				
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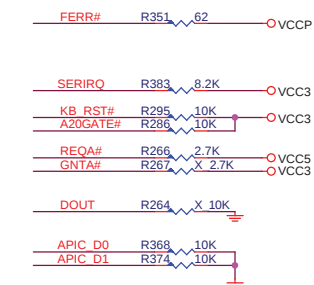




ICH2 SMI# SIGNAL



FERR# R351 62 VCCP

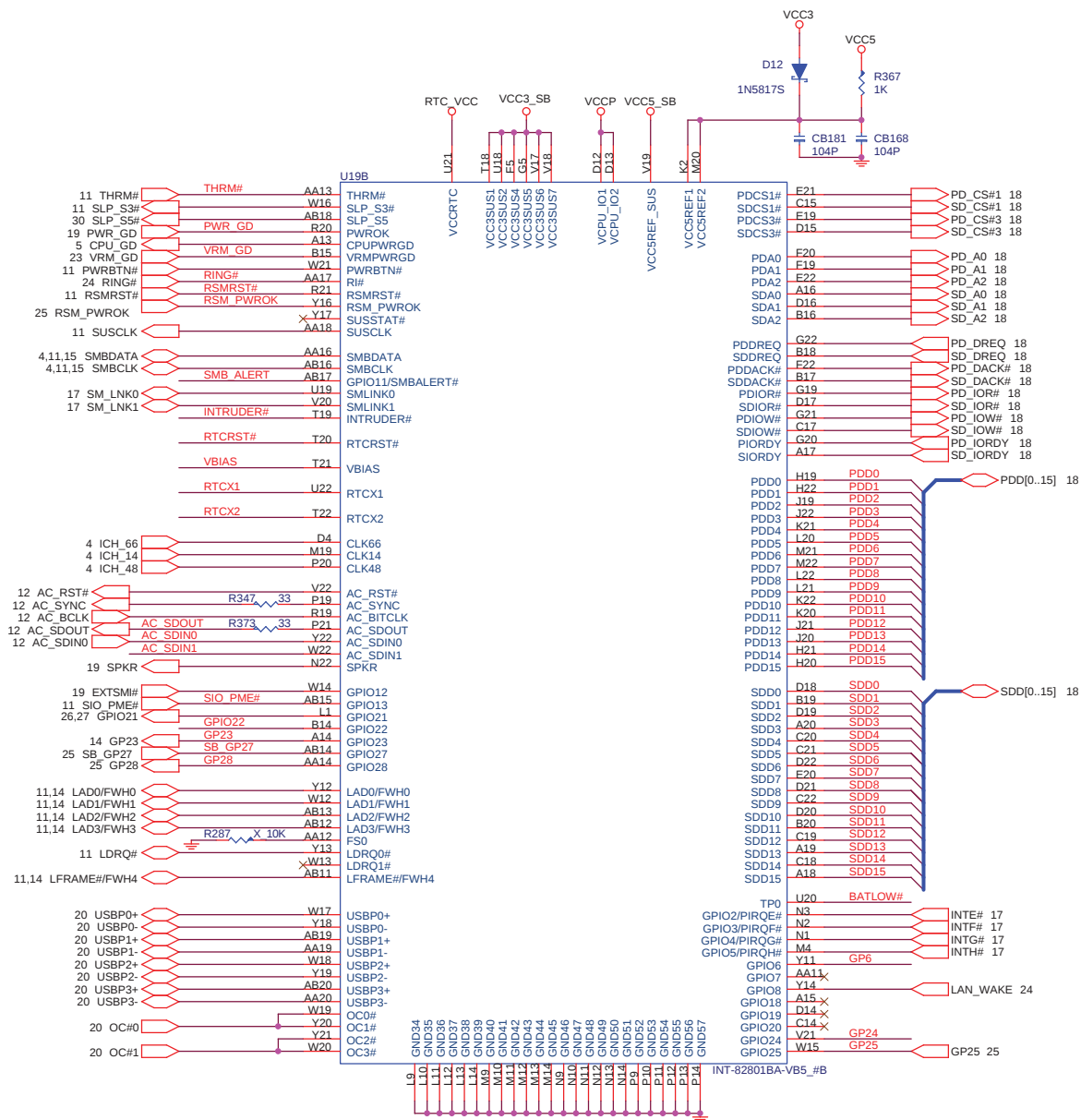


Micro-Star	Title	MS-6550	Rev	10A
Document Number				
Brookdale ICH2 PCI				
Last Revision Date: Thursday, June 27, 2002		Sheet	9	of 35

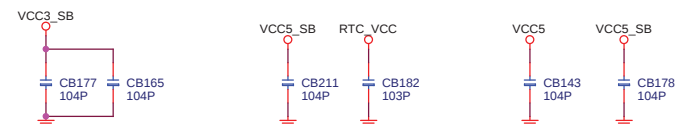
Distribute near the 1.8V power pin of the ICH2

Distribute near the VCC1_8SB
Power pin of the ICH2

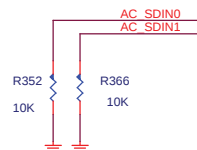
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS



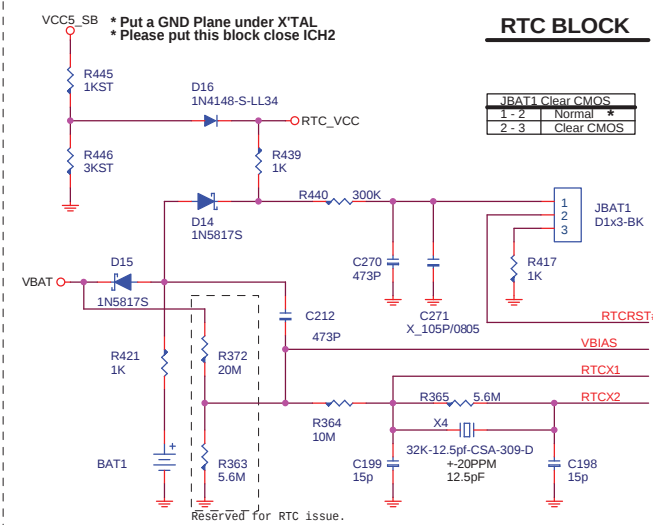
ICH2 DECOUPLING CAPACITOR



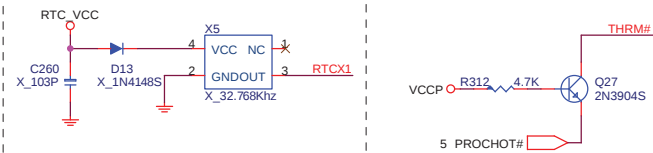
Distribute near the VCC3_SB power pin of the ICH



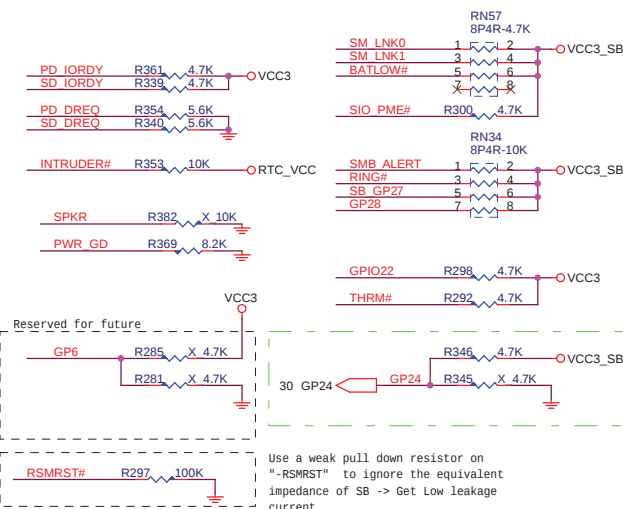
RTC BLOCK



PROCHOT BLOCK

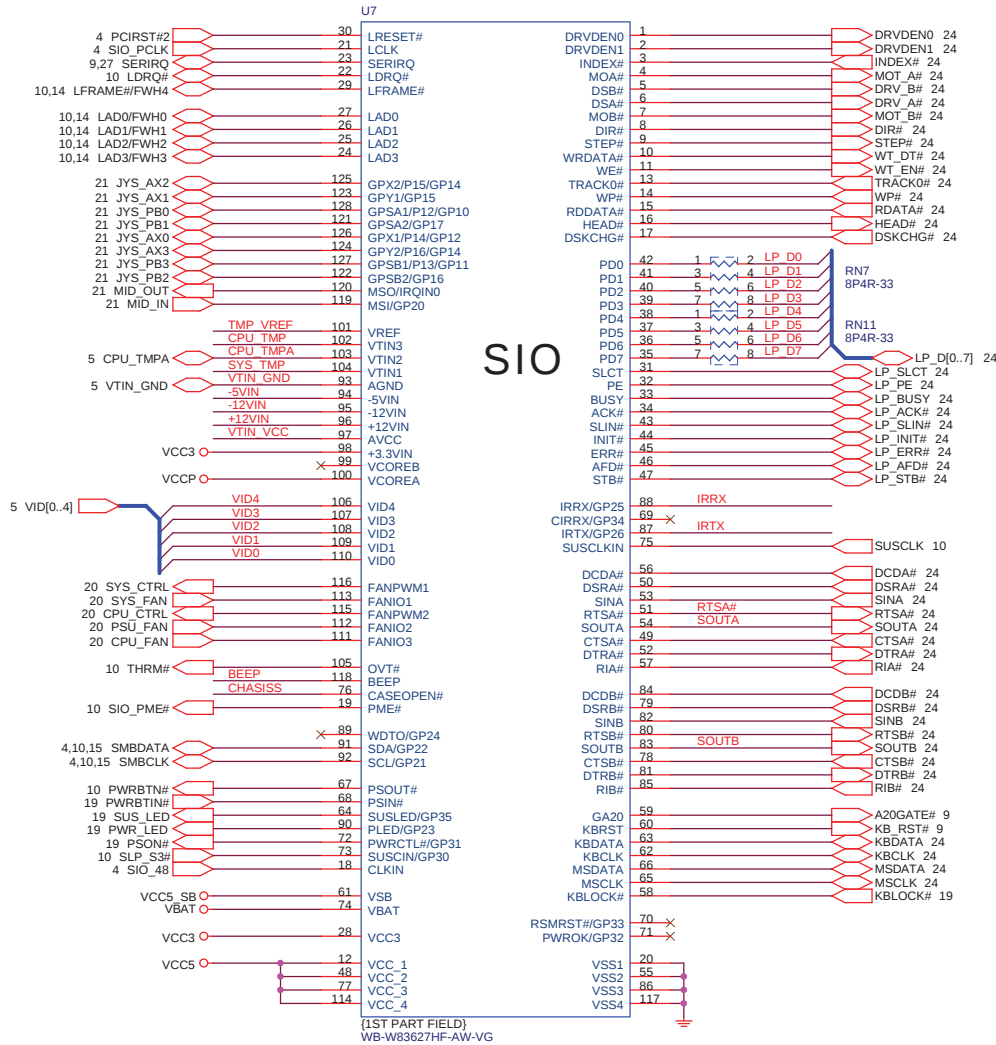


ICH2 STRAPPING RESISTORS



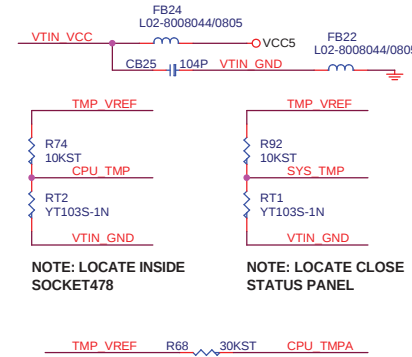
<i>Micro-Star</i>	Title <i>MS-6550</i>	Rev <i>10A</i>
Document Number Brookdale ICH2 Other		
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LPC SUPER I/O W83627HF

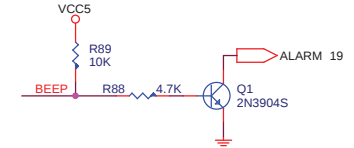


SIO

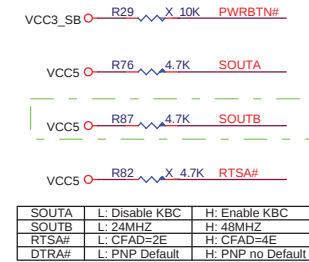
THERMAL RESISTOR BLOCK



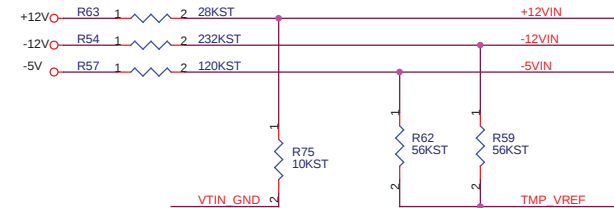
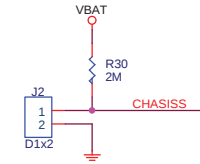
SPEAKER BLOCK



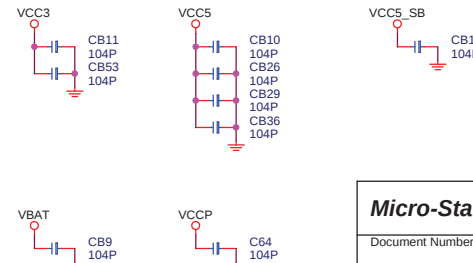
SUPER I/O STRAPPING RESISTOR



CHASSIS INTRUSION HEADER

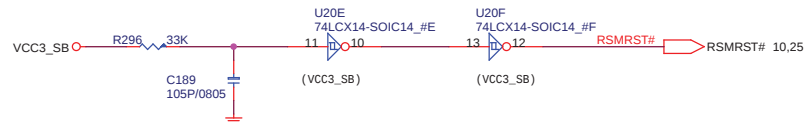


DECOUPLING CAPACITOR

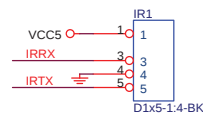


RESUME RESET CIRCUIT BLOCK

Stuff all for D Version bug

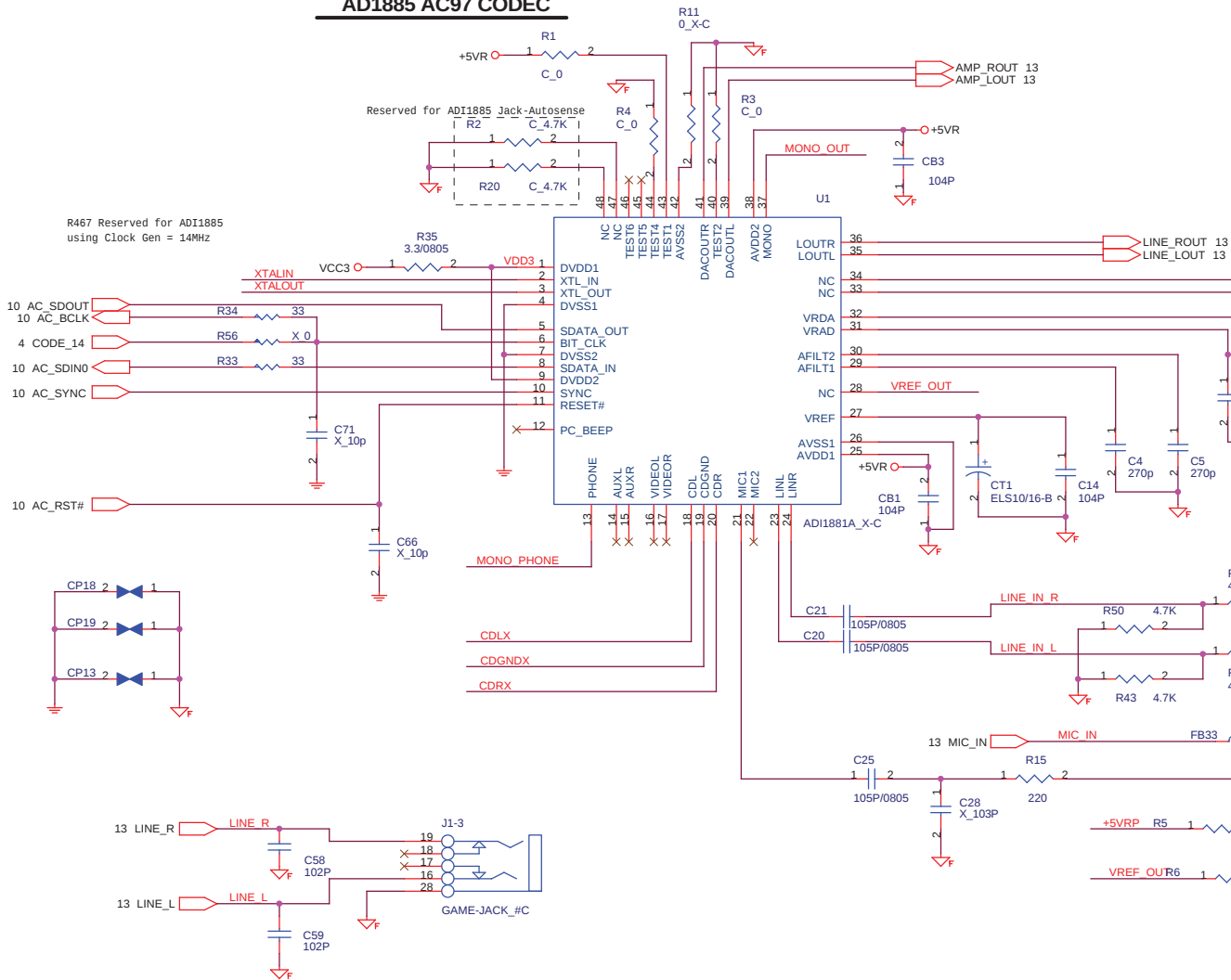


IR HEADER

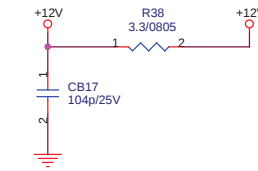


Micro-Star	Title MS-6550	Rev 10A
Document Number	LPC I/O W83627HF	
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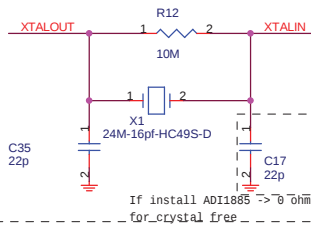
AD1885 AC97 CODEC



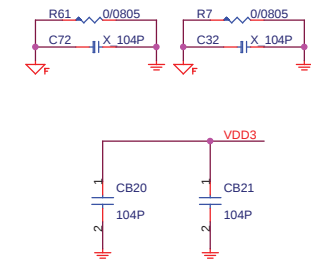
AUDIO CODE REGULATORS



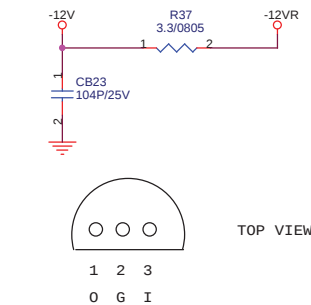
AUDIO CODE CRYSTAL CIRCUIT



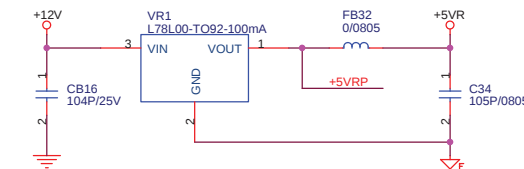
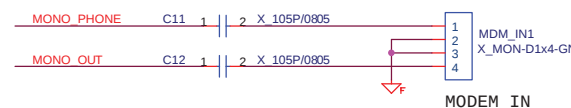
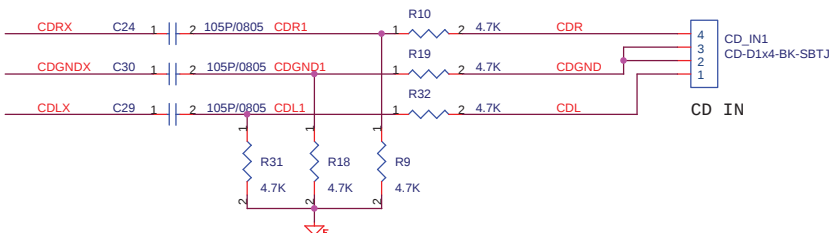
DECOUPLING CAPACITOR



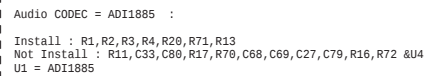
AUDIO CODE REGULATORS



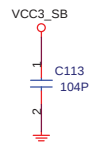
AUDIO CODE CD / AUX / MODEM IN HEADERS



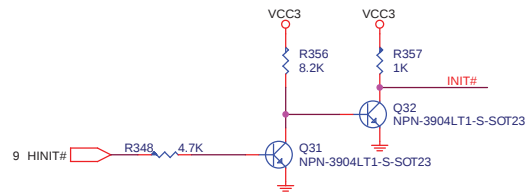
Micro-Star	Title MS-6550	Rev 10A
Document Number	AC97 CODEC	
Last Revision Date: Thursday, June 27, 2002	Sheet	12 of 35



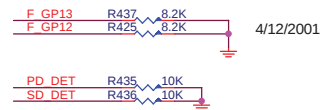
<i>Micro-Star</i>	Title	<i>MS-6550</i>	Rev	<i>10A</i>
Document Number		Audio Amp TL072		
Last Revision Date: Thursday, June 27, 2002		Sheet	13	of 35



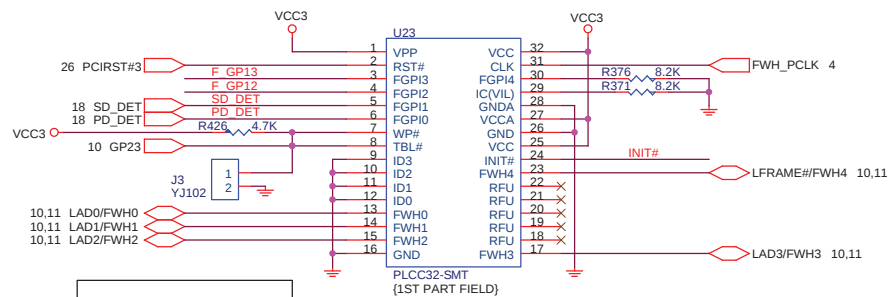
FWH INIT Signal Voltage Translation Block



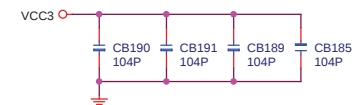
FWH RESISTORS



Firware Hub (FWH)



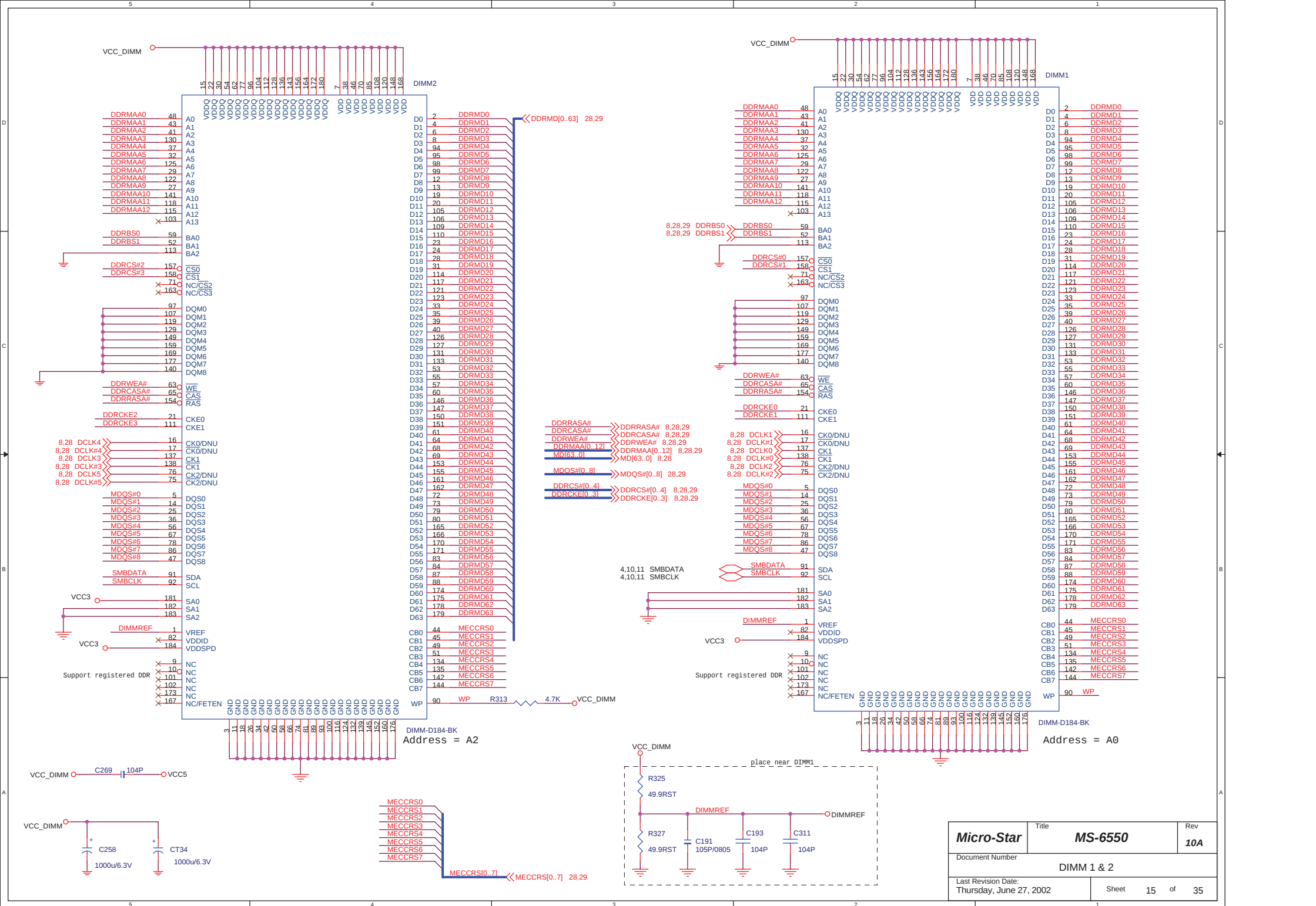
FWH DECOUPLING CAPACITORS



J3 BIOS Update	
SHORT	Locked
OPEN	Unlocked

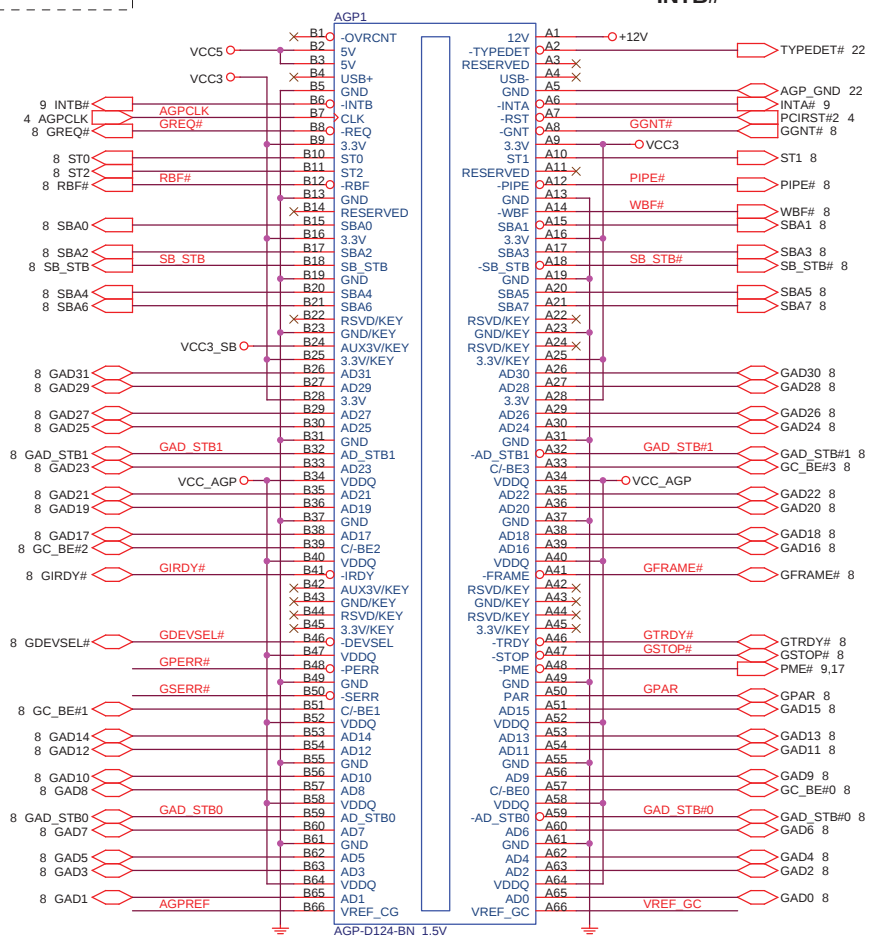
*

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VCC5 = 60mils trace / 15 mils space

AGP Slot Imax
VCC AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A



SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

VCC_AGP

R245
1KST

AGPREF: 10uA

AGPREF

AGPREF 8

R252
1KST

C168
105P/0805

CB144
104P

C166
X 104P

VREF GC

Trace width : 25 mils
C157 should be placed near MCH within 150 mils

NEAR AGP SLOT

Signal	Pin	Signal	Pin	Signal	Pin
GFRAME#	R220 X 6.8K	PIPE#	R163 X 6.8K	VCC_AGP	
GIRDY#	R218 X 6.8K	RBF#	R158 X 6.8K		
GTRDY#	R221 X 6.8K	WBF#	R170 X 6.8K		
GDEVSEL#	R223 X 6.8K				
GSTOP#	R224 X 6.8K				
GPBAR	R228 6.8K	GAD_STB0	R240 X 6.8K	VCC_AGP	
GPERR#	R227 6.8K	GAD_STB1	R198 X 6.8K		
GSERR#	R232 6.8K	SB_STB	R187 X 6.8K		
		GAD_STB#1	R199 X 6.8K		
GREQ#	R152 X 6.8K	GAD_STB#0	R242 X 6.8K		
GGNT#	R147 6.8K	SB_STB#	R241 X 6.8K		

LESS 100MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

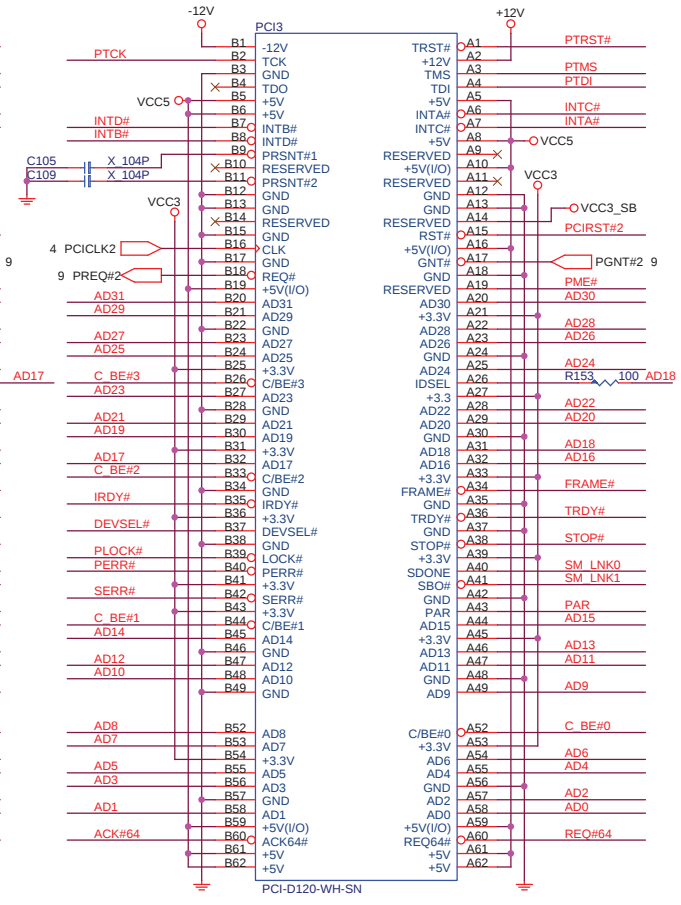
Trace 5mils

Condition	2x / 4x Signals	AGP STB#
15 / 20 mils	~100	~20
30 mils	~100	~20

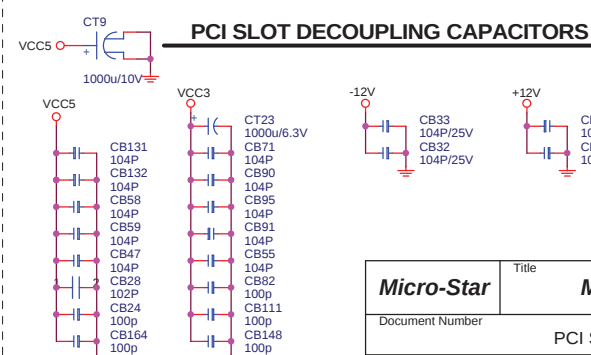
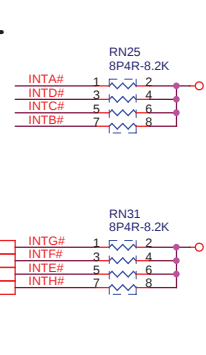
Condition	2x / 4x Signals	AGP STB#
15 / 20 mils	~100	~20
30 mils	~100	~20

Micro-Star	Title	MS-6550	Rev	10A
Document Number		AGP Slot		
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PCI SLOT 3 (PCI VER: 2.2 COMPLY)



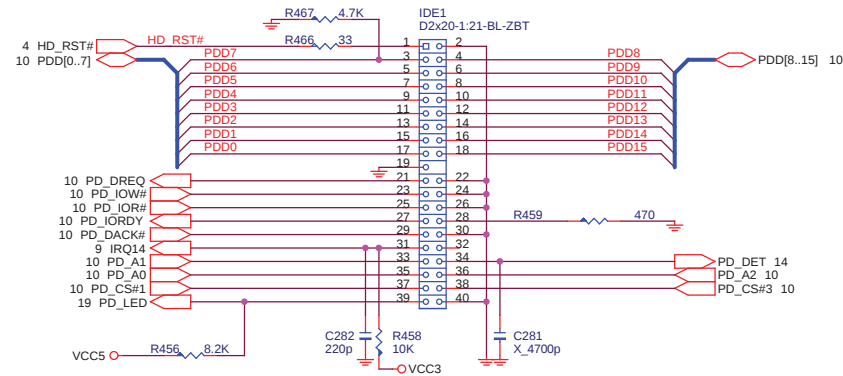
```
IDSEL = AD18
MASTER = PREQ2
INTC#
```



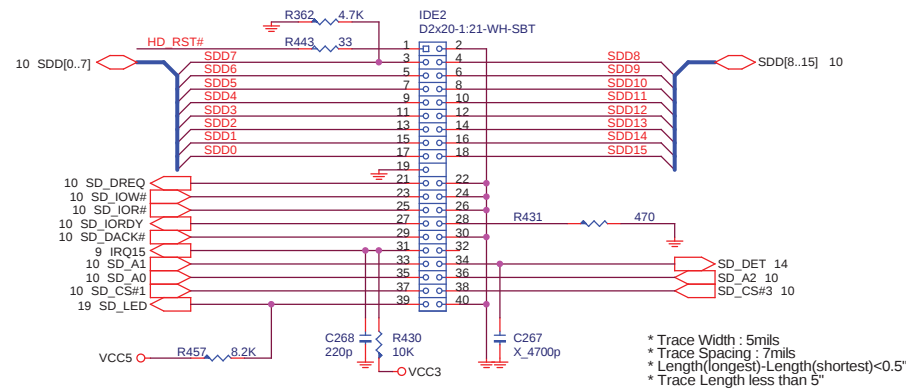
<i>Micro-Star</i>	Title <i>MS-6550</i>	Rev <i>10A</i>
Document Number		
PCI Slot 1 & 2 & 3		
Last Revision Date: Thursday, June 27, 2002		Sheet 17 of 35

ATA100 IDE CONNECTORS

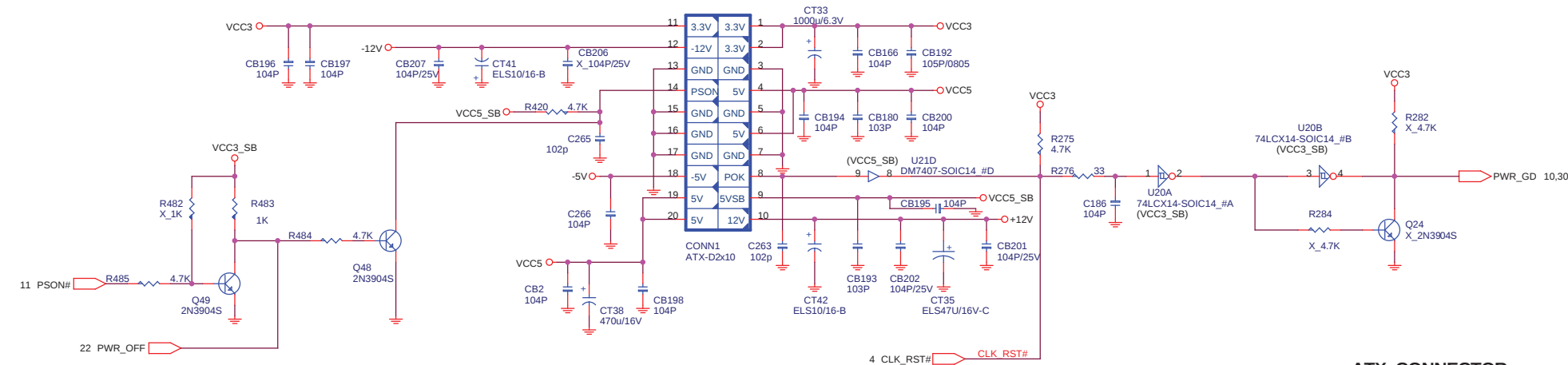
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK

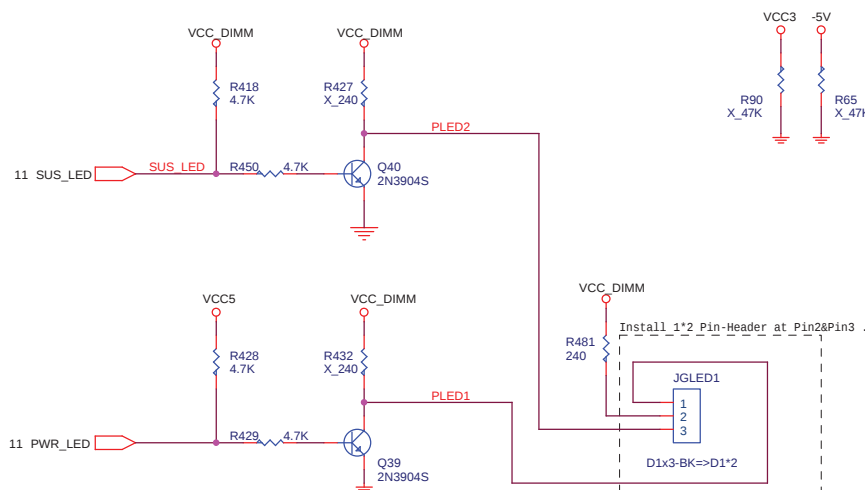
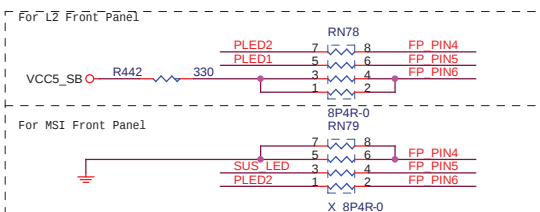
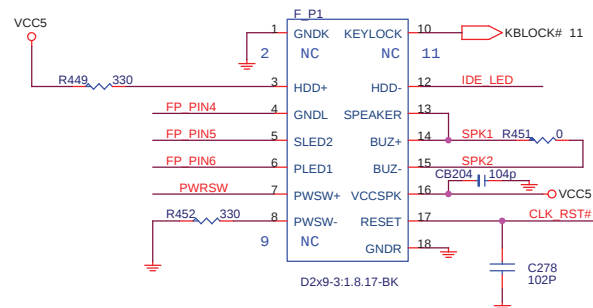


Micro-Star	Title	MS-6550	Rev	10A
	Document Number	ATA100 IDE CONNECTORS		
	Last Revision Date:	Thursday, June 27, 2002	Sheet	18 of 35



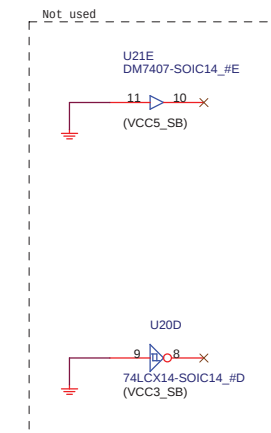
ATX CONNECTOR

Brookdale FRONT PANEL-M

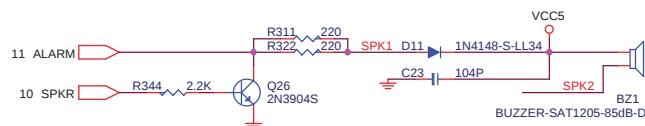


Support MSI => Install R418, R427, =240 ohm , R450=4.7K ohm .
Not install R428, R429, R432, Q39, R481, JGLED1

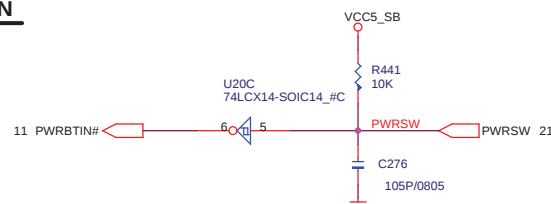
Support L2 => Install R418, R428, R429, R450 =4.7K ohm , R481=240 ohm .
Not install R427, R432



SPEAKER

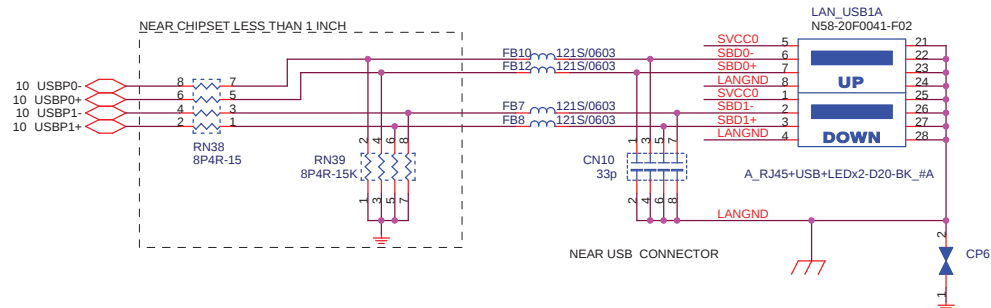


POWER BUTTON

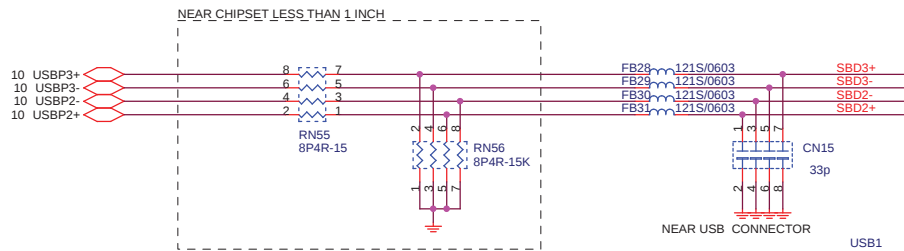


Micro-Star	Title	MS-6550	Rev	10A
	Document Number	Front Panel & Connector		
Last Revision Date:		Thursday, June 27, 2002	Sheet	19 of 35

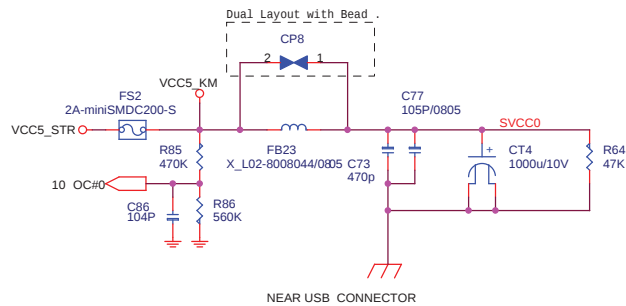
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

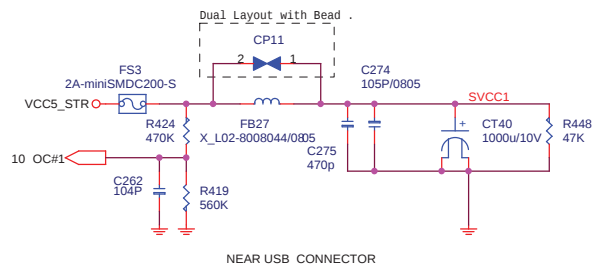


POWER CIRCUIT FOR USB PORT 0,1

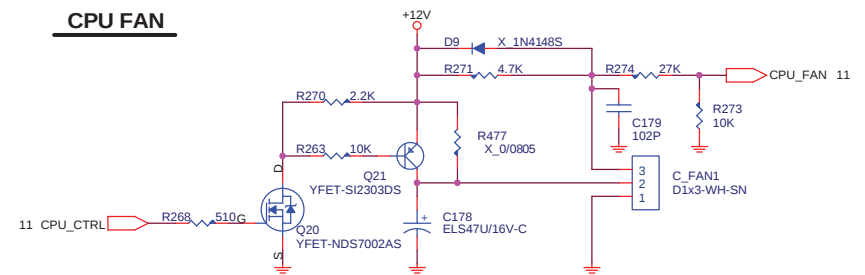


- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signals Trace Spacing : 18 mils
- * USB Power Trace must be 40mils width

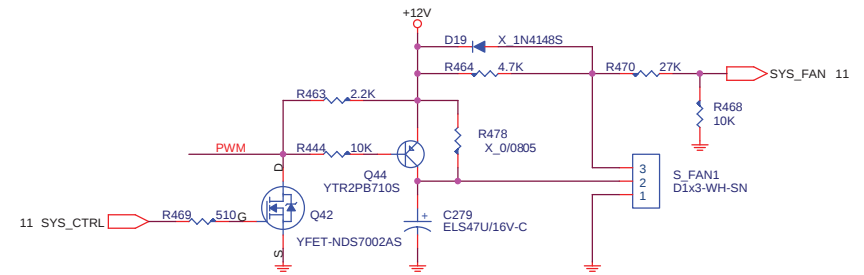
POWER CIRCUIT FOR USB PORT 2, 3



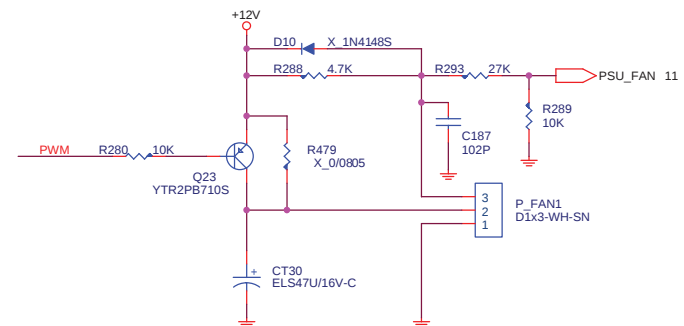
CPU FAN



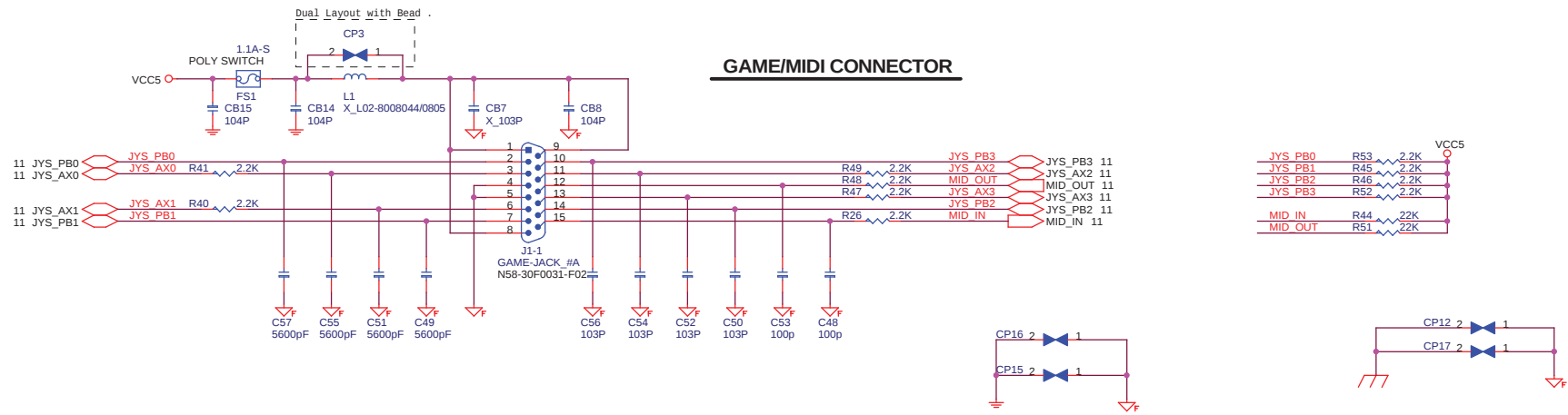
SYSTEM FAN



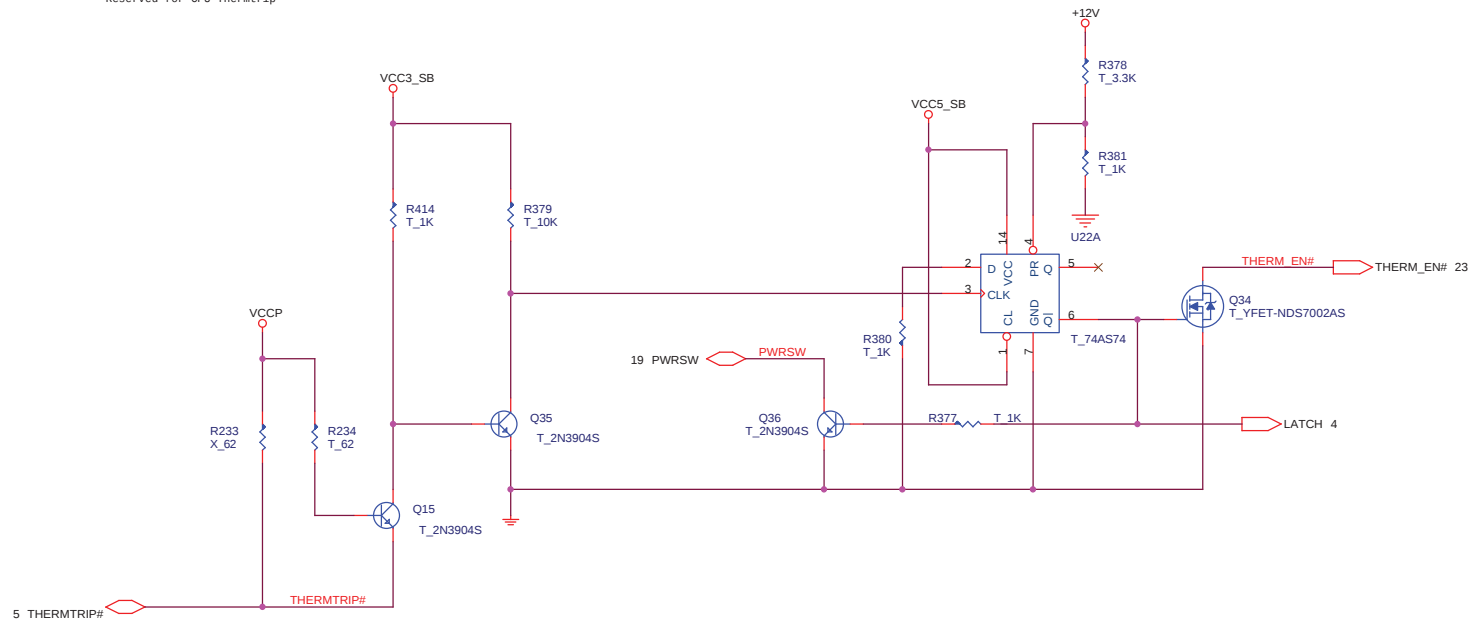
ATX PSU FAN ON/OFF CONTROL



Micro-Star	Title	MS-6550	Rev	10A
Document Number	USB & FAN Connectors			
Last Revision Date:	Thursday, June 27, 2002			Sheet 20 of 35

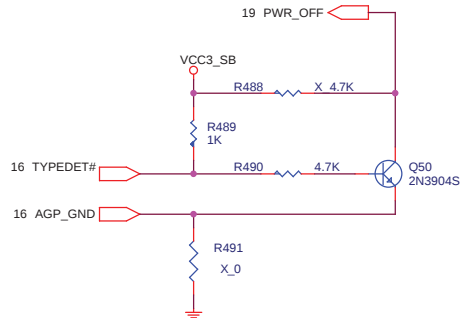


Reserved for CPU Thermtrip



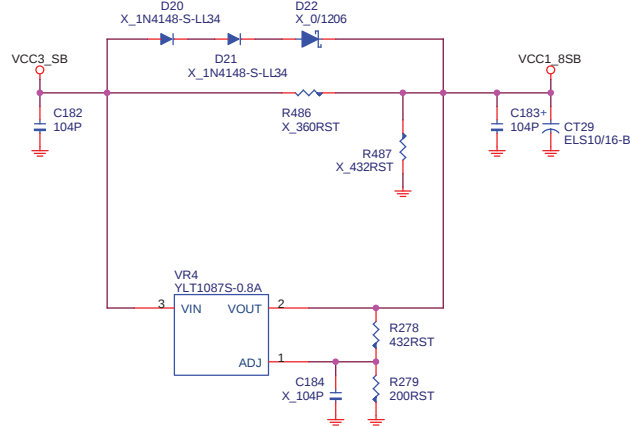
Micro-Star	Title	MS-6550	Rev	10A
	Document Number	GAME PORT		
Last Revision Date: Thursday, June 27, 2002		Sheet	21	of 35

VCC_AGP



1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC AGP	VCC1_8	VCC3 DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1881A	0	0	0	0	0	0	0	0	0
FWH-SST	0	0	0	0	0	0	0	0	0
W83627HF	0	0	0	0	0	0	0	0	0
HIP6301	0	0	0	0	0	0	0	0	0
HIP6602A	0	0	0	0	0	0	0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0	0	0	0
DIMM	0	0	0	NOTE2	0	0	NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0	0	0	0	0	0
USB	0	0	0	0	0	0	0	0	0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0	0	0	0	0	0
OTHER	0	0	0	0	0	0	0	0	0

DIP Cap Dual Layout for 1000uF/6.3V & 220uF/10V

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

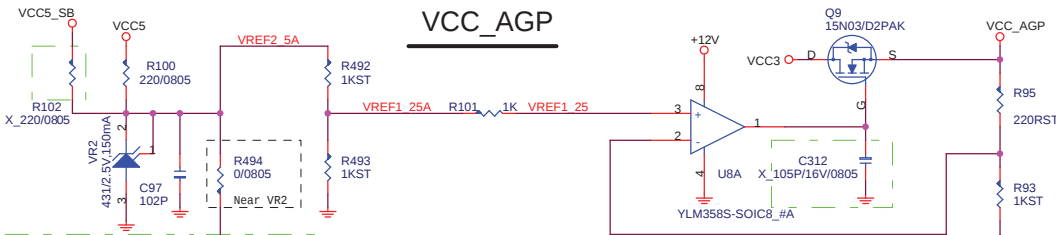
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A --> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA --> VCC3_SB
VCC3_SB --> 600mA * 3.3V/5V = 396mA --> VCC5_SB

Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

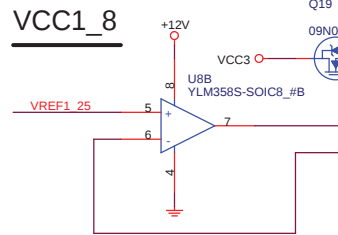
VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB



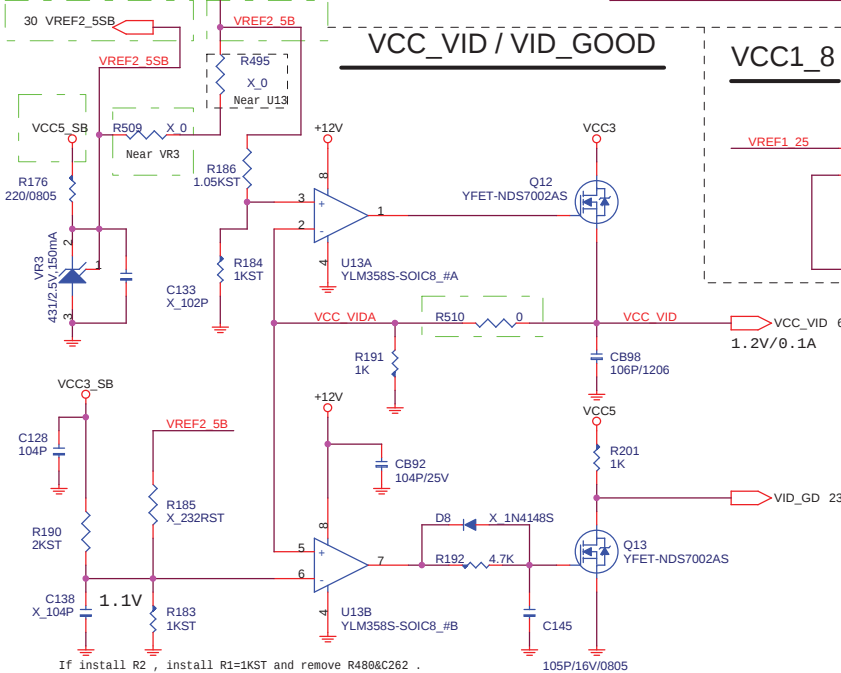
VCC_AGP



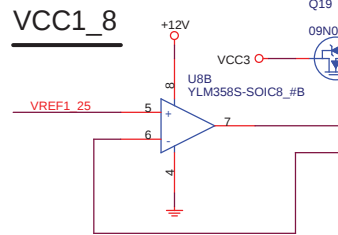
VCC1_8



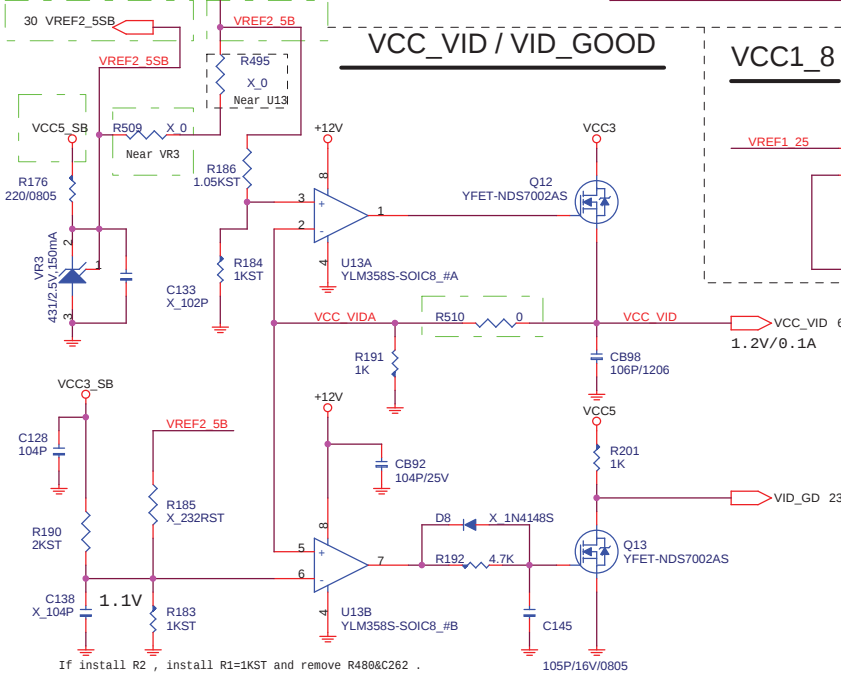
VCC5_SB



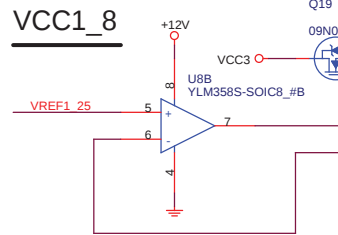
VCC3



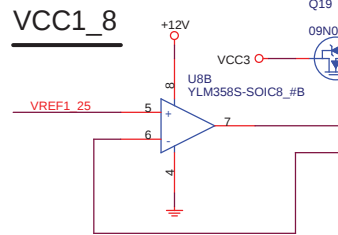
VCC5



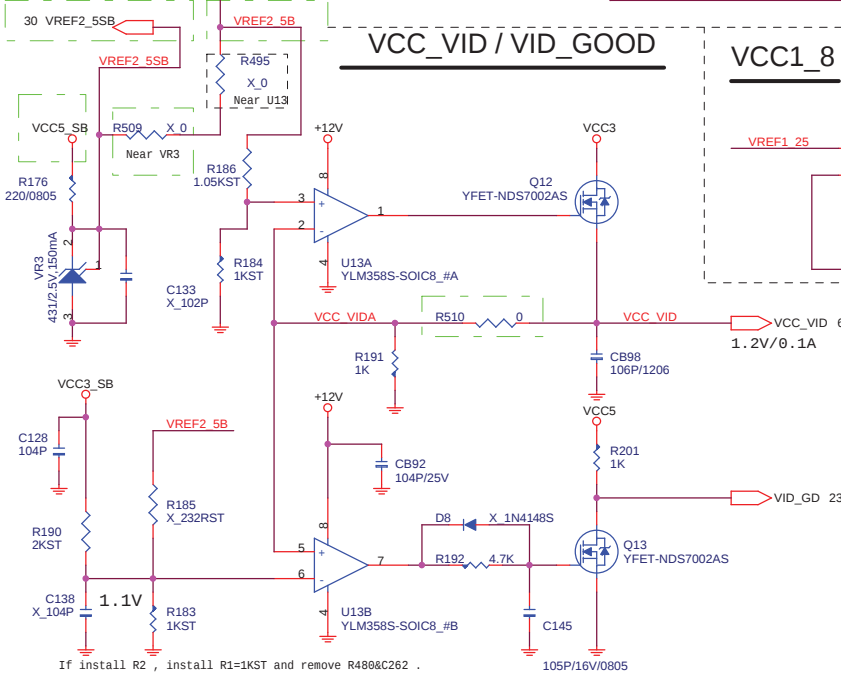
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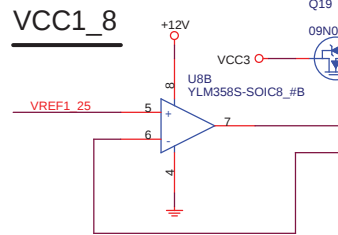
VCC3



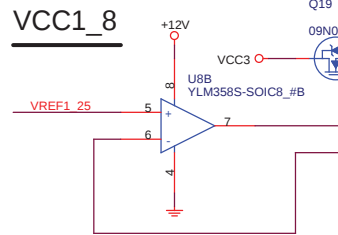
VCC5



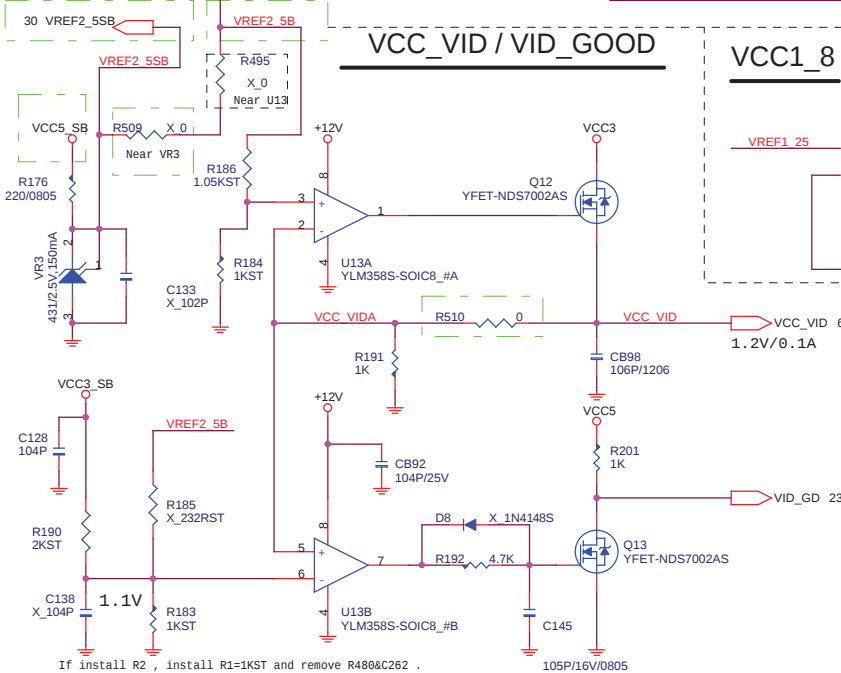
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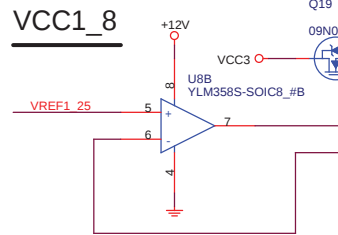
VCC3



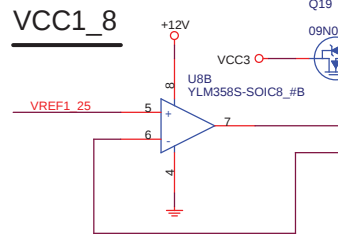
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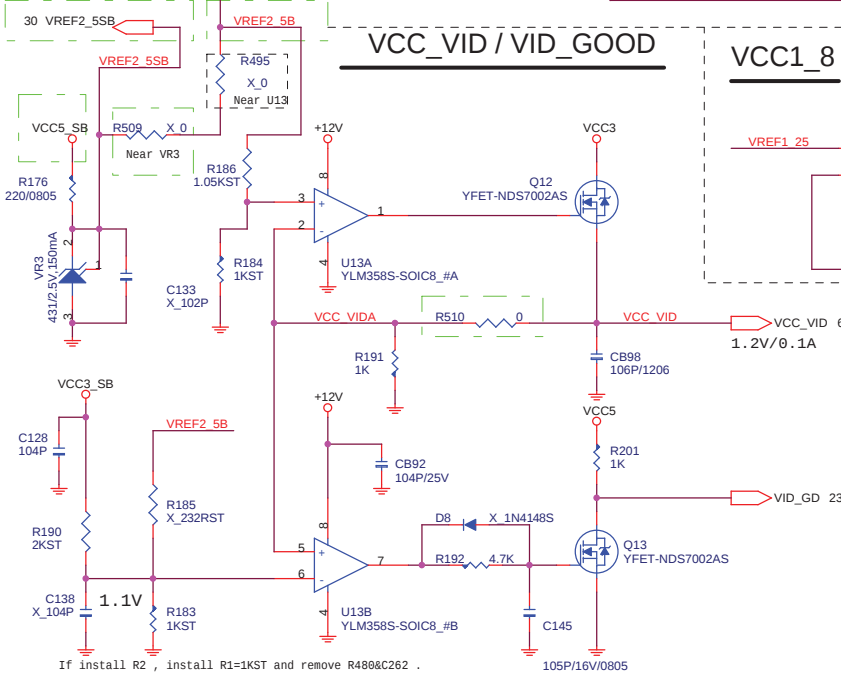
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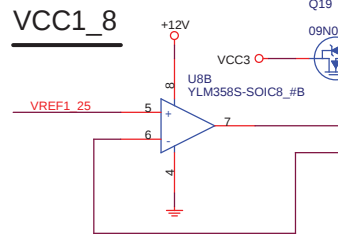
VCC3



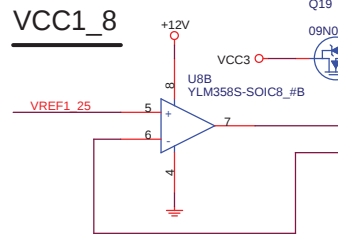
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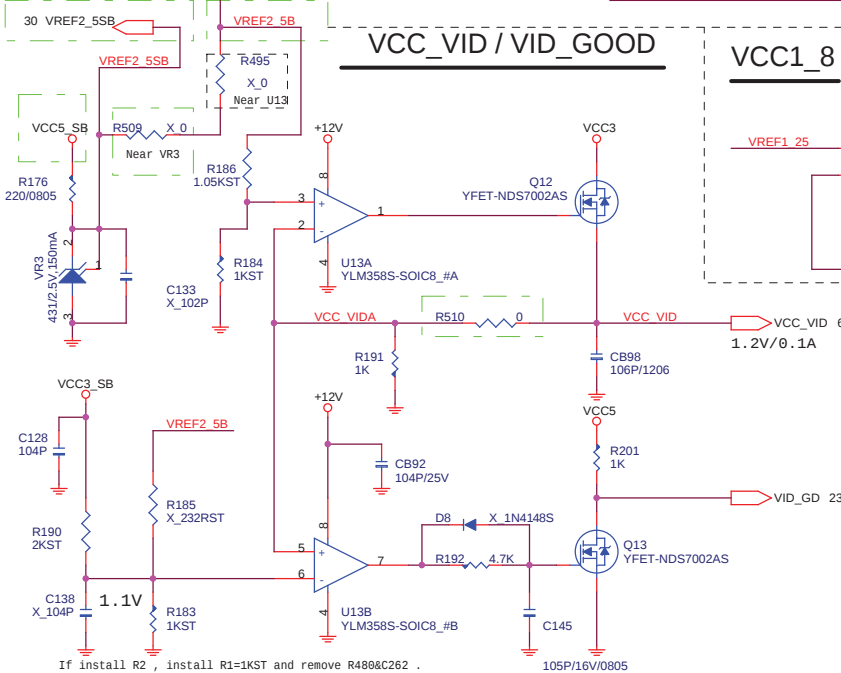
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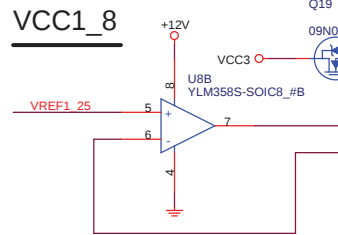
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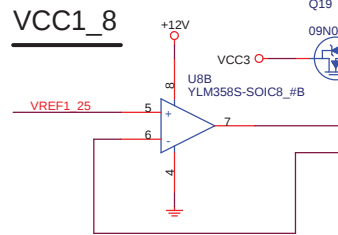
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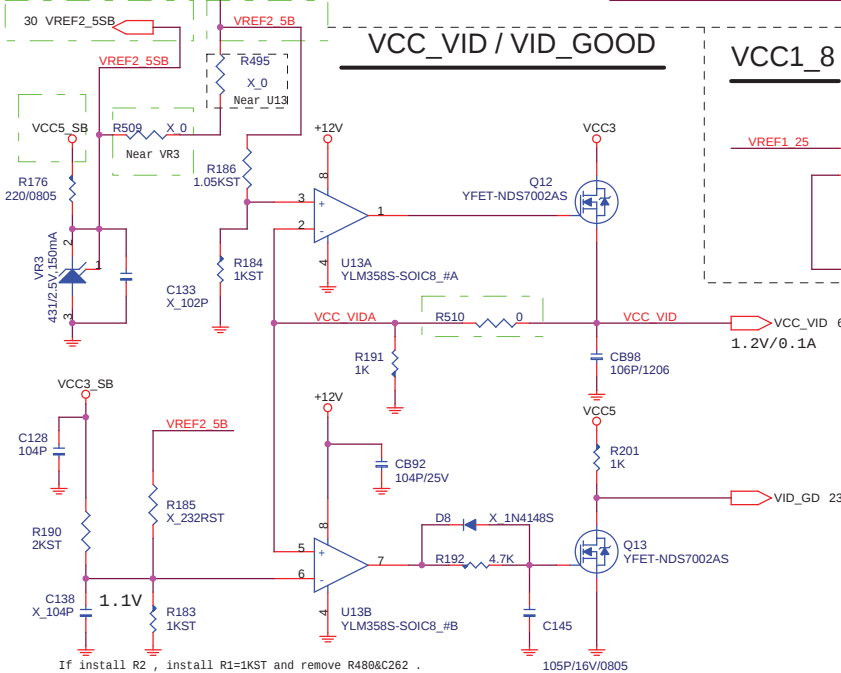
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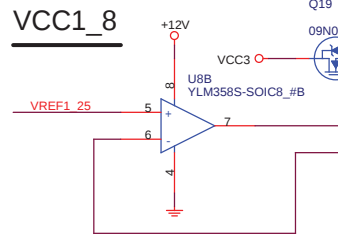
VCC3



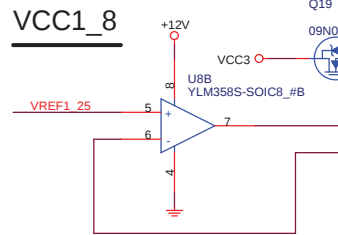
VCC5



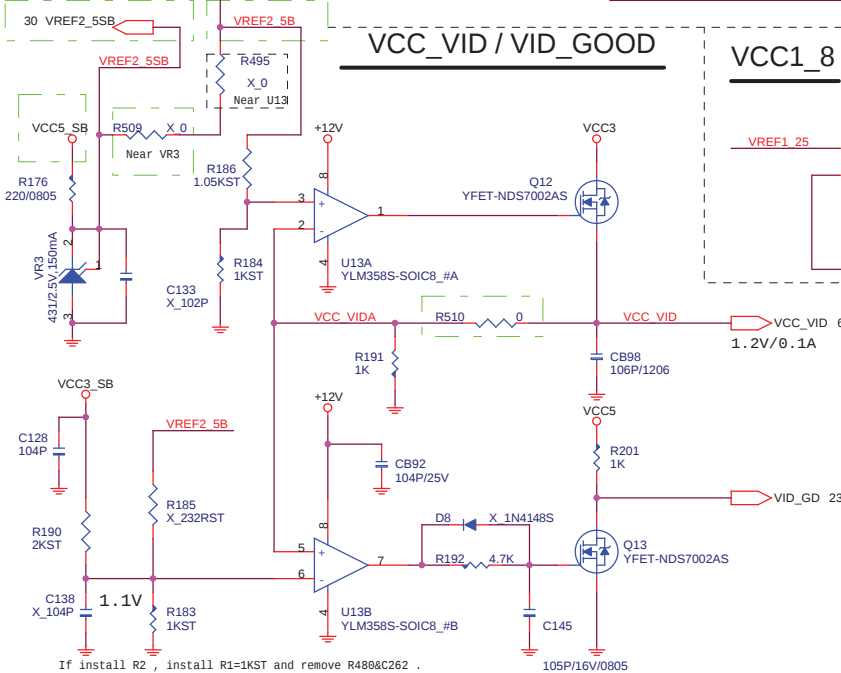
VCC1_8



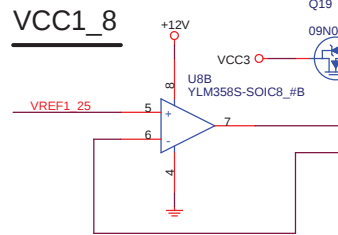
VCC3



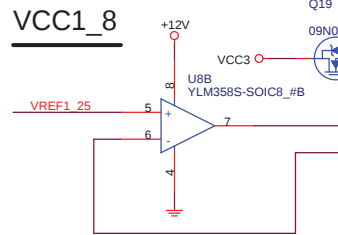
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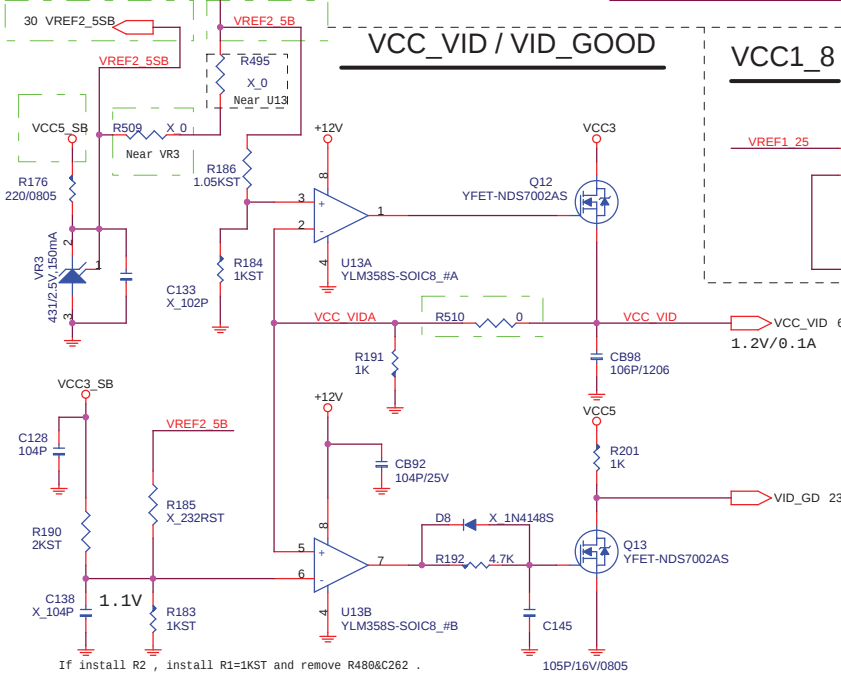
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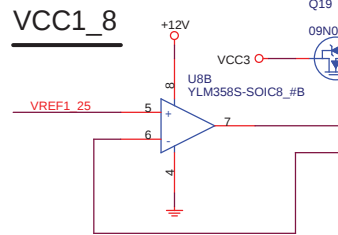
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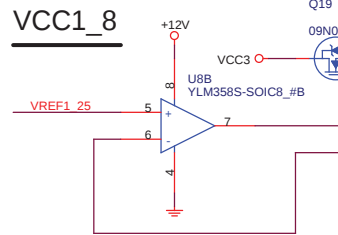
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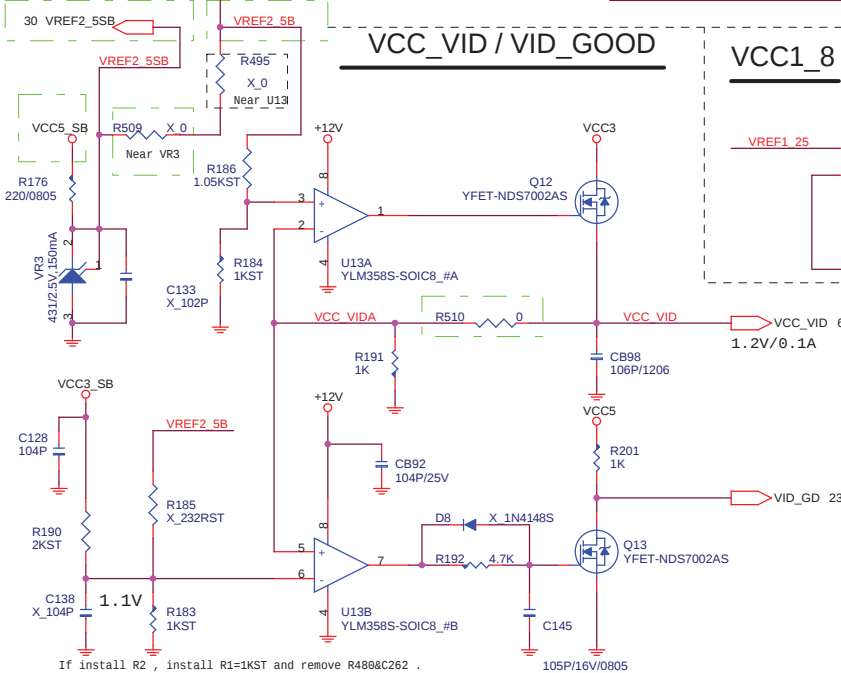
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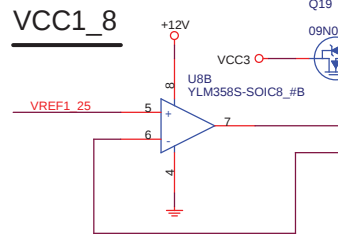
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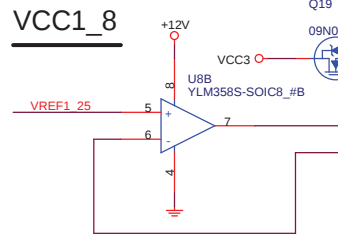
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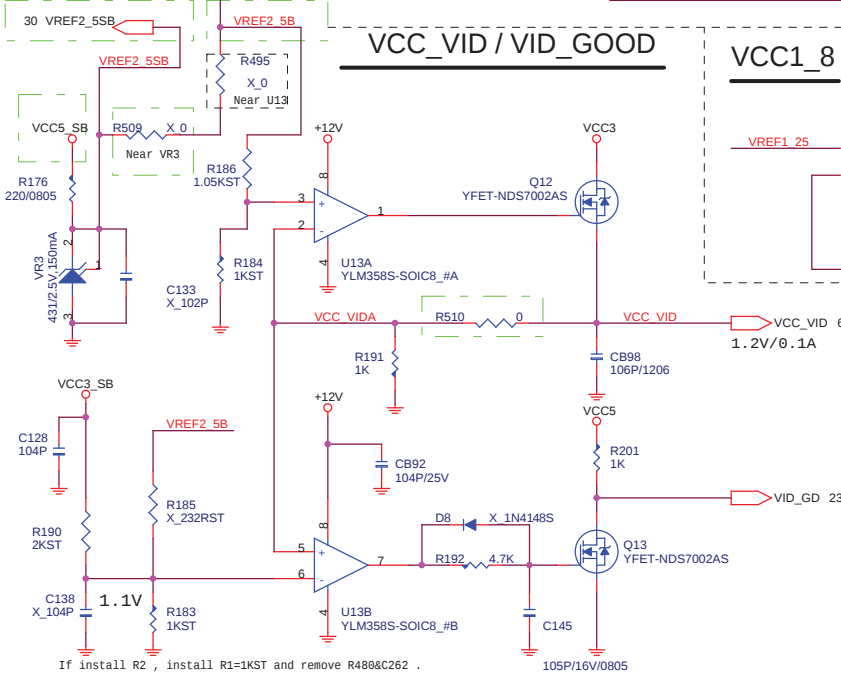
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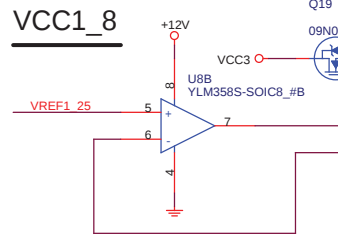
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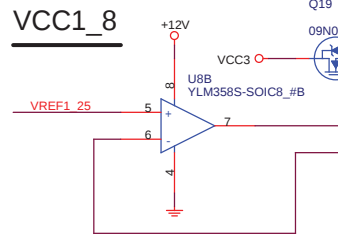
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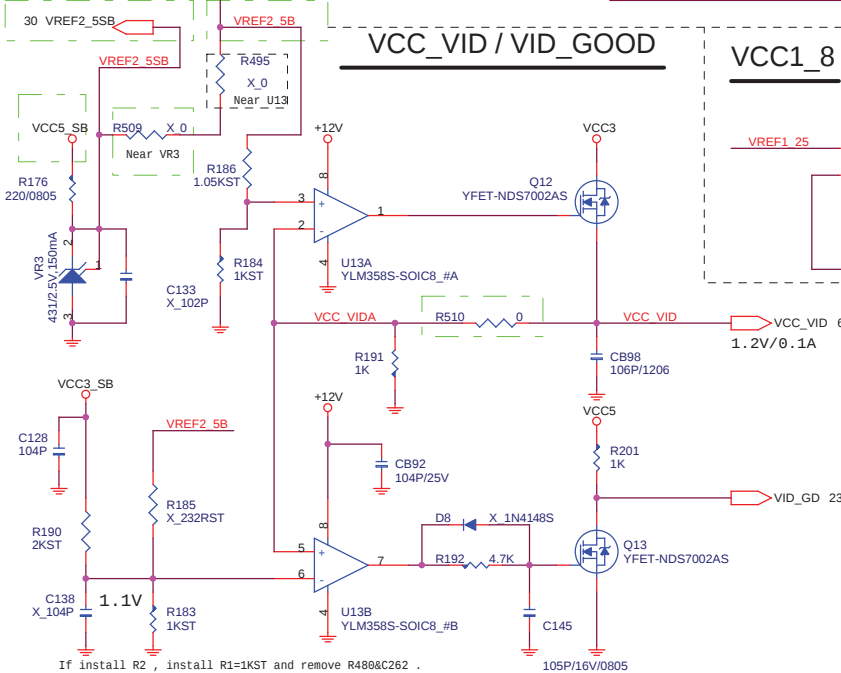
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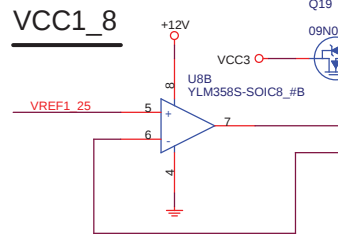
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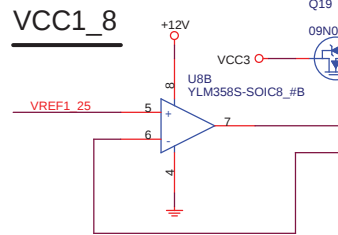
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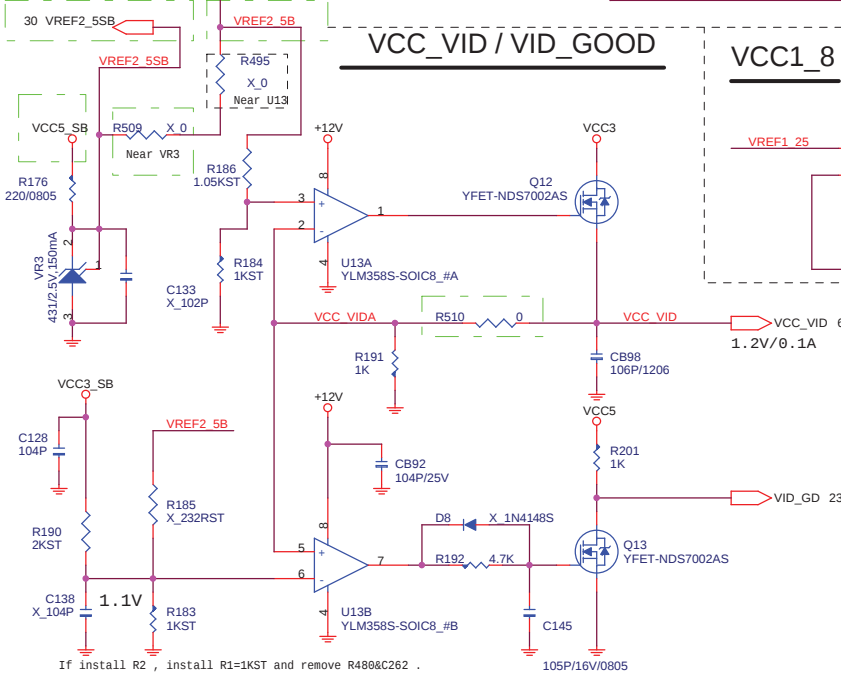
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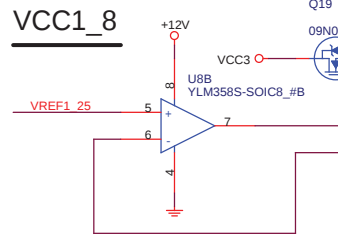
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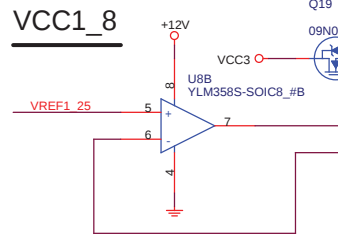
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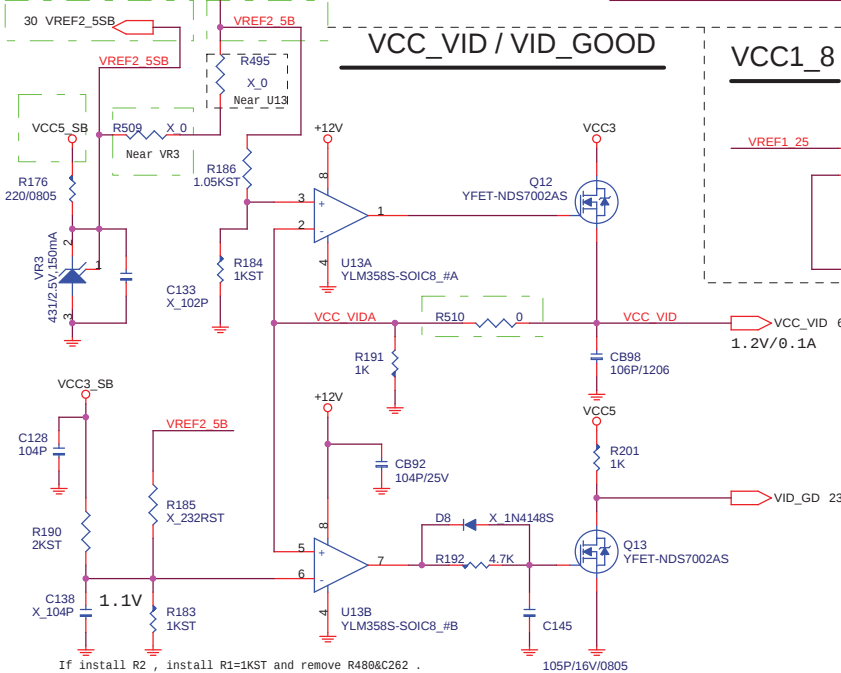
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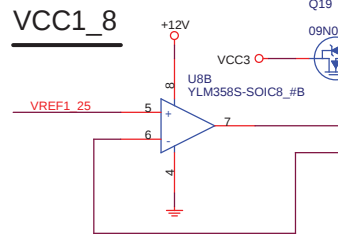
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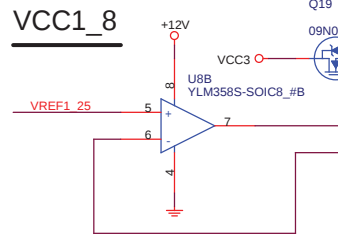
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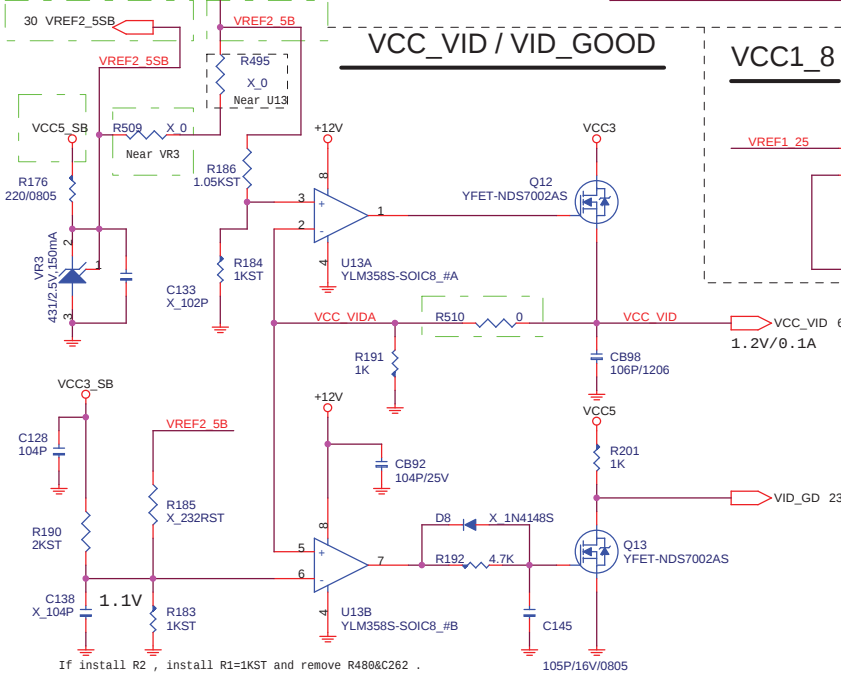
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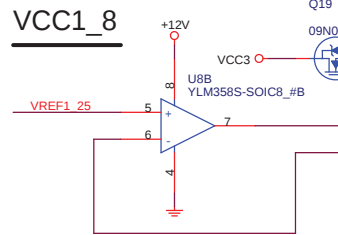
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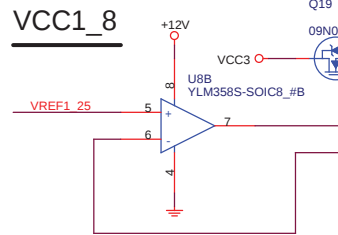
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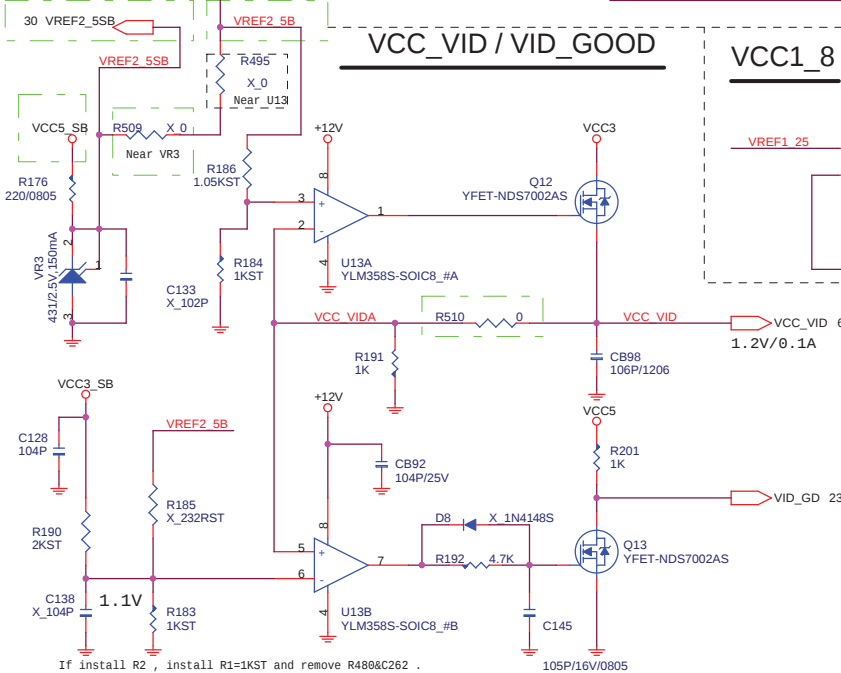
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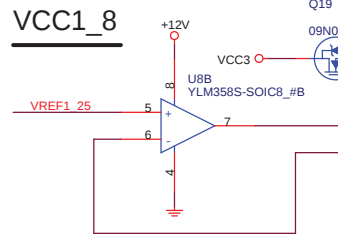
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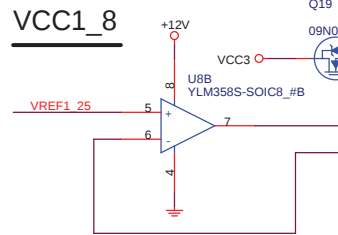
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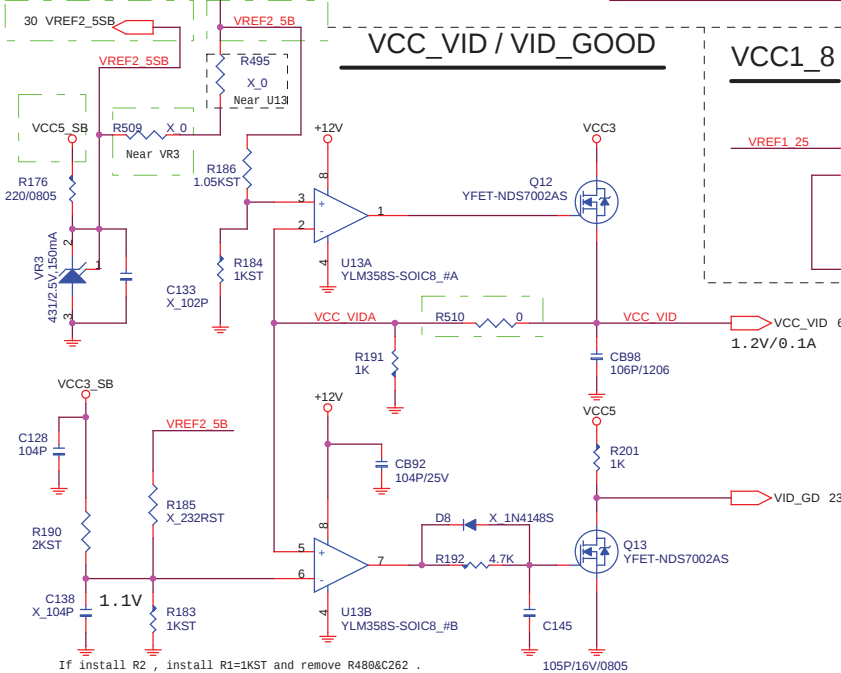
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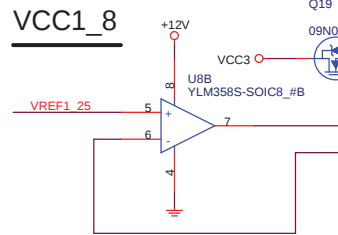
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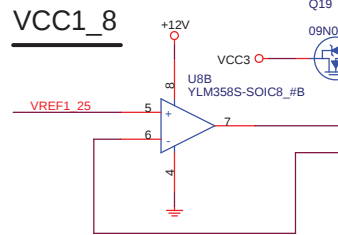
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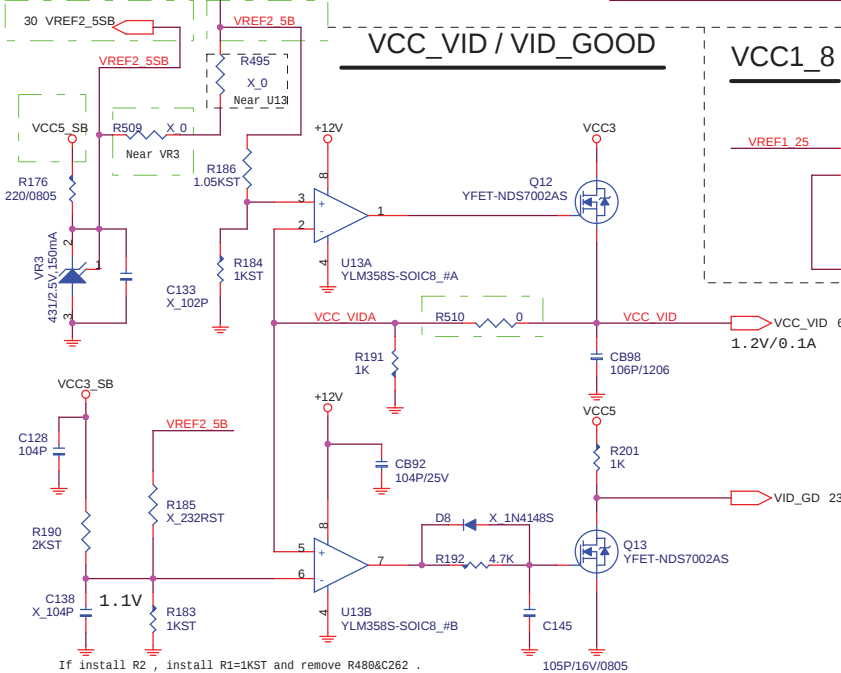
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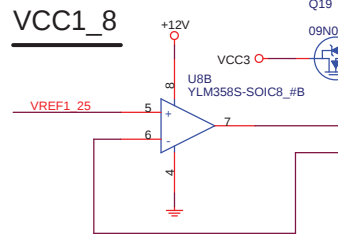
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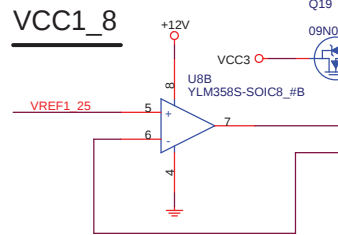
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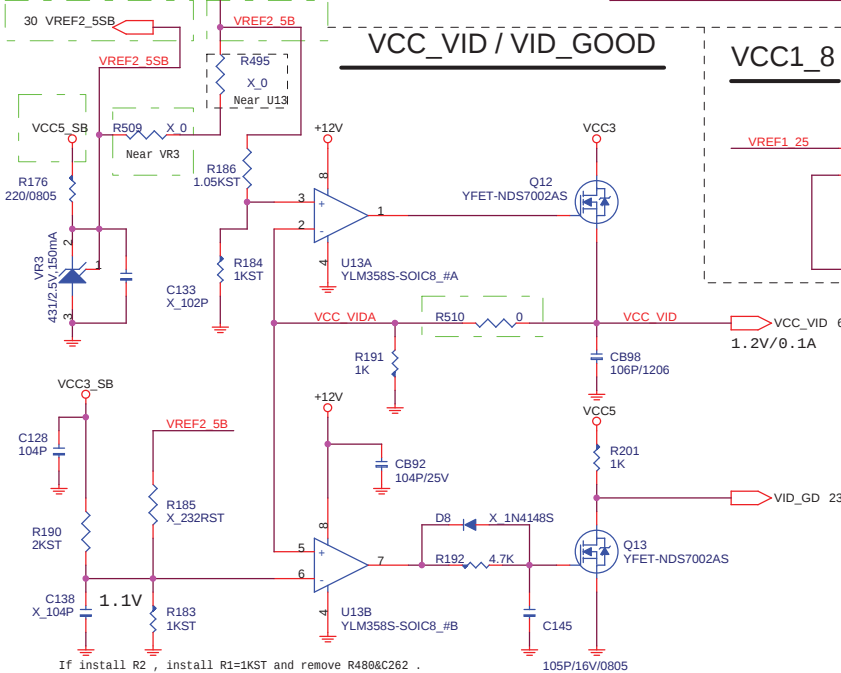
VCC1_8



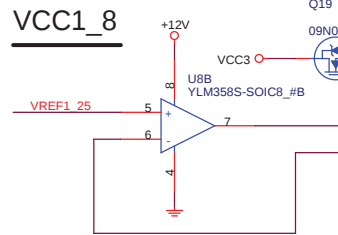
VCC3



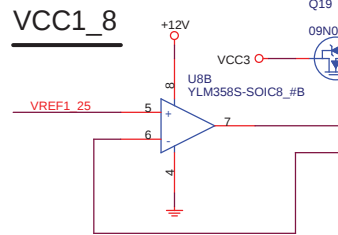
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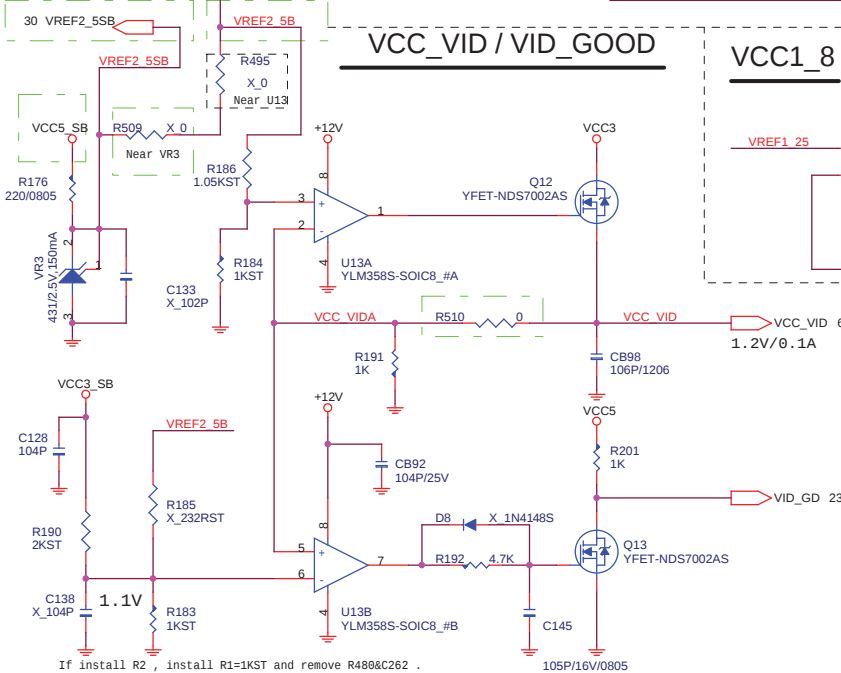
VCC1_8



VCC3



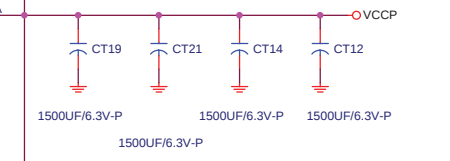
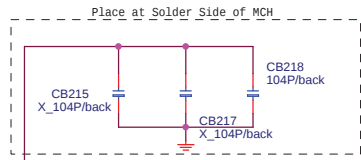
VCC5



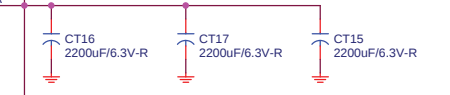
1500uF/16V
Original source:
C94-1521641-N07(NCC)
Second source:
C94-1521641-R07(RUBYCON)
C94-1521641-N10(NICHICON)

CHOK1 : L04-11A7061-T15
=> 2'nd Source
:L04-11A7031-W15 ,
L04-11A7031-M18

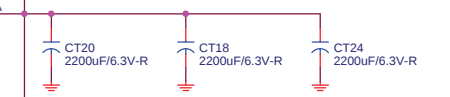
CHOK2,3,4 : L04-75B7011-W15 =>
2'nd Source :L04-75B7011-M18



Hi-side MosFET
Original source:
15N03 : D03-15N030B-I14(INFINEON)
Second source:
FDB6035AL : D03-6035ALB-F01(FAIRCHILD)
FDB6030BL : D03-6030B0B-F01(FAIRCHILD)



Low-side MosFET
Original source:
6670AL : D03-6670ALB-F01(FAIRCHILD)
Second source:
PHB95N03LT : D03-95N030B-P03(PHILIPS)
SUB85N03 : D03-85N030B-V02(VISHAY)
IPB07N03L : D03-07N031B-I14(INFINEON)



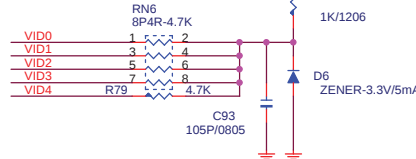
1500uF/6.3V
Original source:
C94-1520631-P01(PANASONIC)
Second source:
C94-1520631-R07(RUBYCON)
C94-1520631-N07(NCC)

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

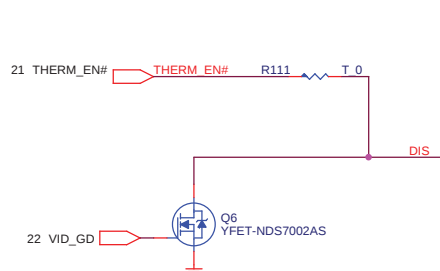
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

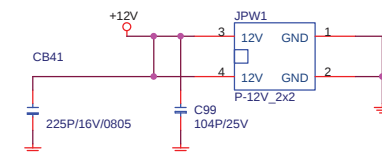
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWM GOOD

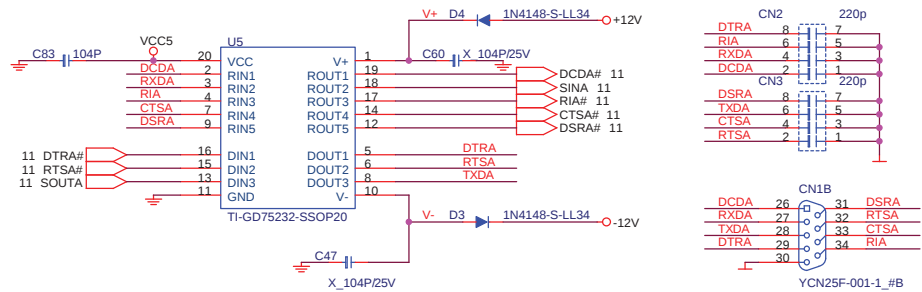


ATX12V POWER CONNECTOR

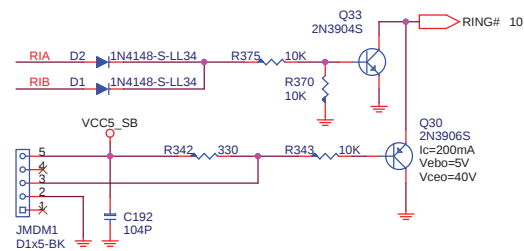


Micro-Star	Title MS-6550	Rev 10A
Document Number	VRM 9.X	
Last Revision Date: Thursday, June 27, 2002	Sheet 23	of 35

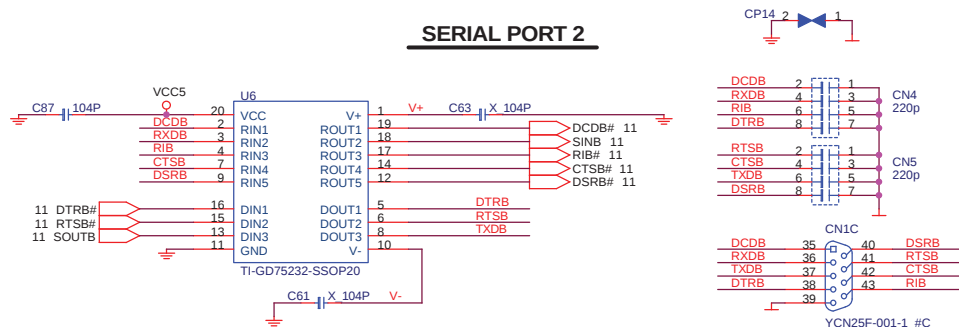
SERIAL PORT 1



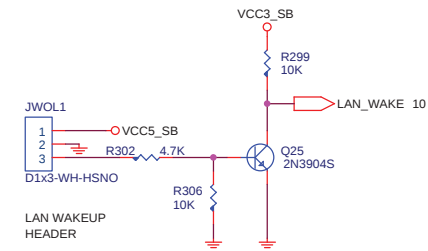
MODEM RING BLOCK



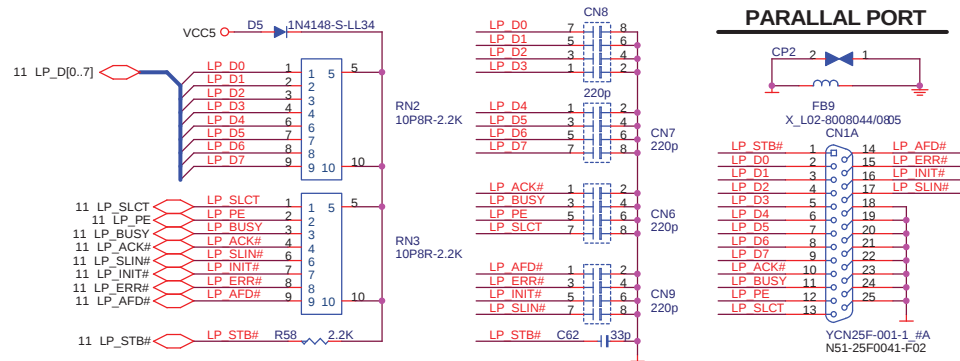
SERIAL PORT 2



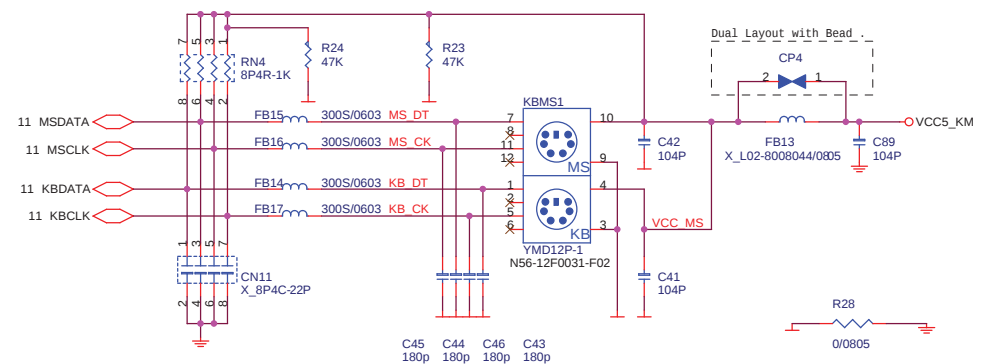
LAN WAKEUP BLOCK



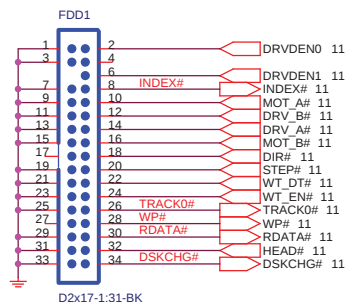
PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR



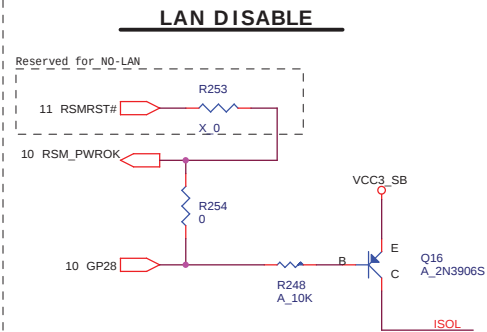
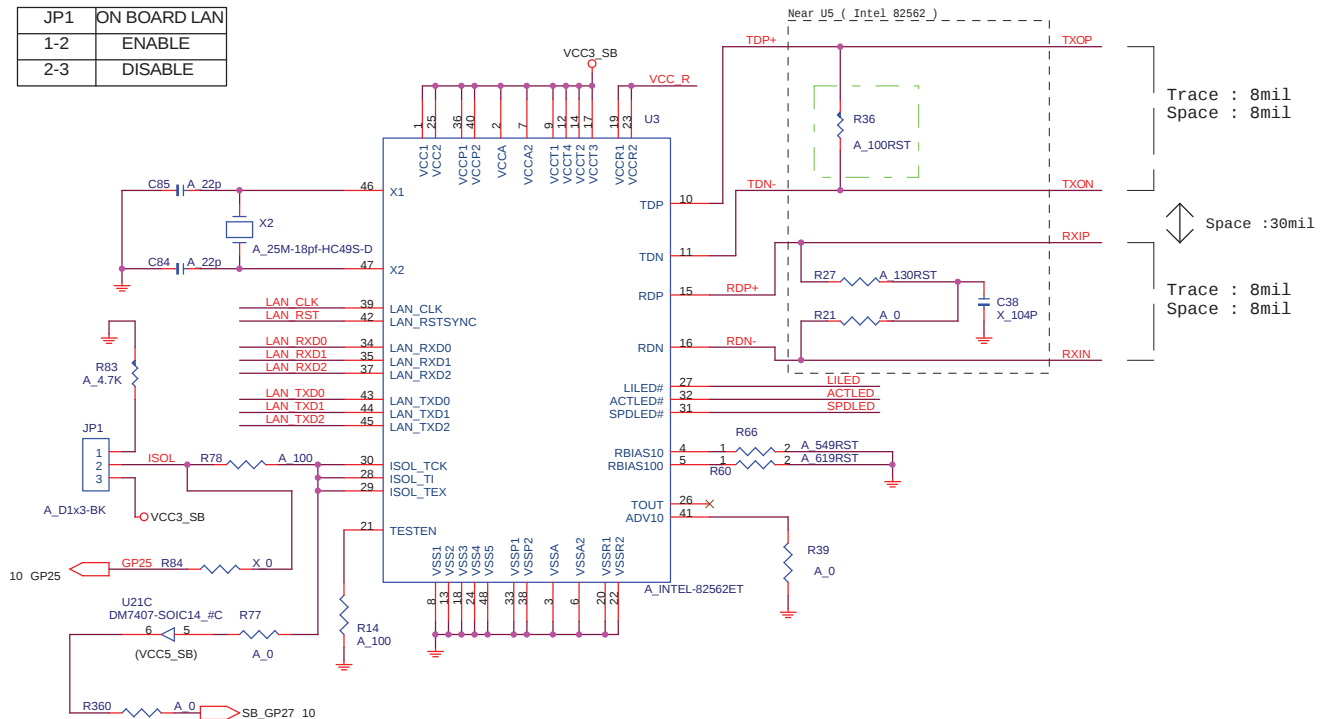
FLOPPY CONNECTOR



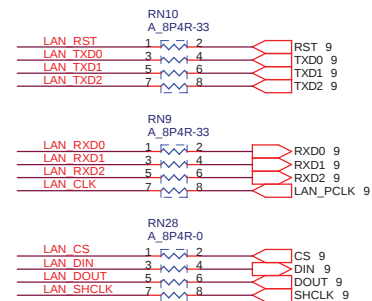
<i>Micro-Star</i>	Title <i>MS-6550</i>	Rev <i>10A</i>
Document Number IO Connector		
Last Revision Date: Thursday, June 27, 2002	Sheet 24 of 35	

Place Termination R as close to 82562EM as possible

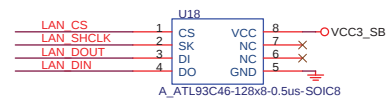
JP1	ON BOARD LAN
1-2	ENABLE
2-3	DISABLE



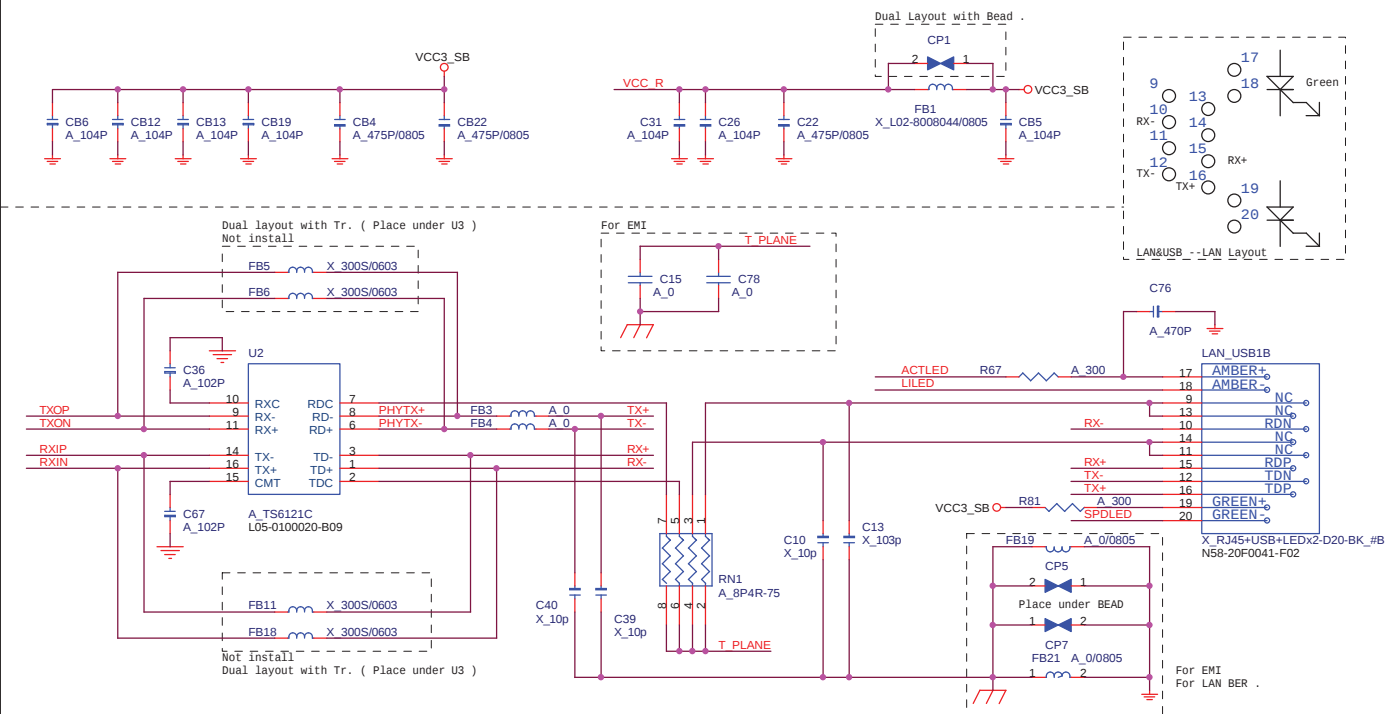
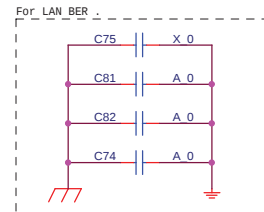
LAN OPTION RESISTORS



LAN EEPROM

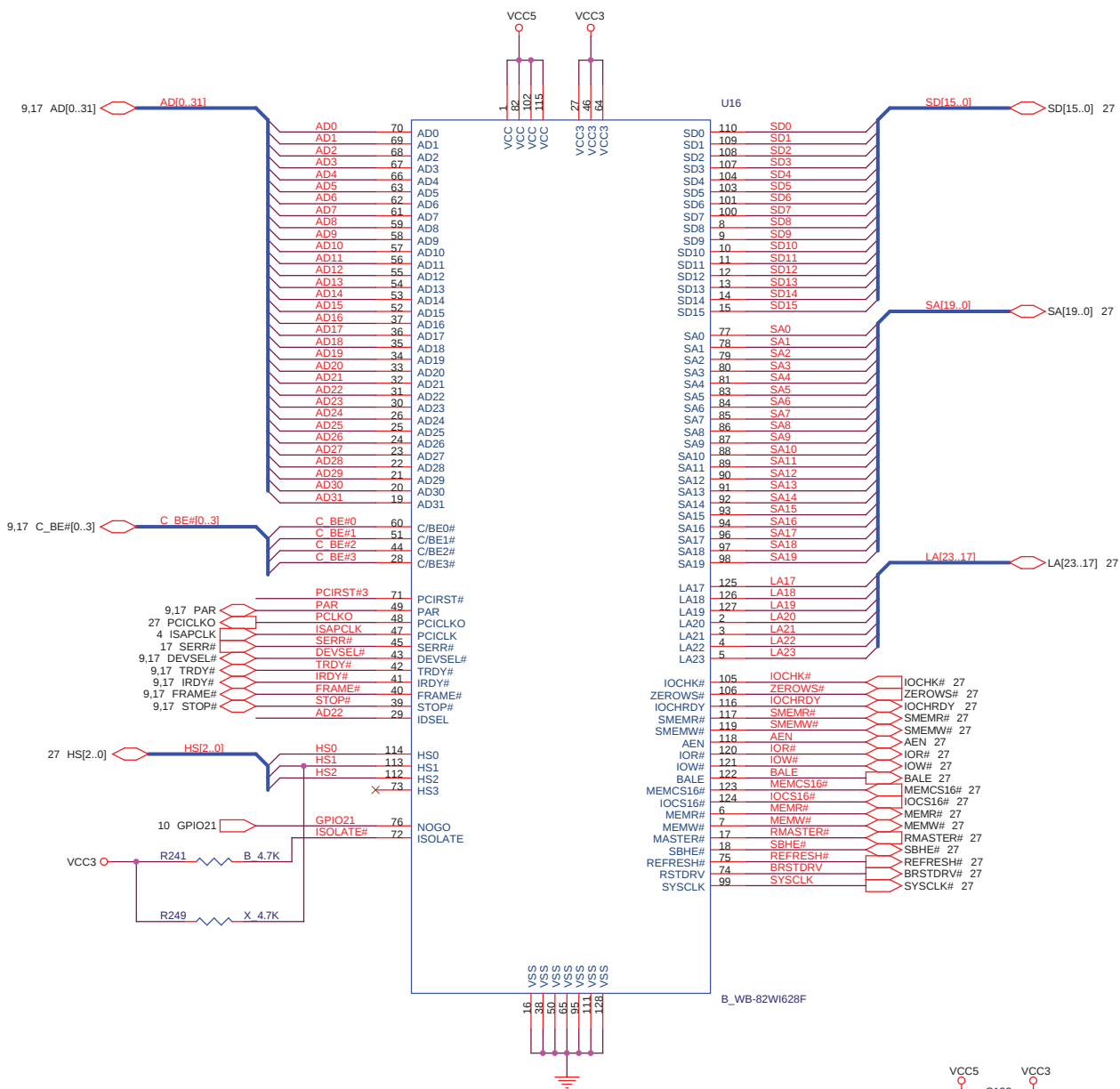


Remark:	
82562EM with 93C66:M33-26N0103-A26	
82562ET with 93C46:M33-1500203-A26	*

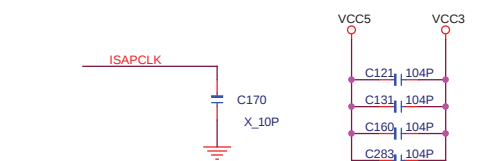
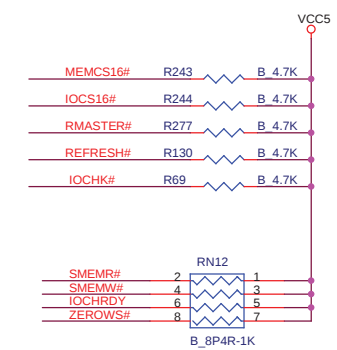


Micro-Star	Title MS-6550	Rev 10A
Document Number LAN INTEL 82562EM/ET		
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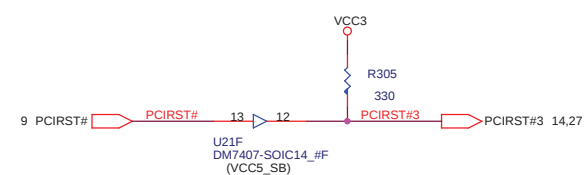
PCI To ISA Bridge, Part 1



PCI to ISA Bridge Pull Up / Low

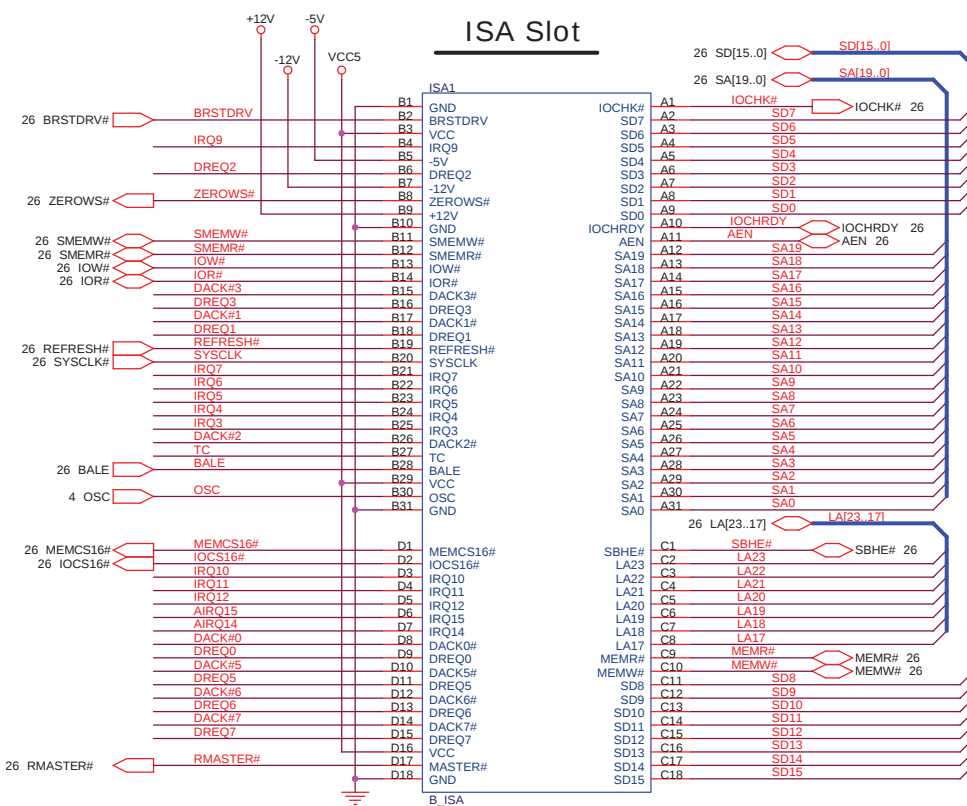
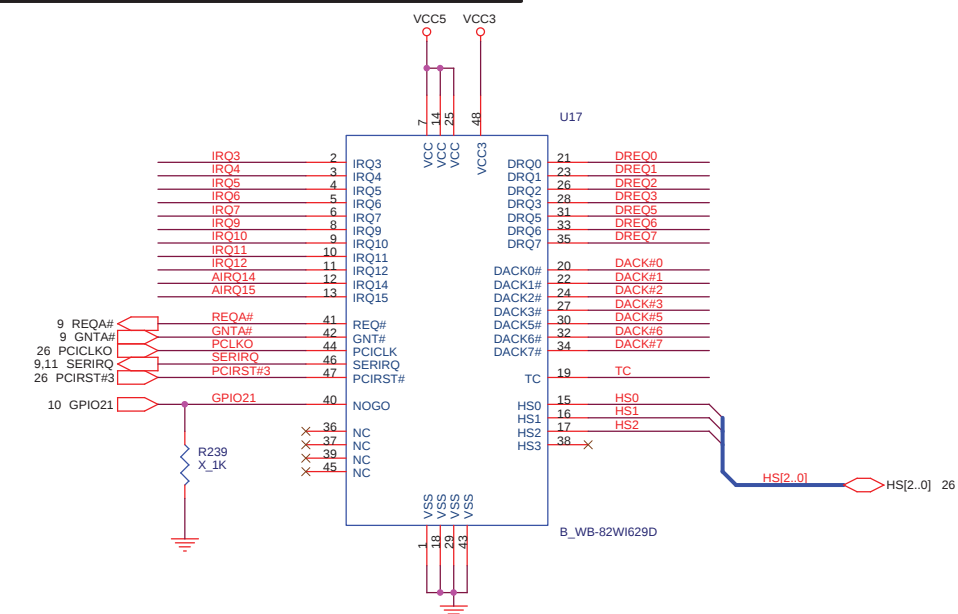


PCI to ISA Bridge Reset

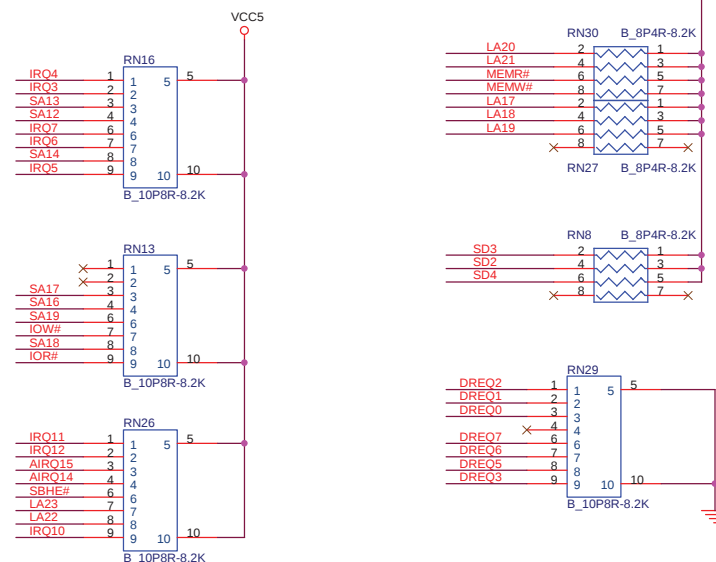
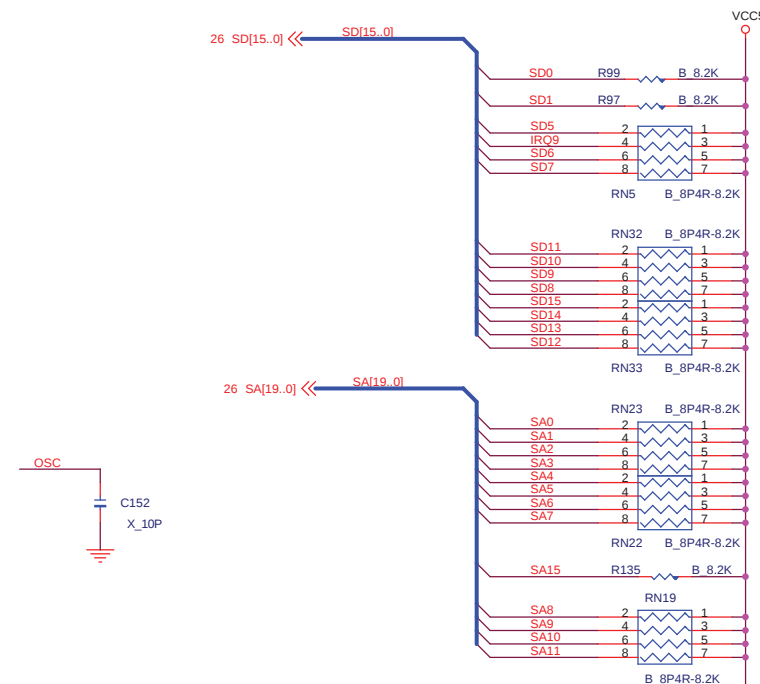


Micro-Star	Title	MS-6550	Rev	10A
	Document Number	ISA Bridge Part 1		
Last Revision Date:		Thursday, June 27, 2002	Sheet	26 of 35

PCI To ISA Bridge, Part 2

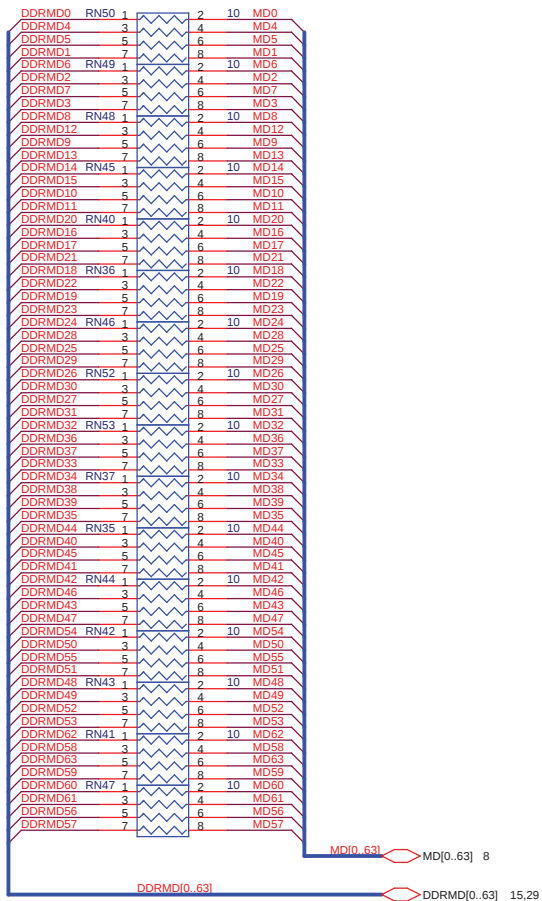


PCI to ISA Bridge Pull Up / Low

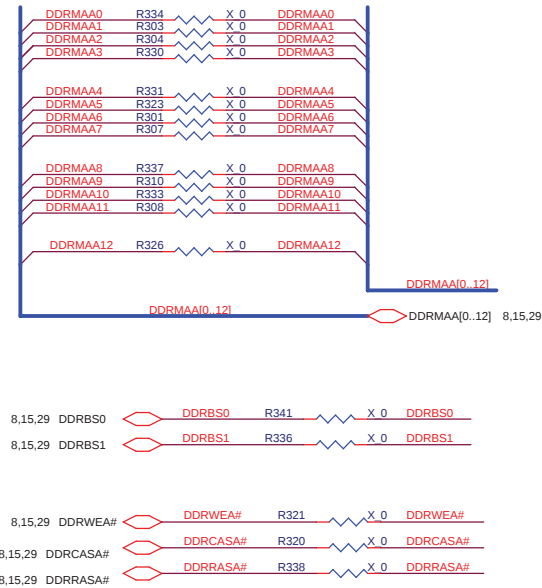


Micro-Star	Title	MS-6550	Rev	10A
Document Number		ISA Bridge Part 2 / ISA SLOT		
Last Revision Date: Thursday, June 27, 2002		Sheet	27	of 35

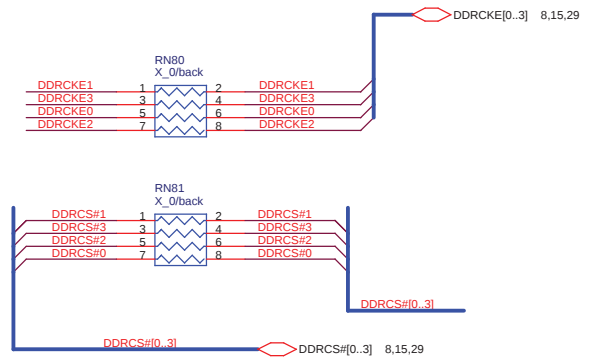
DDR Data Signals



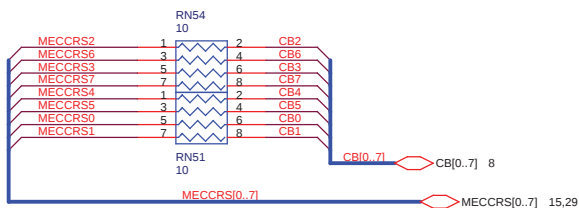
DDR Command Signals



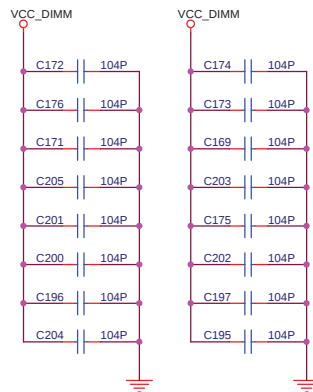
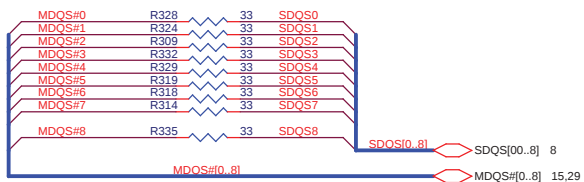
DDR Control Signals



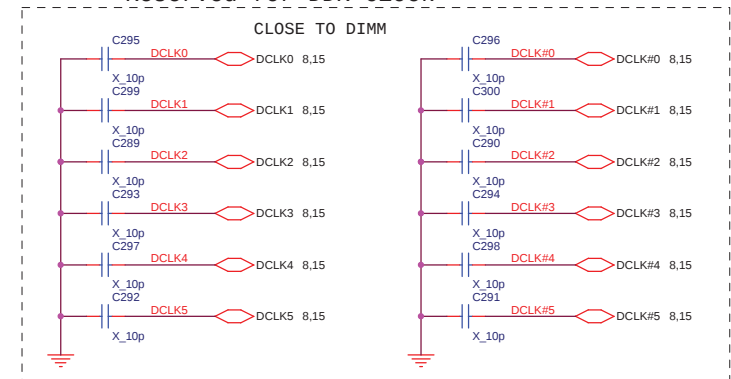
DDR Data ECC Signals



DDR Data Strobe Signals

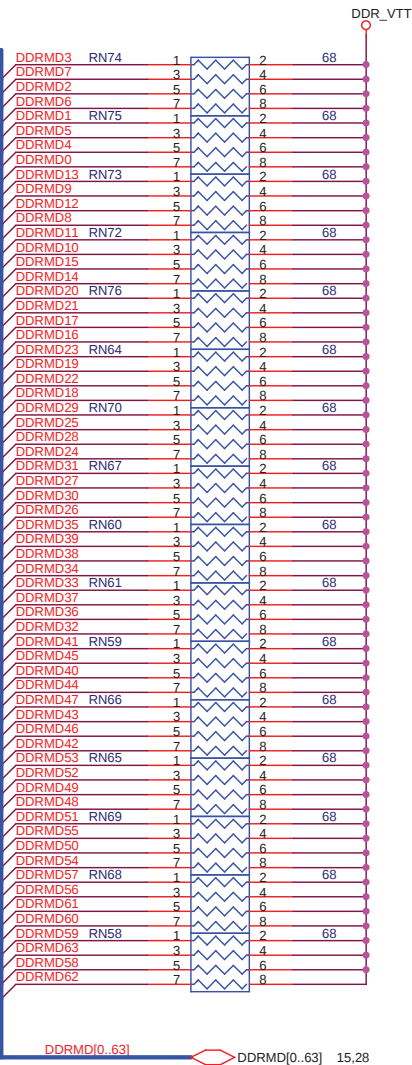


Reserved for DDR Clock

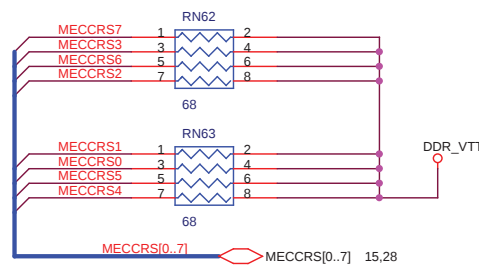


Micro-Star	Title MS-6550	Rev 10A
Document Number DDR_DAMPING		
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DDR Data Terminator Resistor



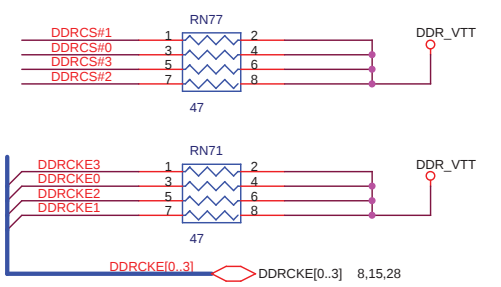
DDR Data ECC Terminator Resistor



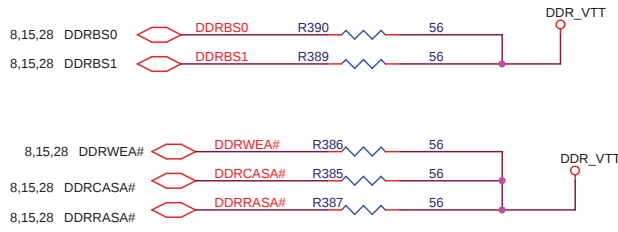
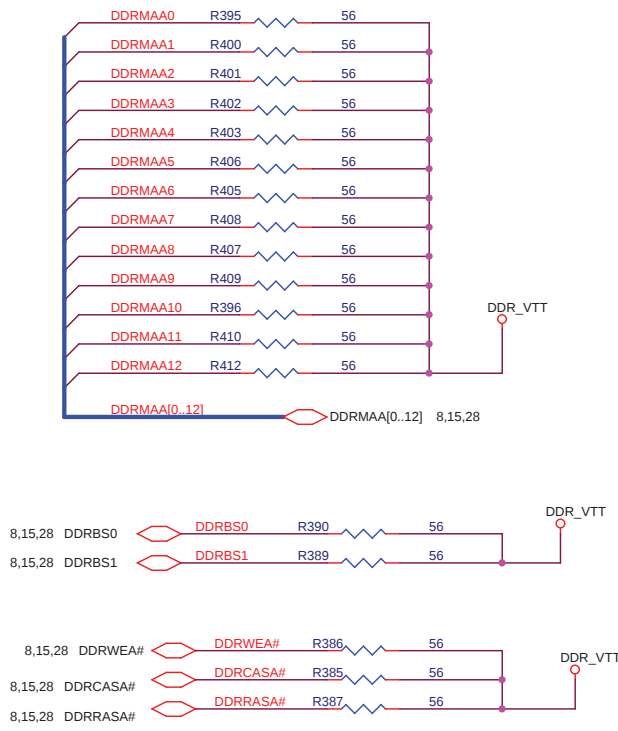
DDR Data Strobe Terminator Resistor



DDR Control Signal Terminator Resistor

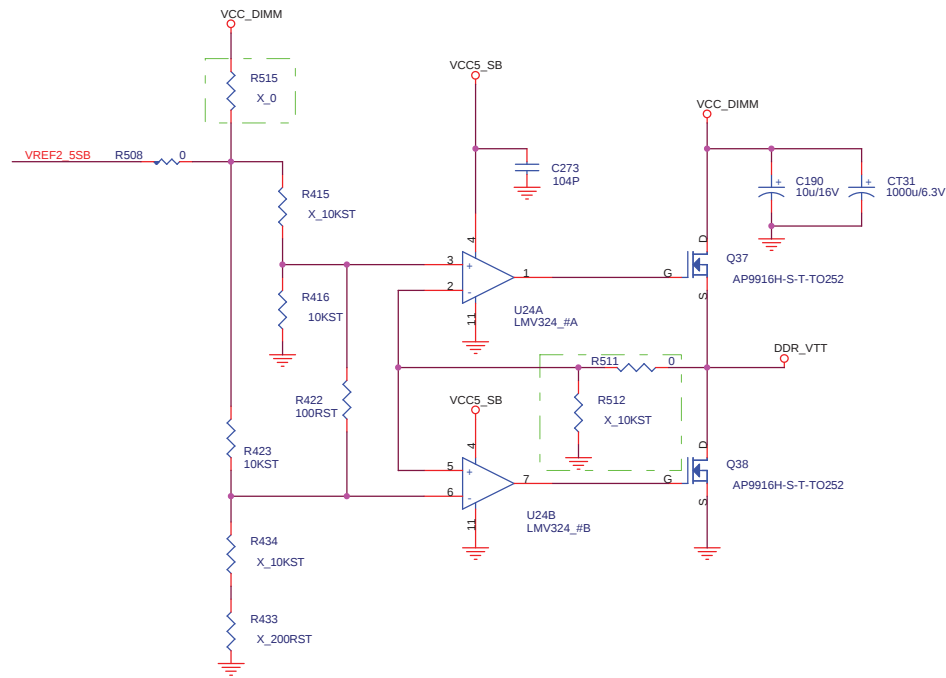


DDR Command Signal Terminator Resistor

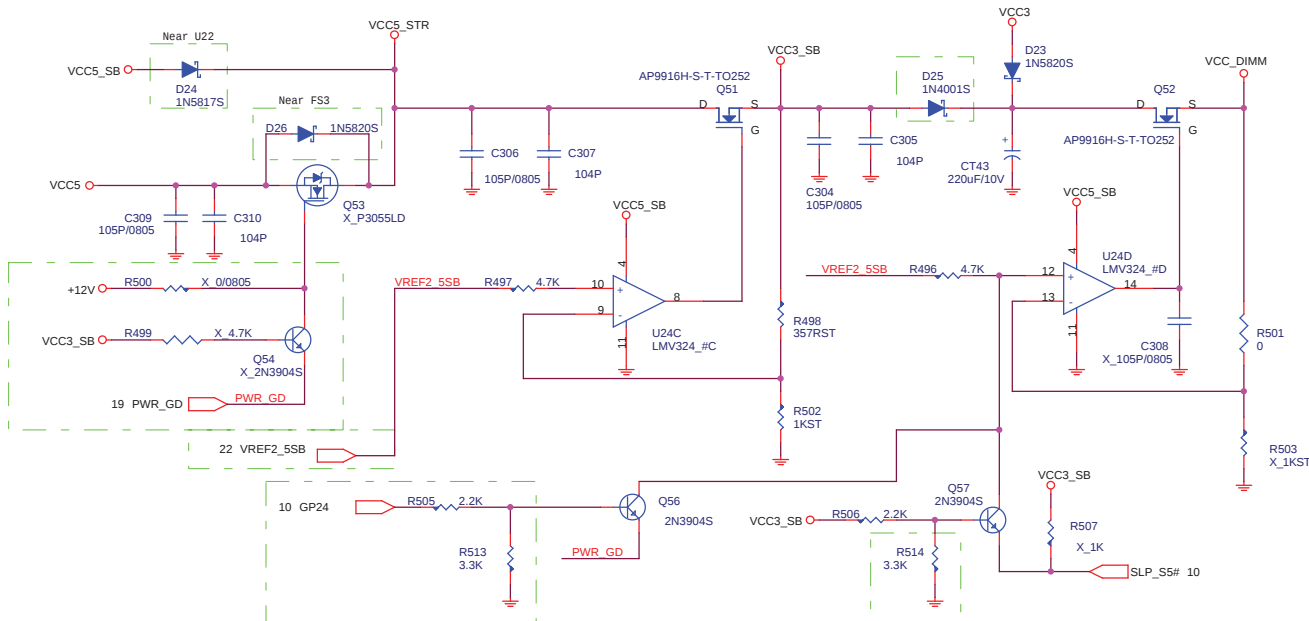


Micro-Star	Title	MS-6550	Rev	10A
	Document Number	DDR_TERMINATION		
	Last Revision Date:	Thursday, June 27, 2002	Sheet	29 of 35

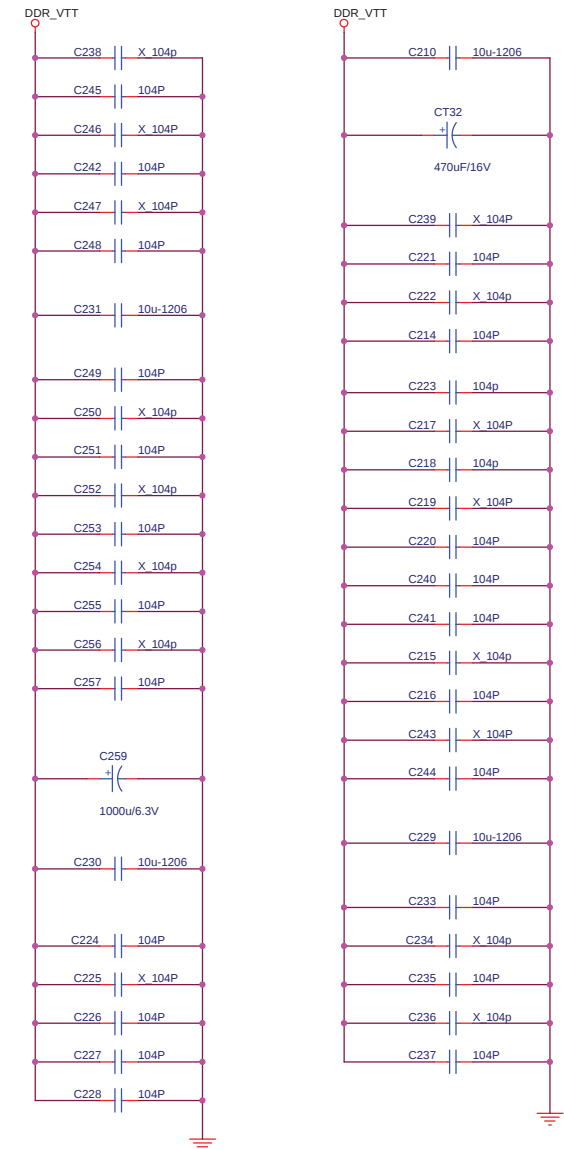
DDR_VTT Power



VCC5_STR & VCC3_SB & VCC_DIMM

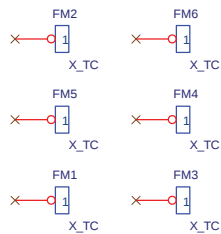
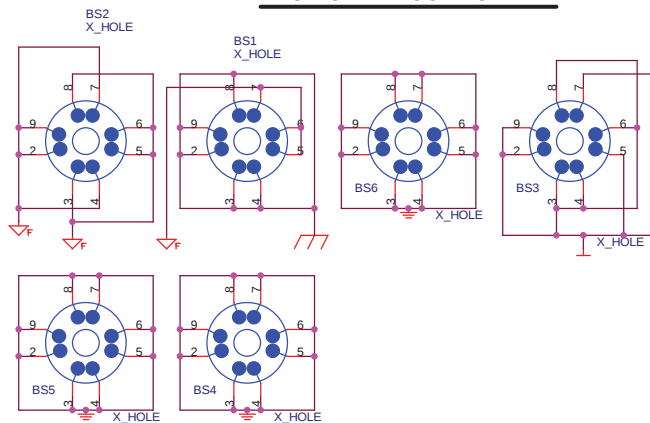


DDR Terminator Capacitance

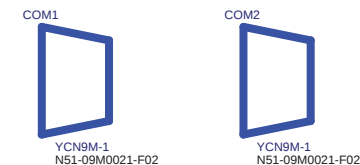
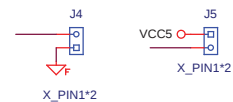


Micro-Star	Title MS-6550	Rev 10A
Document Number DDR_T_POWER		
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PCB OTHER COMPONENT



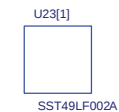
SIMULATION TRACE



MS6550/VER:1.0A PCB



BIOS



BAT SOCKET



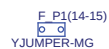
JBAT1 Clear CMOS		
1 - 2	Normal	*
2 - 3	Clear CMOS	



LEGEND AUDIO



Enable Buzzer



J3 BIOS Update

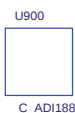
SHORT	Locked
OPEN	Unlocked *



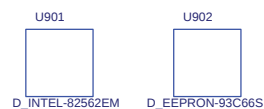
JP1	ON BOARD LAN
1-2	ENABLE
2-3	DISABLE



Note C : Support ADI1885



Note : D (Need add Note:A) Support Intel-82562EM LAN

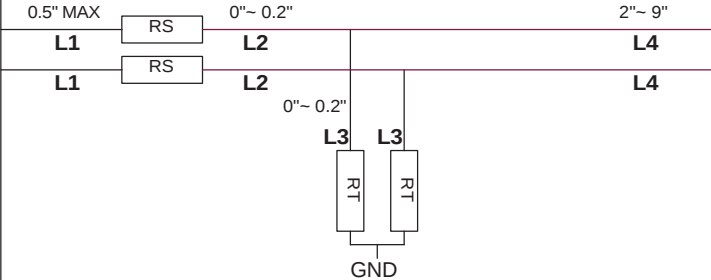
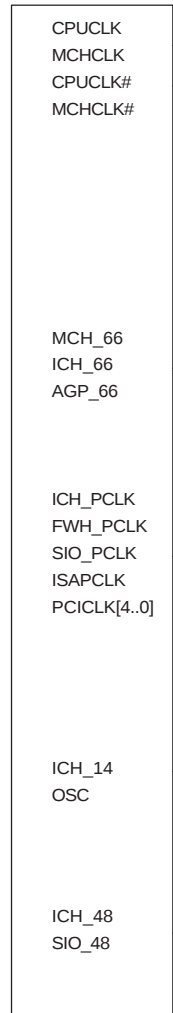


Jumper Setting & Connector Setting

Jumper	Description
J3	BIOS Protection function Open = Unlocked (Default) Short = Locked
JP1	H/W Control On Board LAN Function Enable = Short 1-2 (Default) Disable = Short 2-3
JBAT1	CLEAR CMOS 1-2 => NORMAL (Default) 2-3 => CLEAR CMOS
J2	CHASSIS INTRUSION HEADER Low = Enable (Short) Hi = Disable (Open)
JGS1	EXTSMI# (Low Enable => Short)

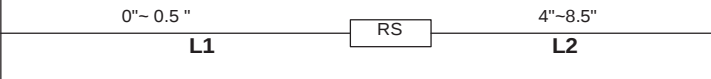
Connector	Description
U14	INTEL mPGA478-B CPU
IDE1 IDE2 FDD1	Primary Secondary Floppy
DIM1 DIM2	SDRAM DIMM1 SDRAM DIMM2
AGP1	AGP Slot
PCI1 PCI2 PCI3	PCI Slot1 PCI Slot2 PCI Slot3
COM1 COM2 LPT (CN1)	Serial Port Serial Port Parallel Port
JMDM1 JWOL1	MODEM RING HEADER LAN WAKEUP HEADER
KBMS1 LAN_USB1 USB1	PS/2 Keyboard and PS/2 mouse USB REAR CONNECTOR USB Front Panel HEADER
F_P1 IR1	Front Panel IR HEADER
POWER JPW1	ATX Power ATX12V Power
C_FAN1 S_FAN1 P_FAN1	CPU FAN HEADER SYS FAN HEADER ATX FAN HEADER
J1 JAUDIO1 CD_IN1 MDM_IN1	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN) AUDIO HEADER FOR LEGEND CD IN HEADER MODEM_IN HEADER

Micro-Star	Title MS-6550	Rev 10A
Document Number JUMPER SETTING		
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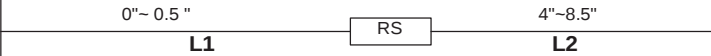
DEVICE	L1+L2
CPU	X
MCH	X + (0.4"~0.6")
ITP	X

- * Line Width : 7.0 mil
- * Differential pair spacing : 7.0mil
- * Spacing to other traces : 28 mil
- * BCLK0/BCLK1 LENGTH MATCH +/- 10 mil



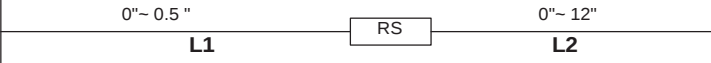
DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

- * Line Width : 5.0 mil
- * Spacing to other traces : 20 mil



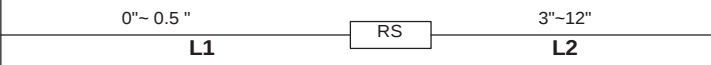
DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

- * Line Width : 5.0 mil
- * Spacing to other traces : 20 mil
- * L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH



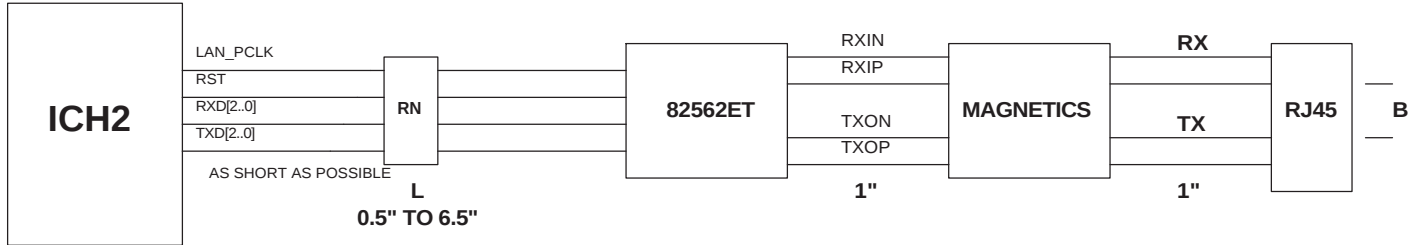
DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

- * Line Width : 5.0 mil
- * Spacing to other traces : 10 mil



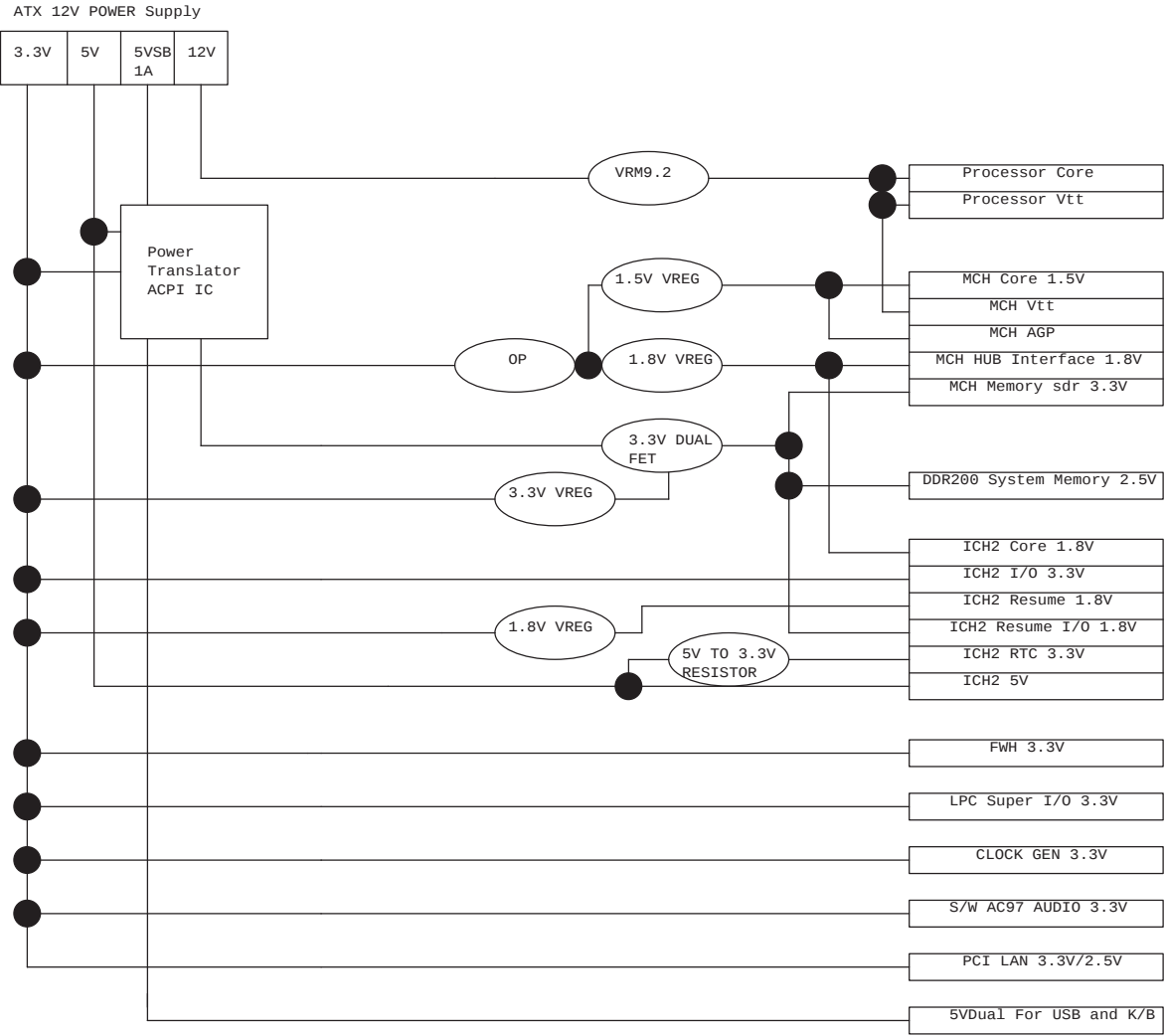
DEVICE	L1+L2
ICH	
SIO	

- * Line Width : 5.0 mil
- * Spacing to other traces : 20 mil



- * Line Width :6.0 mil
- * Differential signls space : 8mils
- * Differential signls space with other signal 16mil
- * TX/RX group gap need min 30 mils

Power Delivery Map



Revision	Date	Page	Description
0A	09/26/2001		Creat new schematics (16556-0A_09-26.dsn)
1.0	10/11/2001	18	Correct IDE1 & IDE2 part number .
		19	Turn CONN1(ATX_Power) around 180 degree for technical issue .
		4,5	Reserved for future CPU , Add R473 & R474 & R475 to "BSEL0" .
		19	For costdown ,Add U20B & R476 to replace Q24 & R284 & R 282 .
		20	For costdown , Add R477 & R478 & R479 in order to replace Q21 & Q44 & Q23 . (Reserved)
1.0A	11/14/2001 (16550-10A_11-12A.dsn)	25	Modify LAN Enable/Disable control circuit for M/B space . (Delete unused component)
		6	For costdown , Replace all SP-CAP. (in CPU) by ceramic-CAP (10uF76.3V) .
		8	For "VCC_DIMM" voltage quality in margine test , Add two 105pF/0805 CAP (C301 & C302) . (Reserved)
		30	For power quality ("VCC_DIMM" & " DDR_VTT") ; Change C132 to connecting "DDR_VTT" and change "C258" to connecting "VCC_DIMM" .
			For thchnical issue , Move layout location of C14 & C17 .
	11/26/2001 (16550-10A_11-26.dsn)	30	For "VCC_DIMM" power loss issue when power-connect connect to M/B at first time , Add "GP24" (as GP0) & R513=3.3k ohm and change R505=1.5k ohm .
		19	For costdown , Delete R283 & R476 (0 ohm) .
		22	Modify circuit of VR2 & VR3 for correct power sequence and quality .
		25	Delete C65 & turn U2->180 degree for signal quality , And delete C38 and add FB19=0 ohm & C82=0 ohm for LAN testing (Cable=150 Meter) .
		30	Add R511 & R512 for changing "DDR_VTT" power level (Reserved) , And change Q37&Q38 for low Vgs CMOSFET (D03-9916H0B-A36) at heavy loading .
		30	Change D25 from 1N4148S to 1N5817S for power quality of "VCC_DIMM" at S3 mode .
		30	For costdown , Add D26 (1N5820S) to replace Q53 .
		30	Change Q53 to Q54 power control circuit for low "VCC5_STR" power issue .
		30	Add R514=3.3k ohm & change R506=1.5k ohm for power-loss issue .
		11	Install R87=4.7k ohm for 48MHz SIO frequency . (Change SIO Freq. from 24MHz to 48MHz for ICS 950213 clock-generator (not supporting 24MHz) .
23	For better Vcore power quality , Change Vcore VIA & Layout position & CHOK2-4 ->L04-75B7011-W15(0.8uH/35A) , Add CB228 .		
17	Change " VCC3_SB " trace width from Q51 to PCI slot for PCI standby-power heavy loading testing (power decrese over-SPEC) .		
11/28/2001 (16550-10A_11-28.dsn)	6,8	For costdown delete : CB87,C134,CB83,CB88,CB84,CB85,C135,CB89,CB68,CB70,CB69,CB63,CB64,CB62,CB65,CB66,CB67,CB74,CB75,CB106,CB113 . (Vcore CAP.)	
	9,10	Change ICH2 to VER:B5 .	
	22	For "VCC1_8SB" delete R486 & R487 . (Don't need install)	
	23	For Vcore power quality , Change R113 = 240 KST & R117 = 1.65 KST ohm .	
	25	For LAN BER , Change C74=0 ohm & add C75=C81=0 ohm & change R21=0 ohm , R27=130RST ohm .	
12/10/2001	30	For "VCC_DIMM" power quality , Change D25 from 1N5817 -> 1N4001 & change R498 = 357RST ohm .	
	12,13	For customer requested L2 , Change audio CODEC from ADI1881A to ADI1885 . (Needed to modify relative component) .	
	25	For Intel LAN Lab IEEE802.3 test , delete C39&C40&C75 , and change C36&C67 from 104pF to 102pF .	
		(16550-10A_12-10.dsn)	
	23	For Vcore power issue , Change CB30=104pF & CB38=0.47uF & R114=R80=R123=3.3RST .	
01/21/2002 (16550-10A_01-21-91.dsn)	19	For customer issue (L2) , Install R451=0 ohm (Default=>Enable Buzzer) & limited "I/O port" (CN1,COM1,COM2,J1,KBMS1,LAN_USB1) to Foxcon .	
	10	For RTC issue , Delete R372 & R363 . (For Intel ICH2/VER:B5)	
04/25/2002	23	For voltage issue , Change CB41 from 4.7uF/10V to 2.2uF/16V .	
06/10/2002	30	For L2 P.S. compatibility and MOSFET/Q51&Q52 too hot issue , Delete R515 & add R508 = 0 ohm .	
06/11/2002		For PM requested , Creat 2 new-BOM from MS6550L2/VER:1.0A OPT:I+L(6550-020) to (1)MS6550L2 OPT:I & (2)MS6550L2 Standard .	

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