MS-6549

Version 00B
11/27/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:
Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:
INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:
BIOS -- FWH
LPC Super I/O -- W83627HF
Clock Generation -- CY28323
PCI SOUND -- C-MEDIA CMI8738MX
PCI 1394 --TI TSB43AB22

Expansion Slots:
AGP2.0 SLOT * 1
PCI2.2 SLOT * 4

Standard:Wo/1394, Wo/Front Audio
Opt A:W/1394, W/Front Audio, Wo/PCI4

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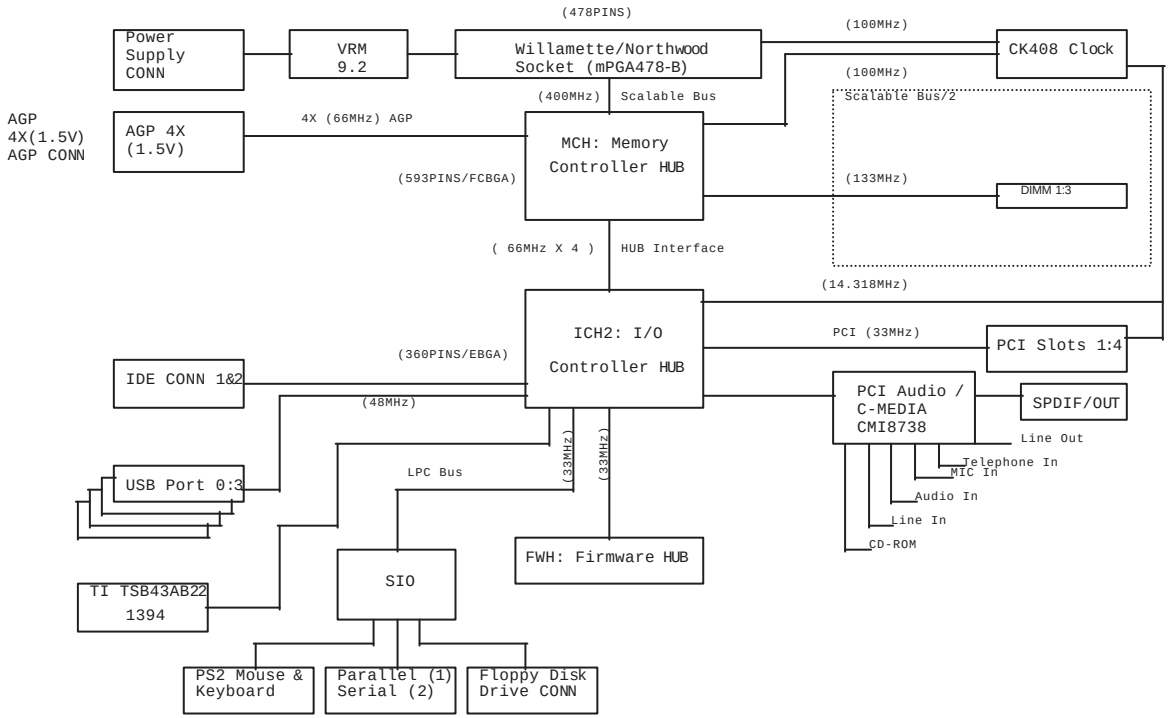

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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Not Implemented
GPIO 22	OD	4.7K pull up VCC3
GPIO 23	O	BIOS Locked/Unlocked
GPIO 24	I/O	Non
GPIO 25	I/O	Non
GPIO 26	I/O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	Non
GPIO 29~31	O	Not Implemented

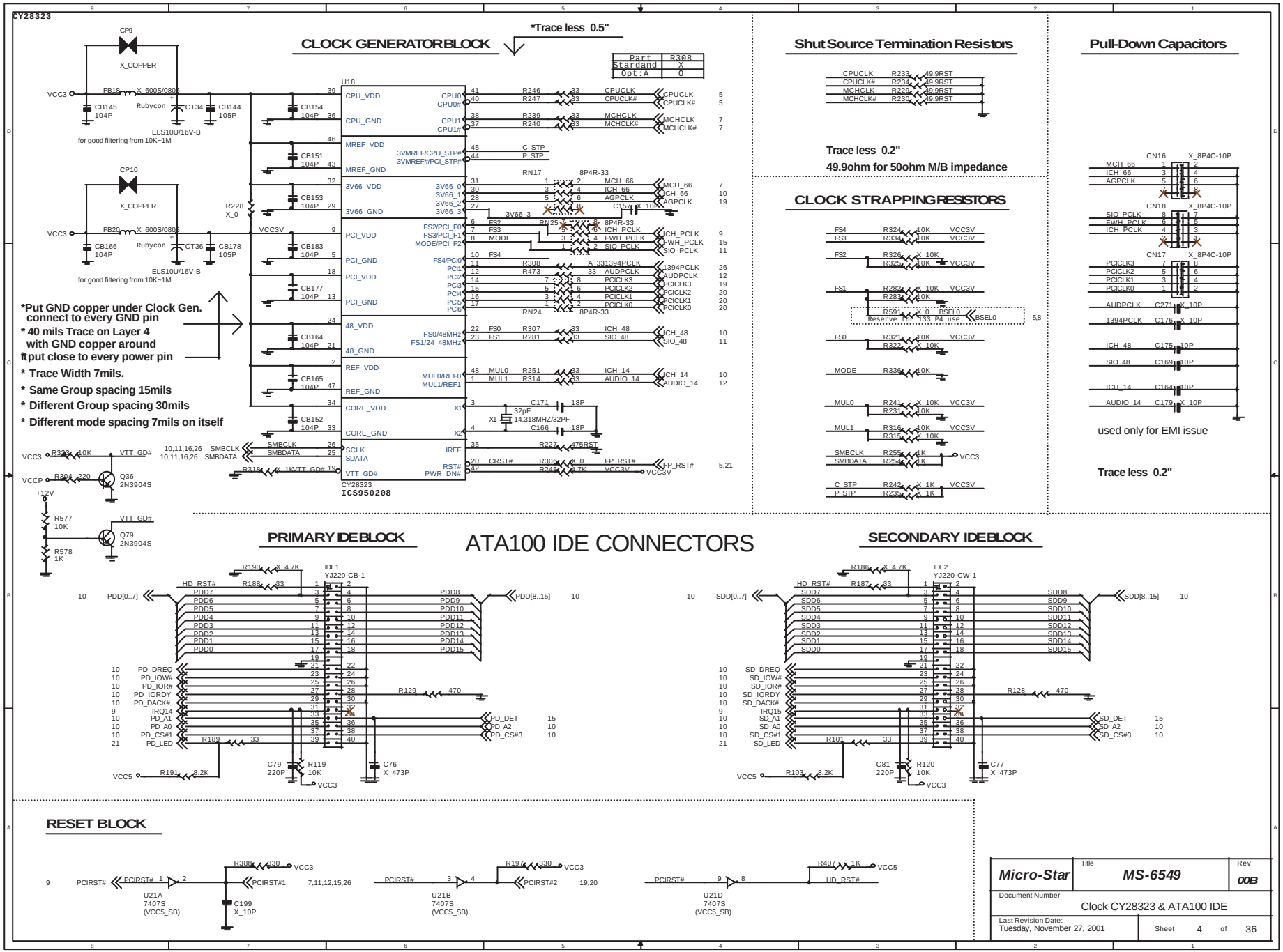
FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DLED-Super I/O

GPIO Pin	Type	Function
GP32	I/OD	Non Connect
GP24	I/OD	Non Connect
GP34	I/OD	Non Connect
GP33	I/OD	Non Connect

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19
PCI Audio	INTF#	AD25
PCI 1394	INTH#	AD23


CY28323
CLOCK GENERATOR BLOCK
*Trace less 0.5"
Part | R308
Stardand | X
Opt:A | 0
U18
CPU_VDD
CPU_GND
MREF_VDD
MREF_GND
3V66_VDD
3V66_GND
PCI_VDD
PCI_GND
48_VDD
48_GND
REF_VDD
REF_GND
CORE_VDD
CORE_GND
CPU0
CPU0#
CPU1
CPU1#
3VMREF/CPU_STP#
3VMREF#/PCI_STP#
3V66_0
3V66_1
3V66_2
3V66_3
FS2/PCI_F0
FS3/PCI_F1
MODE/PCI_F2
FS4/PCI0
PCI1
PCI2
PCI3
PCI4
PCI5
PCI6
FS0/48MHz
FS1/24_48MHz
MUL0/REF0
MUL1/REF1
X1
X2
IREF
SCLK
SDATA
RST#
PWR_DN#
CY28323
ICS950208
CPUCLK
CPUCLK#
MCHCLK
MCHCLK#
C_STP
P_STP
MCH_66
ICH_66
AGPCLK
FWH_PCLK
SIO_PCLK
1394PCLK
AUDPCLK
PCICLK3
PCICLK2
PCICLK1
PCICLK0
ICH_48
SIO_48
ICH_14
AUDIO_14
FP_RST#
CRST#
SMBCLK
SMBDATA
Shut Source Termination Resistors
CPUCLK R233 49.9RST
CPUCLK# R234 49.9RST
MCHCLK R229 49.9RST
MCHCLK# R230 49.9RST
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
FS4 R324 10K VCC3V
FS3 R334 10K VCC3V
FS2 R326 X 10K
R325 10K VCC3V
FS1 R282 X 10K VCC3V
R283 10K
R591 X 0 BSEL0
Reserve for 133 P4 use.
BSEL0 5,8
FS0 R321 10K VCC3V
R322 X 10K
MODE R336 10K
MUL0 R241 X 10K VCC3V
R231 10K
MUL1 R316 10K VCC3V
R315 X 10K
SMBCLK R255 1K VCC3
SMBDATA R254 1K
C_STP R242 X 1K VCC3V
P_STP R235 X 1K
Pull-Down Capacitors
CN16 X_8P4C-10P
MCH_66 1 2
ICH_66 3 4
AGPCLK 5 6
7 8
CN18 X_8P4C-10P
SIO_PCLK 8 7
FWH_PCLK 6 5
ICH_PCLK 4 3
2 1
CN17 X_8P4C-10P
PCICLK3 7 8
PCICLK2 5 6
PCICLK1 3 4
PCICLK0 1 2
AUDPCLK C271 X_10P
1394PCLK C176 X_10P
ICH_48 C175 10P
SIO_48 C169 10P
ICH_14 C164 10P
AUDIO_14 C179 X_10P
used only for EMI issue
Trace less 0.2"
*Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Different mode spacing 7mils on itself
ATA100 IDE CONNECTORS
PRIMARY IDE BLOCK
IDE1
YJ220-CB-1
PDD[0..7]
PDD[8..15]
PD_DREQ
PD_IOW#
PD_IOR#
PD_IORDY
PD_DACK#
IRQ14
PD_A1
PD_A0
PD_CS#1
PD_LED
PD_DET
PD_A2
PD_CS#3
SECONDARY IDE BLOCK
IDE2
YJ220-CW-1
SDD[0..7]
SDD[8..15]
SD_DREQ
SD_IOW#
SD_IOR#
SD_IORDY
SD_DACK#
IRQ15
SD_A1
SD_A0
SD_CS#1
SD_LED
SD_DET
SD_A2
SD_CS#3
RESET BLOCK
PCIRST#
PCIRST#1
PCIRST#2
HD_RST#
U21A 7407S (VCC5_SB)
U21B 7407S (VCC5_SB)
U21D 7407S (VCC5_SB)
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Clock CY28323 & ATA100 IDE
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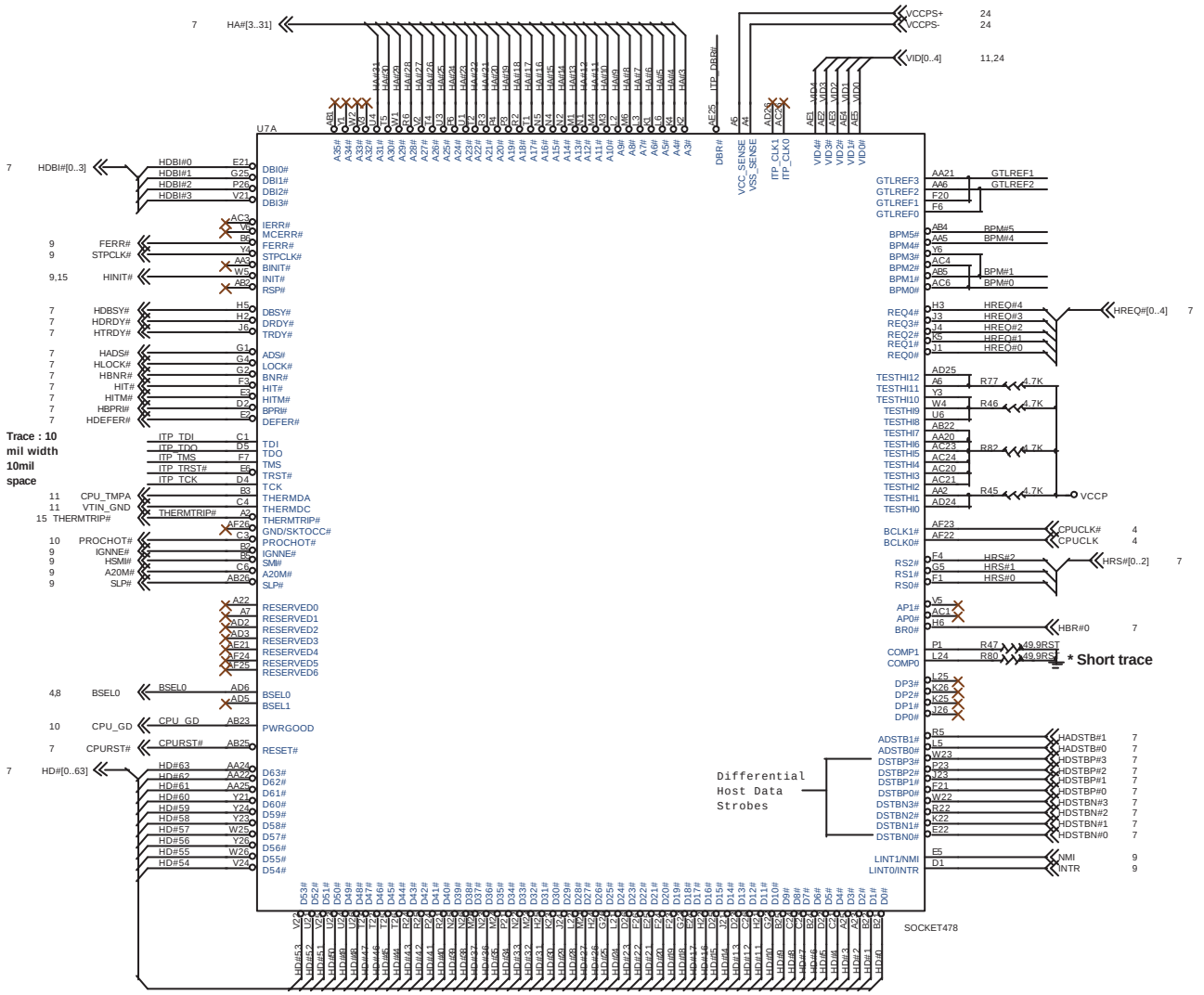
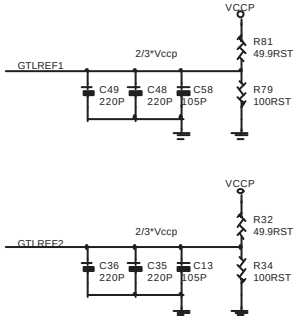
CPU SIGNAL BLOCK

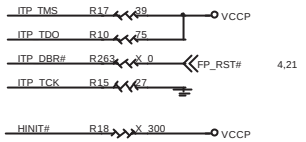


CPU GTL REFERNCE VOLTAGE BLOCK

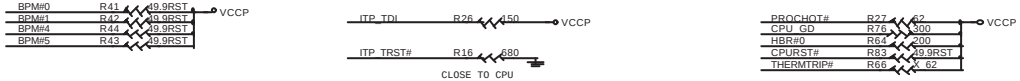


Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU

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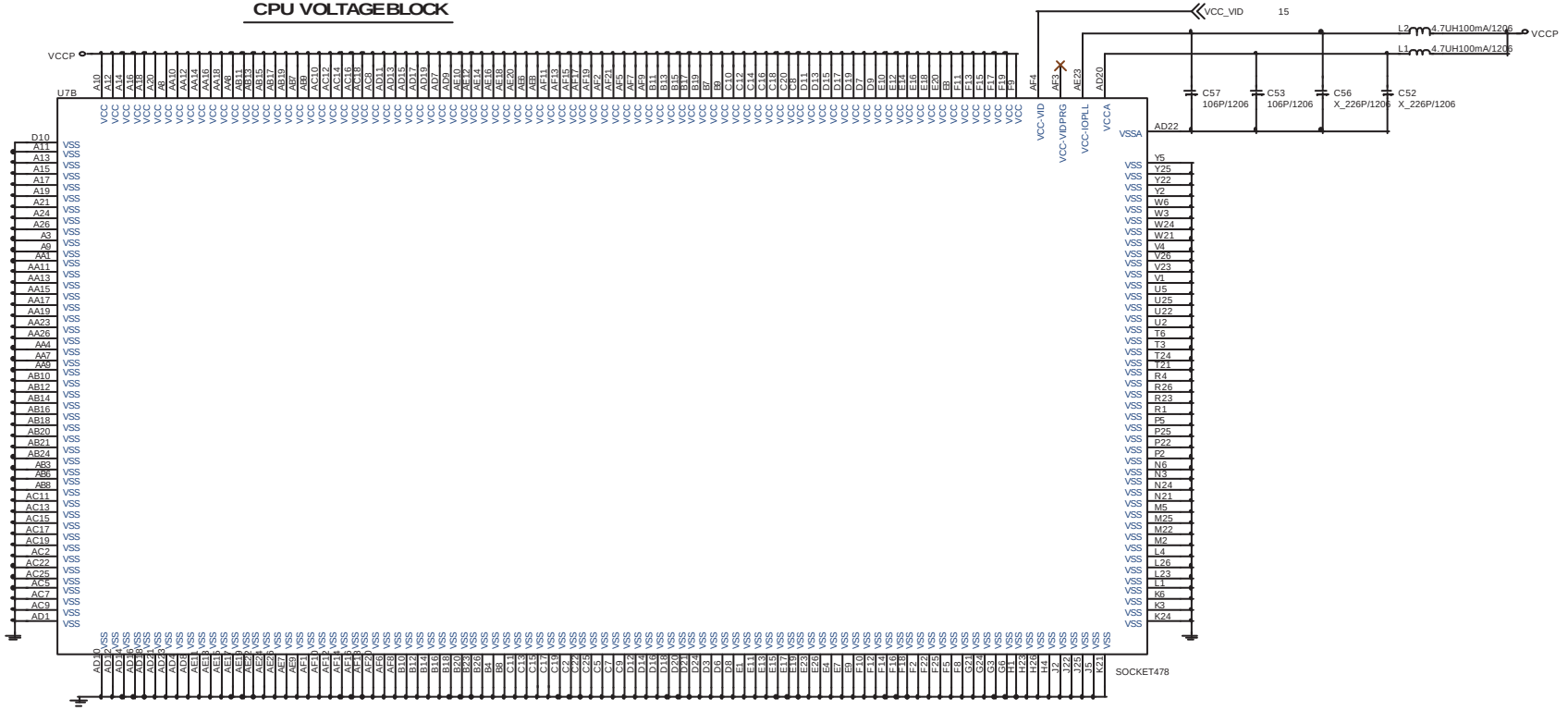
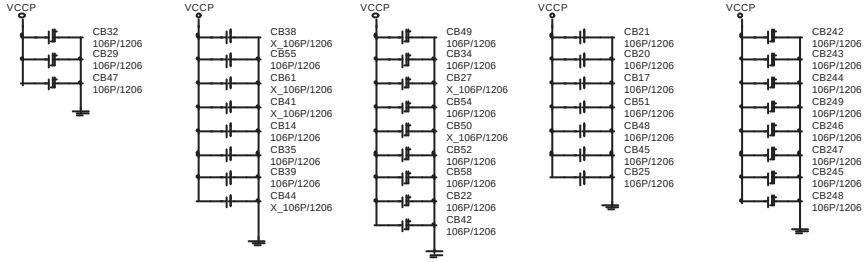
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

Micro-Star	Title: MS-6549	Rev: 00B
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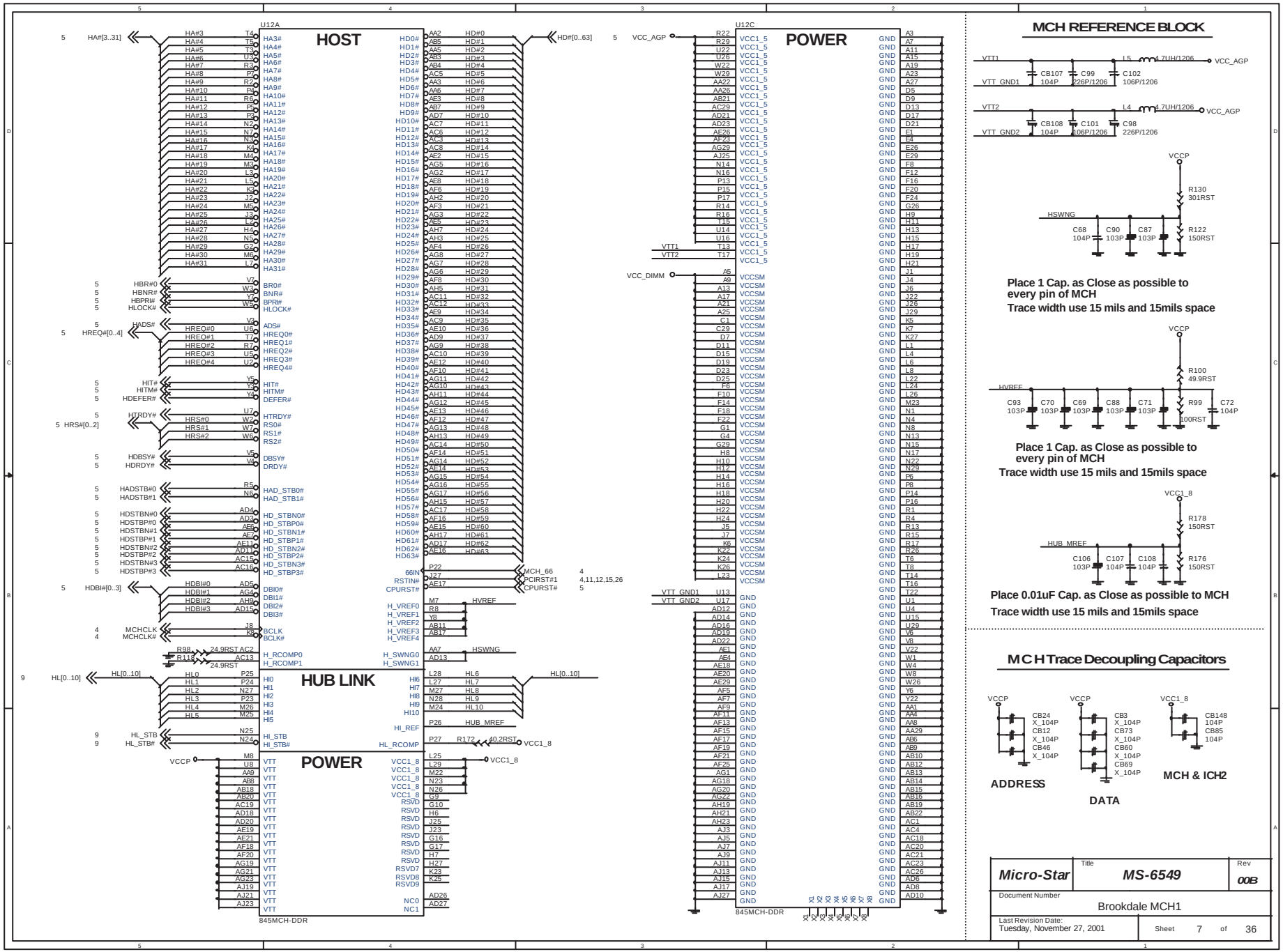

MCH REFERENCE BLOCK

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space

MCH Trace Decoupling Capacitors

ADDRESS

DATA

MCH & ICH2

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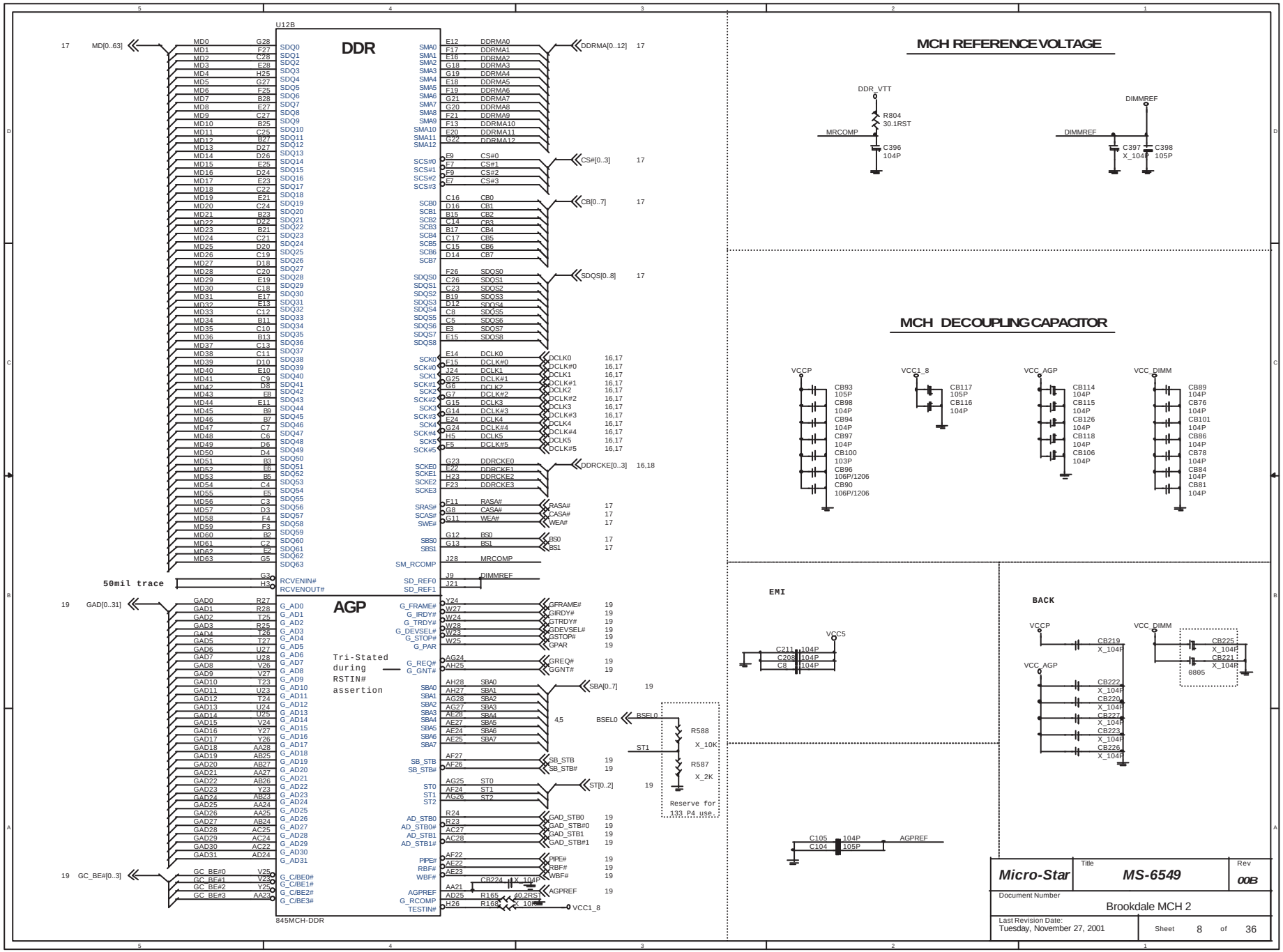
U12B
DDR
AGP
845MCH-DDR
Tri-Stated during RSTIN# assertion
50mil trace
Reserve for 133 P4 use.
MCH REFERENCE VOLTAGE
DDR_VTT
R804 30.1RST
MRCOMP
C396 104P
DIMMREF
C397 X_104P
C398 105P
MCH DECOUPLING CAPACITOR
VCCP
VCC1_8
VCC_AGP
VCC_DIMM
EMI
VCC5
BACK
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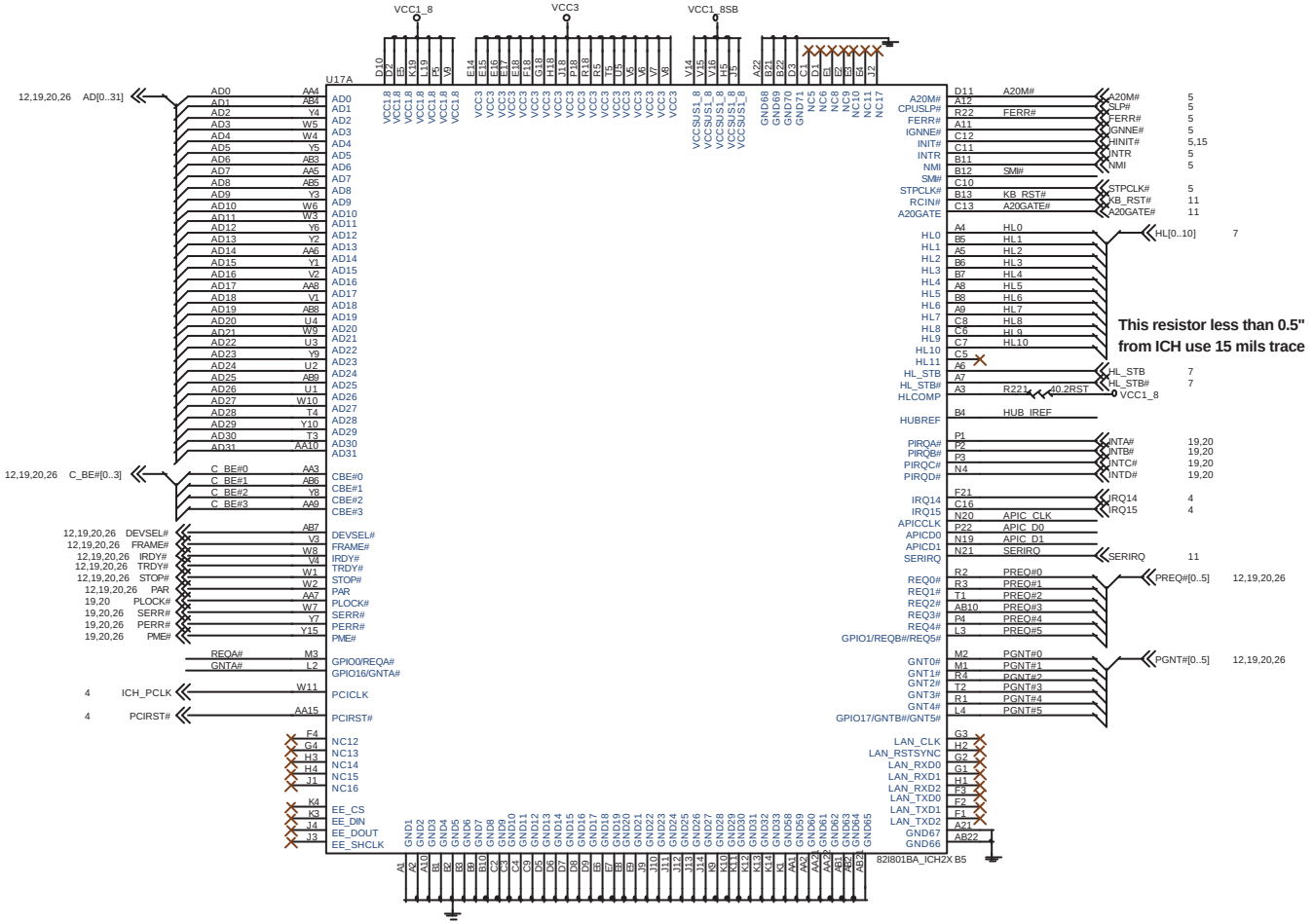
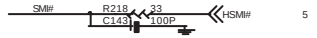
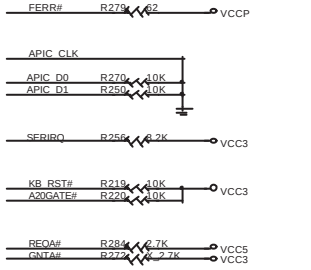
ICH2 PCI / HUB LINK / CPU/LAN/INTERRUPT SIGNALS



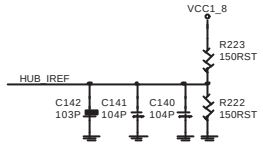
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

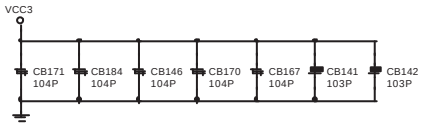


ICH2 REFERENCE VOLTAGE

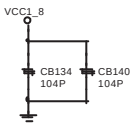


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

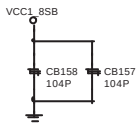
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



Distribute near the 1.8V power pin of the ICH2



Distribute near the VCC1_8SB Power pin of the ICH2

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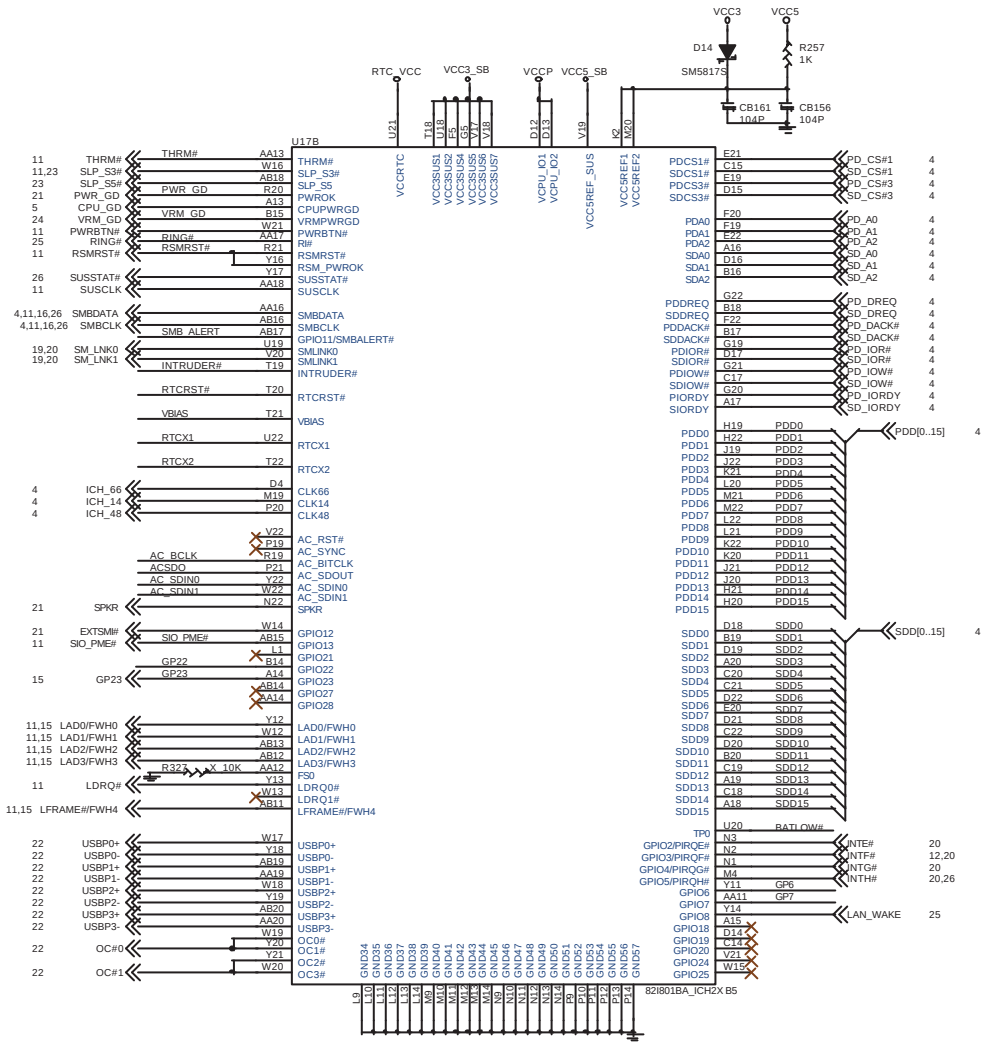
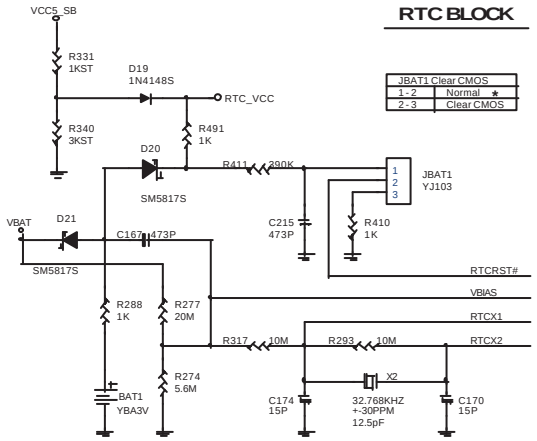
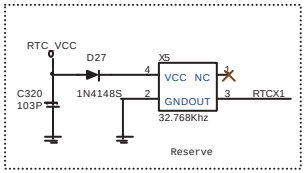
ICH2 ASIC / RTC / AC'97/GPIO/LPC/USB/IDE SIGNALS

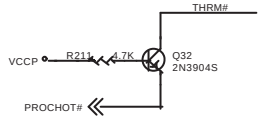


RTC BLOCK

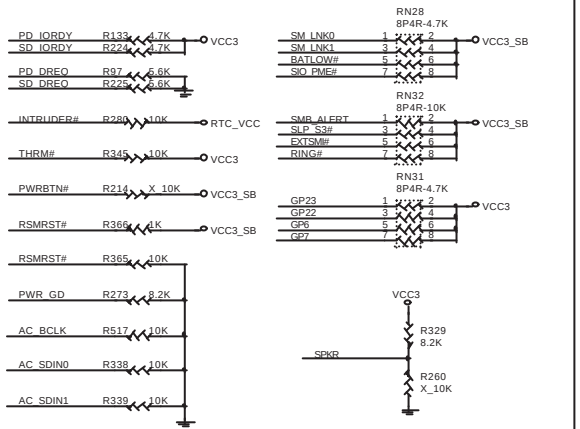




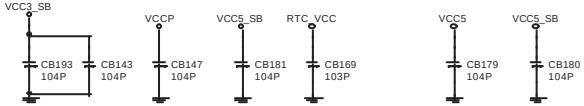
PROCHOT BLOCK



ICH2 STRAPPING RESISTORS

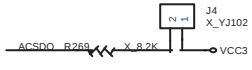


ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

CPU ratio safe mode strapping



Short	Safe Mode
Open	Normal

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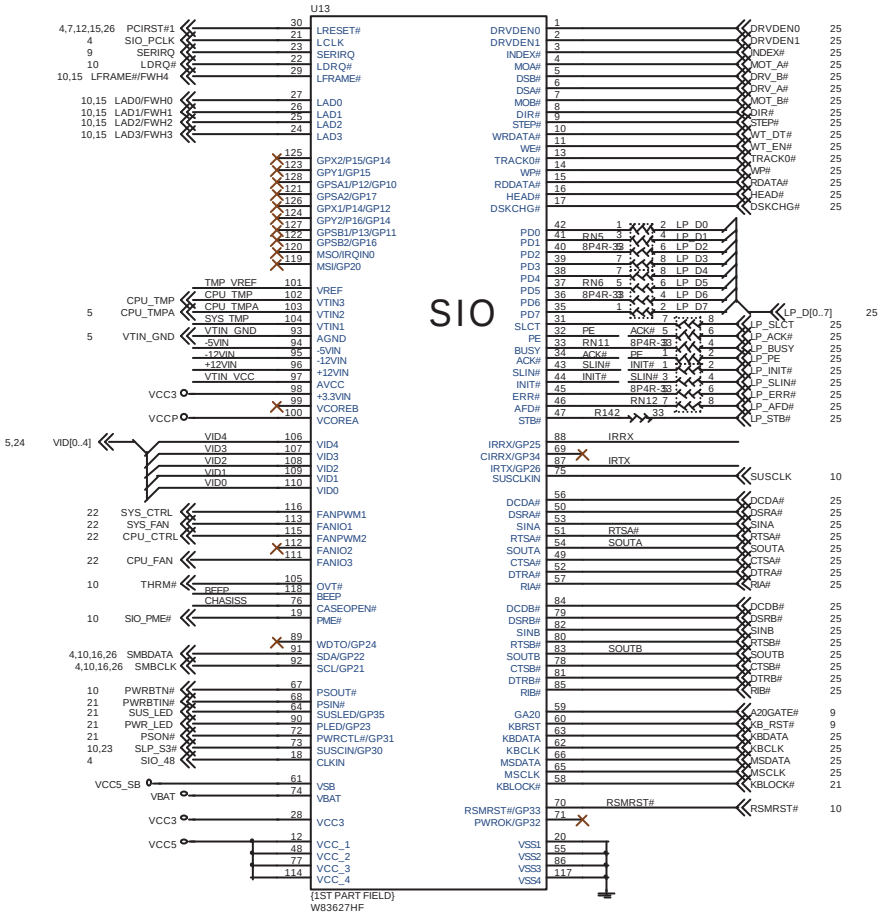
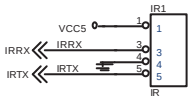
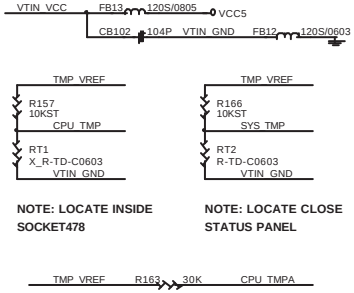
LPC SUPER I/O W83627HF



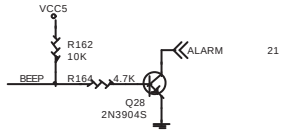
IR HEADER



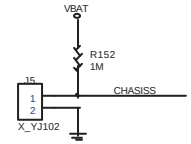
THERMAL RESISTOR BLOCK



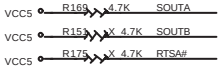
SPEAKER BLOCK



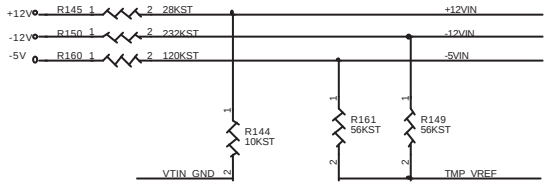
CHASISS INTRUSION HEADER



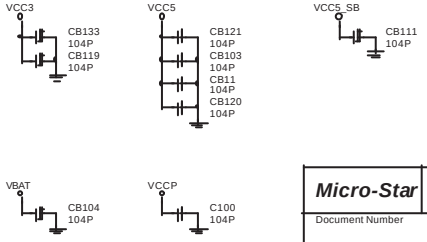
SUPER I/O STRAPPING RESISTOR



SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default



DECOUPLING CAPACITOR



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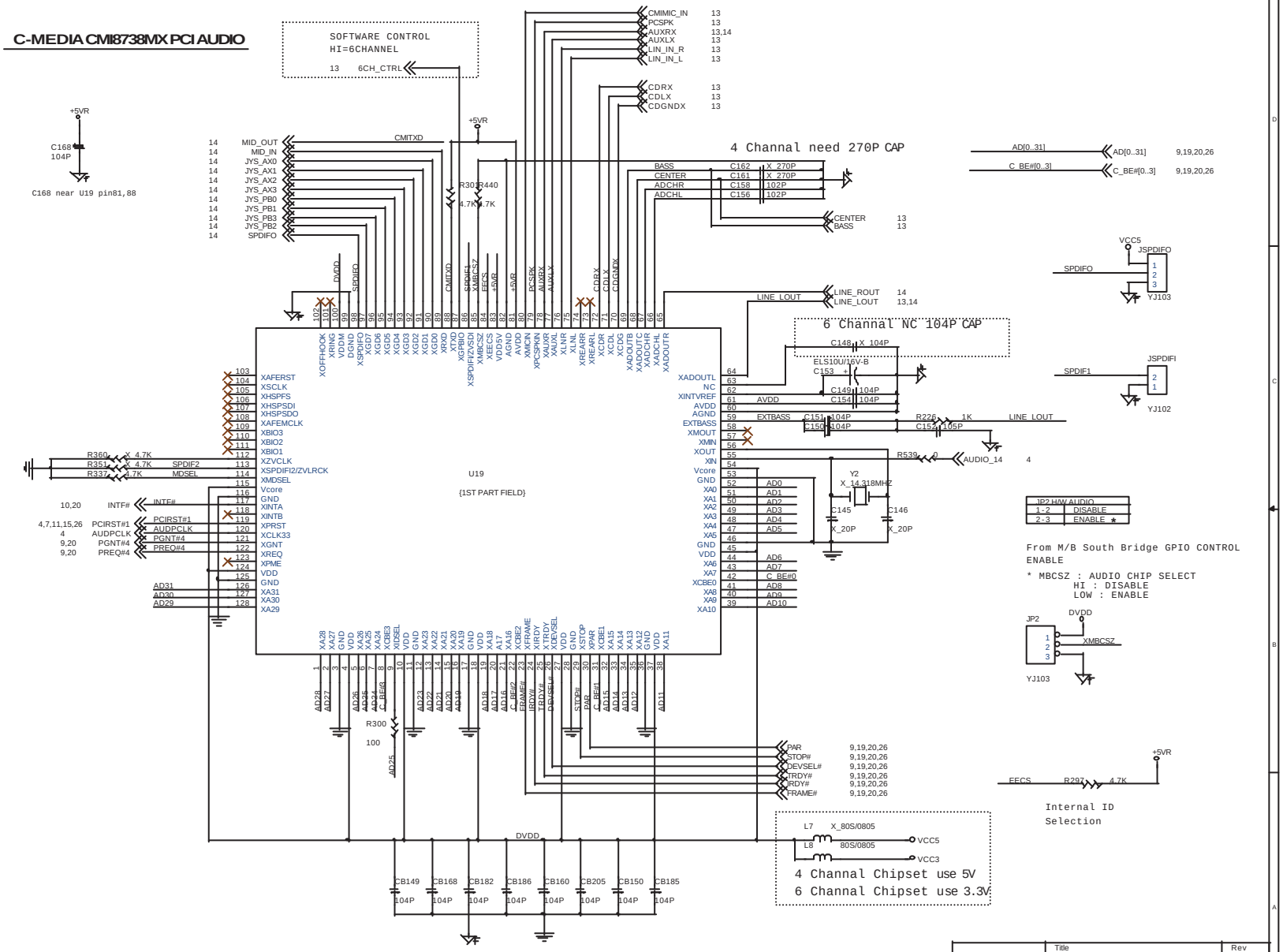
C-MEDIA CMI8738MX PCI AUDIO



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: CMI8738 PCI AUDIO		
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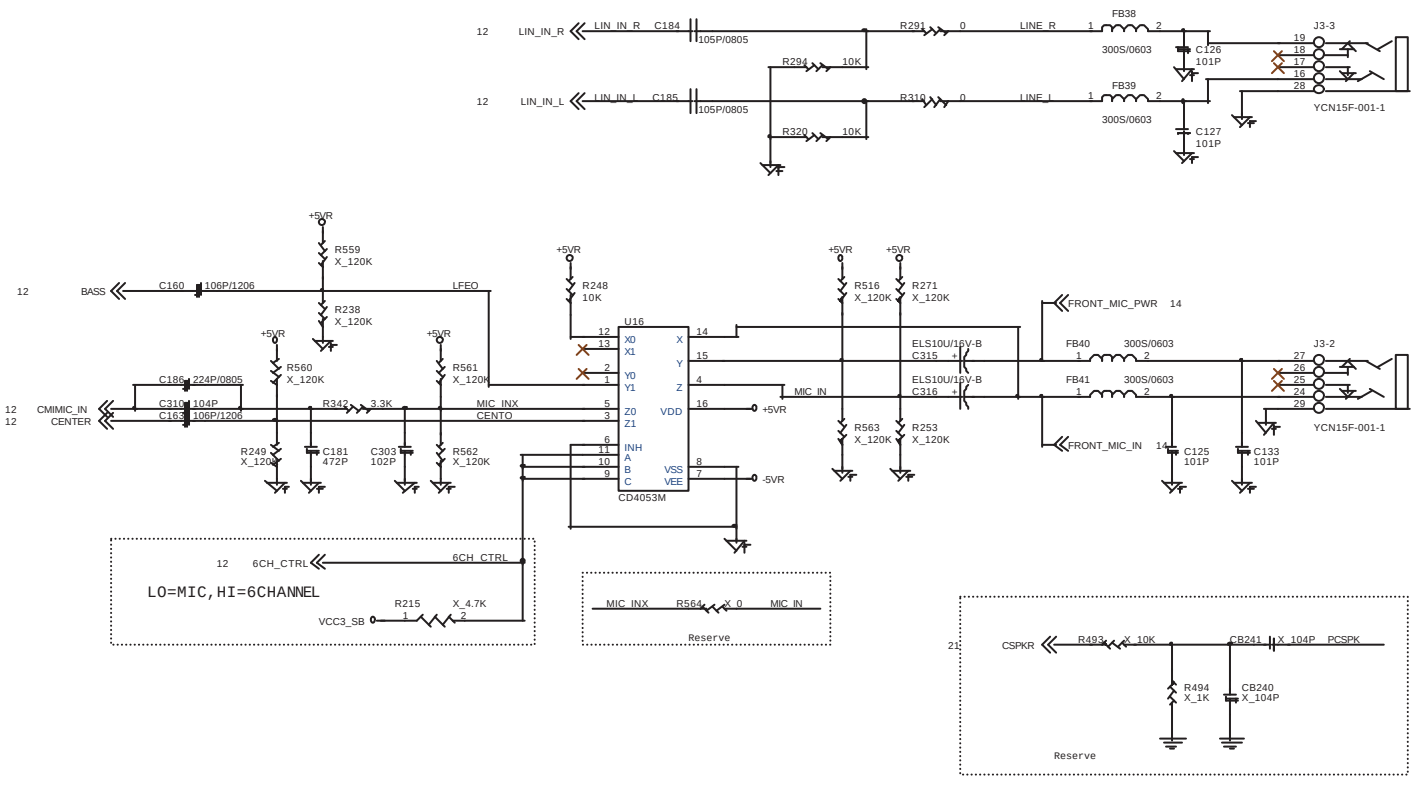
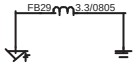
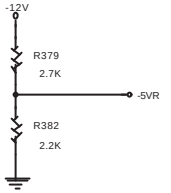


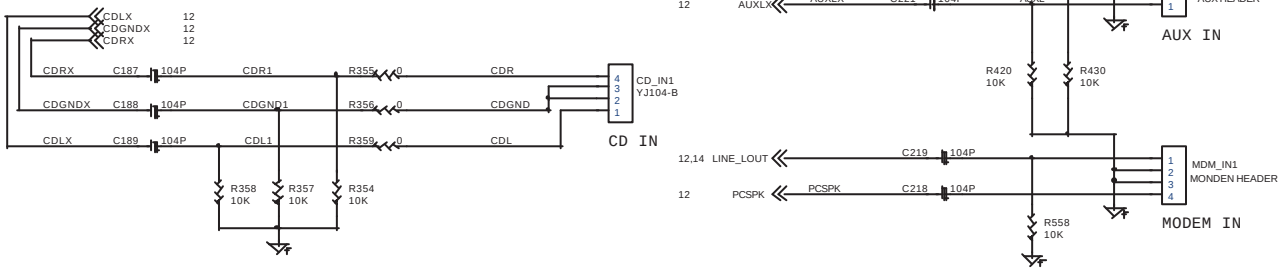
DECOUPLING CAPACITOR

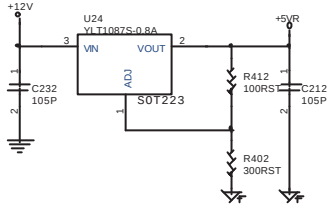


AUDIO CODE REGULATORS



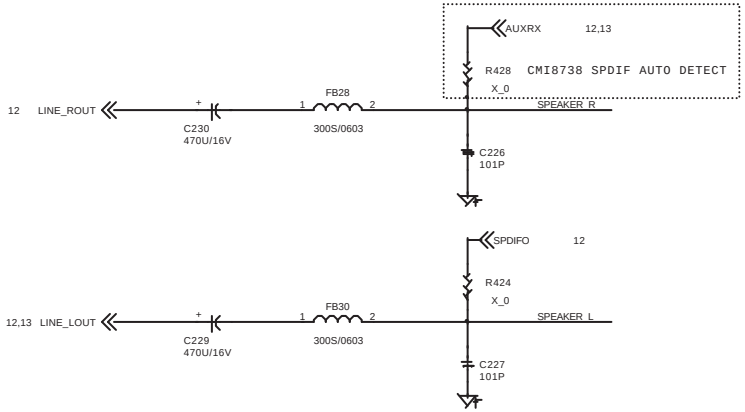
AUDIO CODE CD / AUX /MODEMINHEADERS



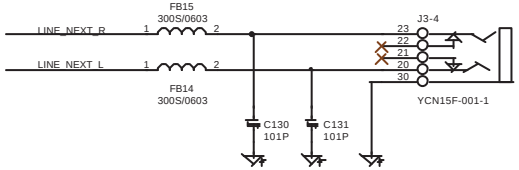


Micro-Star	Title: MS-6549	Rev: 00B	
Document Number: 6 CHANNEL CONTROL			
Last Revision Date: Thursday, November 29, 2001	Sheet 13 of 36		

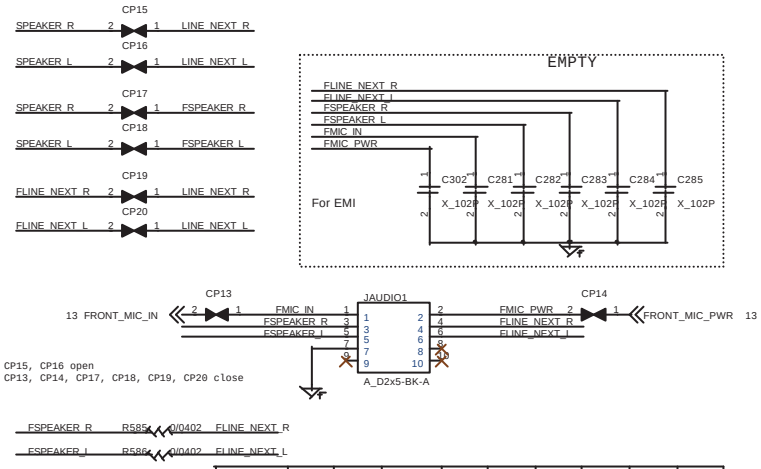
SPEAKER OUT CIRCUIT



SPEAKER OUT JACK

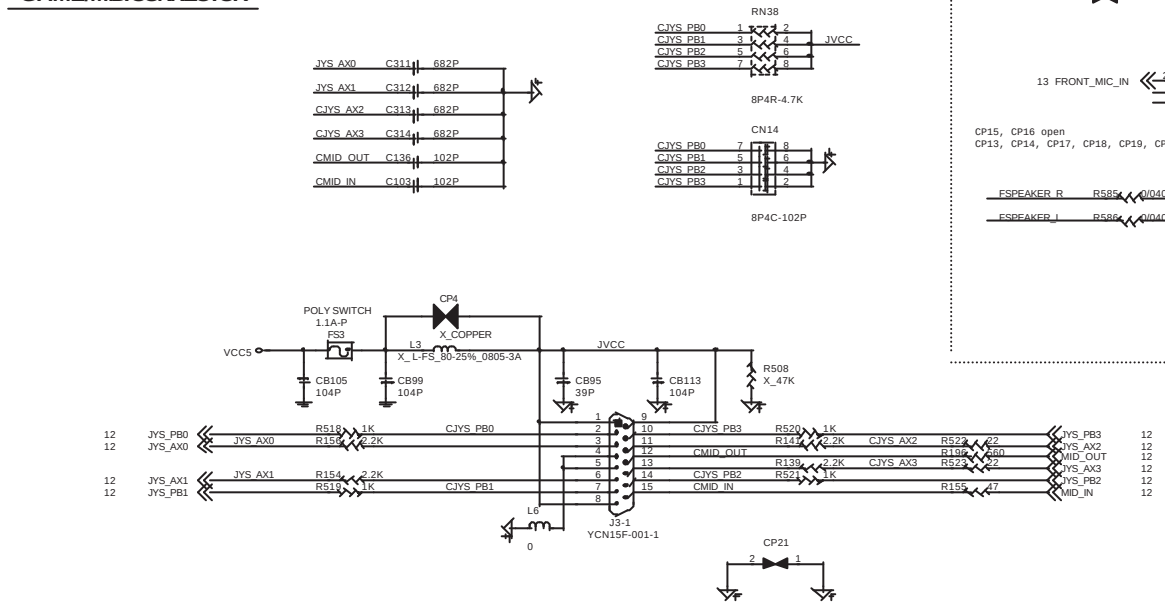


FOR MSI INTERNALHEADER



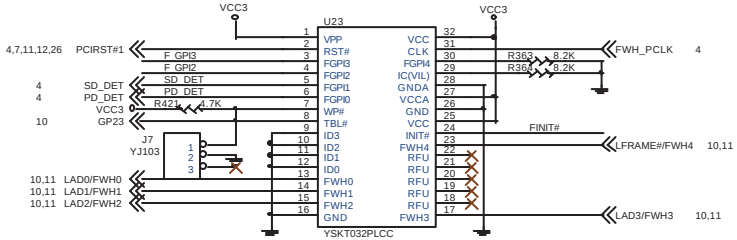
Part	R585	R586	Jaudio1	C281	C282	C283	C284	C285	C302
Stardand	0	0	X	X	X	X	X	X	X
Opt:A	X	X	0	X	X	X	X	X	X

GAME/MIDI CONNECTOR



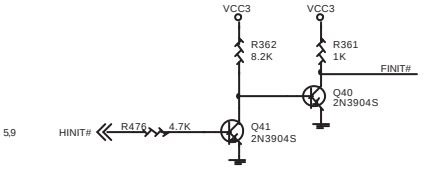
Micro-Star	Title: MS-6549	Rev: 00B
Document Number: Front Audio & GAME		
Last Revision Date: Tuesday, November 27, 2001	Sheet 14 of 36	

FirwareHub(FWH)

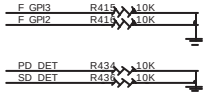


J7 BIOS Update	
1-2	Locked
2-3	Unlocked *

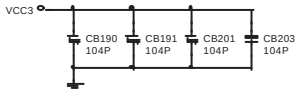
FWH INIT Signal Voltage Translation Block



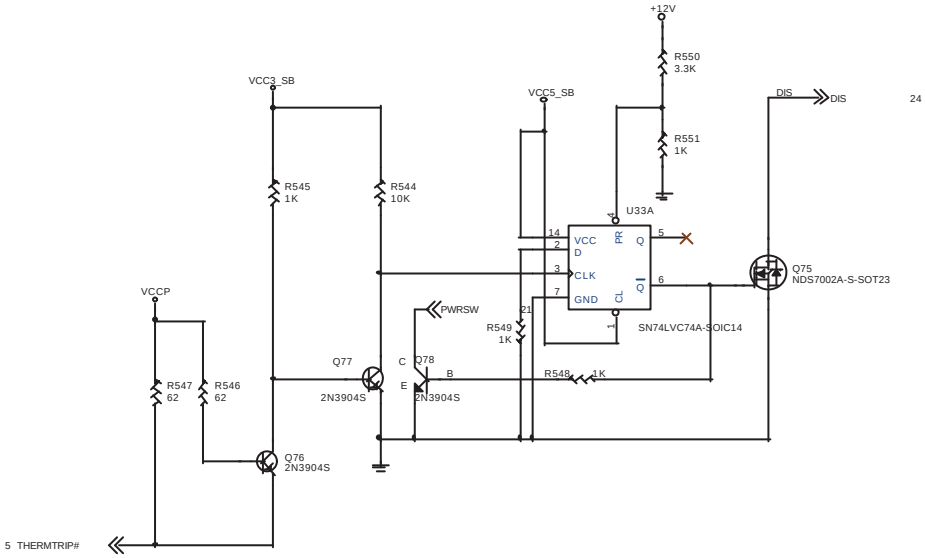
FWH RESISTORS



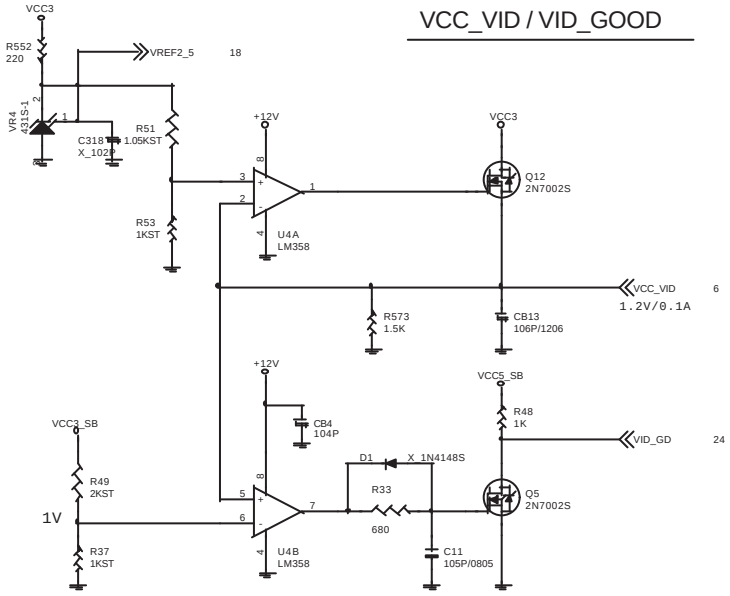
FWH DECOUPLING CAPACITORS



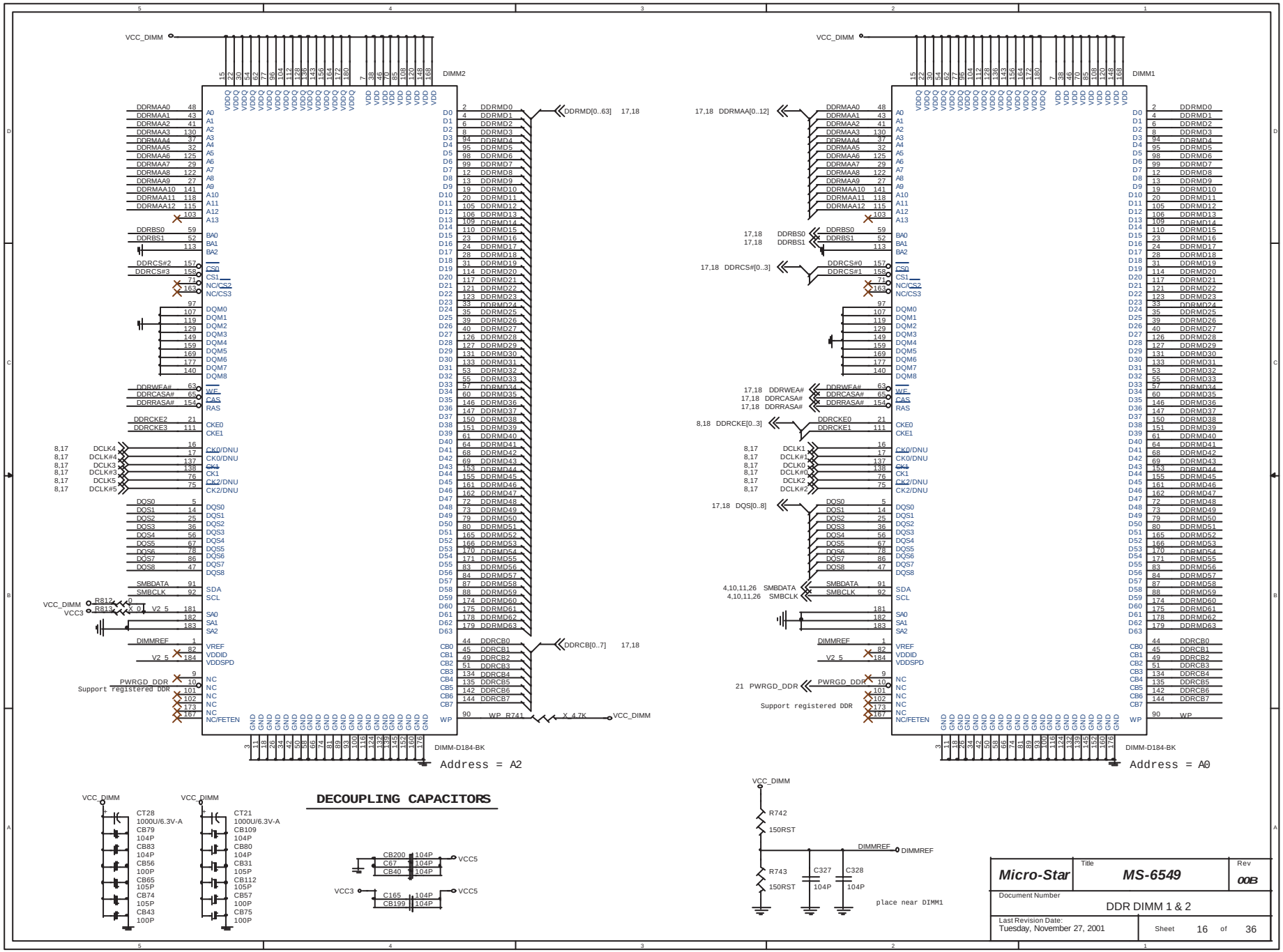
Thermtrip#



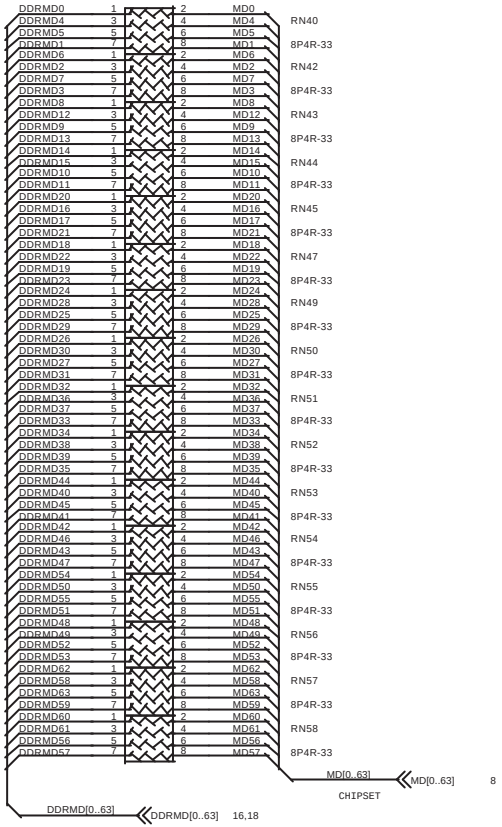
VCC_VID / VID_GOOD

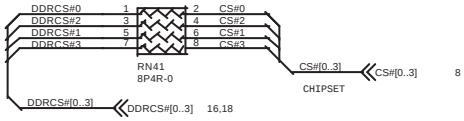


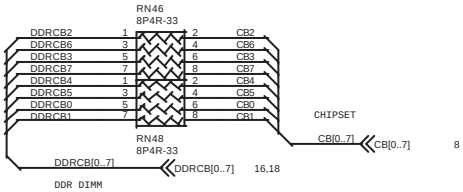
Micro-Star	Title: MS-6549	Rev: 00B
	Document Number: FWH & VCC/VID Good	
Last Revision Date: Wednesday, November 28, 2001	Sheet 15 of 36	

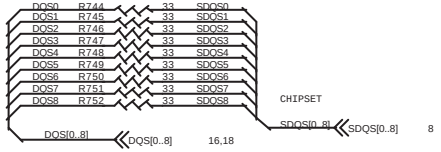

VCC_DIMM
DIMM2
DIMM-D184-BK
Address = A2
VCC_DIMM
DIMM1
DIMM-D184-BK
Address = A0
DECOUPLING CAPACITORS
CT28 1000U/6.3V-A
CB79 104P
CB83 104P
CB56 100P
CB65 105P
CB74 105P
CB43 100P
CT21 1000U/6.3V-A
CB109 104P
CB80 104P
CB31 105P
CB112 105P
CB57 100P
CB75 100P
CB200 104P
C67 104P
CB40 104P
C165 104P
CB199 104P
VCC5
VCC3
R742 150RST
R743 150RST
C327 104P
C328 104P
DIMMREF
place near DIMM1
Micro-Star
MS-6549
00B
DDR DIMM 1 & 2
Tuesday, November 27, 2001
Sheet 16 of 36

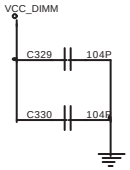
DDR DAMPING

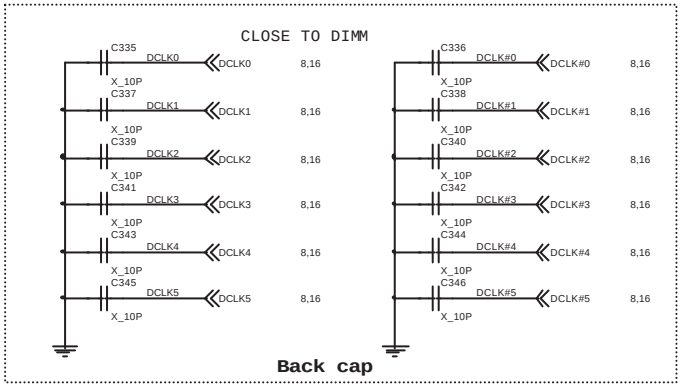


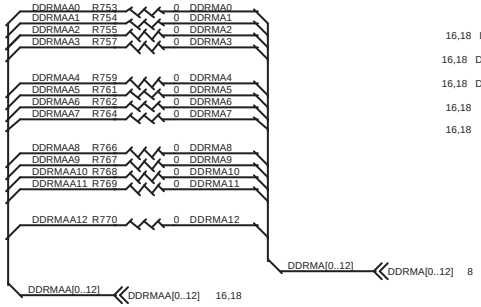


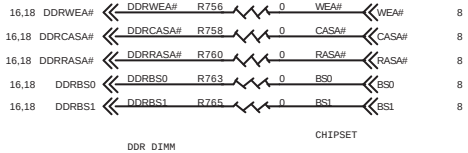












Micro-Star	Title: MS-6549		Rev: 00B
Document Number: DDR DAMPING			
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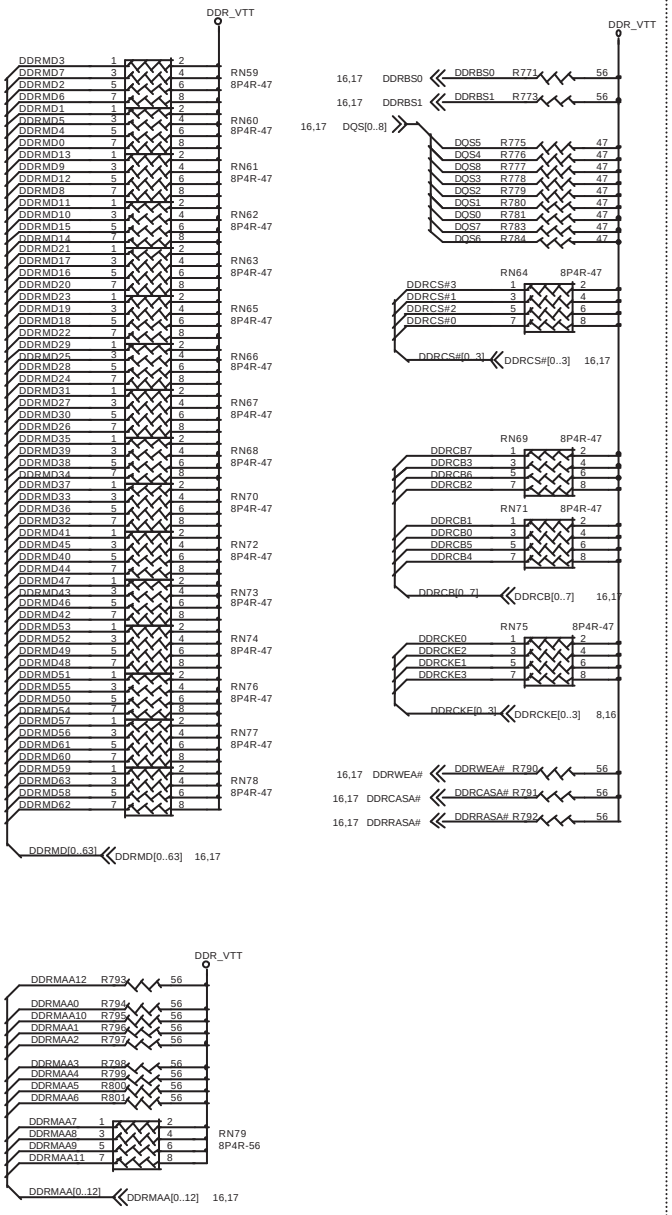
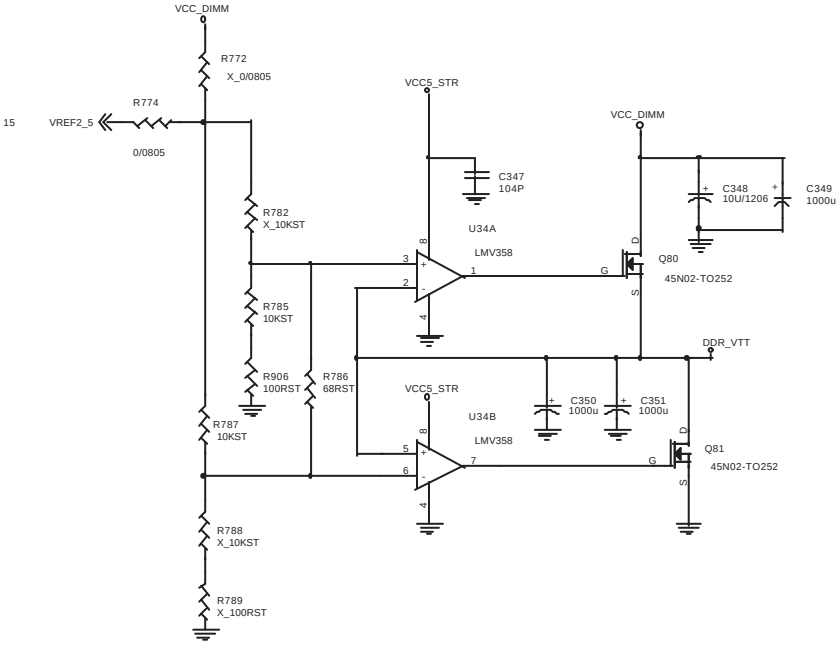
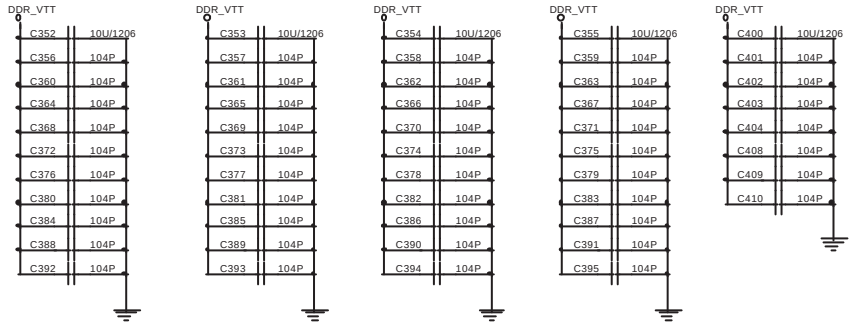
DDR TERMINATION



DDR POWER





Micro-Star	Title: MS-6549	Rev: 00B
Document Number: DDR TERMINATION & POWER		
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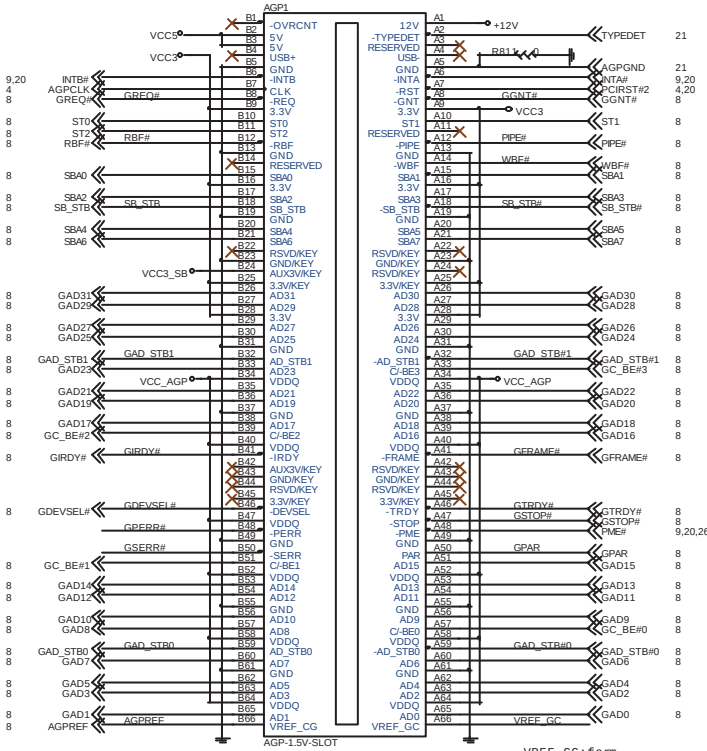
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

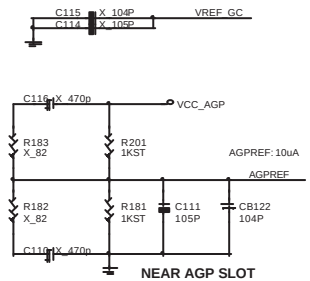


AGP Slot Imax

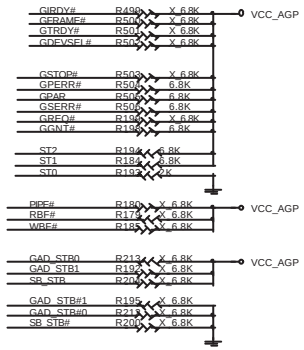
VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#

AGP SIGNAL REFERENCE CIRCUIT



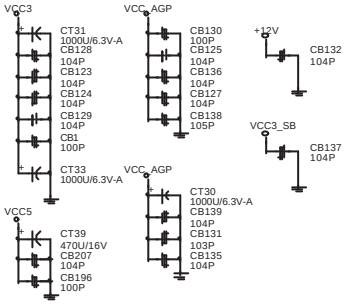
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BEFOLLOWING.

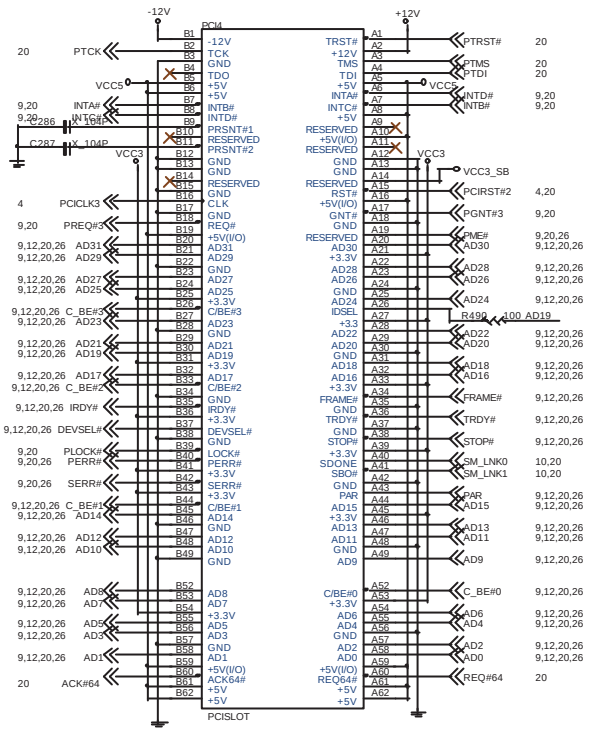
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Part	PCI4	R490
Stardand	0	0
Opt:A	X	X

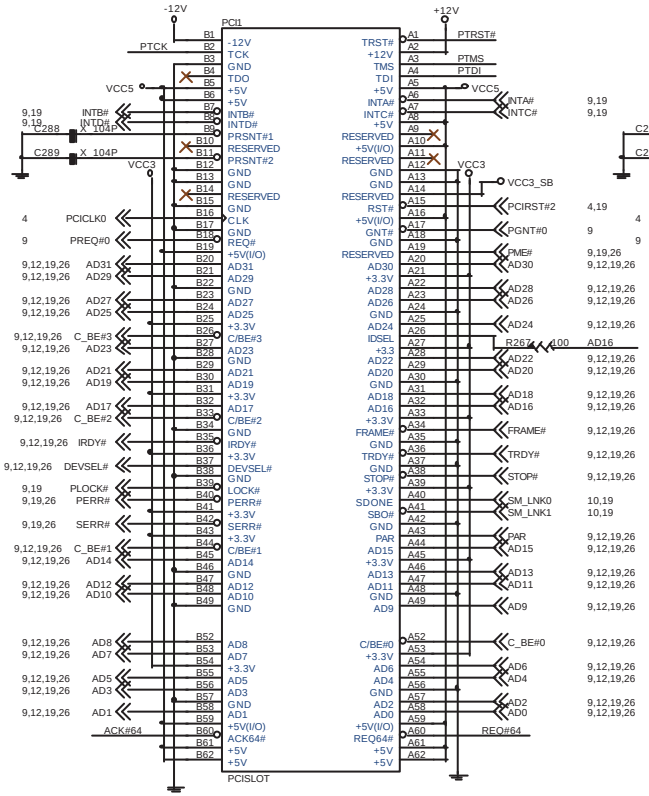
PCI SLOT 4 (PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER = PREQ3
INTD#

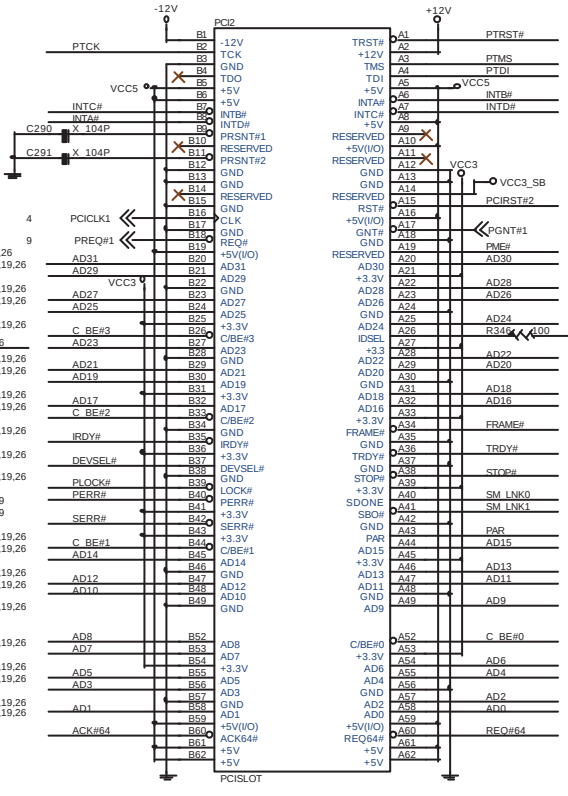
Micro-Star	Title: MS-6549		Rev: 00B
	Document Number: AGP Slot & PCI SLOT4		
	Last Revision Date: Tuesday, November 27, 2001	Sheet 19 of 36	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



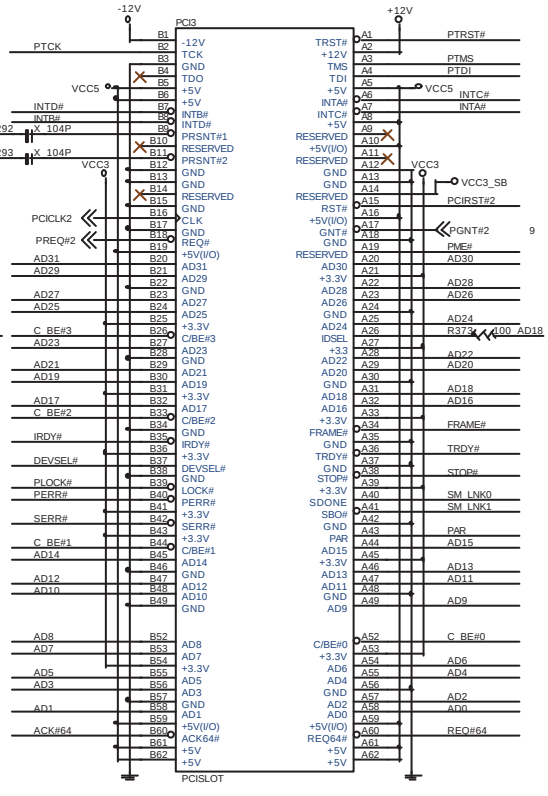
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



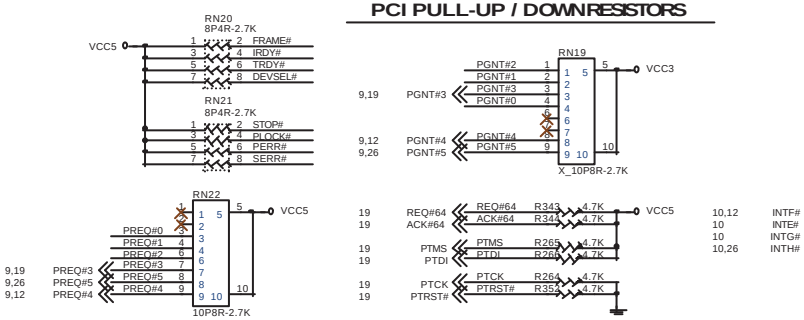
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

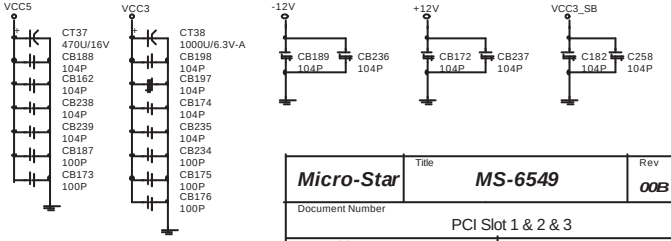


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: PCI Slot 1 & 2 & 3		
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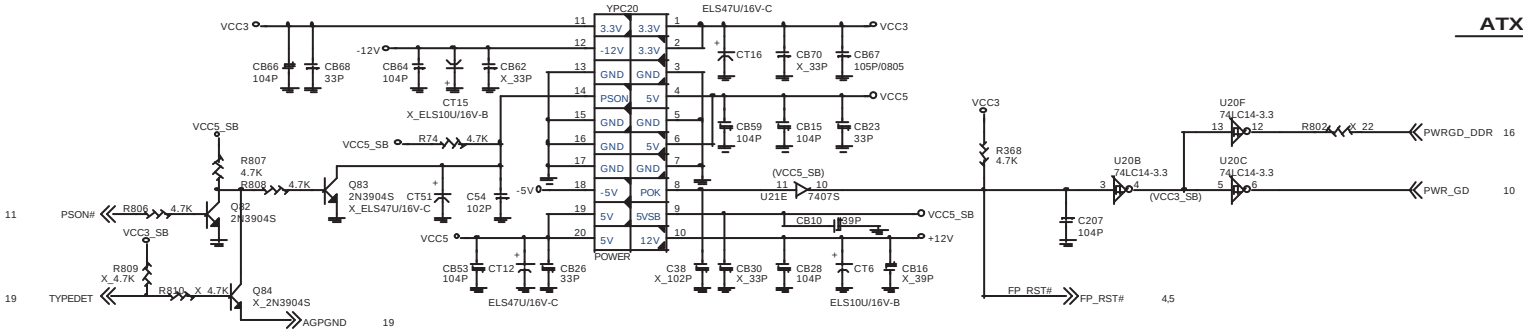
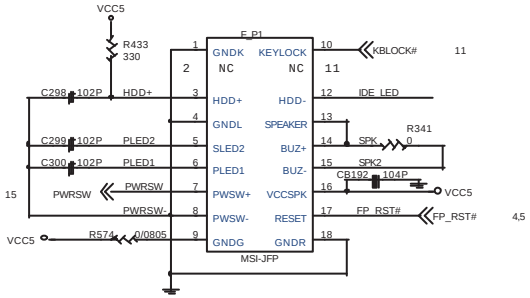
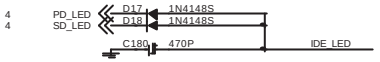
ATX CONNECTOR

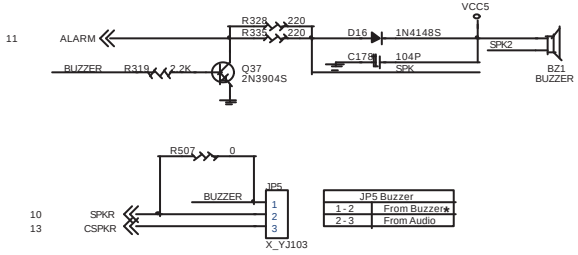


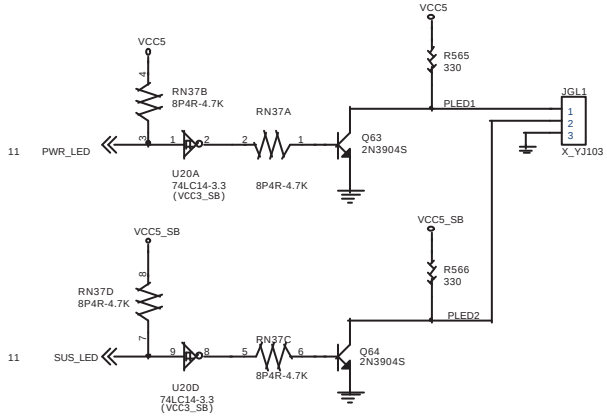
BrookdaleFRONTPANEL-M

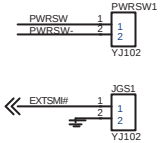




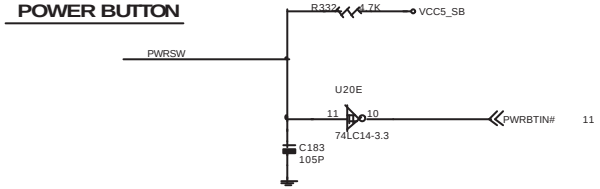
SPEAKER







POWER BUTTON



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: Front Panel & Connector		
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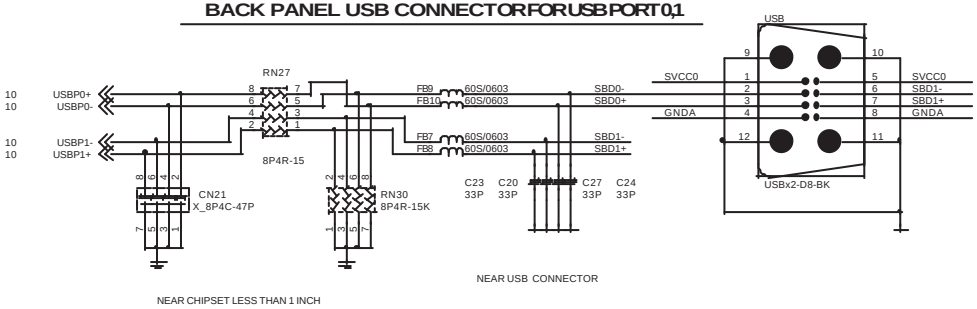
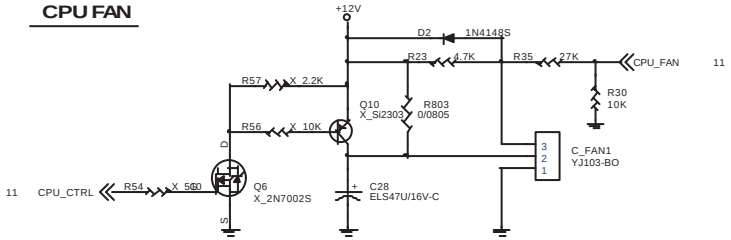
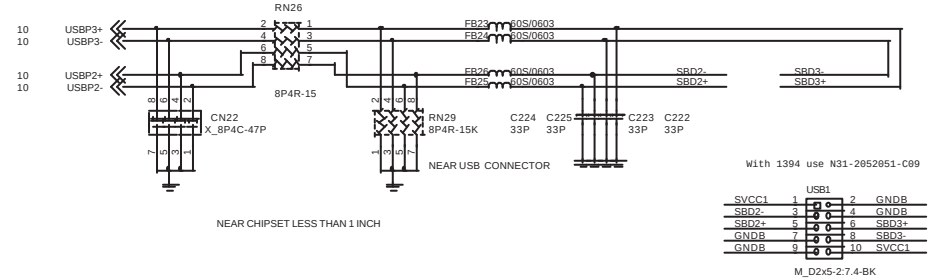
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



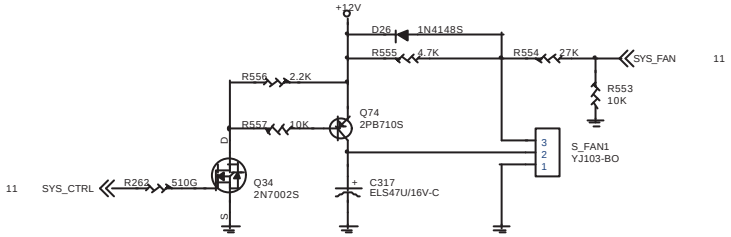
CPU FAN



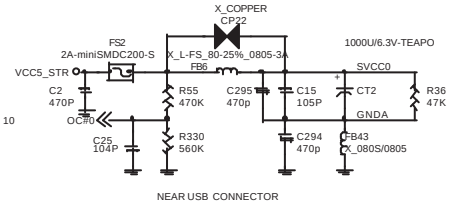
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



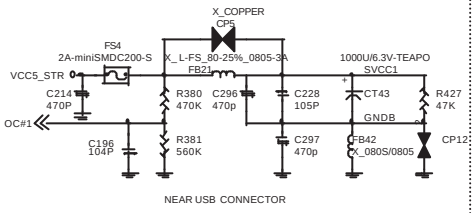
SYSTEM FAN1



POWER CIRCUIT FOR USB PORT 0,1



POWER CIRCUIT FOR USB PORT 2,3



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: USB & FAN Connectors		
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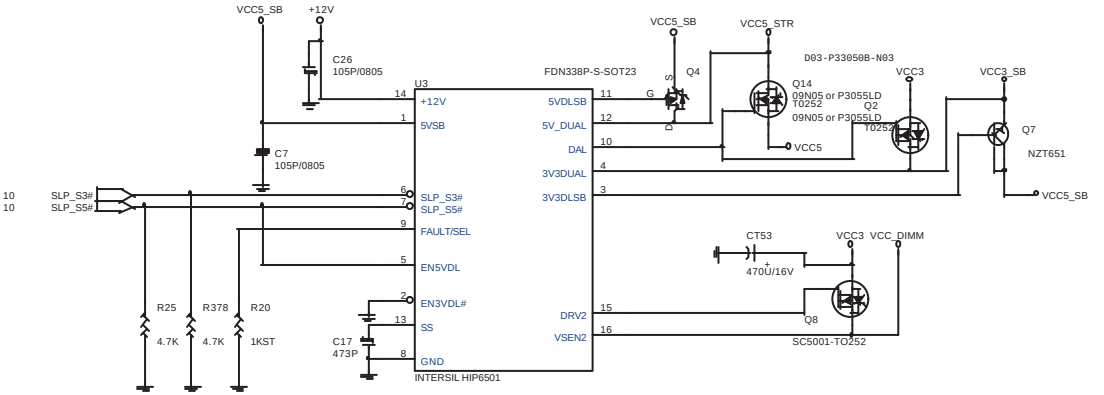
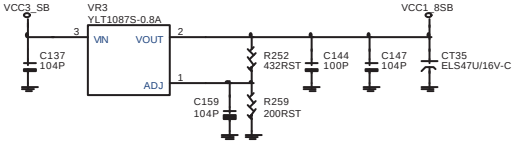
POWER TRANSLATOR

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V



1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH-SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

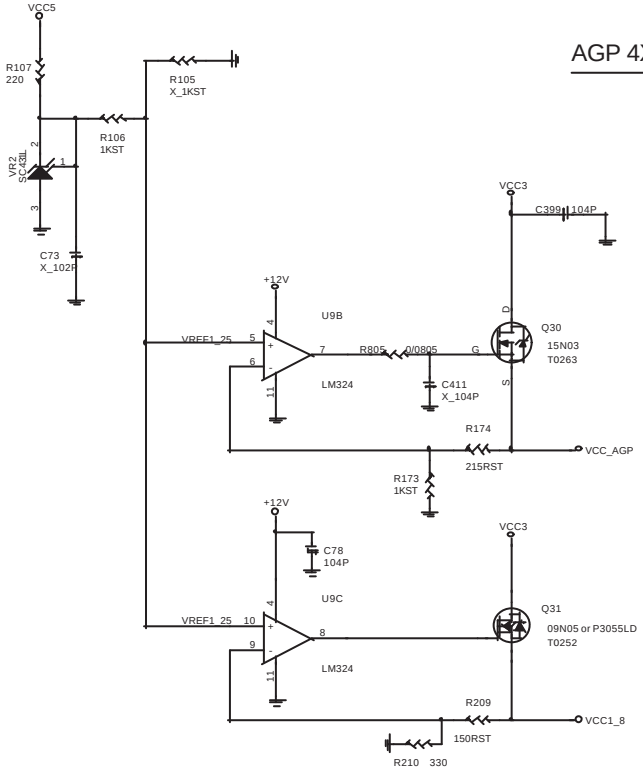
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

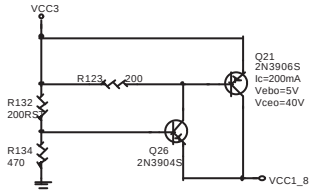
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

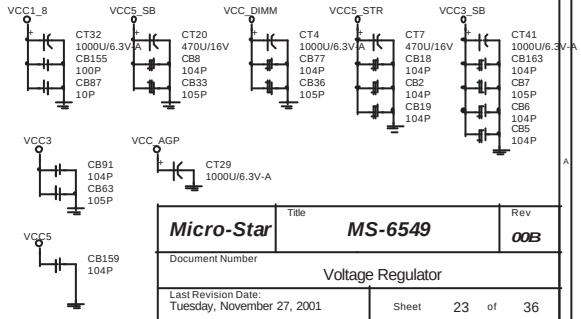
AGP 4X 1.5V POWER TRANSLATOR



1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: Voltage Regulator		
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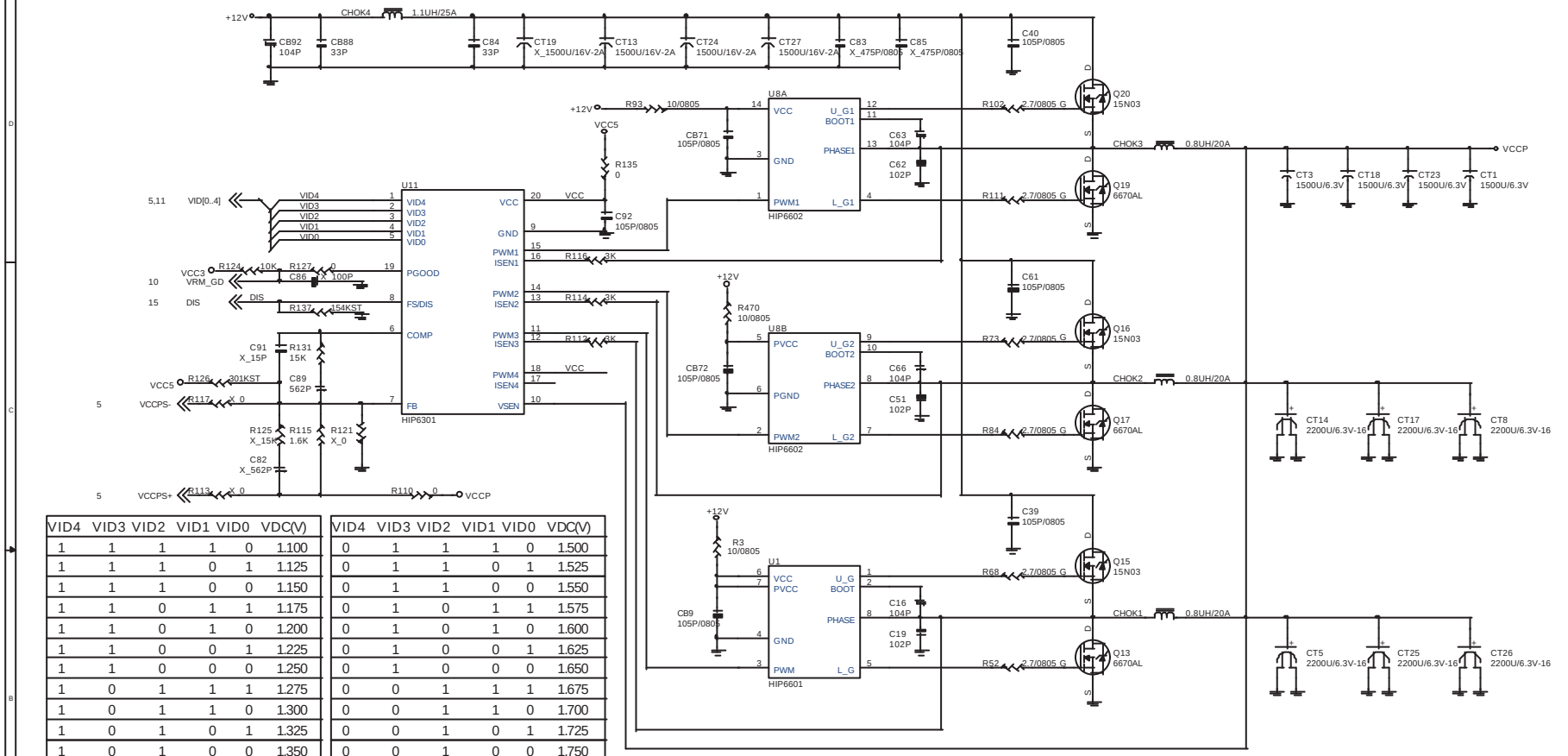
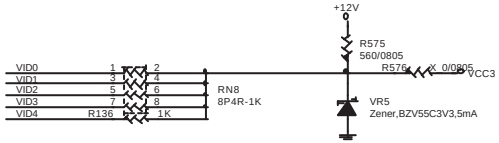


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

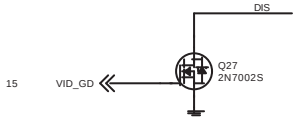
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

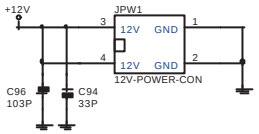
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWMGOOD

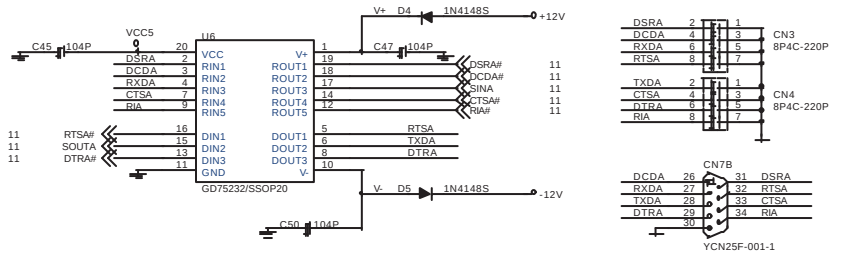


ATX12V POWERCONNECTOR

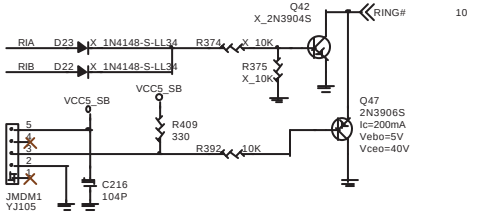


Micro-Star	Title: MS-6549	Rev: 00B
Document Number: VRM 9.2		
Last Revision Date: Wednesday, November 28, 2001	Sheet 24 of 36	

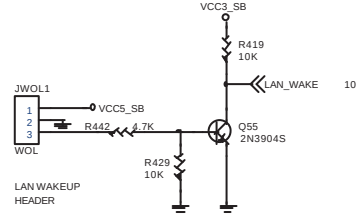
SERIAL PORT1



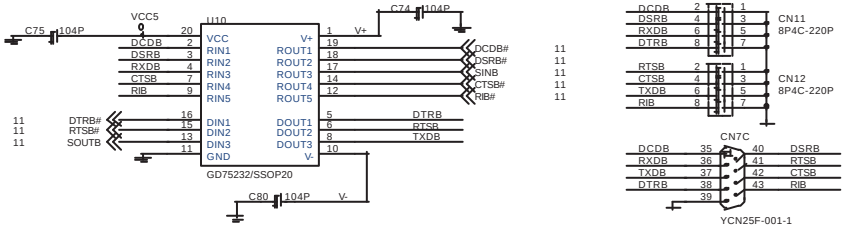
MODEM RING BLOCK



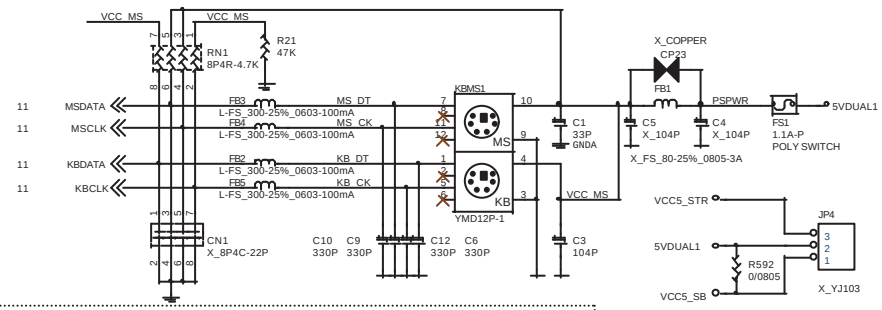
LAN WAKEUP BLOCK



SERIAL PORT2

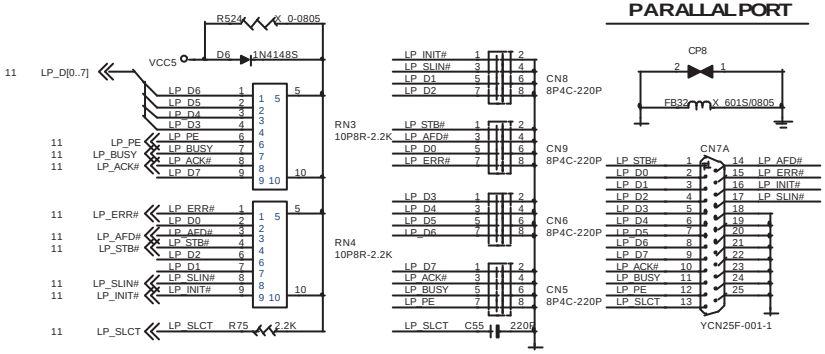


PS2 KEYBOARD & MOUSE CONNECTOR

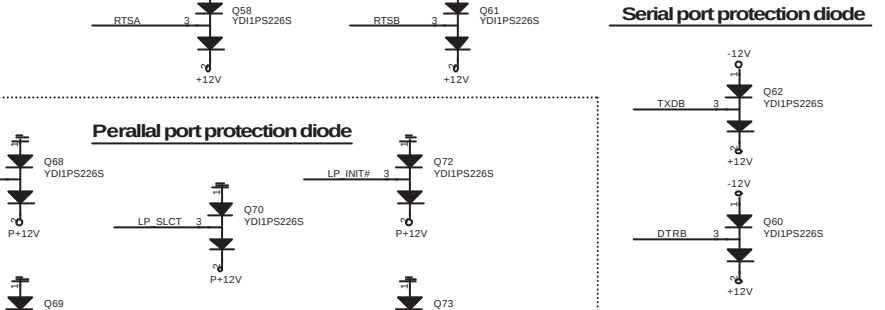


JP4	K/M power on wake up
1-2	S3,S5 both work
2-3	Only S3 work

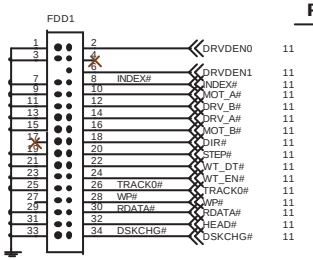
PARALLAL PORT



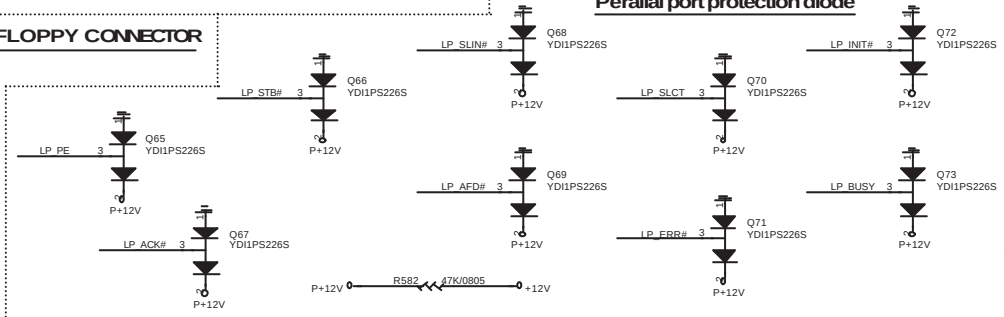
Serial port protection diode



FLOPPY CONNECTOR



Perallal port protection diode



Micro-Star	Title: MS-6549	Rev: 00B
	Document Number: IO Connector	
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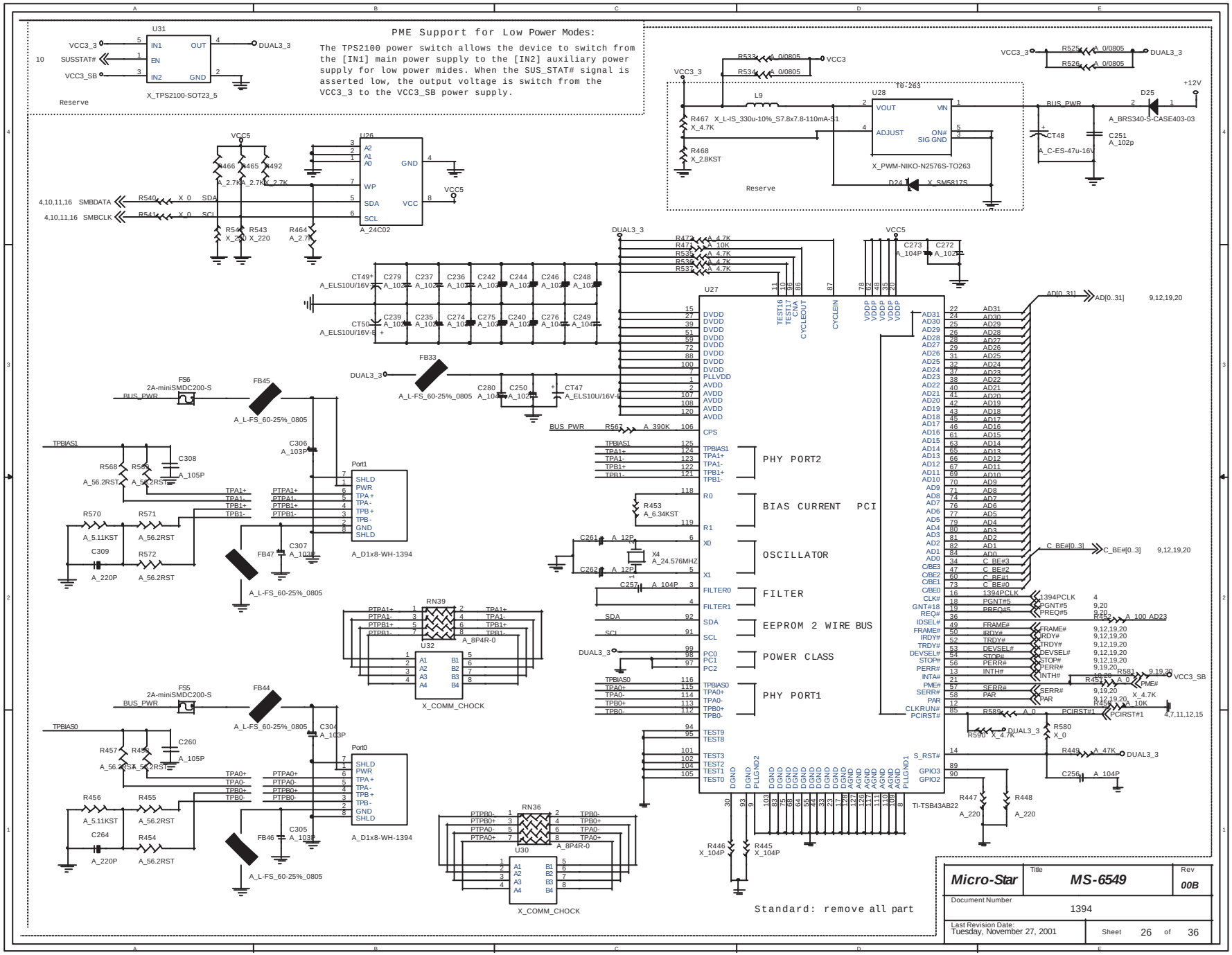
PME Support for Low Power Modes:
The TPS2100 power switch allows the device to switch from the [IN1] main power supply to the [IN2] auxiliary power supply for low power mides. When the SUS_STAT# signal is asserted low, the output voltage is switch from the VCC3_3 to the VCC3_SB power supply.
U31
X_TPS2100-SOT23_5
Reserve
U28
X_PWM-NIKO-N2576S-TO263
X_SM5817S
A_BRS340-S-CASE403-03
U26
A_24C02
U27
TI-TSB43AB22
PHY PORT2
BIAS CURRENT PCI
OSCILLATOR
FILTER
EEPROM 2 WIRE BUS
POWER CLASS
PHY PORT1
Port1
Port0
A_D1x8-WH-1394
X_COMM_CHOCK
Standard: remove all part
Micro-Star
MS-6549
00B
Document Number
1394
Last Revision Date:
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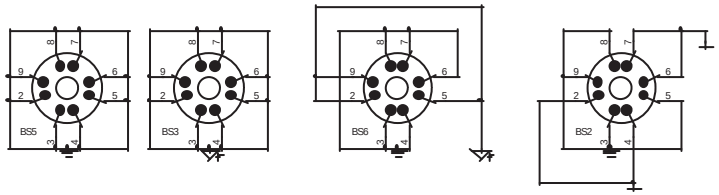
Jumper Setting & Connector Setting

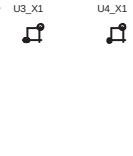
Jumper	Description	
J1	SDR SIMULATION	
J2	AGP SIMULATION	
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	
J4	AC_SDOUT HEADER	
J5	CHASISS INTRUSION HEADER	
J7	BIOS function	
1-2	Normal	(Default)
2-3	Configuration Mode	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
IR1	IR HEADER	
CD_IN1	CDROM HEADER (ATAPI)	
AUX_IN1	AUDIO AUX HEADER (ATAPI)	
MDM_IN1	TELEPHONY HEADER (ATAPI)	
JP2	H/W AUDIO SELECT HEADER	
1-2	Disable	
2-3	Enable	(Default)
JP4	K/M Power on	
1-2	S3,S5 both work	(Default)
2-3	Only S3 work	
JP5	Buzzer	
1-2	From Buzzer	(Default)
2-3	From Audio	

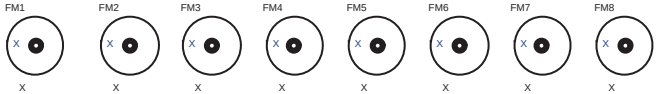
Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
PCI4	PCI Slot4
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
CPU_FAN	CPU FAN HEADER
SYS_FAN	System FAN HEADER
USB	USB REAR CONNECTOR
USB1	USB FRONT HEADER
POWER	ATX Power
F_P1	Front Panel
JPW1	ATX12V Power
JSPDIFO	SPDIF_OUT
JSPDIFI	SPDIF_IN
JAUDIO1	Front AUDIO HEADER

Micro-Star	Title: MS-6549	Rev: 00B
Document Number: JUMPER SETTING		
Last Revision Date: Tuesday, November 27, 2001	Sheet 27 of 36	

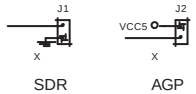
PCB OTHER COMPONENT



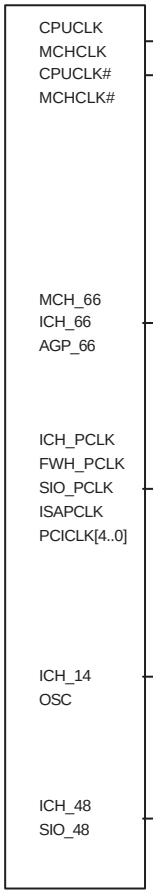




SIMULATION TRACE



Micro-Star	Title: MS-6549	Rev: 00B
Document Number: MANUAL		
Last Revision Date: Tuesday, November 27, 2001	Sheet 28 of 36	



DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

Micro-Star	Title: MS-6549	Rev: 00B
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Last Revision Date: Tuesday, November 27, 2001	Sheet 29 of 36	

Norminal 4-layer Board Stackup

1.Board spec.

Description	Target Value	notes
Micro-stripline Er	4.2 - 4.5	
Trace Thickness	1.3 - 1.42 mils	1
Board Thickness	62 mils	
Material	FR4	
Fab Construction	4 layer	

2.Board each layer thickness .

Description	Target Value	Tolerance(+/- mils)
(Layer 1) Top layer	1.4 mil	See notes 1
Perpreg	4.0 mil	0.3
(Layer 2) Power layer	1.4 mil	0.2
Core	48 mil	5
(layer 3) Ground layer	1.4 mil	0.2
Perpreg	4.0 mil	0.3
(layer 4) Bottom layer	1.4 mil	See notes 1

3.Via Stack

Description	Target Value
Via Pad	26 mil
Via Anti-Pad	40 mil
Via Finiched hole	14 mil
Signal Pad(BGA)	20 mil

4.CPU GTL+ bus impedance = 50 Ohm(7mil trace width)

5.CPU asynchronous GTL+,AGP,Memory and Hub-link bus impedance = 60 Ohm(5mil trace width)

CPU Routing Guidelines

1.CPU data synchronous signal groups and the associate strobe

Signals	Associated Strobe
REQ[4:0]#,A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

***All the system bus signals must be referenced to GND**

2.Trace edge to edge spacing greater than 3:1(about 12 mils) versus trace to GND plane height ratio

3.2" - 10" from pin to pin and each data signal group should be routed to same length within +/-100 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

4.A pair data strobe should be routed to the same length within +/- 25mils, if one strobe switch layers, and another switch layer in the same manner.Additional CPU,MCH internal trace length(See Table-1)must be inculded.The calculation trace length follow (Table-2)

5.2" - 10" from pin to pin and each address signal group should be routed to same length within +/-200 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

6.Internal adderss strobe trace length(See Table-1) of CPU,MCH must be inculded.The calculation trace length follow (Table-2)

Table - 1

CPU package length + PCB trace length + MCH package length = Total length					
L1	+	L2	+	L3	= Total L4

7.Keep the voltage divider with in 1.5 inches of GTLREF pin.and do not allow the GTLREF routing to splits or discontinuities power plane.

8.CPU Asynchronous GTL+ bus connect to ICH2 trace length

Signal Name	Trace Spacing	Trace Length	Pull-up Resistor
FERR#	7 MIL	1"-12"	62 Ohm +/- 5%
PROCHHOT#	7 MIL	1"-17"	62 Ohm +/- 5%
THERMTRIP#	7 MIL	1"-17"	62 Ohm +/- 5%
A20M#	7 MIL	1"-12"	None
IGNNE#	7 MIL	1"-12"	None
LINT[1:0]	7 MIL	1"-12"	None
SLP#	7 MIL	1"-12"	None
SMI#	7 MIL	1"-12"	None
STPCLK#	7 MIL	1"-12"	None
INIT#	7 MIL	1"-17"	None
PWRGOOD	7 MIL	1"-12"	300 Ohm +/- 5%

9.CPU BCLK,BCLK# should be routed as a differential pair with 7 mil trace and 7 mil spacing between them,2.5" to 10" pin to pin common clock lengths, and 25 mil spacing away form all the signal or clock.

10.DBSY#,DRDY#,TRDY#,ADS#,LOCK#,BNR#,HIT#,HITM#,BPRI#,DEFER#,BR0#,RESET# and RS[2:0]# CPU signal trace length around 2.5" to 10"

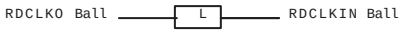
11.CPU and MCH package length

SDRAM Routing Guidelines

5.Feedback - RDCLKO,RDCLKIN routing rule

2 or 3 DIMM feedback layout guideline

Signal	Length	Width	Trace Spacing
Trace L	50 mils	7 mil	5 mil



DDR-SDRAM Routing Guidelines

1.DDR bus reference plane stack-up

PCB Layer	Description
Layer 1	Signal
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Power / Signal

***All the memory bus signals must be referenced to GND**

2.DDR signal groups

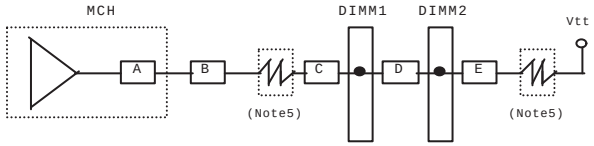
Group	Signals
Data	SDQ[63:0],SCB[7:0],SDQS[8:0]
Command	SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE#
Control	SCKE[3:0],SCS#[3:0]
Clock	SCK[5:0],SCK#[5:0]
Feedback	RCVENOUT#,RCVENIN#

3.SDQ[63:0],SCB[7:0],SDQS[8:],SCK/SCK#[5:0]routing rule

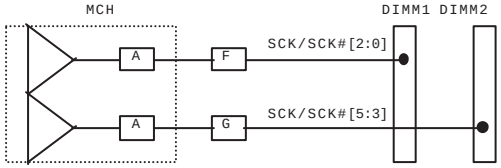
Signal	Length A	Length B	Length C	Length D	Length E	Width	Spacing	Routing Layer
SDQ[63:0] SCB[7:0] SQDS[8:0]	Package length	2.0" - 5.0"	Max = 0.5"	0.3' - 0.5"	0.1" - 0.8"	5 mil	(Note2)	Top
(Note1)	DIMM 1 = A + B + C = X DIMM 2 = A + B + C + D = X + D							
SCK/SCK#[2:0]	Package length	B+C+2">= Length F >= B+C+1" 2.0" - 6.5"		None	None	5 mil	(Note4)	Bottom
	DIMM 1 = A + F =X + 1" to X + 2"							
SCK/SCK#[5:3] (Note3)	Package length	B+C+D+2">=Length G >= B+C+D+1" 2.5" - 7.0"				5 mil	(Note4)	Bottom
	DIMM 2 = A + G =X + D + 1" to X + D + 2"							

*** Package length see Table - 4**

SDQ[63:0],SCB[7:0],SDQS[8:] layout guideline



SCK[5:0] layout guideline



Note1:Each data and strobe signal group must be length matching +/- 25 mils

SDQS[X] = +/- 25 mils SDQ[X]/SCB[X] group length

Signals	Associated Strobe
SDQ[7:0]	SDQ0
SDQ[15:8]	SDQ1
SDQ[23:16]	SDQ2
SDQ[31:17]	SDQ3
SDQ[39:32]	SDQ4
SDQ[47:40]	SDQ5
SDQ[55:48]	SDQ6
SDQ[63:56]	SDQ7
SCB[7:0]	SDQ8

Note2:Trace spacing normally = 12 mils and through between DIMM 2 pin = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils

Note3:

- * SCK[X] length = SCK#[X] length
- * SCK/SCK#[2:0] routed to DIMM 0 are equal in length, and SCK/SCK#[5:3] routed to DIMM 1 are equal in 1ength

Note4:

- * Between the pair differential clock 2 signal trace spacing = 7 mils
- * Differential Trace with 2.5V copper flood spacing = 10 mils minimum
- * Serpentine spacing = 20 mils minimum
- * Differential signals breakout form MCH = 5 mil width with 7 mil differential spacing and 7 mil isolation spacing from another signal for a max of 350 mils

Note5:Data group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the command or control group signal

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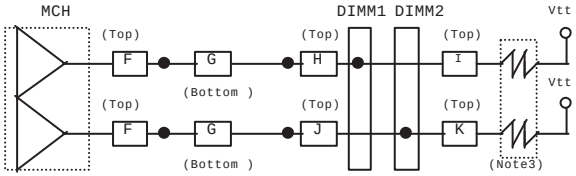
DDR-SDRAM Routing Guidelines

4.SCKE[3:0],SCS#[3:0] routing rule

DIMM 0					
Signal	Length F	Length G	Length H	Length I	Width
SCS#[1:0] SCKE[1:0] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils (Note2)	0.4" - 1.3"	5 mils
Total lenght	DIMM0 SCK/SCK#[2:0] length = X" DIMM0 SCS#/SCKE length = F + G + H =X"- 1"				

DIMM 1					
Signal	Length F	Length G	Length J	Length K	Width
SCS#[3:2] SCKE[3:2] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 1" (Note2)	0.1" - 0.8"	5 mils
Total lenght	DIMM1 SCK/SCK#[5:3] length = Y" DIMM1 SCS#/SCKE length = F + G + J =Y"- 1"				



Note1:

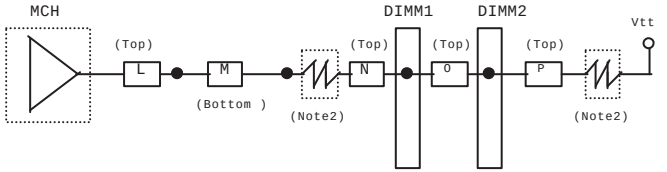
* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Control signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:This purpose prevent break form DIMM0 bottom size 2.5V copper flood to MCH power plane

Note3:Control group signal can NOT placed within the same parallel resistor packs as the command or data group signal

5.SMA[12:0],SBS[1:0],SRAS#,SCAS# routing rule

Signal	Length L	Length M	Length N	Length O	Length P	Width
SMA[12:0] SBS[1:0] SRAS# SCAS# (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils	0.3" - 0.5"	0.1" - 0.8"	5 mils
DIMM 0 Total lenght	DIMM0 SCK/SCK#[2:0] length = X" Command signal length = L + M + N = X" - 1"					
DIMM 1 Total lenght	DIMM0 SCK/SCK#[5:3] length = Y" Command signal length = L + M + N + O = Y" - 1"					



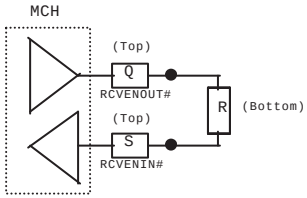
Note1:

* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:Command group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the data or control group signal

5.Feedback - RCVENOUT#,RCVENIN# routing rule

Signal	Length Q	Length R	Length S	Width
RCVENOUT# RCVENIN# (Note1)	40 mils	Equal 1"	40 mils	5 milS
Total Length	Q + R + S = 1080 mils			



Note1:

* Trace spacing = 12 mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 10 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

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DDR Data Signals(1)		
Signal	MCH ball	Package length(")
SDQ0	G28	0.716
SDQ1	F27	0.699
SDQ2	C28	0.874
SDQ3	E28	0.754
SDQ4	H25	0.532
SDQ5	G27	0.666
SDQ6	F25	0.592
SDQ7	B28	0.892
SDQ8	E27	0.797
SDQ9	C27	0.833
SDQ10	B25	0.812
SDQ11	C25	0.753
SDQ12	B27	0.886
SDQ13	D27	0.867
SDQ14	D26	0.773
SDQ15	E25	0.645
SDQ16	D24	0.722
SDQ17	E23	0.602
SDQ18	C22	0.699
SDQ19	E21	0.566
SDQ20	C24	0.785
SDQ21	B23	0.781
SDQ22	D22	0.640
SDQ23	B21	0.711
SDQ24	C21	0.627
SDQ25	D20	0.555
SDQ26	C19	0.587
SDQ27	D18	0.522
SDQ28	C20	0.615
SDQ29	E19	0.487
SDQ30	C18	0.579
SDQ31	E17	0.521

DDR Data Signals(2)		
Signal	MCH ball	Package length(")
SDQ32	E13	0.432
SDQ33	C12	0.543
SDQ34	B11	0.596
SDQ35	C10	0.590
SDQ36	B13	0.639
SDQ37	C13	0.552
SDQ38	C11	0.588
SDQ39	D10	0.626
SDQ40	E10	0.533
SDQ41	C9	0.605
SDQ42	D8	0.587
SDQ43	E8	0.522
SDQ44	E11	0.523
SDQ45	B9	0.715
SDQ46	B7	0.706
SDQ47	C7	0.643
SDQ48	C6	0.700
SDQ49	D6	0.664
SDQ50	D4	0.760
SDQ51	B3	0.922
SDQ52	E6	0.640
SDQ53	B5	0.846
SDQ54	C4	0.810
SDQ55	E5	0.670
SDQ56	C3	0.859
SDQ57	D3	0.811
SDQ58	F4	0.723
SDQ59	F3	0.814
SDQ60	B2	0.949
SDQ61	C2	0.893
SDQ62	E2	0.865
SDQ63	G5	0.689

DDR ECC Signals		
Signal	MCH ball	Package length(")
SCB0	C16	0.570
SCB1	D16	0.526
SCB2	B15	0.623
SCB3	C14	0.533
SCB4	B17	0.621
SCB5	C17	0.583
SCB6	C15	0.540
SCB7	D14	0.503

DDR Data Strobe Signals		
Signal	MCH ball	Package length(")
SDQS0	F26	0.651
SDQS1	C26	0.775
SDQS2	C23	0.738
SDQS3	B19	0.636
SDQS4	D12	0.493
SDQS5	C8	0.596
SDQS6	C5	0.776
SDQS7	E3	0.821
SDQS8	E15	0.520

DDR Clock Signals		
Signal	MCH ball	Package length(")
SCK0	E14	0.453
SCK#0	F15	0.432
SCK1	J24	0.454
SCK#1	G25	0.587
SCK2	G6	0.551
SCK#2	G7	0.543
SCK3	G15	0.371
SCK#3	G14	0.349
SCK4	E24	0.610
SCK#4	G24	0.548
SCK5	H5	0.589
SCK#5	F5	0.693

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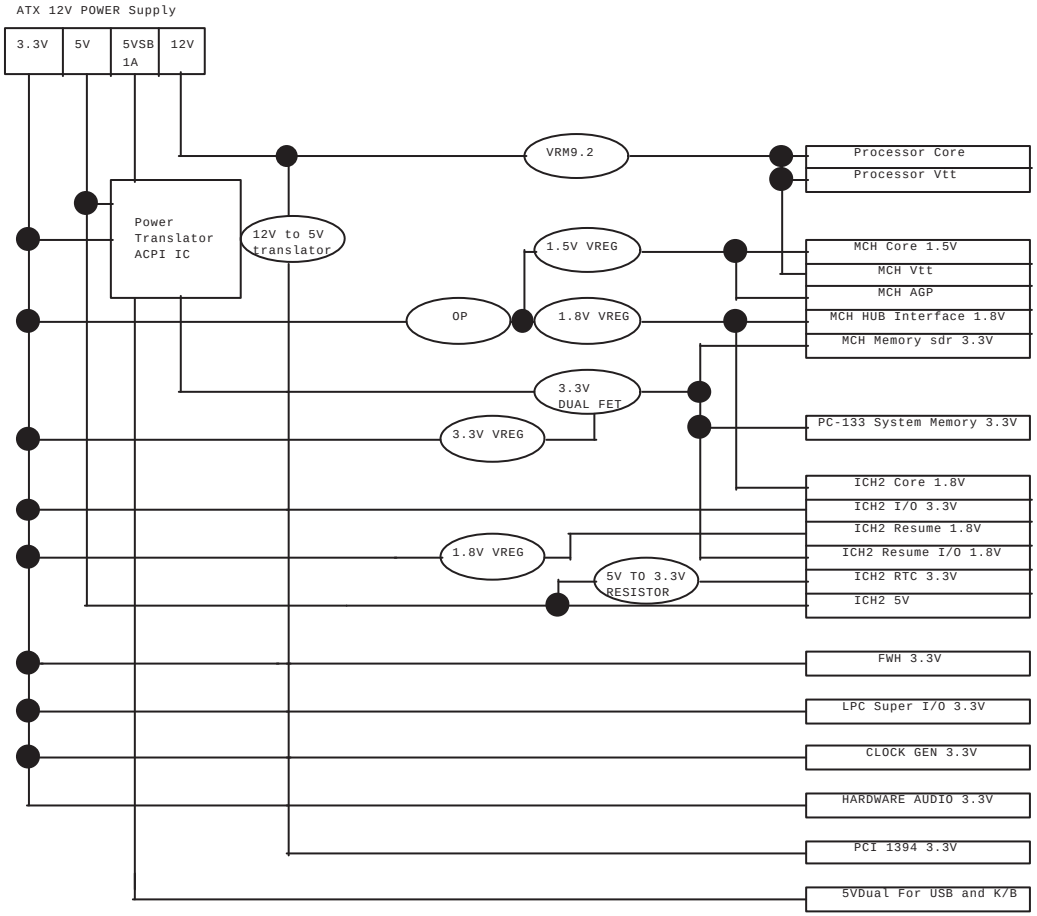
Power Delivery Map



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UUU=JAUDIO1(3-4,5-6)

UUU

JC-D2x2-GN

BIOS

BAT SOCKET

BAT1[A]

YSKTBT

U23[1]

1	VPP	VCC	32
2	RST#	CLK	31
3	FGPI3	FGPI4	30
4	FGPI2	IC(VIL)	29
5	FGPI1	GNDA	28
6	FGPI0	VCCA	27
7	WP#	GND	26
8	TBL#	VCC	25
9	ID3	INIT#	24
10	ID2	FWH4	23
11	ID1	RFU	22
12	ID0	RFU	21
13	FWH0	RFU	20
14	FWH1	RFU	19
15	FWH2	RFU	18
16	GND	FWH3	17

SST49LF002A

JBAT1(1-2)

YJUMPER-MG

JP2(2-3)

YJUMPER-MG

J7(1-2)

YJUMPER-MG

JP5(1-2)

X_YJUMPER-MG

JP4(1-2)

X_YJUMPER-MG

MS6549PCB

PCB

MS-6549-00B

COM1

YCN9M-1

COM2

YCN9M-1

USB900

M_D2x5-2:7.4-BK

AGP1-1

B1		12V	A1
B2	OVRCNT#	TYPEDET#	A2
B3	5V	RESV	A3
B4	5V	USB-	A4
B5	USB+	GND	A5
B6	GND	INTA#	A6
B7	INTB#	RST#	A7
B8	CLK	GNT#	A8
B9	REQ#	VCC3	A9
B10	VCC3	ST1	A10
B11	ST0	RESV	A11
B12	ST2	PIPE#	A12
B13	RBF#	GND	A13
B14	GND	WBF#	A14
B15	RESV	SBA1	A15
B16	SBA0	VCC3	A16
B17	VCC3	SBA3	A17
B18	SBA2	ST_STB#	A18
B19	SB_STB	GND	A19
B20	GND	SBA5	A20
B21	SBA4	SBA7	A21
B22	SBA6	RESV_C	A22
B23	RESV	GND_D	A23
B24	GND N	RESV_D	A24
B25	3_3VAUX1	VCC3_3_C	A25
B26	VCC3	AD30	A26
B27	AD31	AD28	A27
B28	AD29	VCC3	A28
B29	VCC3	AD26	A29
B30	AD27	AD24	A30
B31	AD25	GND	A31
B32	GND	AD_STB1#	A32
B33	AD_STB1	C/BE#3	A33
B34	AD23	VDDQ	A34
B35	VDDQ	AD22	A35
B36	AD21	AD20	A36
B37	AD19	GND	A37
B38	GND	AD18	A38
B39	AD17	AD16	A39
B40	C/BE#2	VDDQ	A40
B41	VDDQ	FRAME#	A41
B42	IRDY#	RESV	A42
B43	3_3VAUX2	GND	A43
B44	GND	RESV	A44
B45	RESV	VCC3	A45
B46	VCC3	TRDY#	A46
B47	DEVSEL#	STOP#	A47
B48	VDDQ	PME#	A48
B49	PERR#	GND	A49
B50	GND	PAR	A50
B51	SERR#	AD15	A51
B52	C/BE#1	VDDQ	A52
B53	VDDQ	AD13	A53
B54	AD14	AD11	A54
B55	AD12	GND	A55
B56	GND	AD9	A56
B57	AD10	C/BE#0	A57
B58	AD8	VDDQ	A58
B59	VDDQ	AD_STB0#	A59
B60	AD_STB0	AD6	A60
B61	AD7	GND	A61
B62	GND	AD4	A62
B63	AD5	AD2	A63
B64	AD3	VDDQ	A64
B65	VDDQ	AD0	A65
B66	AD1	VREF_GC	A66
	VREF_CG		

Retention Module

X_U12-A

845-MCH-PIN

X_U12-B

X_845-MCH-PIN

X_U12-C

X_845-MCH-PIN

X_U12-D

845-MCH-PIN

X_U12

845-MCH-H

U7_1

CPU Retention Module

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Revision History

Revision History (Changes from Rev 0A)

15	Change J7 from 2 pin to 3 pin for LG request
18	Add R906 for VCC_DIMM work normal.