

MS-6541 Micro-ATX

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INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

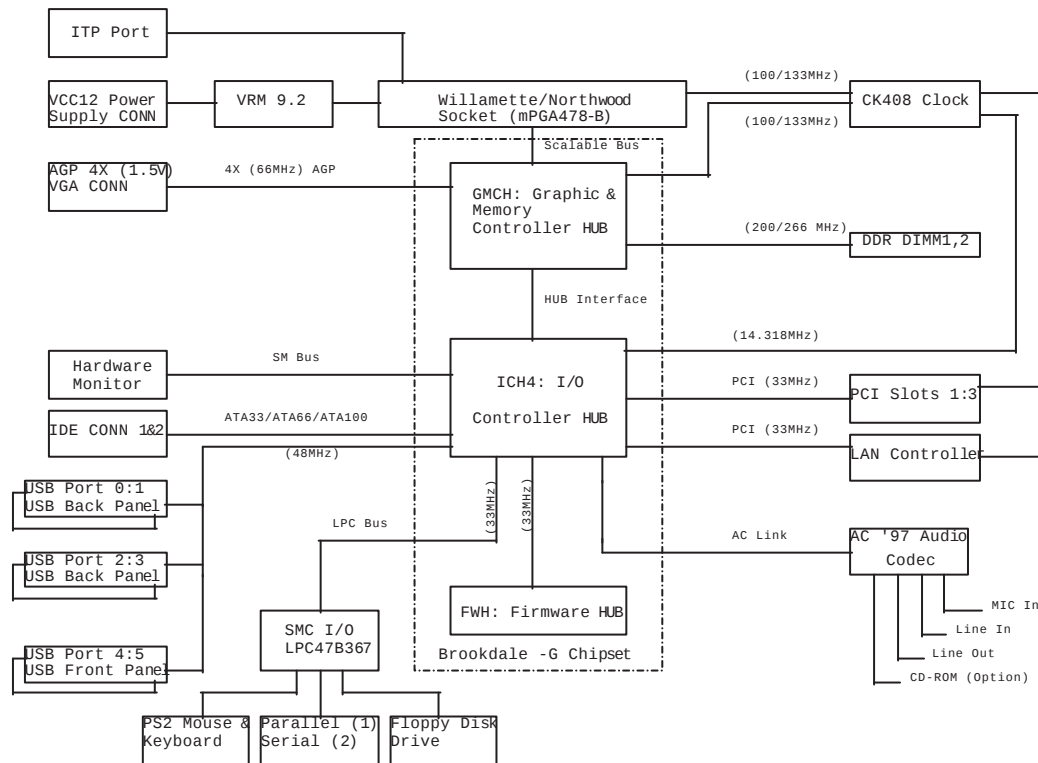
CPU:
Willamette/Northwood mPGA-478B Processor

System Brookdale-G Chipset:
INTEL GMCH (North Bridge) +
INTEL ICH4 (South Bridge)

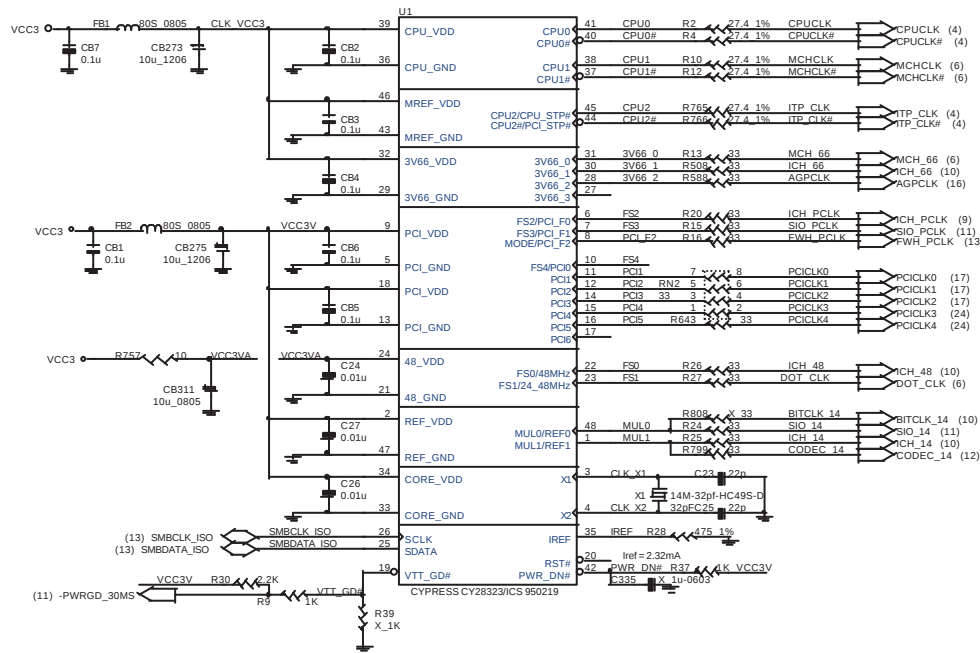
On Board Chipset:
BIOS -- FWH
AC'97 Codec -- AD1981
LPC Super I/O -- LPC47B367
Clock Generation -- CY28323 / ICS950219
LAN -- Intel KINNERITH controller

Expansion Slots:
PCI2.2 SLOT * 3
PCI Extender Connector * 1

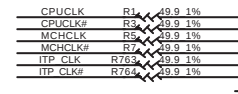
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Title COVER SHEET			
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CLOCK GENERATOR BLOCK

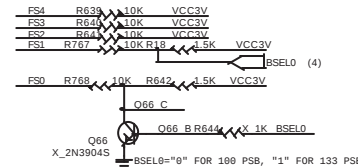


Shut Source Termination Resistors



Trace less 0.2"
49.9ohm for 50ohm M/B impedance

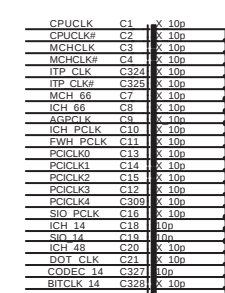
CLOCK STRAPPING RESISTORS



FS4 FS3 FS2 FS1 FS0 CPU (MHz)
1 1 1 0 1 100 MHz
1 1 1 1 1 133 MHz

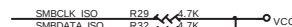
MUL0 R31 X 1K VCC3V
MUL1 R509 X 1K VCC3V
MUL 1:0 0 0 4X
0 1 5X
1 0 6X
1 1 7X

Pull-Down Capacitors



used only for EMI issue

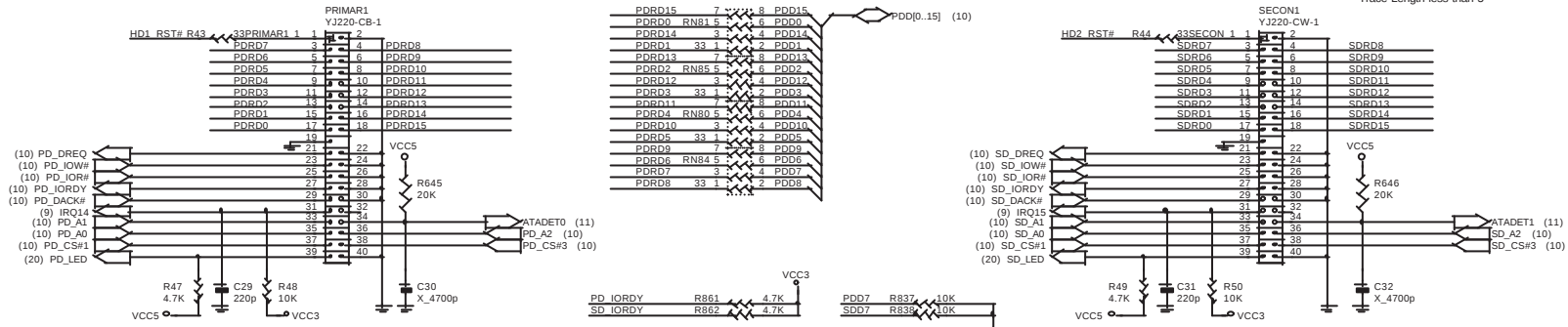
Trace less 0.2"



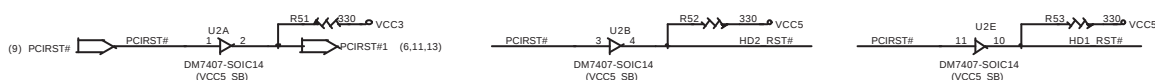
PRIMARY IDE BLOCK

ATA100 IDE CONNECTORS

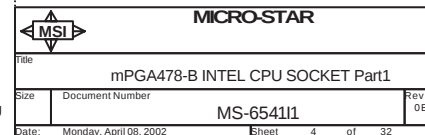
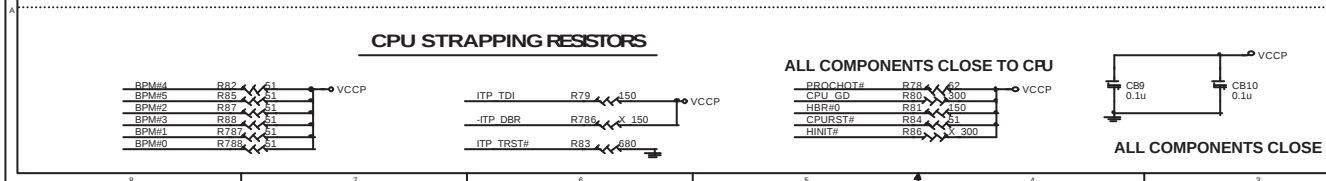
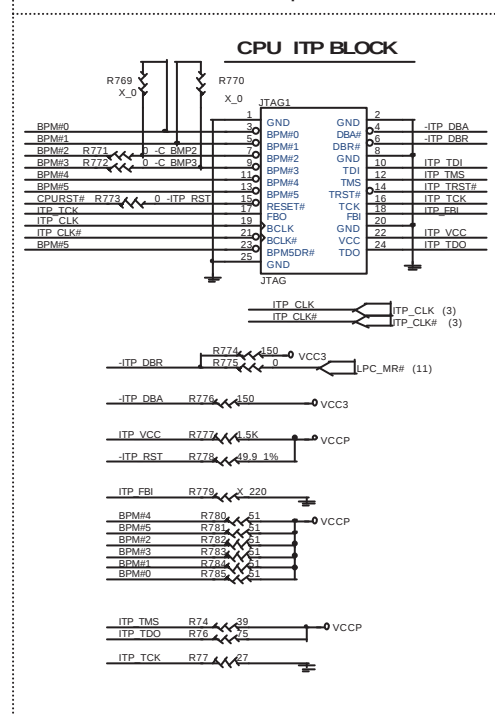
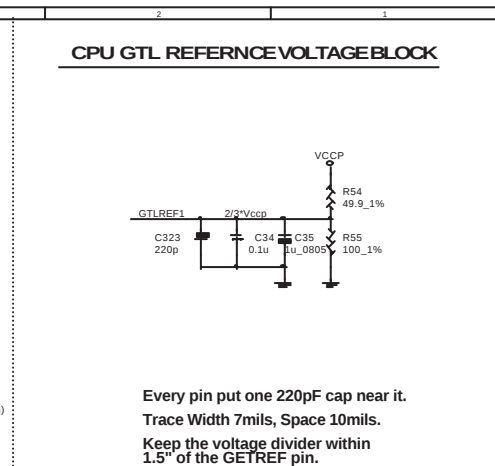
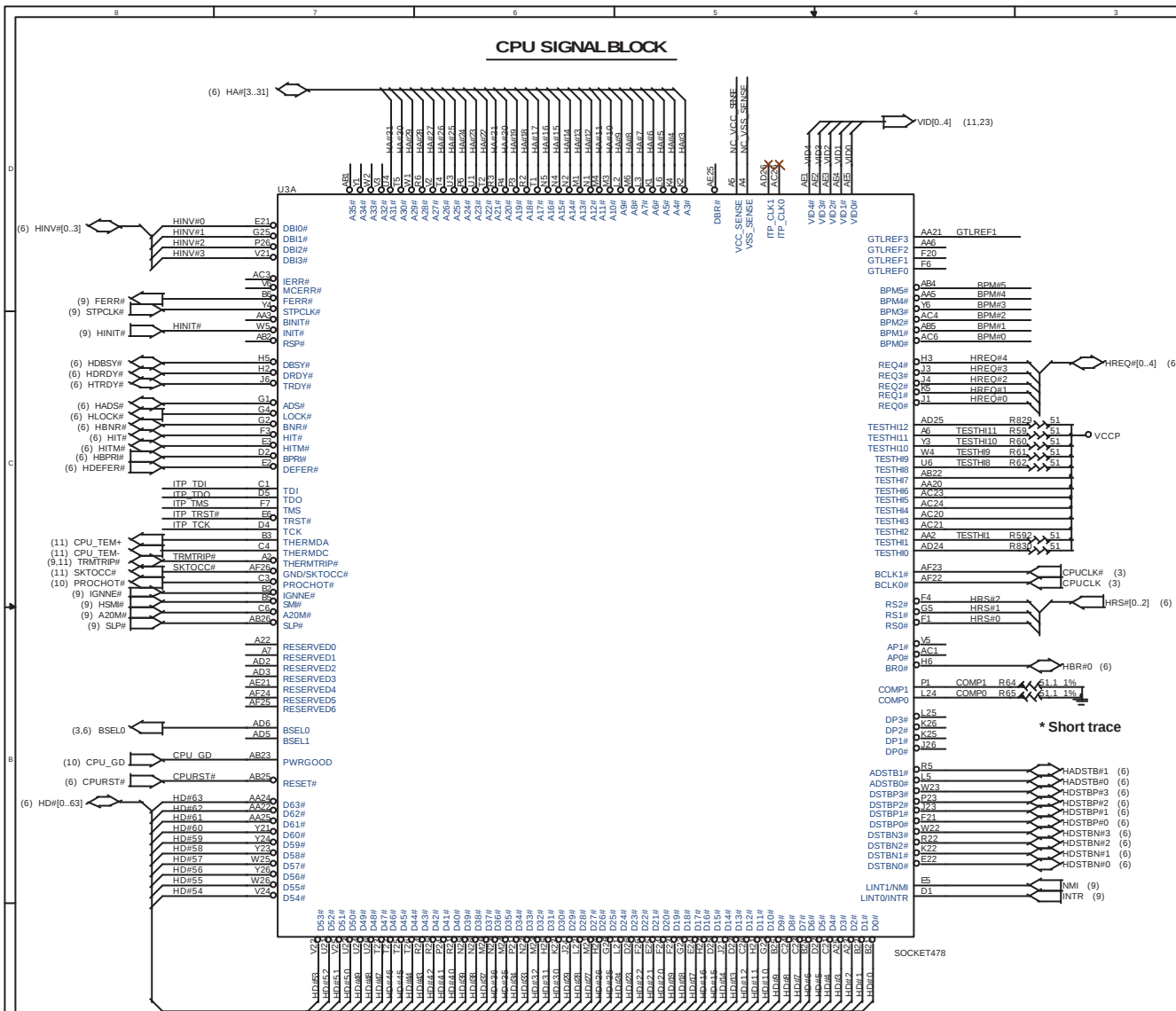
SECONDARY IDE BLOCK

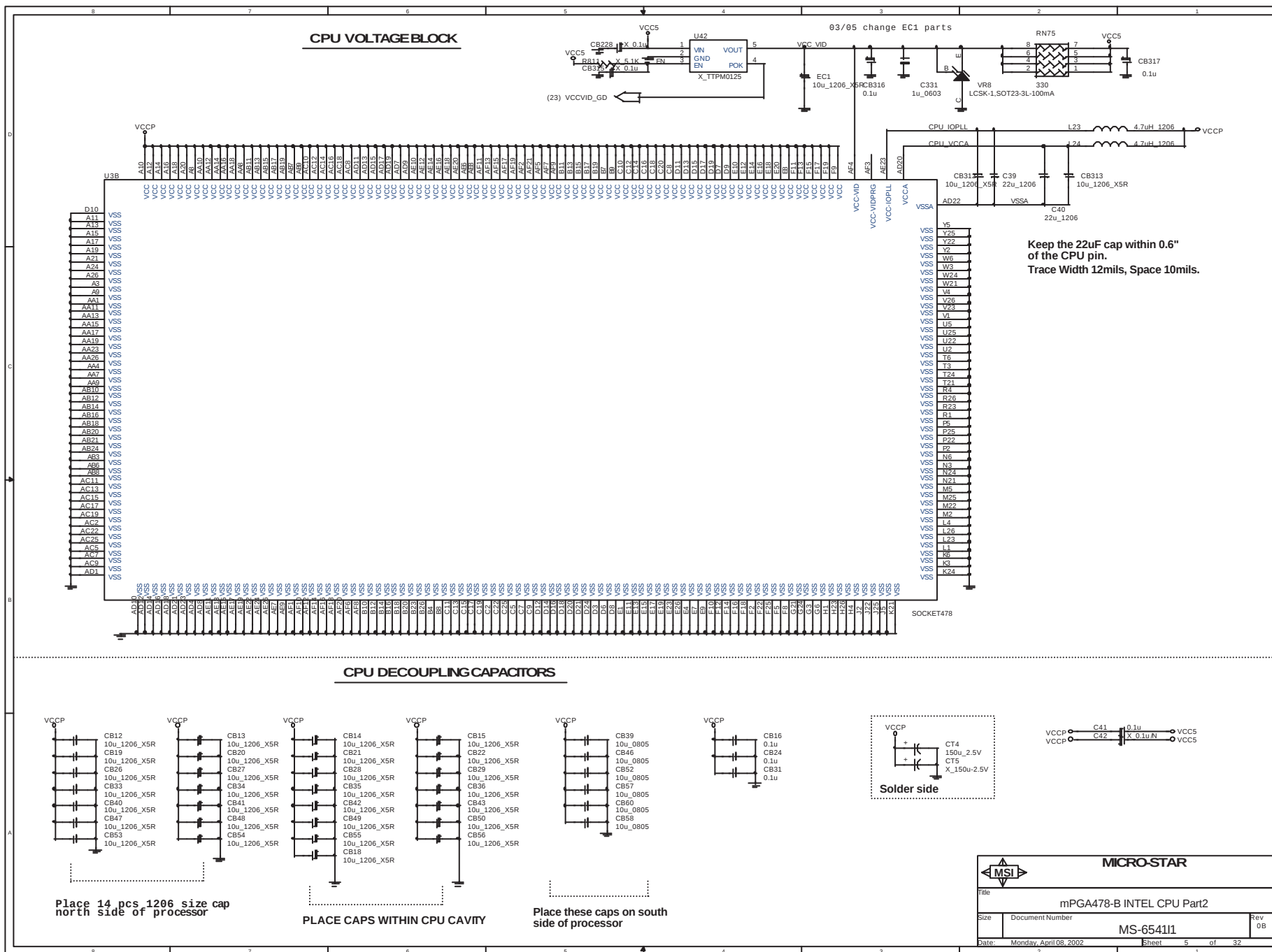


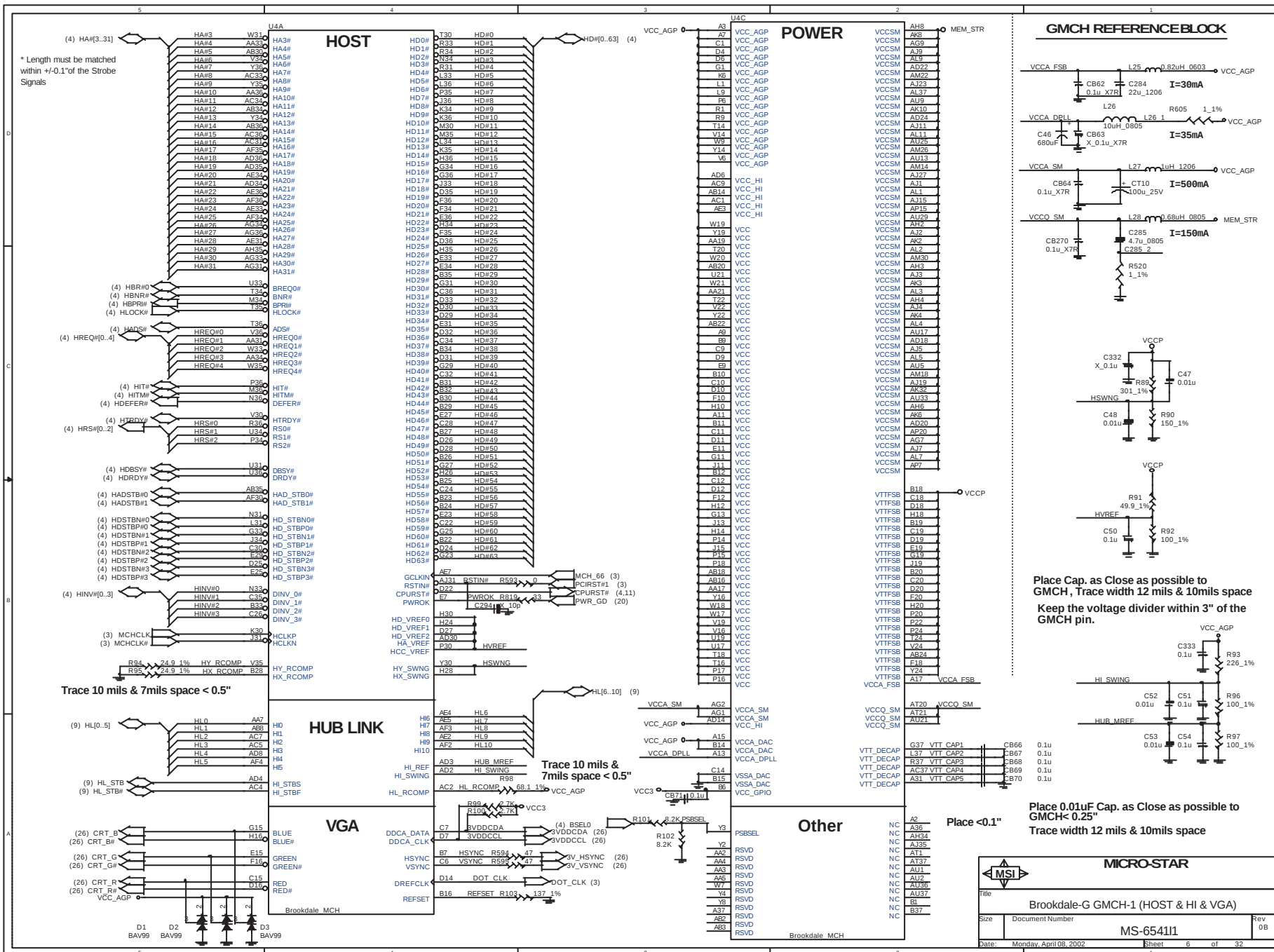
RESET BLOCK

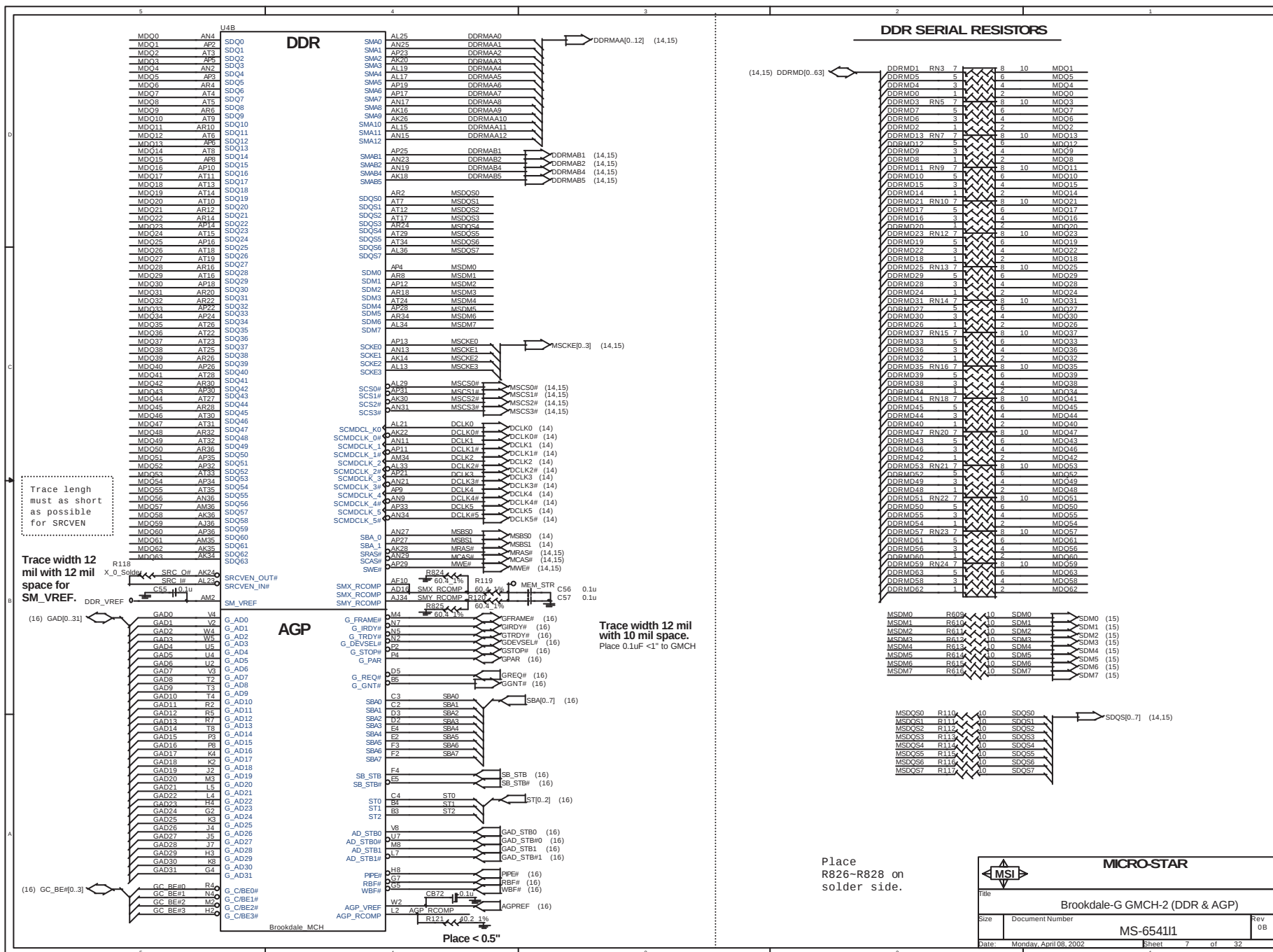


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Title: Clock CY28323 & ATA100 IDE CONNECTORS	
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Place
R826~R828 on
solder side.



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Broodale GMCH(VSS)			
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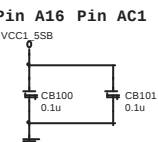
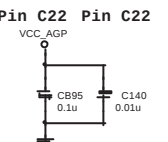
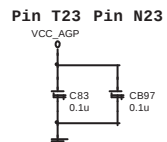
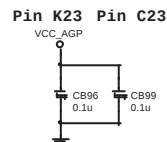
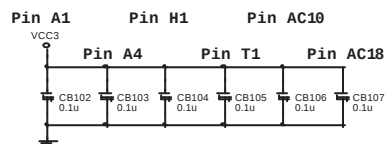
Figure 10: Schematic diagram of the power supply section. The diagram shows two 5V regulators. The first regulator has inputs FERR# (R123, 62), TRMTRIP# (R124, 62), and TRIP# R (R822, 62) connected to VCCP. Its outputs SERIRQ (R125, 6.2K), KB_RST# (R126, 10K), A20GATE# (R127, 10K), REQ#A (R131, 10K), and SYSMAG_INT (R132, 10K) are connected to VCC3. The second regulator has inputs APIC_D0 (R128, 10K), APIC_D1 (R129, 10K), and APICCLK connected to ground. Its output EE_DOUT (R133, 10K) is connected to ground.

Trace width use 12 mils and 10mils space

Figure 10 shows the LAN_RST# and LAN_DIS# circuit. It includes a DM7407-SOIC14 U2F component. The RSMRST# signal is connected to pin 5, and LAN_DIS is connected to pin 13. Both pins are also connected to VCC3_5B through resistors R522 (330 ohms) and R569 (8.2K ohms) respectively. The output of the U2F is connected to LAN_RST#.

```
If LAN_DIS="H", LAN_RST#="L"
```

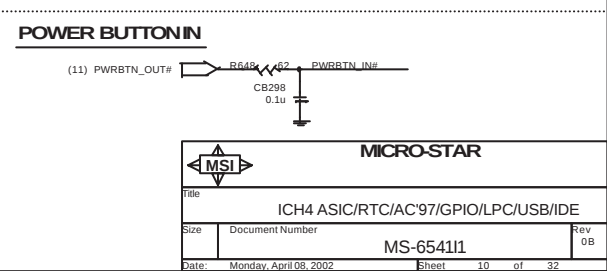
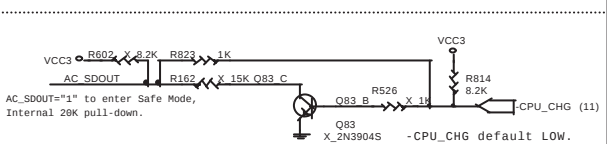
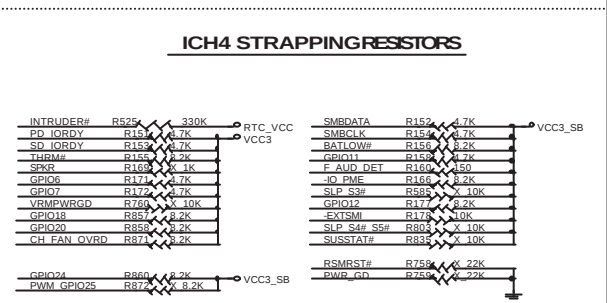
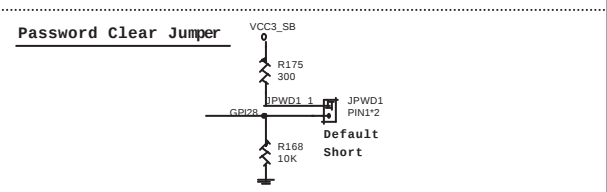
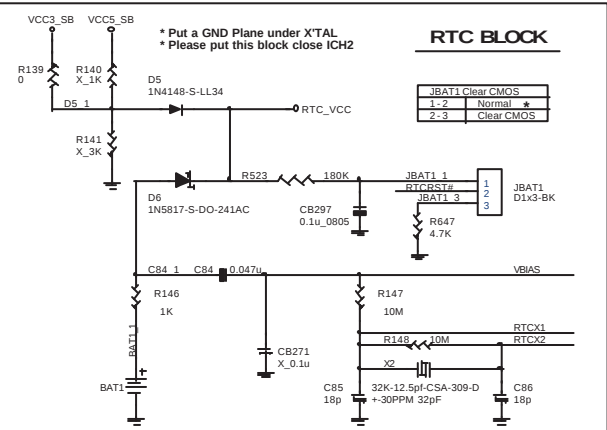
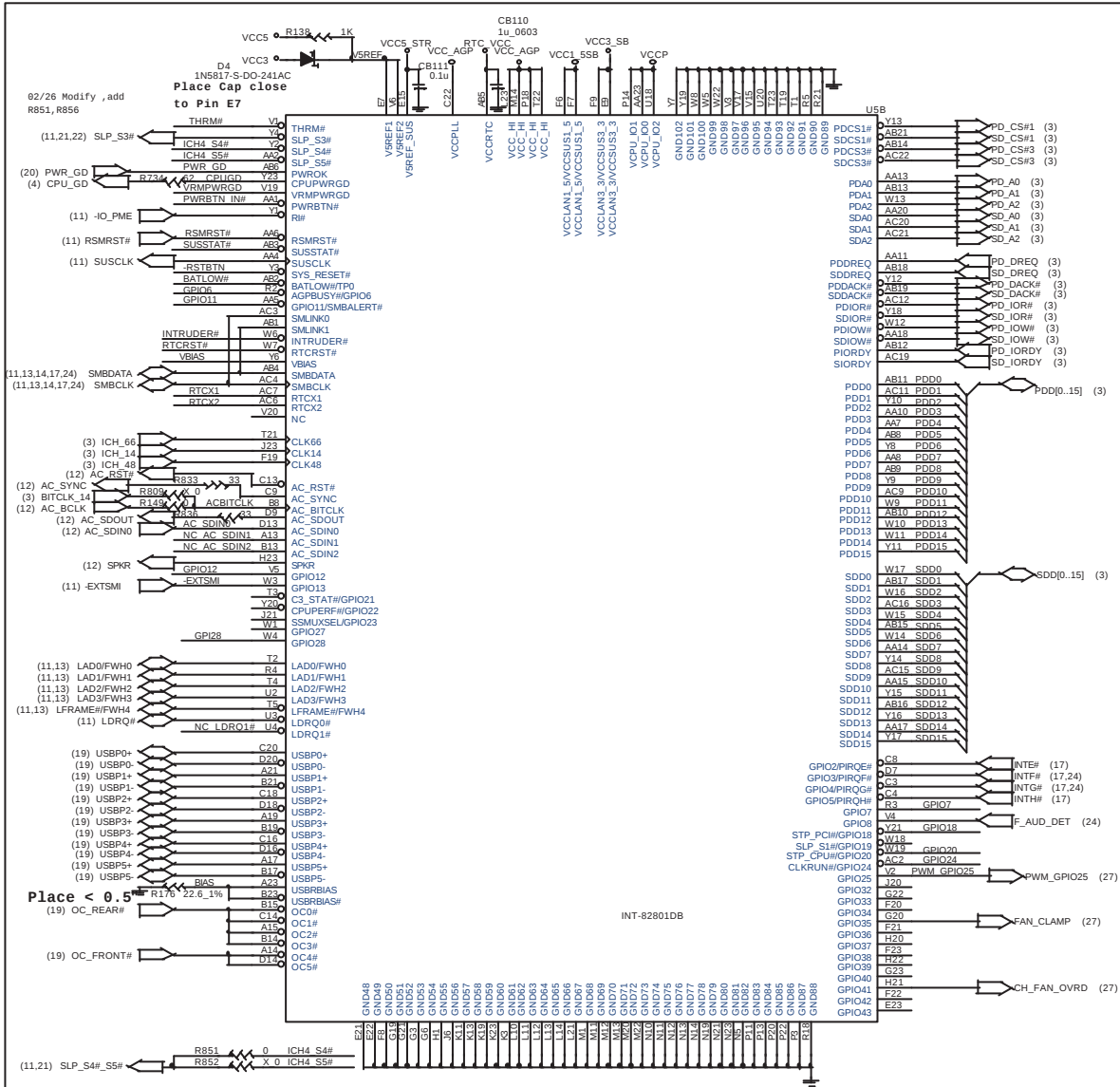
Place one 0.1u close to ICH4 <100 mil



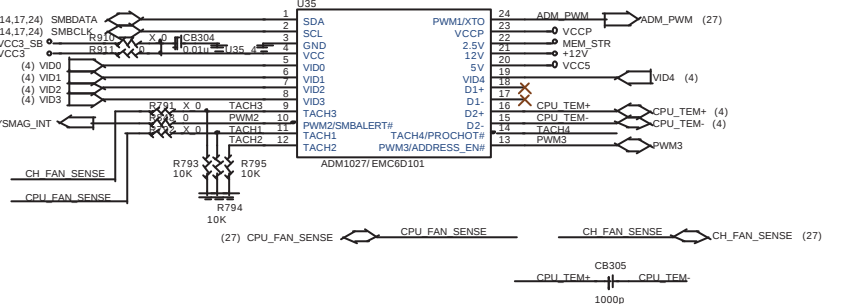
FOR PLL



Title			Brookdale-G ICH4 PCI & HI & LAN		
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U8



Schematic diagram of the R667 pin connections. The diagram shows a horizontal line representing the R667 package with pins numbered 1 to 16. Pin 1 is connected to R15E1 and R667 1.2K. Pin 2 is connected to R15E2 and R667 0.2K. Pin 3 is connected to GP33 and R667 1K. Pin 4 is connected to PWR_GD_10MS and R667 10K. Pin 5 is connected to PWRBTN_OUT# and R667 4.7K. Pin 6 is connected to RSMRST# and R667 0.2K. Pin 7 is connected to C87 and X_2.0u-0805. Pin 8 is connected to SKTOCC# and R673 10M. Pin 9 is connected to IAN_DIS and R674 10K. Pin 10 is connected to PHY_DIS and R817 2.2K. Pin 11 is connected to SIO_ADDR and R183 4.7K. Pins 12, 13, 14, 15, and 16 are connected to VCC3 and VCC5.

VCC3

R728
8.2K

IO_TRMTRIP

Q22
2N3904

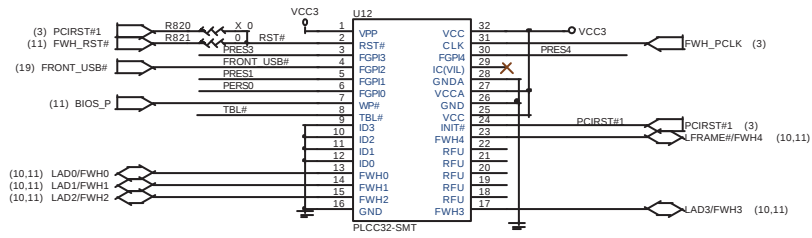
R729 45K Q22 B

VCC3

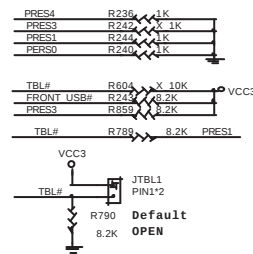
Q2/28 ADD R855 for PW pull-up resistor

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Title					
I/O LPC47B367 & ADM1028					
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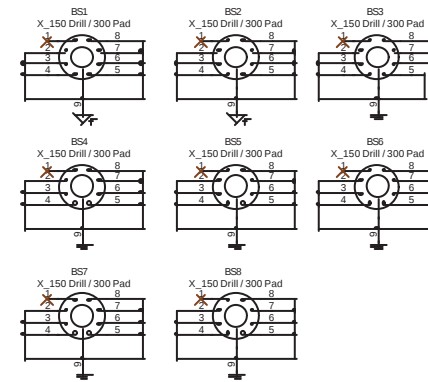
FirmwareHub (FWH)



FWH RESISTORS



PCB OTHER COMPONENT

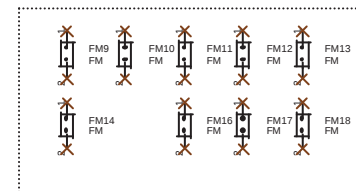
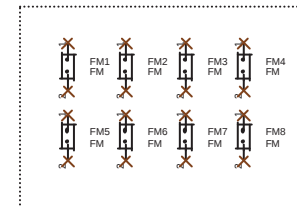


3/18 Delete FWH INIT Signal Voltage
Transiation Block Circuit

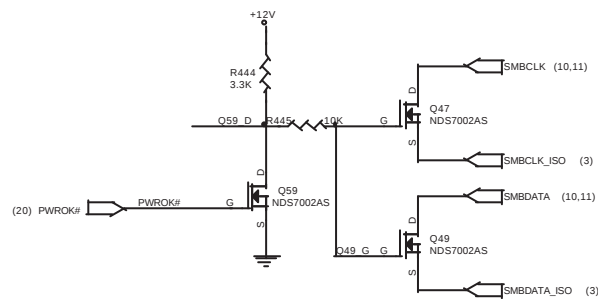
SIMULATION TRACE



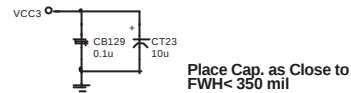
Location Reference Hold



SMBus Isolation



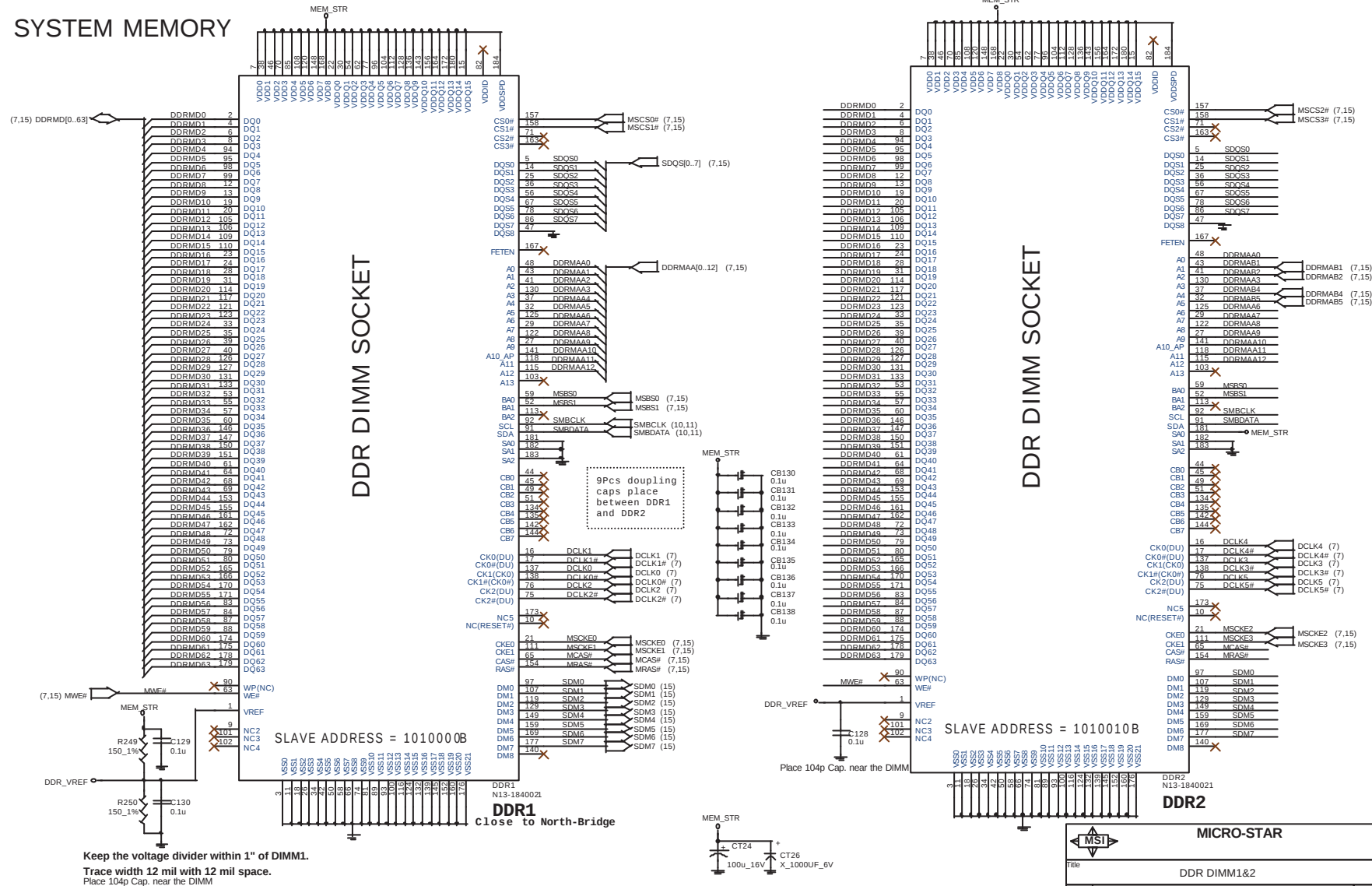
FWH DECOUPLING CAPACITORS



Place Cap. as Close to
FWH< 350 mil

MICRO-STAR	
Title: FWH & Write Protect	
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SYSTEM MEMORY



DDR DIMM SOCKET

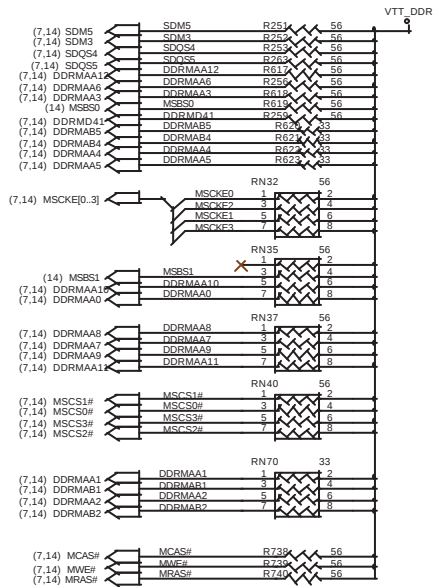
MICRO-STAR

DDR DIMM1&2

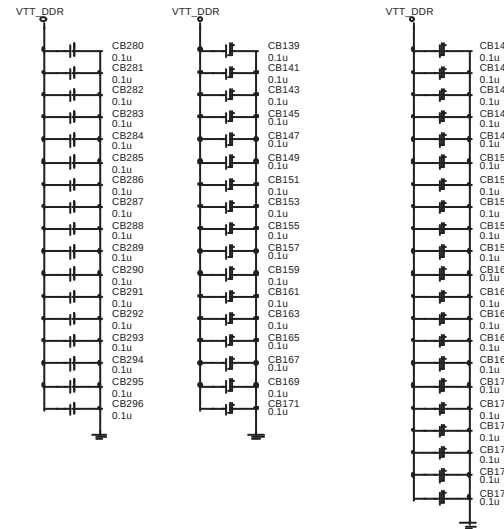
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DDR TERMINATORS

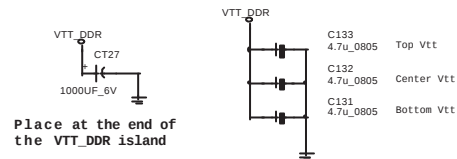


DDR Decoupling Caps



Total 110 signal, need 55 pcs decoupling.

Place for VTT_DDR island



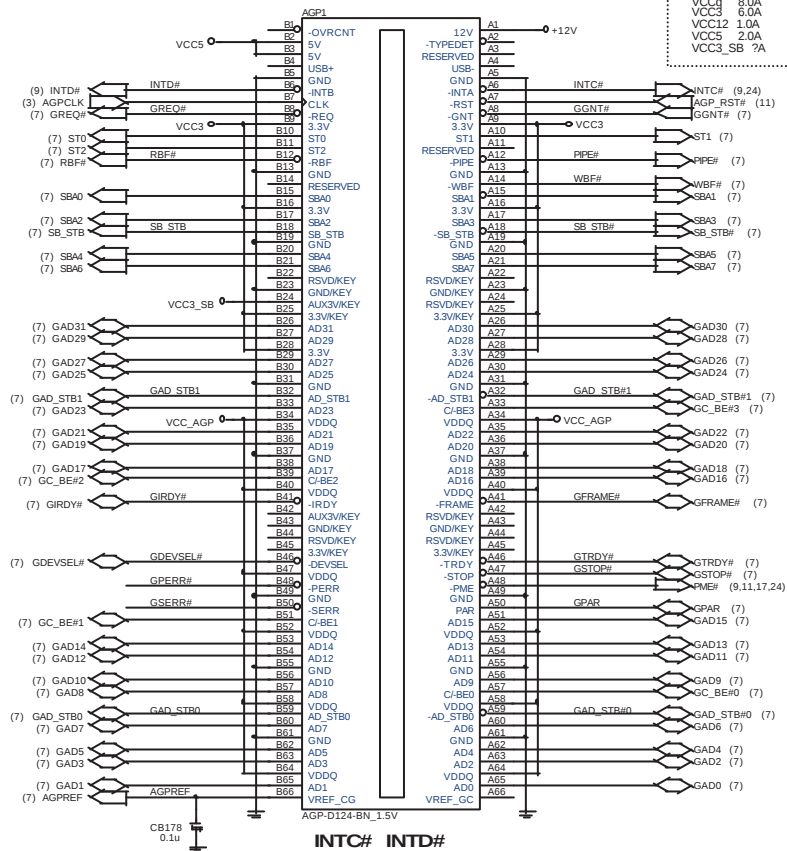
MST		
MICRO-STAR		
Title: DDR Terminator Resistor		
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AGP 1.5V 2X4X SLOT(AGP VER:2.0 COMPLY)

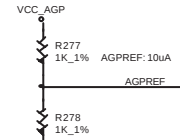
VCC5 = 60mils trace / 15 mils space

AGP Slot Imax

VCCg 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A
VCC3_SB 7A

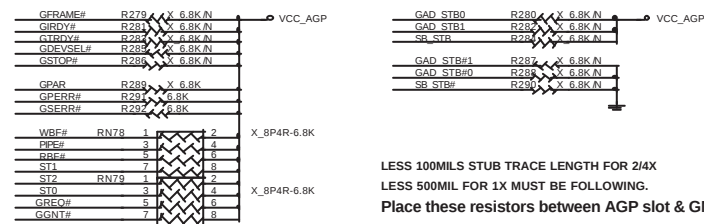


AGP SIGNAL REFERENCE CIRCUIT



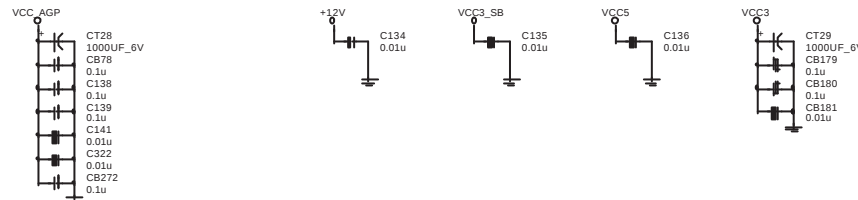
NEAR AGP SLOT

AGP TERMINATION RESISTORS

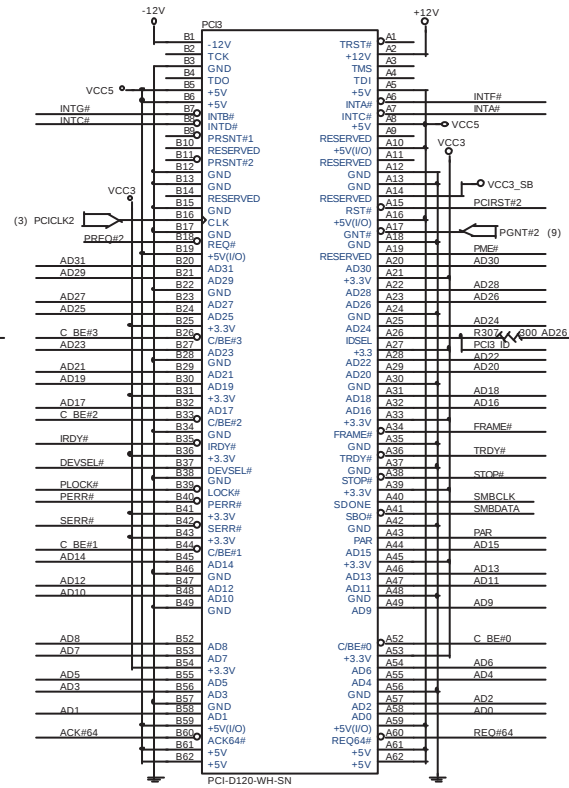
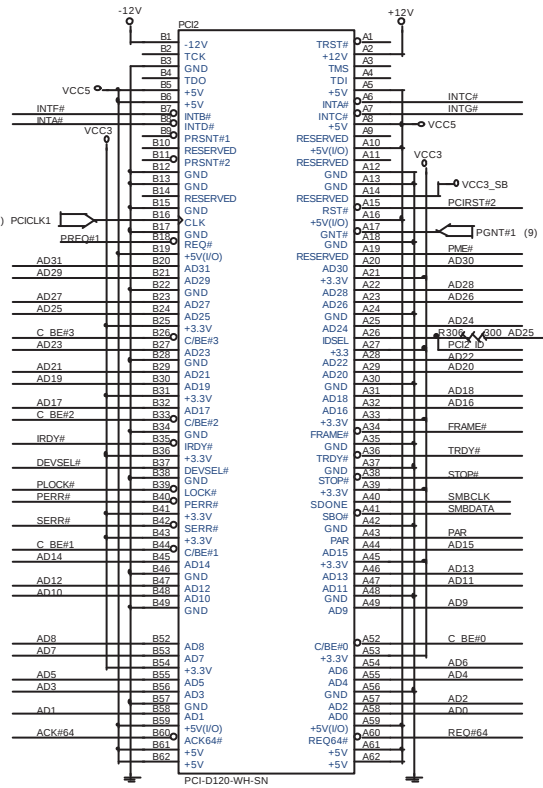
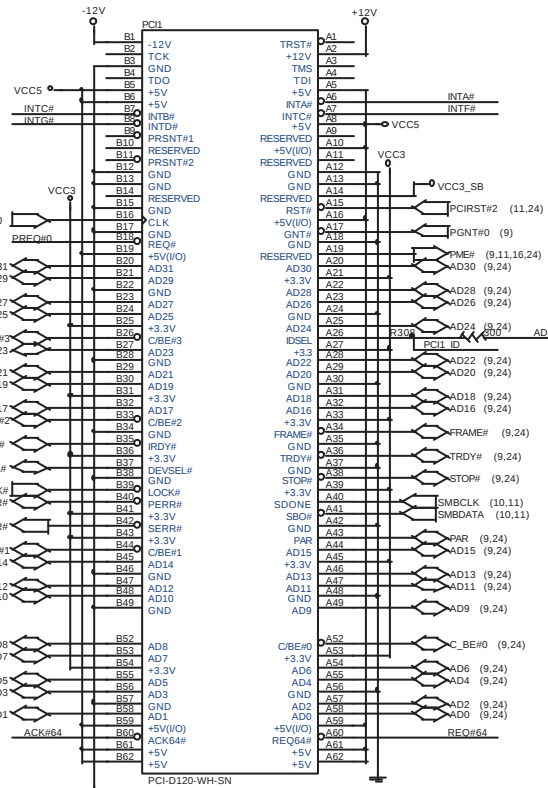


LESS 100MILS STUB TRACE LENGTH FOR 2/4X
LESS 500MIL FOR 1X MUST BE FOLLOWING.
Place these resistors between AGP slot & GMCH

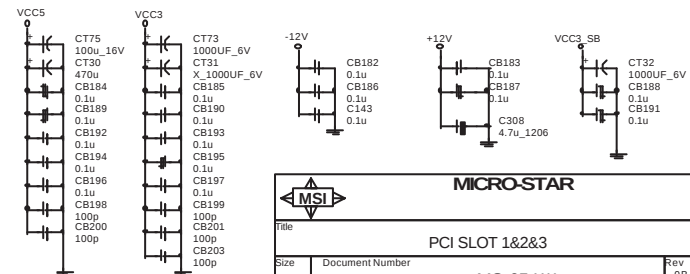
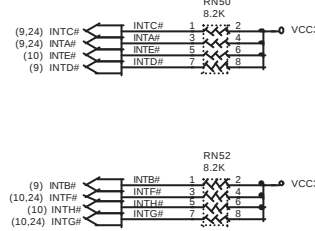
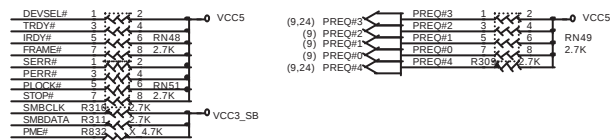
AGP SLOT DECOUPLING CAPACITORS



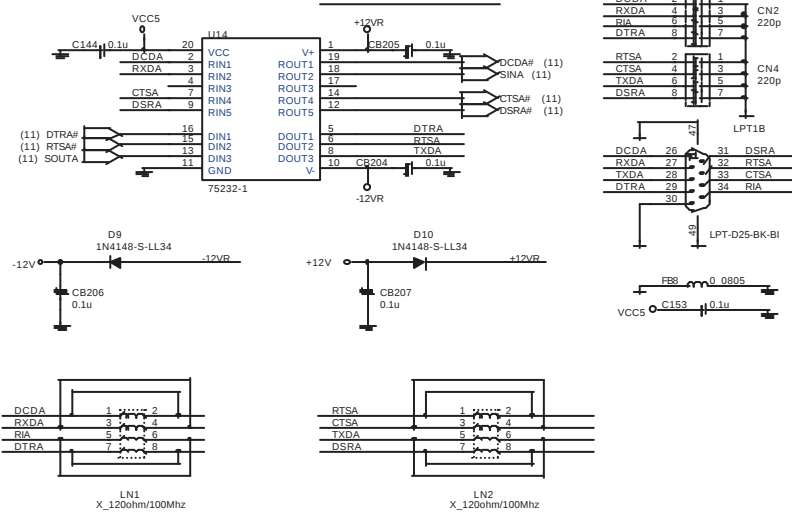
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AGP SLOT			
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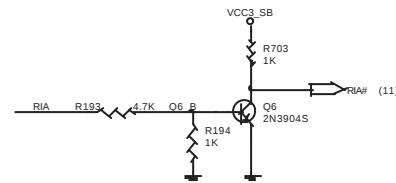
```
IDSEL = AD26
MASTER = PREQ2
INTF#
```



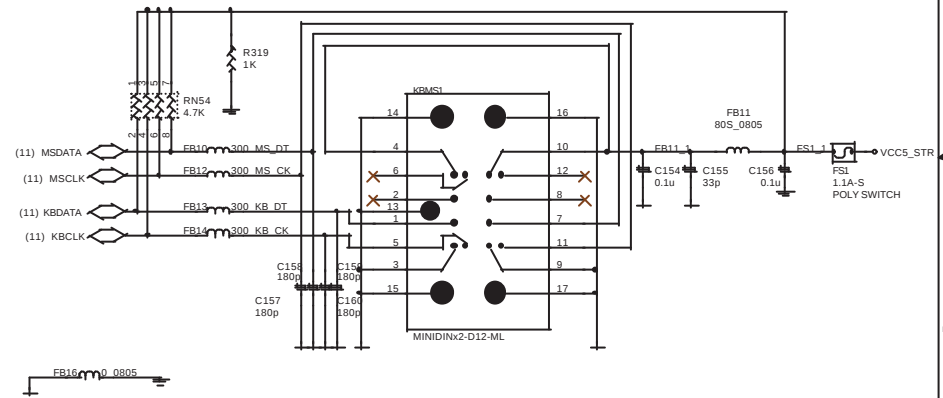
SERIAL PORT1



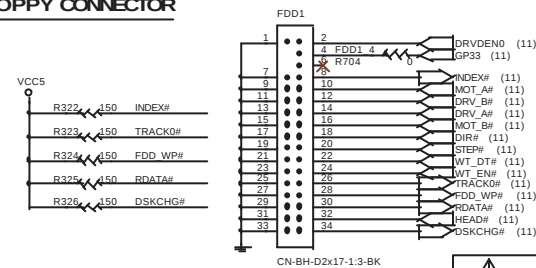
INTERNAL MODEM WAKEUP HEADER



PS2 KEYBOARD & MOUSE CONNECTOR

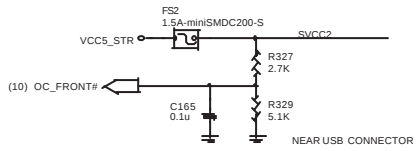


FLOPPY CONNECTOR

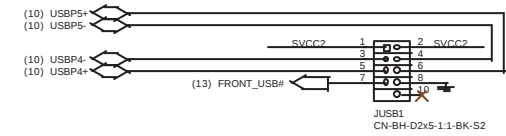


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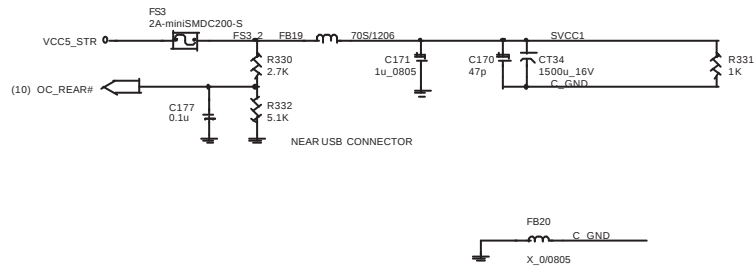
POWER CIRCUIT FOR USB PORT 45



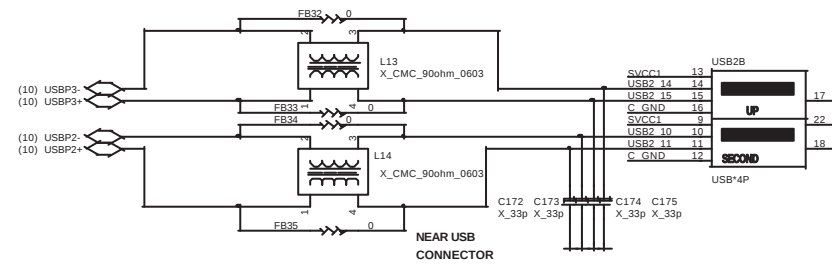
FRONT PANEL USB CONNECTOR FOR USB PORT 45



POWER CIRCUIT FOR USB PORT 0,1,2,3



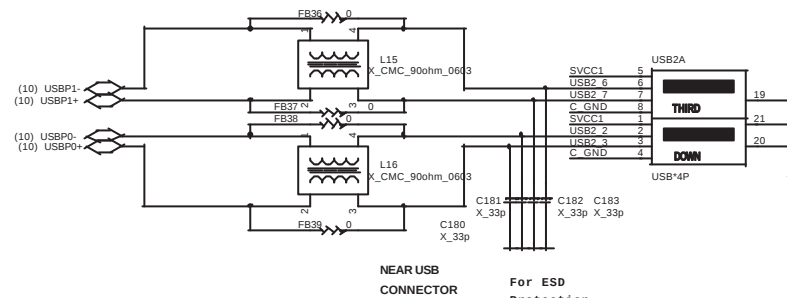
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



02/22 L13,L14,L15,L16 not install and
FB32,FB33,FB34,FB35,FB36,FB37,FB38,FB39 change to 0 ohm

For ESD
Protection
D01-0220K00-105

REAR PANEL USB CONNECTOR FOR USB PORT 0,1



For ESD
Protection
D01-0220K00-105

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USB CONNECTORS		
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ATX CONNECTOR

For CPQ Power Supply PS0N="1" to power on system. For Normal Power Supply PS0N="0" to power on system.

Customer Front Panel

IDE_LED

(3) PD_LED

R716 17K

R IDEACTP

2N3906S

Q73

IDE_LED

Q74

R IDEACTS

R717 17K

SD_LED (3)

POWER BUTTON

VCC3_SB

R371 4.7K

PWRSW

R372 40K

U7E 74LCX14_SOIC14

U7F 74LCX14_SOIC14

PWRBTN#

PWRBTN# (11)

C196 1u0.0805

C197 1uF

STATE	S0	S1	S3	S4/S5
P_LED (Green)	BRIGHT	DARK	DARK	DARK
S_LED (Yellow)	DARK	BRIGHT	BRIGHT	DARK

VCC5_5B

R713
500

GNRP

(11) SUS_LED

R714
4.7K

R SUS LED

Q72
2N3904S

SLEEP LED



Title			
Front Panel & ATX Connector & FAN			
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

VSEN2 output current
250mA to 300mA.

Figure 1: Schematic diagram of the power supply circuit for the ATmega16. The diagram shows five power supply nodes: MEM_STR, VCC5, VCC5_SB, VCC3, and VCC5_STR. Each node is connected to a specific capacitor and a diode. MEM_STR is connected to a 0.1uF capacitor (CB227) and a 1uF capacitor (1u_0805). VCC5 is connected to a 0.1uF capacitor (C329). VCC5_SB is connected to a 1000uF capacitor (CT45) and a 0.1uF capacitor (CB232). VCC3 is connected to a 0.1uF capacitor (CB234) and a 1uF capacitor (1u_0805). VCC5_STR is connected to a 0.1uF capacitor (CT47) and a 1uF capacitor (CB235).

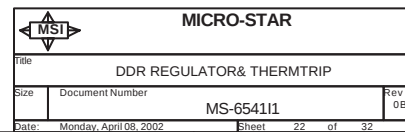
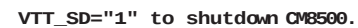
[illegible]

03/13 change Q56,Q57,Q87 to 12N03L_T0252



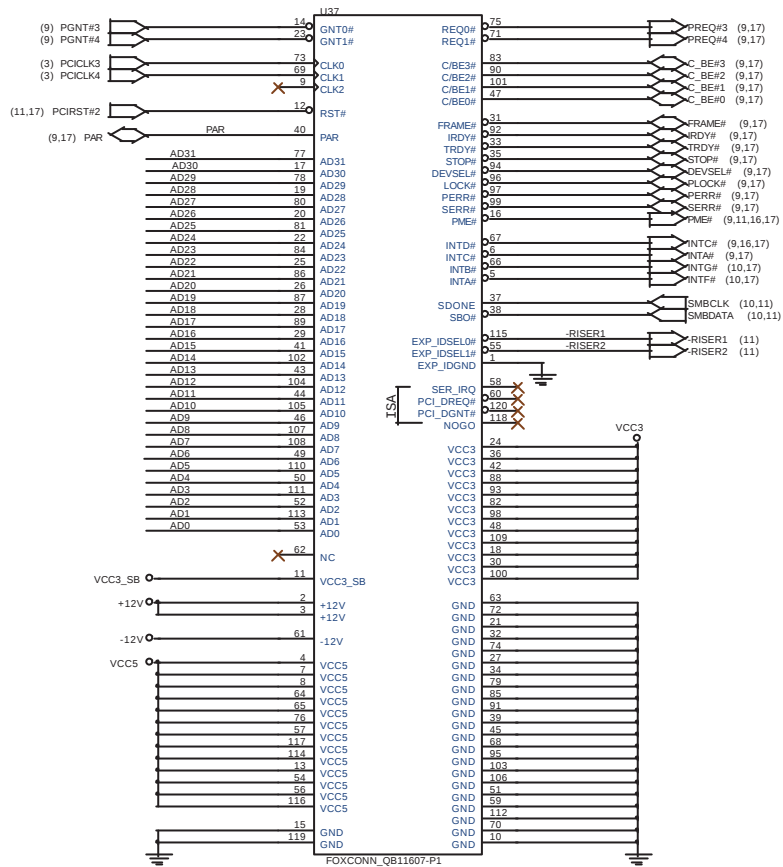
Title			
VOLTAGE REGULATOR			
Size	Document Number	Rev	
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Date:	Monday, April 08, 2002	Sheet	21 of 32

03/05 Change CM8500 to CM8501/A
03/06 Change CM8501A to SOP-8 package

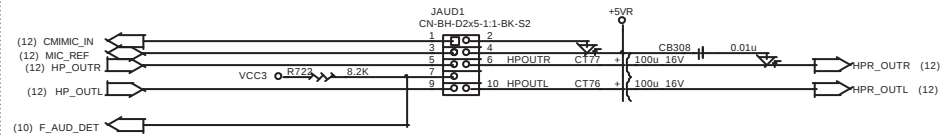


PCI EXPANSION

(9.17) AD[31..0] AD[31..0]



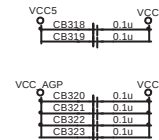
FRONT AUDIO HEADERS



JAUD1 Default 5-6 PIN, 9-10 PIN short

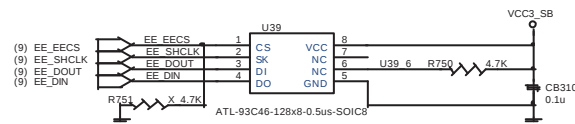
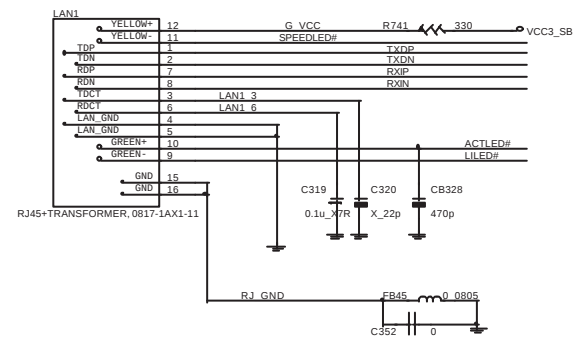
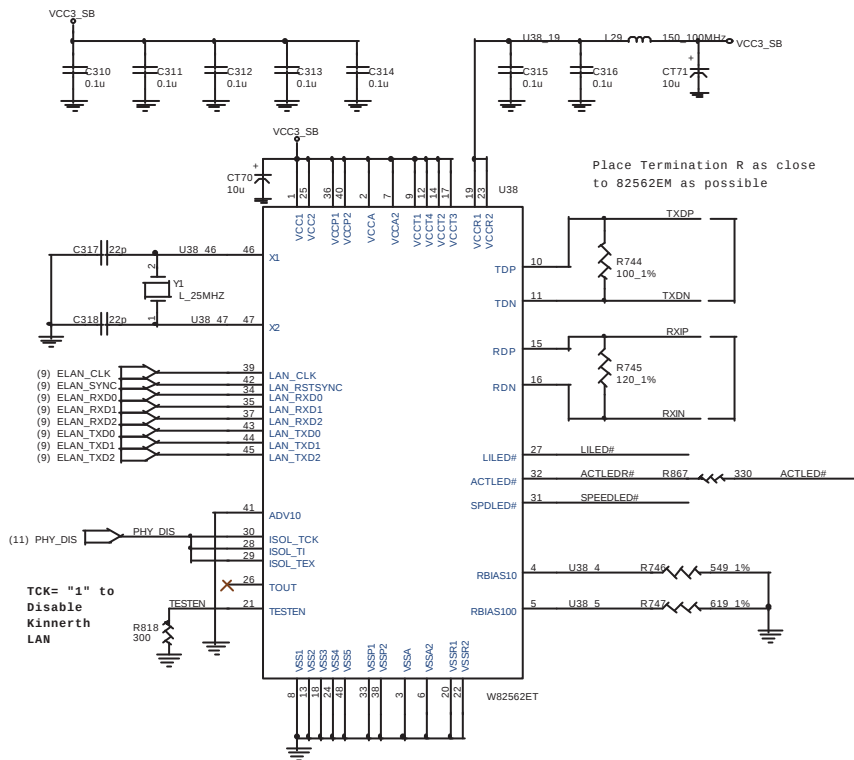
1. DON'T USE FRONT AUDIO BOARD
USE MINI JUMPER TO
CONNECT PIN5&6 AND PIN9&10
2. USE FRONT AUDIO BOARD
UNINSTALL MINI JUMPER

Stitch CAP



03/08 Remove JAUD1 pin 3 MIC_REF ,
connect to net JS1.
03/05 change CT77,CT76 parts.
02/25 Modify Front Audio Headers Circuit

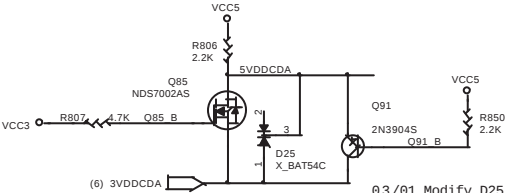
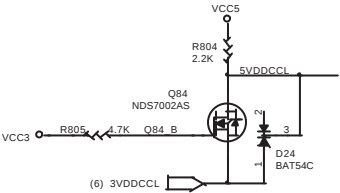
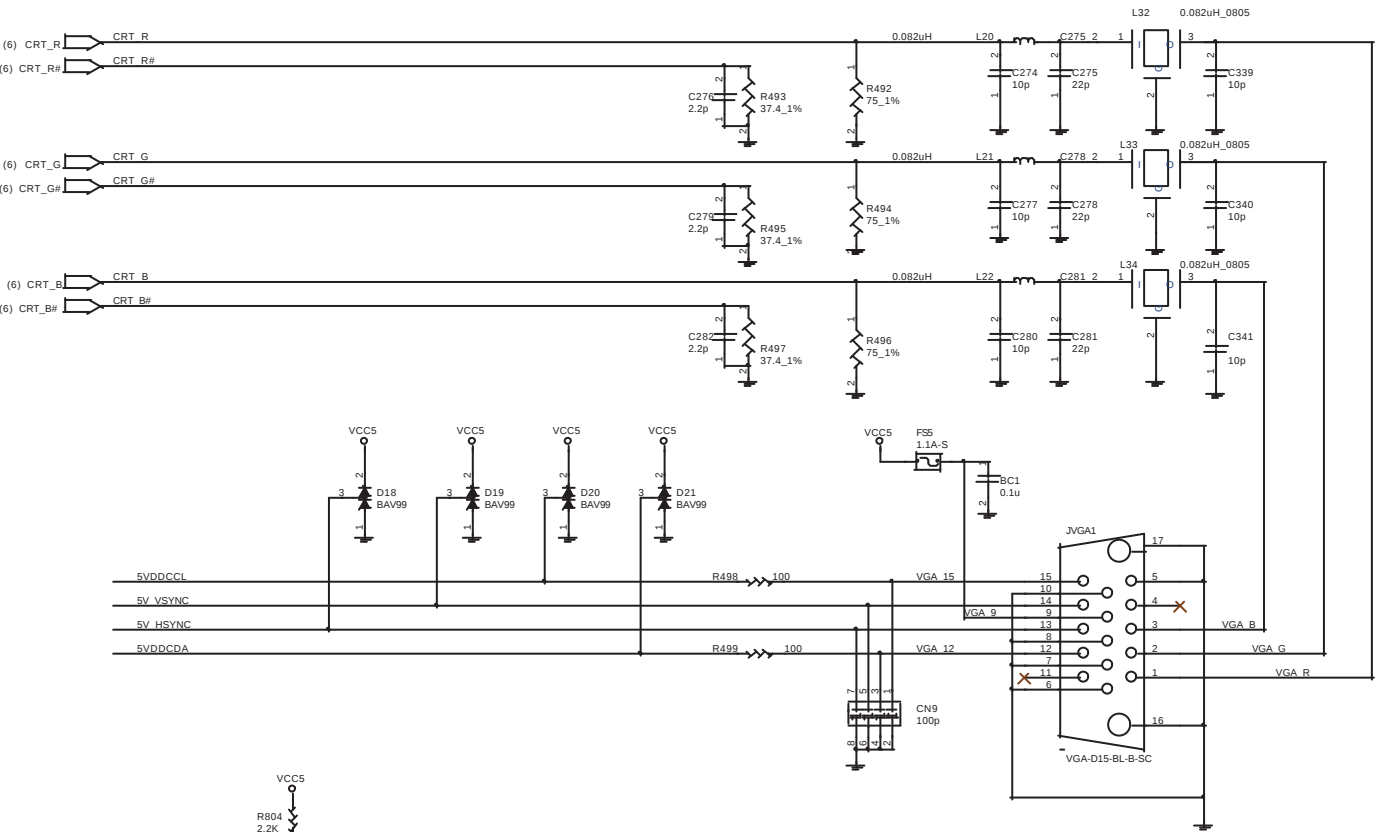
MICRO-STAR			
Title: SMBUS_ISOLATION			
Size:	Document Number:	MS-654111	Rev: 0B
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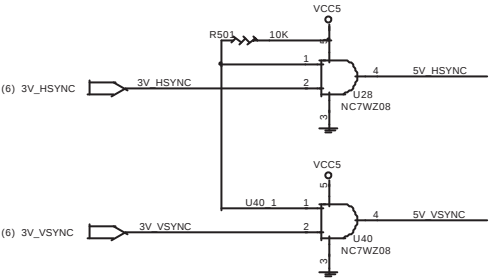
MICRO-STAR		
Title: LAN LAVON/KENAI32		
Size:	Document Number:	Rev: 0B
MS-654111		
Date:	Monday, April 08, 2002	Sheet 25 of 32

Video Connector

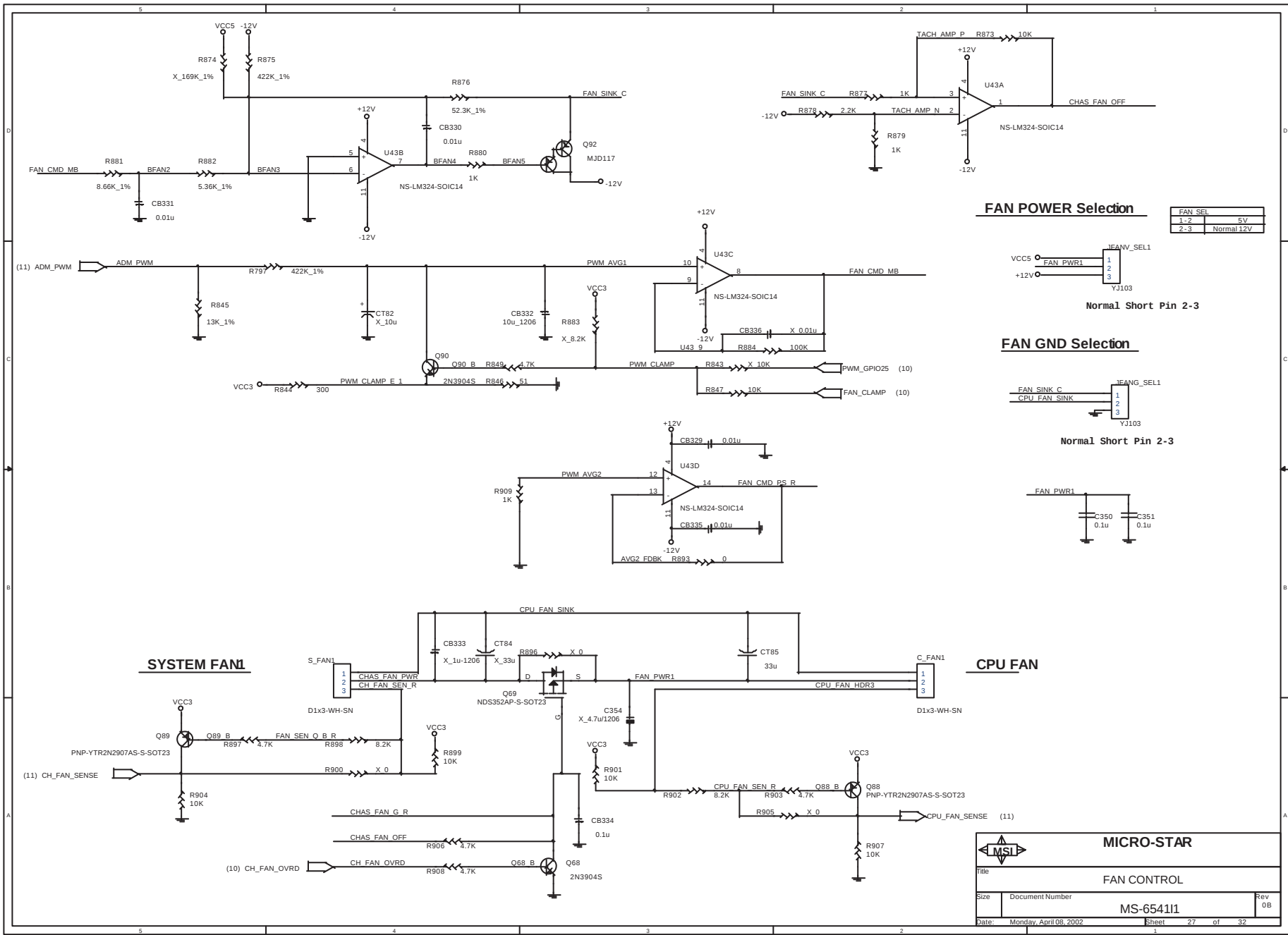
02/28 ADD L32,L33,L34,C339,C340,C341 for RGB filter circuit



03/01 Modify D25 to not installed



MICRO-STAR			
File			
VGA Connector			
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MANUAL

PCB P01-6541-0B BAT1_X1
BH-D2

U4_X1

HEATSINK

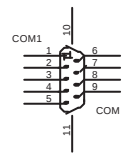
U12_X
BIOS_4Mbit

U4_X21

U4_X22

U3_X

X_RETENTION MODUL



MINI JUMPER

JPWD1_M
GREEN

JBAT1_M
YELLOW

JANV_SEL1M
RED

JFANG_SEL1M
RED

JAUD1_56M
RED

JAUD1_910M
RED

			MICRO-STAR		
File					
MANUAL PART					
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ICH4

PIN NAME	POWER WELL	USAGE	DURING RESET	S3/S4/S5	NOTES
GPI0	CORE	REQA#			
GPI1	CORE	SYSMAG_INT			
GPI2	CORE	INTE#			
GPI3	CORE	INTF#			
GPI4	CORE	INTG#			
GPI5	CORE	INTH#			
GPI6	CORE	GPI06			
GPI7	CORE	GPI07			
GPI8	RESUME	F_AUD_DET			Front Audio Cable detection, active LOW
GPI11	RESUME	GPI011			
GPI12	RESUME	GPI12			Connect to SMBALERT# signal of ADM1028.
GPI13	RESUME	-EXTSMI			From LPC I/O IO_SMI# signal.
GPO16	CORE	UNUSED	HIGH	OFF	
GPO17	CORE	UNUSED	HIGH	OFF	
GPO18	CORE	GPI018	HIGH	OFF	
GPO19	CORE	UNUSED	HIGH	OFF	
GPO20	CORE	GPI020	HIGH	OFF	
GPO21	CORE	UNUSED	HIGH	OFF	
GPO22	CORE	UNUSED	HIGH-Z	OFF	
GPO23	CORE	UNUSED	LOW	OFF	
GPO24	RESUME	GPI024	LOW	DEFINED	
GPO25	RESUME	PWM_GPIO25	HIGH	DEFINED	
GPO27	RESUME	UNUSED	HIGH	DEFINED	
GPO28	RESUME	GPI28	HIGH	DEFINED	Clear password indicator, Active LOW.
GPI32	CORE	UNUSED	HIGH	OFF	
GPI33	CORE	UNUSED	HIGH	OFF	
GPI34	CORE	UNUSED	HIGH	OFF	
GPI35	CORE	FAN_CLAMP	HIGH	OFF	
GPI36	CORE	UNUSED	HIGH	OFF	
GPI37	CORE	UNUSED	HIGH	OFF	
GPI38	CORE	UNUSED	HIGH	OFF	
GPI39	CORE	UNUSED	HIGH	OFF	
GPI40	CORE	UNUSED	HIGH	OFF	
GPI041	CORE	CH_FAN_OVRD	HIGH	OFF	
GPI042	CORE	UNUSED	HIGH	OFF	
GPI043	CORE	UNUSED	HIGH	OFF	
RI*	RESUME	-IO_PME			From LPC I/O IO_PME# signal
THERM*	CORE	THRM#			From CPU PROHOT# signal
GPI0		UNUSED	INPUT	DEFINED	
GPI1		TBL#	INPUT	DEFINED	FWH TBL function, Active High.
GPI2		FRONT_USB#	INPUT	DEFINED	Front USB Cable detection, active LOW
GPI3		UNUSED	INPUT	DEFINED	
GPI4		UNUSED	INPUT	DEFINED	

FWH

		MICRO-STAR	
Title			
GPIO SETTING			
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SIO

PIN NAME	USAGE	Input/Output	NOTES
GPIO14	CHASSID_ID0	INPUT	CHASSIS ID 0
GPIO15	CHASSID_ID1	INPUT	CHASSIS ID 1
GPIO30	COLOR	OUTPUT	For POWER LED use
GPIO31	SUS_LED	OUTPUT	For Suspend LED use
GPIO65	-CPU_CHG	OUTPUT	When CPU had been changed, let this signal to LOW to enter SAFE mode.
GPIO20	ATADET0	INPUT	Detect ATA cable type for Primary IDE.
GPIO21	ATADET1	INPUT	Detect ATA cable type for Secondary IDE.
GPIO26	SKTOCC#	INPUT	Connect to CPU SKTOCC#, Low to High means CPU had been changed.
GPIO41	LAN_DIS	OUTPUT	LAN disable control. Active High.
GPIO71	-RISER1	INPUT	Riser card 1 insert, active LOW.
GPIO72	-RISER2	INPUT	Riser card 2 insert, active LOW.
GPIO73	CH_FAN_SENSE	INPUT	System FAN techometer input.
GPIO12	CPU_FAN_SENSE	INPUT	CPU FAN techometer input.
GPIO34	BIOS_P	OUTPUT	FWH write protection function, active LOW.
GPIO35	FWH_RST#	OUTPUT	FWH reset signal. Need to confirm this signal's level.
GPIO32	-IO_TRMTRIP	INPUT	Connect to CPU TRMTRIP#, active LOW.
GPIO75	PWR_GD_10MS	OUTPUT	Power Good delay 10m Second output.
GPIO76	PWR_GD_30MS	OUTPUT	Power Good delay 30m Second output.
GPIO62	PWRBTN#	INPUT	Power button input
GPIO63	SLP_S3#	INPUT	S3 state indicator signal
GPIO64	SLP_S4#_S5#	INPUT	S5 state indicator signal
GPIO67	PS_ON	OUTPUT	Connector to Power Supply to turn Power.
GPIO42	-IO_PME	OUTPUT	LPC I/O PME function.
GPIO13	PME#	INPUT	PCI PME# signal input.
GPIO60	PCIRST#2	OUTPUT	Reset signal output for PCI Slot.
GPIO61	AGP_RST#	OUTPUT	Reset signal output for AGP Slot.
GPIO27	BRD_ID1	INPUT	Board ID 1
GPIO23	BRD_ID0	INPUT	Board ID 0
GPIO10	BRD_REV0	INPUT	Initial Version ID
GPIO11	BRD_REV1	INPUT	Initial Version ID
GPIO85	-FAN_OFF	OUTPUT	FAN ON/OFF control, HIGH to turn on FAN.
GPIO66	PWRBTN_OUT#	OUTPUT	Power button output, connect to ICH4 power button input.
GPIO46	-EXTSMI	OUTPUT	LPC I/O SMI# signal.
GPIO33	GP33	INPUT	Floppy TYPE indicator
GPIO24	SIO_ADDR	INPUT	SYS_ADDR

Before 11/6

GPIO74	PHY_DIS	OUTPUT	PHY disable control. Active High.
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		MICRO-STAR	
Title			
GPIO SETTING			
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MSI

MICRO-STAR

Title

Revsion History

Size

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0B

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Revision Initial ver:0B

1. Modify resistor & capacitor value for Audio precision test. R216, R219 change from10kto1k,C109,C116 change from 1000p to 560p, R215 change from 1k to 100 ohm, C106 changefrom001ufo0.1uf,C107 change from 1000p to 390p, C99, C103 change from 1000pto330p.

2. Change some capacitor for MEM_STR & DDR_VTT from 470uF to 1000uF(CT27,CT26,CT72).

3. L27 use dual footprint for 0805 & 1206 size.(p/n need torequest).

4. Add VCC5 (CT78) bulk capacitor for COM&LPTpot.

5. Change SMX_RCOMP & SMY_RCOMP connect to 60 ohm 1% to MEM_STR(add 0.1uf decoupling cap) and 60ohm1%to60nd.

6. Change R521 from 62 ohm to60ohm.

7. R704 default not mount

8. Add resistor for TESTH10 & 12 (R829&R830).

9. Change C323 value to 220p.

10. Delete R145,R338.

11. Change CB62, CB64, CB270 from Y5V to X7R(C11-1042023-W08).

12. Change R523 from 150K to 180K, CB297 change from 1u_0805 to 0.1u_0805(C11-1042014-W08).

13. mount C153 for LPT VCC5 power decouling.

14. Reserve R834 (2.2k ohm) connect to MIC_REF for ADI suggestion.

15. Chagne R149 from 33ohm to0ohm.

16. Chagne R206 from 0 ohm to 33 ohm to improve signalquality.

17. Add R833 (33 ohm) for AC_SYNC to improve overshoot.

18. Change R205 from 33 ohm to 0 ohm for AC_SDOUT to improveovershoot.

19. Reserve CT80, CT81 (10u_16v) for +12V & +5VR power for ADI suggestion.

20. Reserve R835 for SUS_STAT# pullup.

21. Add R836 (33_ohm) for AC_SDOUT to reduce overshoot.

22. Reserve VR9, C336, C337, CT82 for ADI suggestion.

23. Change R410, R419, R431 from 0 ohm_0603 to 10 ohm_0805; R411, R421, R432 from 3.3 ohm_0603 to 3.3 ohm_0805; R413,R425,R434from0ohm_0603to0ohm_0805.

24. Change CB246 from 1u_0805 to 0.1u_0805, CB248 from 1u_0805to0.22u_0805.

25. Reserve capacitor (C335) to PWR_DN# pin, for ICH4 1.5V rail sensitivity issue.

26. Add CT79 for VCC3_SB & R832 for PME# (defaultnotmount).

27. Change R31 from mount to non-mount, R727 from non-mount to mount to set multiplifierfrom6Xto7X.

02/22/Modify

1.SHEET 3 : ADD R837,R838 pull down resistorforPDD7&SDD7.

2.SHEET 11 : Change ADM1027 to EMC6D100 , modify CPU FAN and SYSTEMFAN1circuit.

3.SHEET 19 : Not install L13,L14,L15,L16 ,replace FB32,FB33,FB34,FB35,FB36,FB37,FB38,FB38 and change valuefrom 80ohmto0ohmresistor.

02/25/Modify

1.SHEET 3 : ADD ICS950219 as second source clockgenerator.

2.SHEET 11 : Change R796 to not installed,FAN_CLAMP signal connect to ICH4pinG20GPIO05.

3.SHEET 24: Modify Front Audio Headers Circuit.

4.SHEET 26: Modify 3VDDCDA Circuit,ADDQ91,R850.

5. SHEET 27: Modify MANUAL PARTS, Yellow jumper for JBAT1 (CMOS), Green jumper for JPWD1(PASSWORD), Redjumperfor others.

02/26/Modify

1. SHEET 13: Modify FWH INIT Signal Voltage Conversioncircuit.

2. SHEET 10: Modify SLP_S4#_S5# SignalCircuit.

02/27/Modify

1. SHEET 11: Modify R681 is installed, R679 is not installed.

2. SHEET 24: Connect LOCK# pin 96 from PCI Expansion connector to net PLOCK#.

02/28/Modify

1. SHEET 11: Move R796 to net ADM_PWM and pull-up to VCC2.5,R796 from 8.2K change to 1K, add R855 10K pull-upresistorfor U35pin13.

2. SHEET 11& 10 : Install R848 ,Connect U35 Pin 10 to ICH4pinAA5.

3. SHEET 21:Modify signal SLP_S4#_S5#.

4. SHEET 26: ADD L32,L33,L34,C339,C340,C341forRGB filtercircuit.

03/01/Modify

1. SHEET 11: Change CB305 to 1000pF,ConnectCPU_TEM+ to D2+,CPU_TEM- to D2-,D1+ and D1- not installed.

2. SHEET 26: Add net nameQ91_B.

3. SHEET 13: Add net nameQ7_B.

4. SHEET 26: Modify RGB filter circuit, change D25 to notinstalled.

5. SHEET 11: Add CB324 33uF capacitor.

03/02/Modify

1. SHEET 9: Change R632,R633,R634,R635,R636,R637,R122,R638to0ohm.

2. SHEET 18: Change R704 to installed.

03/05/Modify

1. SHEET 12: Modify Audio codec regulatorcircuit.

2. SHEET 5:Change ECI part.

3. SHEET 21: Change CT12 to 100uF.

4. SHEET 8: Change CT11 to 100uF.

5. SHEET 20: Change CT36,CT37 to 100uF.

6. SHEET 14: Change CT24 to 100uF.

7. SHEET 8: Change CT16 to 1000uF.

8. SHEET 24: Change CT76,CT77 to 100uF.

9. Change CT14,CT13,CT31,CT70,CT26,CT47 to not installed.

10. SHEET 22: Change CM8500 toCM8501/A.

03/06/Modify

1. SHEET 22 : Change CM8501A toSOP8.

2. SHEET 11: Change U35 pin 22 (VCC2_5)toMEM_STR.

03/07/Modify

1. SHEET 12 : Change R215 to 1Kohm.

03/08/Modify

1. SHEET 12 : Change C106 to 0.01uF , Change R199 to not installed, Add Max Bracket Header Circuit .

2. SHEET 10: Remove SYSMAG_INT from pin AA5.Connect net SYSMAG_INTto ICH4pin A6(GPIO1).

3. SHEET 16: Change AGP SLOT connector pin B6 connect to net INTD#ChangepinA6 connect to INTD#.

03/12/Modify

1. SHEET 06 : Change R137 to 137%1ohm.

03/13/Modify

1. SHEET 10 : Add R177 8.2K ohm pull-up VCC3_SBforGPIO12.

2. SHEET 10 : Add R857 8.2K ohm pull-up VCC3forGPIO18.

3. SHEET 10 : Add R858 8.2K ohm pull-up VCC3forGPIO20.

4. SHEET 10 : Add R860 8.2K ohm pull-up VCC3forGPIO24.

5. SHEET 13 : Add R859 8.2K ohm pull-up VCC3forPRESS3.

6. SHEET 21 : Change Q56,Q57,Q87to 12N03L-T0252.

03/14/Modify

1. SHEET 12 : Remove Max Bracket Header Circuit.

03/15/Modify

1. SHEET 12 : Add Decoupling Capacitor.

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