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Last Schematic Update Date:
10/29/2002 V20b

MS-6535

VERSION:2.0B

SIS 651 CHIPSET

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System SIS651 Chipset:

**SIS 651 (North Bridge B0)
+ 962L (South Bridge C1)**

On Board Chip:

LPC Super I/O -- W83697HF_UB

BIOS -- ISA

AC' 97 CODEC -- ALC650 Ver:F

CLOCK GENERATION -- ICS 952001

LAN -- RTL8101L

PCMCIA -- OZ6933

DVO -- SIS301B DVI + TV-OUT + 2nd CRT

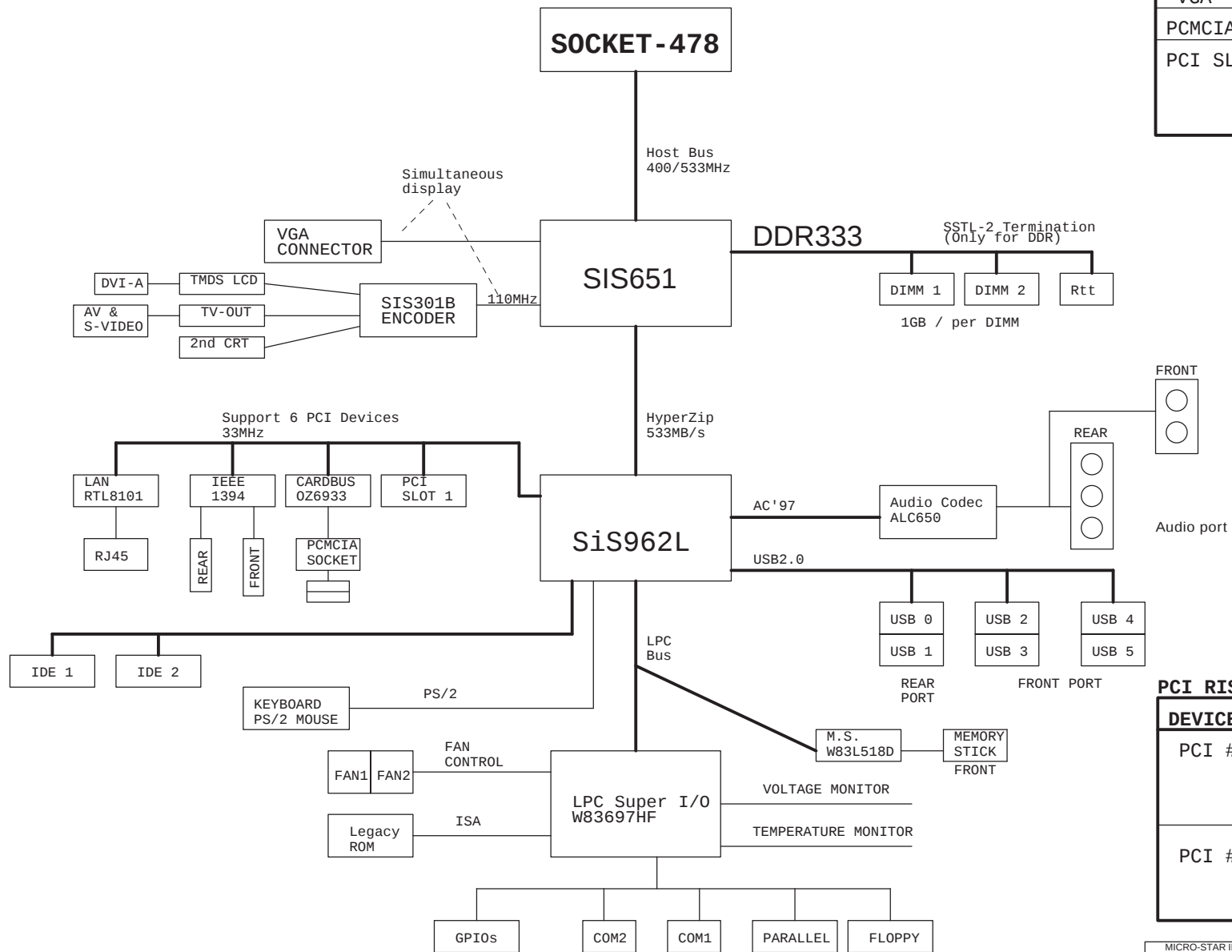
1394 -- NEC72874- 2ports VER:E

MEMORY STICK -- W83L518D Ver:B

Expansion Slots:

PCI2.2 SLOT* 1 (RISER CARD PCI*2)

System Block Diagram



PCI DEVICE ROUTING TABLE

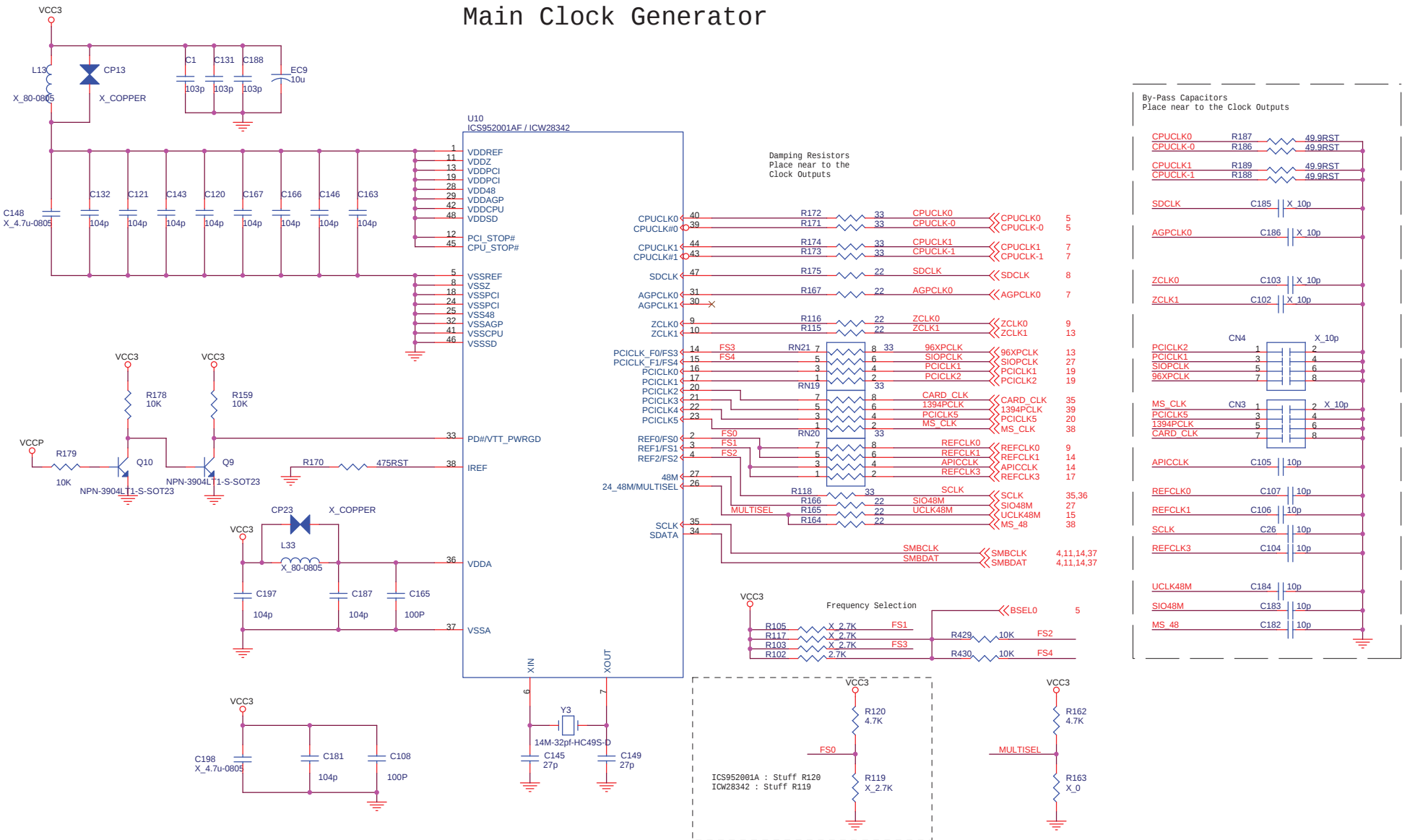
DEVICE	INT pin	IDSEL
1394	INTD#	AD23
LAN	INTC#	AD26
MODEM	INTB#	
VGA	INTA#	
PCMCIA	INTB#	AD25
PCI SLOT	INTB# INTC# INTD# INTA#	AD17

PCI RISER

DEVICE	INT pin	IDSEL
PCI #1	INTB# INTC# INTD# INTA#	AD17
PCI #2	INTC# INTD# INTA# INTB#	AD18

MICRO-STAR INT'L CO.,LTD.			
Title System Block Diagram			
Size	Document Number		Rev
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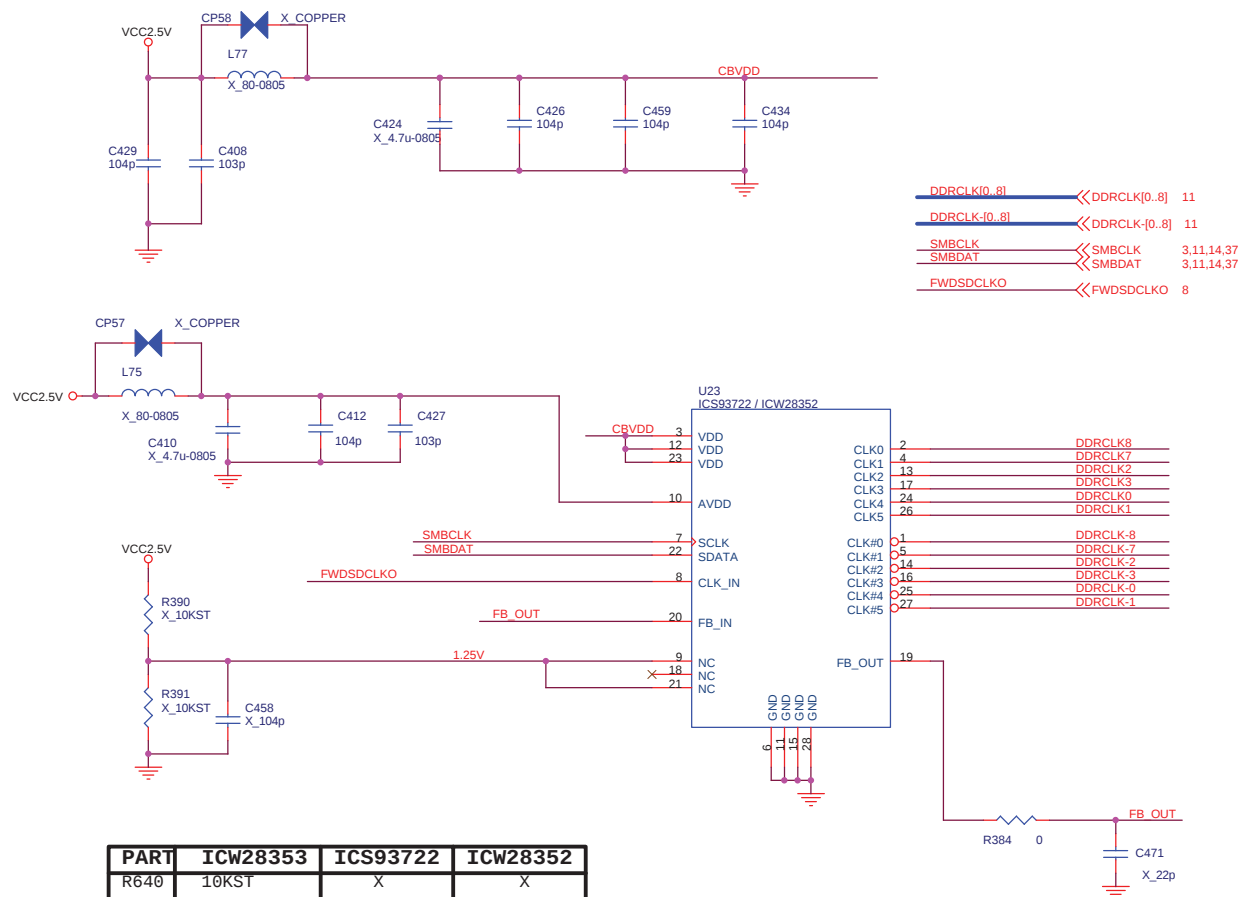
Main Clock Generator



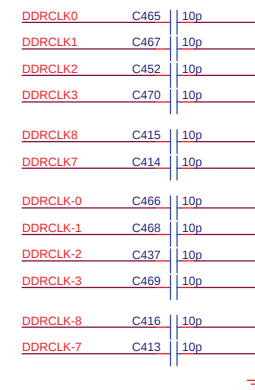
FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	1	100	100	66	66	33
1	0	1	0	1	133	100	66	66	33

Clock Buffer (DDR)

(OPTIONS)
1: (ICS-93785)

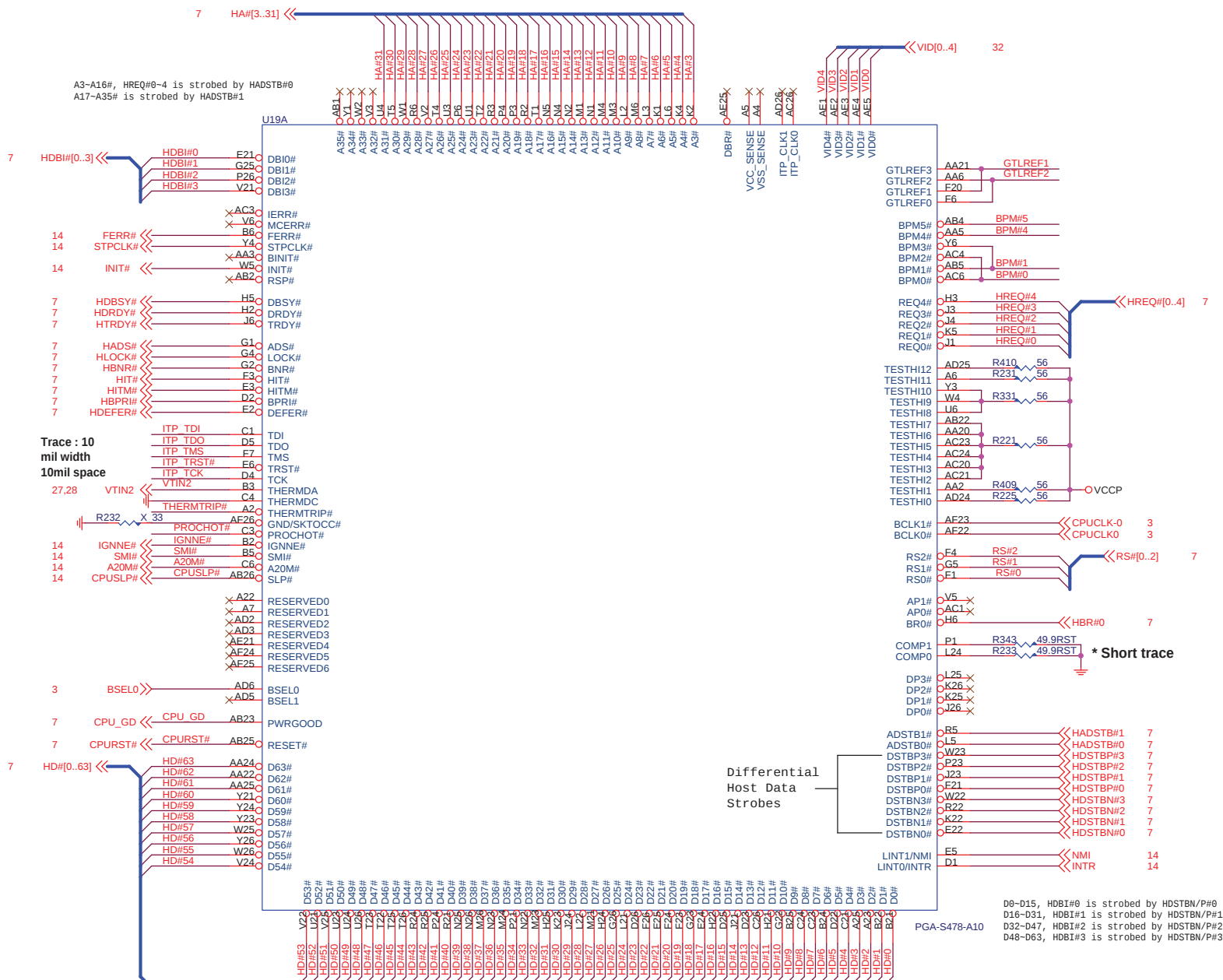


By-Pass Capacitors
Place near to the Clock Buffer

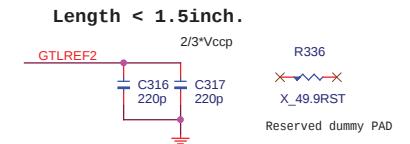
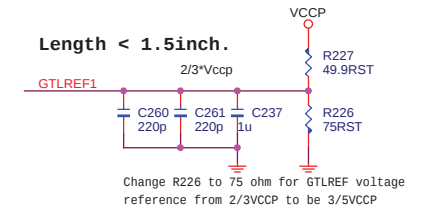


PART	ICW28353	ICS93722	ICW28352
R640	10KST	X	X
R641	10KST	X	X
C642	104p	X	X

CPU SIGNAL BLOCK



CPU GTL REFERENCE VOLTAGE BLOCK



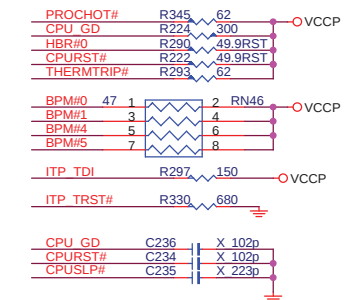
Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



D0-D15, HDBI#0 is strobed by HDSTBN/P#0
D16-D31, HDBI#1 is strobed by HDSTBN/P#1
D32-D47, HDBI#2 is strobed by HDSTBN/P#2
D48-D63, HDBI#3 is strobed by HDSTBN/P#3

PGA-S478-A10

MICRO-STAR INT'L CO.,LTD.

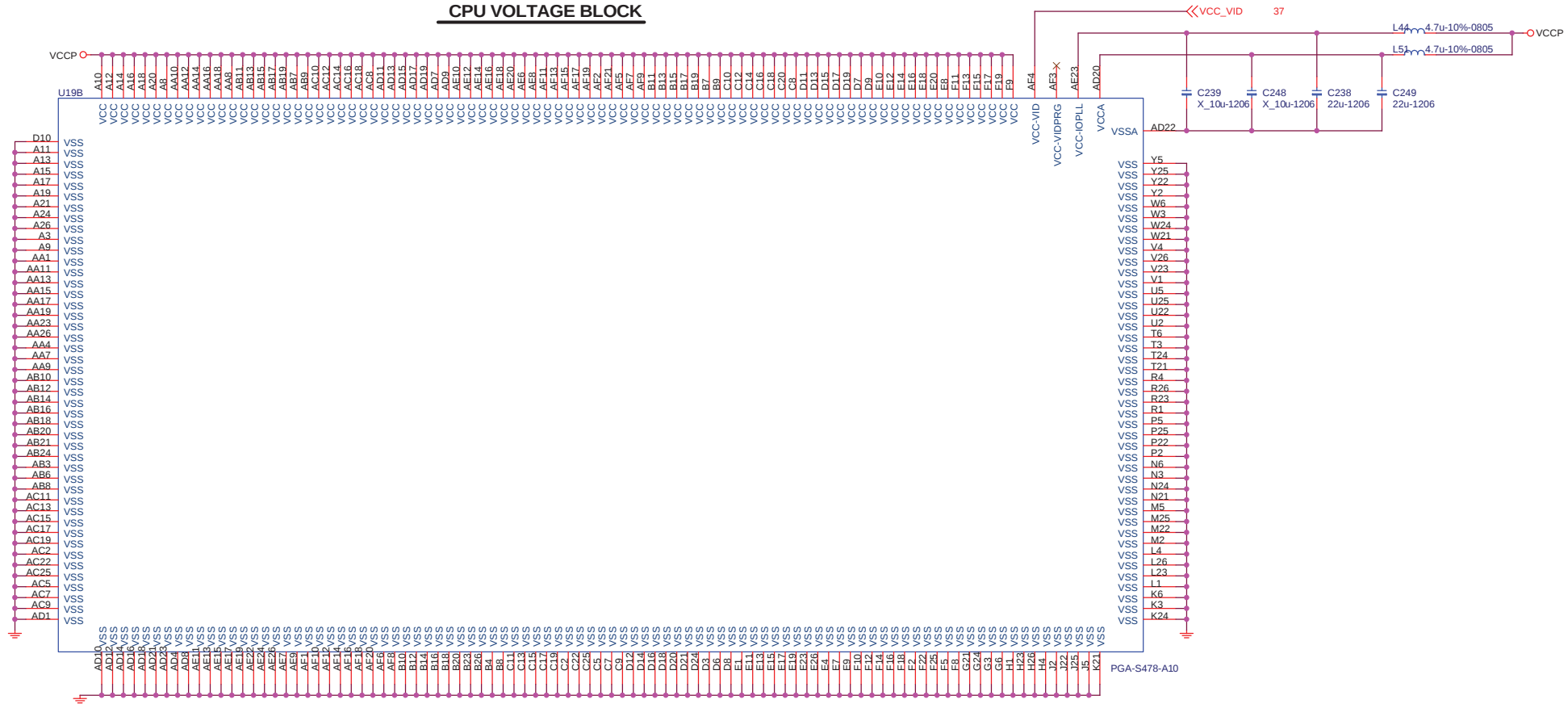
Title	mPGA478 CPU-1
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Size	Document Number MS-6535
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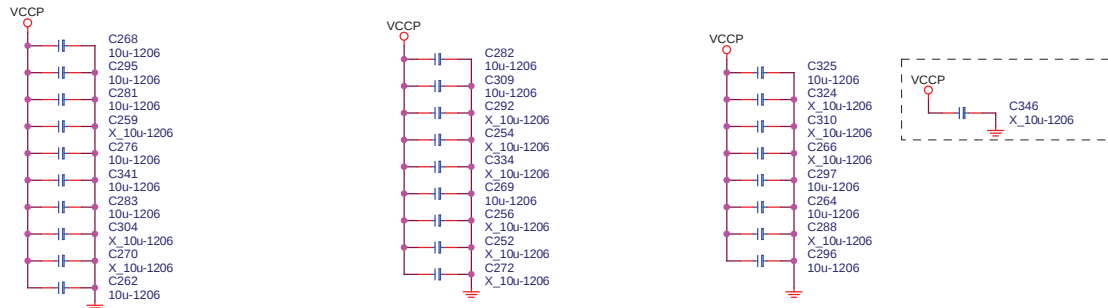
Custom
Date: Friday, January 24, 2003

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CPU VOLTAGE BLOCK

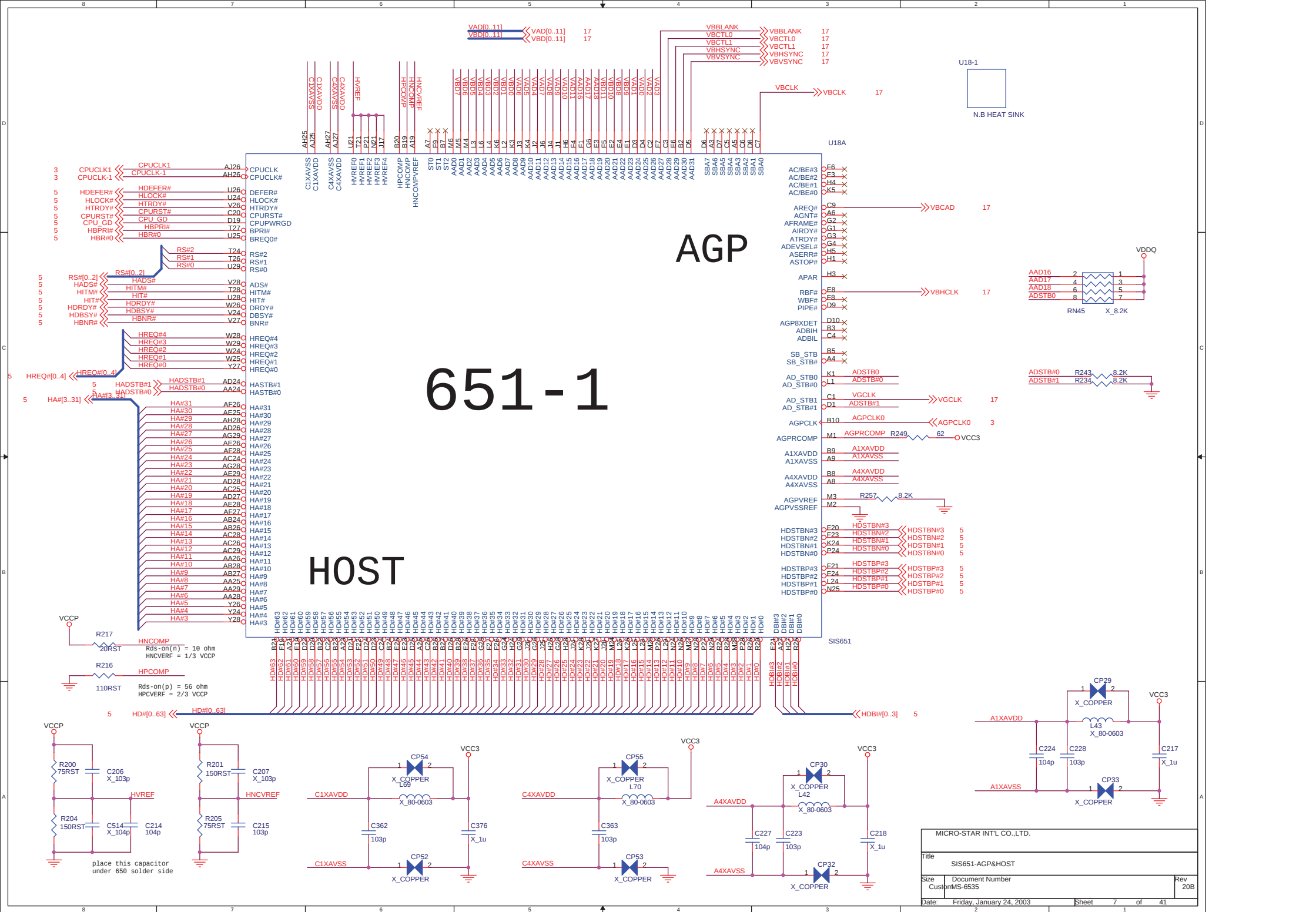


CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

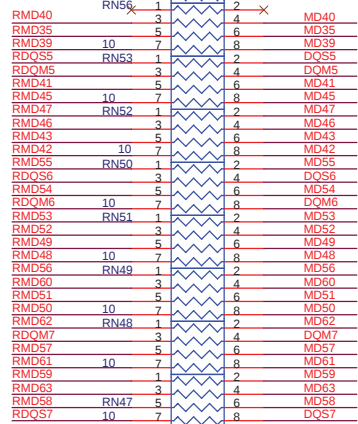
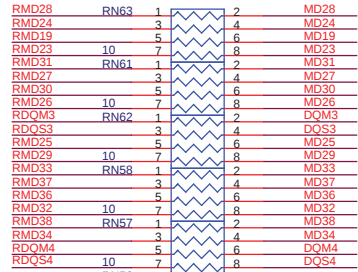
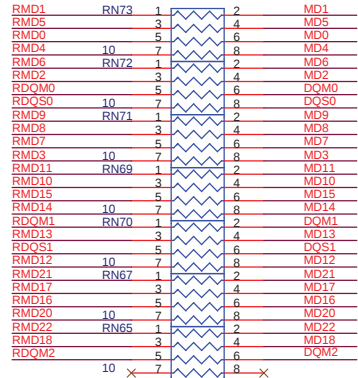
MICRO-STAR INT'L CO.,LTD.			
Title mPGA478 CPU-2			
Size Custom	Document Number MS-6535		Rev 20B
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The L of RN to DDR1 is 0.4"

L = 2"-4"

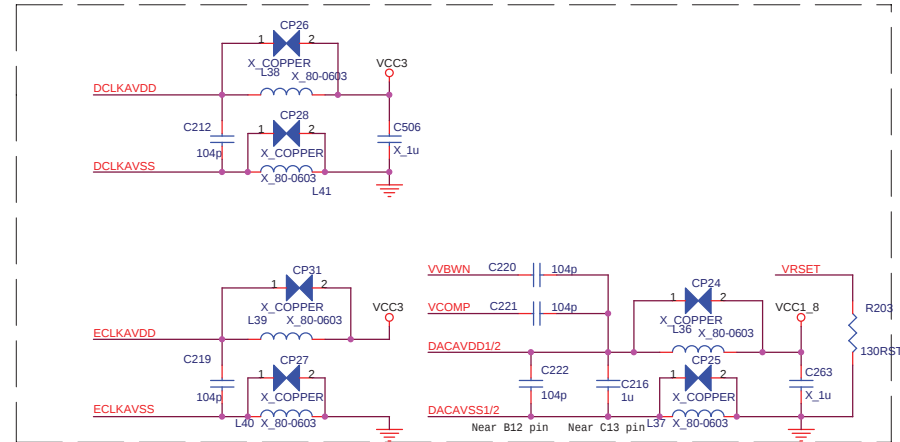
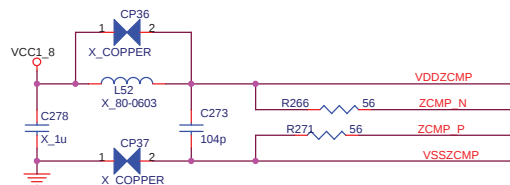
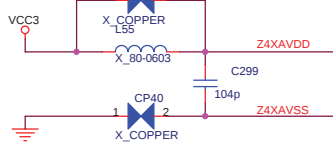
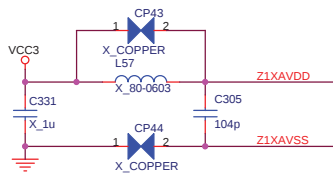
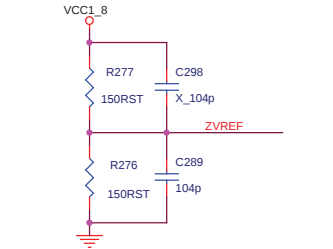
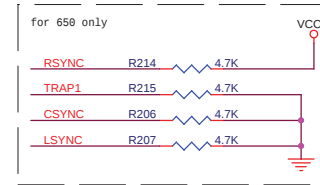
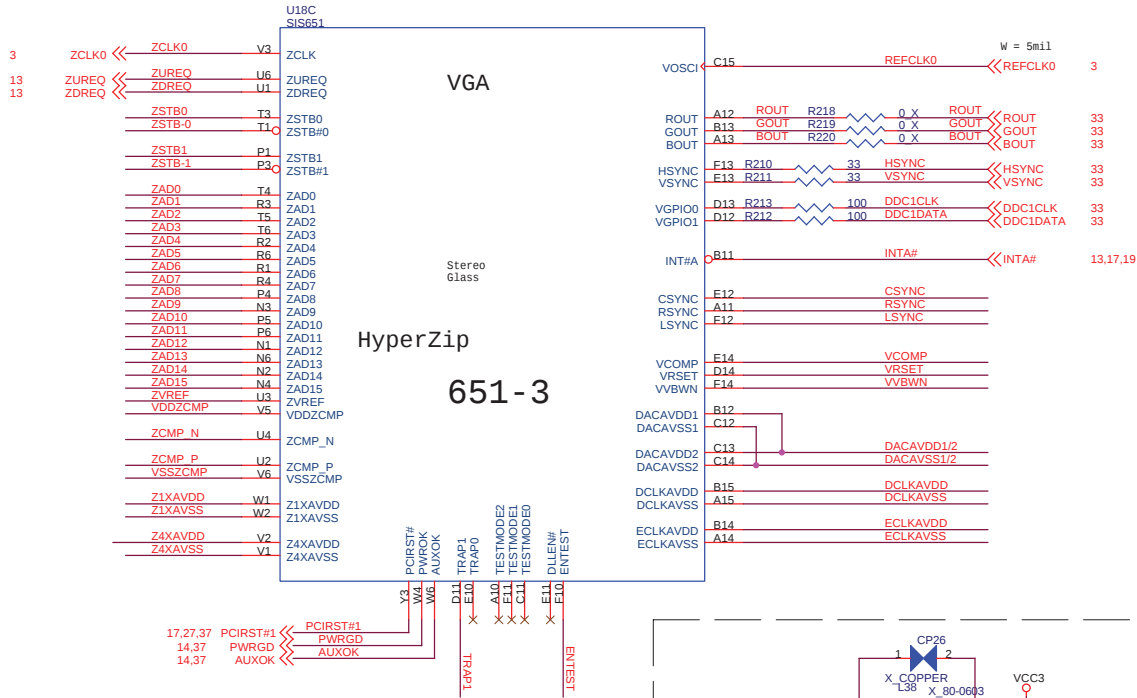
Rs place close to DDR1



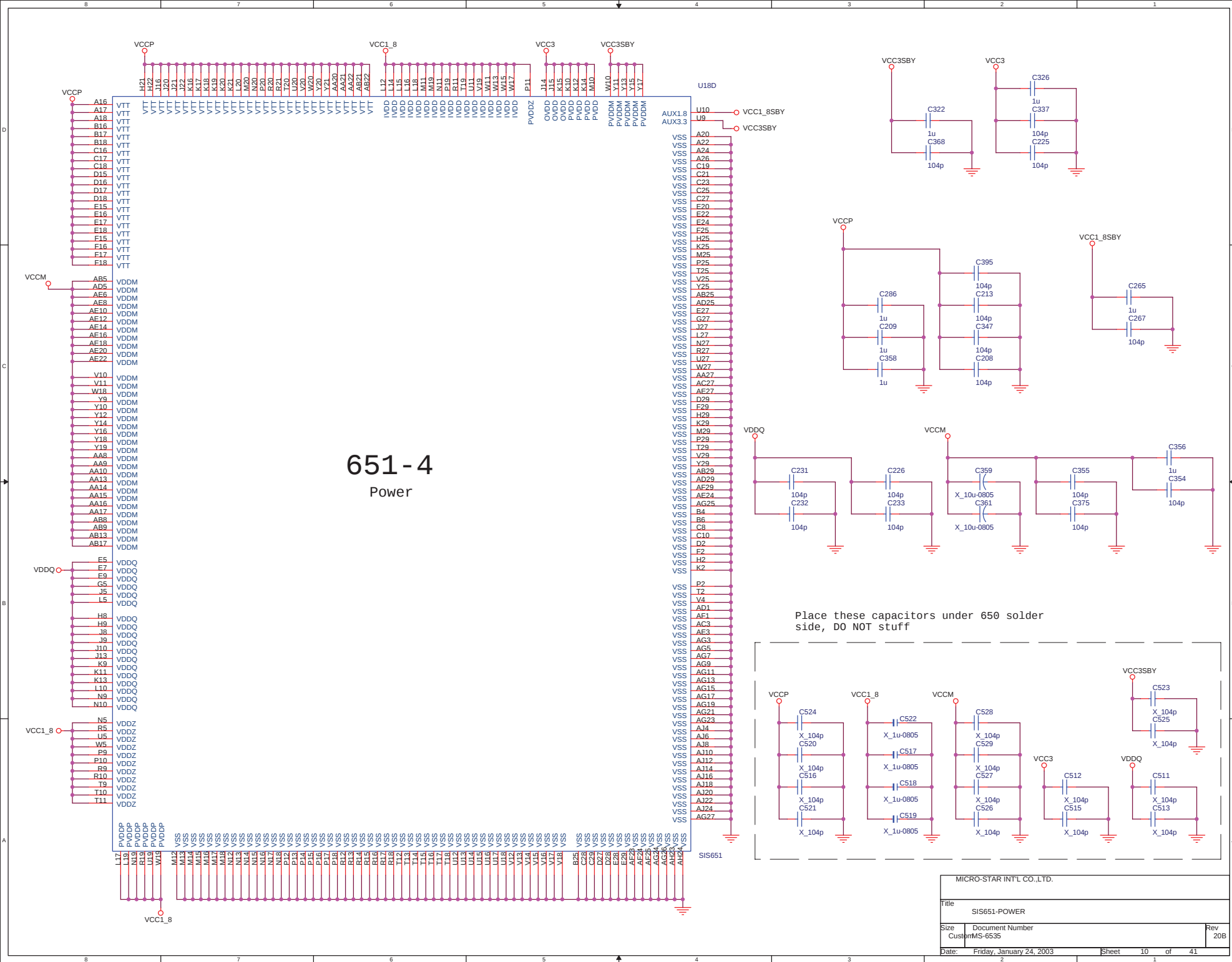
NOTE: This page is for universal PCB design(suitable for both 645 or 650)

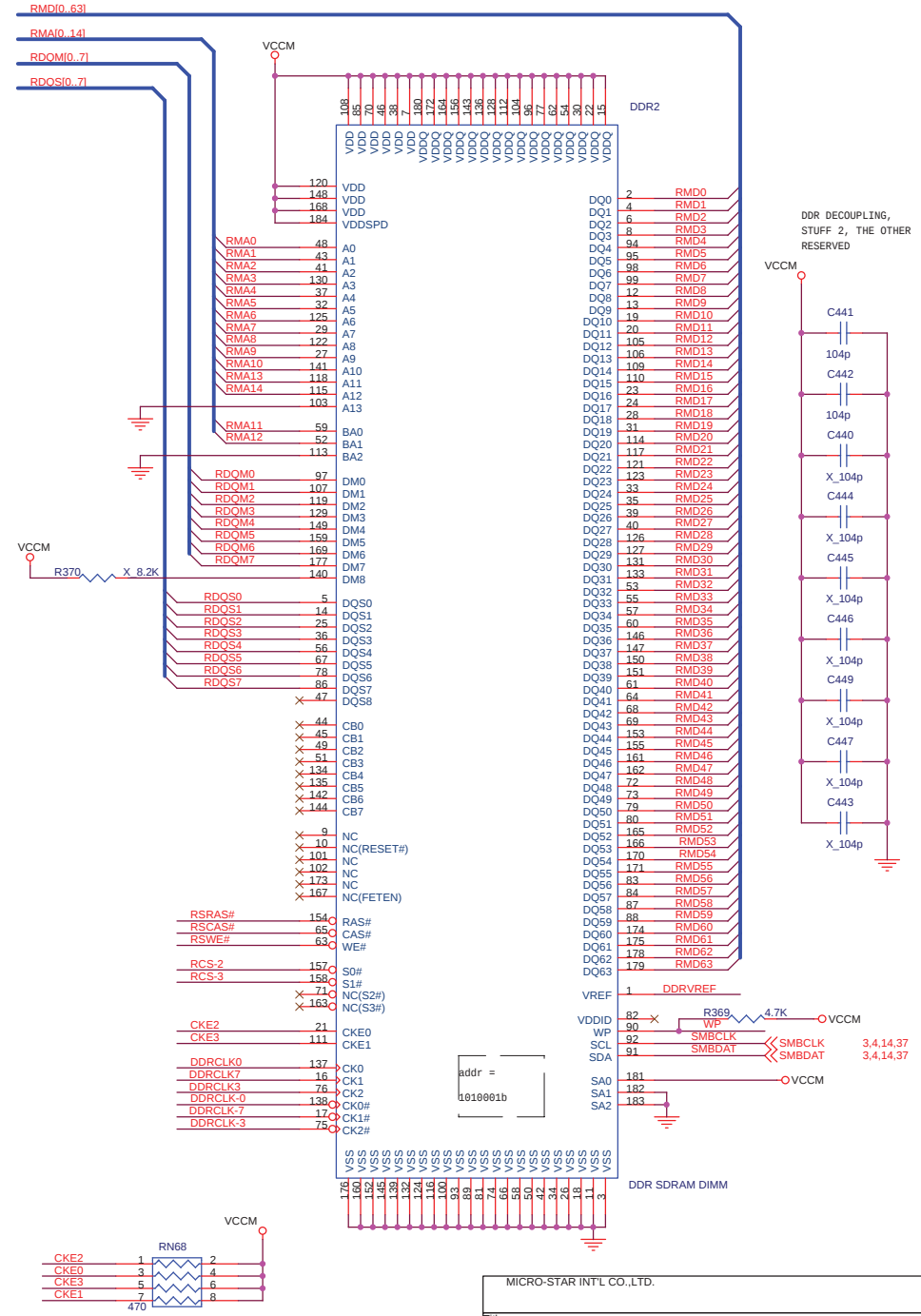
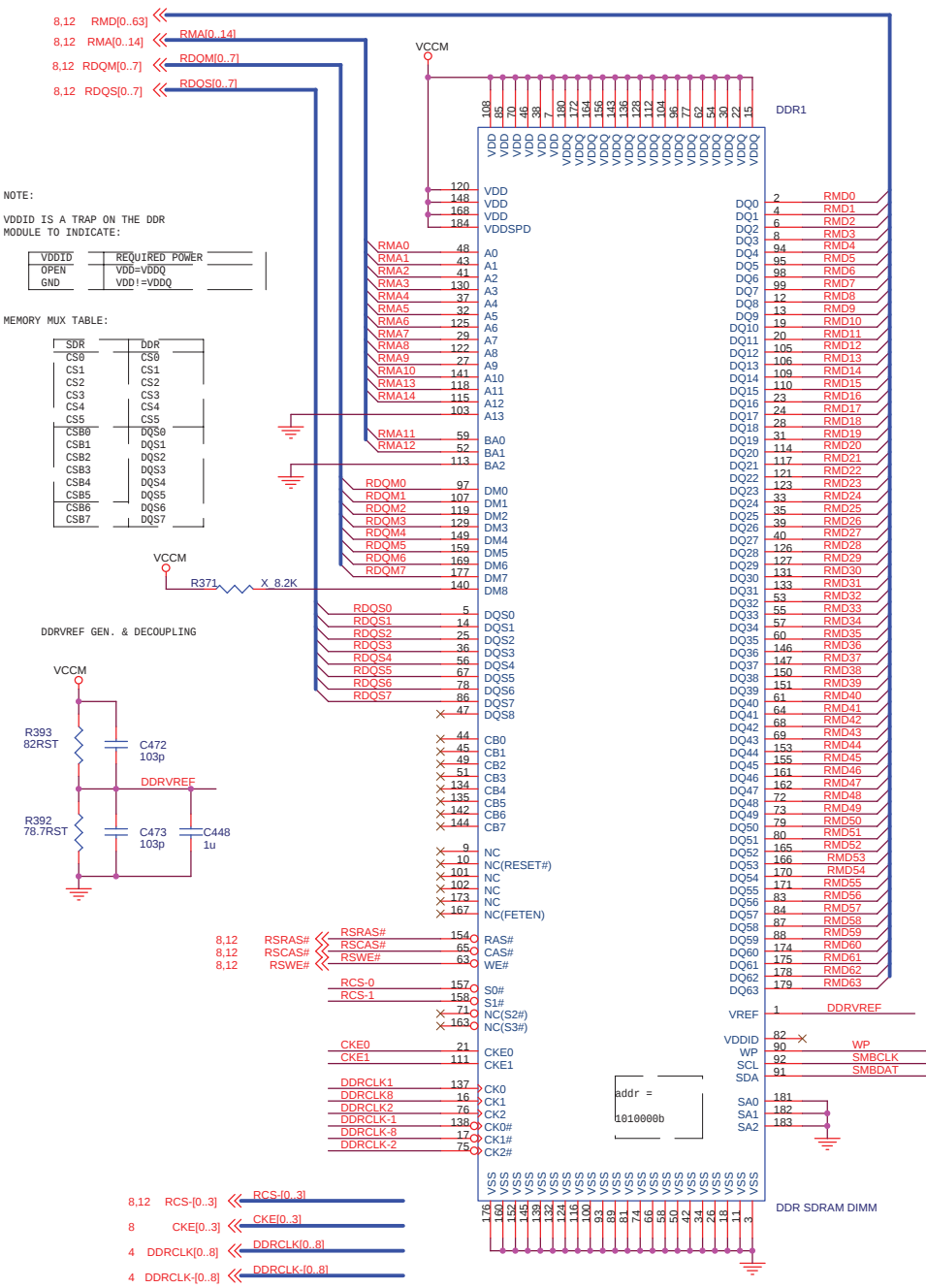
NB Hardware Trap Table

	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAW_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0
CSYNC	enable V8			0
RSYNC	enable VGA interface			1
LSYNC	enable panel link			0



MICRO-STAR INT'L CO.,LTD.			
Title SIS651-VGA & Z-link			
Size Custom	Document Number MS-6535		Rev 20B
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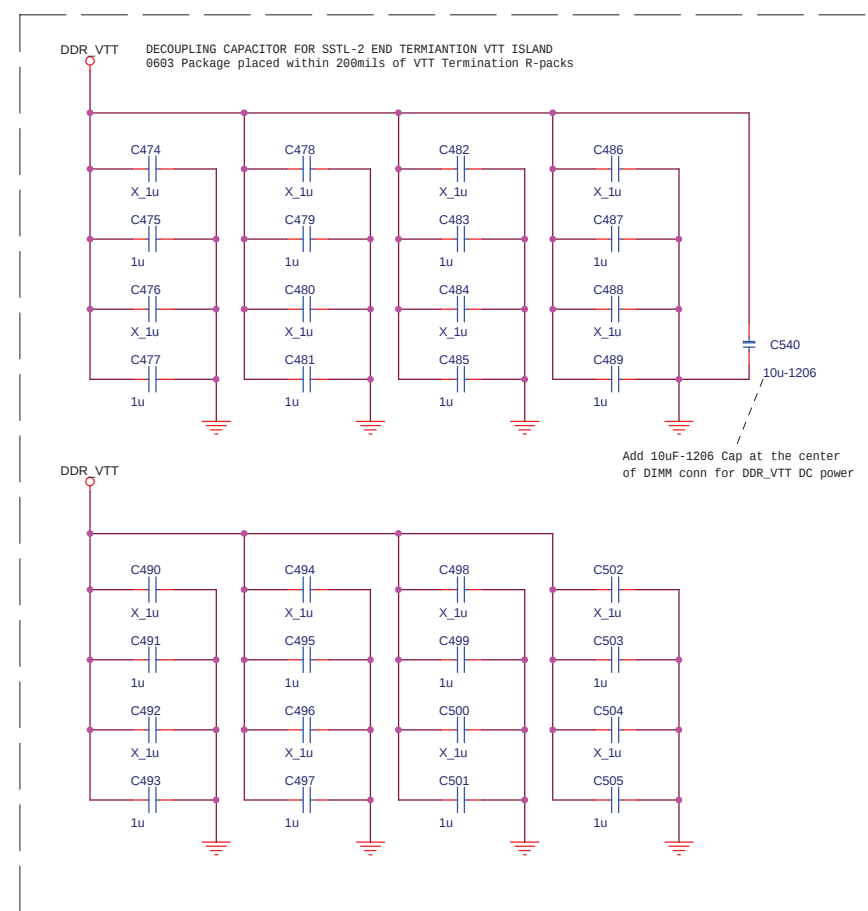
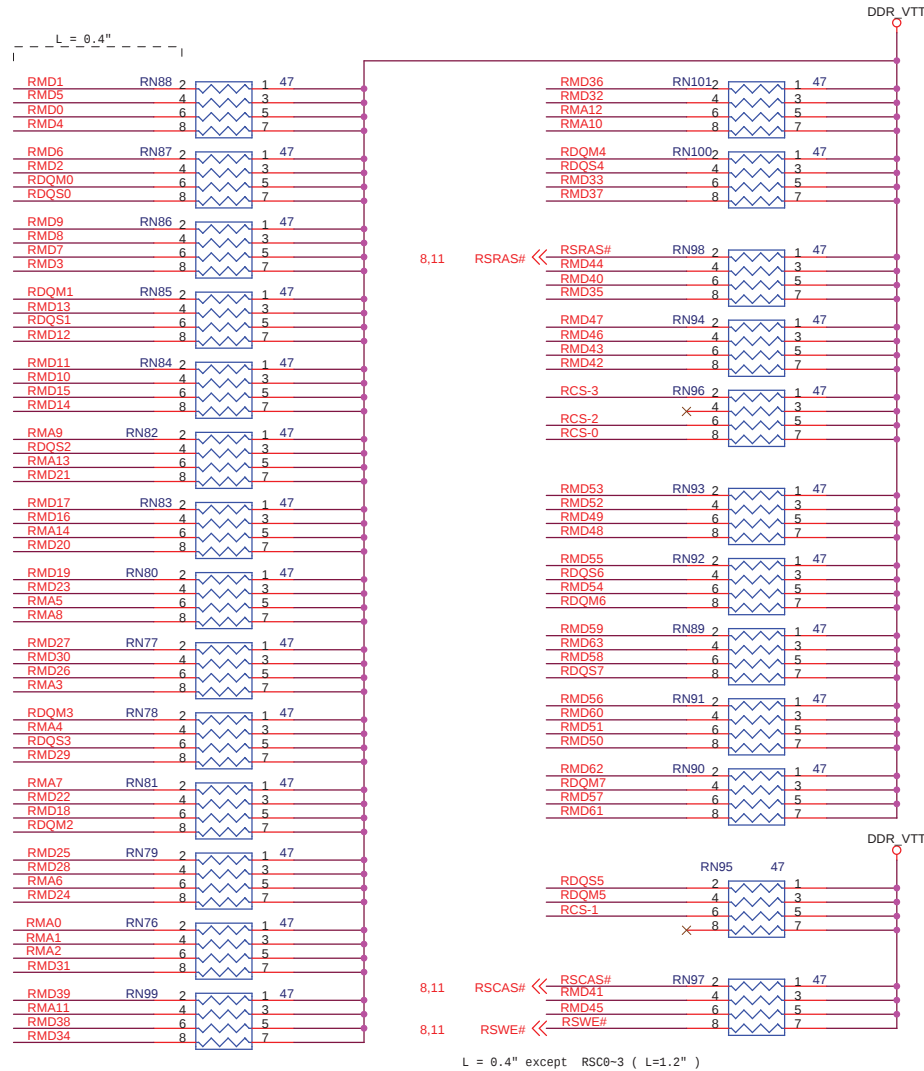




SSTL-2 Termination Resistors

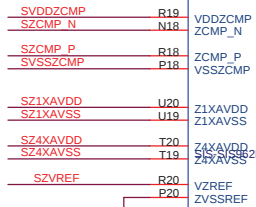
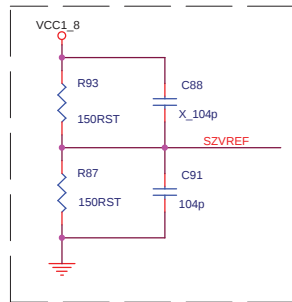
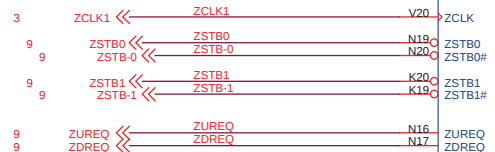
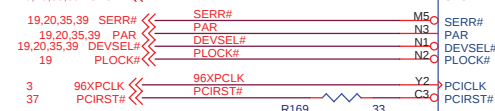
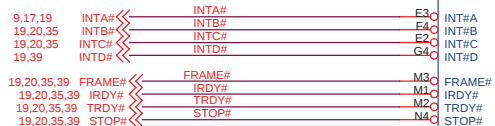
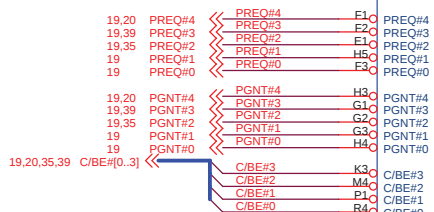
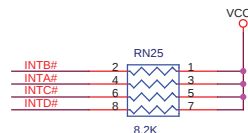
RMD[0..63]	<<RMD[0..63]	8,11
RDOM[0..7]	<<RDQM[0..7]	8,11
RDS[0..7]	<<RDQS[0..7]	8,11
RMA[0..14]	<<RMA[0..14]	8,11
RCS[0..3]	<<RCS[0..3]	8,11

	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	RS	SSTL-2	RS	47
MA/Control	LV-CMOS	10/10/-	SSTL-2	47	
CS	LV-CMOS	10	SSTL-2	47	
CKE	DD 3.3V		DD 2.5V		



Did not stuff C476, C479, C482, C485, C488, C491, C494, C497, C500, C503 for DDR_VTT OK

MICRO-STAR INT'L CO.,LTD.			
Title DDR TERMINATOR			
Size Custom	Document Number MS-6535	Rev 20B	
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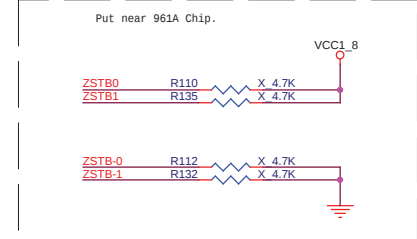
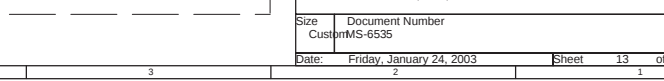
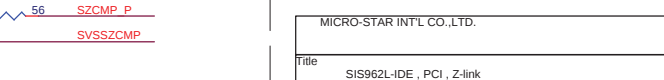
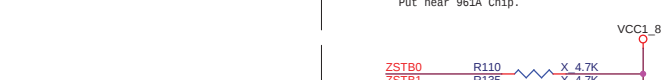
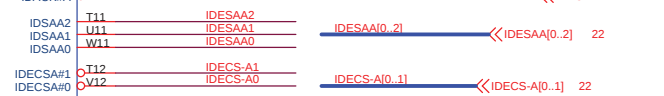


PCI

IDE

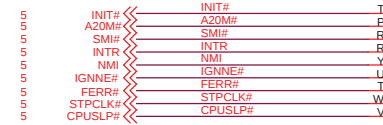
962L-1

HyperZip



MICRO-STAR INT'L CO.,LTD.			
Title SIS962L-IDE , PCI , Z-link			
Size CustomMS-6535	Document Number	Rev 20B	
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Programmable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)

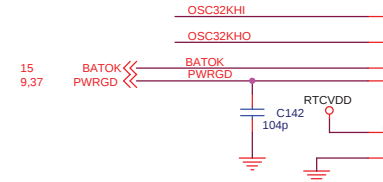
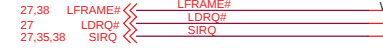


CPU_S



APIC

LPC

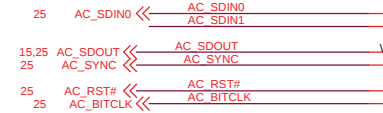


RTC

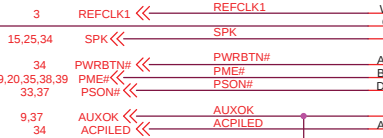
962L-2



GPIO



AC97



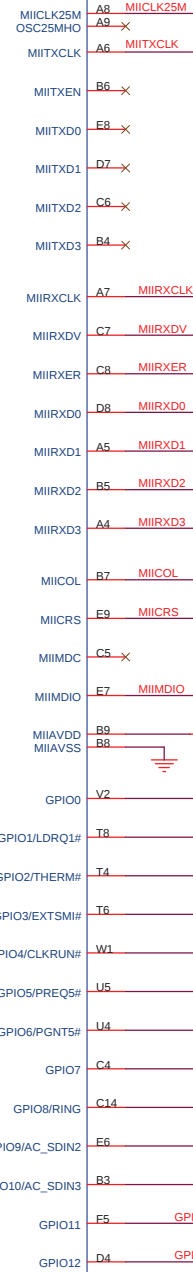
ACPI
/others



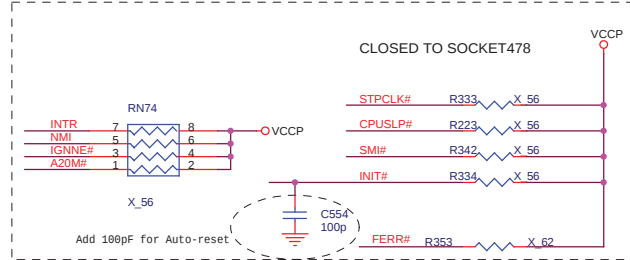
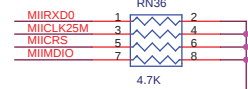
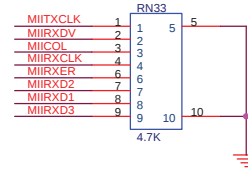
KBC
/geyserville



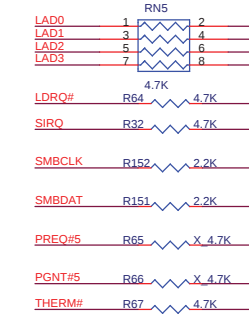
GPIO pins pull down
NEED NOT to place
close to 962



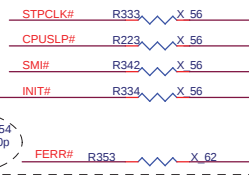
MII



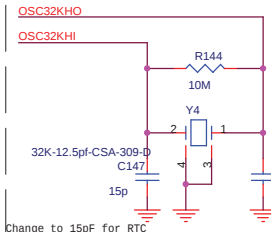
NEED NOT to place
close to 962



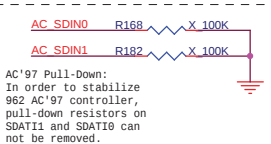
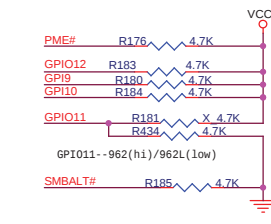
CLOSED TO SOCKET478



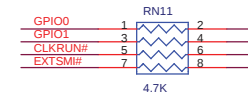
Put closed to 962 CHIP



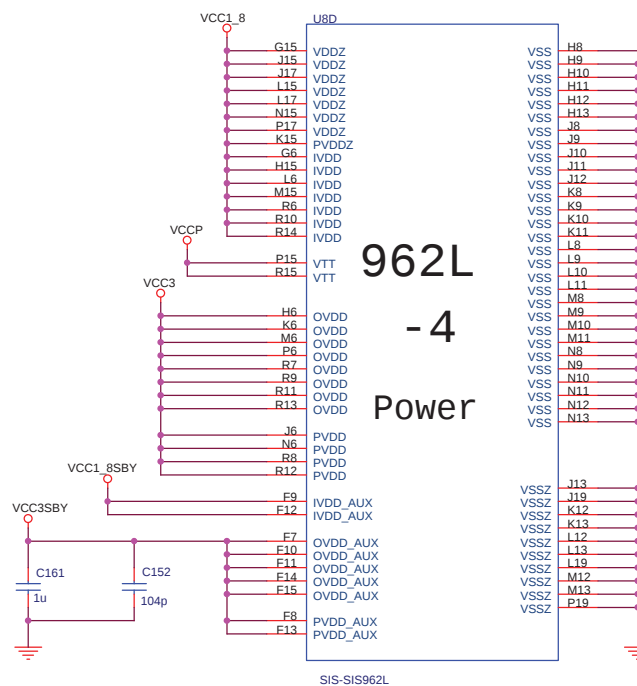
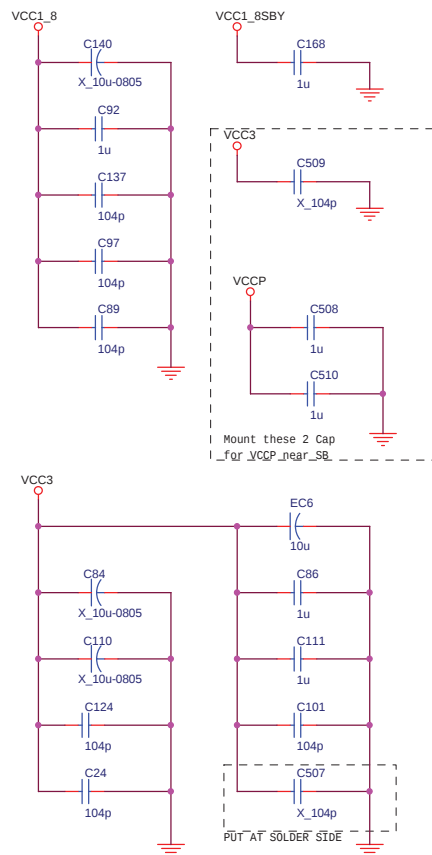
Change to 15pF for RTC

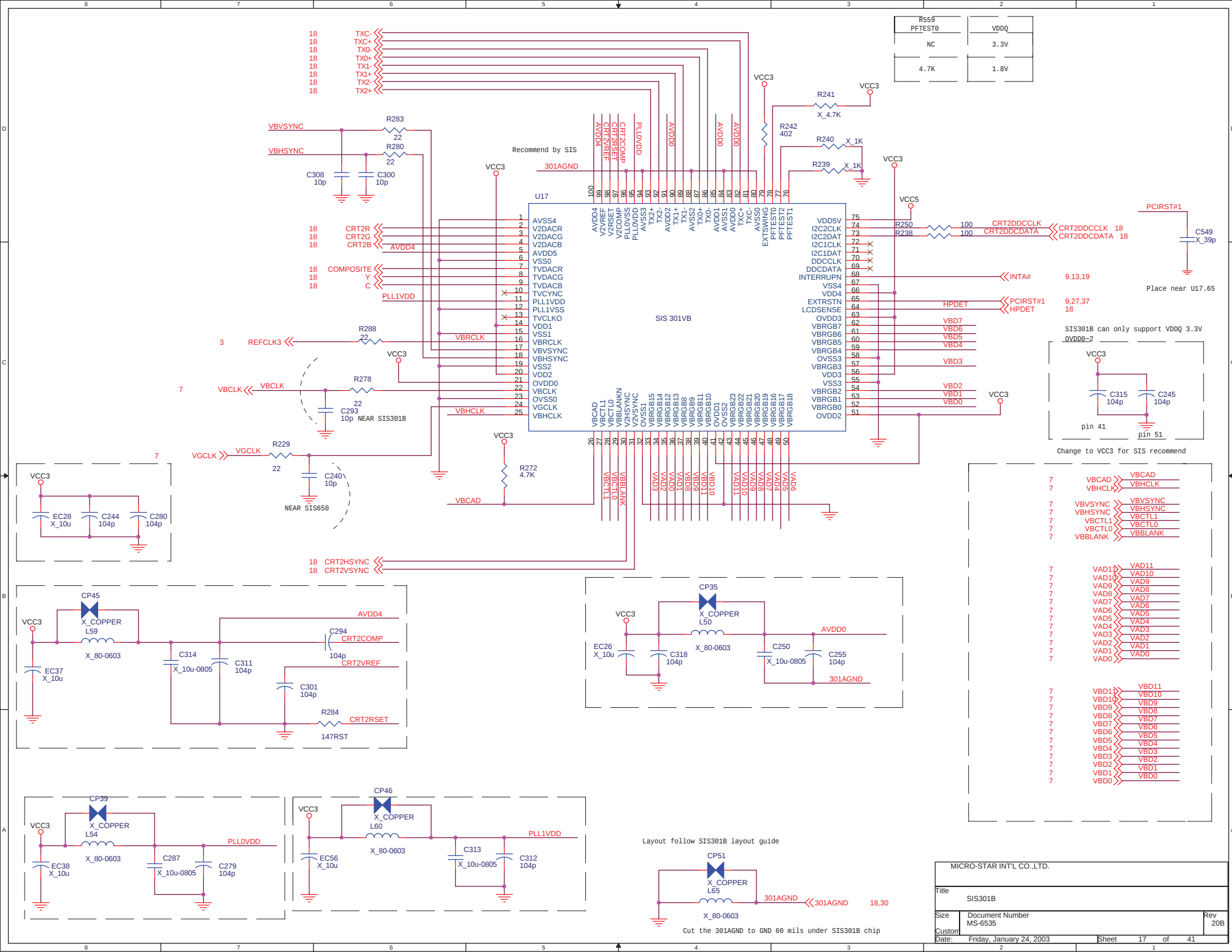


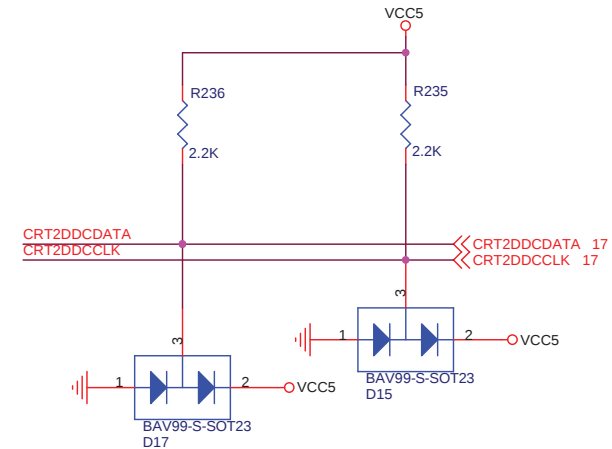
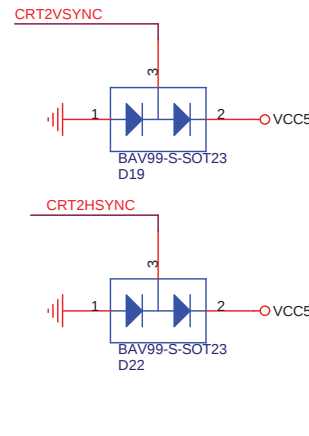
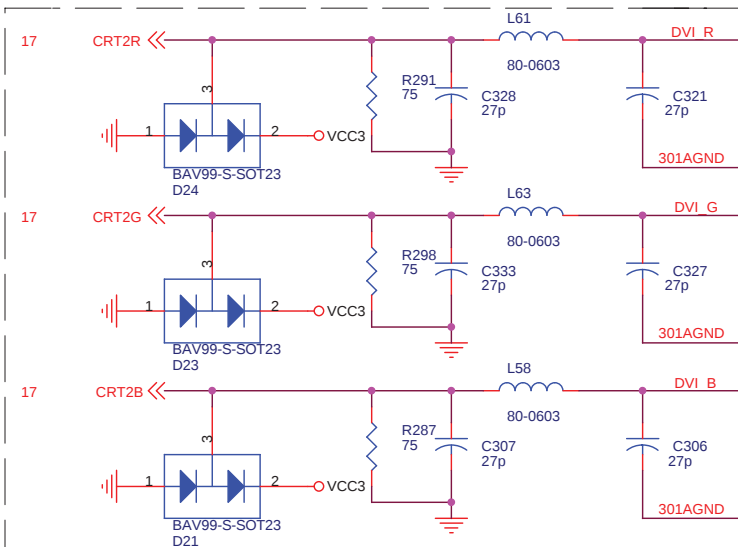
AC'97 Pull-down:
In order to stabilize
962 AC'97 controller,
pull-down resistors on
SDAT11 and SDAT10 can
not be removed



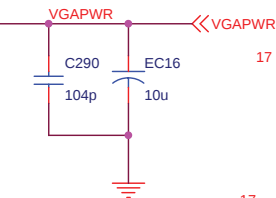
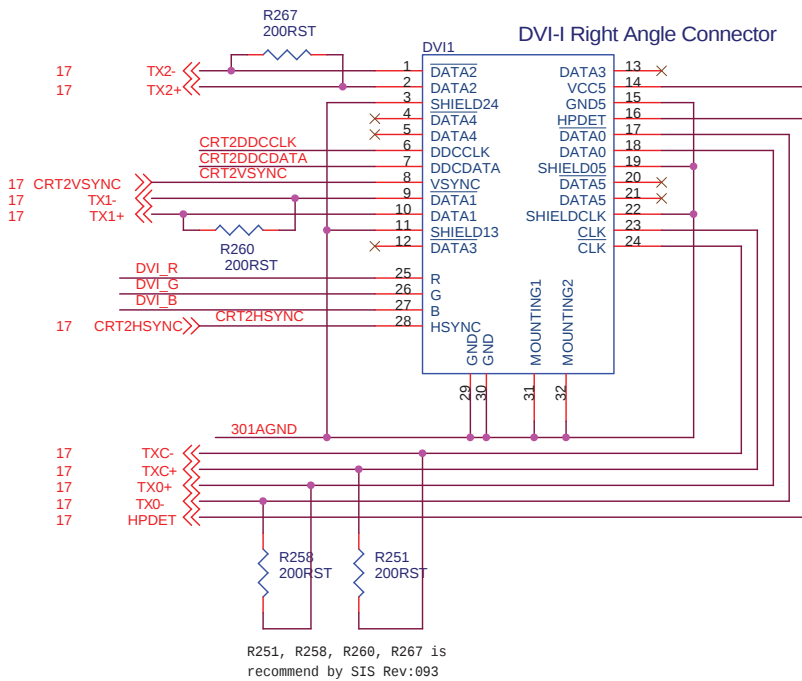
MICRO-STAR INT'L CO.,LTD.			
Title SIS962L-MISC			
Size Custom	Document Number MS-6535	Rev 20B	
Date: Friday, January 24, 2003	Sheet 14	of 41	



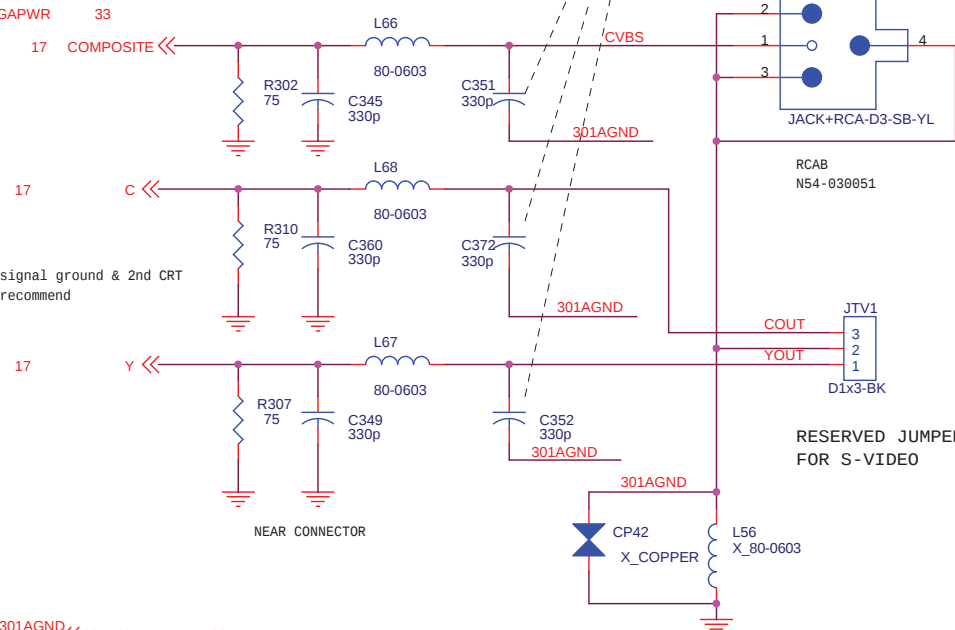
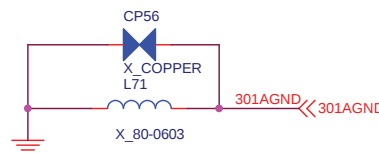




DVI Interface



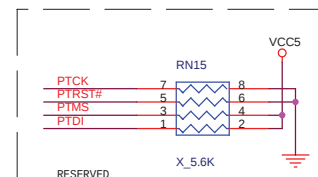
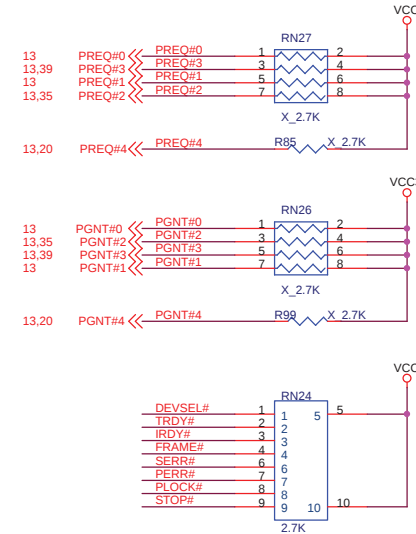
Connect the DVI, TV, TMS signal ground & 2nd CRT ground to 301AGND for SIS recommend



MSI COMPUTER			
Title DVI, TV-OUT, 2nd CRT CONN			
Size Custom	Document Number MS-6535		Rev 20B
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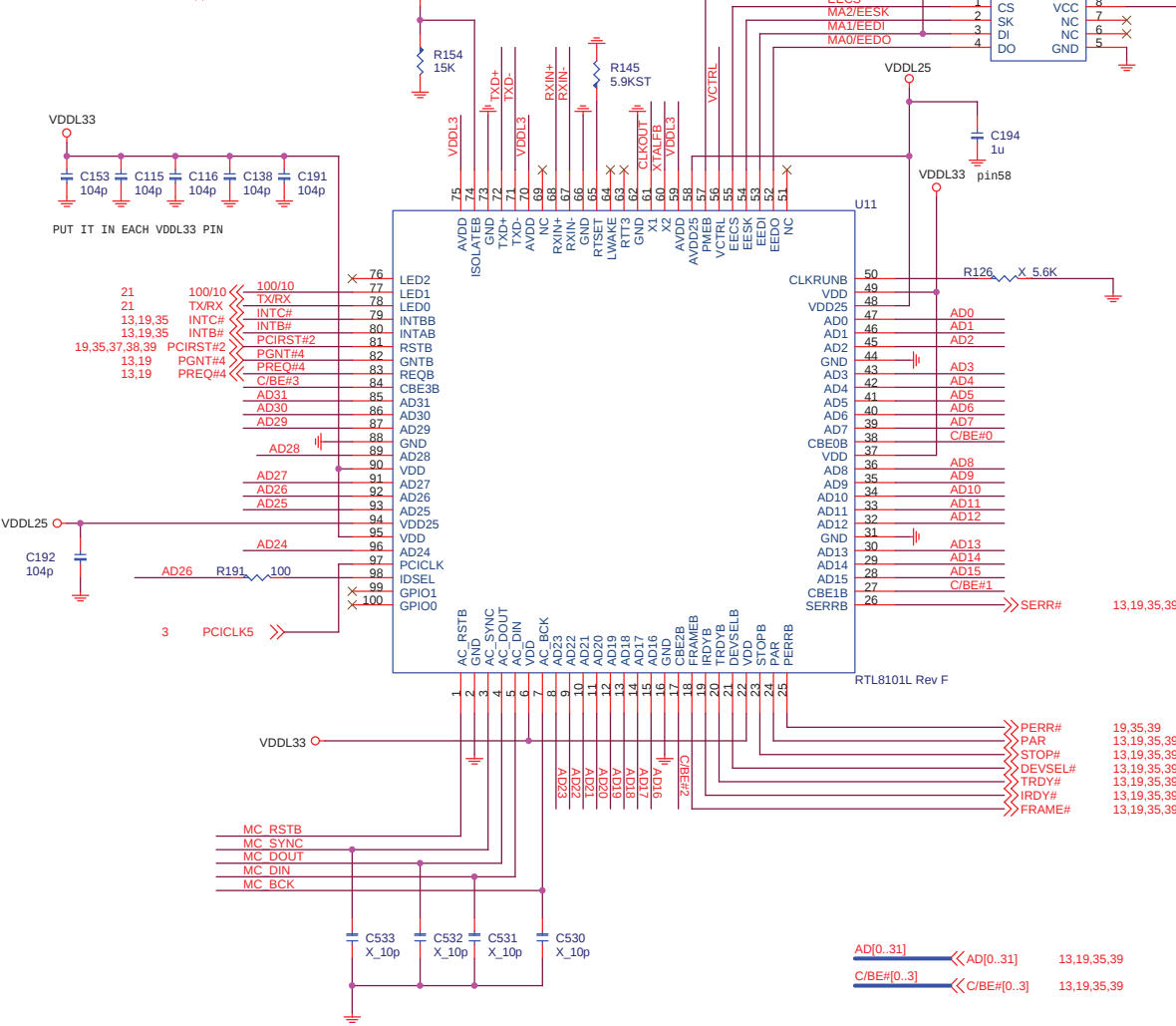
AD17
INTB#

PCI BUS PULL-UP

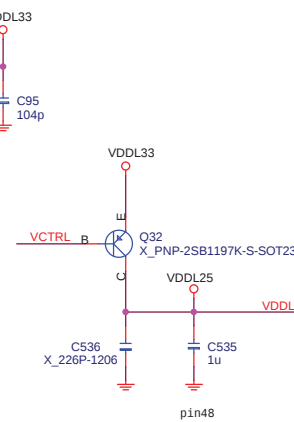
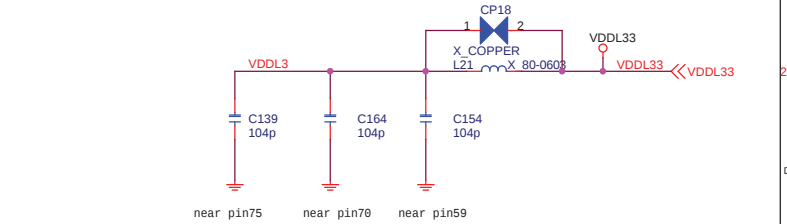


RTL8101 LAN + MODEM

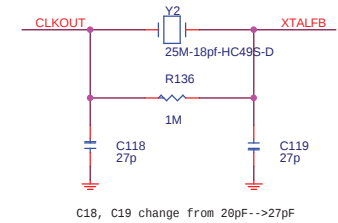
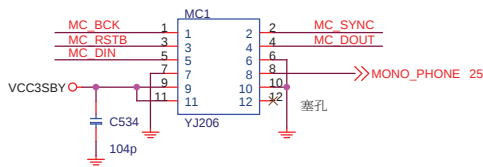
LAN = INTC#
MODEM = INTB#
AD26



THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.

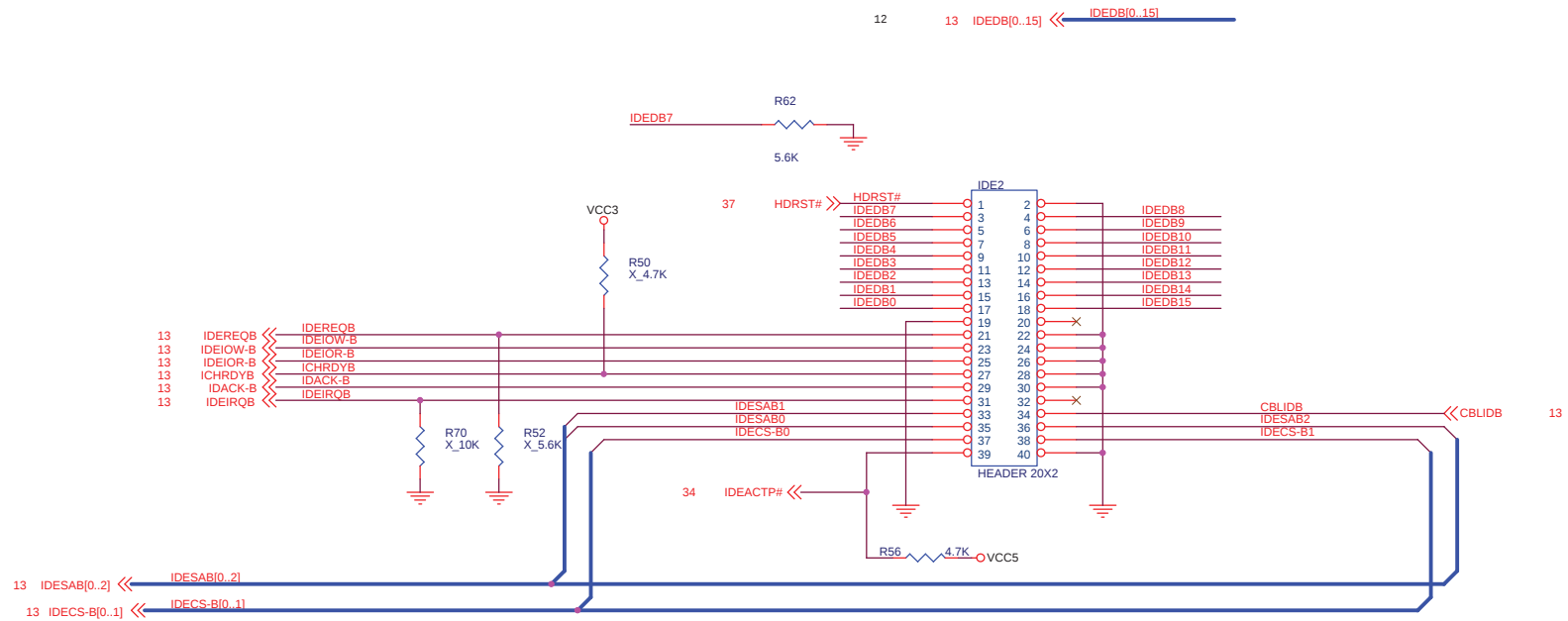
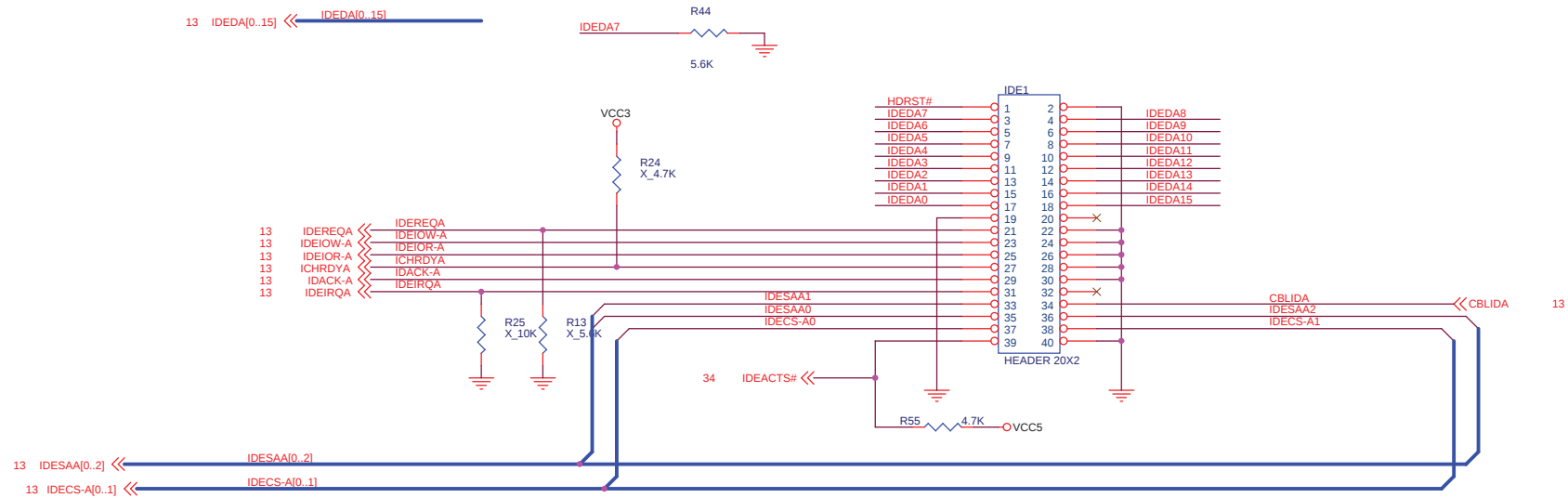


Did not mount Q32 & C536 unless VDDL25 is not stable. VDDL25 is derived from RTL8101 (from D version).



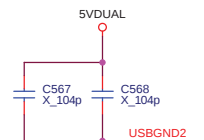
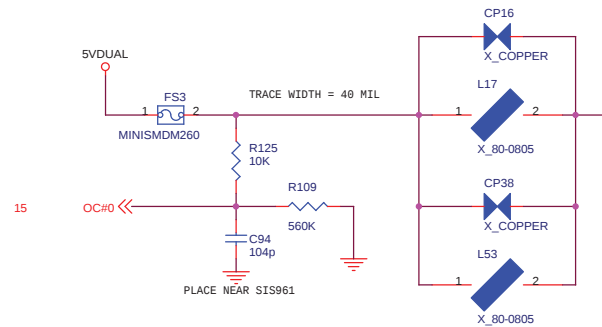
AD[0..31] <-> AD[0..31] 13,19,35,39
C/BE#[0..3] <-> C/BE#[0..3] 13,19,35,39

MICRO-STAR INT'L CO., LTD.			
Title LAN CONTROLLER			
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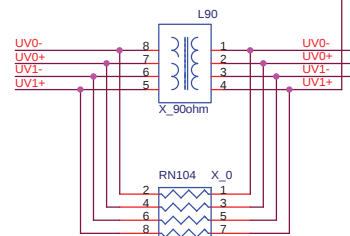


The series esistor of " IDESAB0-2, IDECS-B0-1, IDEIOR-B, IDEIOW-B, IDACK-B " is close to SIS650. The others is near connector

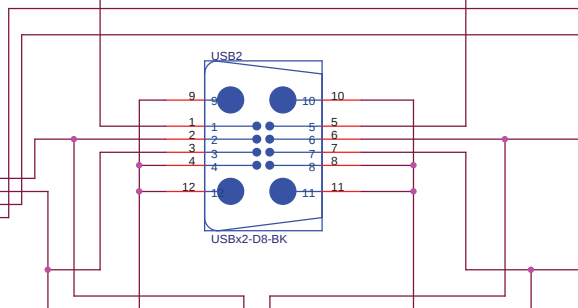
MICRO-STAR INT'L CO.,LTD.			
Title IDE CONNECTOR			
Size	Document Number		Rev
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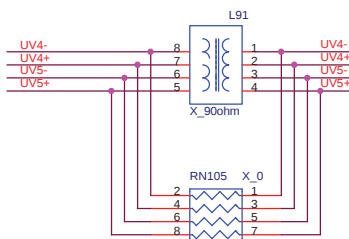
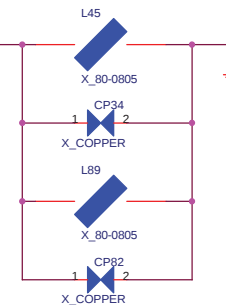
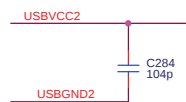
FOR EMI



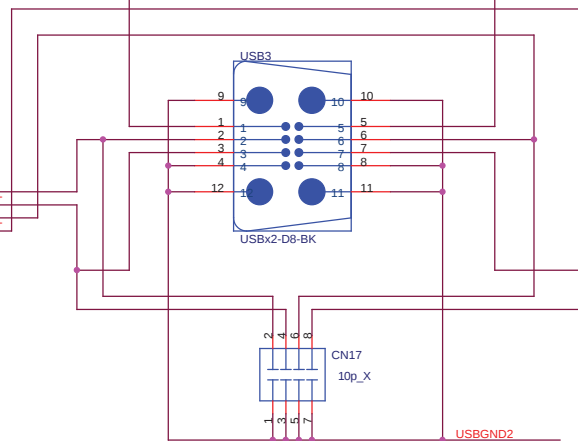
USB port 0,1
connector (FRONT)



USB port 4,5
connector (FRONT)

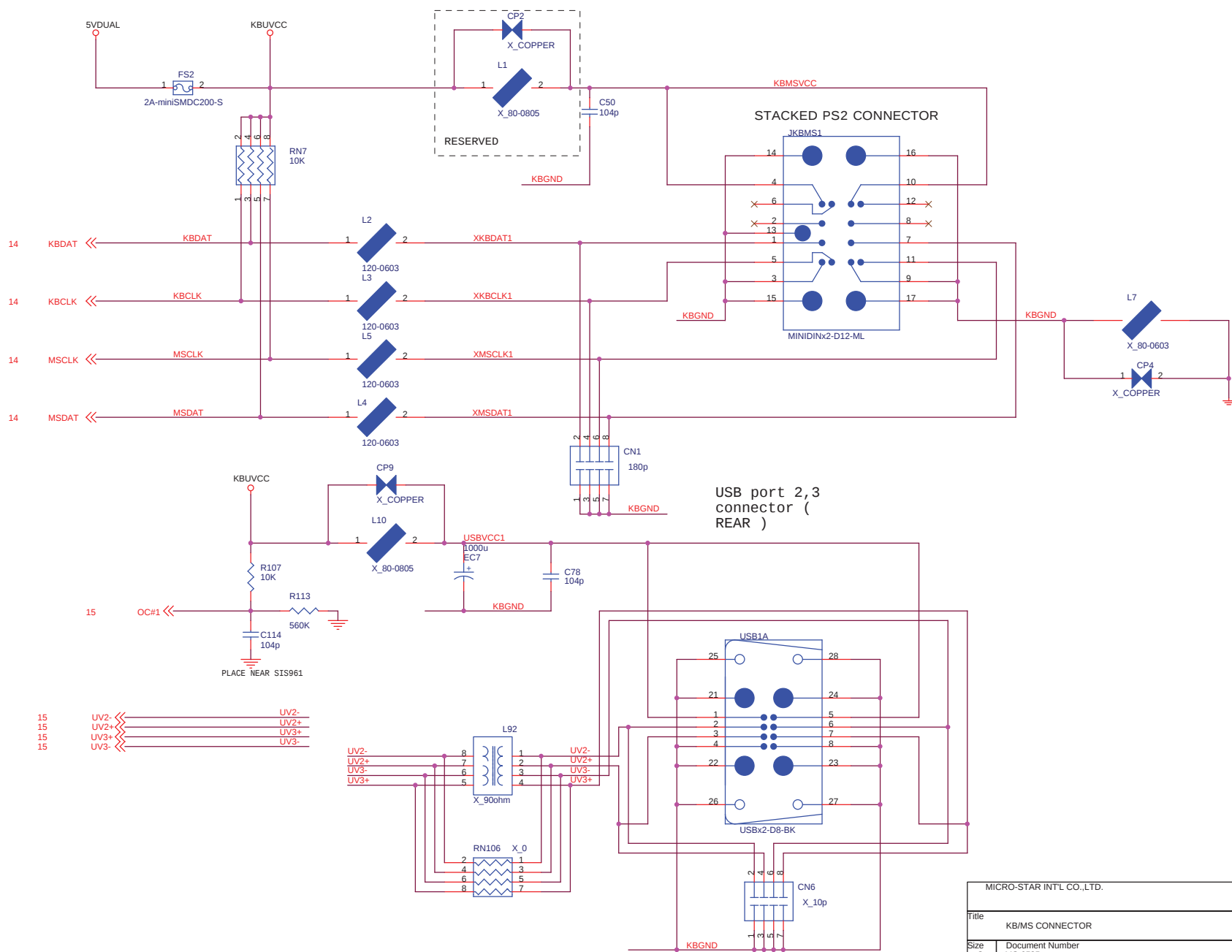


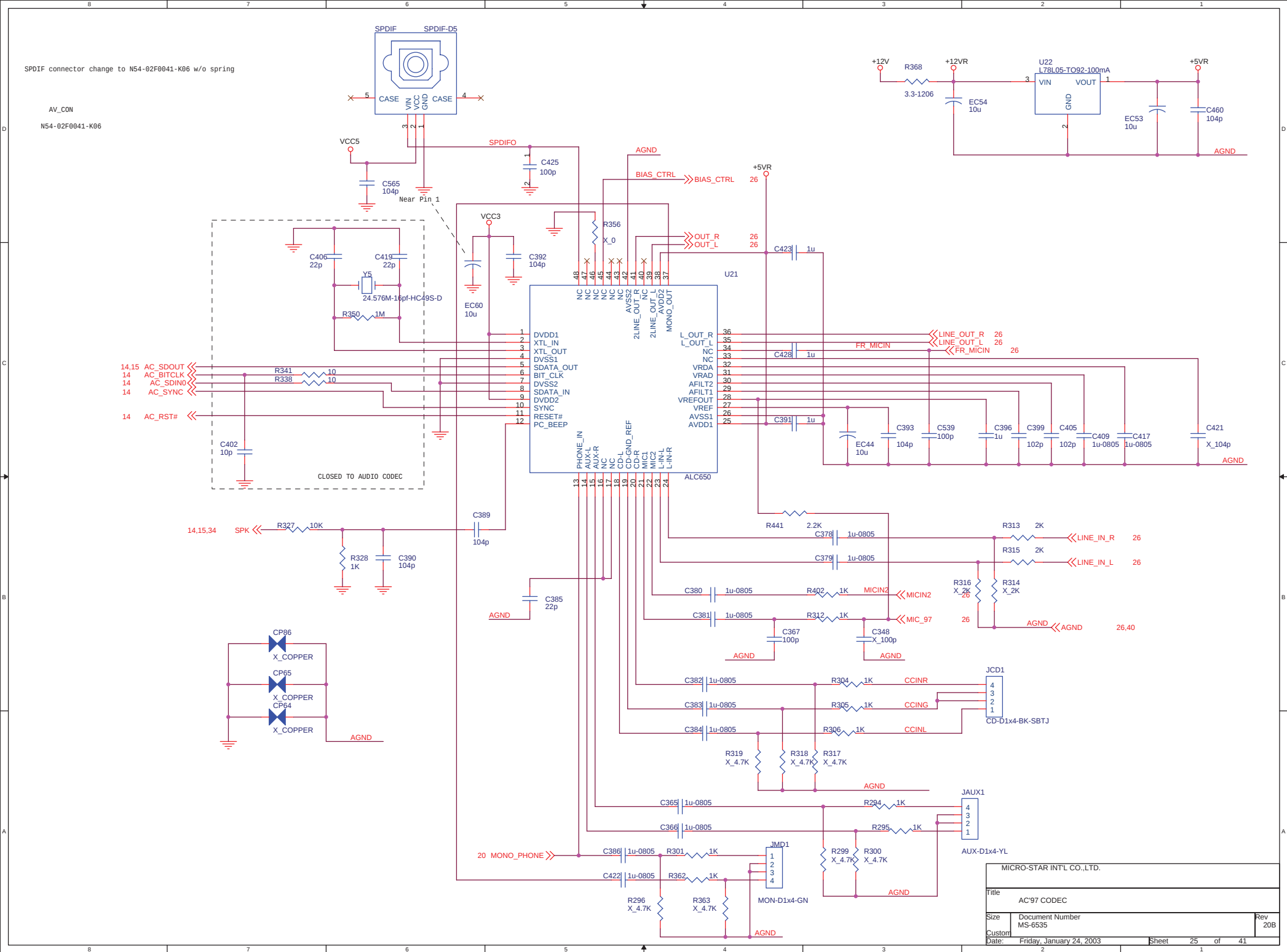
Place near connector

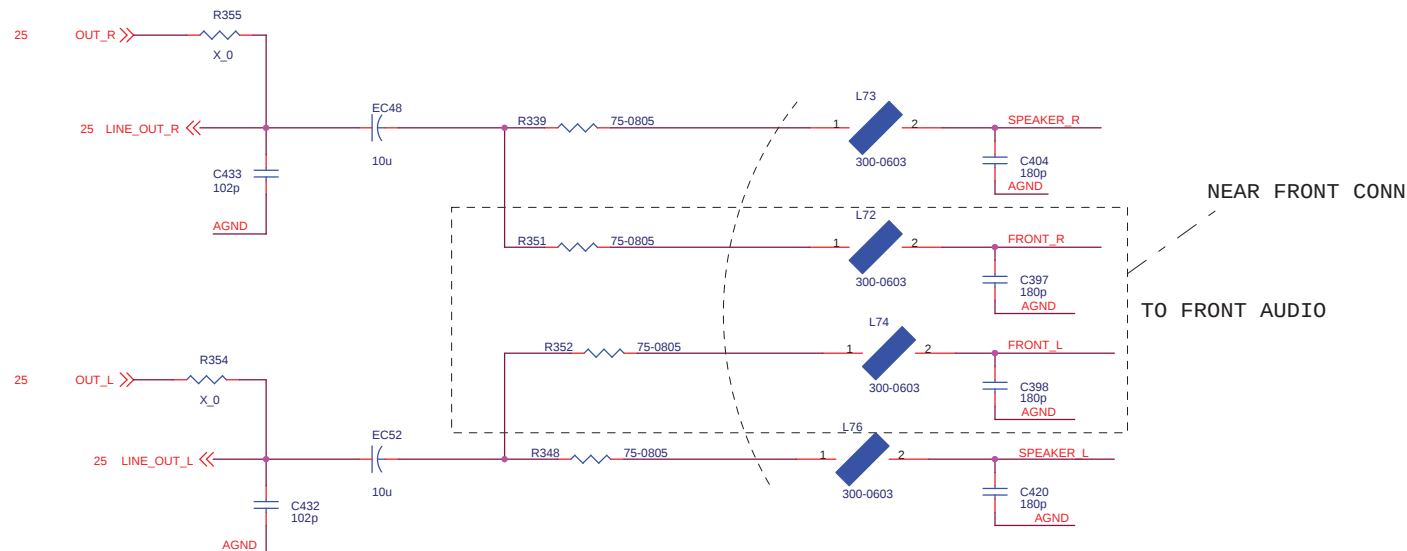


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Title USB CONNECTOR			
Size MS-6535	Document Number		Rev 20B
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KEYBOARD/MOUSE PORTS

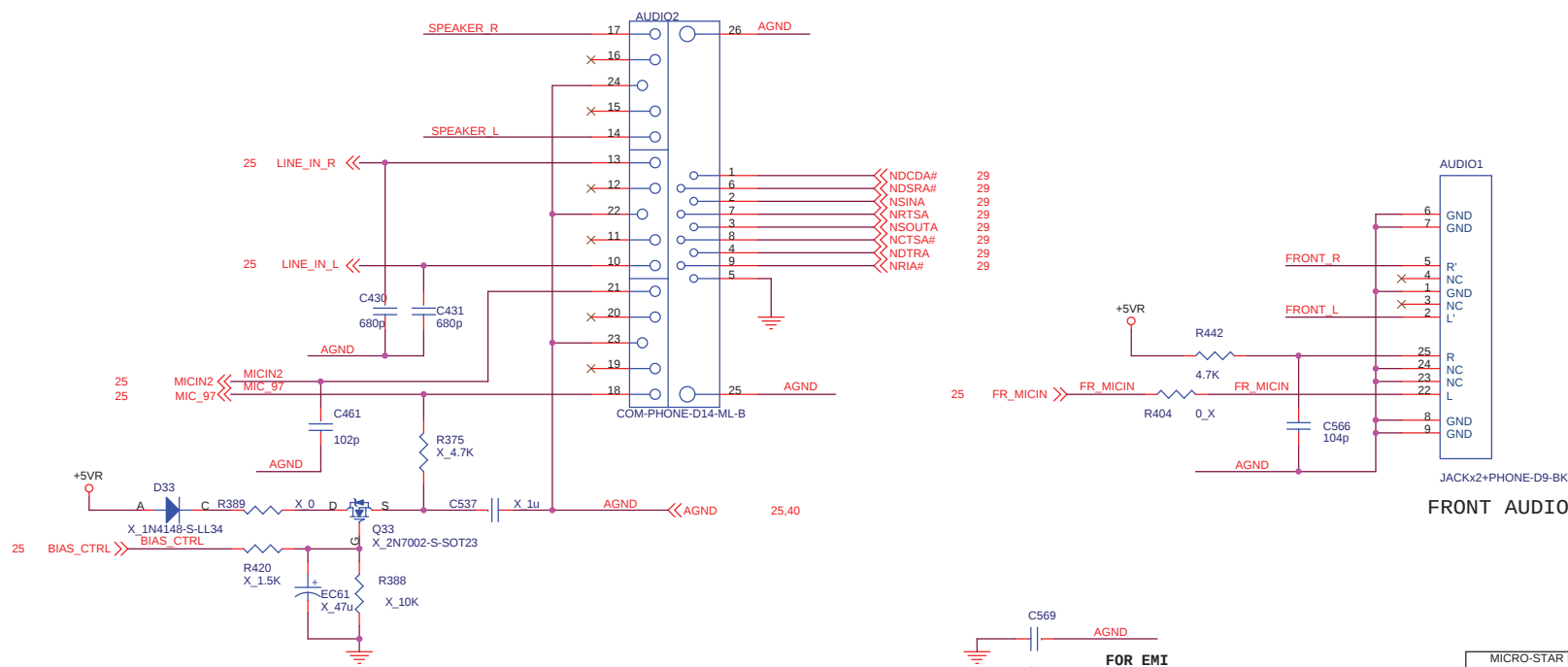






NEAR FRONT CONN
TO FRONT AUDIO

Add a AGND trace at the 3rd layer for Audio

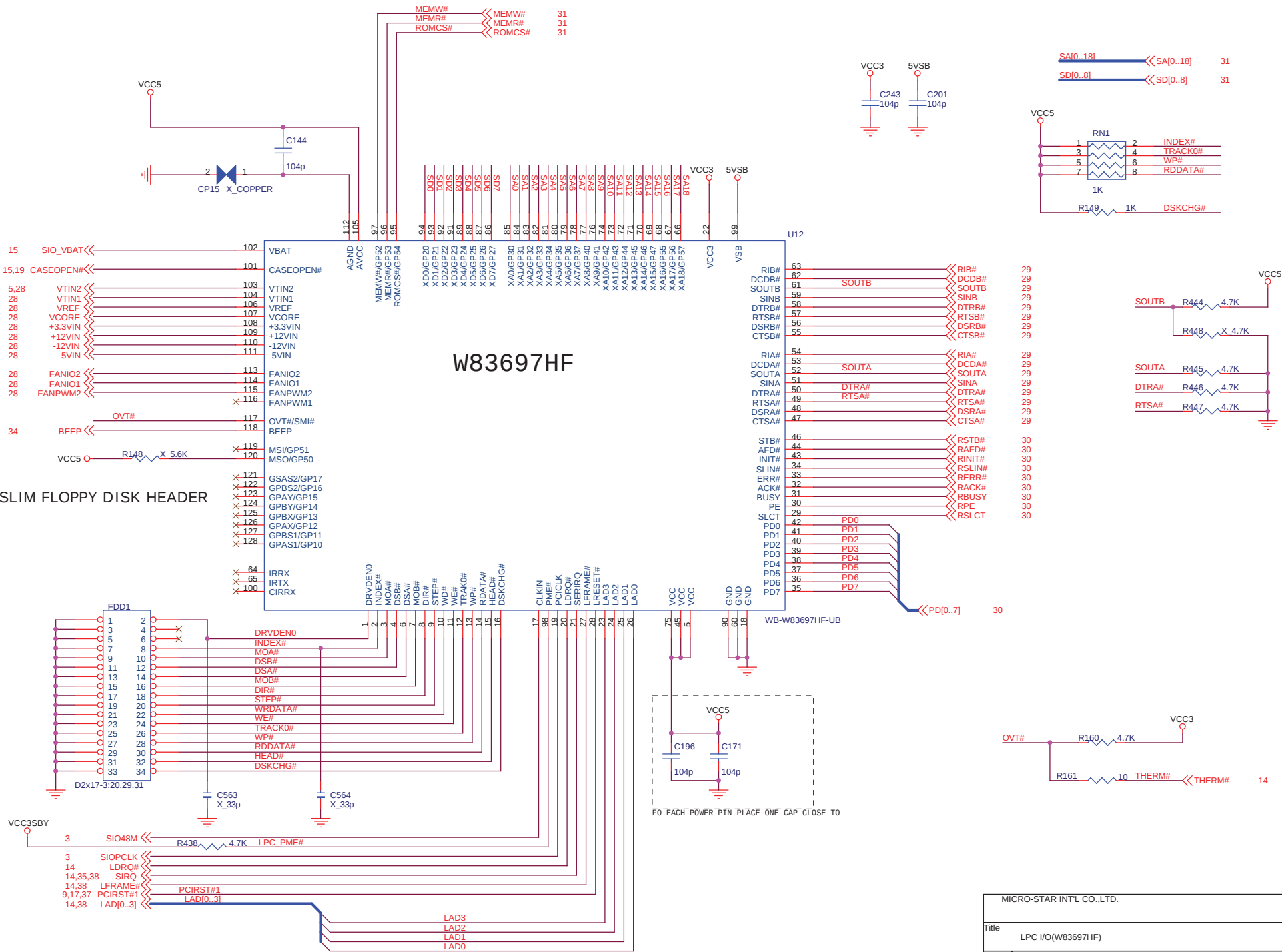


FRONT AUDIO

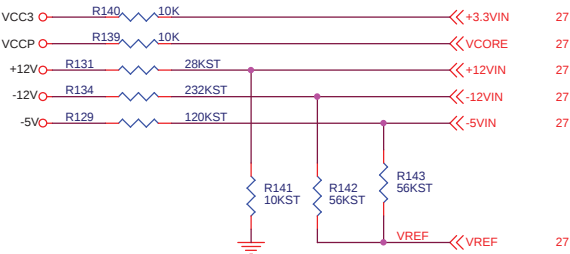
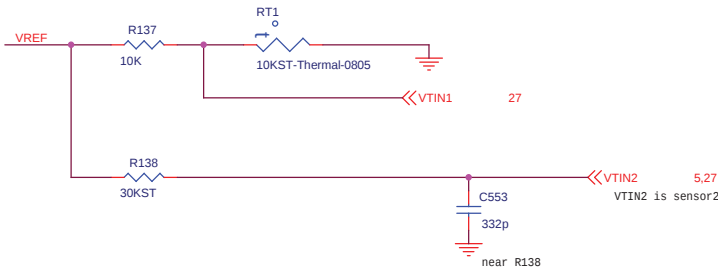
MICRO-STAR INT'L CO.,LTD.		
Title AUDIO CONNECTOR		
Size Custom	Document Number MS-6535	Rev 20B
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SLIM FLOPPY DISK HEADER

W83697HF

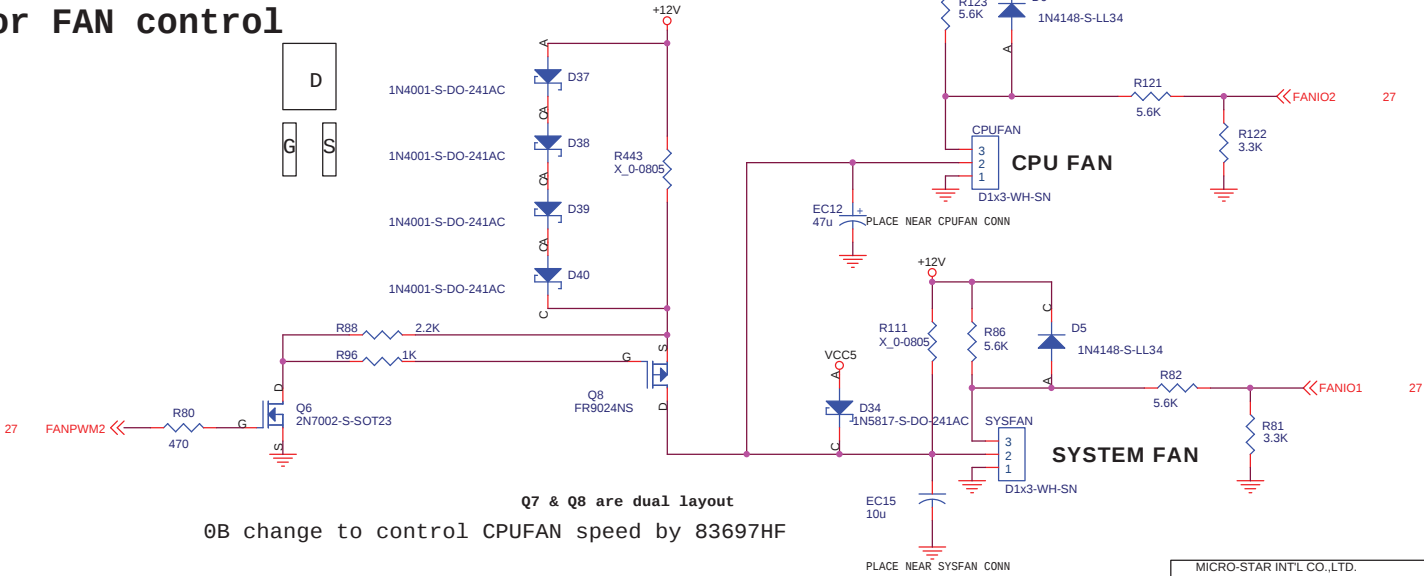


Hardware Monitor

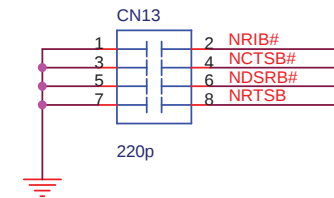
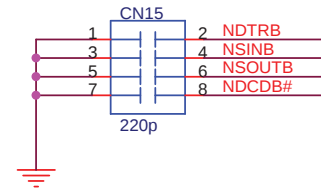
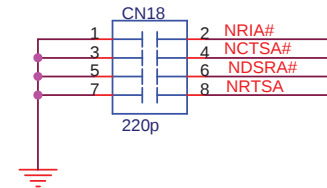
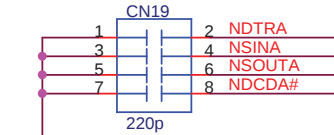
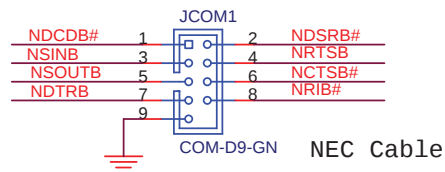
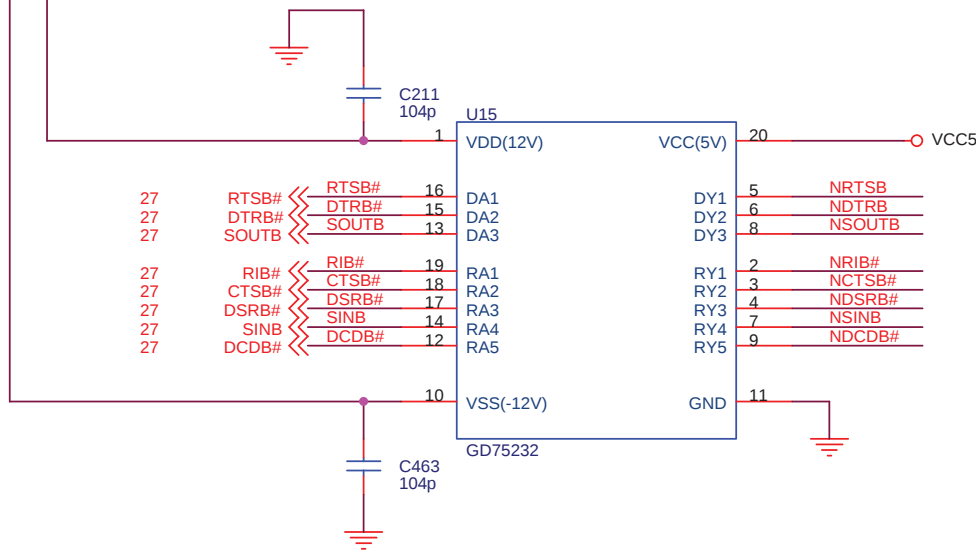
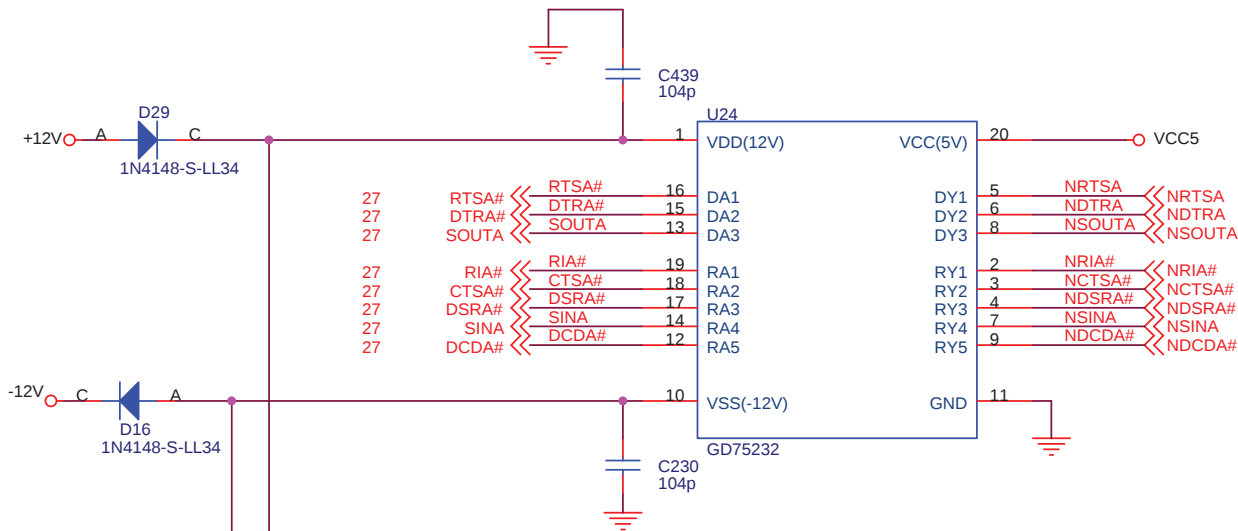


PART	SYSFAN ONLY	SYSFAN & CPUFAN	BOTH NOT (default)
R80	☐	☐	☒
Q6	☐	☐	☒
R96	☐	☐	☒
R88	☐	☐	☒
Q8	☒	☐	☒
Q7	☐	☒	☒
RN22	☐	☒	☐
RN23	☒	☐	☒
R111	☒	☒	☐

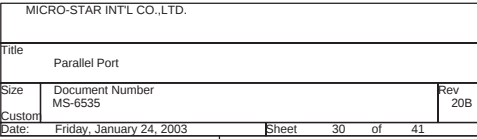
Option for FAN control



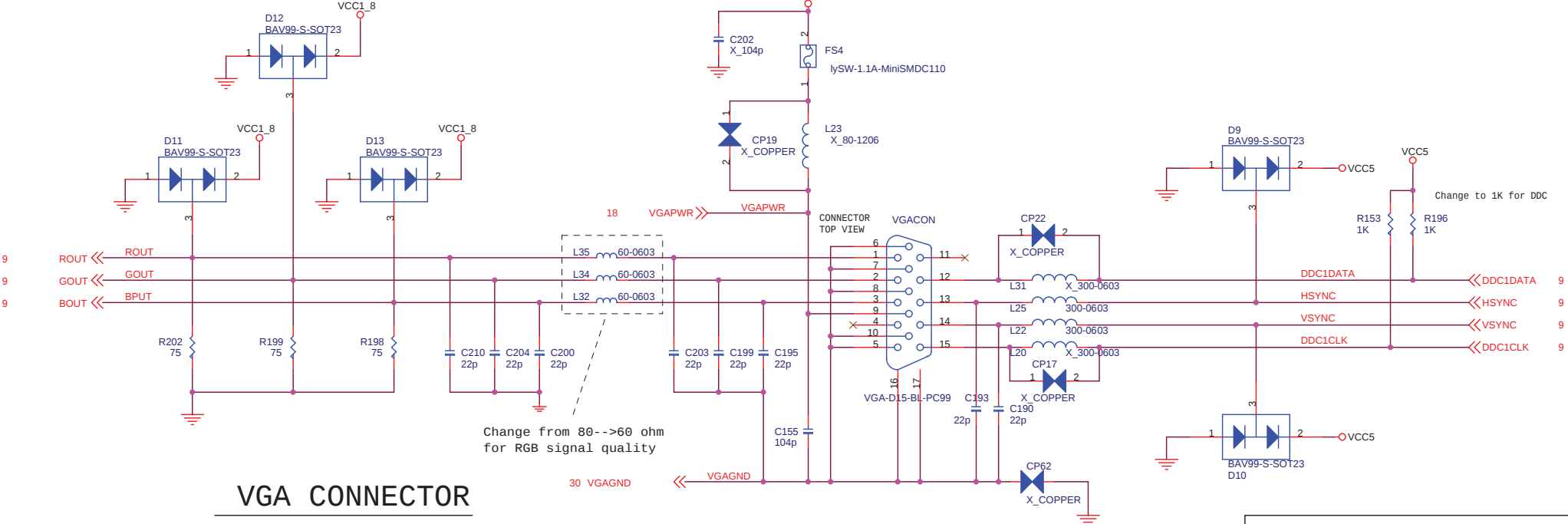
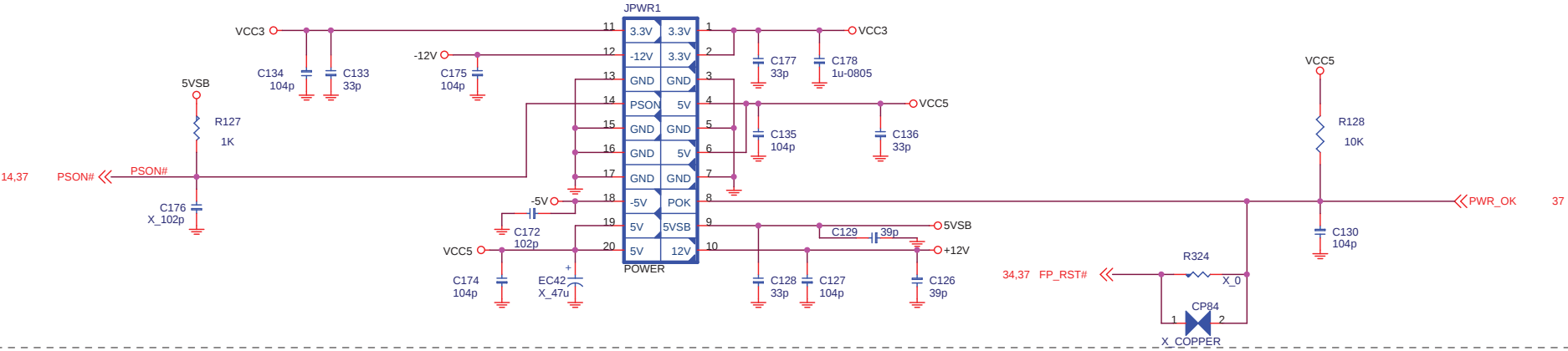
Q7 & Q8 are dual layout
0B change to control CPUFAN speed by 83697HF



MICRO-STAR INT'L CO.,LTD.			
Title SERIAL PORT			
Size	Document Number MS-6535		Rev 20B
Custom			
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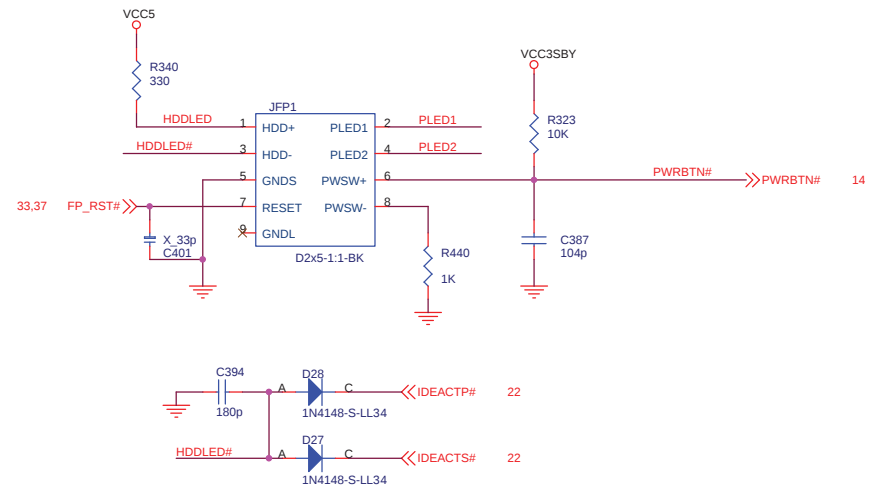
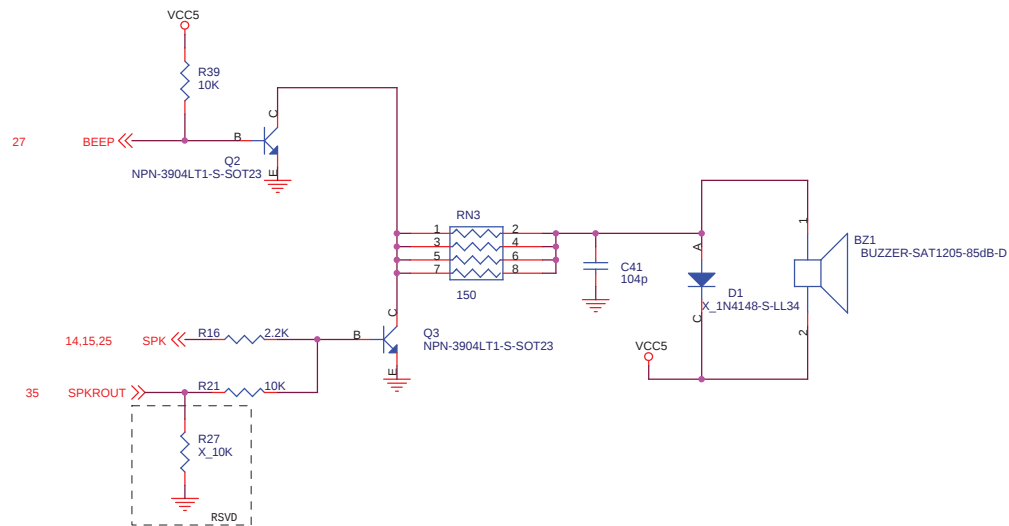


ATX CONNECTOR

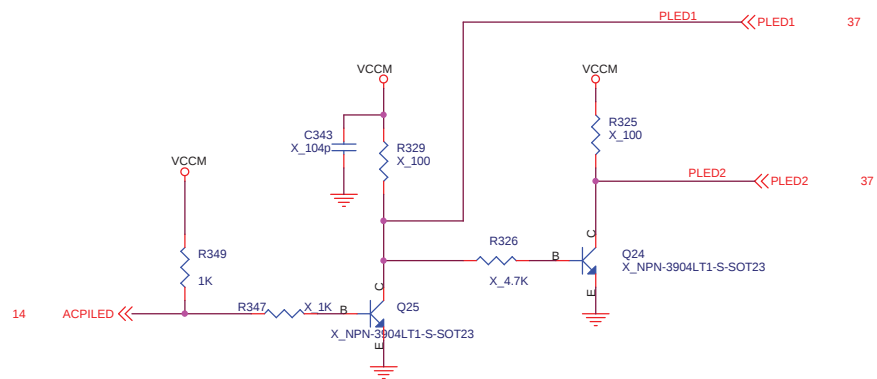


VGA CONNECTOR

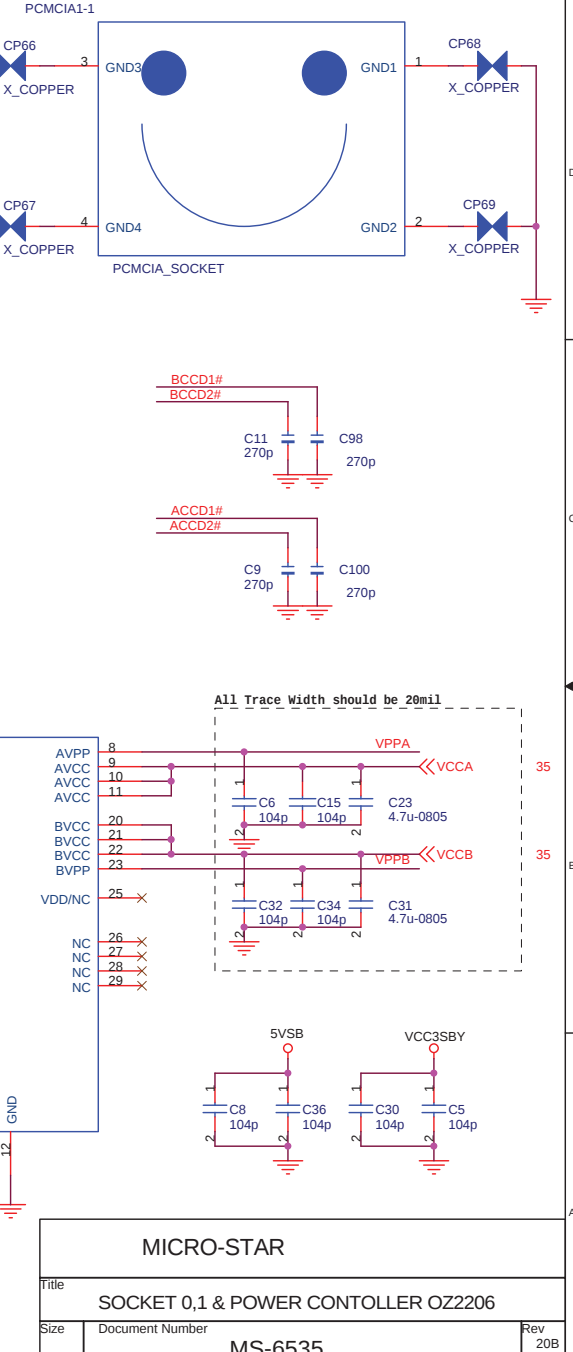
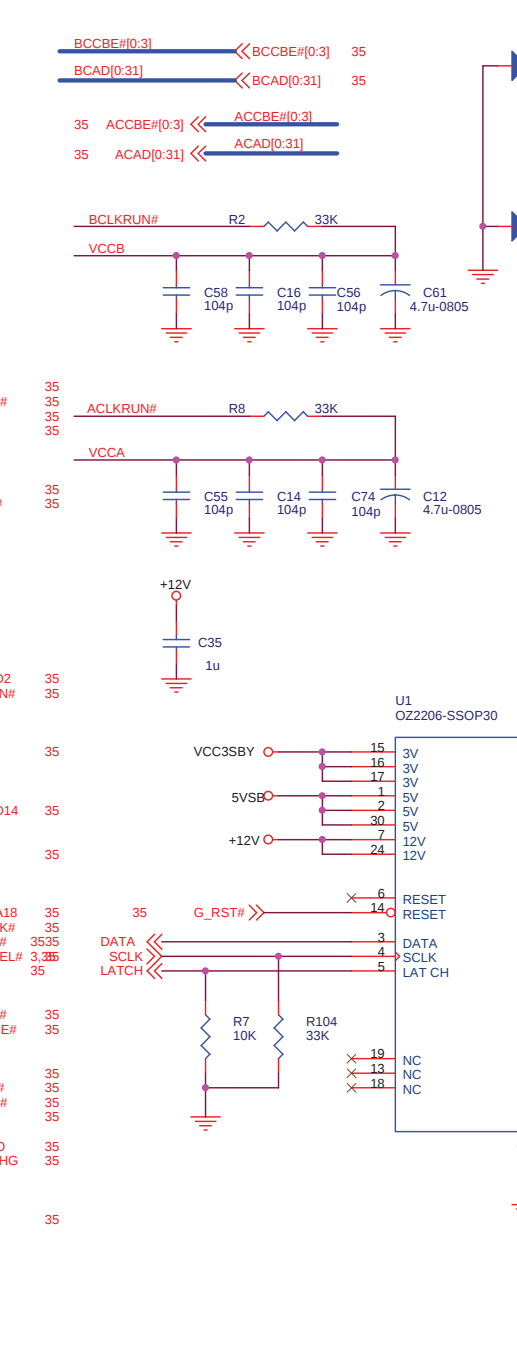
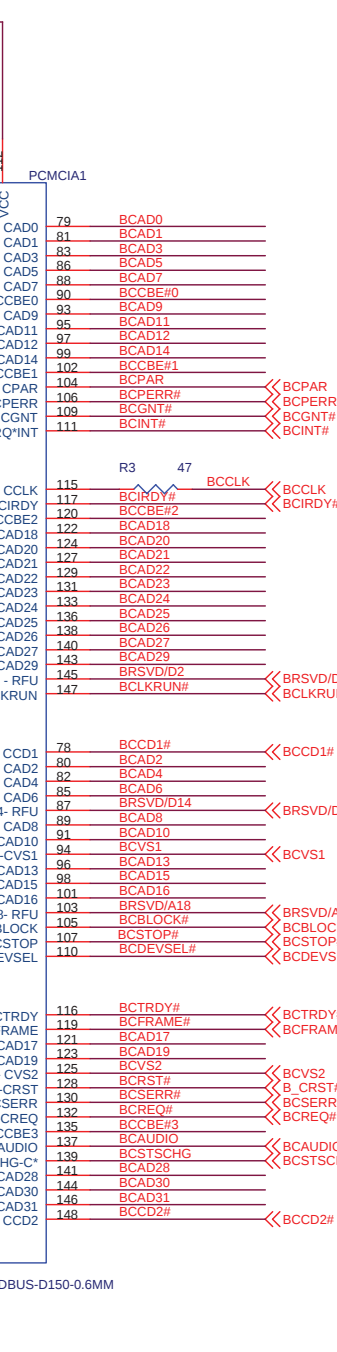
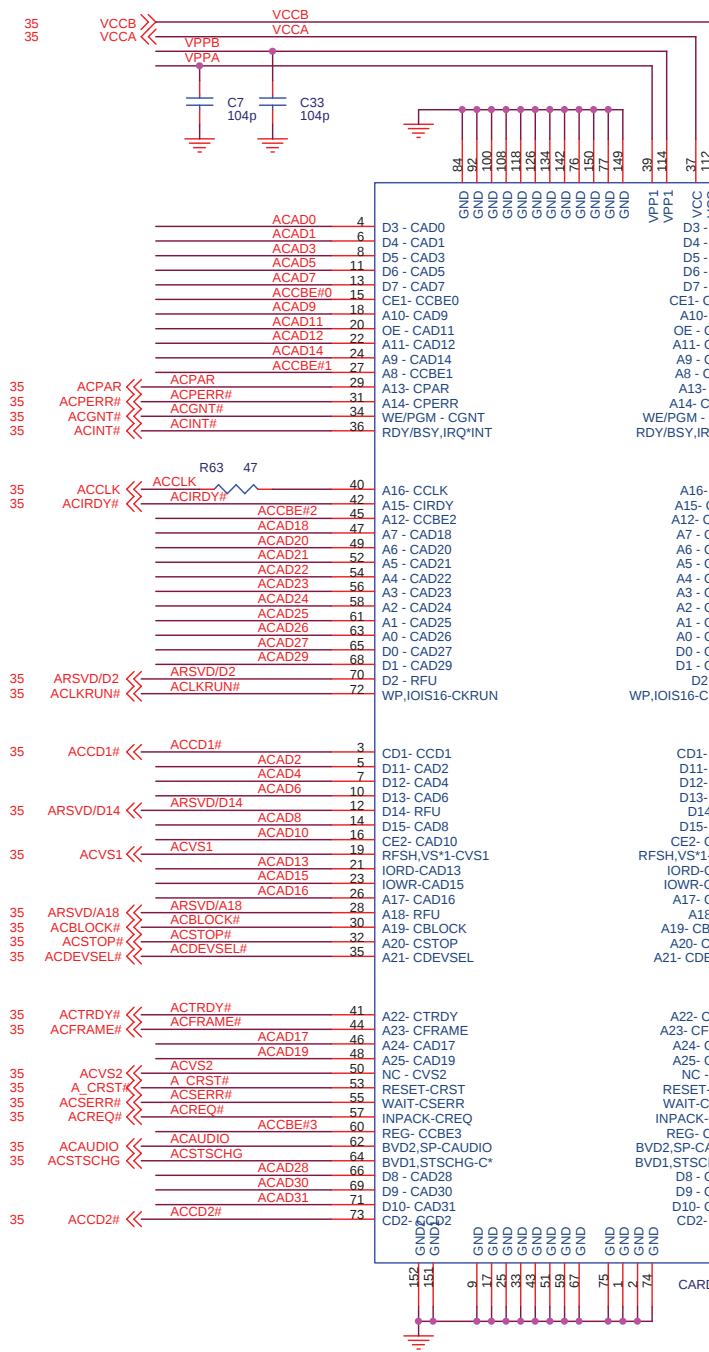
MICRO-STAR INT'L CO.,LTD.		
Title ATX Power Conn. & VGA Conn.		
Size B	Document Number MS-6535	Rev 20B
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Dual Color LED Block

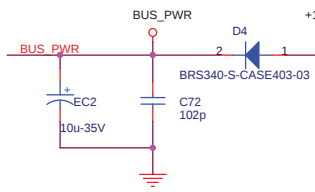


MICRO-STAR INT'L CO.,LTD.			
Title			
FRONT PANEL			
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MICRO-STAR			
Title			
SOCKET 0,1 & POWER CONTROLLER OZ2206			
Size		Document Number	Rev
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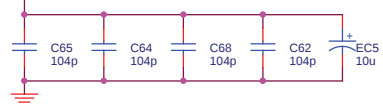




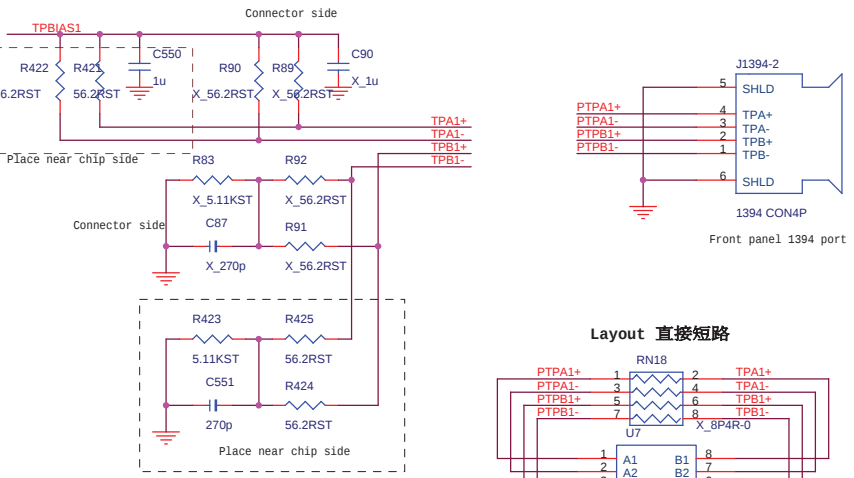
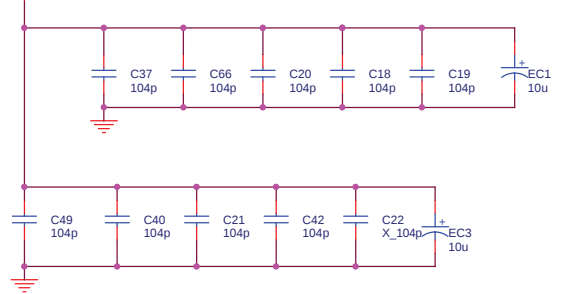
IEEE-1394

INTD# AD23

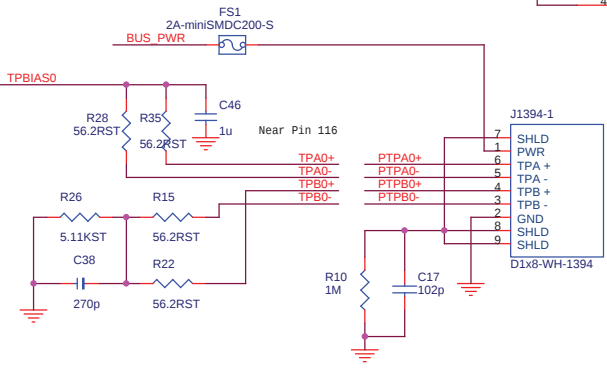
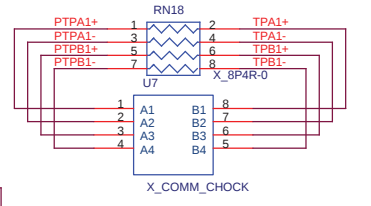
Did not support S3 wake-up



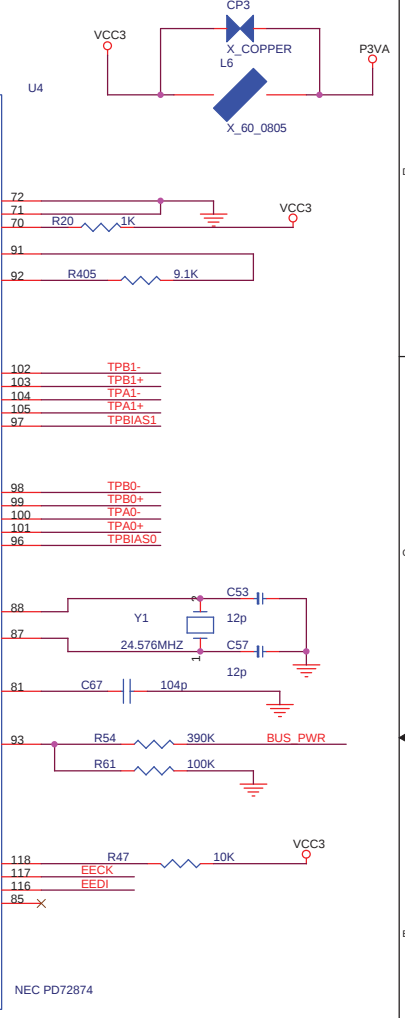
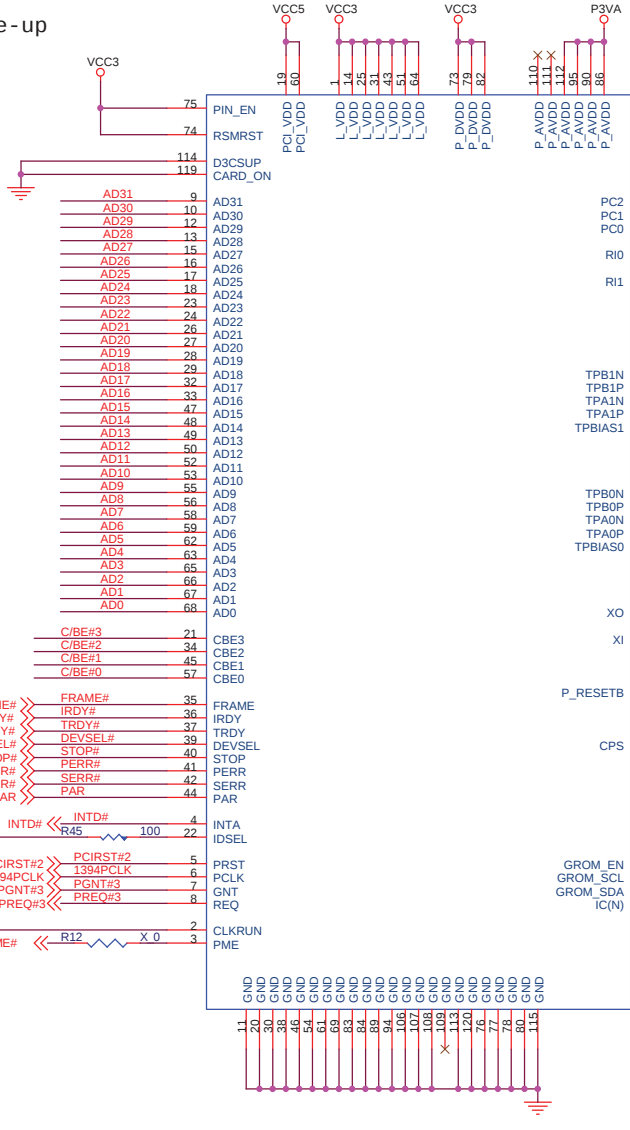
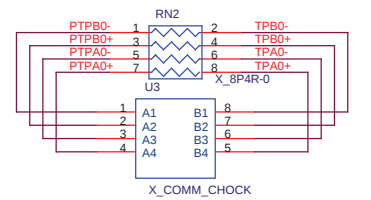
NEAR EACH POWER PIN



Layout 直接短路



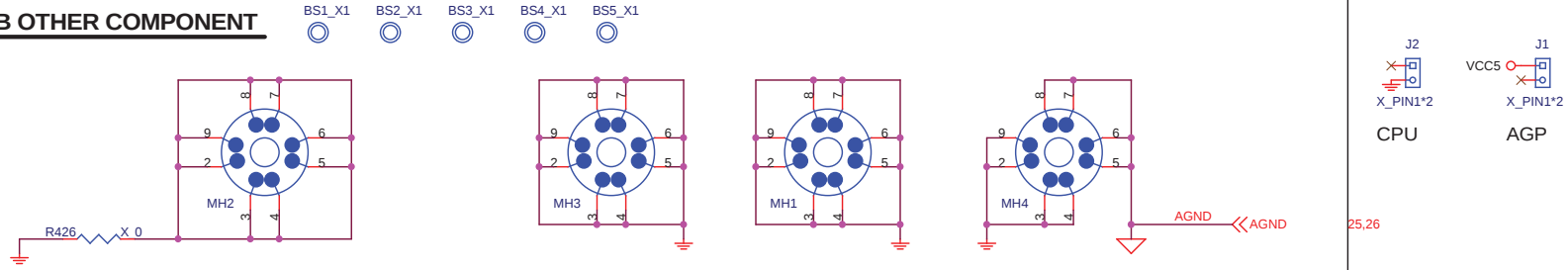
Layout 直接短路



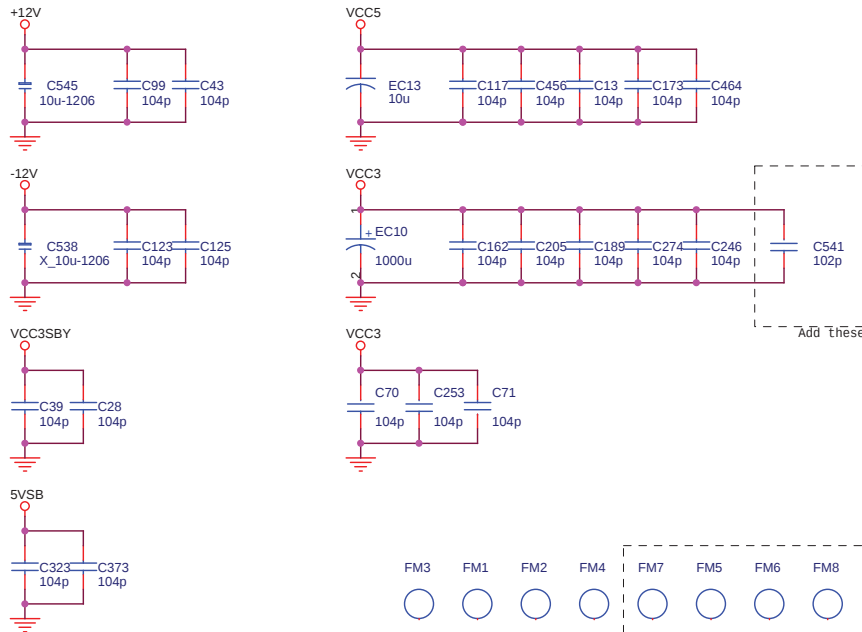
AD[0..31] << AD[0..31] 13,19,20,35
C/BE#[0..3] << C/BE#[0..3] 13,19,20,35

MICRO-STAR INT'L CO.,LTD.			
Title 1394-NEC72874			
Size Document Number MS-6535			
Custom			
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2		1	

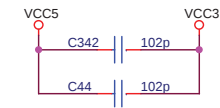
PCB OTHER COMPONENT



System Decoupling Capacitors

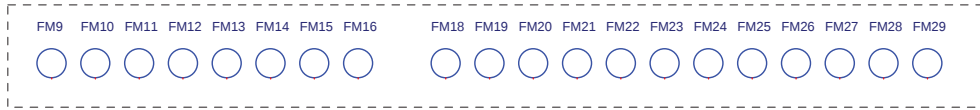


High Freq. return current decoupling



For chip positioning

At solder side



MICRO-STAR INT'L CO.,LTD.		
Title DECOUPLING CAPACITOR		
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PAGE	Description
9.SCH	Add R674 at DDC1DATA 100 ohm for SIS recommend
17.SCH	Add R675 R676 at CRT2DDC 100 ohm for SIS recommend
3.SCH	Add R702 at FS0 for ICS/ICW clock gen dual layout
37.SCH	1.Del EC199, EC43, EC5, EC118 & add C701, C702 10u-1206 for VCCM
	2.Connect VDDQ from VCC3 by 0-0805
	3.change AUXOK circuit to 473p and 510K for power sequence delay
38.SCH	Add C704/104p and change R624 to 4.7K for Winbond recommend
11/12	
25.SCH	Delete JAUX conn and the relative component
27.SCH	Delete the IR component and the DLED signals
40.SCH	Delete the DLED components and the signals, del this page
11/19	
32.SCH	Change PWM R54 form 100-->10-0805 for ST recommend
15.SCH	Change C254 to be 474p for RC time constant is 100ms
11/21	Update the New Part Number for each part! to V11
11/29	
35.SCH	Change PCMCIA controller to OZ6933
36.SCH	Change the A,B slot for layout
4.SCH	Swap the DDRCLK for layout
12/10	GERBER OUT

1/31	
3.SCH	Change SIO 48MHz with UCLK48M and change CLK GEN to ICS
	Did not stuff R119 and stuff R120/4.7K for ICS
4.SCH	Change U23 to ICS 93722
8.SCH	Swap DDR pin for DDR signal (MA0~3, SRAS#, MD44)
12.SCH	Add C540 10uF-1206 and change DDR_VTT decoupling cap to 105pF
14.SCH	R151,R152 : 4.7K-->2.2K, change SMBALT# R185 to GND for SMBUS
15.SCH	Del C151 and change C112 to X7R cap
16.SCH	Change C508,C510 to component side and stuff and del C169
20.SCH	Change RTL8100 to RTL8101 and add Modem solution
21.SCH	Do not mount R155, C156, C159, C160, R94, R95
23.SCH	Change RN31, RN35 & RN38 15-->27 ohm for eye pattern
25.SCH	Change CODEC to ALC650 and change the following:
	Change SPDIF signal , remove R361, C436, R364
	Add FR_MICIN, MICIN2, BIAS_CTRL circuit for 6 channel
	Did not stuff R317~R319, R299, R300, R296, R363 and del C418
	Add C539 for FR_MICIN and change R304~ R306 to 1K ohm
26.SCH	Change AGND2 to AGND for Audio Precision SNR THD+N
	Change the MIC ckt for 6 channel line-out
27.SCH	Change FDD to be slim type and change FAN control to FANPWM2
28.SCH	Mount R80, R88, R96, Q8, RN23 and remove RN22, R111
	Change EC12 to 47uF for FAN 12V
32.SCH	Add VRM_EN circuit to U25.17 for leakage current
	Did not mount EC49, EC50, Q12, Q30 for VRM9.0 OK
	change R386 to 1.5K and R376 to 200KST for VRM9.0
33.SCH	Change L32, L34,L35 to 60S-0603 for RGB signal quality
	change R153, R196 to 1K for DDC
34.SCH	Did not stuff R347,Q25,R329,R325,Q24,R326 for 302 to control LED

37.SCH	Change EC45 to 10mm Cap for DDR_VTT and stuff C371
	Change C339 to X7R cap for soft-star & Remove R273
39.SCH	Change 1394 from VIA 6306 to NEC PD72874 for VIA PHY bug
	Did not support S3 wake-up
40.SCH	Add C541 and C542 at VCC3 for EMI

[illegible]

5.SCH	Delete R335 and change R336 to be dummy pad
14.SCH	Add C554 at INIT# signal for Auto-reset issue!Remove R334-C
27.SCH	Delete L14 & CP14 and connect C144 direct to VCC5
28.SCH	Add C553 332pF at VTIN2 near 697HF for CPU Temp issue!
	Change RT1 from 0603 to 0805 size to meet the size of L14
	Do not change any paste & ICT test pad for the same as 1.0A

32.SCH	Remove +12V trace from JPW1(4 pin) to JPWR1(20 pin)--->Rename page#32 from +12V to +12V4P
33.SCH	Move EC55 from page#33 to page#32 and connect to +12V4P

Title				
HISTORY				
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