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Version 1.0B

# MS-6532 (LEGEND)

INTEL (R) Brookdale Chipset  
Willamette/Northwood 478pin mPGA-B Processor Schematics

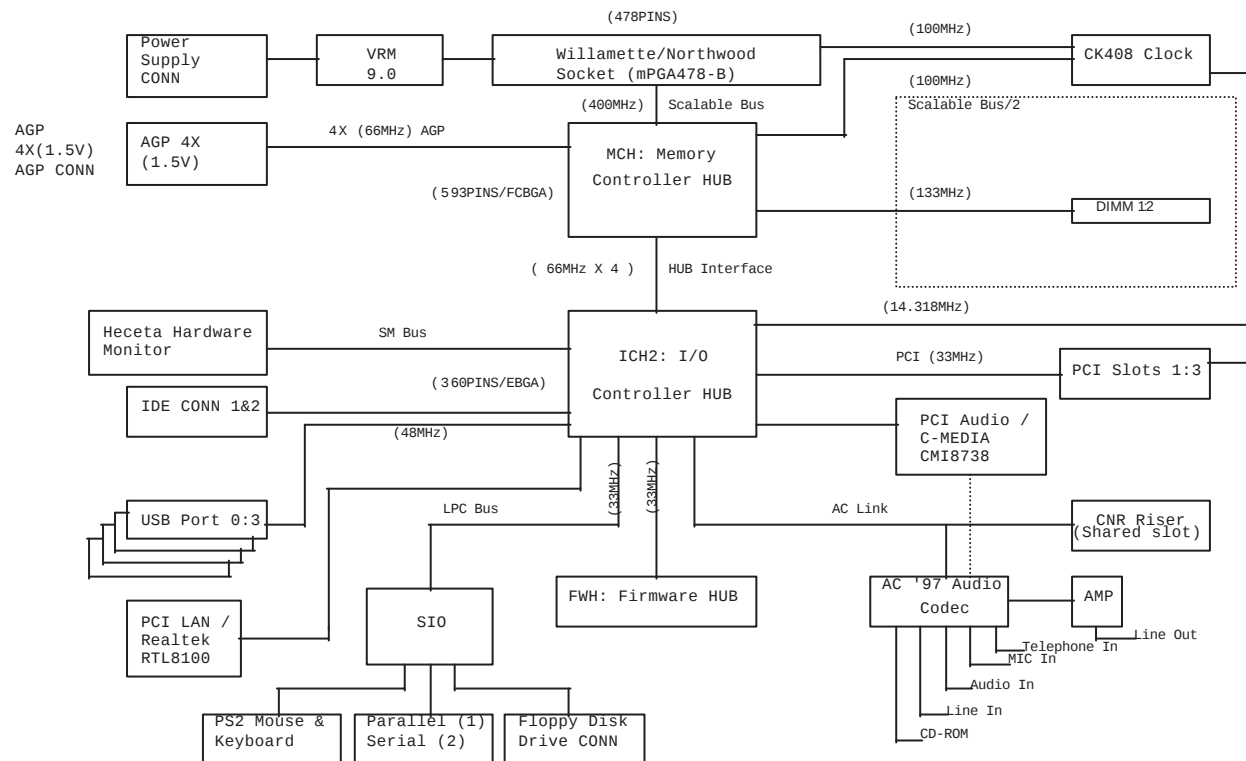
**CPU:**  
**Willamette/Northwood mPGA-478B Processor**

**System Brookdale Chipset:**  
**INTEL MCH (North Bridge) +  
INTEL ICH2 (South Bridge)**

**On Board Chipset:**  
**BIOS -- FWH**  
**LPC Super I/O -- W83627HF**  
**Clock Generation -- ICS94208**  
**PCI SOUND -- C-MEDIA CMI8738**

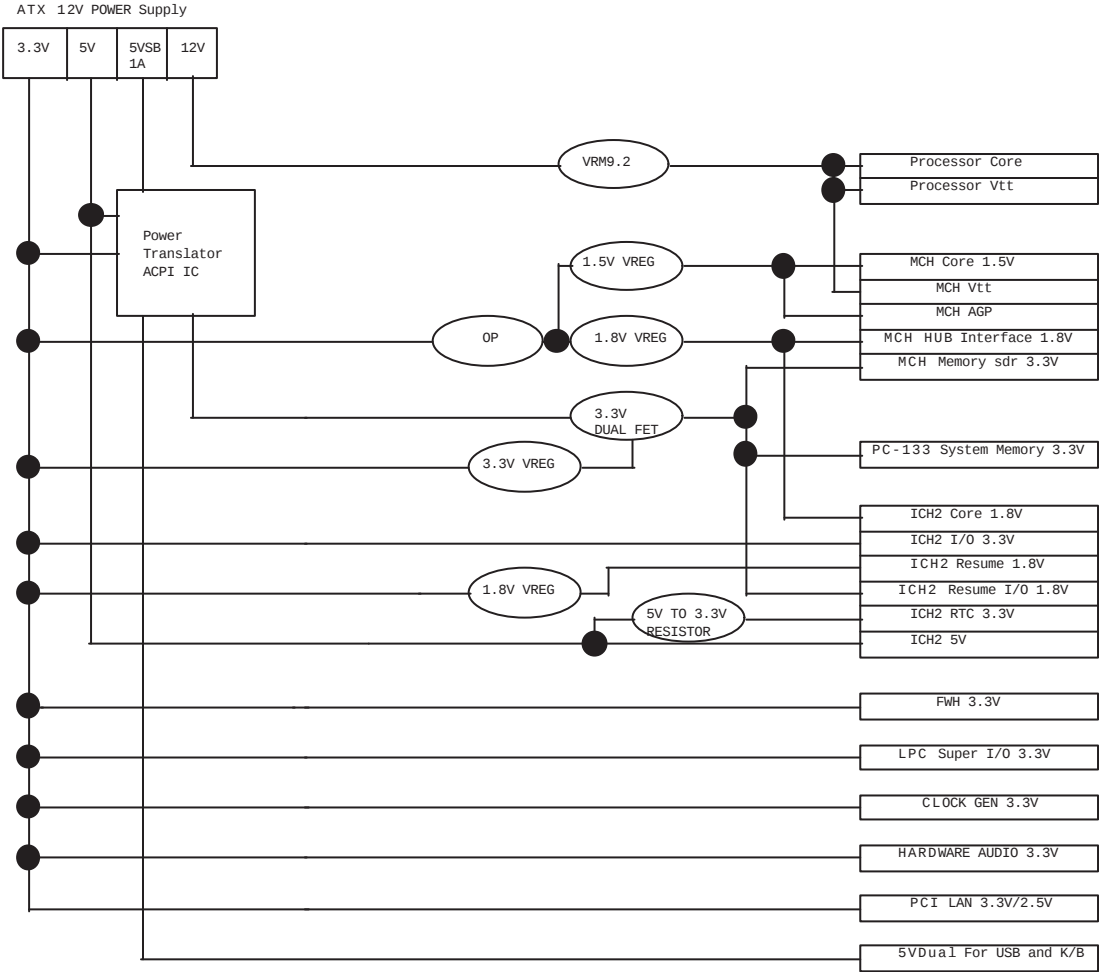
**Expansion Slots:**  
**AGP2.0 SLOT \* 1**  
**PCI2.2 SLOT \* 3**  
**CNR SLOT \* 1**

|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| Micro-Star                                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                 | Cover Sheet             |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 | Sheet                   | 1 of 32            |



|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| <b>Micro-Star</b>                               | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number<br><b>Block Diagram</b>         |                         |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |                         | Sheet 2 of 32      |

Power Delivery Map



|            |                     |                          |       |         |
|------------|---------------------|--------------------------|-------|---------|
| Micro-Star | Title               | MS-6532                  | Rev   | 1.0B    |
|            | Document Number     | Power Delivery Map       |       |         |
|            | Last Revision Date: | Wednesday, July 25, 2001 | Sheet | 3 of 32 |

General Purpose I/O Spec.

ICH2

| GPIO Pin   | Type | Function              |
|------------|------|-----------------------|
| GPIO 0     | I    | Non Connect           |
| GPIO 1     | I    | Non Connect           |
| GPIO 2~4   | I    | Not Implemented       |
| GPIO 5     | I    | Non Connect           |
| GPIO 6     | I    | AC97 Enabled/Disabled |
| GPIO 7     | I    | None                  |
| GPIO 8     | I    | LAN Wake Up           |
| GPIO 9     | I    | AC'97 Serial Data In  |
| GPIO 10    | I    | Non Connect           |
| GPIO 11    | I    | Non Connect           |
| GPIO 12    | I    | External SMI          |
| GPIO 13    | I    | LPC PME               |
| GPIO 14~15 | I    | Not Implemented       |
| GPIO 16    | O    | Non Connect           |
| GPIO 17    | O    | Non Connect           |
| GPIO 18    | O    | Not Implemented       |
| GPIO 19    | O    | Not Implemented       |
| GPIO 20    | O    | Non                   |
| GPIO 21    | O    | Not Implemented       |
| GPIO 22    | O    | Non                   |
| GPIO 23    | OD   | BIOS Locked/Unlocked  |
| GPIO 24    | O    | Non                   |
| GPIO 25    | O    | Non                   |
| GPIO 26    | O    | Non                   |
| GPIO 27    | I/O  | Non                   |
| GPIO 28    | I/O  | Non                   |
| GPIO 29~31 | I/O  | Not Implemented       |

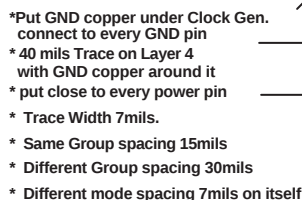
FWH

| GPIO Pin | Type | Function         |
|----------|------|------------------|
| GPI 0    | I    | ATA IDE 1 Detect |
| GPI 1    | I    | ATA IDE 2 Detect |
| GPI 2    | I    | Reserved         |
| GPI 3    | I    | Reserved         |

| DEVICE     | ICH INT Pin                            | IDSEL |
|------------|----------------------------------------|-------|
| PCI Slot 1 | INTA#<br>INTB#<br>INTC#<br>INTD#       | AD16  |
| PCI Slot 2 | INTB#<br>INTC#<br>INTD#<br>INTA#       | AD17  |
| PCI Slot 3 | INTC#<br>INTD#<br>INTA#<br>INTB#       | AD18  |
| PCI Audio  | INTD#/INTE#<br>INTA#<br>INTB#<br>INTC# | AD23  |
| PCI Lan    | INTC#/INTF#<br>INTD#<br>INTA#<br>INTB# | AD22  |

### CLOCK GENERATOR BLOCK

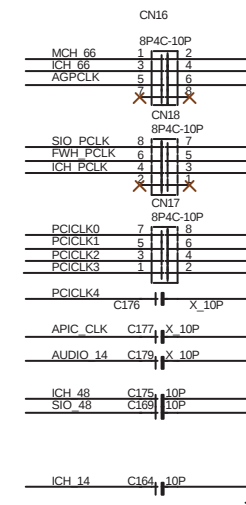
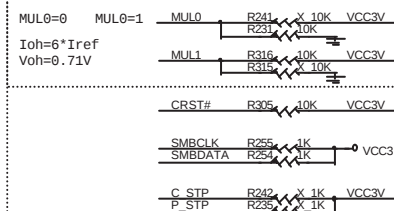
\*Trace less 0.5"



### Pull-Down Capacitors



Figure 1 is a schematic diagram of the input circuit of the ADXL045. It shows several input pins (FS4, FS3, FS1, FS0, FS2, MODE) connected to resistors (R324, R334, R282, R283, R321, R322, R326, R325, R336) which are then connected to either VCC3V or ground. Some resistors are marked with 'X' and '10K'.

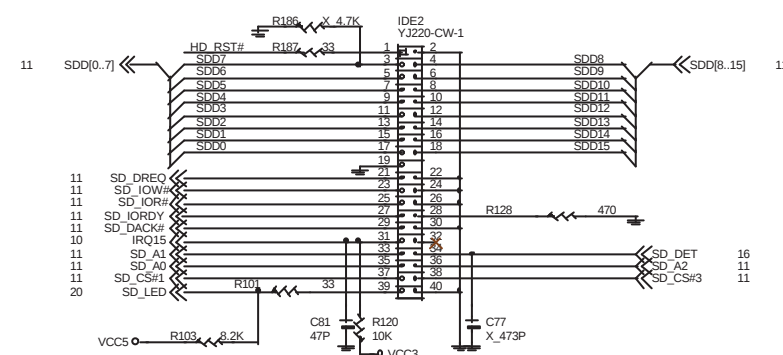


used only for EMI issue

Trace less 0,2"

## ATA100 IDE CONNECTORS

## SECONDARY IDE BLOCK



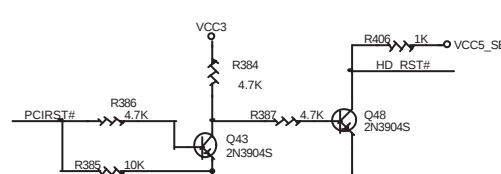
### RESET BLOCK

10 PCIRST#  $\ll$  PCIRST#1  $\triangleright$  2  $\xrightarrow{R388, 330}$  VCC3 8.12.13.16.26  $\xrightarrow{R197, 330}$  VCC3

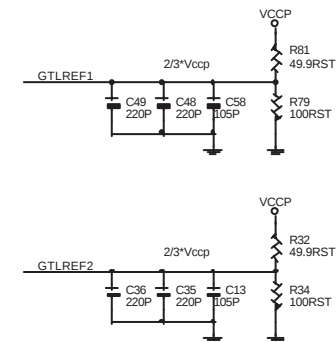
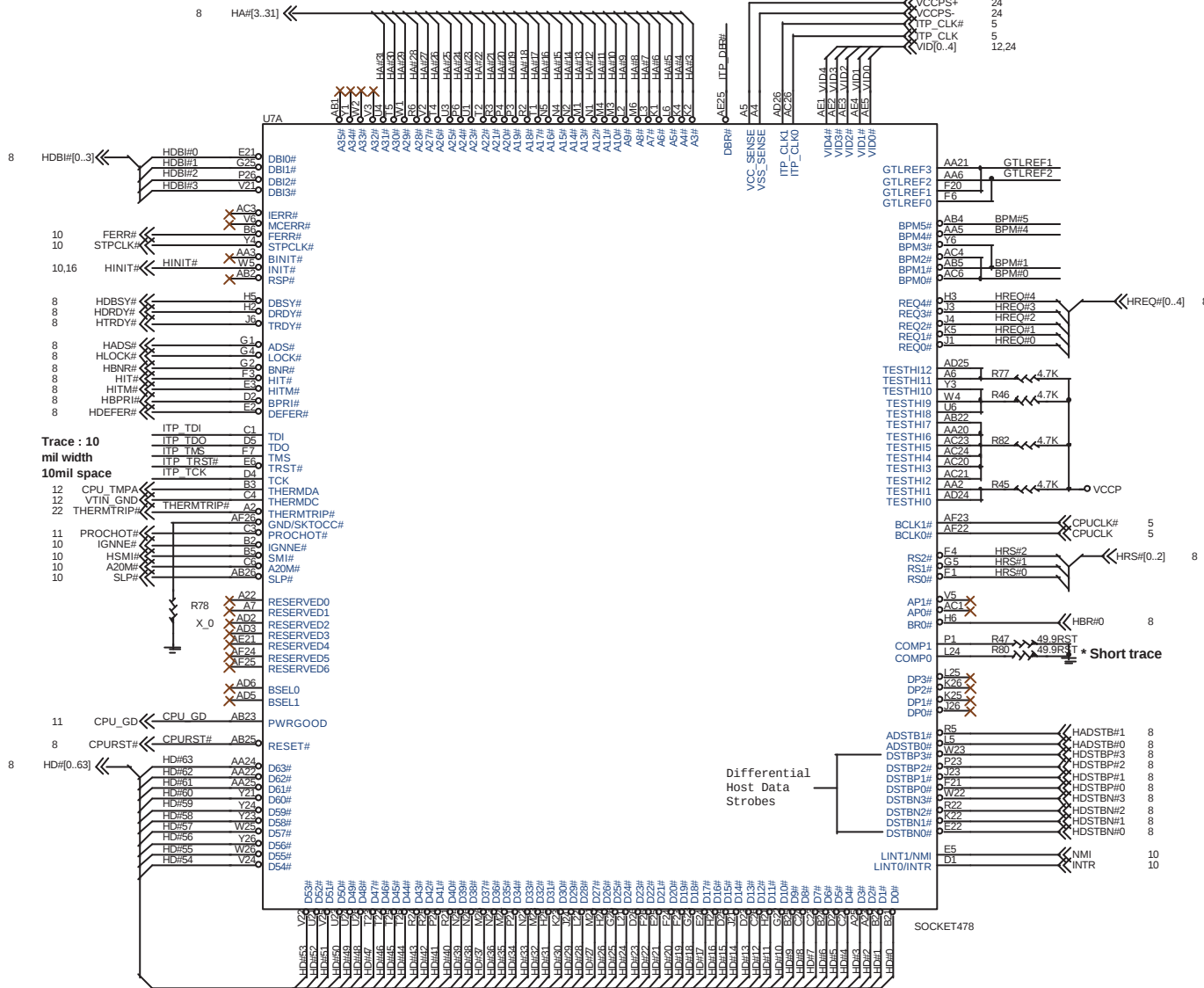
U21A 7407S (VCC5\_STR) C199 X\_10P

PCIRST#  $\triangleright$  9  $\xrightarrow{R724, 330}$  VCC5 HD\_RST#

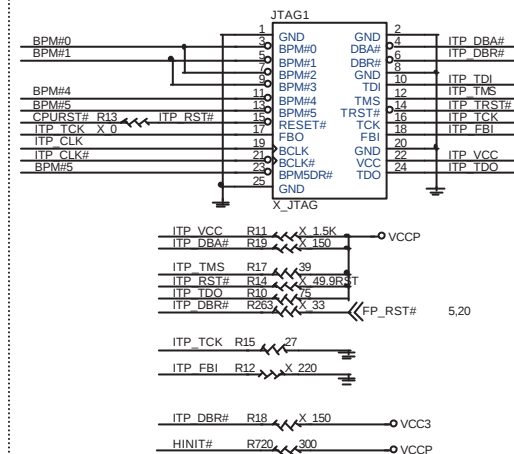
U21B 7407S (VCC5\_STR) PCIRST#  $\triangleright$  4  $\xrightarrow{R197, 330}$  VCC3 18.19



|                                                 |       |                              |     |             |
|-------------------------------------------------|-------|------------------------------|-----|-------------|
| <b>Micro-Star</b>                               | Title | <b>MS-6532</b>               | Rev | <b>1.0B</b> |
| Document Number                                 |       | Clock CY28323/4 & ATA100 IDE |     |             |
| Last Revision Date:<br>Wednesday, July 25, 2000 |       | Sheet                        | 5   | of 32       |



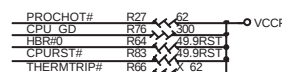
CPU ITP BLOCK



```

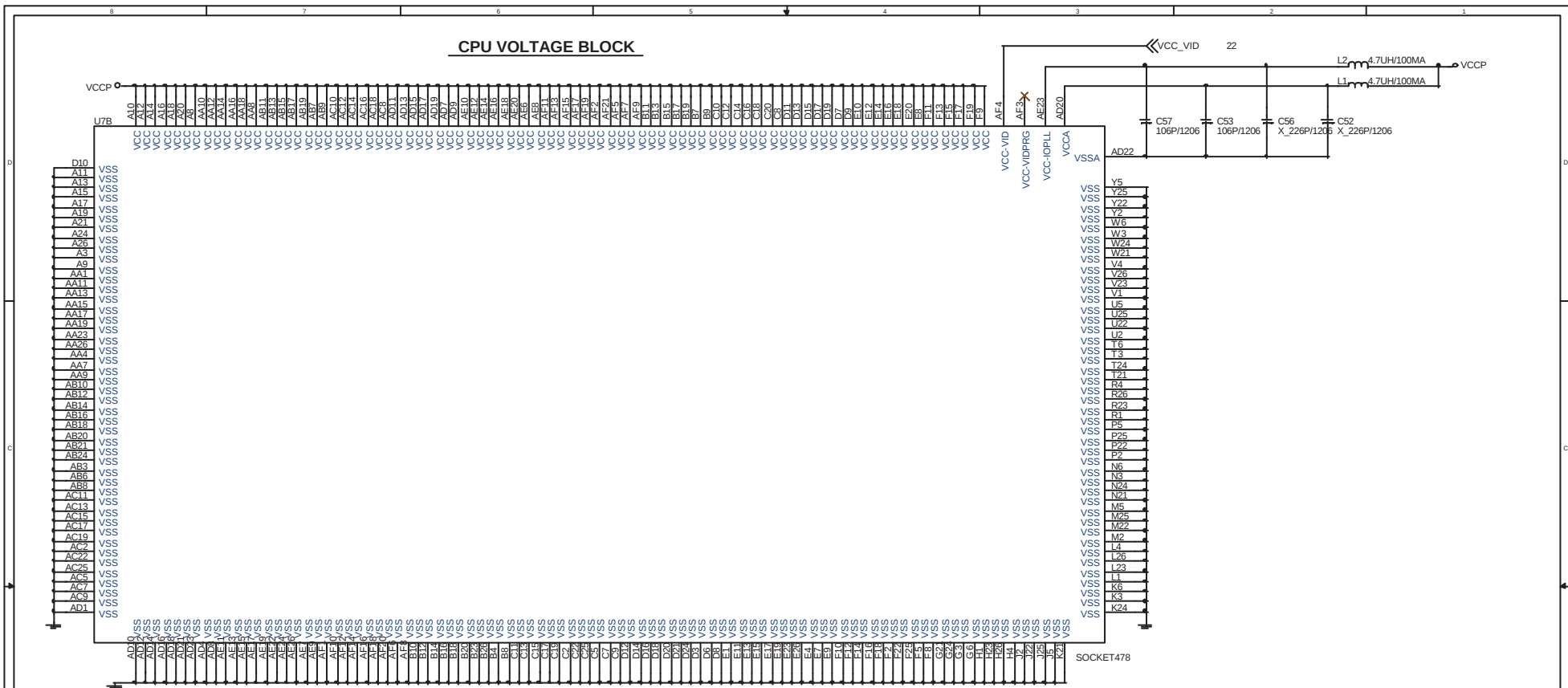
: NO USE 11
: 1.JTAG1 NC
: 2.R13 NC
: 3.R11 NC
: 4.R14 NC
: 5.R263 NC
: 6.R18 NC

```

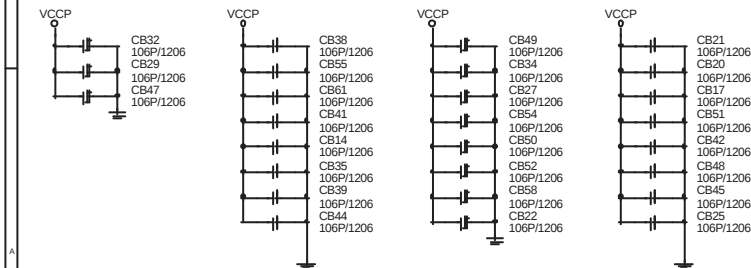


|                                                 |       |                       |     |                    |
|-------------------------------------------------|-------|-----------------------|-----|--------------------|
| <i><b>Micro-Star</b></i>                        | Title | <i><b>MS-6532</b></i> | Rev | <i><b>1.0B</b></i> |
| Document Number                                 |       |                       |     |                    |
| INTEL mPGA478-B CPU1                            |       |                       |     |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |       | Sheet 6 of 32         |     |                    |

## CPU VOLTAGE BLOCK

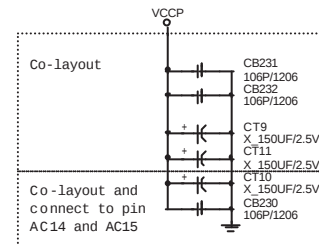


## CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

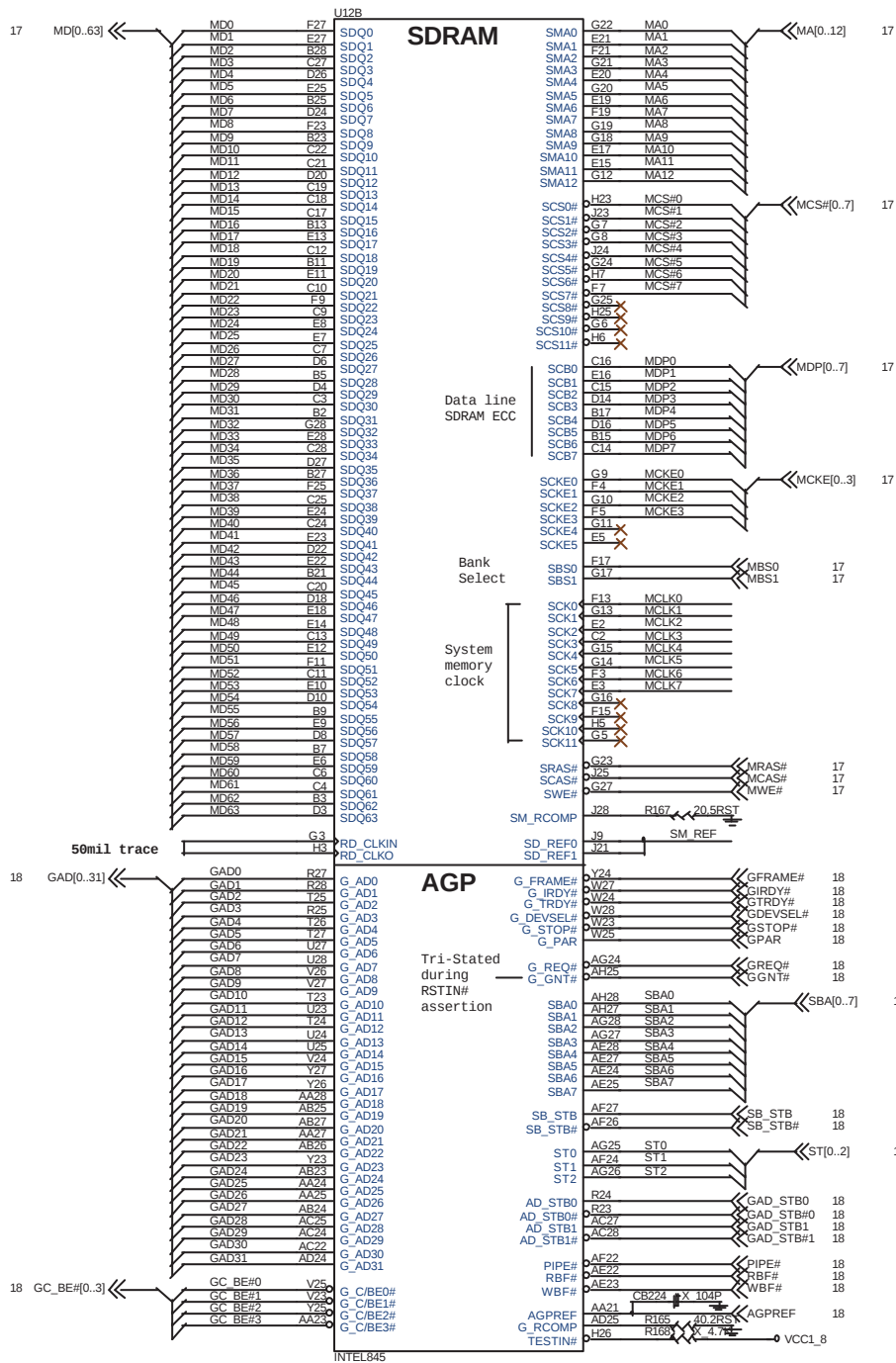
## CPU DECOUPLING CAPACITORS



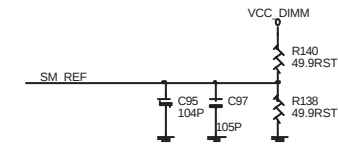
PLACE CAPS WITHIN CPU CAVITY SOLDER

|            |                     |                          |               |
|------------|---------------------|--------------------------|---------------|
| Micro-Star | Title               | MS-6532                  | Rev           |
|            | Document Number     | INTEL mPGA478-B CPU2     | 1.0B          |
|            | Last Revision Date: | Wednesday, July 25, 2001 | Sheet 7 of 32 |

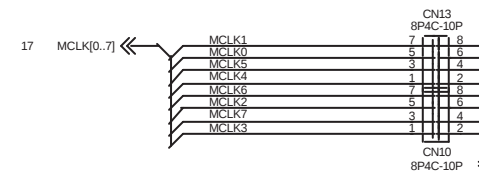




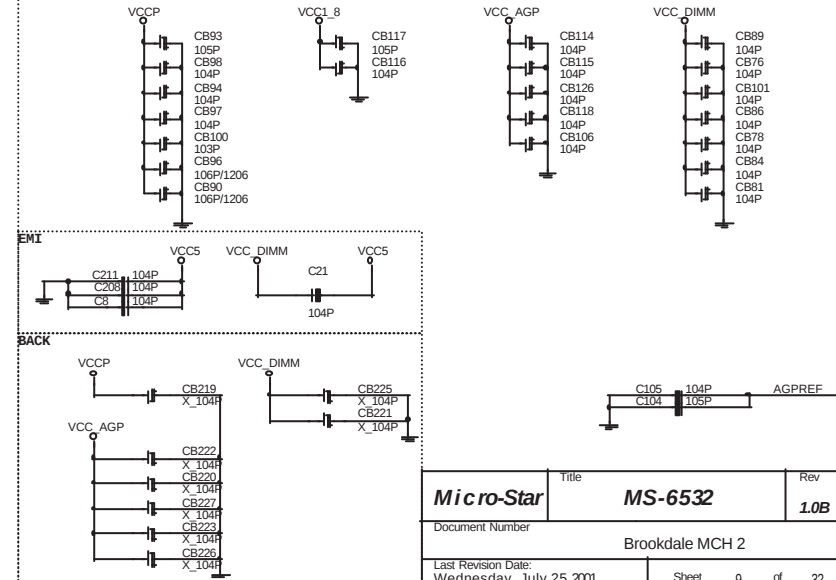
## MCH REFERENCE VOLTAGE



## MCH MEMORY CLOCK RC CIRCUITS

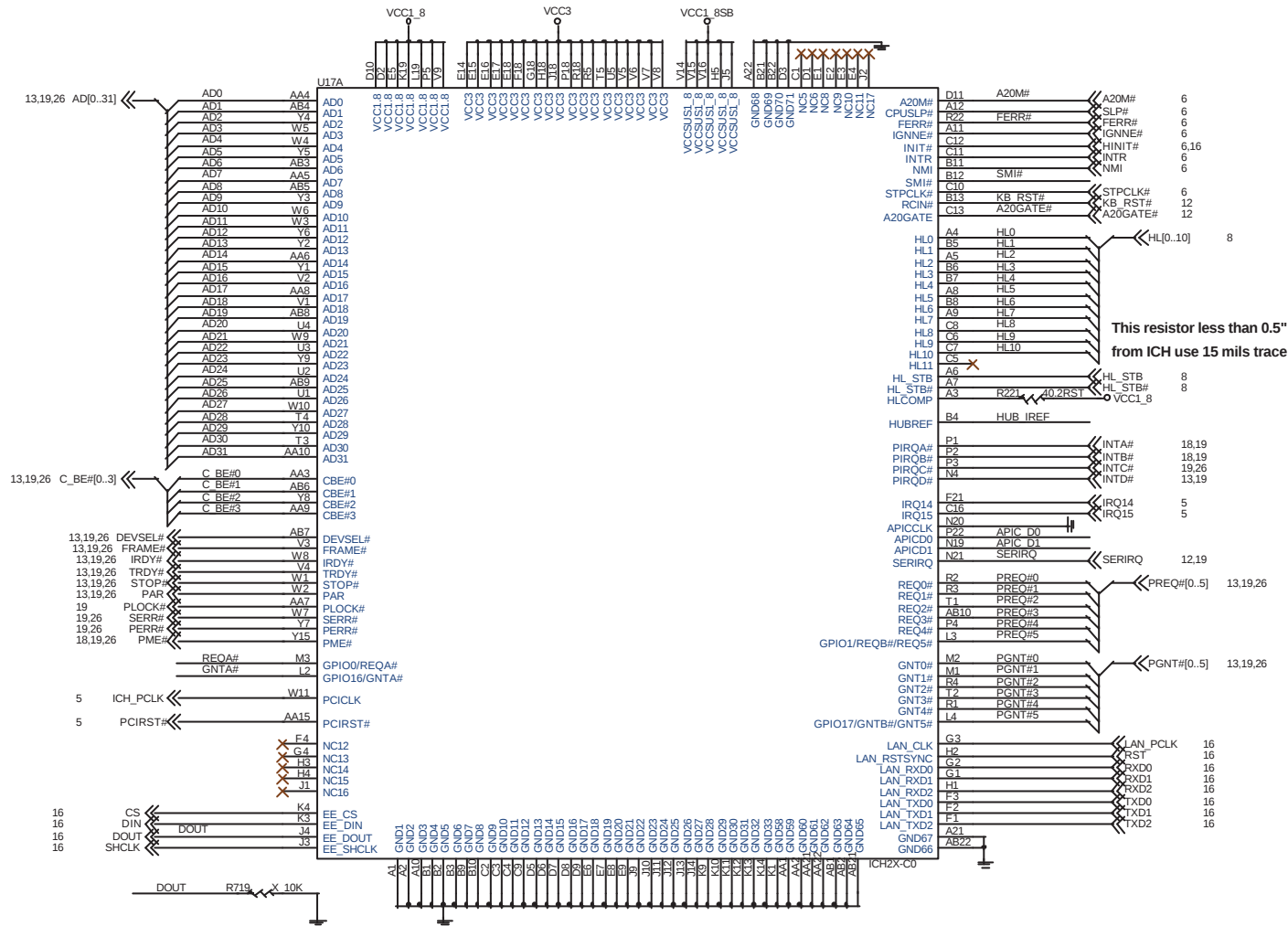


## MCH DECOUPLING CAPACITOR

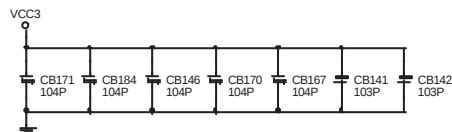


|                     |                          |         |     |      |
|---------------------|--------------------------|---------|-----|------|
| Micro-Star          | Title                    | MS-6532 | Rev | 1.0B |
| Document Number     | Brookdale MCH 2          |         |     |      |
| Last Revision Date: | Wednesday, July 25, 2001 |         |     |      |
| Sheet               | g                        | of      | 32  |      |

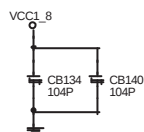
## ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



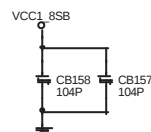
## ICH2 DECOUPLING CAPACITORS



Place one 0.1uF/0.01uF pair in each corner and 2 on opposite sides close to ICH2 if it fits

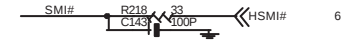


Distribute near the 1.8V power pin of the ICH2

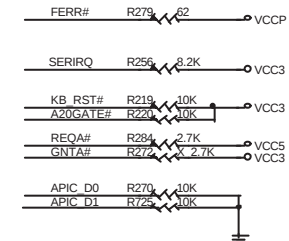


Distribute near the VCC1\_8SB power pin of the ICH2

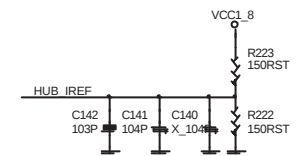
## ICH2 SMI# SIGNAL



## ICH2 STRAPPING RESISTORS



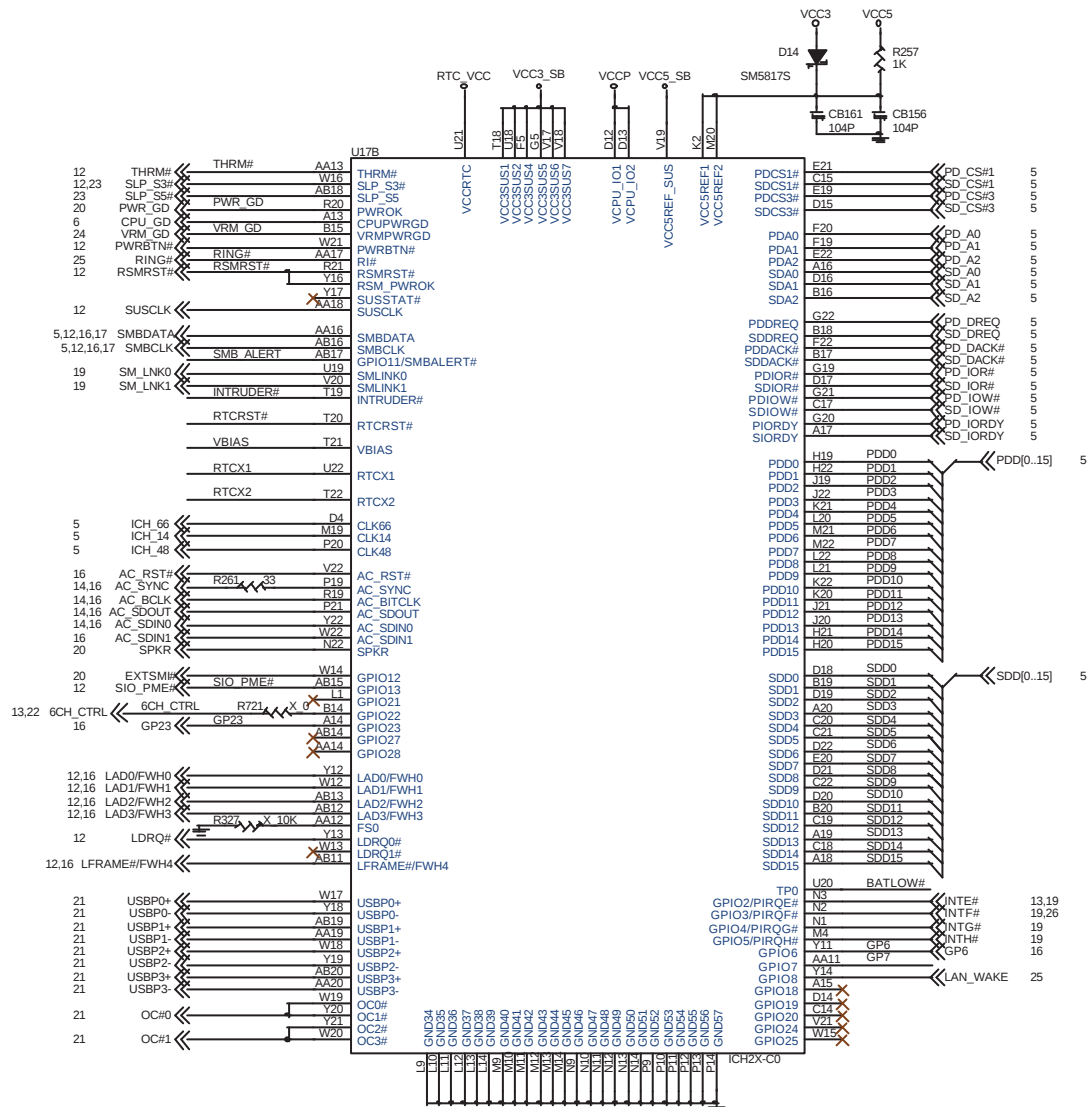
## ICH2 REFERENCE VOLTAGE



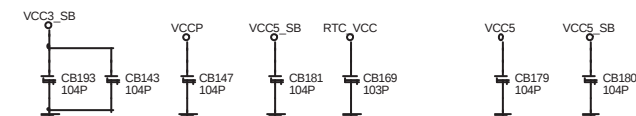
Place Cap. as Close as possible to ICH2  
Trace width use 15 mils and 15mils space

|            |                     |                          |       |          |
|------------|---------------------|--------------------------|-------|----------|
| Micro-Star | Title               | MS-6532                  | Rev   | 1.0B     |
|            | Document Number     | Brookdale ICH2 PCI       |       |          |
|            | Last Revision Date: | Wednesday, July 25, 2001 | Sheet | 10 of 32 |

# ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

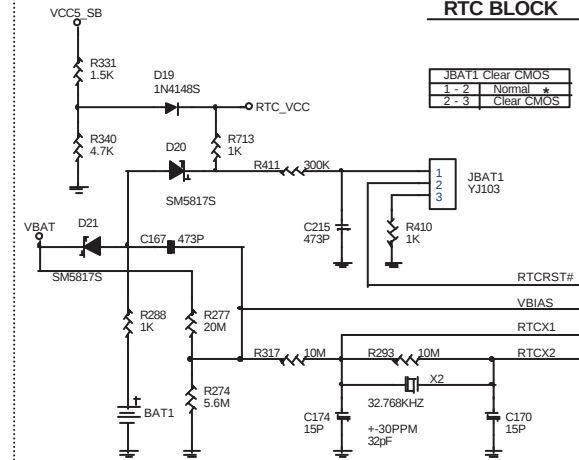


## ICH2 DECOUPLING CAPACITOR

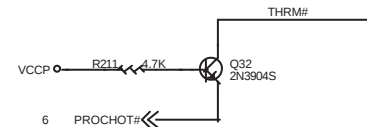


Distribute near the VCC3\_SB power pin of the ICH

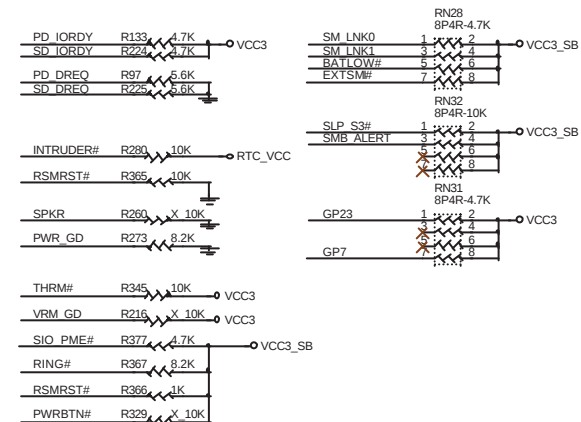
## RTC BLOCK



## PROCHOT BLOCK

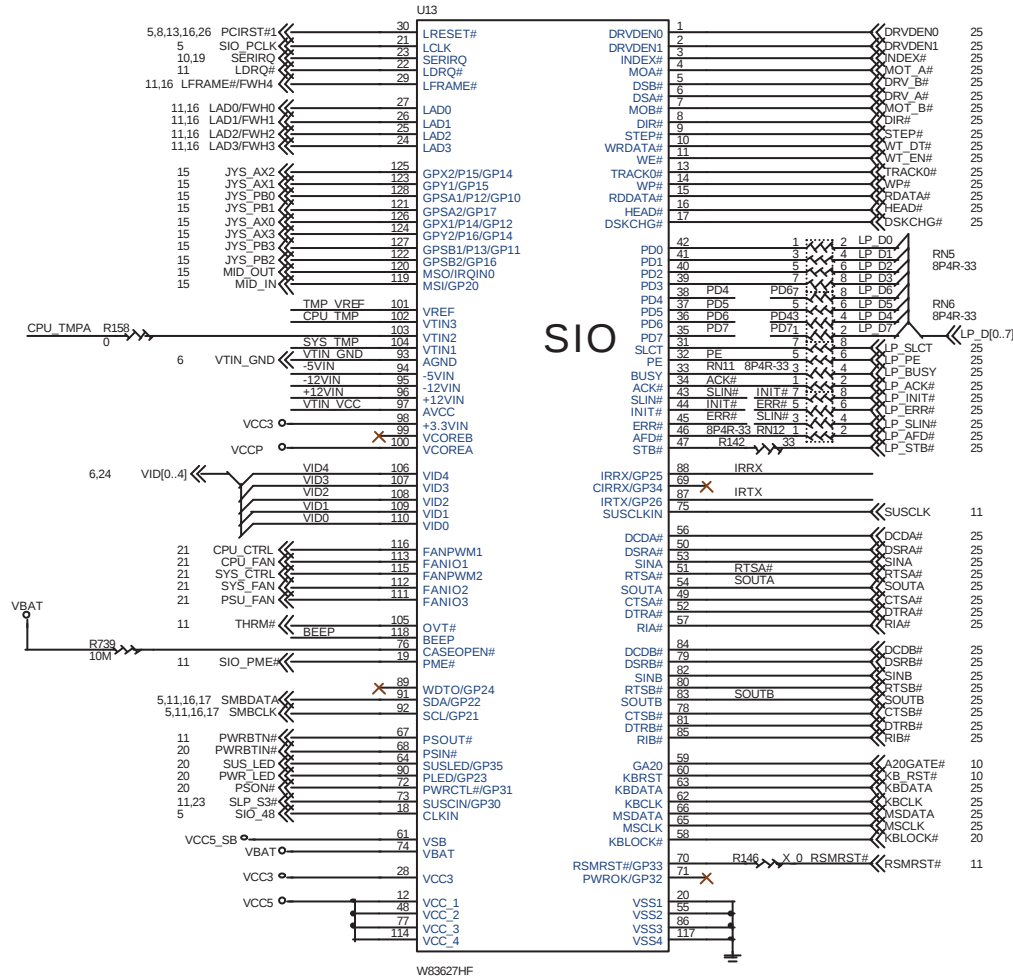


## ICH2 STRAPPING RESISTORS



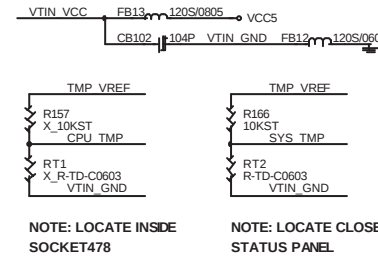
|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| Micro-Star                                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                 | Brookdale ICH2 Other    |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 | Sheet                   | 11 of 32           |

## LPC SUPER I/O W83627HF

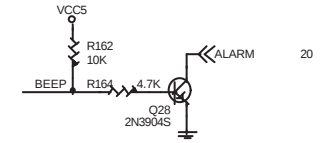


W83627HF

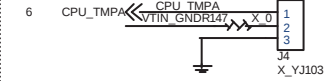
## THERMAL RESISTOR BLOCK



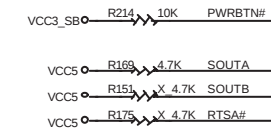
## SPEAKER BLOCK



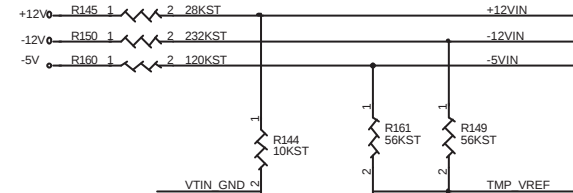
## CPU Temperature Read



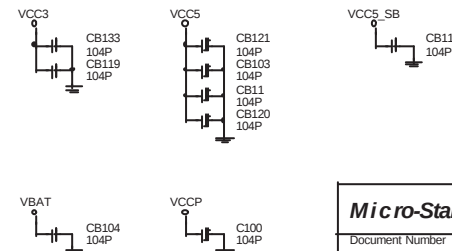
## SUPER I/O STRAPPING RESISTOR



|       |                |                   |
|-------|----------------|-------------------|
| SOUTA | L: Disable KBC | H: Enable KBC     |
| SOUTB | L: 24MHz       | H: 48MHz          |
| RTSA# | L: CFAD=2E     | H: CFAD=4E        |
| DTRA# | L: PNP Default | H: PNP no Default |

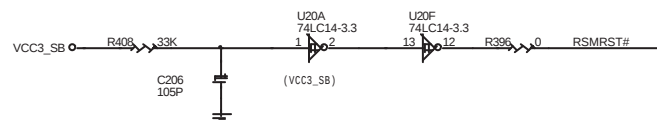


## DECOUPLING CAPACITOR

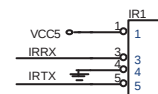


## RESUME RESET CIRCUIT BLOCK

Stuff all for D Version bug

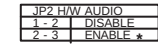


## IR HEADER

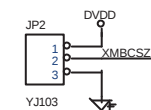


|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| Micro-Star                                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                 | LPC I/O W83627HF        |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 | Sheet                   | 12 of 32           |

IF Use AD1881  
S/W Codec  
remove all  
H/W Audio  
Components

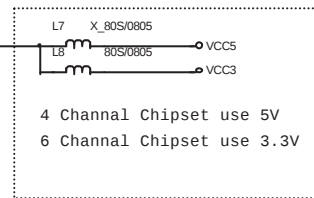


```
* MBCSZ : AUDIO CHIP SELECT
    HI : DISABLE
    LOW : ENABLE
```



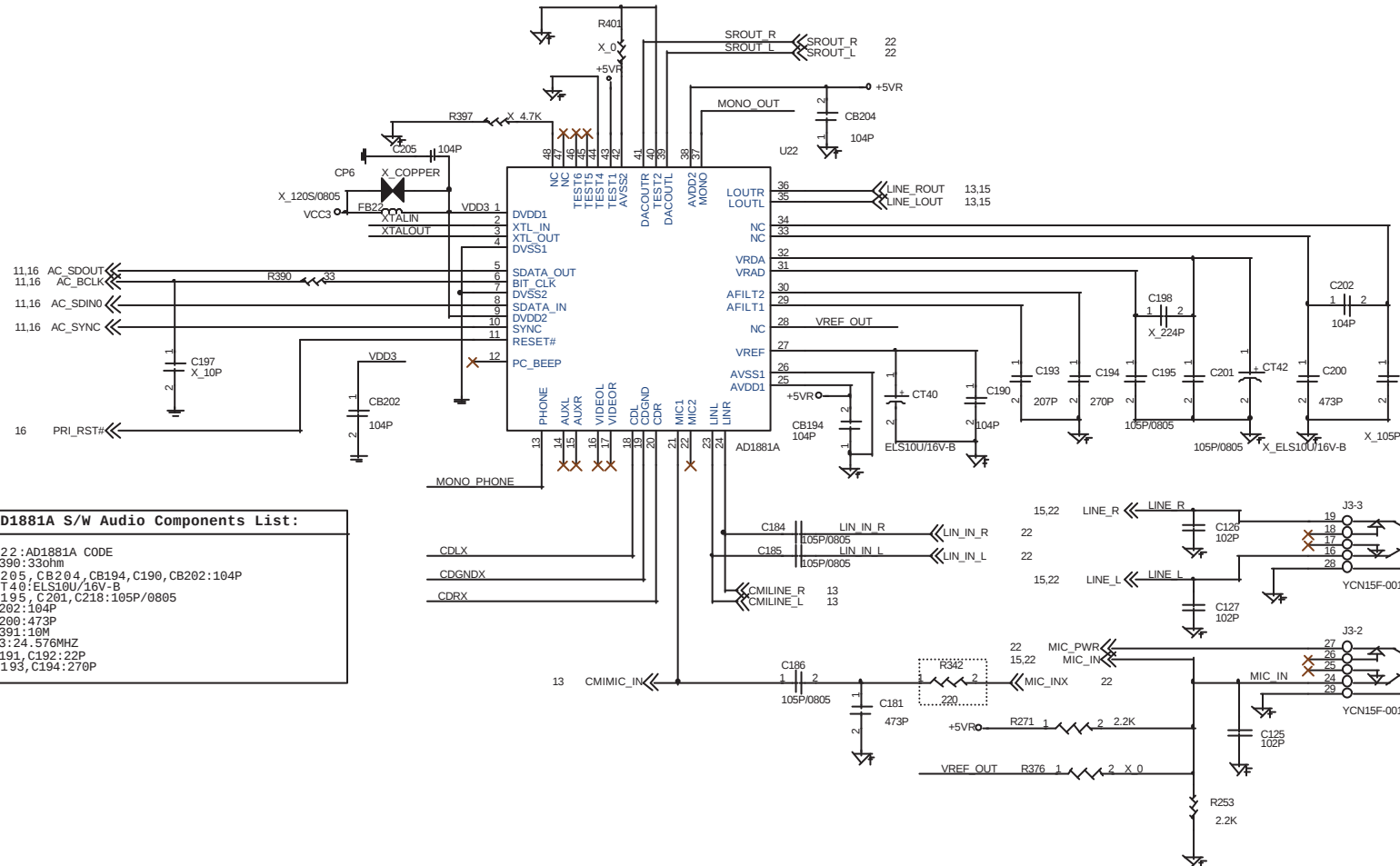
EECS R297 4.7K +5VR

Internal ID Selection



|                                                 |       |                       |     |                    |
|-------------------------------------------------|-------|-----------------------|-----|--------------------|
| <b><i>MicroStar</i></b>                         | Title | <b><i>MS-6532</i></b> | Rev | <b><i>1.0B</i></b> |
| Document Number                                 |       |                       |     |                    |
| CM18738 PCI AUDIO                               |       |                       |     |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |       | Sheet                 | 13  | of 32              |

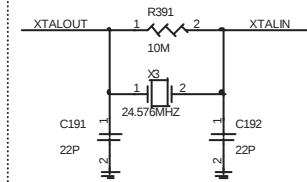
## AD1881A AC97 CODEC



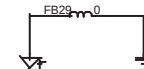
### AD1881A S/W Audio Components List:

U22:AD1881A CODE  
R390:330hm  
C205, CB204, CB194, C190, CB202:104P  
CT40:ELSI0U/16V-B  
C195, C201, C218:105P/0805  
C202:104P  
C200:473P  
R391:10M  
X3:24.576MHZ  
C191, C192:22P  
C193, C194:270P

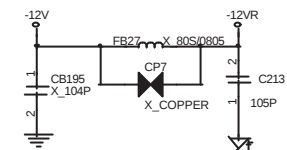
### AUDIO CODE CRYSTAL CIRCUIT



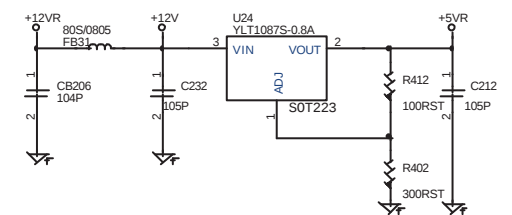
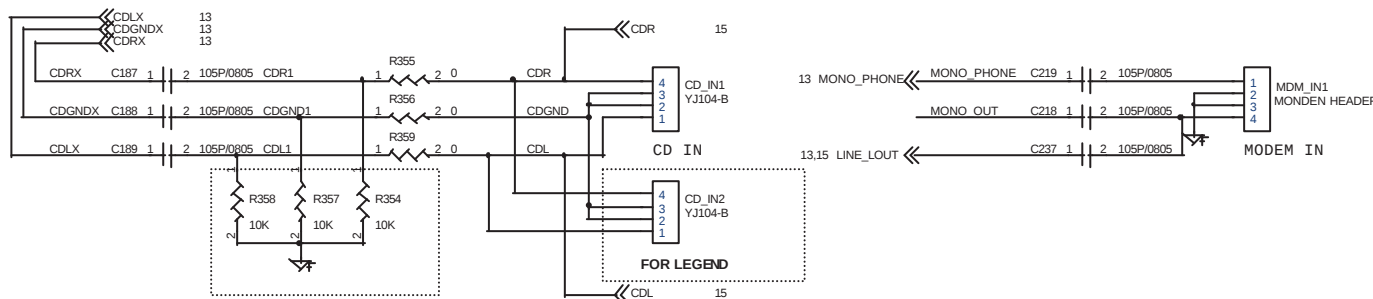
### DECOUPLING CAPACITOR



### AUDIO CODE REGULATORS

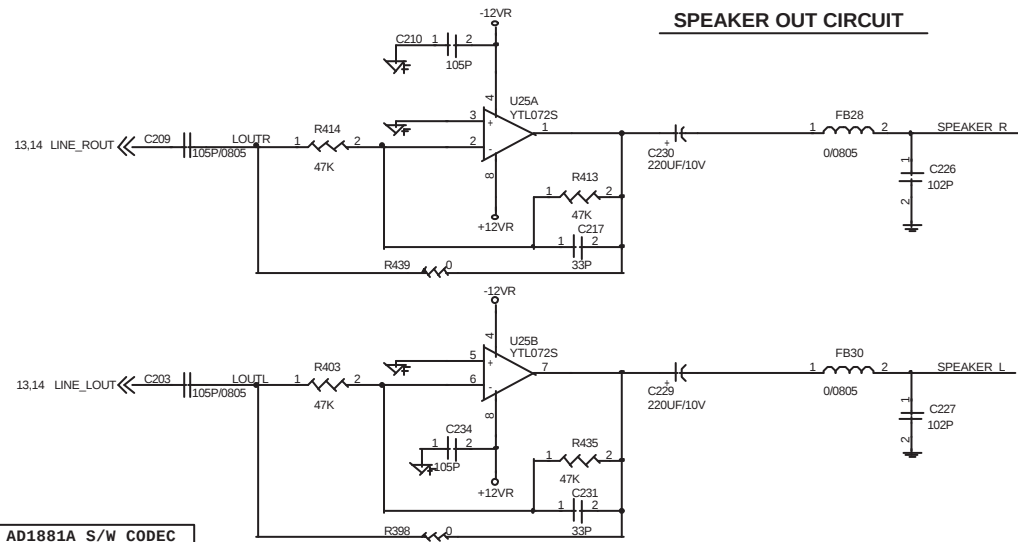


### AUDIO CODE CD / AUX / MODEM IN HEADERS

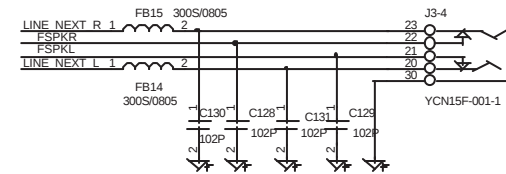


|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| Micro-Star                                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                 | AC97 CODEC AD1885       |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 | Sheet                   | 14 of 32           |

## SPEAKER OUT CIRCUIT

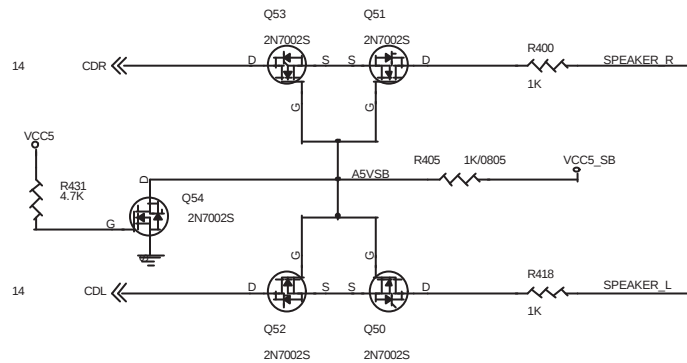


## SPEAKER OUT JACK

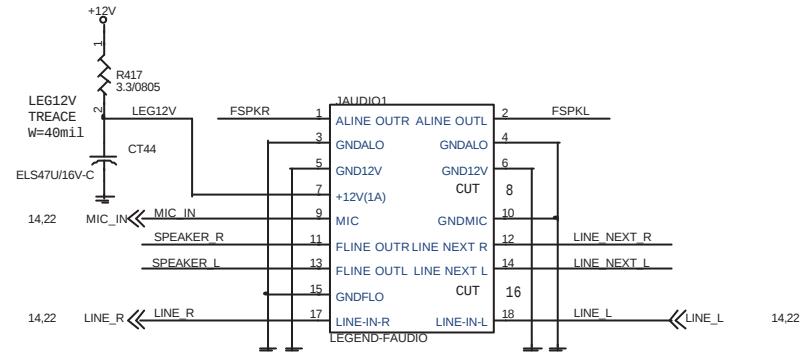


**AD1881A S/W CODEC COMPONENTS LIST:**  
 C210, C234:105P  
 R414, R435, R413, R403:47K  
 C217, C231:33P  
 R439, R398:NC

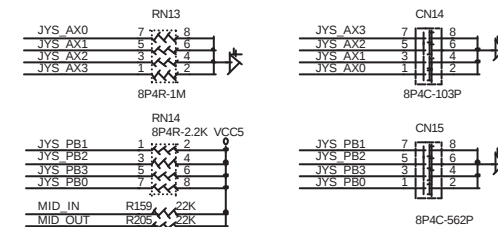
## CD PANEL PLAY WITHOUT PC POWER\_ON



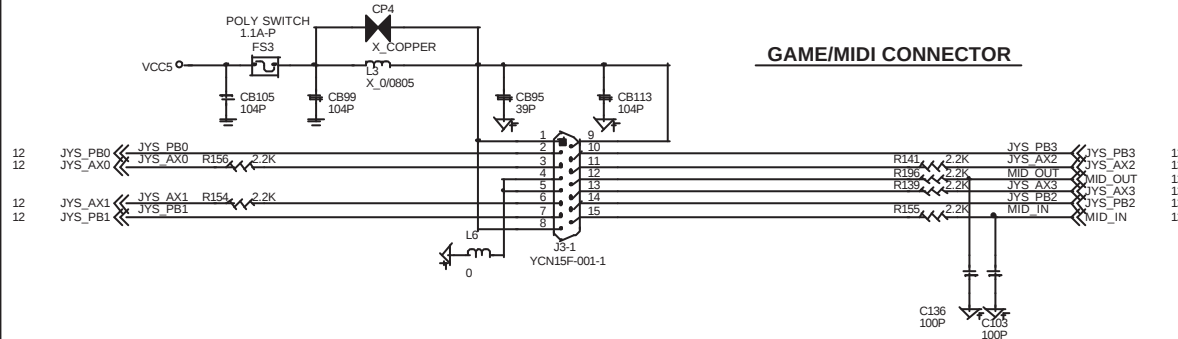
## FOR MSI INTERNAL HEADER



## FOR LEGEND

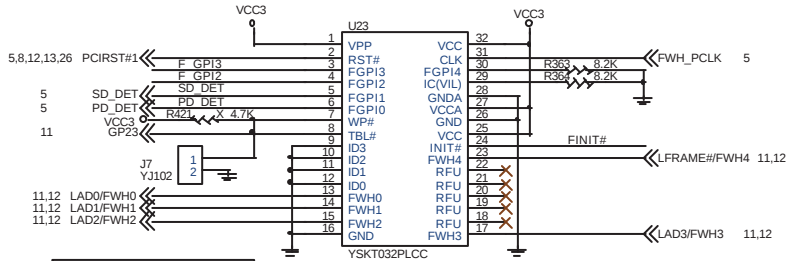


## GAME/MIDI CONNECTOR



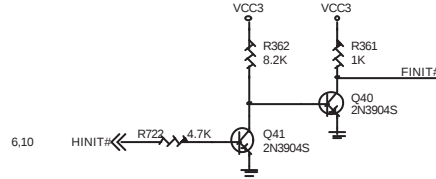
|                     |                          |         |     |       |
|---------------------|--------------------------|---------|-----|-------|
| Micro-Star          | Title                    | MS-6532 | Rev | 1.0B  |
| Document Number     | Audio Amp TL072 & GAME   |         |     |       |
| Last Revision Date: | Wednesday, July 25, 2001 | Sheet   | 15  | of 32 |

## Firmware Hub (FWH)

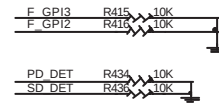


|                |            |
|----------------|------------|
| J7 BIOS Update |            |
| SHORT          | Locked     |
| OPEN           | Unlocked * |

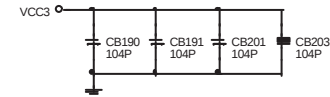
## FWH INIT Signal Voltage Translation Block



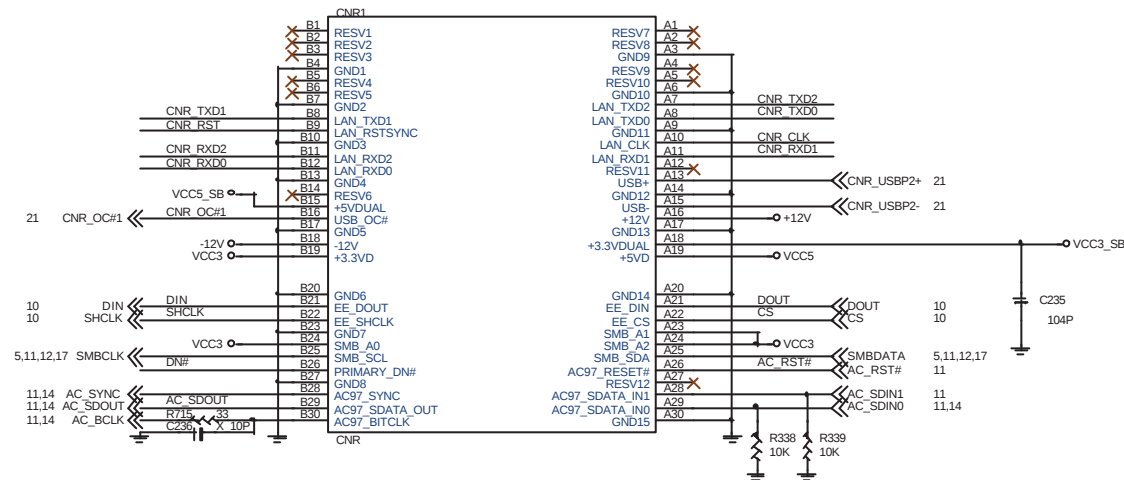
## FWH RESISTORS



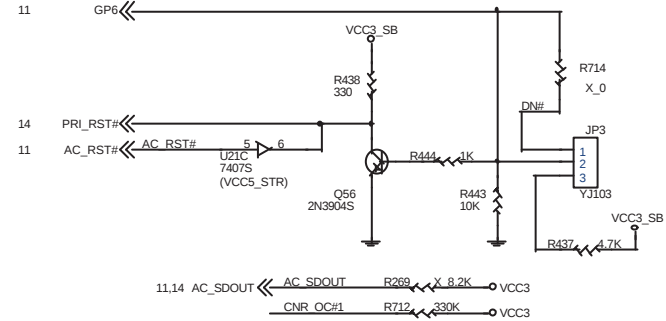
## FWH DECOUPLING CAPACITORS



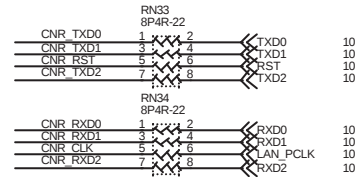
## CNR RISE



|       |                              |
|-------|------------------------------|
| JP3   | AUDIO DOWN                   |
| 1 - 2 | Auto mode                    |
| 2 - 3 | Disabled onboard audio codec |



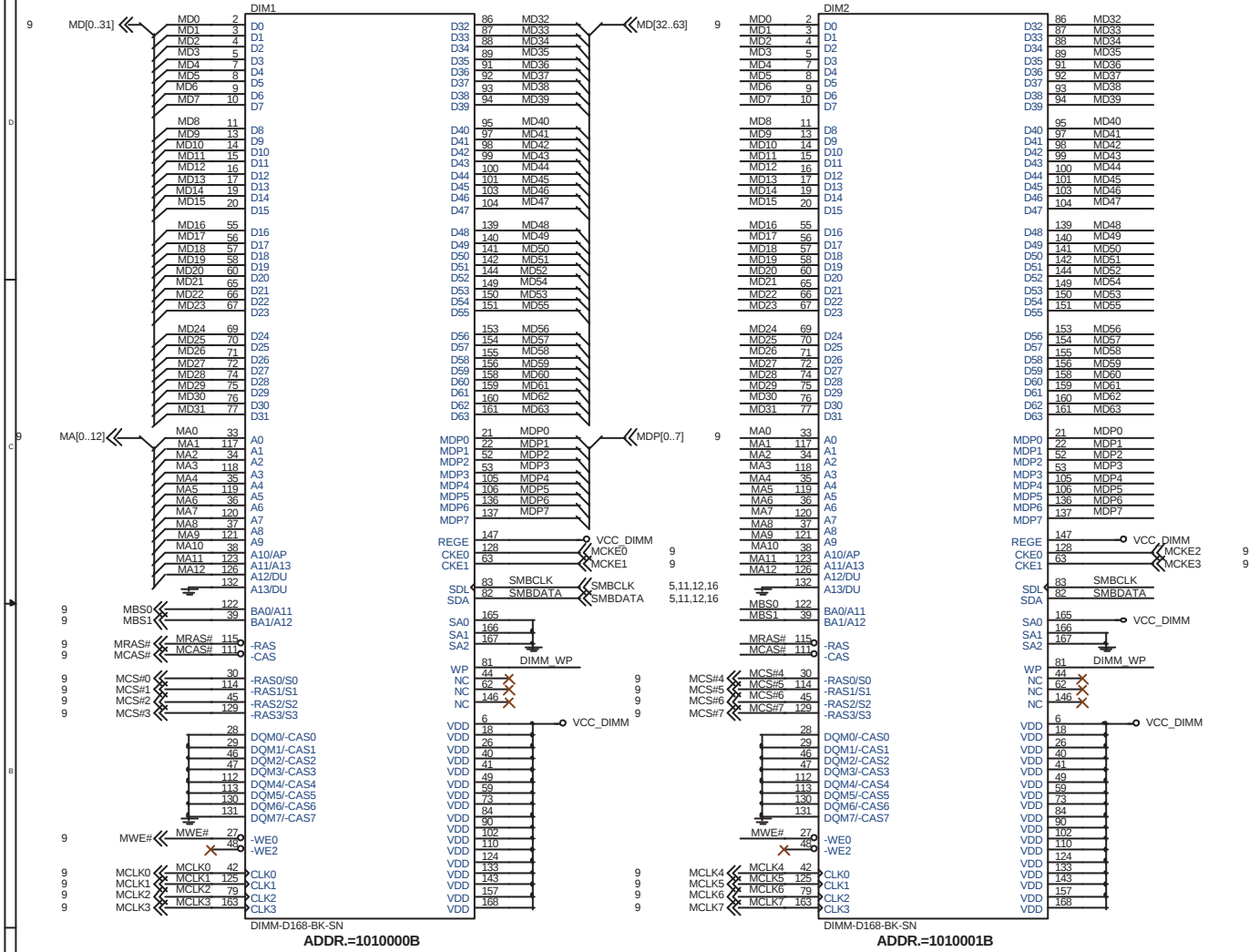
## NEAR ICH2

 $2.5'' < L < 9$ 

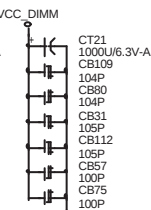
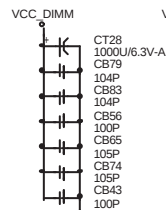
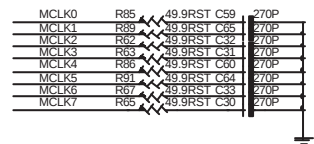
|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| <b>Micro-Star</b>                               | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number<br><b>FWH &amp; CNR</b>         |                         |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |                         | Sheet 16 of 32     |

# DIMM1

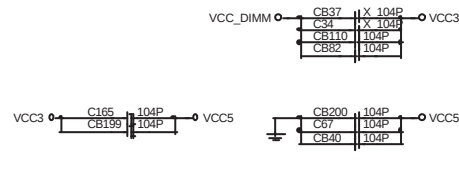
# DIMM2



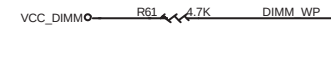
## DIMM CLOCK



## DECOUPLING CAPACITORS



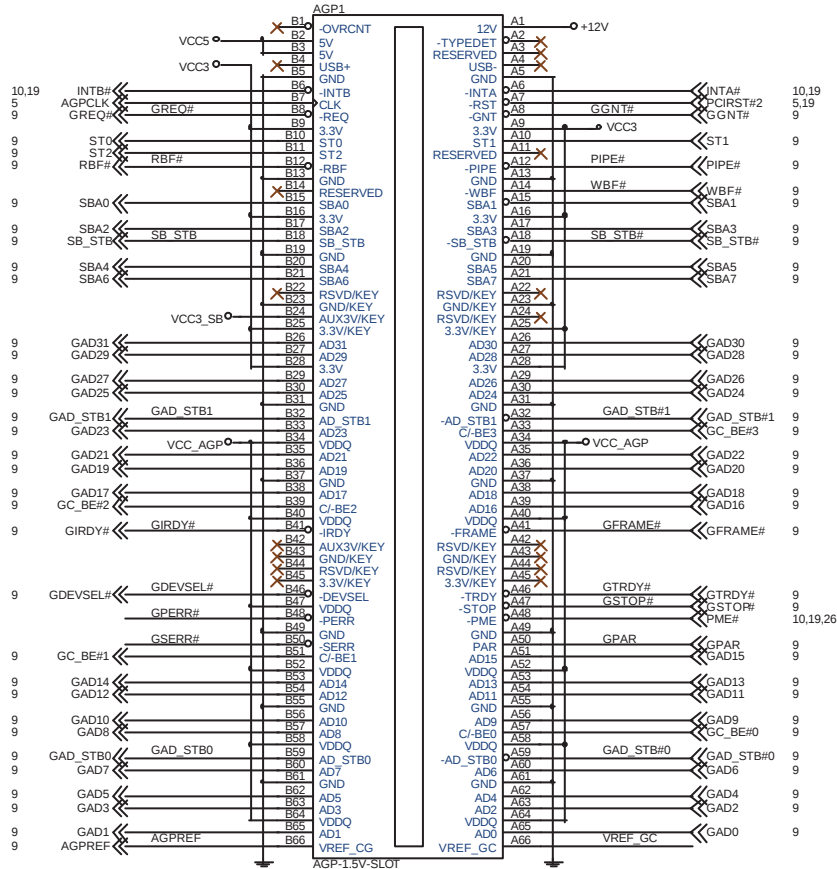
## DIMM SPD WE BLOCK



|            |                     |                          |       |          |
|------------|---------------------|--------------------------|-------|----------|
| Micro-Star | Title               | MS-6532                  | Rev   | 1.0B     |
|            | Document Number     | DIMM 1 & 2               |       |          |
|            | Last Revision Date: | Wednesday, July 25, 2001 | Sheet | 17 of 32 |

# AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



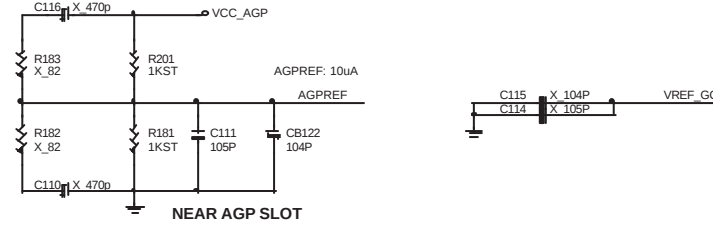
VREF\_GC:form  
the chipset  
to the  
graphics  
controller

AGP Slot Imax  
VCC\_AGP 8.0A  
VCC3 6.0A  
VCC12 1.0A  
VCC5 2.0A

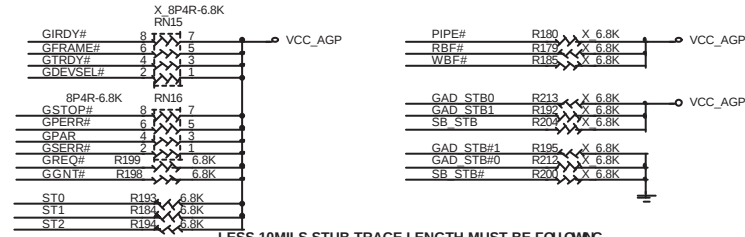
INTA#  
INTB#

VREF\_GC:form  
the graphics  
controller to  
the chipset

## AGP SIGNAL REFERENCE CIRCUIT

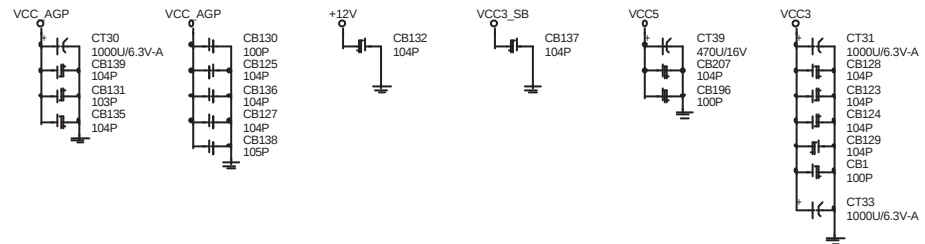


## AGP TERMINATION RESISTORS

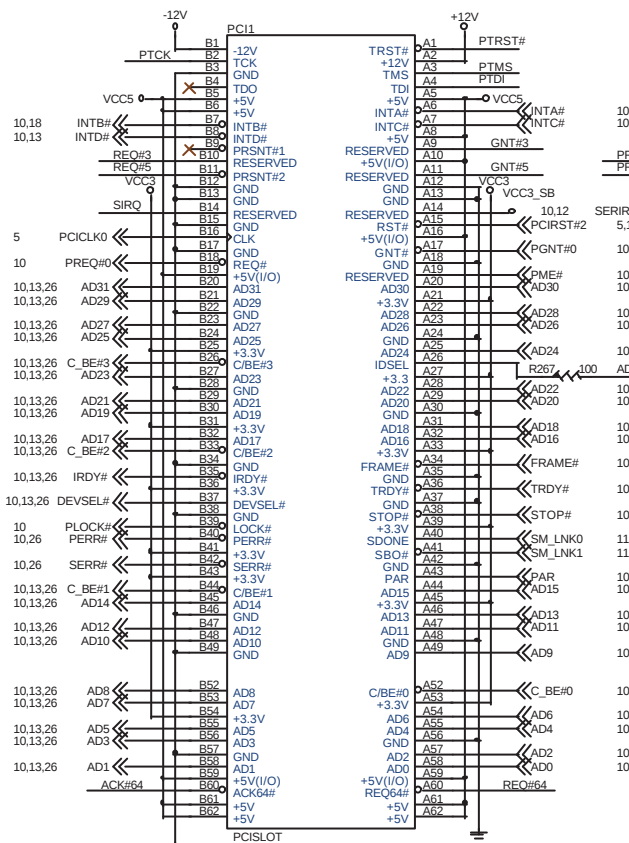


Place these resistors between PCI and AGP slot

## AGP SLOT DECOUPLING CAPACITORS



|                     |                          |         |     |      |
|---------------------|--------------------------|---------|-----|------|
| Micro-Star          | Title                    | MS-6532 | Rev | 1.0B |
| Document Number     | AGP Slot                 |         |     |      |
| Last Revision Date: | Wednesday, July 25, 2001 |         |     |      |
| Sheet               | 18                       | of      | 32  |      |



Pin-to-pin comparison diagram for the PCISLOT connector. The diagram shows two rows of pins, one for the PCISLOT (left) and one for the PCISLOT (right). Each pin is labeled with its number, a signal name, and its function. The PCISLOT pins are numbered 1 to 100, and the PCISLOT pins are numbered 1 to 100. The diagram shows the mapping between the two connectors, including power pins (VCC, GND), data pins (DATA0-19), control pins (CS, RD, WR, INT), and status pins (ACK, TRDY, STOP, FRAME, SERR, PERR, SERP, SERR#, PERR#, SERP#).

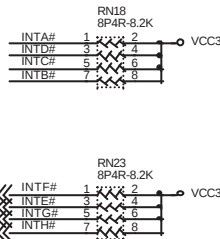
| PCISLOT Pin | Signal | PCISLOT Pin | Signal |
|-------------|--------|-------------|--------|
| 1           | B1     | 1           | A1     |
| 2           | B2     | 2           | A2     |
| 3           | B3     | 3           | A3     |
| 4           | B4     | 4           | A4     |
| 5           | B5     | 5           | A5     |
| 6           | B6     | 6           | A6     |
| 7           | B7     | 7           | A7     |
| 8           | B8     | 8           | A8     |
| 9           | B9     | 9           | A9     |
| 10          | B10    | 10          | A10    |
| 11          | B11    | 11          | A11    |
| 12          | B12    | 12          | A12    |
| 13          | B13    | 13          | A13    |
| 14          | B14    | 14          | A14    |
| 15          | B15    | 15          | A15    |
| 16          | B16    | 16          | A16    |
| 17          | B17    | 17          | A17    |
| 18          | B18    | 18          | A18    |
| 19          | B19    | 19          | A19    |
| 20          | B20    | 20          | A20    |
| 21          | B21    | 21          | A21    |
| 22          | B22    | 22          | A22    |
| 23          | B23    | 23          | A23    |
| 24          | B24    | 24          | A24    |
| 25          | B25    | 25          | A25    |
| 26          | B26    | 26          | A26    |
| 27          | B27    | 27          | A27    |
| 28          | B28    | 28          | A28    |
| 29          | B29    | 29          | A29    |
| 30          | B30    | 30          | A30    |
| 31          | B31    | 31          | A31    |
| 32          | B32    | 32          | A32    |
| 33          | B33    | 33          | A33    |
| 34          | B34    | 34          | A34    |
| 35          | B35    | 35          | A35    |
| 36          | B36    | 36          | A36    |
| 37          | B37    | 37          | A37    |
| 38          | B38    | 38          | A38    |
| 39          | B39    | 39          | A39    |
| 40          | B40    | 40          | A40    |
| 41          | B41    | 41          | A41    |
| 42          | B42    | 42          | A42    |
| 43          | B43    | 43          | A43    |
| 44          | B44    | 44          | A44    |
| 45          | B45    | 45          | A45    |
| 46          | B46    | 46          | A46    |
| 47          | B47    | 47          | A47    |
| 48          | B48    | 48          | A48    |
| 49          | B49    | 49          | A49    |
| 50          | B50    | 50          | A50    |
| 51          | B51    | 51          | A51    |
| 52          | B52    | 52          | A52    |
| 53          | B53    | 53          | A53    |
| 54          | B54    | 54          | A54    |
| 55          | B55    | 55          | A55    |
| 56          | B56    | 56          | A56    |
| 57          | B57    | 57          | A57    |
| 58          | B58    | 58          | A58    |
| 59          | B59    | 59          | A59    |
| 60          | B60    | 60          | A60    |
| 61          | B61    | 61          | A61    |
| 62          | B62    | 62          | A62    |
| 63          | B63    | 63          | A63    |
| 64          | B64    | 64          | A64    |
| 65          | B65    | 65          | A65    |
| 66          | B66    | 66          | A66    |
| 67          | B67    | 67          | A67    |
| 68          | B68    | 68          | A68    |
| 69          | B69    | 69          | A69    |
| 70          | B70    | 70          | A70    |
| 71          | B71    | 71          | A71    |
| 72          | B72    | 72          | A72    |
| 73          | B73    | 73          | A73    |
| 74          | B74    | 74          | A74    |
| 75          | B75    | 75          | A75    |
| 76          | B76    | 76          | A76    |
| 77          | B77    | 77          | A77    |
| 78          | B78    | 78          | A78    |
| 79          | B79    | 79          | A79    |
| 80          | B80    | 80          | A80    |
| 81          | B81    | 81          | A81    |
| 82          | B82    | 82          | A82    |
| 83          | B83    | 83          | A83    |
| 84          | B84    | 84          | A84    |
| 85          | B85    | 85          | A85    |
| 86          | B86    | 86          | A86    |
| 87          | B87    | 87          | A87    |
| 88          | B88    | 88          | A88    |
| 89          | B89    | 89          | A89    |
| 90          | B90    | 90          | A90    |
| 91          | B91    | 91          | A91    |
| 92          | B92    | 92          | A92    |
| 93          | B93    | 93          | A93    |
| 94          | B94    | 94          | A94    |
| 95          | B95    | 95          | A95    |
| 96          | B96    | 96          | A96    |
|             |        |             |        |

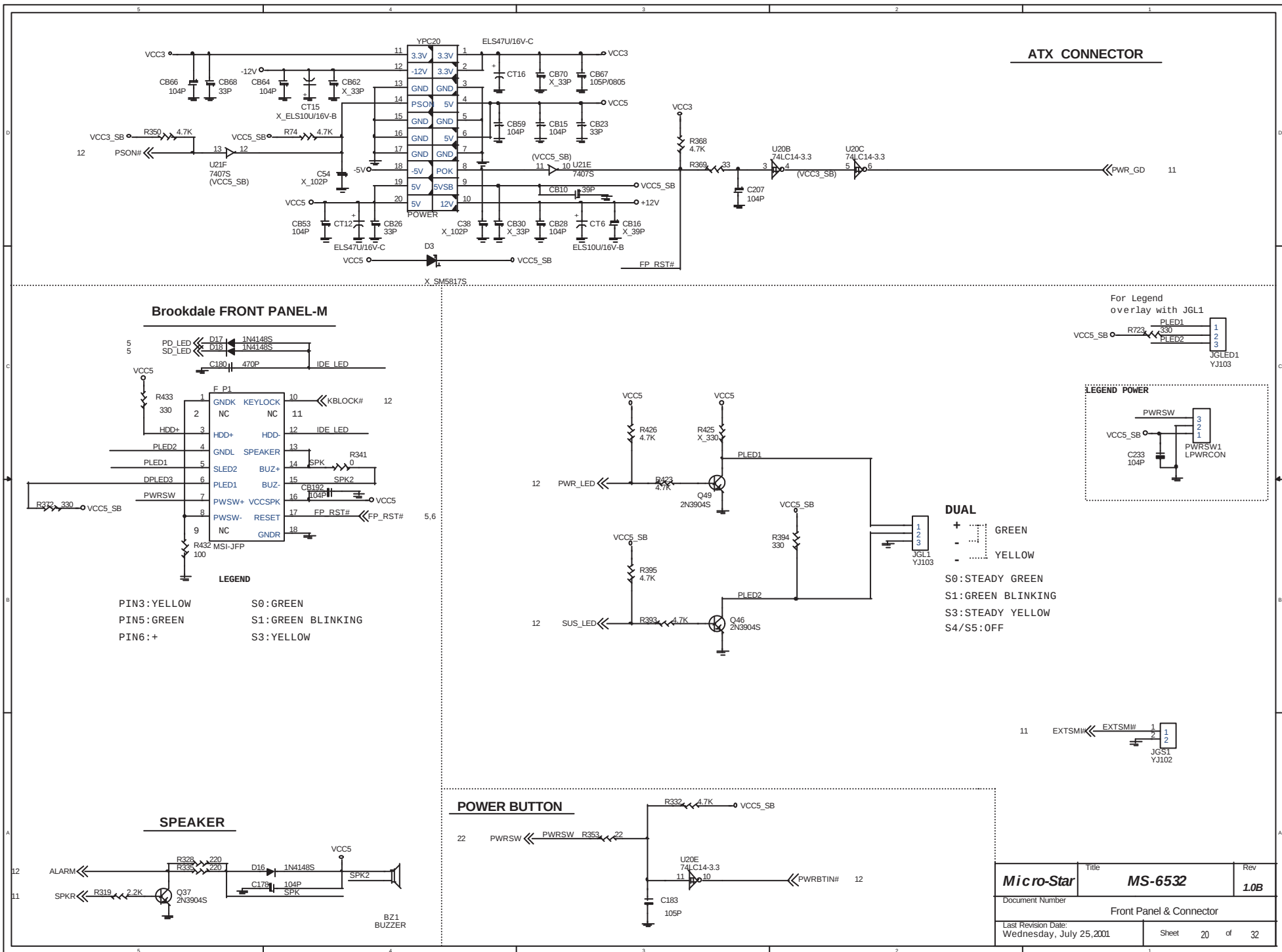
Pin connections for the 894R-2.7K microcontroller:

- Header RN20 (894R-2.7K):**
  - Pin 1: VCC5
  - Pin 2: FRAME#
  - Pin 3: TRDY#
  - Pin 4: DEVSEL#
  - Pin 5: IXX#
- Header RN21 (894R-2.7K):**
  - Pin 1: STOP#
  - Pin 2: PLOCK#
  - Pin 3: PERR#
  - Pin 4: SERR#
  - Pin 5: PREQ#0
  - Pin 6: PREQ#2
  - Pin 7: PREQ#1
  - Pin 8: PREQ#3
  - Pin 9: PREQ#5
  - Pin 10: PREQ#7
  - Pin 11: Q#3
  - Pin 12: Q#4
- Header RN22 (894R-2.7K):**
  - Pin 1: PREQ#0
  - Pin 2: PREQ#2
  - Pin 3: PREQ#1
  - Pin 4: PREQ#3
  - Pin 5: PREQ#5
  - Pin 6: PREQ#7
  - Pin 7: Q#3
  - Pin 8: Q#4
  - Pin 9: Q#5
  - Pin 10: Q#6
  - Pin 11: VCC5
  - Pin 12: GND

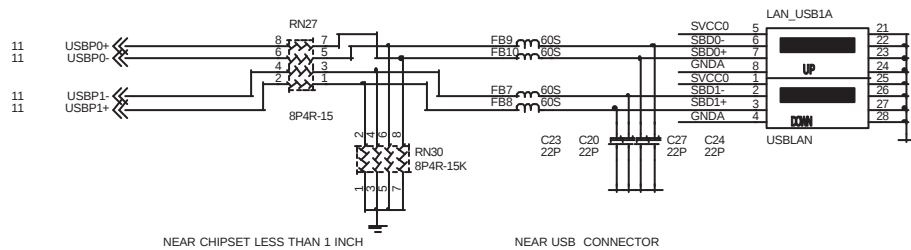
Figure 10 shows the pin connections for the R1919 module. The module is labeled 'RN19' and 'X\_10PBR-2.7K'. The connections are as follows:

| Signal  | Pin | Connection |
|---------|-----|------------|
| PGNT#2  | 1   | VCC5       |
| PGNT#1  | 2   | VCC5       |
| PGNT#3  | 3   | VCC5       |
| PGNT#0  | 4   | VCC5       |
| PGNT#4  | 5   | VCC5       |
| PGNT#5  | 6   | VCC5       |
| PGNT#7  | 7   | VCC5       |
| PGNT#8  | 8   | VCC5       |
| PGNT#9  | 9   | VCC5       |
| PGNT#10 | 10  | VCC5       |
| REQ#64  | 11  | VCC5       |
| ACK#64  | 12  | VCC5       |
| PTMS    | 13  | VCC5       |
| PTDI    | 14  | VCC5       |
| PTCK    | 15  | VCC5       |
| PTRS#   | 16  | VCC5       |

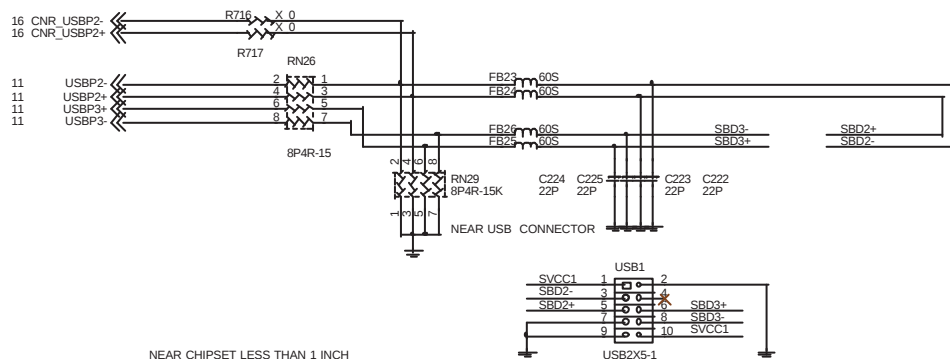
8



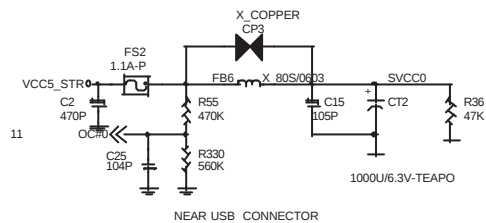
### BACK PANEL USB CONNECTOR FOR USB PORT 0,1



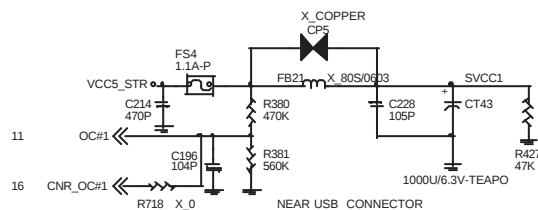
### FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



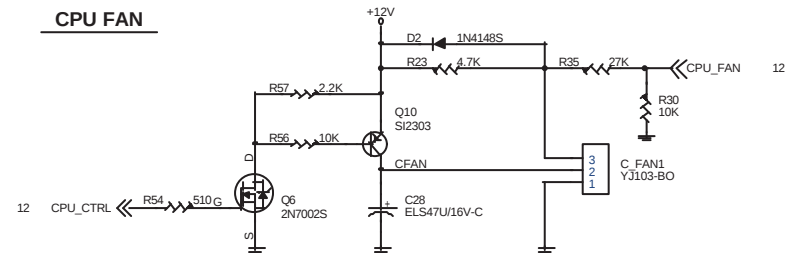
### POWER CIRCUIT FOR USB PORT 0,1



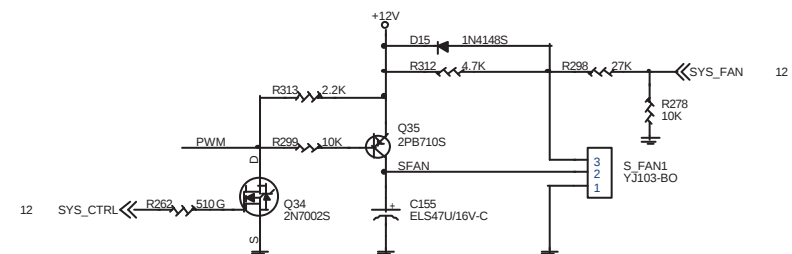
### POWER CIRCUIT FOR USB PORT 2, 3



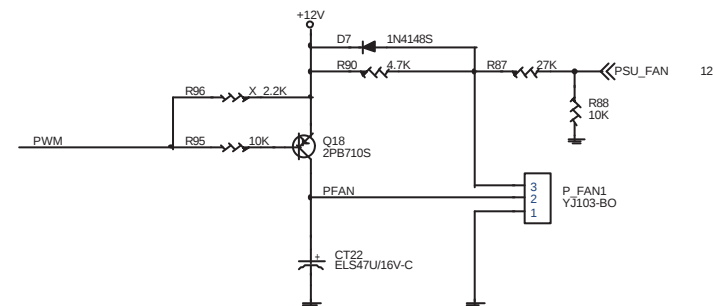
### CPU FAN



### SYSTEM FAN



### ATX PSU FAN ON/OFF CONTROL

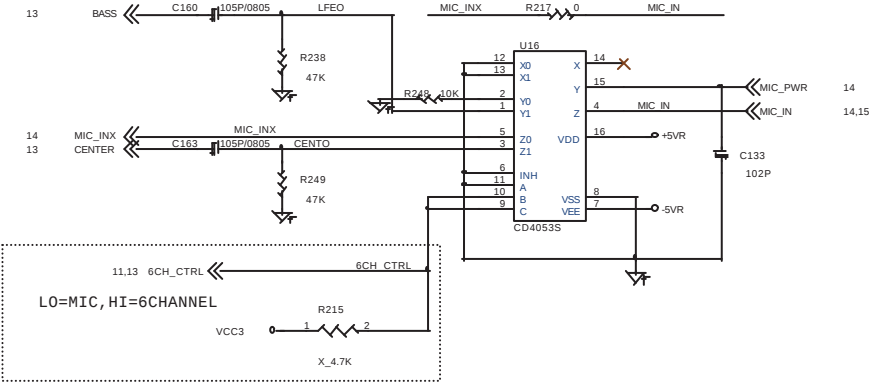
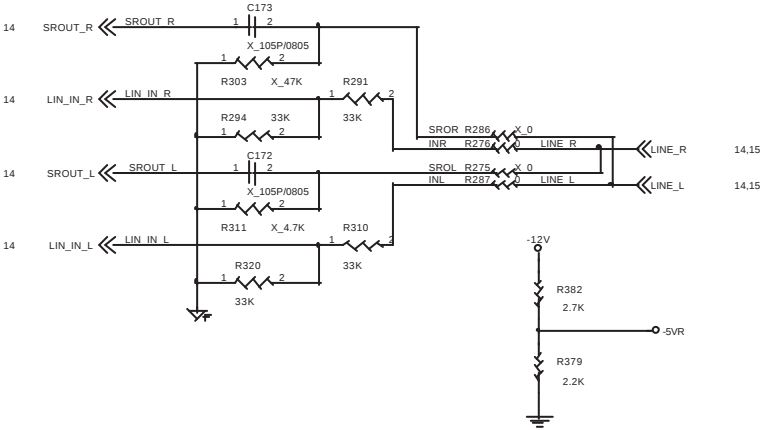


|                          |       |                |     |      |
|--------------------------|-------|----------------|-----|------|
| Micro-Star               | Title | MS-6532        | Rev | 1.0B |
| Document Number          |       |                |     |      |
| USB & FAN Connectors     |       |                |     |      |
| Last Revision Date:      |       | Sheet 21 of 32 |     |      |
| Wednesday, July 25, 2001 |       |                |     |      |

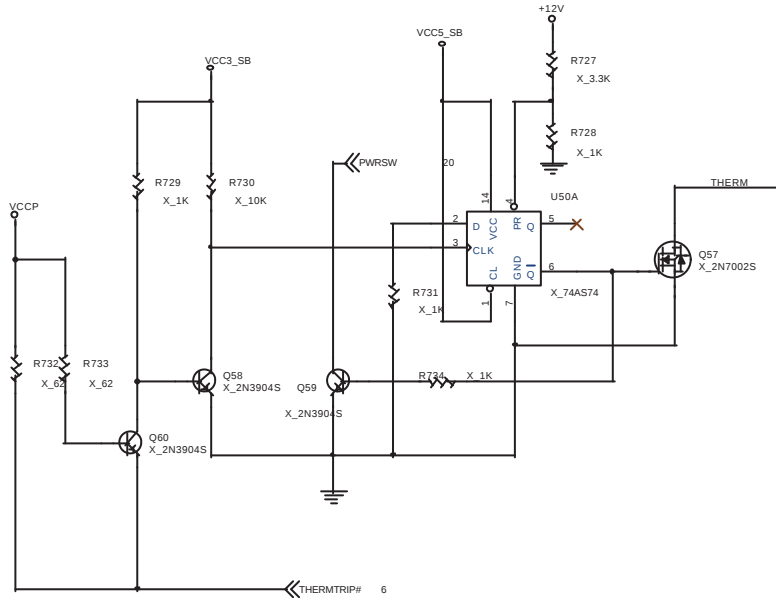
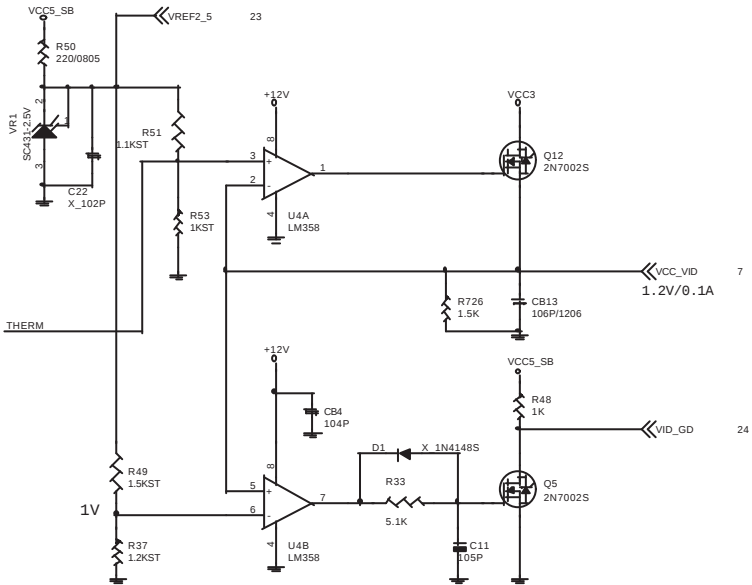
6 CHANNEL CONTROLLER

AD1881A S/W CODEC COMPONENTS LIST:

R217:0ohm  
C160, R238, C163, R249, U16, C133, R382, R379:X



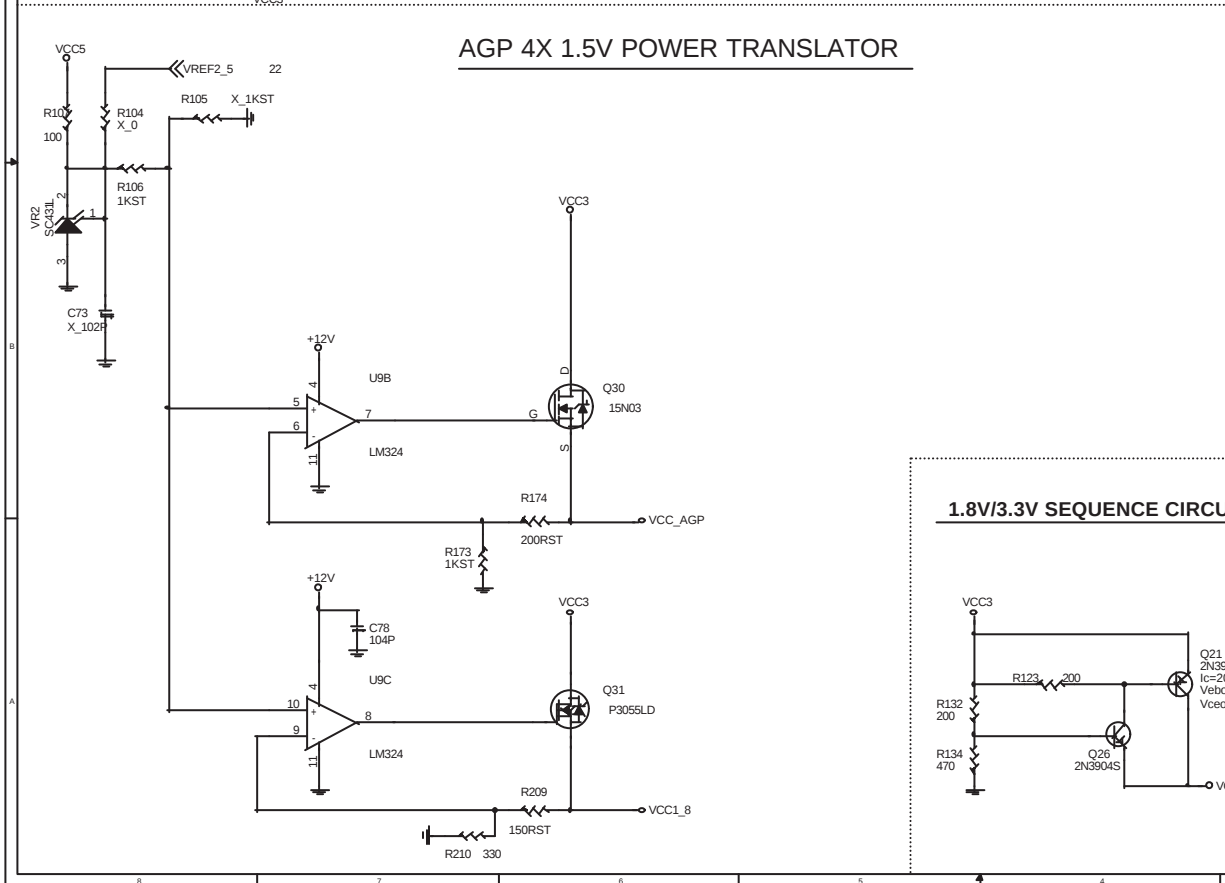
VCC\_VID / VID\_GOOD



|                          |       |         |          |      |
|--------------------------|-------|---------|----------|------|
| Micro-Star               | Title | MS-6532 | Rev      | 1.0B |
| Document Number          |       |         |          |      |
| VID & 6 CHANNEL CONTROL  |       |         |          |      |
| Last Revision Date:      |       |         | Sheet    |      |
| Wednesday, July 25, 2001 |       |         | 22 of 32 |      |

### POWER TRANSLATOR

| Power    | S0   | S3      | S5      |
|----------|------|---------|---------|
| VCC3_SB  | Main | Standby | Standby |
| VCC5_STR | Main | Standby | 0V      |
| VCC_DIMM | Main | Standby | 0V      |



### 1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)

The circuit diagram illustrates a 1.8V Standby Power Translator. It features a VLT10875-0.8A voltage translator (VR3) with three pins: VIN, VOUT, and ADJ. The VIN pin is connected to a VCC3\_SB supply, which is also connected to a 104pF capacitor (C137). The VOUT pin is connected to a VCC1\_8SB supply, which is also connected to a 104pF capacitor (C147). The ADJ pin is connected to ground through a 104pF capacitor (C159). The output of the translator is connected to a load, represented by a 432 ohm resistor (R252) in series with a 200 ohm resistor (R259). The output is also connected to a 100pF capacitor (C144) and a 104pF capacitor (C147). The output is labeled CT35 ELS47U/16V-C.

## POWER CONSUMPTION

|           | VCCP  | VCC_AGP | VCC1_8 | VCC3_DIMM | VCC3  | VCC5 | VCC5_SB | +12V  | -12V |
|-----------|-------|---------|--------|-----------|-------|------|---------|-------|------|
| CPU       | 69.0A | 0       | 0      | 0         | 0     | 0    | 0       | NOTE4 | 0    |
| PMCH      | 2.4A  | NOTE1   | 0.2A   | 2.0A      | 0     | 0    | 0       | 0     | 0    |
| ICH2      | 0     | 0       | NOTE3  | 0         | NOTE3 | 0    | NOTE3   | 0     | 0    |
| CY28324   | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| AD1885    | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| FWH_SST   | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| W83627HF  | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| HIP6301   | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| HIP6602A  | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| HIP6602A  | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| SC1547    | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| DIMM      | 0     | 0       | 0      | NOTE2     | 0     | 0    | NOTE2   | 0     | 0    |
| AGP       | 0     | 8.0A    | 0      | 0         | 6.0A  | 2.0A | ?       | 1.0A  | 0    |
| Pci       | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| USB       | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| USB HUB   | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| FAN       | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| TTL       | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| AMPLIFIER | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |
| OTHER     | 0     | 0       | 0      | 0         | 0     | 0    | 0       | 0     | 0    |

NOTE1 --- MCH  
 $VCC\_AGP = VCC1\_5 (1.5A) + VCC\_AGP (0.37A)$

NOTE2 --- DIMM  
 $S0 STATE \rightarrow 2.0A * 3 = 6.0A \rightarrow VCC3$   
 $S1/S3 STATE \rightarrow 200mA * 3 = 600mA \rightarrow VCC3\_SB$   
 $VCC3\_SB \rightarrow 600mA * 3.3V/5V = 396mA \rightarrow VCC5\_SB$

NOTE3 --- ICH2

| Power      | S0    | S1    | S3/S4/S5 |
|------------|-------|-------|----------|
| 1.8V       | 300mA | 100mA | N/A      |
| 1.8V_LAN   | 36mA  | 28mA  | N/A      |
| VCC1_8SB   | 45mA  | 30mA  | 7mA      |
| VCC3       | 410mA | 5mA   | N/A      |
| VCC3+562ET | 230mA | 210mA | N/A      |
| VCC3_SB    | 25mA  | 0.6mA | N/A      |

$VCC3\_SB =$   
 $VCC1\_8SB =$   
 $VCC3\_SB = VCC3\_SB + VCC1\_8SB$

## 1.8V/3.3V SEQUENCE CIRCUIT

VCC3

R132 200

R134 470

R123 200

Q21 2N3906S  
Ic=200mA  
Vbeo=5V  
Vceo=40V

Q25 2N3904S

VCC1\_8

## REGULATORS OUTPUT DECOUPLING CAPACITORS

VCC1\_8

CT32  
1000U/6.3V-A  
CB155  
103P  
CB87  
10P

VCC5\_SB

CT20  
470U/16V  
CB8  
104P  
CB33  
105P

VCC\_DIMM

CT4  
1000U/6.3V-A  
CB77  
104P  
CB36  
105P

VCC5\_STR

CT77  
470U/16V  
CB18  
104P  
CB2  
104P  
CB19  
104P

VCC3\_SB

CT41  
1000U/6.3V-A  
CB163  
104P  
CB7  
105P  
CB6  
104P  
CB5  
104P

VCC3

CB91  
104P  
CB63  
105P

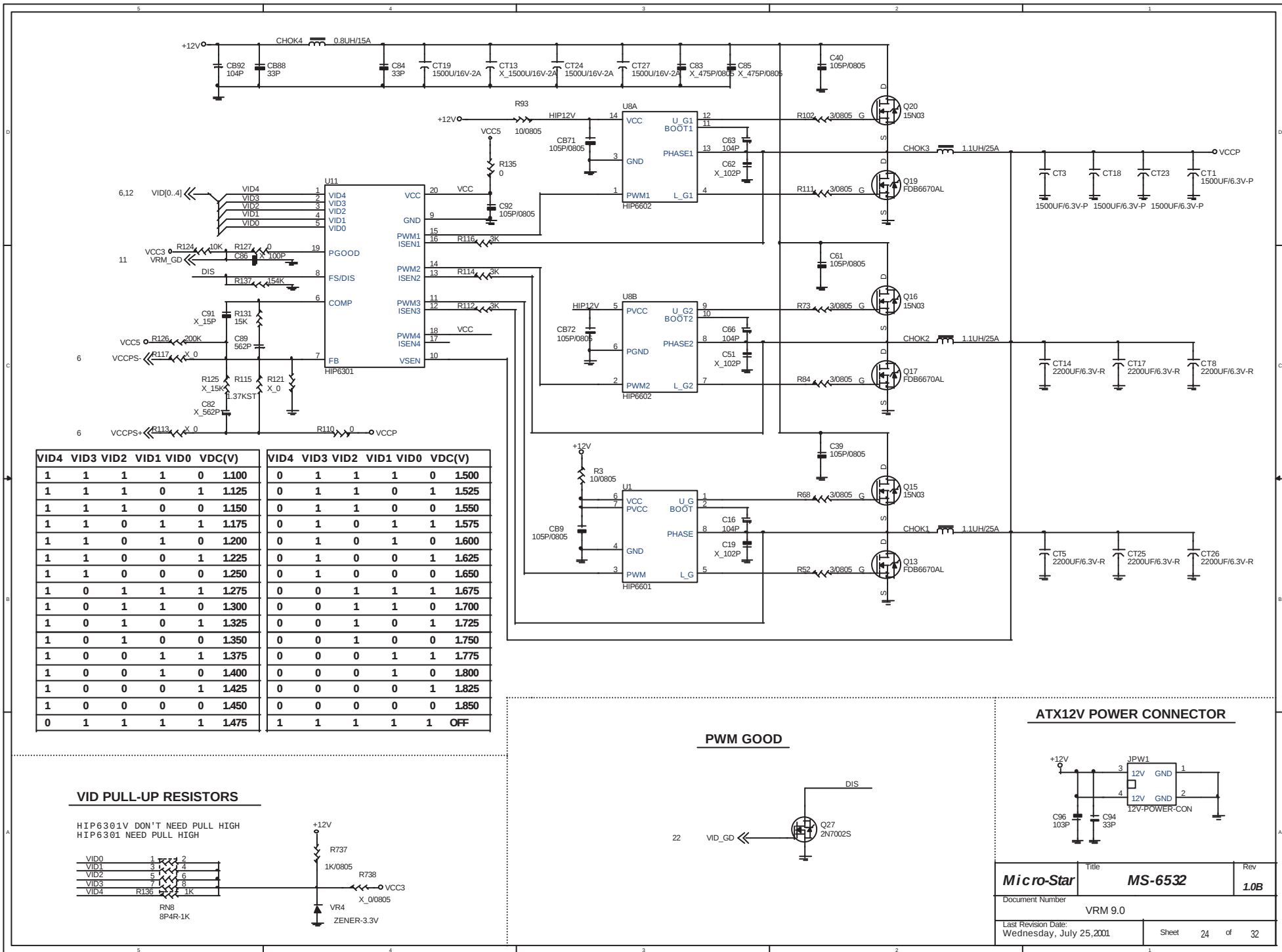
VCC\_AGGP

CT29  
1000U/6.3V-A

VCC5

CB159  
104P

|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| <b>Micro-Star</b>                               | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number<br><b>Voltage Regulator</b>     |                         |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |                         | Sheet 23 of 32     |



Micro-Star

MS-6532

Rev  
1.0B

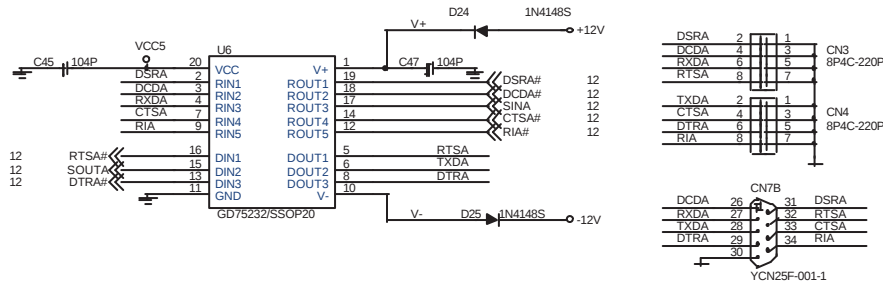
Document Number

VRM 9.0

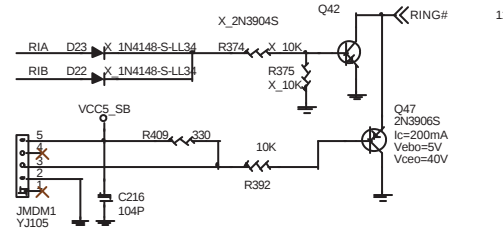
Last Revision Date:  
Wednesday, July 25, 2001

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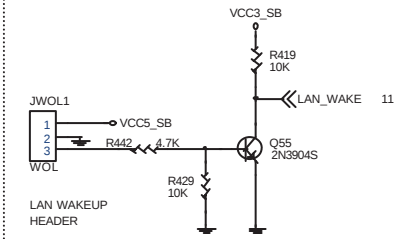
## SERIAL PORT 1



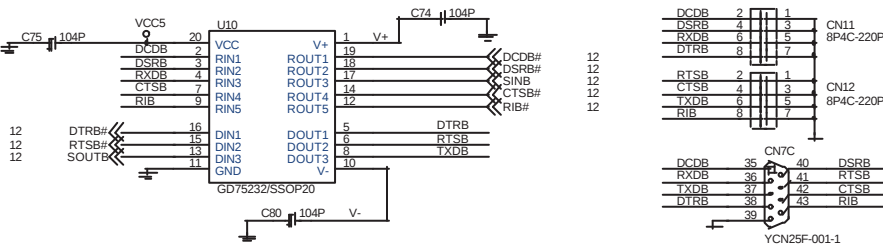
## MODEM RING BLOCK



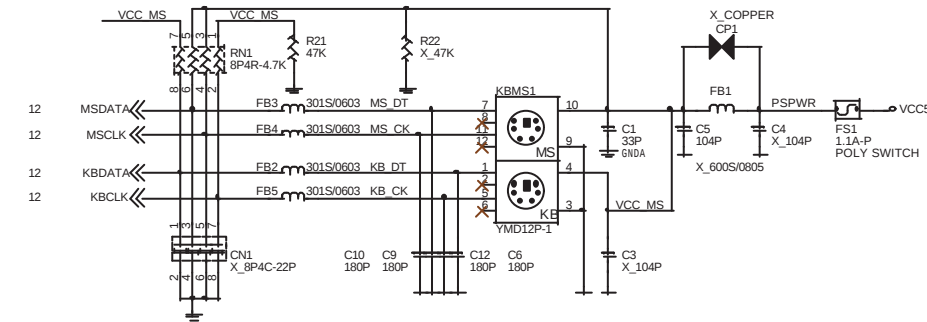
## LAN WAKEUP BLOCK



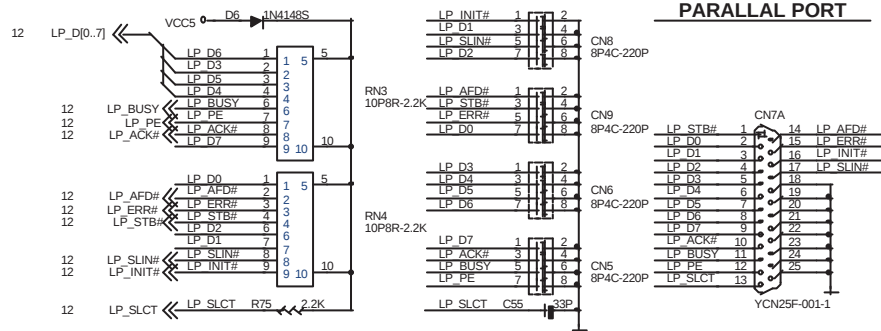
## SERIAL PORT 2



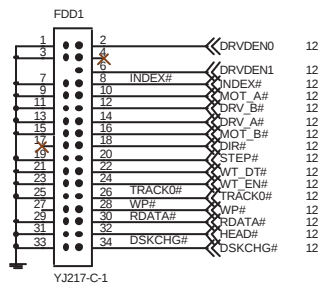
## PS2 KEYBOARD & MOUSE CONNECTOR



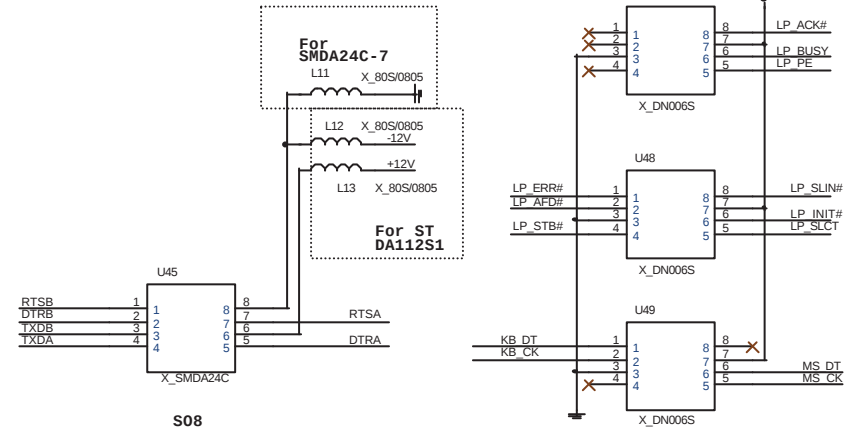
## PARALLAL PORT



## FLOPPY CONNECTOR

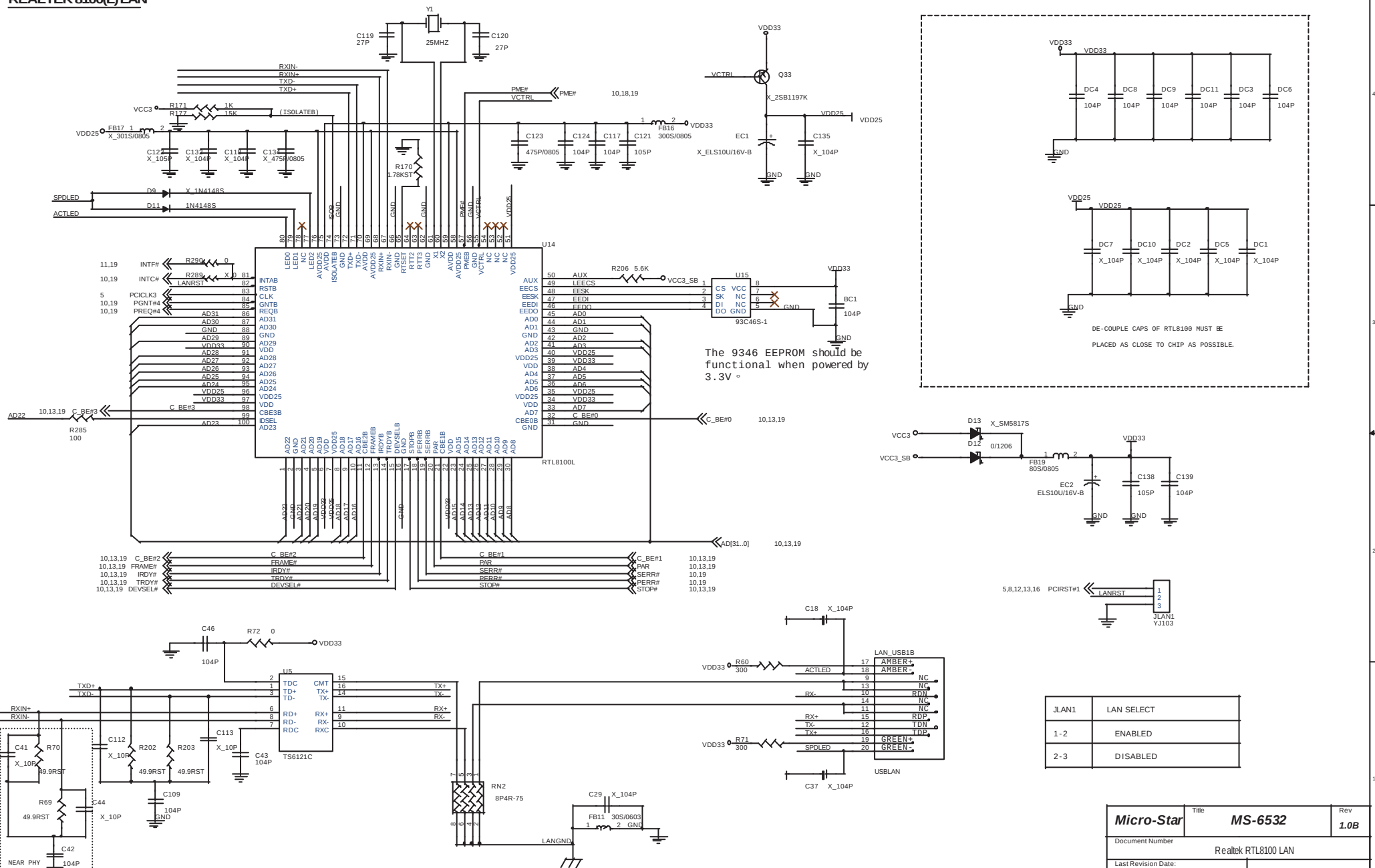


## ESD



|                     |                          |         |     |      |
|---------------------|--------------------------|---------|-----|------|
| Micro-Star          | Title                    | MS-6532 | Rev | 1.0B |
| Document Number     | IO Connector / ESD       |         |     |      |
| Last Revision Date: | Wednesday, July 25, 2001 |         |     |      |
| Sheet               | 25                       | of      | 32  |      |

REALTEK 8100(L) LAN

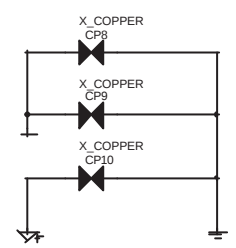
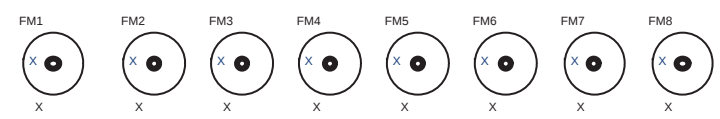
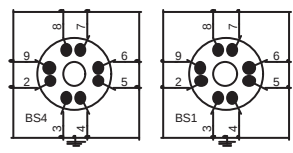
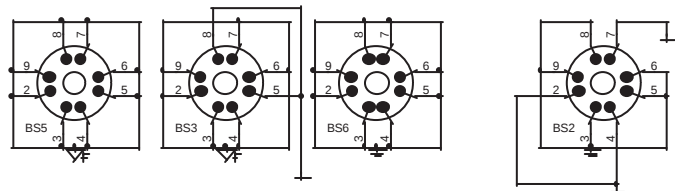


|                                                        |                         |                              |
|--------------------------------------------------------|-------------------------|------------------------------|
| <b>Micro-Star</b>                                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b>           |
| Document Number<br><b>Realtek RTL8100 LAN</b>          |                         |                              |
| Last Revision Date:<br><b>Wednesday, July 25, 2001</b> |                         | Sheet <b>26</b> of <b>32</b> |

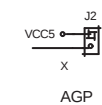
# Jumper Setting

| Jumper  | Description                   |
|---------|-------------------------------|
| JBAT1   | CLEAR CMOS                    |
| 1-2     | NORMAL (Default)              |
| 2-3     | CLEAR CMOS                    |
| IR1     | IR HEADER                     |
| CD_IN1  | CDROM HEADER (ATAPI)          |
| MDM_IN1 | TELEPHONY HEADER (ATAPI)      |
| JP1     | CNR RISER CODEC SELECT HEADER |
| 1-2     | AUTO MODE (Default)           |
| 2-3     | PRIMARY AUDIO CODEC ONBOARD   |

# PCB OTHER COMPONENT



# SIMULATION TRACE



|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| <b>Micro-Star</b>                               | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                 | MANUAL                  |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 | Sheet 28 of 32          |                    |

Pentium 4 Processor /Northwood mPGA 478

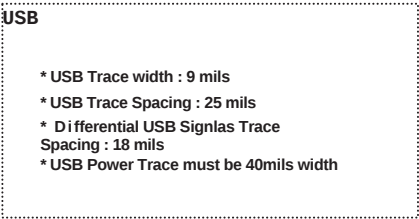
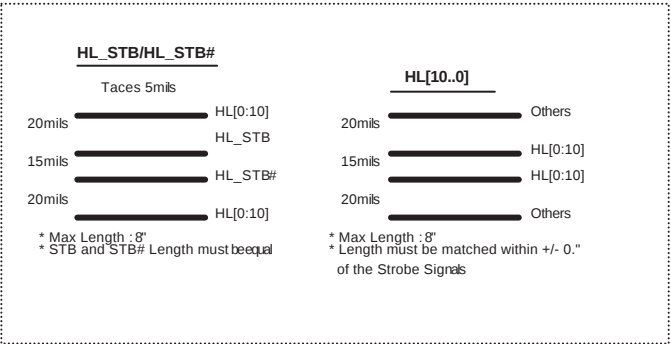
Source Synchronous Signal Group and the Associated Strobes

| Signals           | Associated Strobe |
|-------------------|-------------------|
| REQ[4:0],A[16:3]# | ADSTB0#           |
| A[31:17]#         | ADSTB1#           |
| D[15:0]#,DBI0#    | DSTBP0#,DSTBN0#   |
| D[31:16]#,DBI1#   | DSTBP1#,DSTBN1#   |
| D[47:32]#,DBI2#   | DSTBP2#,DSTBN2#   |
| D[63:48]#,DBI3#   | DSTBP3#,DSTBN3#   |

| Signals | Length        | Inaccuracy  |
|---------|---------------|-------------|
| Data    | 2.0" to 10.0" | +/- 100 mil |
| Address | 2.0" to 10.0" | +/- 200 mil |
| Strobe  | 2.0" to 10.0" | +/- 25 mil  |
| Clock   | 2.0" to 10.0" | Don't need  |

\* Delta=(CPU\_pkglen.net-CPUpkglen.strobe)+(CS\_pkglen.net-CS\_pkglen.strobe)  
Trace : 7 mil width 13mil space

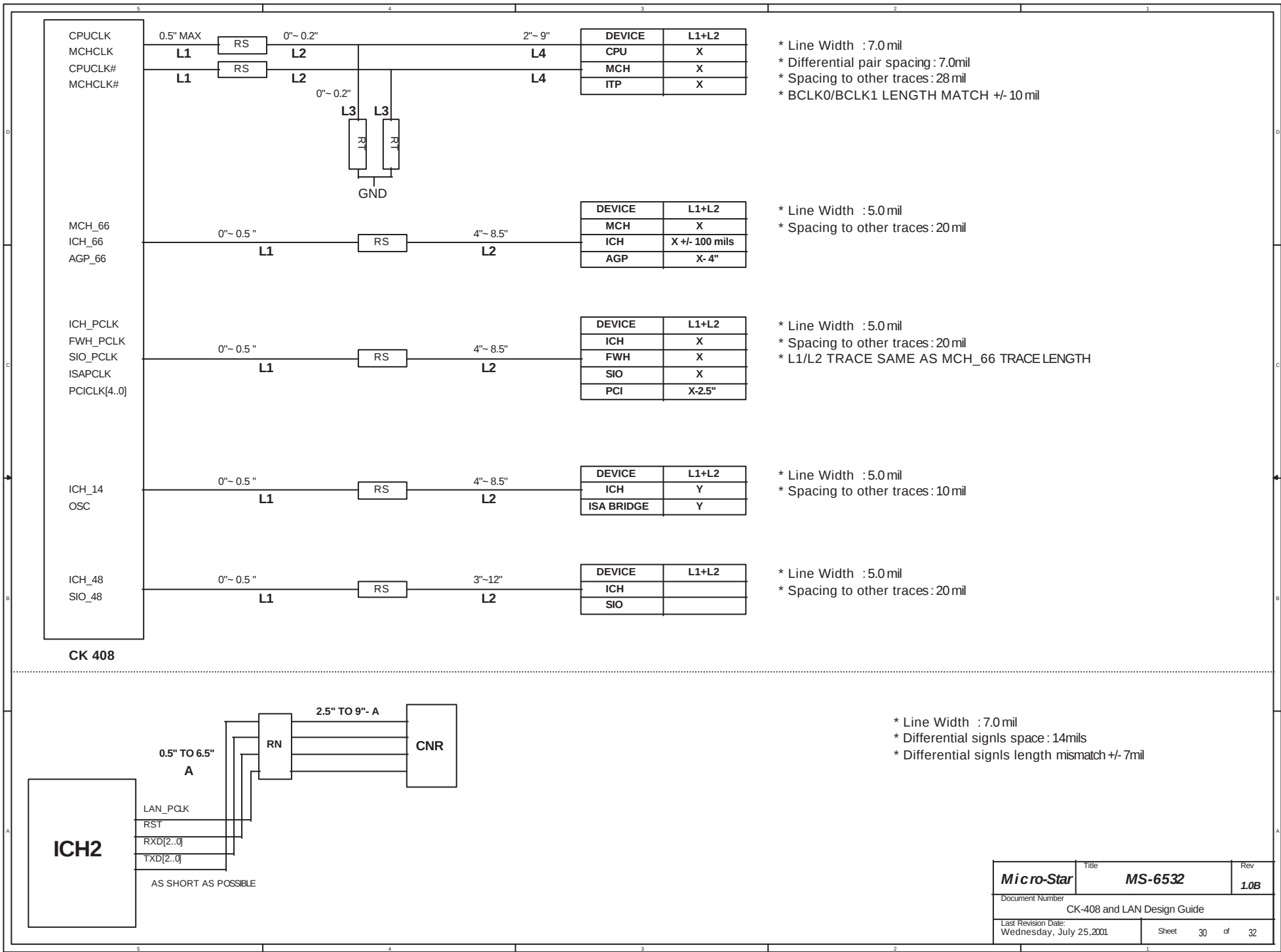
Miscellaneous Signals

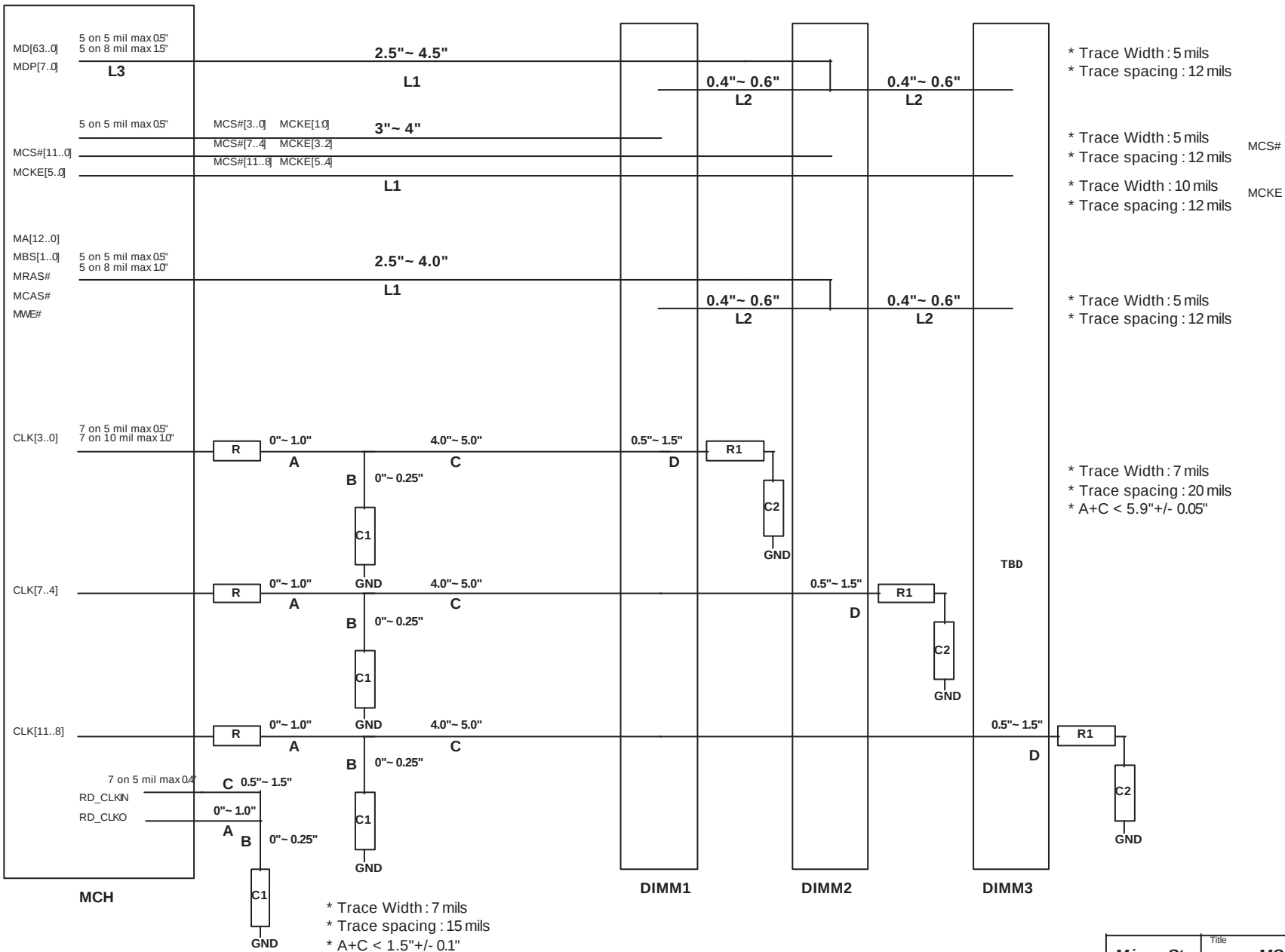


AGP

| 1X Timing group                                                                                                            | 2X/4X Timing group                                                                                                                                                               | SIGNALS                                                                                                                                                                                 | Maximum Length                                    | Width                                                       | Space                                                             | Dismatch Length                                                                    | Relative to                                                                                                                                     |
|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------|------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| AGPCLK<br>PIPE#<br>RBF#<br>WBF#<br>ST[2..0]<br>GFRAME#<br>GIRDY#<br>GTRDY#<br>GSTOP#<br>GDEVSEL#<br>GREQ#<br>GGNT#<br>GPAR | SET#1<br>GAD[15..0]<br>GC_BE#[1..0]<br>GAD_STB0<br>GAD_STB0#<br><br>SET#2<br>GAD[31..16]<br>GC_BE#[3..2]<br>GAD_STB1<br>GAD_STB1#<br><br>SET#3<br>SBA[7..0]<br>SB_STB<br>SB_STB# | 1X Timing group<br>2X/4X Timing group SET#1<br>2X/4X Timing group SET#2<br>2X/4X Timing group SET#3<br>2X/4X Timing group SET#1<br>2X/4X Timing group SET#2<br>2X/4X Timing group SET#3 | 7.5"<br>7.25"<br>7.25"<br>7.25"<br>6"<br>6"<br>6" | 5 mil<br>5 mil<br>5 mil<br>5 mil<br>5 mil<br>5 mil<br>5 mil | 5 mil<br>20 mil<br>20 mil<br>20 mil<br>15 mil<br>15 mil<br>15 mil | X<br>+/- 0.125"<br>+/- 0.125"<br>+/- 0.125"<br>+/- 0.25"<br>+/- 0.25"<br>+/- 0.25" | X<br>GAD_STB0<br>GAD_STB0#<br>GAD_STB1<br>GAD_STB1#<br>SB_STB<br>SB_STB#<br>GAD_STB0<br>GAD_STB0#<br>GAD_STB1<br>GAD_STB1#<br>SB_STB<br>SB_STB# |

|                                                |                         |                    |
|------------------------------------------------|-------------------------|--------------------|
| <b>Micro-Star</b>                              | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number                                | Revision History - 1    |                    |
| Last Revision Date:<br>Wednesday, July 25,2001 | Sheet<br>29             | of<br>32           |





\* Trace Width : 5 mils  
\* Trace spacing : 12 mils

\* Trace Width : 5 mils  
\* Trace spacing : 12 mils

\* Trace Width : 10 mils  
\* Trace spacing : 12 mils

\* Trace Width : 5 mils  
\* Trace spacing : 12 mils

\* Trace Width : 7 mils  
\* Trace spacing : 20 mils  
\* A+C < 5.9" +/- 0.05"

|                                                 |                  |                |
|-------------------------------------------------|------------------|----------------|
| Micro-Star                                      | Title<br>MS-6532 | Rev<br>1.0B    |
| Document Number<br>PC133 DIMM DG                |                  |                |
| Last Revision Date:<br>Wednesday, July 25, 2001 |                  | Sheet 31 of 32 |

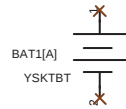
|                  |
|------------------|
| JBAT1 Clear CMOS |
| 1 - 2 Normal *   |
| 2 - 3 Clear CMOS |



#### LEGEND AUDIO



#### BAT SOCKET



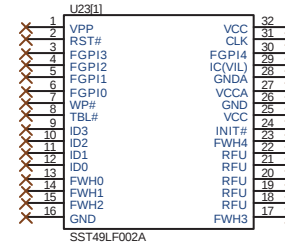
|                |
|----------------|
| JP2 HW AUDIO   |
| 1 - 2 DISABLE  |
| 2 - 3 ENABLE * |



|                |            |
|----------------|------------|
| J7 BIOS Update |            |
| SHORT          | Locked     |
| OPEN           | Unlocked * |



#### BIOS



#### FRONT PANNEL BUZZER



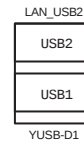
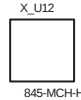
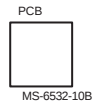
|     |                              |
|-----|------------------------------|
| JP3 | AUDIO DOWN                   |
| 1-2 | Auto mode                    |
| 2-3 | Disabled onboard audio codec |



|       |            |
|-------|------------|
| JLAN1 | LAN SELECT |
| 1-2   | ENABLED    |
| 2-3   | DISABLED   |



#### MS6532 PCB



**STD BOM:AD1881A**  
**OPTA BOM:CMI8738-LX**  
**T4 BOM:WITHOUT LAN,WITHOUT H/W AUDIO**

|                                                 |                         |                    |
|-------------------------------------------------|-------------------------|--------------------|
| <b>M i c r o - S t a r</b>                      | Title<br><b>MS-6532</b> | Rev<br><b>1.0B</b> |
| Document Number<br><b>PACKING BOM</b>           |                         |                    |
| Last Revision Date:<br>Wednesday, July 25, 2001 |                         | Sheet 32 of 32     |