

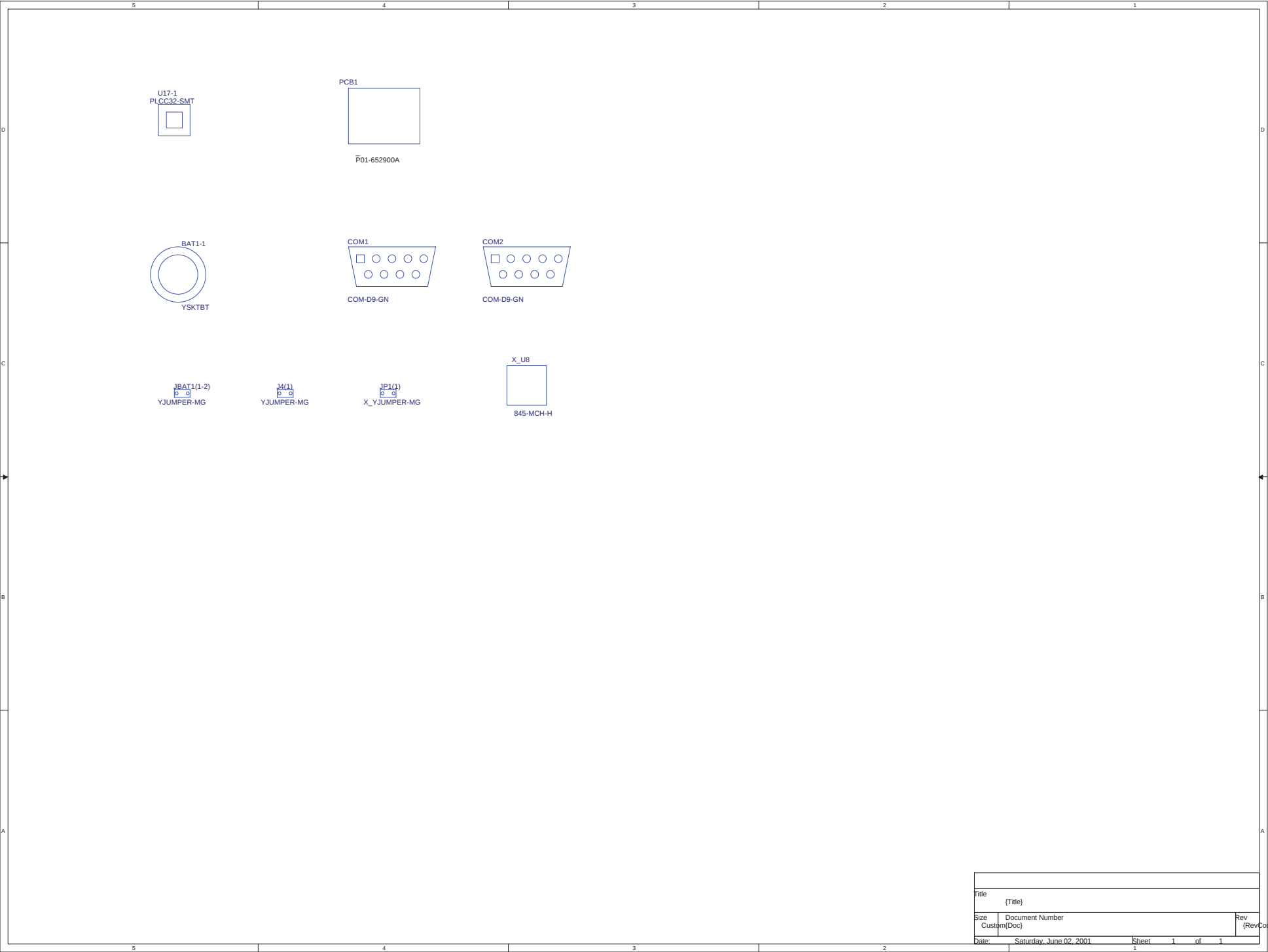
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MS-6529

INTEL (R) Brookdale Chipset
Willamette/Northwood 423pin mPGA-B Processor Schematics

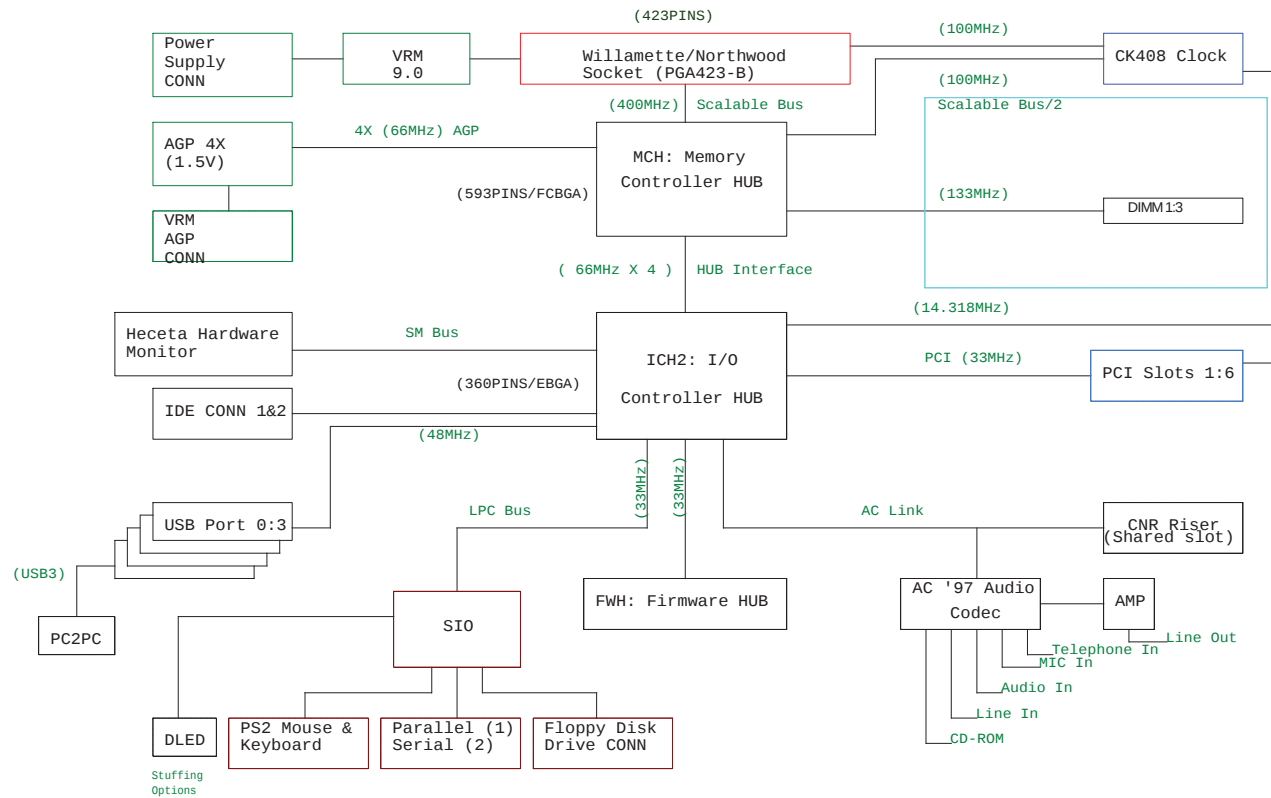
Version 0A

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Title			
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AGP
4X(1.5V)
AGP CONN



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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect (PREQ#5)
GPIO 2	I	INTE#
GPIO 3	I	INTF#
GPIO 4	I	INTG#
GPIO 5	I	INTH#
GPIO 6	I	CNR Detect
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	PGNT#5
GPIO 18	O	Not Implemented
GPIO 19	O	SDR Votlage settig
GPIO 20	O	SDR Votlage settig
GPIO 21	O	CPU VID Control
GPIO 22	OD	Non Connect
GPIO 23	O	BIOS Locked/Unlocked
GPIO 24	O	STR Control
GPIO 25	O	Non Connect
GPIO 26	O	Non Connect
GPIO 27	I/O	Non Connect
GPIO 28	I/O	Non Connect
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

W627HF -AW

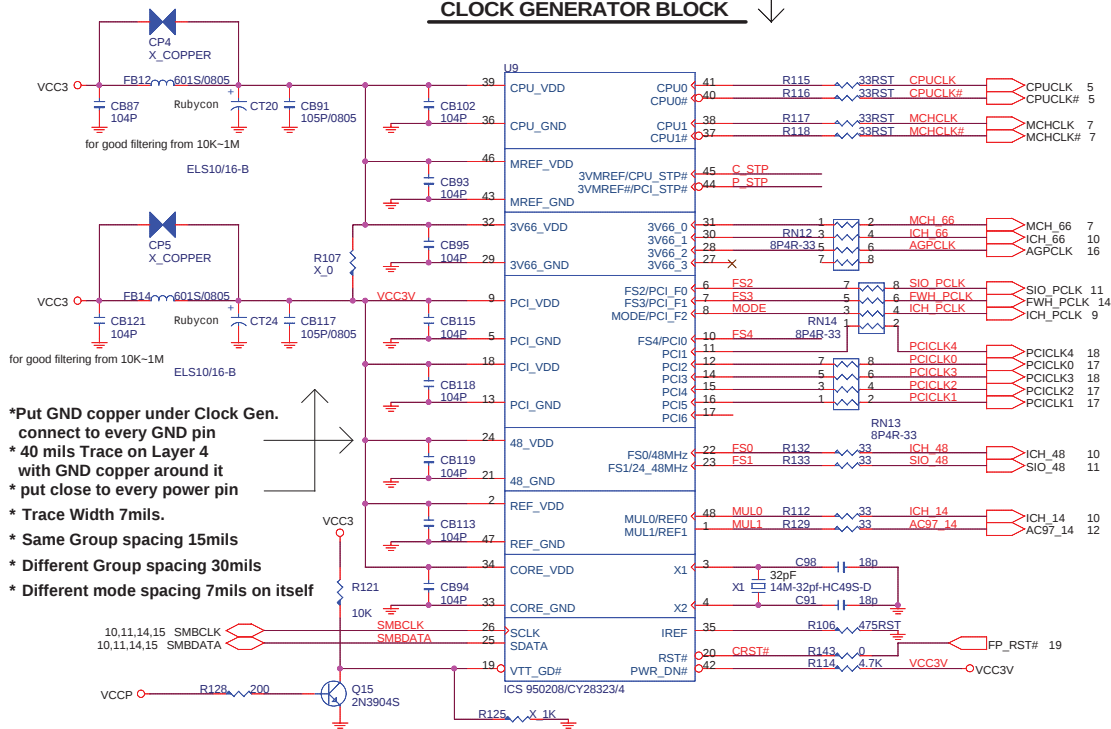
PIN NAME	Function define
GP23/PLED	PLED(POWER LED)
GP24/WDT0	DLED2
GP32/PWR0K	DLED1
GP33/RSMRST#	DLED4
GP34/CIRRX	DLED3
GP35/SUSLED	SUSLED

PCI

DEVICES	INT#	IDSEL	REQ#/GNT#	CLOCK
PCI SLOT 1	INT#A INT#B INT#C INT#D	AD16	PREQ#0 PGNT#0	PCICLK0
PCI SLOT 2	INT#B INT#C INT#D INT#A	AD17	PREQ#1 PGNT#1	PCICLK1
PCI SLOT 3	INT#C INT#D INT#A INT#B	AD18	PREQ#2 PGNT#2	PCICLK2
PCI SLOT 4	INT#D INT#A INT#B INT#C	AD19	PREQ#3 PGNT#3	PCICLK3
PCI SLOT 5	INT#B INT#C INT#D INT#A	AD21	PREQ#4 PGNT#4	PCICLK4

CLOCK GENERATOR BLOCK

*Trace less 0.5"



- *Put GND copper under Clock Gen. connect to every GND pin
- * 40 mils Trace on Layer 4 with GND copper around it put close to every power pin
- * Trace Width 7mils.
- * Same Group spacing 15mils
- * Different Group spacing 30mils
- * Different mode spacing 7mils on itself

Shut Source Termination Resistors

CPUCLK R104 49.9RST
CPUCLK# R105 49.9RST
MCHCLK R108 49.9RST
MCHCLK# R109 49.9RST

Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS

FS4 R136 10K VCC3V
FS3 R150 10K VCC3V
FS1 R145 10K VCC3V
FS0 R144 10K VCC3V
FS2 R142 10K VCC3V
MODE R151 10K
MUL0 R102 10K VCC3V
MUL1 R141 10K VCC3V
CRST# R135 10K VCC3V
SMBCLK R120 4.7K VCC3V
SMBDATA R119 4.7K VCC3V
C_STP R113 1K VCC3V
P_STP R103 1K VCC3V

Pull-Down Capacitors

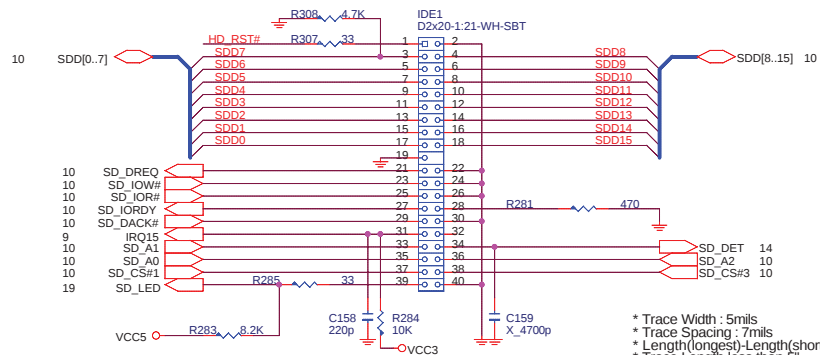
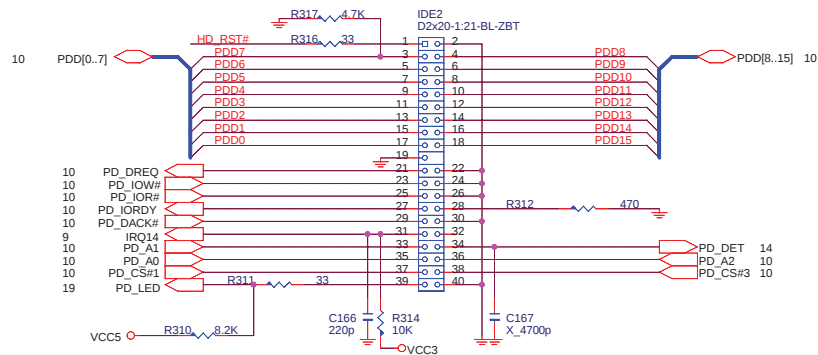
MCH_66 CN12 8P4C-10P
ICH_66
AGPCLK
SIO_PCLK CN15 8P4C-10P
FWH_PCLK
ICH_PCLK
PCICLK4
PCICLK0 CN16 8P4C-10P
PCICLK3
PCICLK2
PCICLK1
ICH_48 C100 10P
SIO_48 C101 10P
ICH_14 C80 10P

used only for EMI issue
Trace less 0.2"

PRIMARY IDE BLOCK

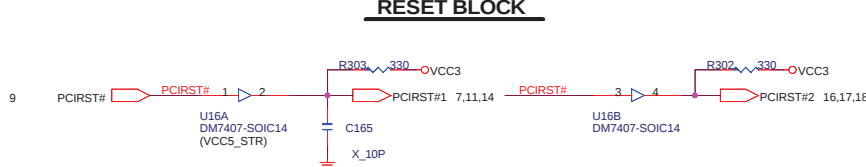
ATA100 IDE CONNECTORS

SECONDARY IDE BLOCK

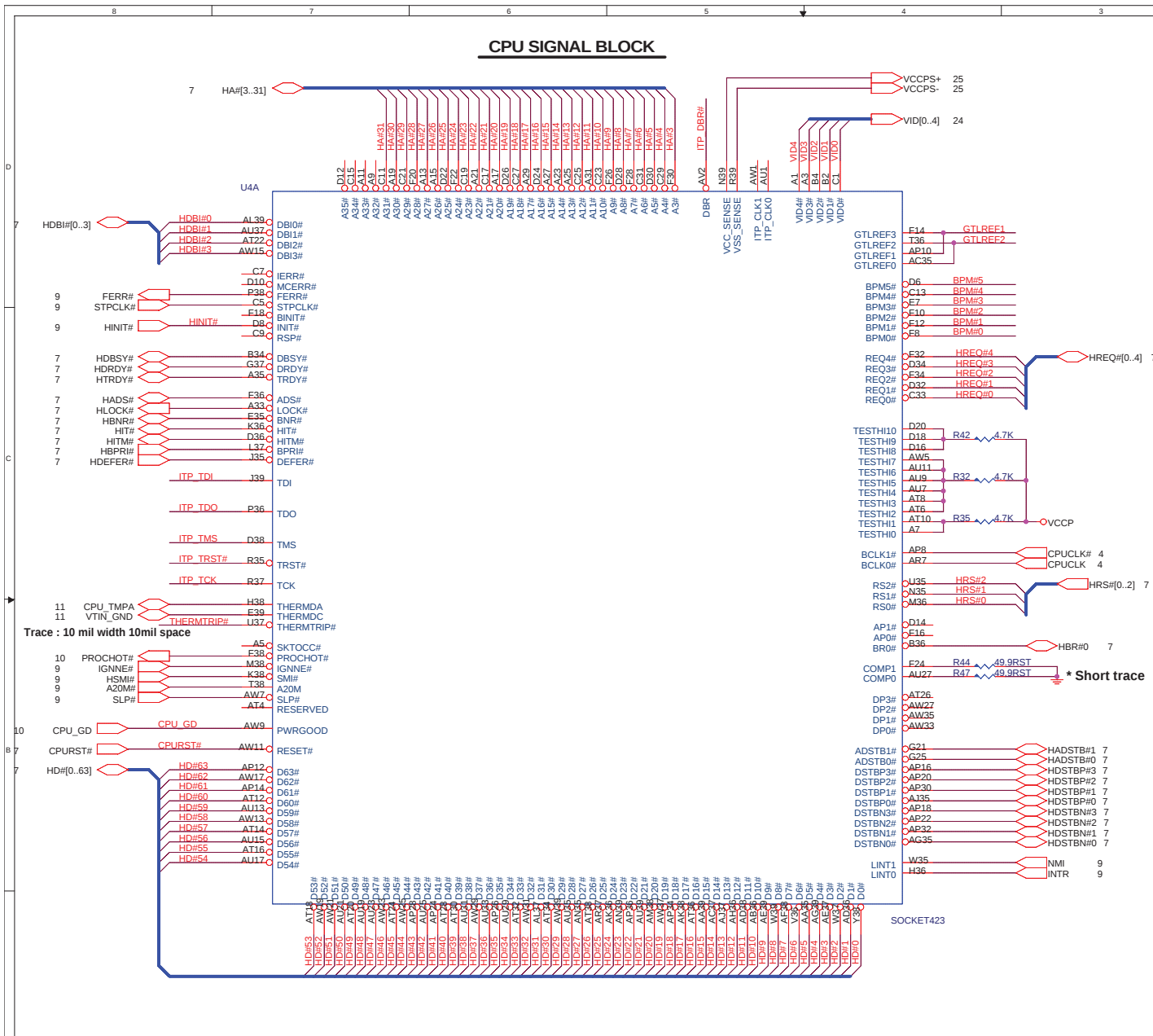


- * Trace Width : 5mils
- * Trace Spacing : 7mils
- * Length(longest)-Length(shortest)<0.5"
- * Trace Length less than 5"

RESET BLOCK



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CPU STRAPPING RESISTORS

Left side components:

- RPM#5 R30 33RST
- BPM#4 R38 33RST
- RPM#3 R29 33RST
- RPM#2 R36 33RST
- RPM#1 R39 33RST
- BPM#0 R37 33RST

Middle side components:

- ITP_TDI R54 150
- ITP_TRST R55 150

Right side components:

- PROCHOT# R306 62
- CPU_GD R25 300
- HBR#0 R46 49RST
- CPU_RST# R28 49RST
- THERMTRIP# R52 X 62
- HINIT# R21 300

PROCHOT#	R306	62	VCCP
CPU_GD	R25	300	
HBR#0	R46	49.9RST	
CPURST#	R28	49.9RST	
THERMTRIP#	R52	X 62	
HINIT#	R21	300	

CPU GTL REFERENCE VOLTAGE BLOCK

The diagram shows two identical circuit blocks for GTL REFERENCE VOLTAGE. Each block consists of a signal line (GTLREF1 or GTLREF2) connected to a voltage divider. The divider is formed by a resistor (R41 or R49) connected to VCCP and another resistor (R40 or R50) connected to ground. The tap point is labeled $2/3 \cdot V_{ccp}$. Three capacitors (C28, C31, C32 for GTLREF1; C41, C40, C39 for GTLREF2) are connected in parallel to ground from the signal line. The capacitors are specified as 220pF and 105P/0805.

Every pin put one 220pF cap near it.

Trace Width 15mils, Space 15mils.

Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP

The diagram shows four signal lines for CPU ITP. Each line is connected to VCCP through a resistor (R17, R48, R56, R53) and to ground through a resistor (150, 39, 75RST, 27). The signal lines are labeled ITP_DBR#, ITP_TMS, ITP_TDO, and ITP_TCK.

The diagram shows two capacitors (CB39, CB30) connected in parallel to ground from a VCCP line. The capacitors are specified as 104P.

ALL COMPONENTS CLOSE TO CPU

CPU ITP



The diagram shows four horizontal lines representing the CPU ITP connections. Each line has a label on the left, a pin number in the middle, and a connection point on the right. The lines are color-coded: the first is red, the second is blue, the third is green, and the fourth is red. The connection points are labeled VCCP, VCCP, VCCP, and GND respectively.

Signal	Pin	Connection
ITP_DBR#	R17	VCCP
ITP_TMS	R48	VCCP
ITP_TDO	R56	VCCP
ITP_TCK	R53	GND

ITP_DBR# R17 150 VCCP

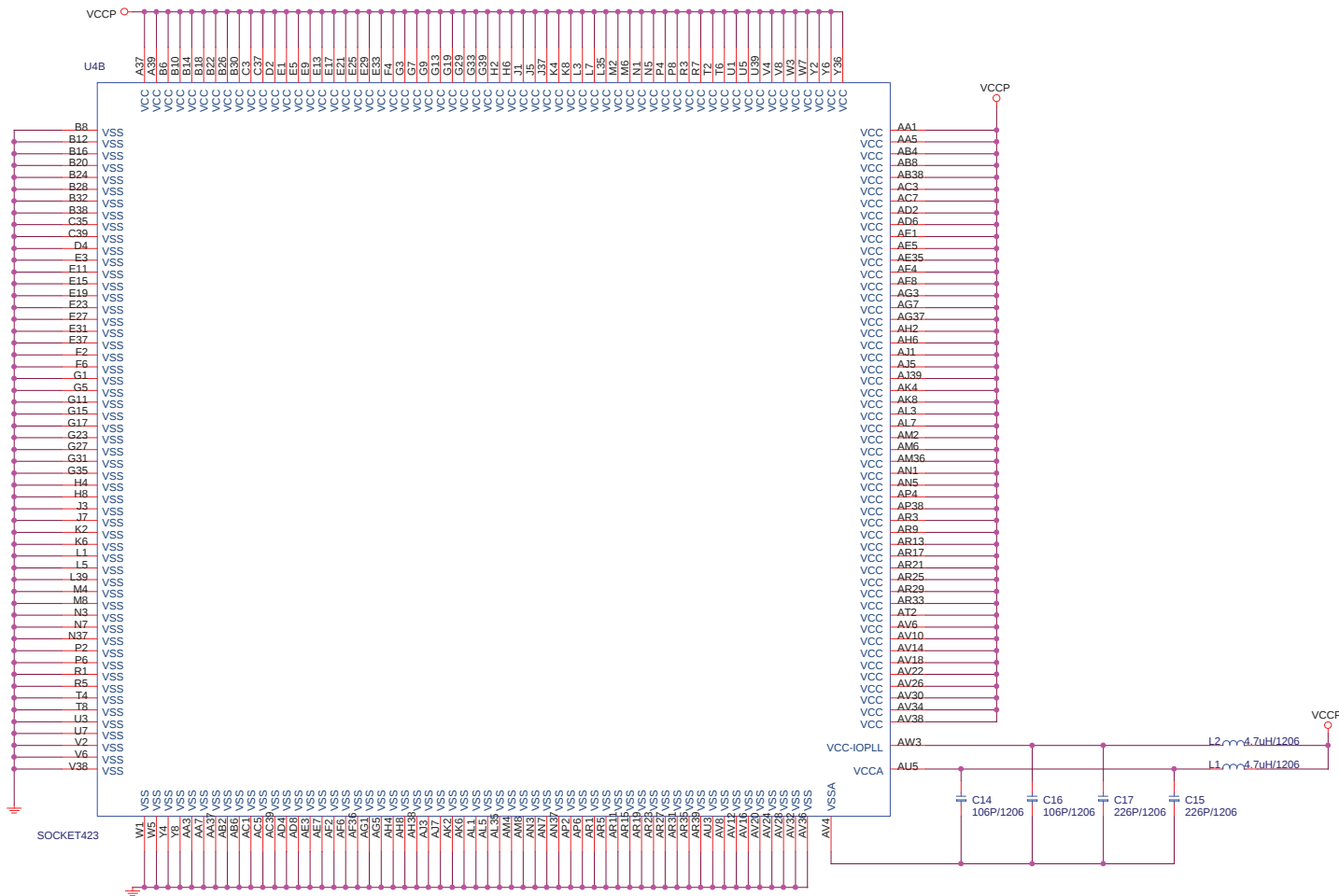
ITP_TMS R48 39 VCCP

ITP_TDO R56 75RST VCCP

ITP_TCK R53 27

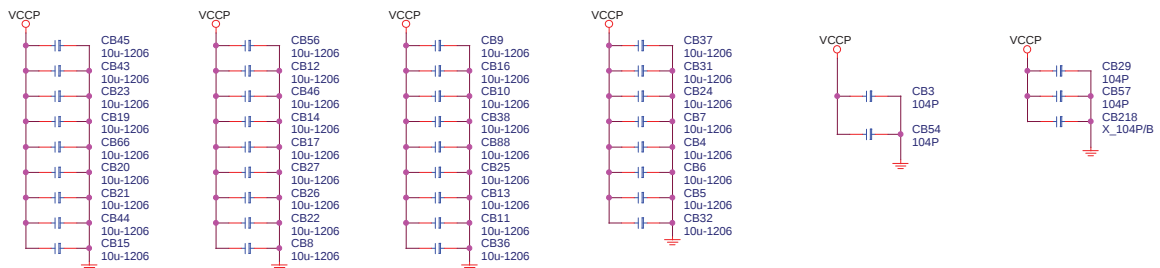
ALL COMPONENTS CLOSE TO CPU

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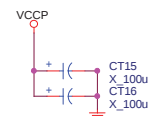


CPU DECOUPLING CAPACITOR

PLACE CAPS WITHIN CPU CAVITY

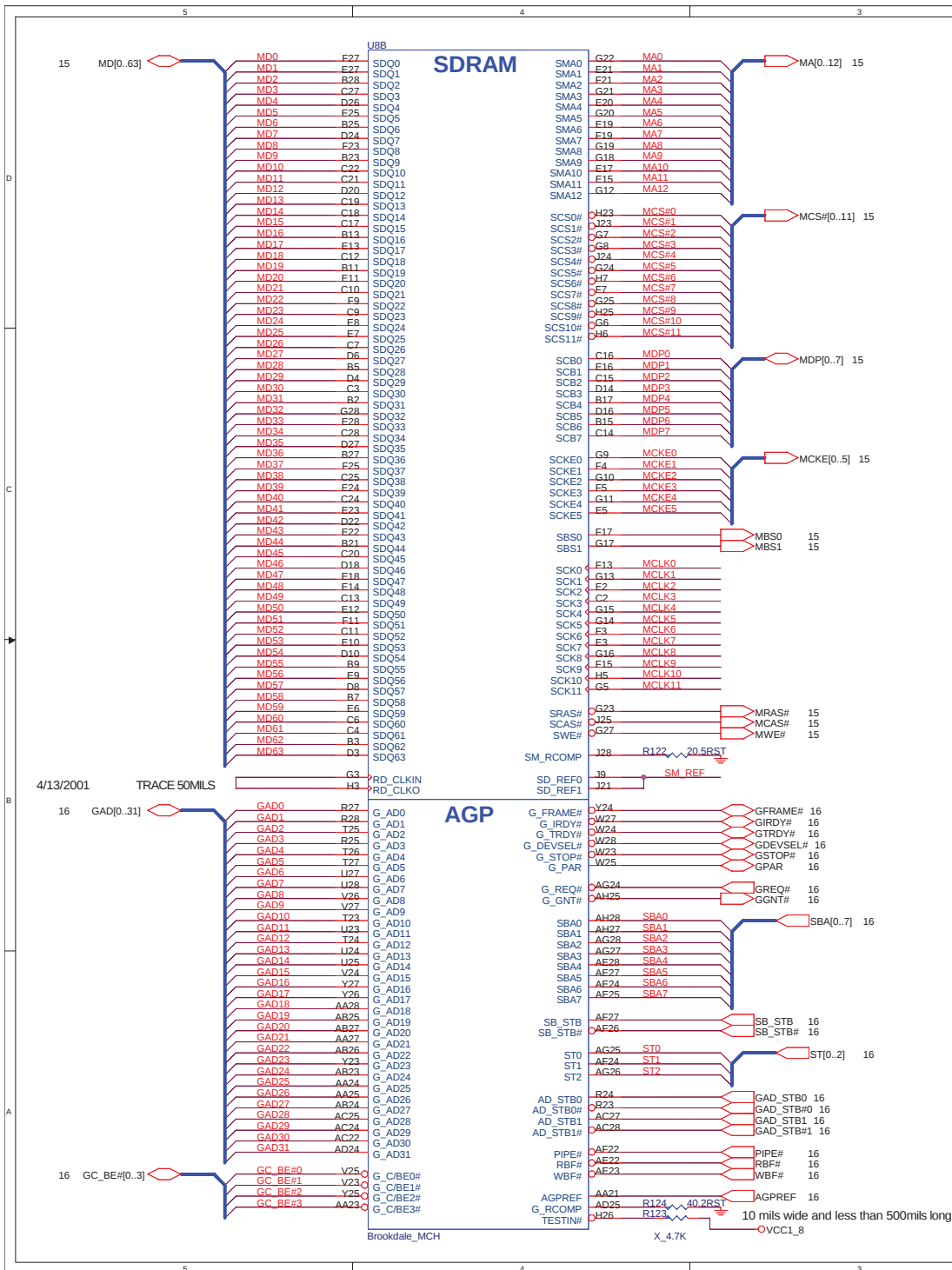


CPU DECOUPLING CAPACITORS

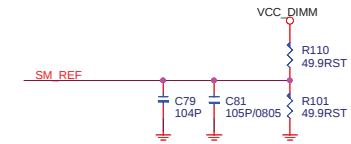


PLACE CAPS WITHIN CPU CAVITY SOLDER

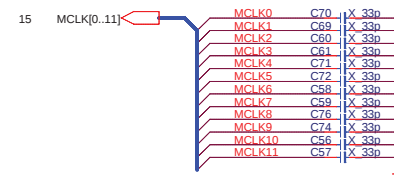
Micro-Star	Title MS-6529	Rev 0A
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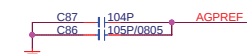
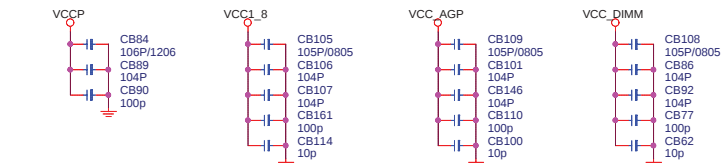
MCH REFERENCE VOLTAGE



MCH MEMORY CLOCK RC CIRCUITS

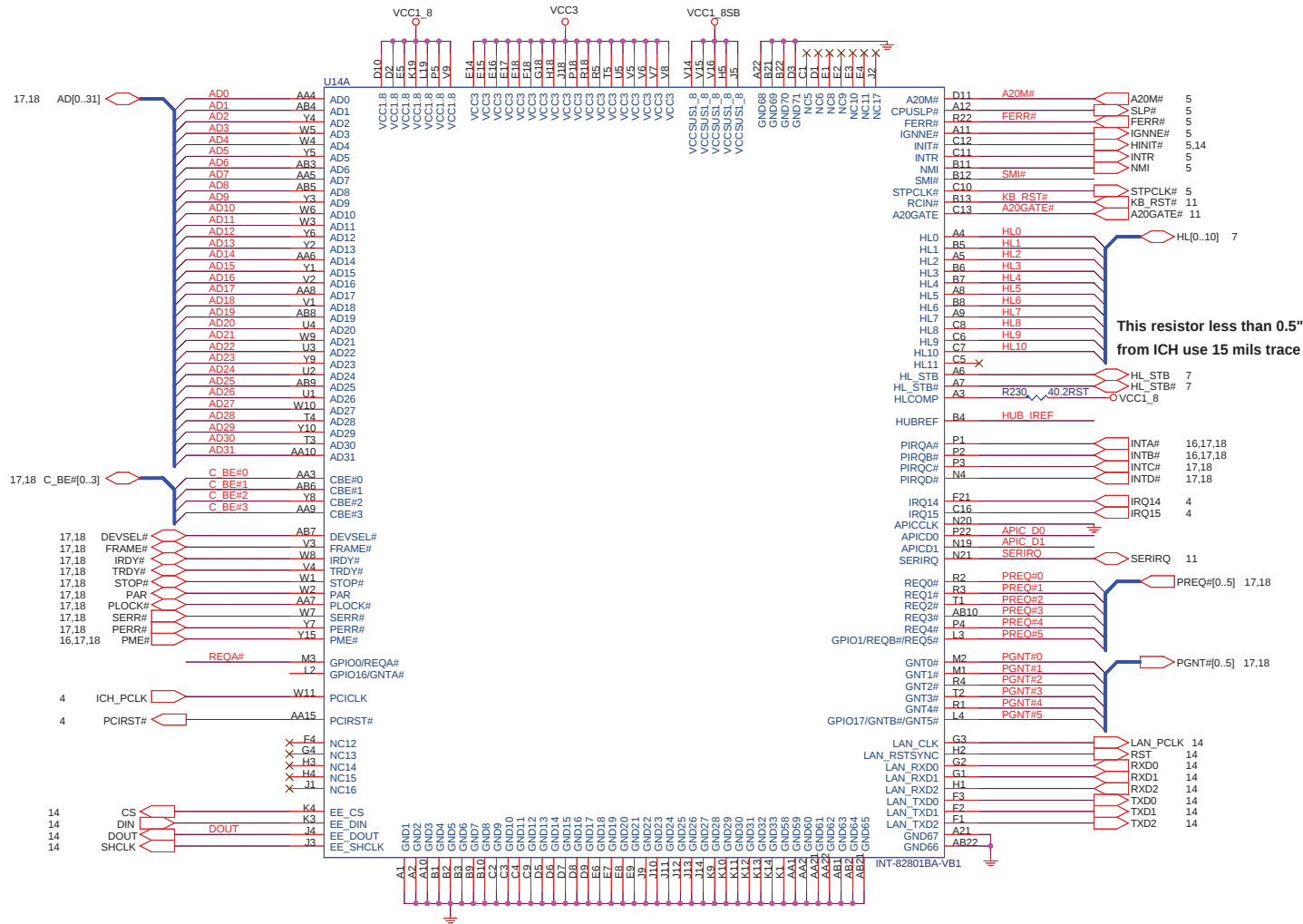


MCH DECOUPLING CAPACITOR

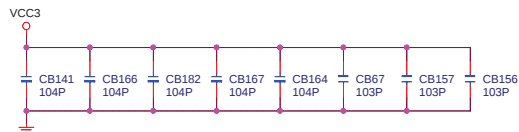


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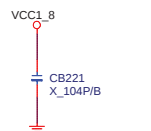
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



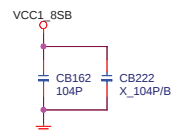
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit

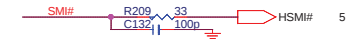


Distribute near the 1.8V power pin of the ICH2

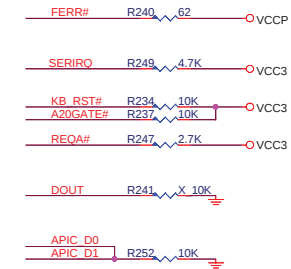


Distribute near the VCC1_8SB Power pin of the ICH2

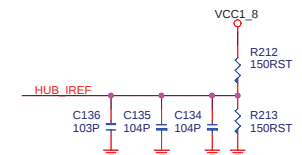
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS



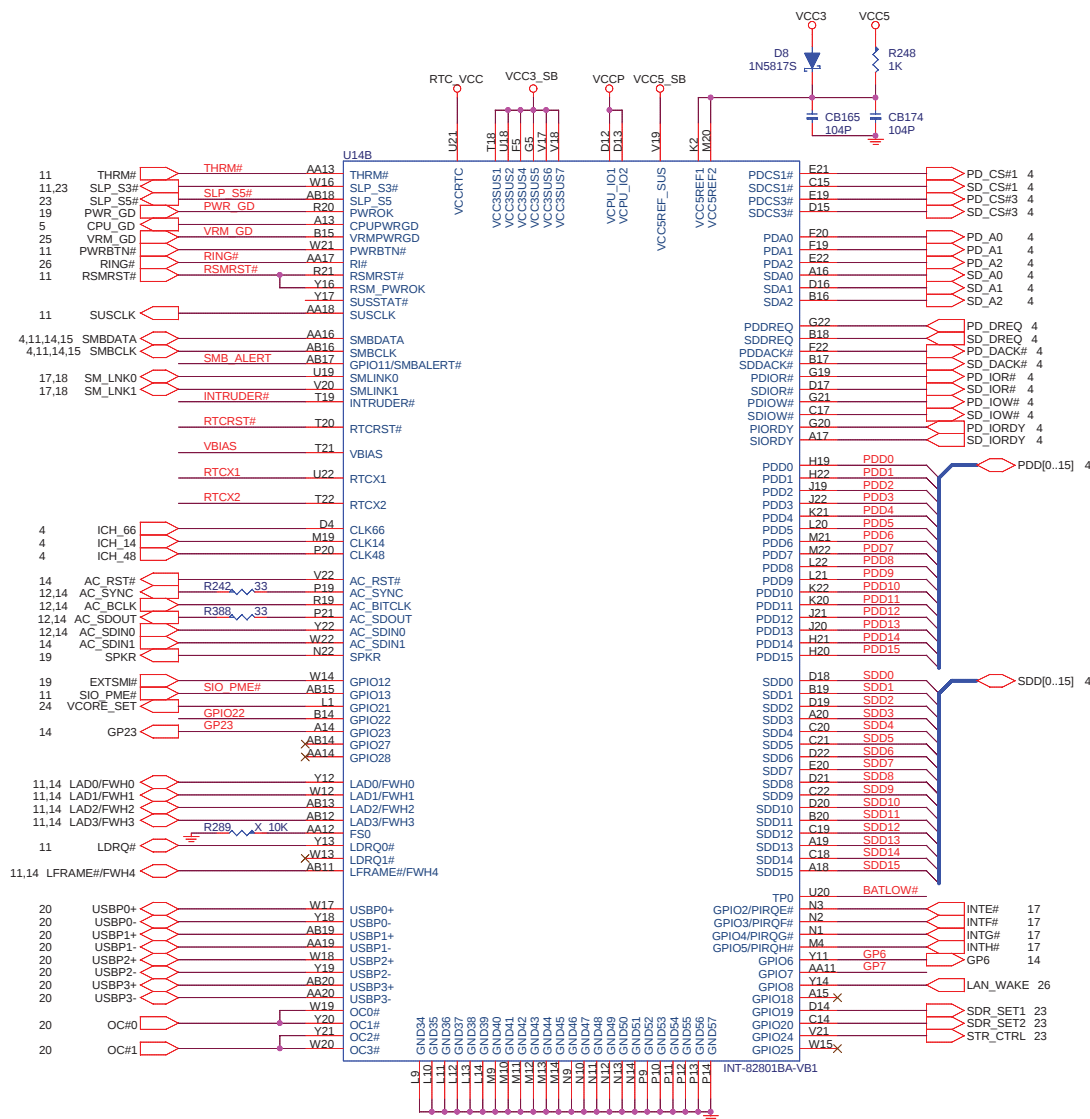
ICH2 REFERENCE VOLTAGE



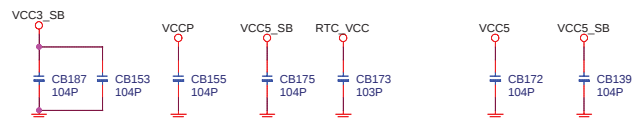
Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

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ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

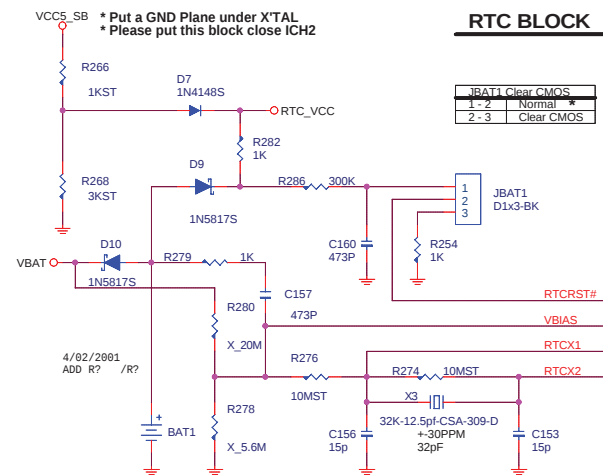


ICH2 DECOUPLING CAPACITOR

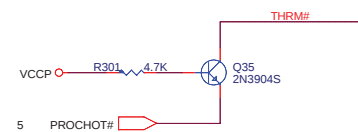


Distribute near the VCC3_SB power pin of the ICH

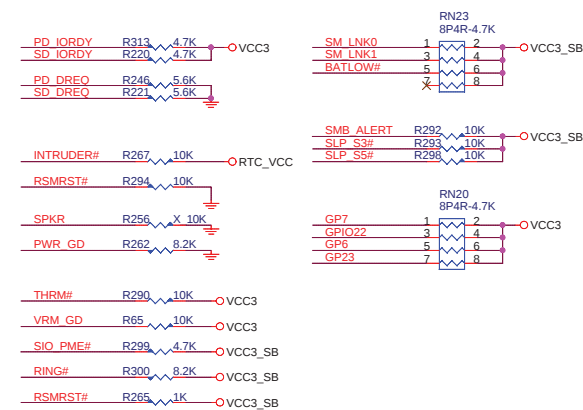
RTC BLOCK



PROCHOT BLOCK

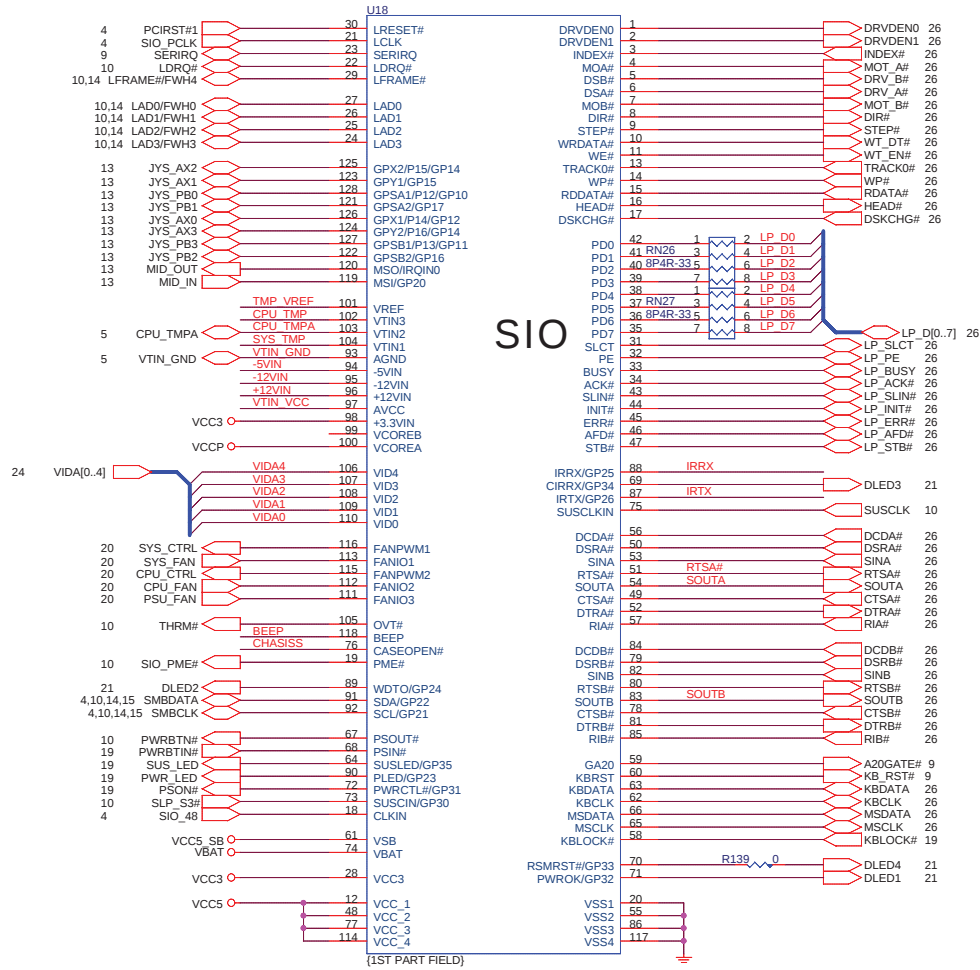


ICH2 STRAPPING RESISTORS



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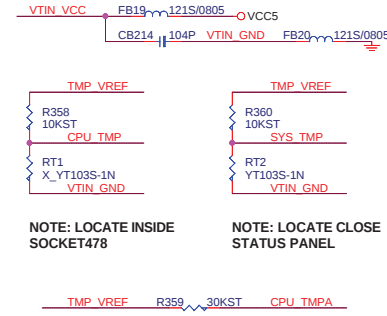
LPC SUPER I/O W83627HF



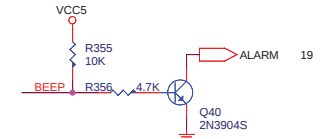
SIO

(1ST PART FIELD)

THERMAL RESISTOR BLOCK



SPEAKER BLOCK

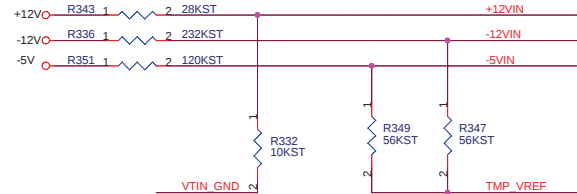
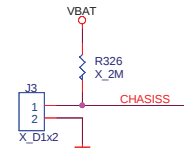


SUPER I/O STRAPPING RESISTOR



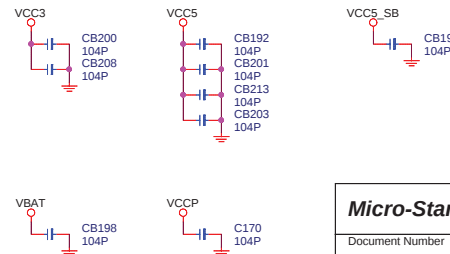
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

CHASSIS INTRUSION HEADER



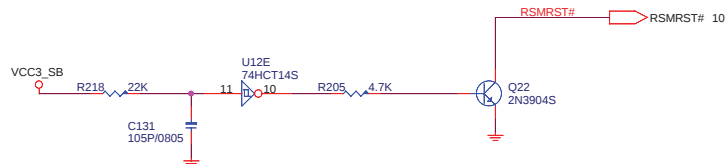
3/16/2001

DECOUPLING CAPACITOR

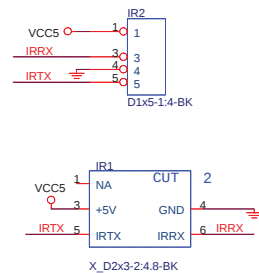


Micro-Star	Title	MS-6529	Rev	0A
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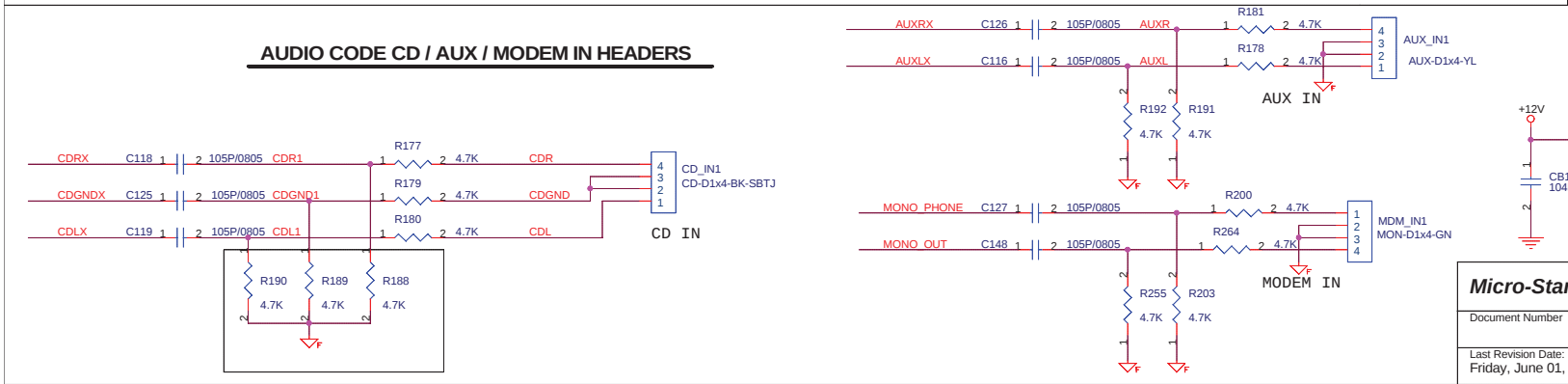
RESUME RESET CIRCUIT BLOCK



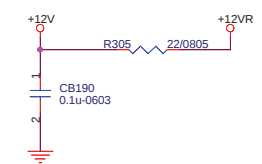
IR HEADER



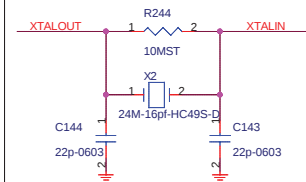
ALC201 AC97 CODEC



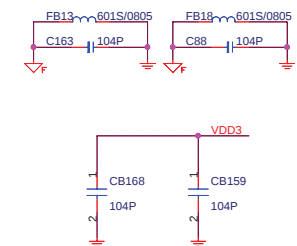
AUDIO CODE REGULATORS



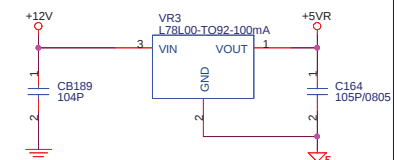
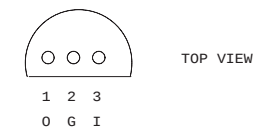
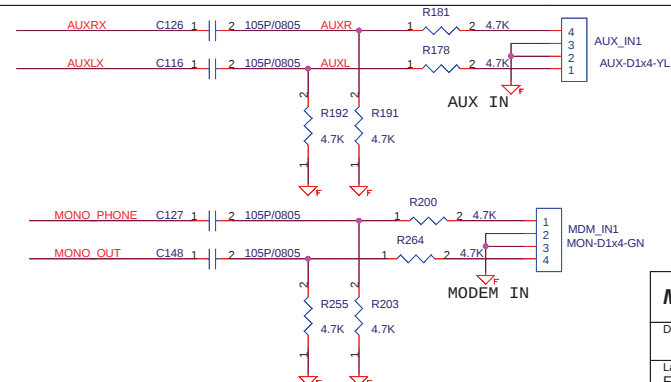
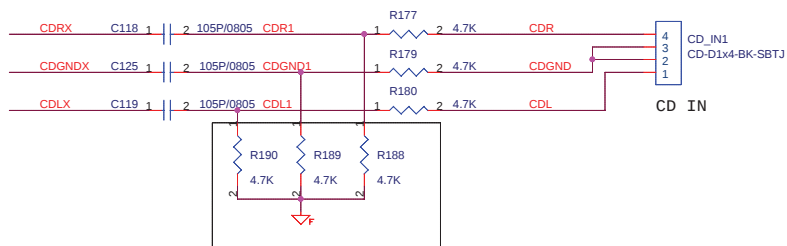
AUDIO CODE CRYSTAL CIRCUIT



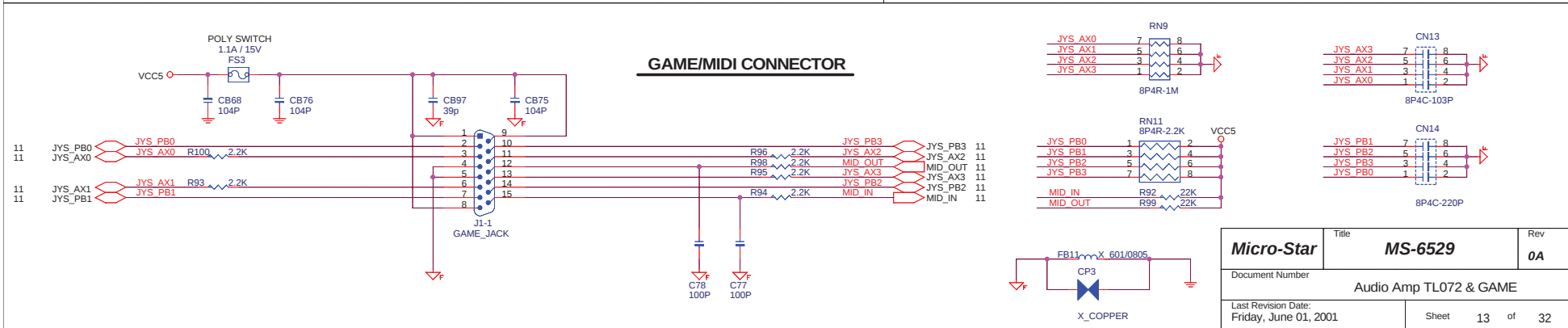
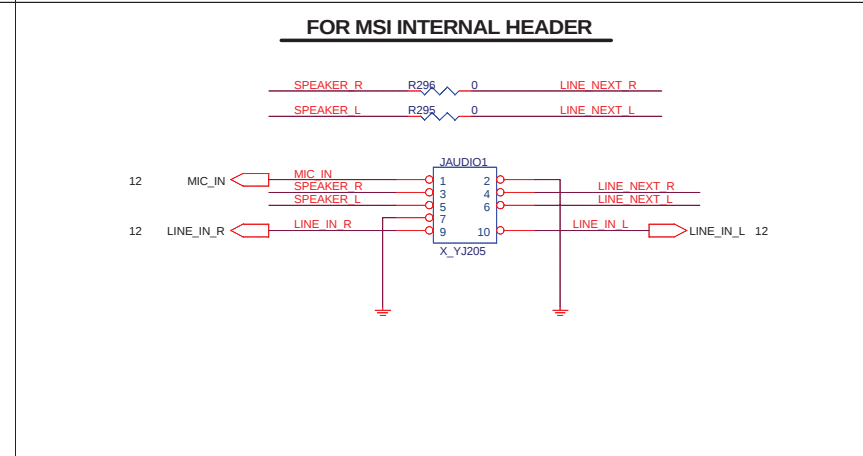
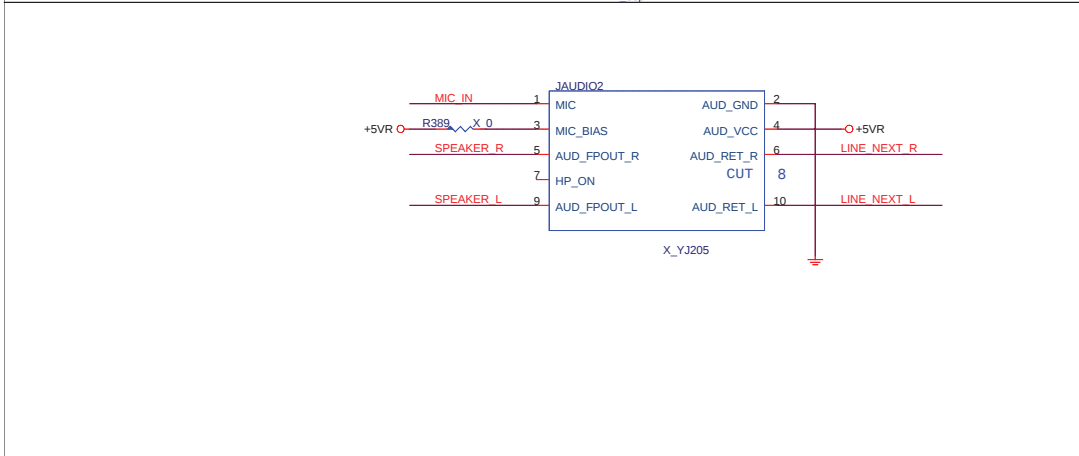
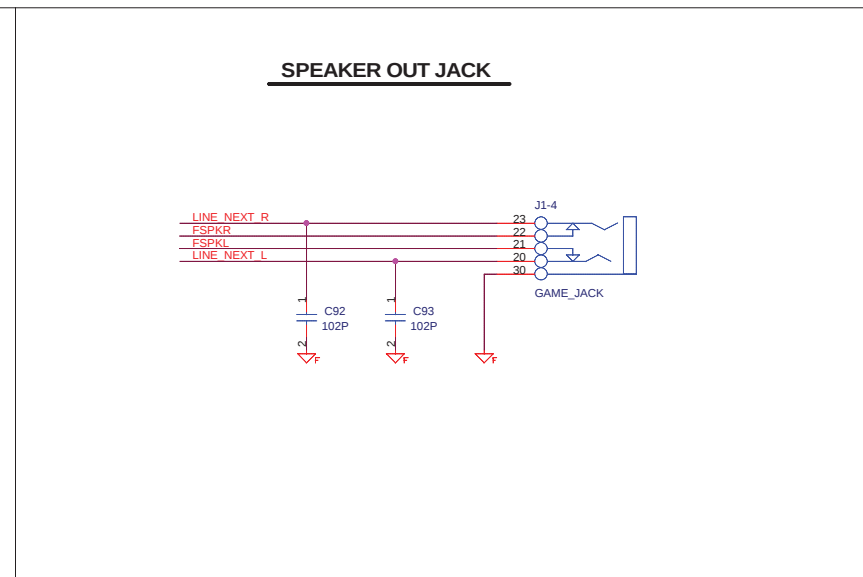
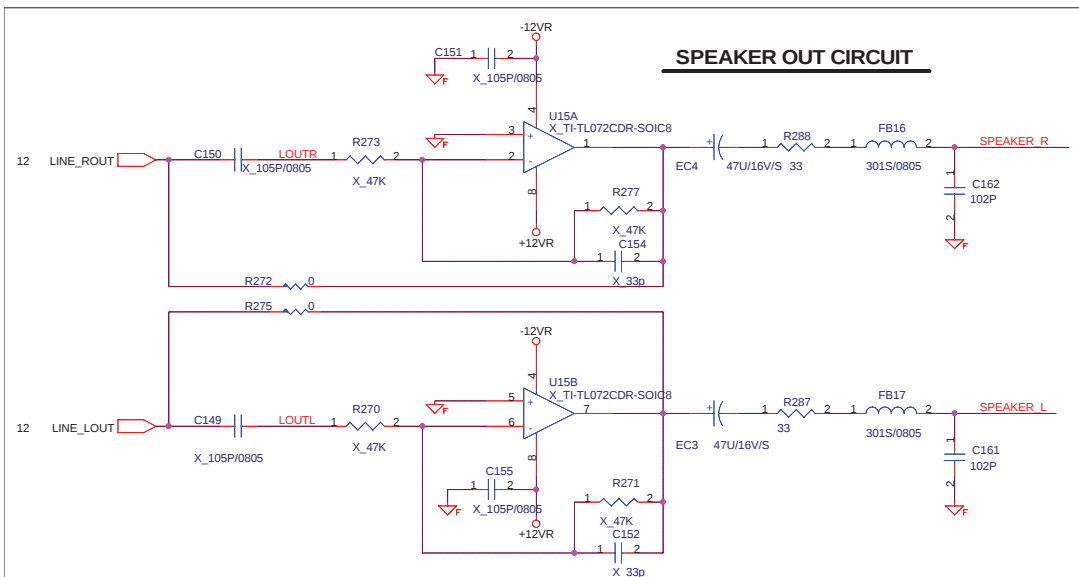
DECOUPLING CAPACITOR



AUDIO CODE CD / AUX / MODEM IN HEADERS



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Firmware Hub (FWH)

The diagram illustrates the Firmware Hub (FWH) circuit. The central component is the U17 PLCC32-SMT (1ST PART FIELD). It is connected to various components including a J4 YJ102 1:2 divider, resistors R327 (4.7K), R338 (8.2K), and R337 (8.2K), and several test points (PCIRST#1, SD_DET, PD_DET, GP23, FWH0-FWH3, LFRAME#/FWH4, LAD3/FWH3). Power is supplied by VCC3 and GND pins. The diagram shows connections for pins 1 through 32 of U17.

J4 BIOS Update	
SHORT	Locked
* OPEN	Unlocked

FWH INIT Signal Voltage Translation Block

9

FWH RESISTORS

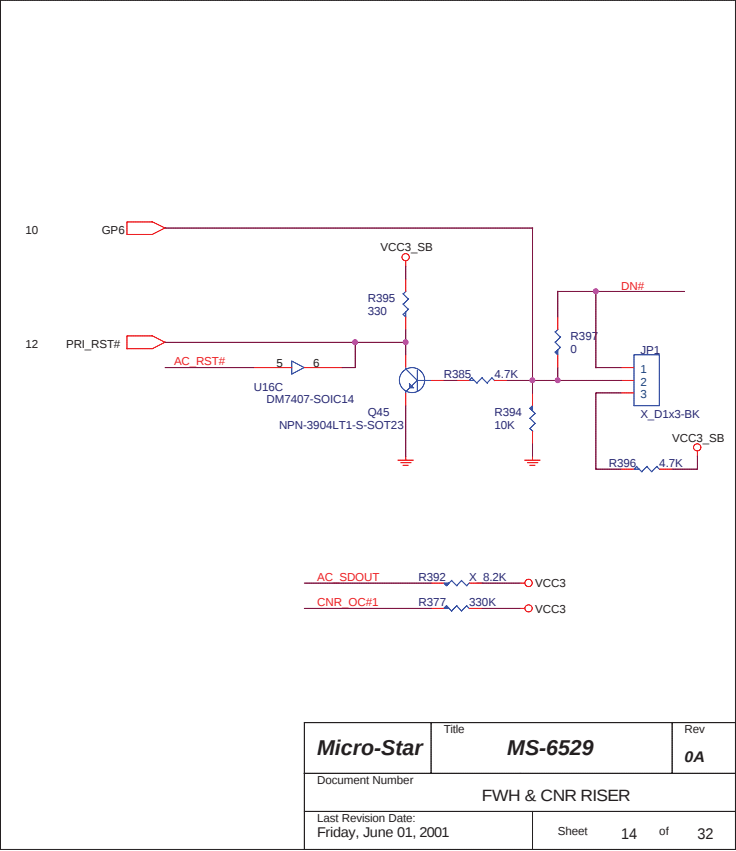
4/12/2001

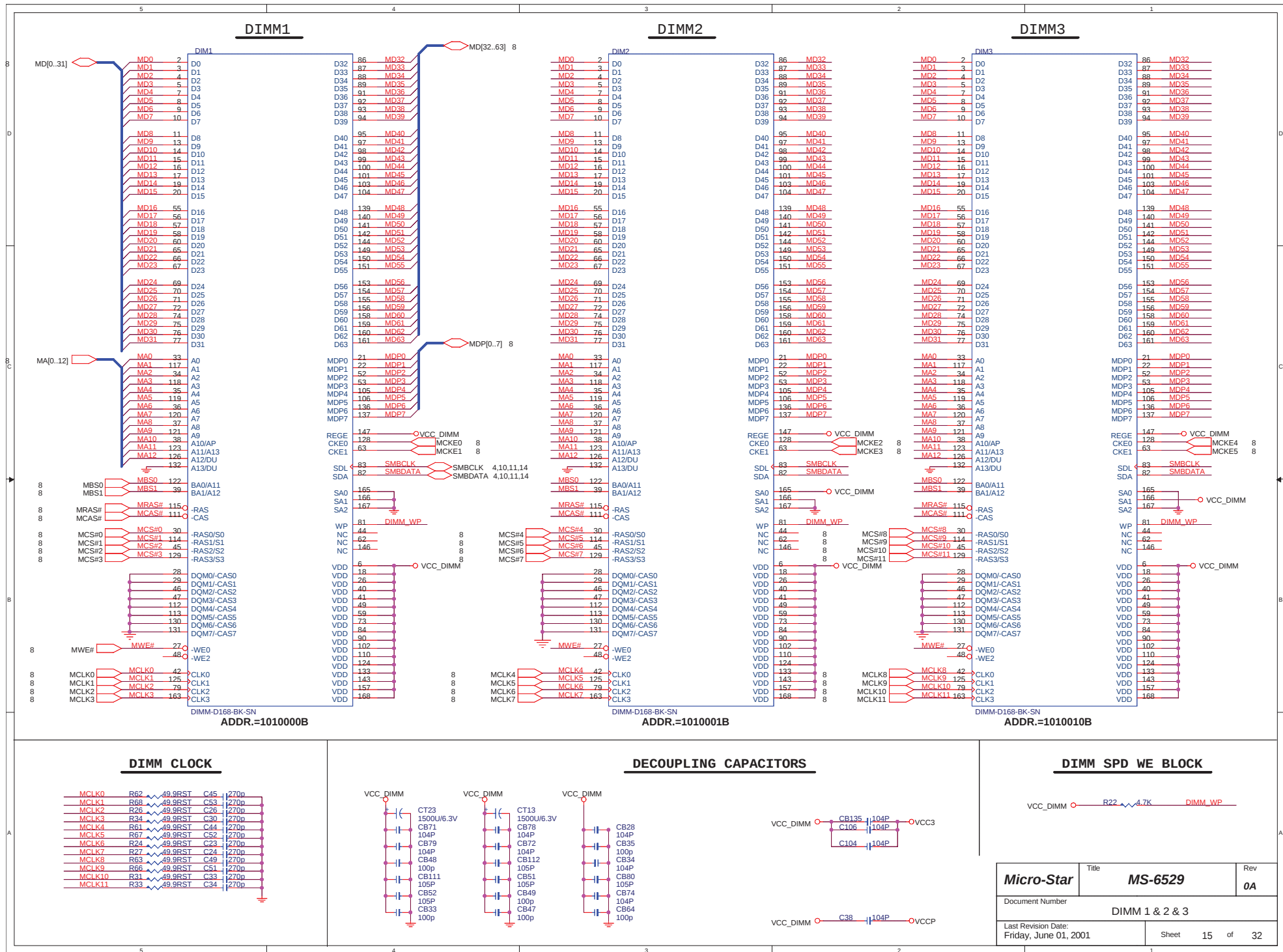
CNR Damping Resistor Net

The diagram illustrates the CNR Damping Resistor Net, showing four sets of connections between a central resistor network and various signal lines. Each set includes a resistor value and a pin number.

- RN31 8P4R-33**: Connects to CNR_RST (pin 1), CNR_TXD0 (pin 3), CNR_TXD1 (pin 5), and CNR_TXD2 (pin 7). The other side of the resistor network connects to RST (pin 2), TXD0 (pin 4), TXD1 (pin 6), and TXD2 (pin 8).
- RN29 8P4R-33**: Connects to CNR_RXD0 (pin 1), CNR_RXD1 (pin 3), CNR_RXD2 (pin 5), and CNR_CLK (pin 7). The other side of the resistor network connects to RXD0 (pin 2), RXD1 (pin 4), RXD2 (pin 6), and LAN_PCLK (pin 8).
- 8P4R-0**: Connects to CNR_DOUT (pin 1), CNR_DIN (pin 3), CNR_CS (pin 5), and CNR_SHCLK (pin 7). The other side of the resistor network connects to DOUT (pin 2), DIN (pin 4), CS (pin 6), and SHCLK (pin 8).
- RN15**: Connects to CNR_DOUT (pin 1), CNR_DIN (pin 3), CNR_CS (pin 5), and CNR_SHCLK (pin 7). The other side of the resistor network connects to DOUT (pin 2), DIN (pin 4), CS (pin 6), and SHCLK (pin 8).

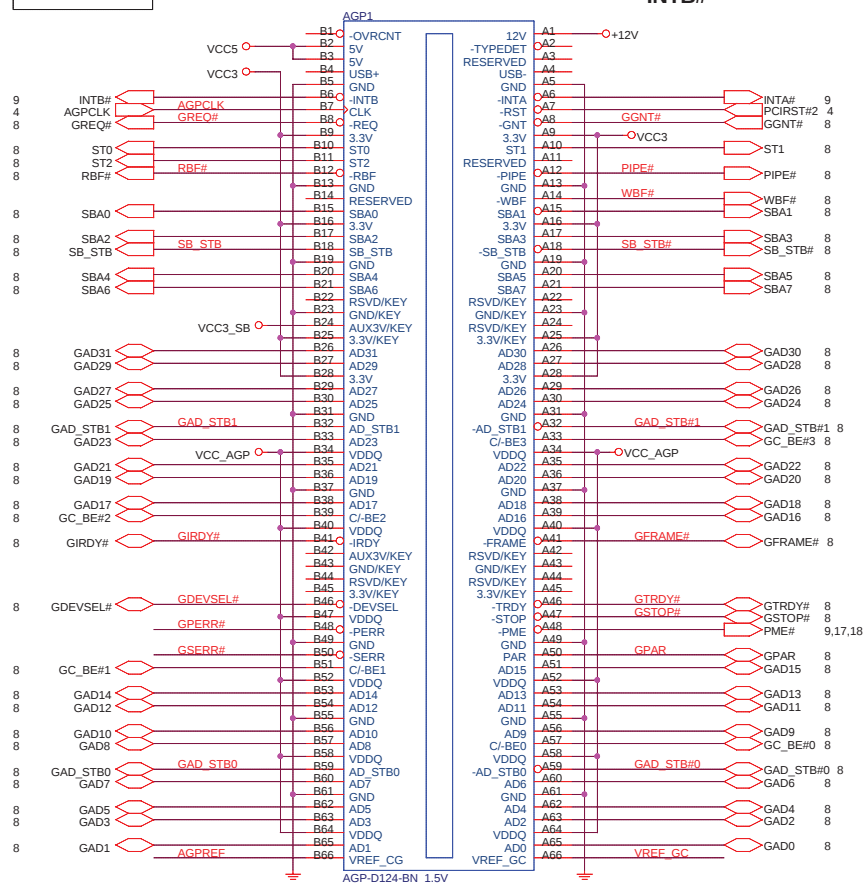
FWH DECOUPLING CAPACITORS

[illegible]



VCC5 = 60mils trace / 15 mils space

VCC AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A



1X Timing group	2X/4X Timing group
AGPCLK	<u>SET#1</u>
PIPE#	GAD[15..0]
RFBI#	GC_BE#1[0]
WFB#	GAD_STB0
ST[2..0]	GAD_STB0#
GFRAME#	<u>SET#2</u>
GRDY#	GAD[31..16]
GTRDY#	GC_BE#3..2
GSTOP#	GAD_STB1
GDEVSEL#	GAD_STB1#
GREQ#	<u>SET#3</u>
GGNT#	SBA[7..0]
GPBAR	SB_STB
	SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

Trace width : 25 mils
C157 should be placed near MCH within 150 mils

The schematic diagram illustrates the VCC_AGP power plane, showing the connection of various components to the VCC_AGP supply and ground. The components are organized into two main sections, each with a list of components and their values, followed by a schematic representation of their connections.

Left Section Components:

- GFRAME# R156 6.8K
- GIRDY# R169 6.8K
- GTRDY# R170 6.8K
- GDEVSEL# R157 6.8K
- GSTOP# R171 6.8K
- GPARR R173 6.8K
- GPERR# R172 6.8K
- GSERR# R158 6.8K
- GREQ# R160 6.8K
- GGNT# R162 6.8K
- ST0 R163 6.8K
- ST1 R164 6.8K
- ST2 R161 6.8K

Right Section Components:

- PIPE# R165 6.8K
- RB# R153 6.8K
- WBF# R166 6.8K
- GAD_STB0 R159 6.8K
- GAD_STB1 R168 6.8K
- SB_STB R154 6.8K
- GAD_STB#1 R155 6.8K
- GAD_STB#0 R174 6.8K
- SB_STB# R167 6.8K

Schematic Representation:

The schematic shows the VCC_AGP supply connected to a network of components. The components are represented by their labels and values, with their connections to the VCC_AGP supply and ground. The components are organized into two main sections, each with a list of components and their values, followed by a schematic representation of their connections.

LESS 100MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

Trace 5mils

The diagram illustrates the relationship between signal rates and AGP STB# for different signal rates and mils. It consists of two rows of horizontal bars. The top row shows two bars for '2x / 4x Signals' at '15 / 20 mils' and '30 mils'. The bottom row shows two bars for 'AGP STB#' at '15 / 20 mils' and '30 mils'. The bars are labeled with their respective signal rates and mils.

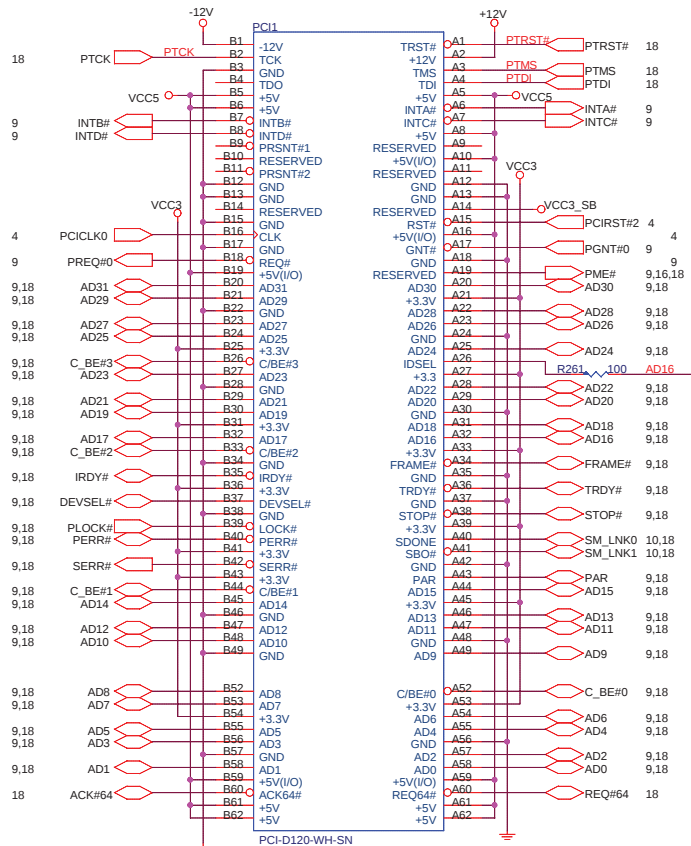
Signal Rate	Mils	AGP STB#
2x / 4x Signals	15 / 20 mils	15 / 20 mils
2x / 4x Signals	30 mils	30 mils

Micro-Star	Title MS-6529	Rev 0A
Document Number		
AGP Slot		
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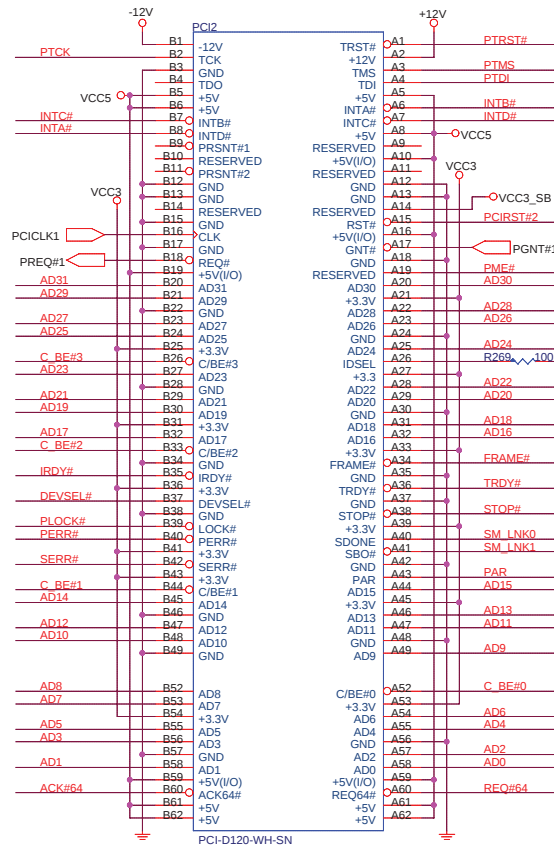
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

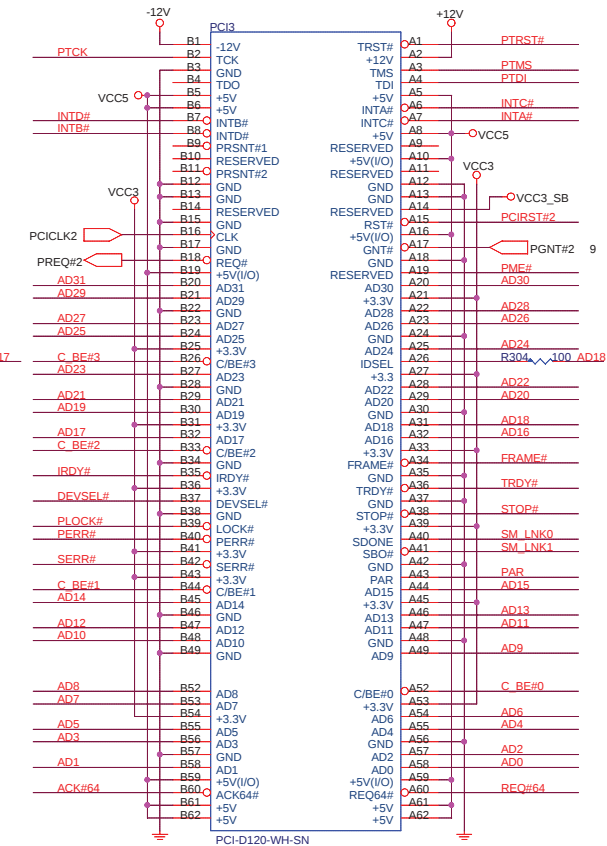
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ0
INTA#



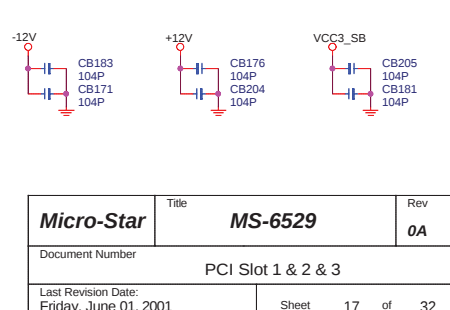
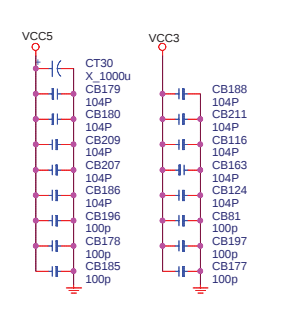
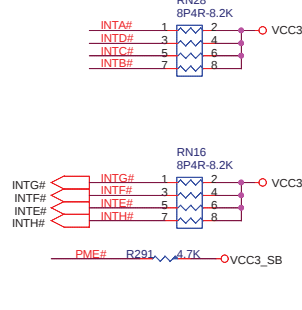
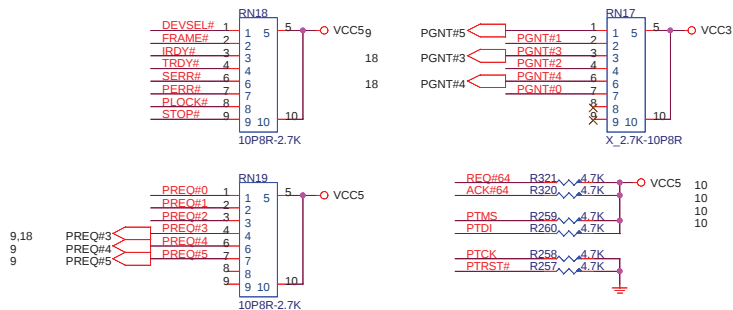
IDSEL = AD17
MASTER = PREQ1
INTB#



IDSEL = AD18
MASTER = PREQ2
INTC#

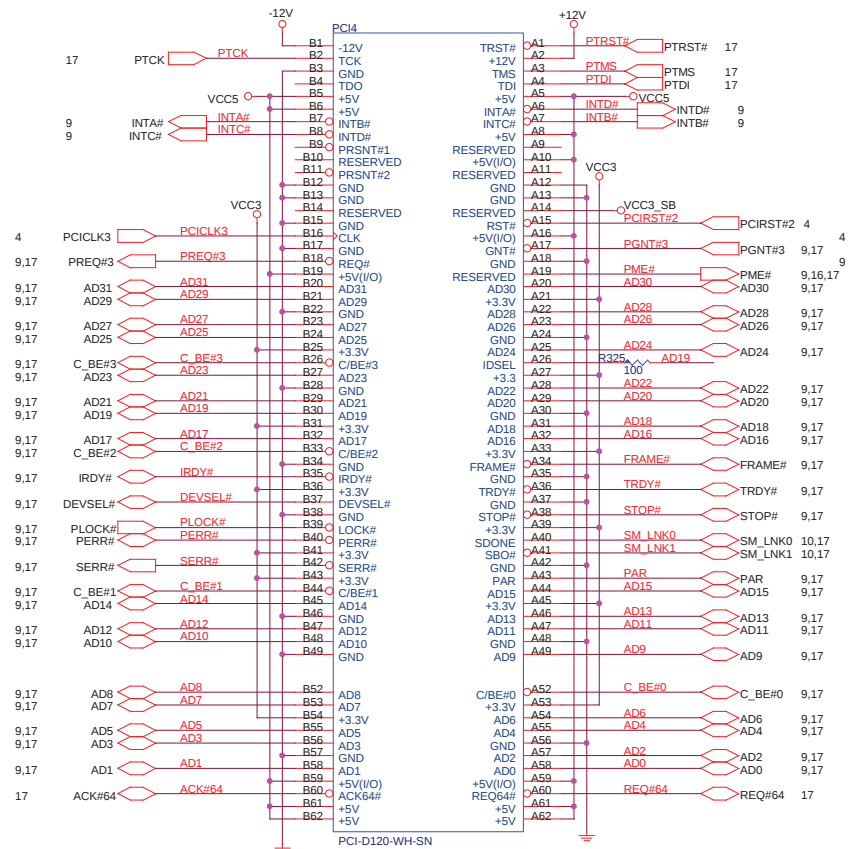
PCI PULL-UP / DOWN RESISTORS

PCI SLOT DECOUPLING CAPACITORS



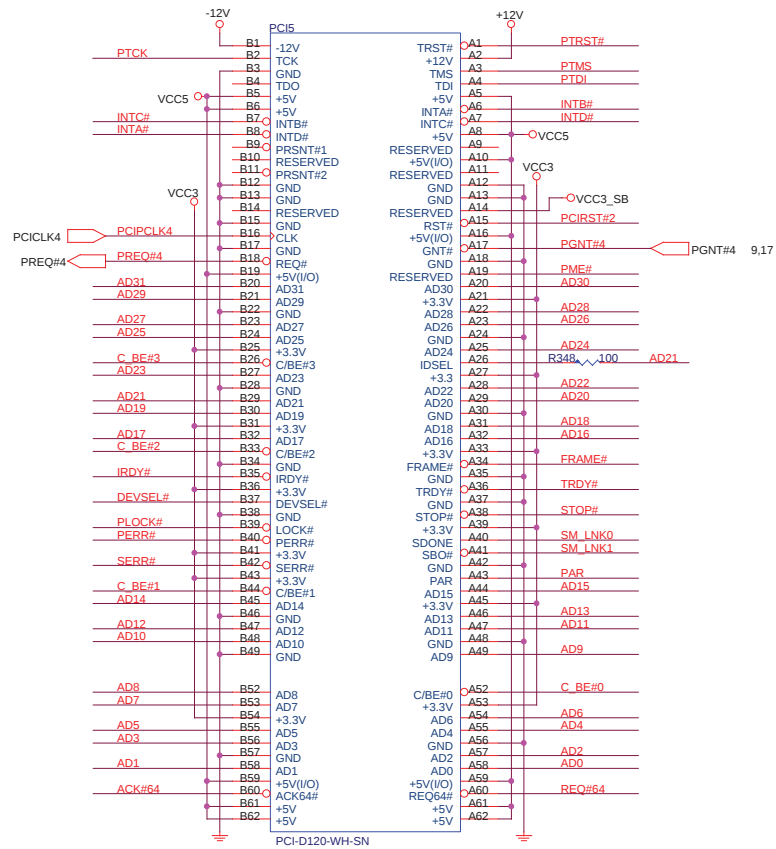
Micro-Star	Title	MS-6529	Rev	0A
Document Number	PCI Slot 1 & 2 & 3			
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PCI SLOT 4 (PCI VER: 2.2 COMPLY)



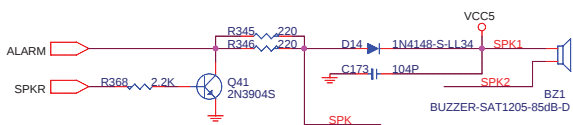
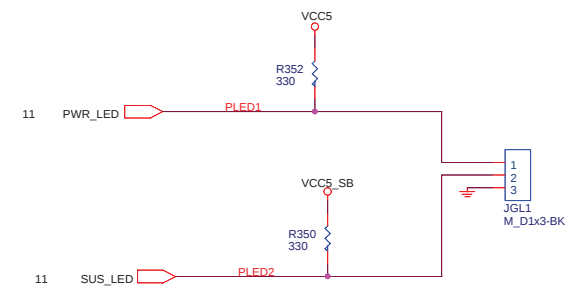
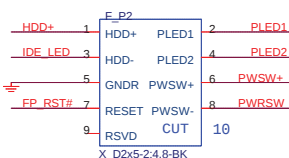
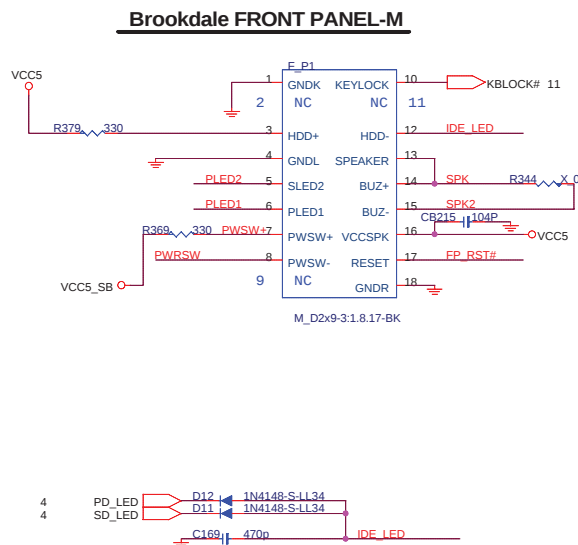
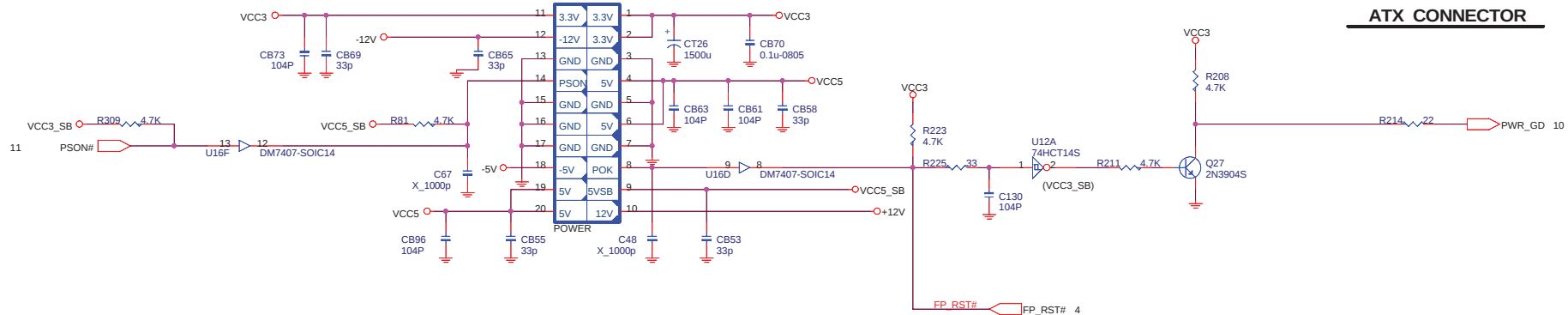
IDSEL = AD19
MASTER = PREQ3
INTD#

PCI SLOT 5 (PCI VER: 2.2 COMPLY)

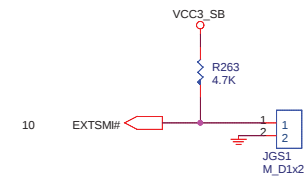
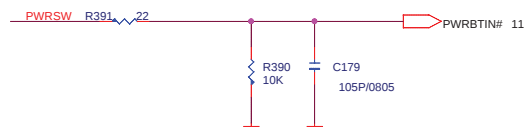


IDSEL = AD21
MASTER = PREQ4
INTA#

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Document Number PCI Slot 4 & 5		
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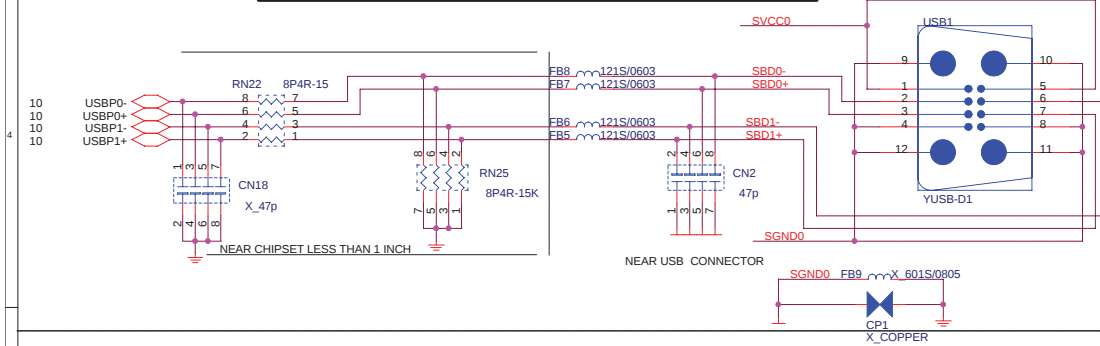


POWER BUTTON

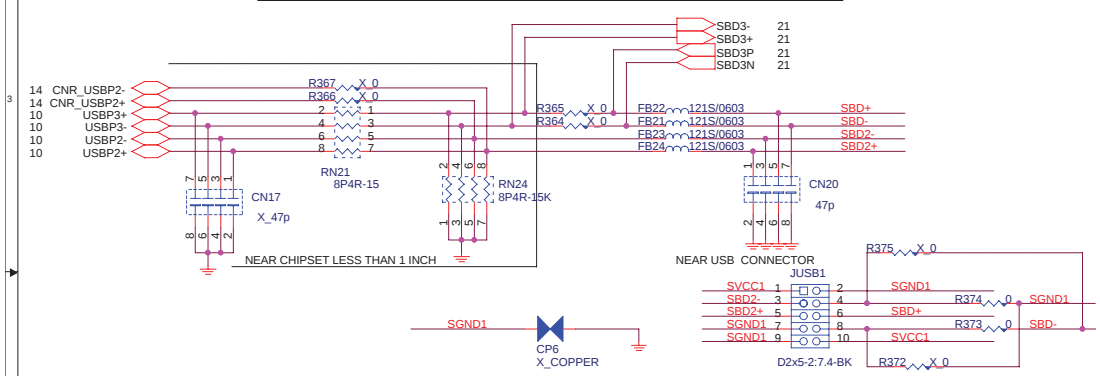


Micro-Star	Title	MS-6529	Rev	0A
	Document Number	Front Panel & Connector		
	Last Revision Date:	Friday, June 01, 2001	Sheet	19 of 32

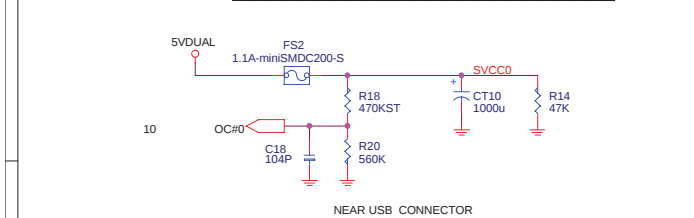
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



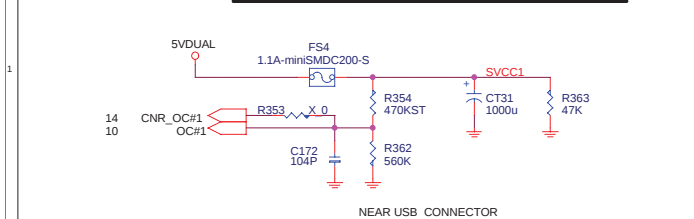
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1

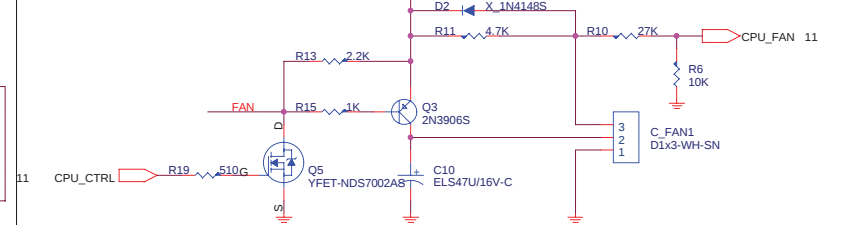


POWER CIRCUIT FOR USB PORT 2, 3

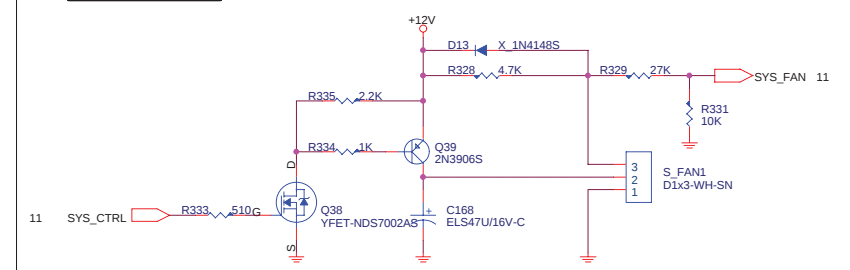


- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signlas Trace Spacing : 18 mils
- * USB Power Trace must be 40mils width

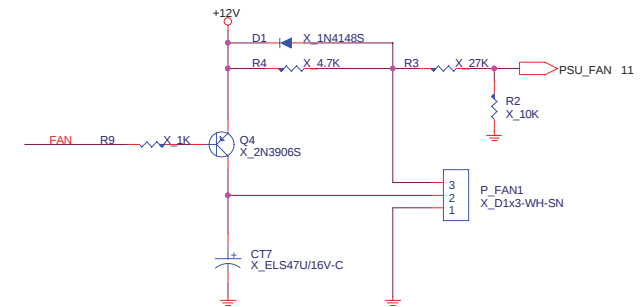
CPU FAN



SYSTEM FAN

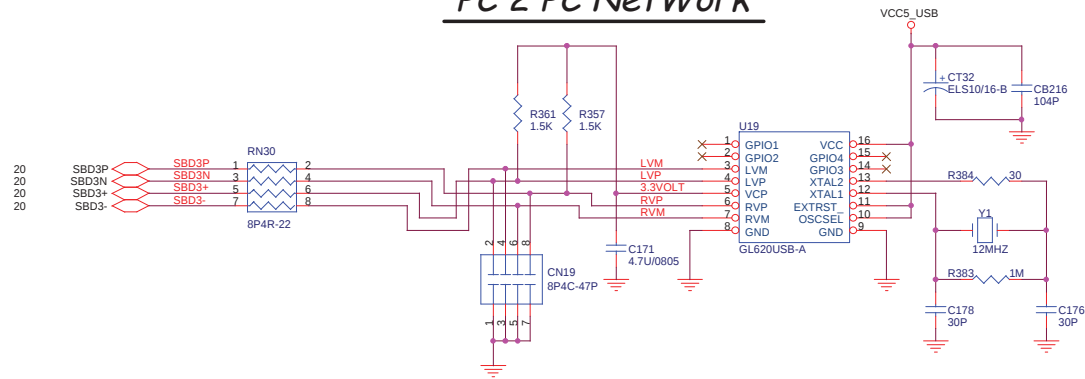


ATX PSU FAN ON/OFF CONTROL

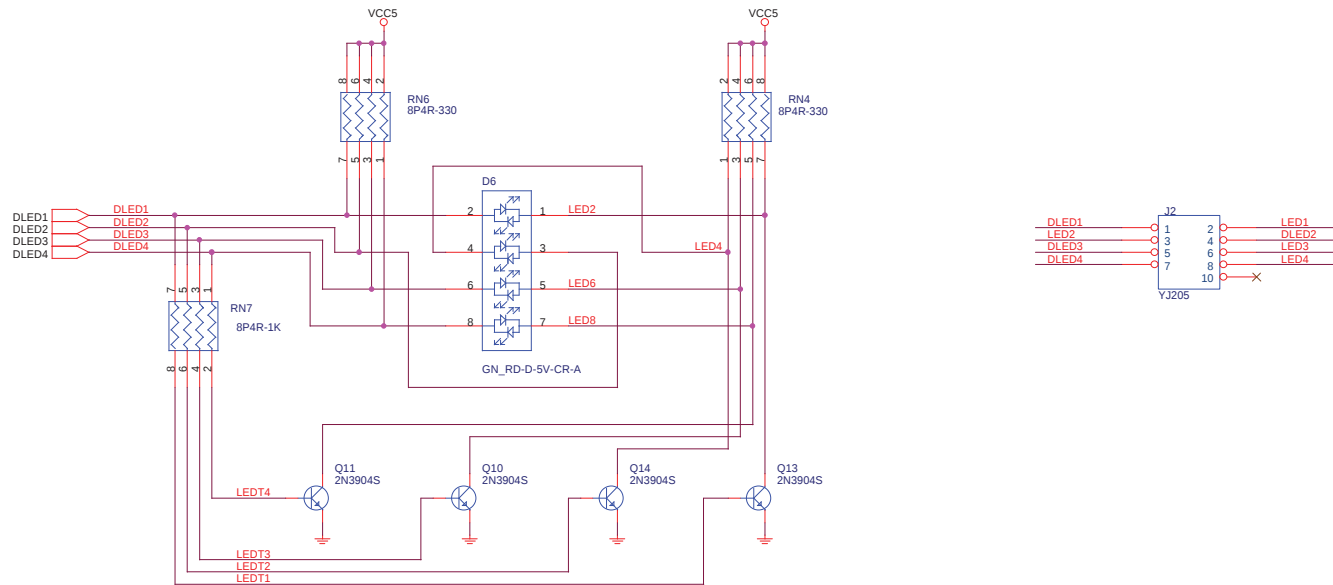


Micro-Star	Title	MS-6529	Rev	0A
Document Number	USB & FAN Connectors			
Last Revision Date: Friday, June 01, 2001	Sheet	20	of	32

PC 2 PC NetWork

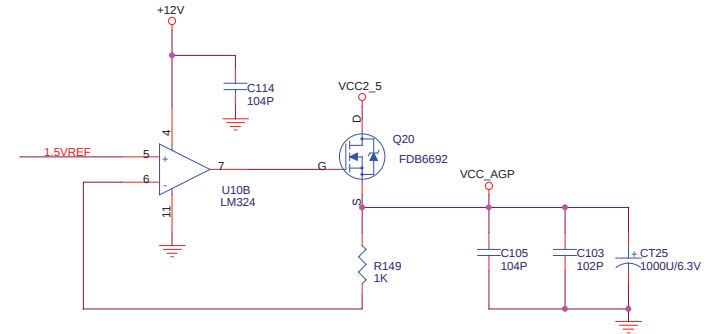
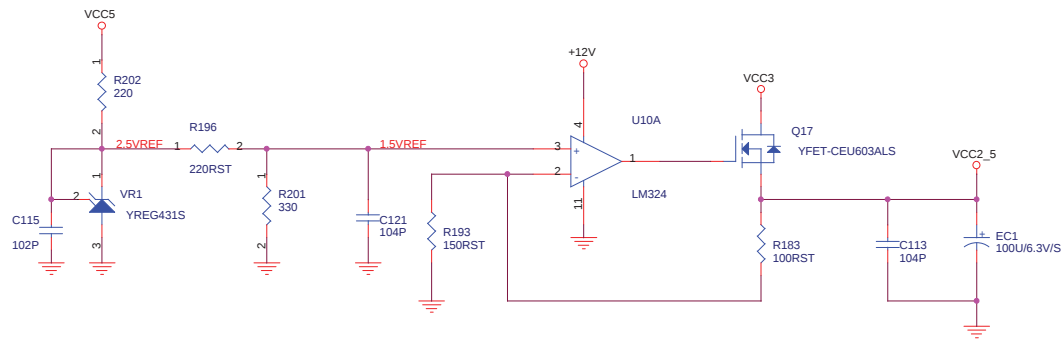


DLED

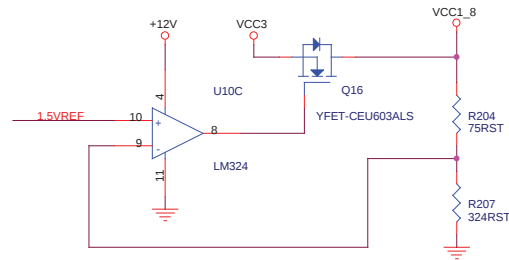


Micro-Star	Title MS-6529	Rev 0A
Document Number PC2PC & D-LED		
Last Revision Date: Friday, June 01, 2001		
Sheet	21	of 32

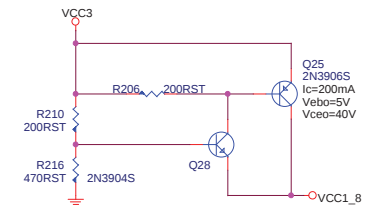
AGP Power



Chipset Power

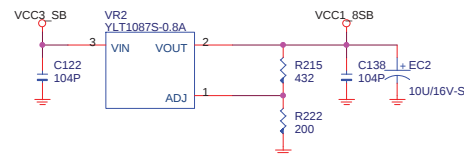


1.8V/3.3V SEQUENCE CIRCUIT

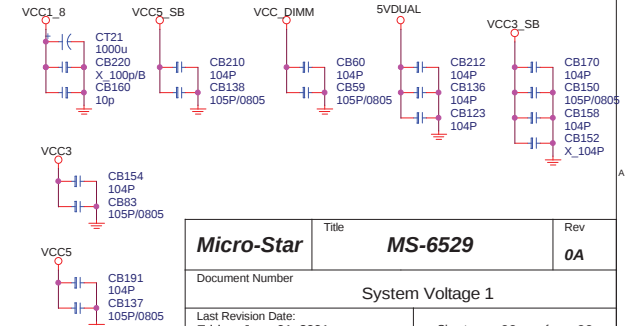


1.8V STANDBY POWER TRANSLATOR

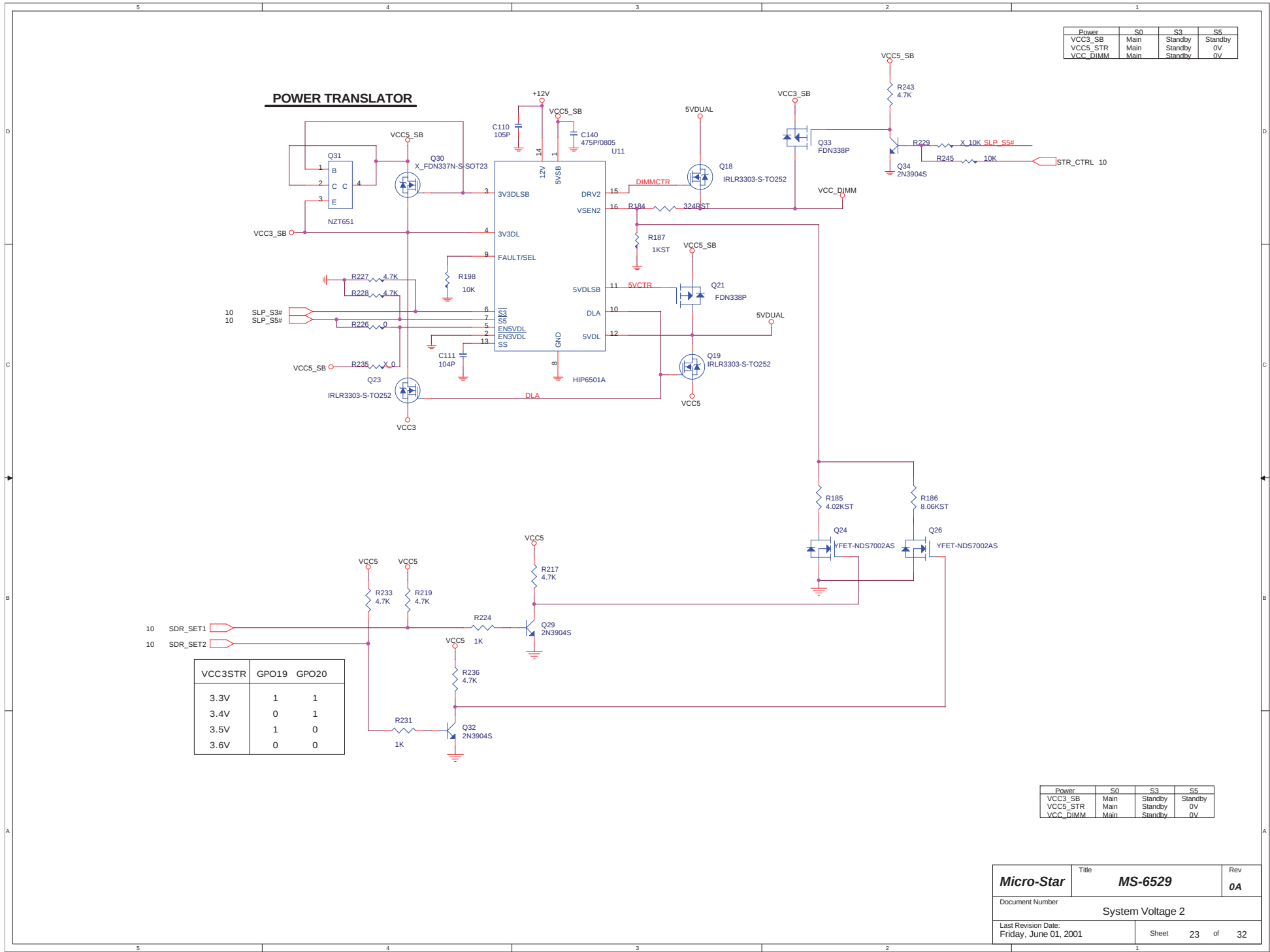
(40mils trace / 20 mils space)



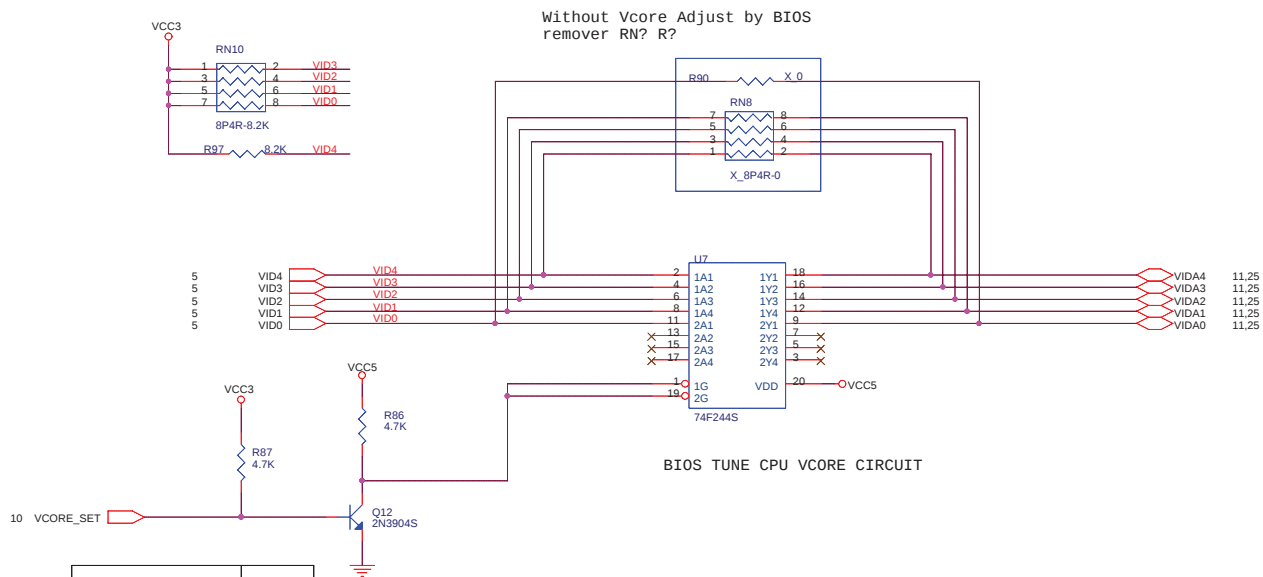
REGULATORS OUTPUT DECOUPLING CAPACITORS



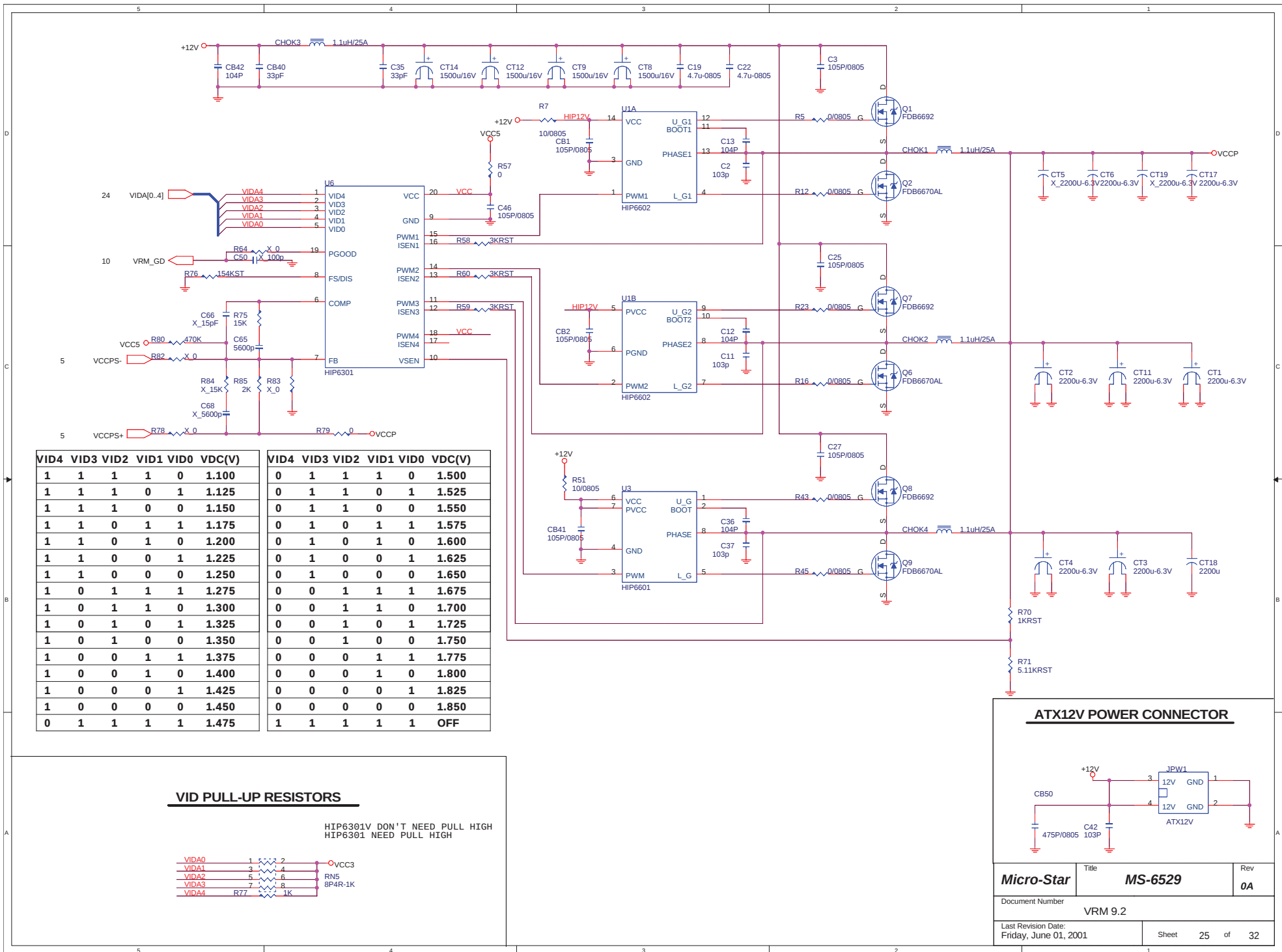
Micro-Star	Title	MS-6529	Rev	0A
Document Number	System Voltage 1			
Last Revision Date:	Friday, June 01, 2001			Sheet 22 of 32

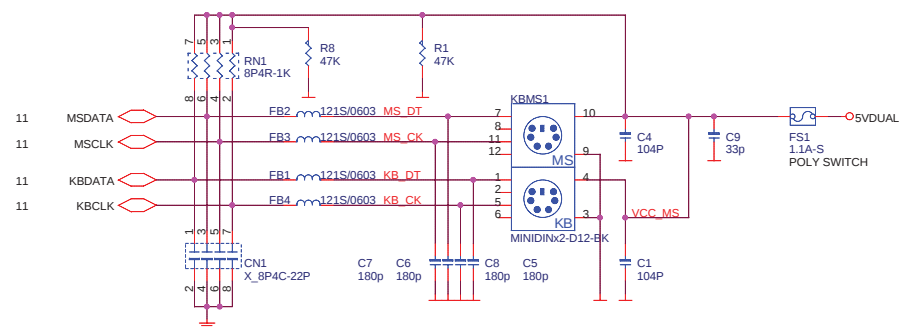
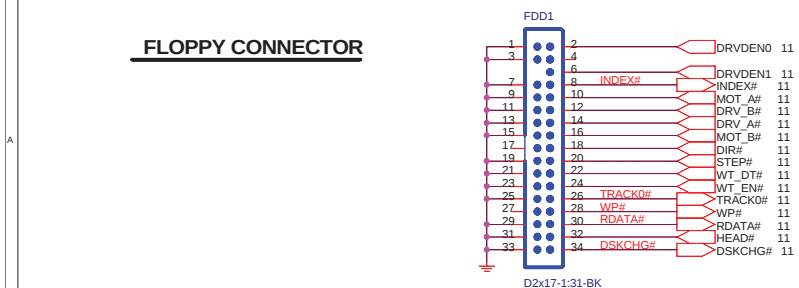
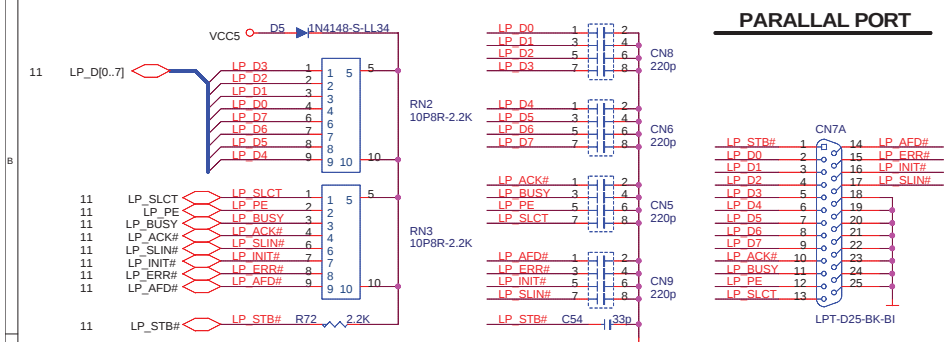
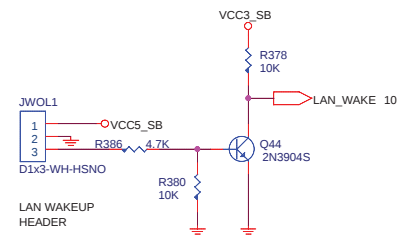
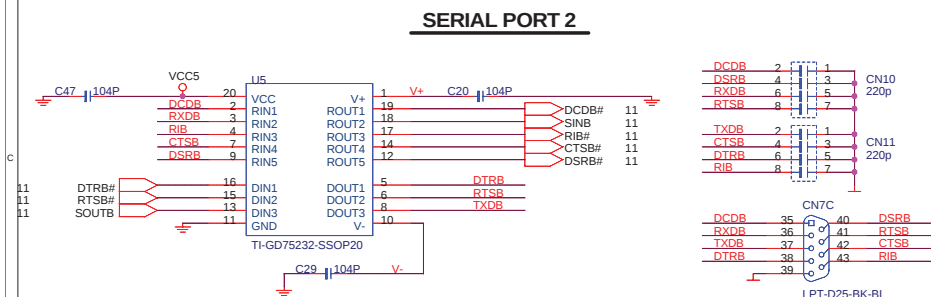
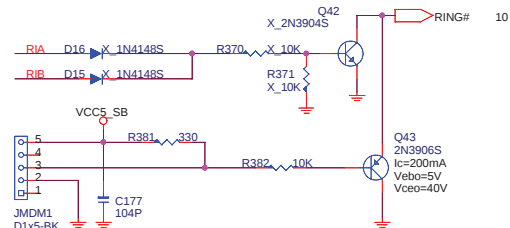
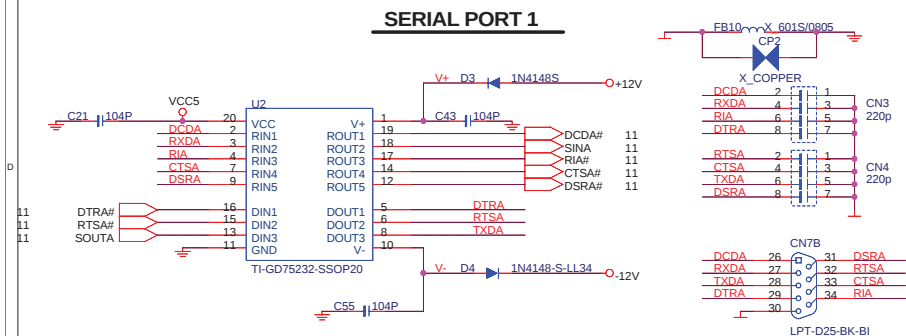


CPU VID Control



VCORE Setting	GPIO21
CPU Default	1
Maanuel Setting	0





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POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1881A	0	0	0	0	0	0	0	0	0
FWH_SST	0	0	0	0	0	0	0	0	0
W33627HE	0	0	0	0	0	0	0	0	0
HIP6301	0	0	0	0	0	0	0	0	0
HIP6602A	0	0	0	0	0	0	0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0	0	0	0
DIMM	0	0	0	NOTE2	0	0	NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0	0	0	0	0	0
USB	0	0	0	0	0	0	0	0	0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0	0	0	0	0	0
OTHER	0	0	0	0	0	0	0	0	0

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A --> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA --> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

Jumper Setting & Connector Setting

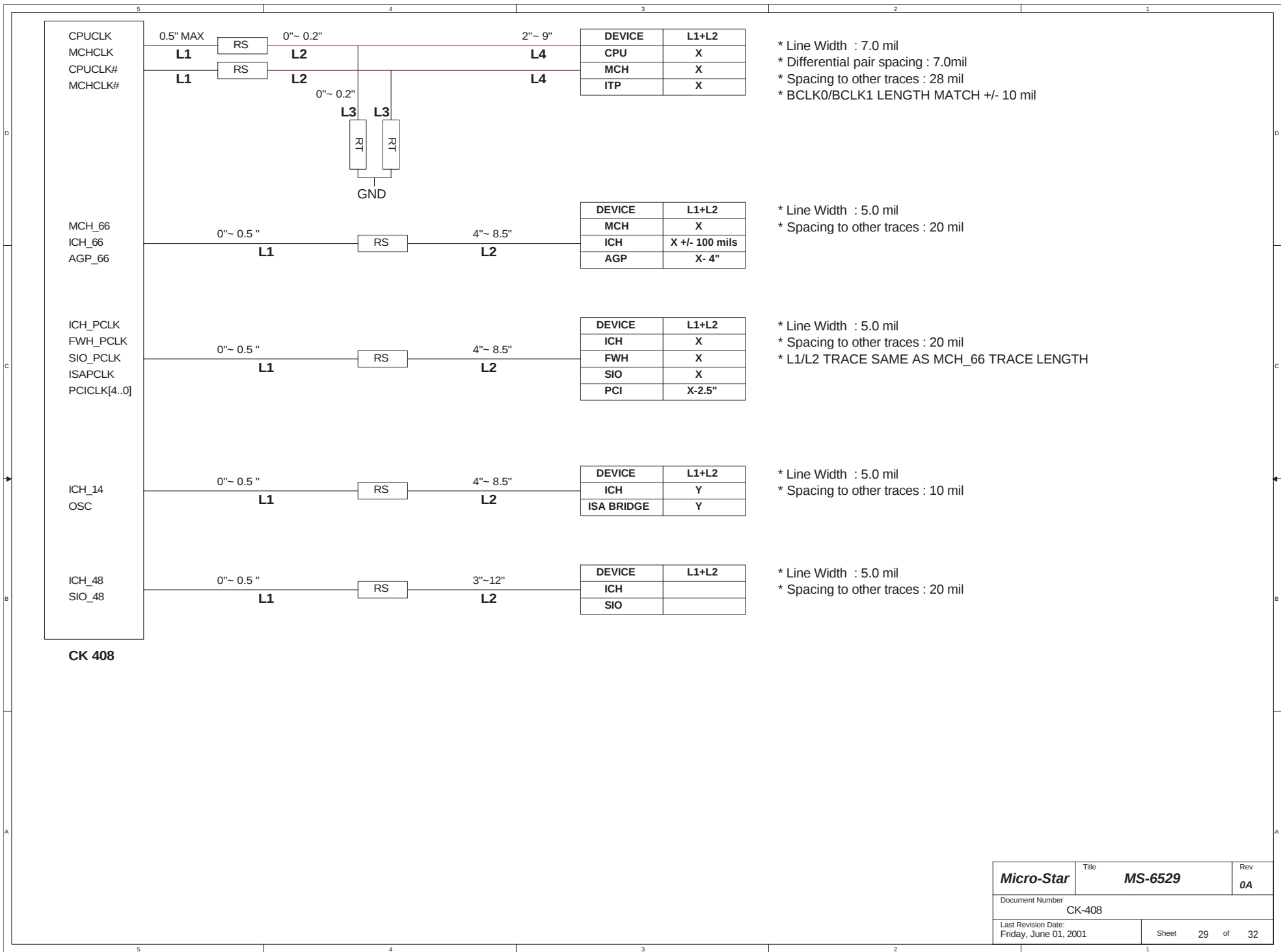
Jumper

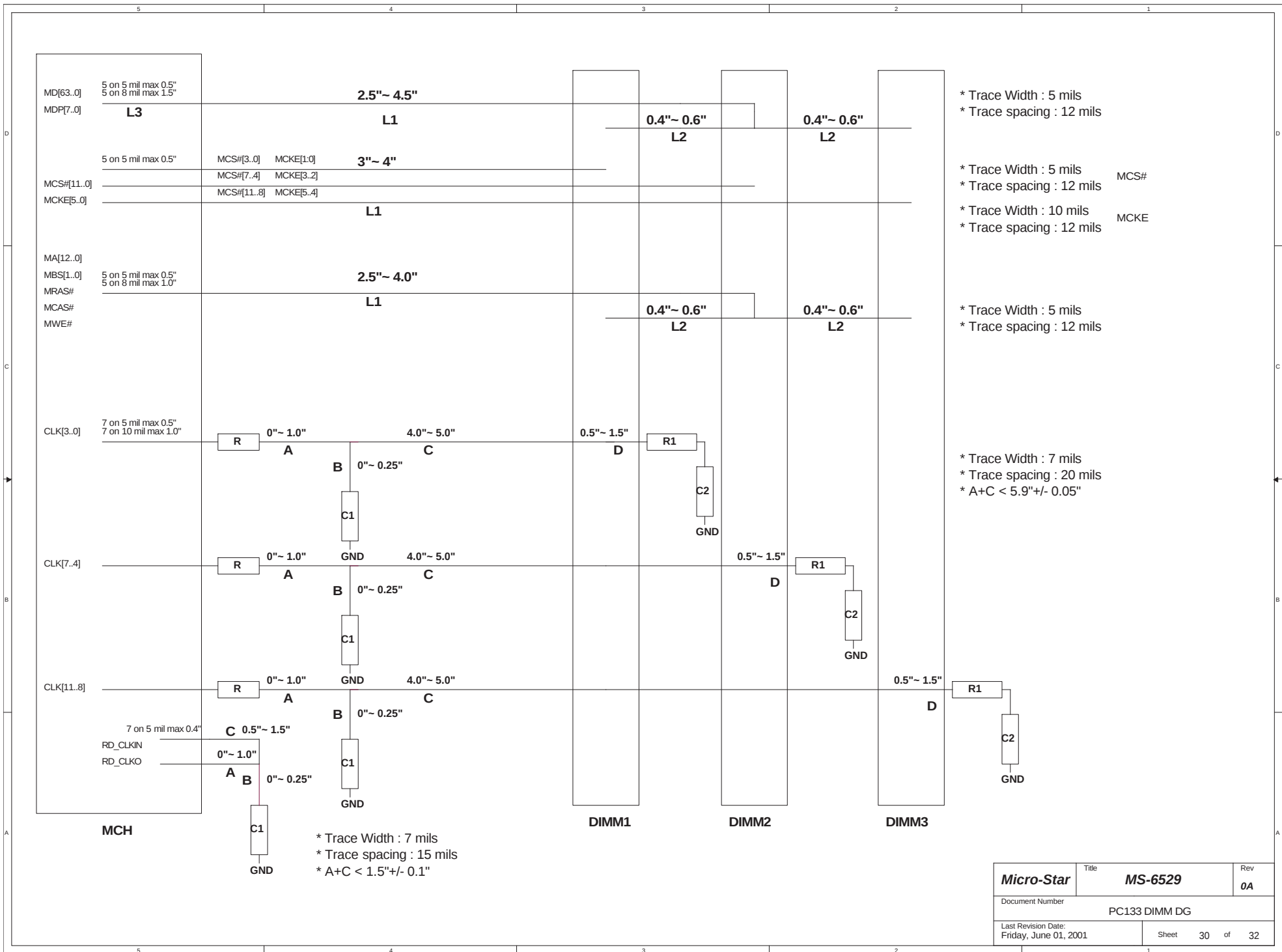
J1	INTERUDER HEADER
J2	CHASSIS INTRUSION HEADER
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)
J4	AUDIO AUX HEADER
J5	AUDIO FRONT PANEL HEADPHONE JACK HEADER
J6	AUDIO INTERNAL SPEAKER HEADER (ATAPI)
J8	CPU SIMULATION PIN
J9	DDR SIMULATION PIN
J10	AGP SIMULATION PIN
J11	BIOS function
1-2	Normal (Default)
2-3	Configuration Mode
JBAT1	CLEAR CMOS
1-2	NORMAL (Default)
2-3	CLEAR CMOS
JP2	CNR RISER CODEC SELECT HEADER
1-2	AUTO MODE (Default)
2-3	PRIMARY AUDIO CODEC ONBOARD
JP3	LEGEND AUDIO HEADER

Connector

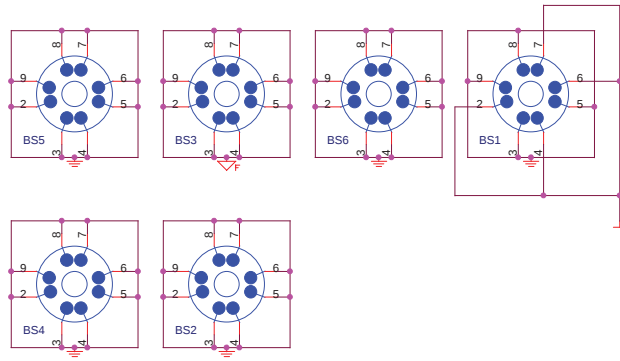
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
PCI4	PCI Slot4
PCI5	PCI Slot5
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floppy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
S_FAN	System FAN HEADER
USB1	USB REAR CONNECTOR
USB2	USB INTERNAL HEADER
POWER	ATX Power
F_P1	Front Panel
C_FAN1	CPU FAN HEADER
S_FAN1	SYS FAN HEADER
P_FAN1	ATX FAN HEADER
JAUDIO1	AUDIO HEADER FOR LEGEND
CD_IN1	CD IN HEADER
CD_IN2 / JSCD1	CD-IN HEADER FOR LEGEND
AUX_IN1	AUX_IN HEADER
MDM_IN1	MODEM_IN HEADER
IR1	IR HEADER
JPW1	ATX12V Power

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PCB OTHER COMPONENT



SIMULATION TRACE



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	Document Number	MANUAL		
	Last Revision Date:	Friday, June 01, 2001	Sheet	31 of 32

Revision Initial ver: 0A on 04/09/00

Schematic Initial Revision 0A

The figure is a large, empty rectangular area representing a schematic diagram. It is bounded by a grid with labels A, B, C, D on the left and 1, 2, 3, 4, 5 on the top. The area is currently blank, with only a few small black marks visible near the bottom left corner.

Micro-Star	Title MS-6529	Rev 0A
Document Number		
Revision History - 1		
Last Revision Date: Friday, June 01, 2001	Sheet	32 of 32

Revision Initial ver: 0A on 04/09/00

Schematic Initial Revision 0A

A large empty rectangular area for a schematic diagram, bounded by a grid with labels A, B, C, D on the left and 1, 2, 3, 4, 5 on the top. The area is currently blank, with only a few small black marks visible near the bottom left corner.

Micro-Star	Title MS-6529	Rev 0A
Document Number		
Revision History - 1		
Last Revision Date: Friday, June 01, 2001	Sheet	32 of 32

Revision Initial ver: 0A on 04/09/00

Schematic Initial Revision 0A

A large empty rectangular area for a schematic diagram, bounded by a grid with labels A, B, C, D on the left and 1, 2, 3, 4, 5 on the top. The area is currently blank, with only a few small black marks visible near the bottom left corner.

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