MS-6527

Version 11A
10/05/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:
Willamette/Northwood mPGA-478B Processor

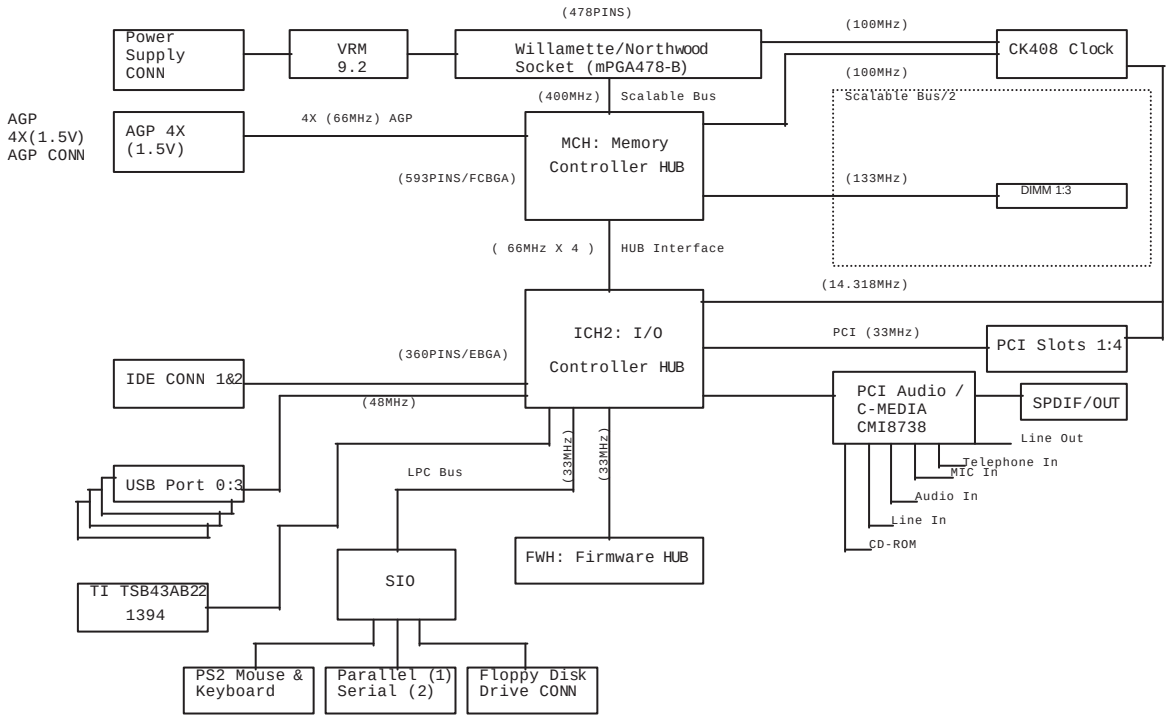
System Brookdale Chipset:
INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:
BIOS -- FWH
LPC Super I/O -- W83627HF
Clock Generation -- CY28324
PCI SOUND -- C-MEDIA CMI8738
PCI 1394 --TI TSB43AB22

Expansion Slots:
AGP2.0 SLOT * 1
PCI2.2 SLOT * 4

Standard:Wo/1394, Wo/Front Audio
Opt A:W/1394, W/Front Audio, Wo/PCI4

Micro-Star	Title: *MS-6527*	Rev: *11A*
Document Number: Cover Sheet		
Last Revision Date: Friday, October 05, 2001	Sheet 1 of 33	



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: Block Diagram		
Last Revision Date: Friday, October 05, 2001	Sheet 2 of 33	

General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Not Implemented
GPIO 22	OD	4.7K pull up VCC3
GPIO 23	O	BIOS Locked/Unlocked
GPIO 24	I/O	Non
GPIO 25	I/O	Non
GPIO 26	I/O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	Non
GPIO 29~31	O	Not Implemented

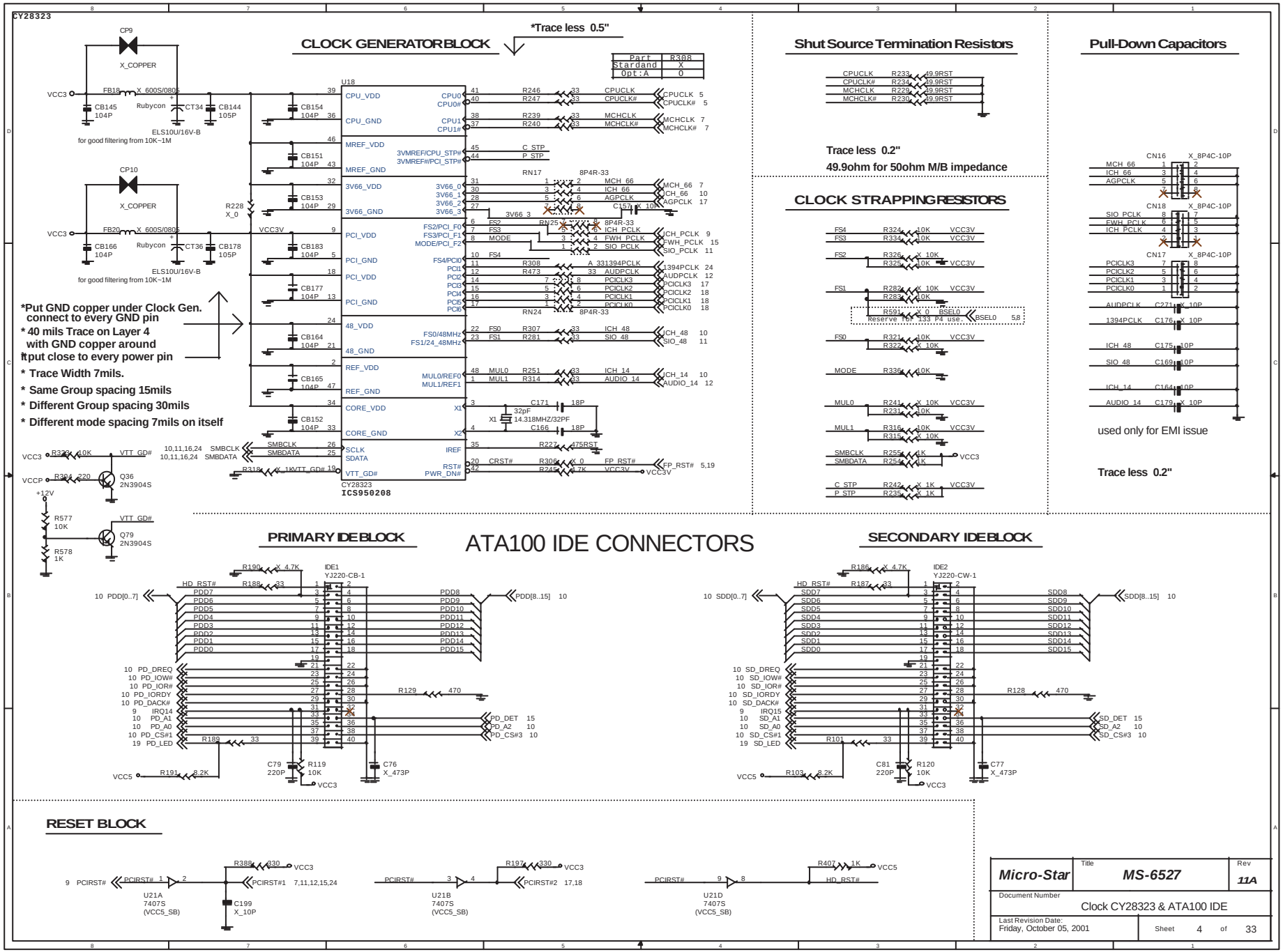
FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

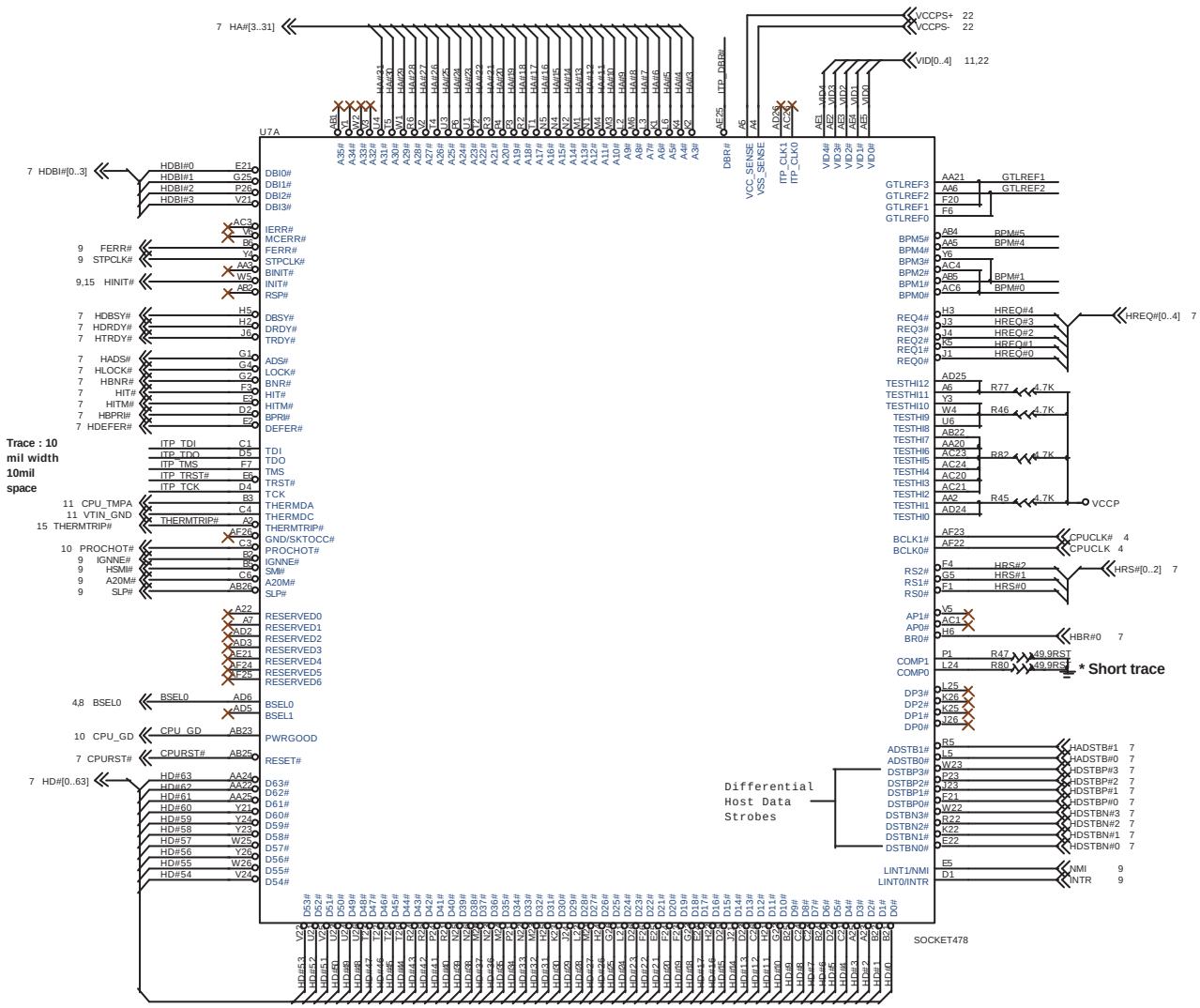
DLED-Super I/O

GPIO Pin	Type	Function
GP32	I/OD	Non Connect
GP24	I/OD	Non Connect
GP34	I/OD	Non Connect
GP33	I/OD	Non Connect

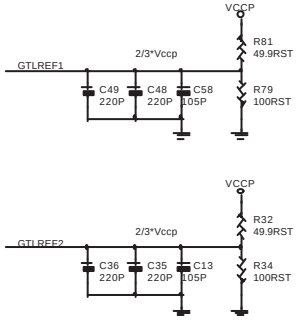
DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19
PCI Audio	INTF#	AD25
PCI 1394	INTH#	AD23


CY28323
CLOCK GENERATOR BLOCK
*Trace less 0.5"
Part | R308
Stardand | X
Opt:A | 0
U18
CPU_VDD
CPU_GND
MREF_VDD
MREF_GND
3V66_VDD
3V66_GND
PCI_VDD
PCI_GND
48_VDD
48_GND
REF_VDD
REF_GND
CORE_VDD
CORE_GND
SCLK
SDATA
VTT_GD#
CPU0
CPU0#
CPU1
CPU1#
3VMREF/CPU_STP#
3VMREF#/PCI_STP#
3V66_0
3V66_1
3V66_2
3V66_3
FS2/PCI_F0
FS3/PCI_F1
MODE/PCI_F2
FS4/PCI0
PCI1
PCI2
PCI3
PCI4
PCI5
PCI6
FS0/48MHz
FS1/24_48MHz
MUL0/REF0
MUL1/REF1
X1
X2
IREF
RST#
PWR_DN#
CY28323
ICS950208
CPUCLK
CPUCLK#
MCHCLK
MCHCLK#
C_STP
P_STP
MCH_66
ICH_66
AGPCLK
ICH_PCLK
FWH_PCLK
SIO_PCLK
1394PCLK
AUDPCLK
PCICLK3
PCICLK2
PCICLK1
PCICLK0
ICH_48
SIO_48
ICH_14
AUDIO_14
FP_RST#
CRST#
SMBCLK
SMBDATA
10,11,16,24 SMBCLK
10,11,16,24 SMBDATA
*Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Different mode spacing 7mils on itself
Shut Source Termination Resistors
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
Reserve for 133 P4 use.
Pull-Down Capacitors
CN16 X_8P4C-10P
CN18 X_8P4C-10P
CN17 X_8P4C-10P
used only for EMI issue
Trace less 0.2"
ATA100 IDE CONNECTORS
PRIMARY IDE BLOCK
SECONDARY IDE BLOCK
IDE1 YJ220-CB-1
IDE2 YJ220-CW-1
PDD[0..7]
PDD[8..15]
SDD[0..7]
SDD[8..15]
PD_DREQ
PD_IOW#
PD_IOR#
PD_IORDY
PD_DACK#
IRQ14
PD_A1
PD_A0
PD_CS#1
PD_LED
PD_DET
PD_A2
PD_CS#3
SD_DREQ
SD_IOW#
SD_IOR#
SD_IORDY
SD_DACK#
IRQ15
SD_A1
SD_A0
SD_CS#1
SD_LED
SD_DET
SD_A2
SD_CS#3
RESET BLOCK
PCIRST#
PCIRST#1 7,11,12,15,24
PCIRST#2 17,18
HD_RST#
U21A 7407S (VCC5_SB)
U21B 7407S (VCC5_SB)
U21D 7407S (VCC5_SB)
Micro-Star
MS-6527
11A
Document Number
Clock CY28323 & ATA100 IDE
Last Revision Date:
Friday, October 05, 2001
Sheet 4 of 33

CPU SIGNAL BLOCK

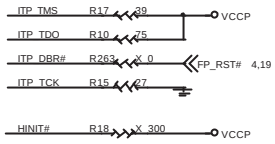


CPU GTL REFERNCE VOLTAGE BLOCK

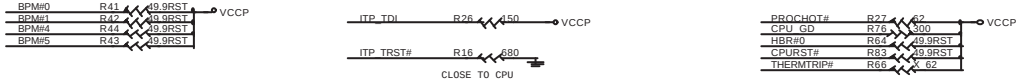


Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



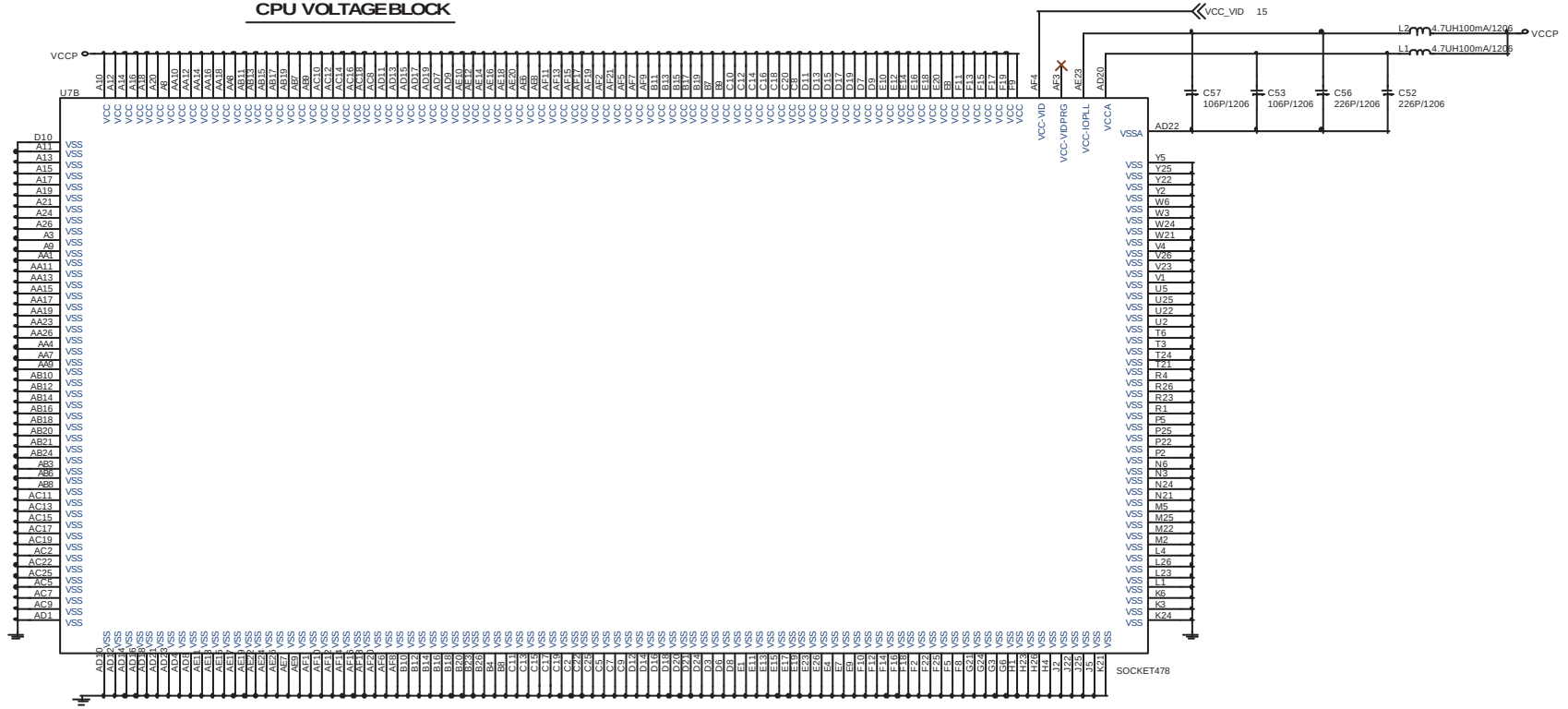
CPU STRAPPING RESISTORS



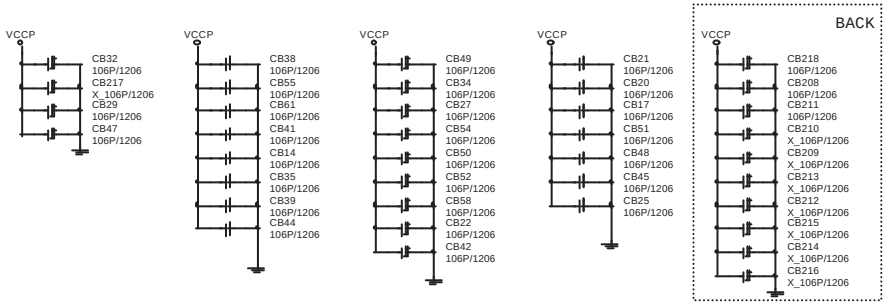
ALL COMPONENTS CLOSE TO CPU

Micro-Star	Title: MS-6527		Rev: 11A
Document Number: INTEL mPGA478-B CPU1			
Last Revision Date: Friday, October 05, 2001		Sheet 5 of 33	

CPU VOLTAGE BLOCK

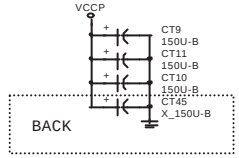


CPU DECOUPLING CAPACITORS



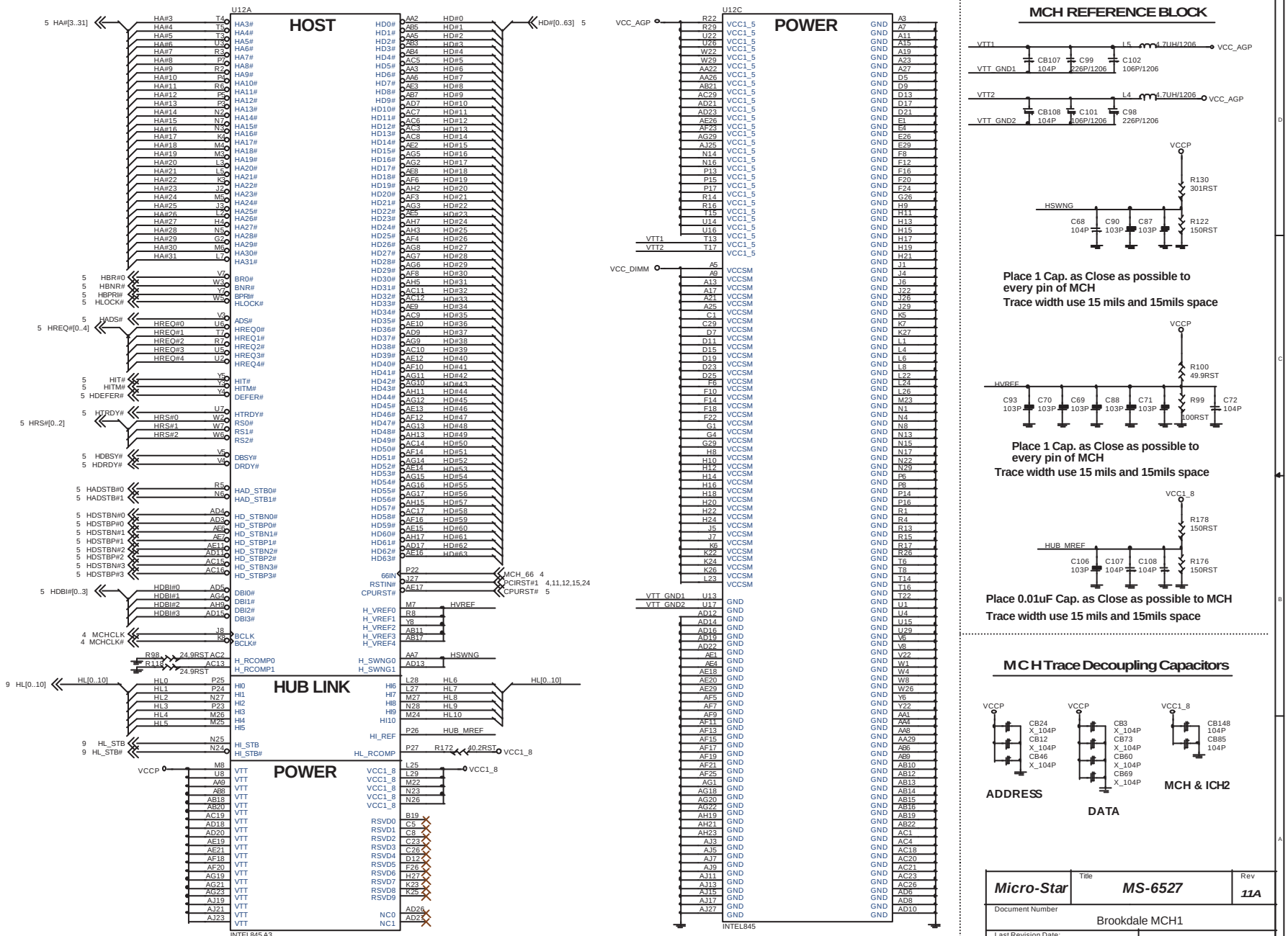
PLACE CAPS WITHIN CPU CAVITY

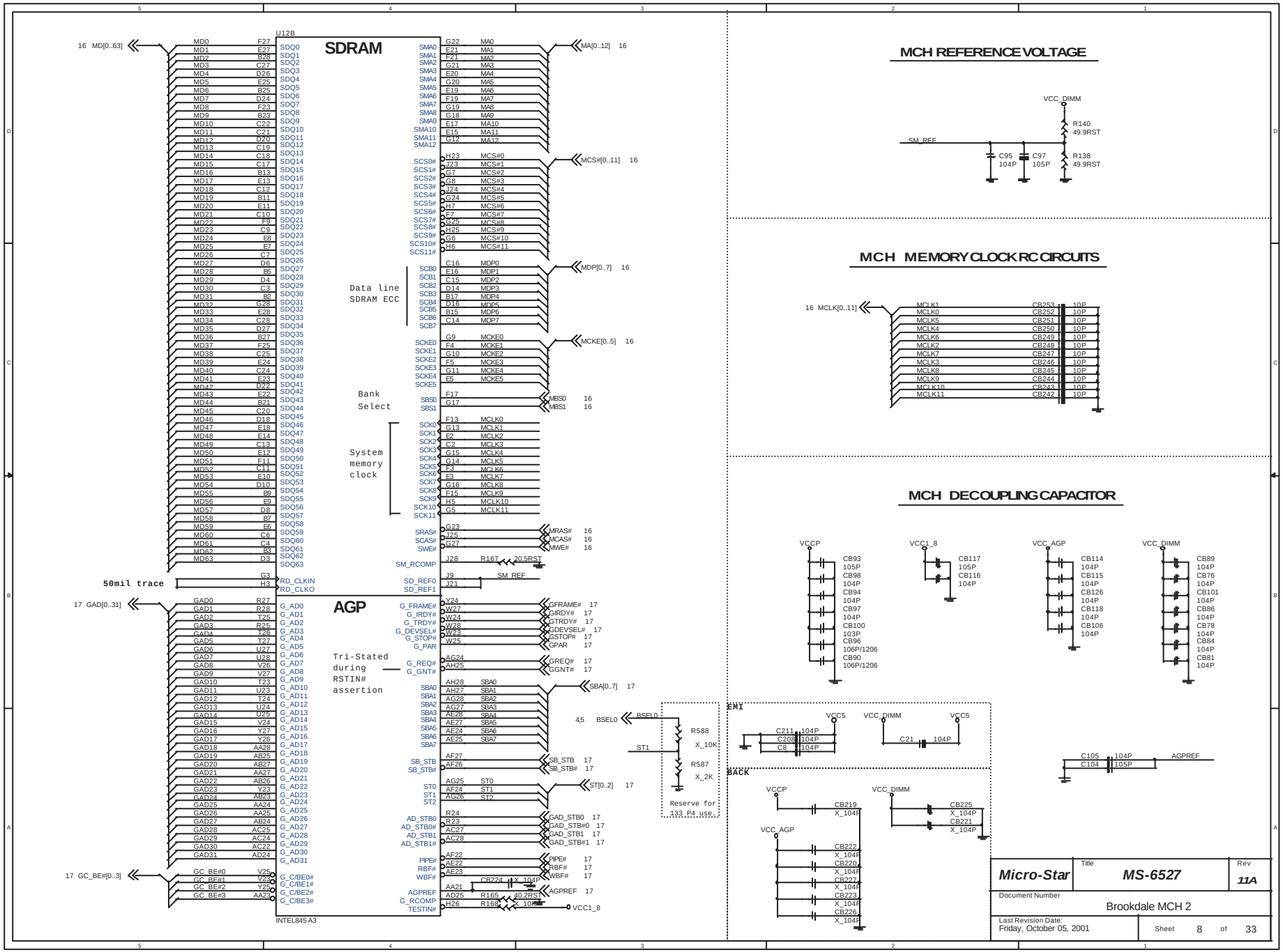
CPU DECOUPLING CAPACITORS



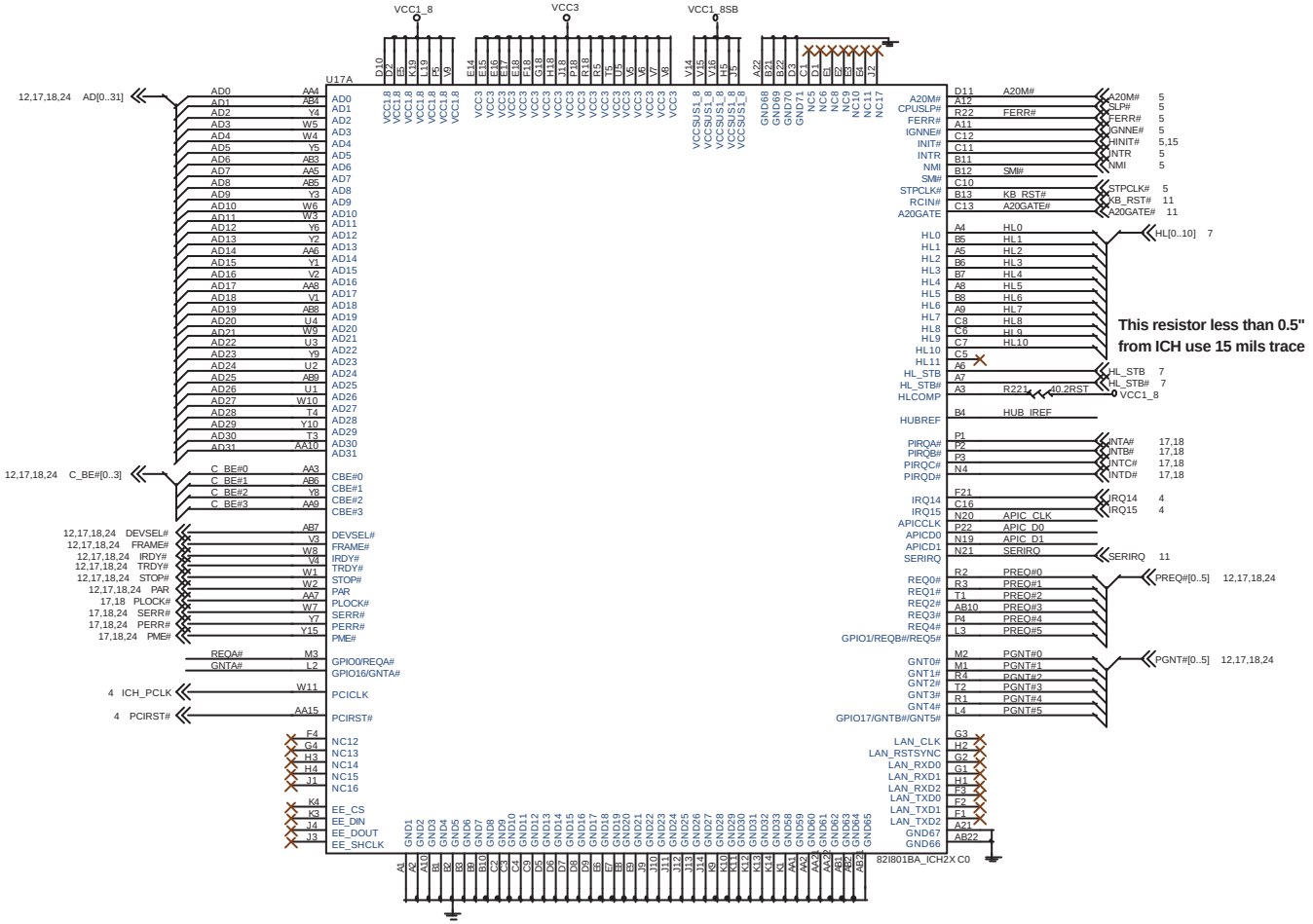
PLACE CAPS WITHIN CPU CAVITY SOLDER

Micro-Star	Title: MS-6527	Rev: 11A
Document Number: INTEL mPGA478-B CPU2		
Last Revision Date: Friday, October 05, 2001	Sheet 6 of 33	

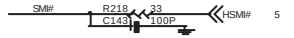

U12A
HOST
HA#[3..31]
HD#[0..63]
HBR#0
HBNR#
HBPRI#
HLOCK#
HADS#
HREQ#[0..4]
HIT#
HITM#
HDEFER#
HTRDY#
HRS#[0..2]
HDBSY#
HDRDY#
HADSTB#0
HADSTB#1
HDSTBN#0
HDSTBP#0
HDSTBN#1
HDSTBP#1
HDSTBN#2
HDSTBP#2
HDSTBN#3
HDSTBP#3
HDBI#[0..3]
MCHCLK
MCHCLK#
R98 24.9RST
R113 24.9RST
HL[0..10]
HL_STB
HL_STB#
VCCP
HUB LINK
POWER
INTEL845 A3
U12C
VCC_AGP
VCC_DIMM
VTT1
VTT2
VTT_GND1
VTT_GND2
HVREF
HSWNG
HUB_MREF
R172 40.2RST
VCC1_8
MCH_66
PCIRST#1 4,11,12,15,24
CPURST# 5
INTEL845
MCH REFERENCE BLOCK
VTT1
VTT2
VTT_GND1
VTT_GND2
VCC_AGP
L5 4.7UH/1206
L4 4.7UH/1206
CB107 104P
C99 226P/1206
C102 106P/1206
CB108 104P
C101 106P/1206
C98 226P/1206
VCCP
R130 301RST
HSWNG
C68 104P
C90 103P
C87 103P
R122 150RST
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
R100 49.9RST
HVREF
C93 103P
C70 103P
C69 103P
C88 103P
C71 103P
R99 100RST
C72 104P
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCC1_8
R178 150RST
HUB_MREF
C106 103P
C107 104P
C108 104P
R176 150RST
Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space
MCH Trace Decoupling Capacitors
VCCP
CB24 X_104P
CB12 X_104P
CB46 X_104P
ADDRESS
VCCP
CB3 X_104P
CB73 X_104P
CB60 X_104P
CB69 X_104P
DATA
VCC1_8
CB148 104P
CB85 104P
MCH & ICH2
Micro-Star
Title
MS-6527
Rev
11A
Document Number
Brookdale MCH1
Last Revision Date:
Friday, October 05, 2001
Sheet 7 of 33


U12B
SDRAM
AGP
Data line SDRAM ECC
Bank Select
System memory clock
Tri-Stated during RSTIN# assertion
50mil trace
INTEL845 A3
MCH REFERENCE VOLTAGE
VCC_DIMM
R140 49.9RST
SM_REF
C95 104P
C97 105P
R138 49.9RST
MCH MEMORY CLOCK RC CIRCUITS
MCH DECOUPLING CAPACITOR
VCCP
VCC1_8
VCC_AGP
VCC_DIMM
EMI
BACK
Reserve for 133 P4 use.
Micro-Star
MS-6527
11A
Brookdale MCH 2
Friday, October 05, 2001
Sheet 8 of 33

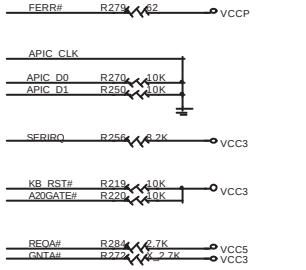
ICH2 PCI / HUB LINK / CPU/LAN/INTERRUPT SIGNALS



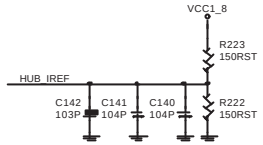
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

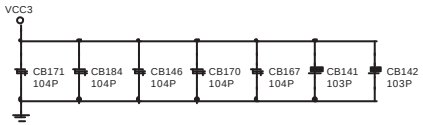


ICH2 REFERENCE VOLTAGE

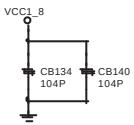


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

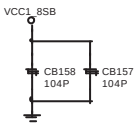
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and
2 on opposite sides close to ICH2 if it fit



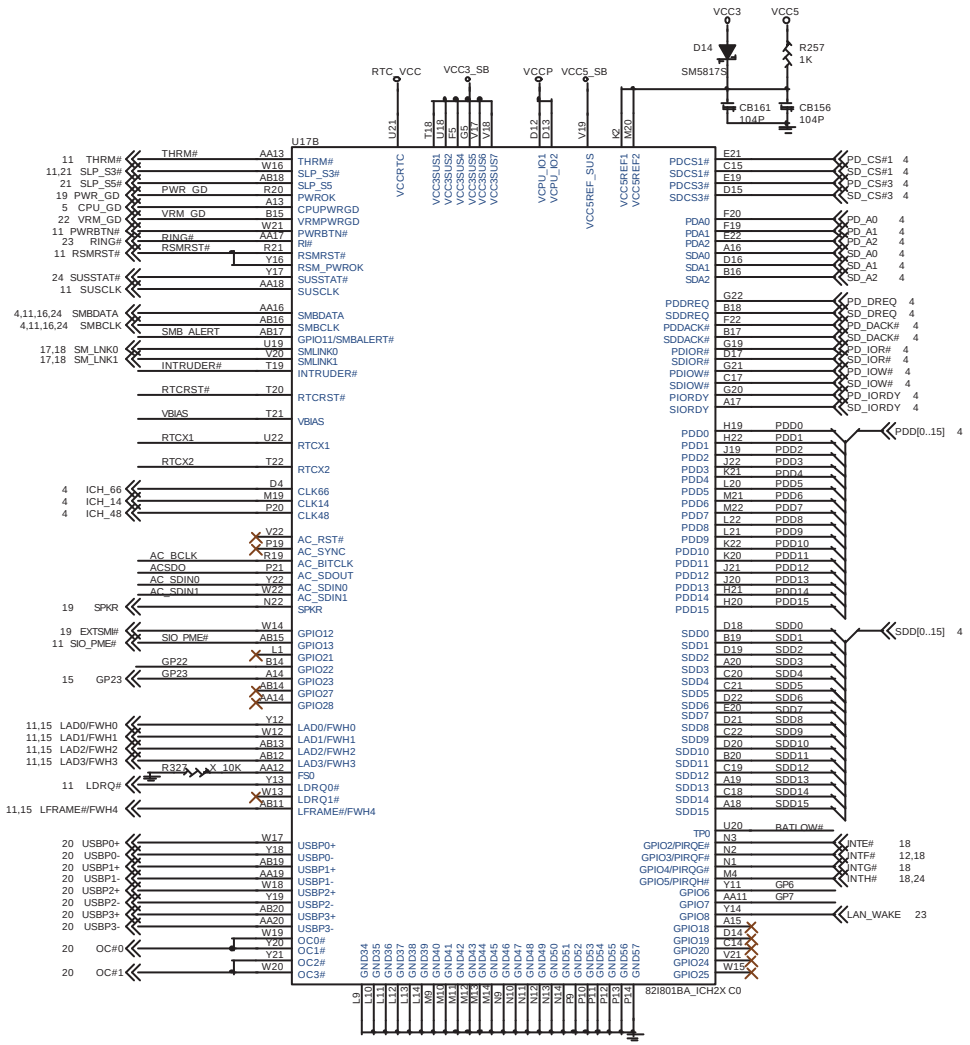
Distribute near the 1.8V
power pin of the ICH2



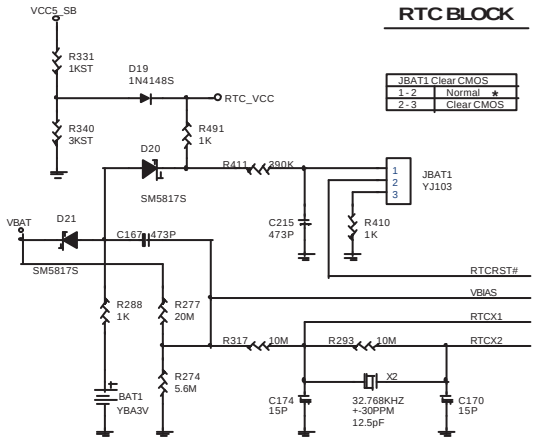
Distribute near the VCC1_8SB
Power pin of the ICH2

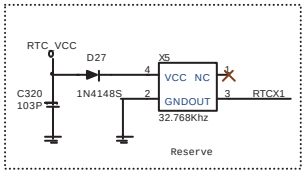
Micro-Star	Title: MS-6527	Rev: 11A
Document Number: Brookdale ICH2 PCI		
Last Revision Date: Friday, October 05, 2001	Sheet 9 of 33	

ICH2 ASIC / RTC / AC'97/GPIO/LPC/USB/IDE SIGNALS

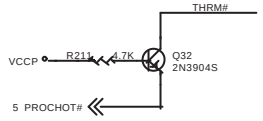


RTC BLOCK

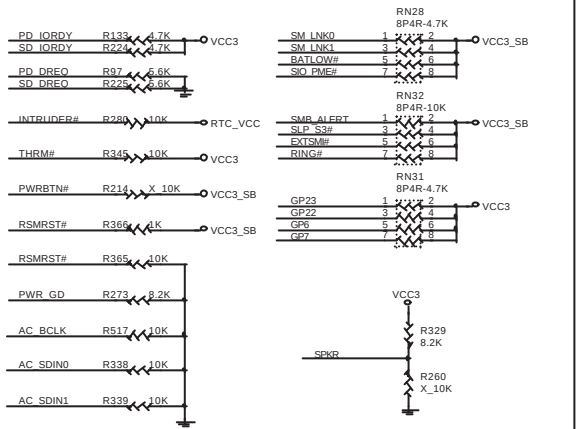




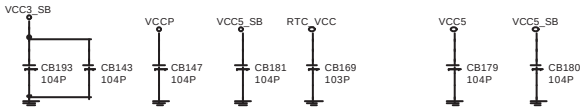
PROCHOT BLOCK



ICH2 STRAPPING RESISTORS

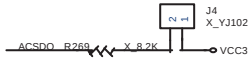


ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

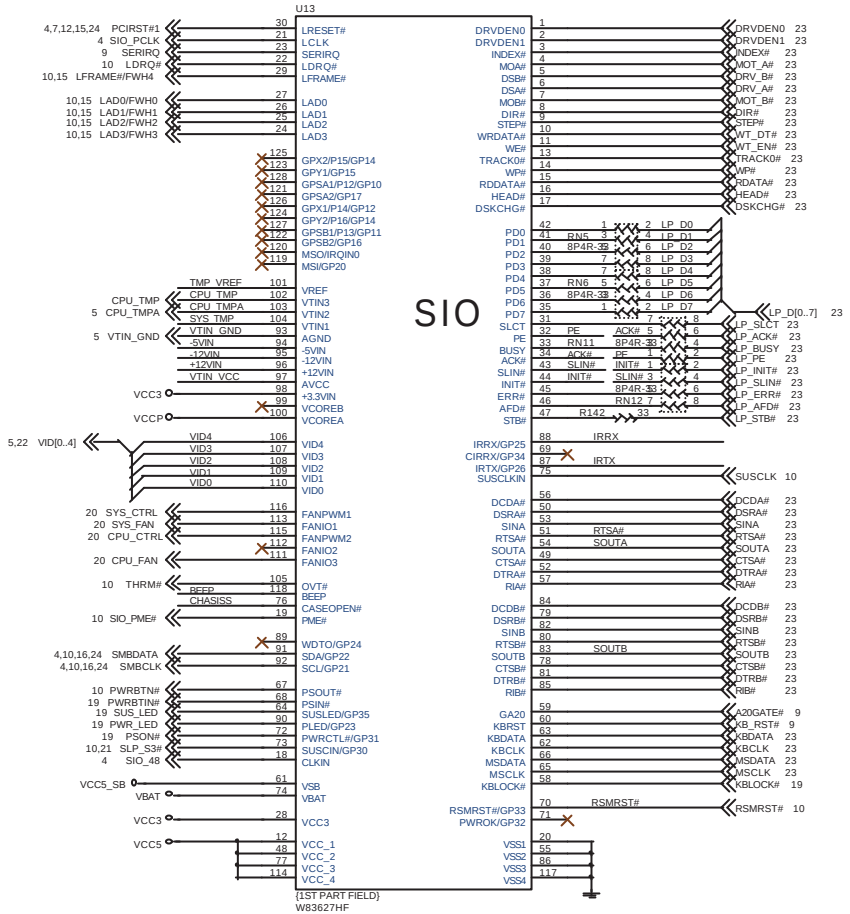
CPU ratio safe mode strapping



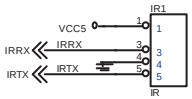
Short	Safe Mode
Open	Normal

Micro-Star	Title: MS-6527		Rev: 11A
	Document Number: Brookdale ICH2 Other		
	Last Revision Date: Friday, October 05, 2001	Sheet 10 of 33	

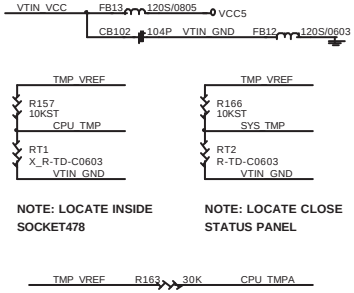
LPC SUPER I/O W83627HF



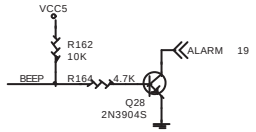
IR HEADER



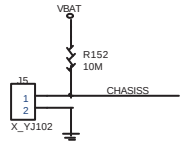
THERMAL RESISTOR BLOCK



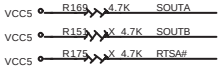
SPEAKER BLOCK



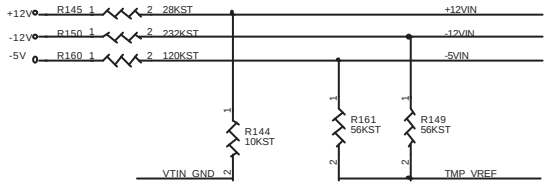
CHASISS INTRUSION HEADER



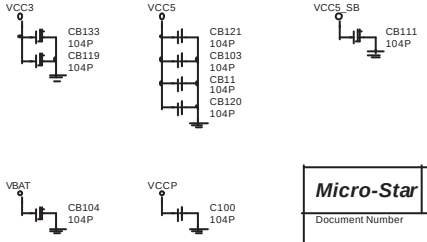
SUPER I/O STRAPPING RESISTOR



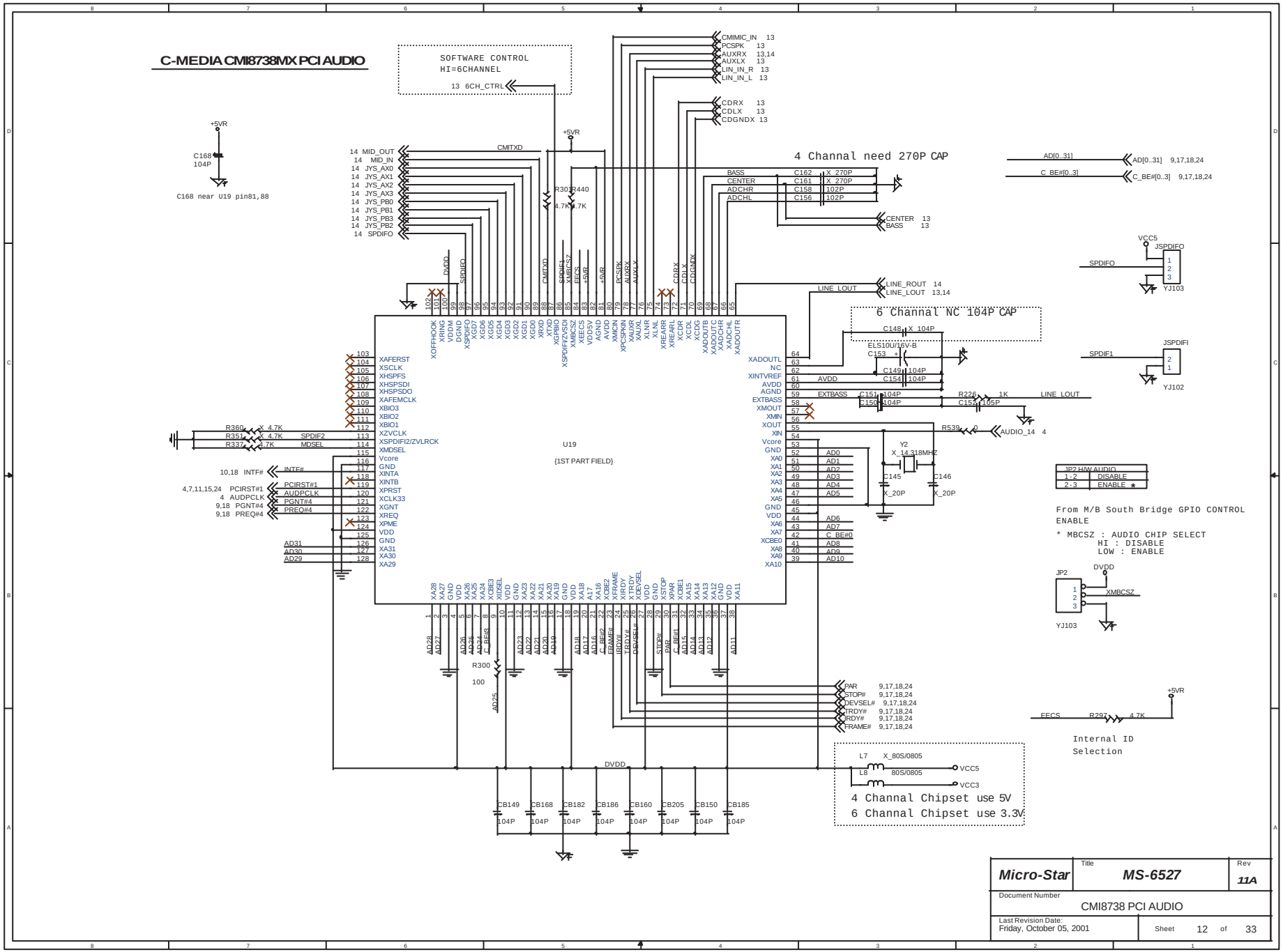
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

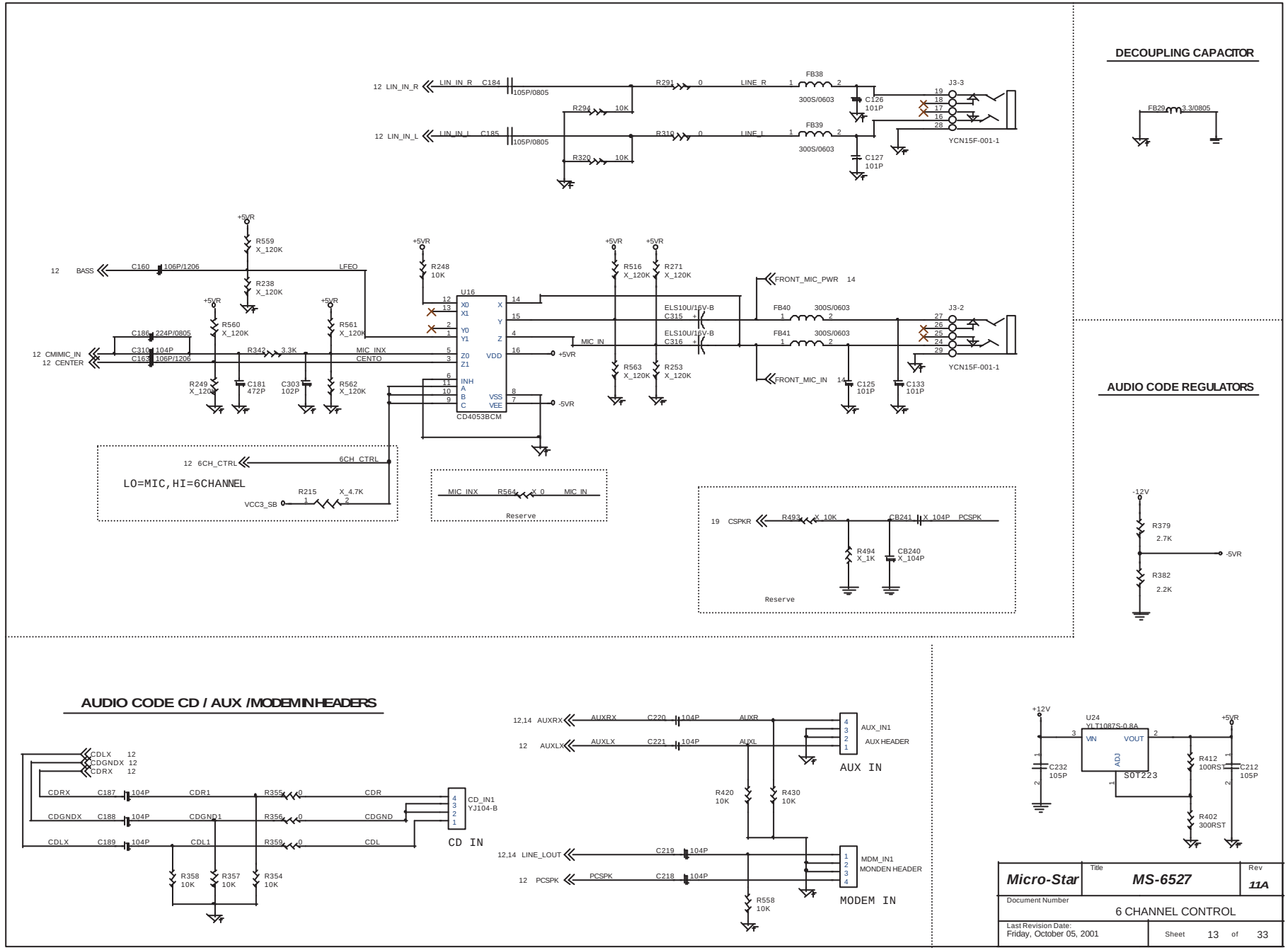


DECOUPLING CAPACITOR

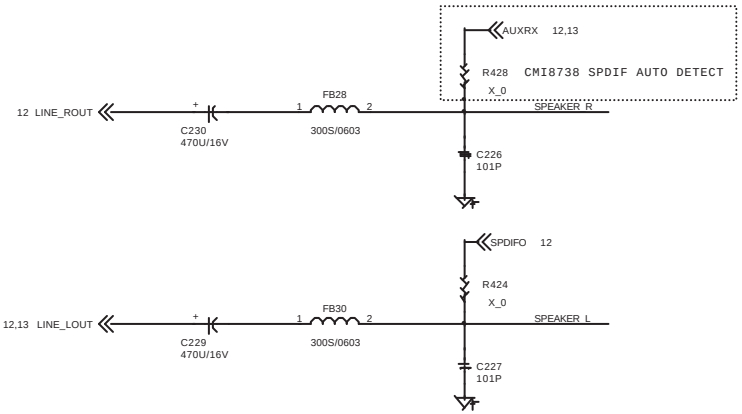


Micro-Star	Title: MS-6527	Rev: 11A
Document Number: LPC I/O W83627HF		
Last Revision Date: Friday, October 05, 2001	Sheet 11 of 33	

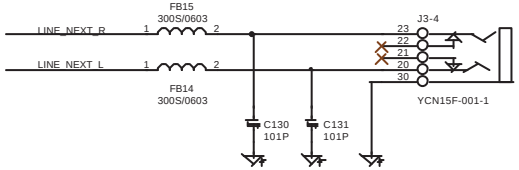

C-MEDIA CMI8738MX PCI AUDIO
SOFTWARE CONTROL
HI=6CHANNEL
13 6CH_CTRL
CMIMIC_IN 13
PCSPK 13
AUXRX 13,14
AUXLX 13
LIN_IN_R 13
LIN_IN_L 13
CDRX 13
CDLX 13
CDGNDX 13
+5VR
C168
104P
C168 near U19 pin81,88
14 MID_OUT
14 MID_IN
14 JYS_AX0
14 JYS_AX1
14 JYS_AX2
14 JYS_AX3
14 JYS_PB0
14 JYS_PB1
14 JYS_PB3
14 JYS_PB2
14 SPDIFO
CMITXD
R303 R440
4.7K 4.7K
4 Channal need 270P CAP
BASS C162 X 270P
CENTER C161 X 270P
ADCHR C158 102P
ADCHL C156 102P
CENTER 13
BASS 13
AD[0..31]
AD[0..31] 9,17,18,24
C_BE#[0..3]
C_BE#[0..3] 9,17,18,24
VCC5
JSPDIFO
SPDIFO
YJ103
LINE_LOUT
LINE_ROUT 14
LINE_LOUT 13,14
6 Channal NC 104P CAP
C148 X 104P
ELS10U/16V-B
C153
C149 104P
C154 104P
AVDD
EXTBASS
C151 104P
C150 104P
R226 1K
C152 105P
LINE_LOUT
JSPDIFI
SPDIF1
YJ102
R539 0
AUDIO_14 4
Y2
X_14.318MHZ
C145 X_20P
C146 X_20P
JP2 H/W AUDIO
1-2 DISABLE
2-3 ENABLE *
From M/B South Bridge GPIO CONTROL
ENABLE
* MBCSZ : AUDIO CHIP SELECT
HI : DISABLE
LOW : ENABLE
JP2
DVDD
XMBCSZ
YJ103
R360 X 4.7K
R351 X 4.7K SPDIF2
R337 4.7K MDSEL
10,18 INTF#
4,7,11,15,24 PCIRST#1
4 AUDPCLK
9,18 PGNT#4
9,18 PREQ#4
AD31
AD30
AD29
U19
{1ST PART FIELD}
XOFFHOOK
XRING
VDDA
DGND
XSPDIFO
XGD7
XGD6
XGD5
XGD4
XGD3
XGD2
XGD1
XGD0
XRXD
XTXD
XGPIO
XSPDIFI/ZVSDI
XMBCSZ
XEECS
VDD5V
AGND
AVDD
XMCIN
XPCSPKIN
XAUXR
XAUXL
XLINR
XLINL
XREARR
XREARL
XCDR
XCDL
XCDG
XADOUTB
XADOUTR
XADCHR
XADCHL
XADOUTR
XAFERST
XSCLK
XHSPFS
XHSPSDI
XHSPSDO
XAFEMCLK
XBIO3
XBIO2
XBIO1
XZVCLK
XSPDIFI2/ZVLRCK
XMDSEL
Vcore
GND
XINTA
XINTB
XPRST
XCLK33
XGNT
XREQ
XPME
VDD
GND
XA31
XA30
XA29
XADOUTL
NC
XINTVREF
AVDD
AGND
EXTBASS
XMOUT
XMIN
XOUT
XIN
Vcore
GND
XA0
XA1
XA2
XA3
XA4
XA5
GND
VDD
XA6
XA7
XCBE0
XA8
XA9
XA10
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
C_BE#0
AD8
AD9
AD10
XA28
XA27
GND
VDD
XA26
XA25
XA24
XCBE3
XIDSEL
VDD
GND
XA23
XA22
XA21
XA20
XA19
GND
VDD
XA18
A17
XA16
XCBE2
XFRAME
XIRDY
XTRDY
XDEVSEL
GND
VDD
XSTOP
XPAR
XCBE1
XA15
XA14
XA13
XA12
GND
VDD
XA11
AD28
AD27
AD26
AD25
C_BE#3
IDSEL
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
C_BE#2
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
C_BE#1
AD15
AD14
AD13
AD12
AD11
R300
100
PAR 9,17,18,24
STOP# 9,17,18,24
DEVSEL# 9,17,18,24
TRDY# 9,17,18,24
IRDY# 9,17,18,24
FRAME# 9,17,18,24
DVDD
CB149 104P
CB168 104P
CB182 104P
CB186 104P
CB160 104P
CB205 104P
CB150 104P
CB185 104P
L7 X_80S/0805
L8 80S/0805
VCC5
VCC3
4 Channal Chipset use 5V
6 Channal Chipset use 3.3V
FECS
R297 4.7K
Internal ID
Selection
Micro-Star
Title
MS-6527
Rev
11A
Document Number
CMI8738 PCI AUDIO
Last Revision Date:
Friday, October 05, 2001
Sheet 12 of 33


DECOUPLING CAPACITOR
FB29 3.3/0805
AUDIO CODE REGULATORS
-12V
R379
2.7K
-5VR
R382
2.2K
12 LIN_IN_R
LIN_IN_R C184
105P/0805
R291 0
LINE_R
FB38
300S/0603
C126
101P
J3-3
YCN15F-001-1
12 LIN_IN_L
LIN_IN_L C185
105P/0805
R310 0
LINE_L
FB39
300S/0603
C127
101P
R294 10K
R320 10K
+5VR
R559
X_120K
12 BASS
C160 106P/1206
LFEO
R238
X_120K
R560
X_120K
R561
X_120K
C186 224P/0805
C310 104P
C163 106P/1206
12 CMIMIC_IN
12 CENTER
R342 3.3K
MIC_INX
CENTO
R249
X_120K
C181
472P
C303
102P
R562
X_120K
R248
10K
U16
CD4053BCM
R516
X_120K
R271
X_120K
R563
X_120K
R253
X_120K
FRONT_MIC_PWR 14
FB40 300S/0603
FB41 300S/0603
ELS10U/16V-B
C315
C316
MIC_IN
FRONT_MIC_IN 14
C125
101P
C133
101P
J3-2
YCN15F-001-1
12 6CH_CTRL
6CH_CTRL
LO=MIC,HI=6CHANNEL
R215 X_4.7K
VCC3_SB
MIC_INX R564 X_0 MIC_IN
Reserve
19 CSPKR
R493 X_10K
CB241 X_104P PCSPK
R494
X_1K
CB240
X_104P
Reserve
AUDIO CODE CD / AUX /MODEMINHEADERS
CDLX 12
CDGNDX 12
CDRX 12
CDRX C187 104P CDR1 R355 0 CDR
CDGNDX C188 104P CDGND1 R356 0 CDGND
CDLX C189 104P CDL1 R359 0 CDL
CD_IN1
YJ104-B
CD IN
R358
10K
R357
10K
R354
10K
12,14 AUXRX
AUXRX C220 104P AUXR
12 AUXLX
AUXLX C221 104P AUXL
AUX_IN1
AUX HEADER
AUX IN
R420
10K
R430
10K
12,14 LINE_LOUT
C219 104P
12 PCSPK
PCSPK C218 104P
MDM_IN1
MONDEN HEADER
MODEM IN
R558
10K
+12V
U24
YLT1087S-0.8A
VIN
VOUT
ADJ
SOT223
C232
105P
R412
100RST
C212
105P
R402
300RST
Micro-Star
Title
MS-6527
Rev
11A
Document Number
6 CHANNEL CONTROL
Last Revision Date:
Friday, October 05, 2001
Sheet 13 of 33

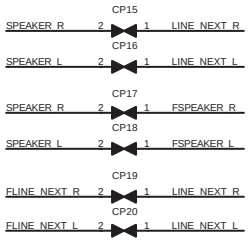
SPEAKER OUT CIRCUIT

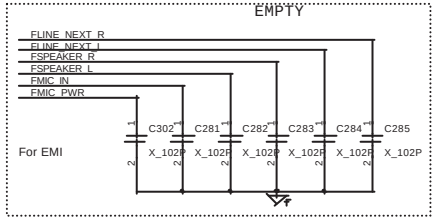


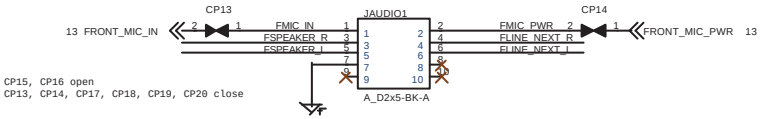
SPEAKER OUT JACK

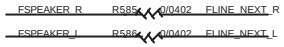


FOR MSI INTERNALHEADER



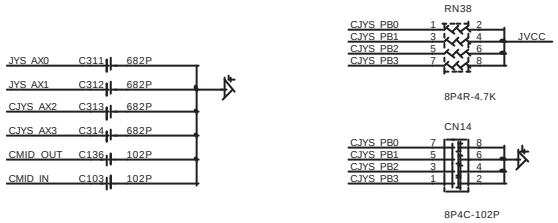


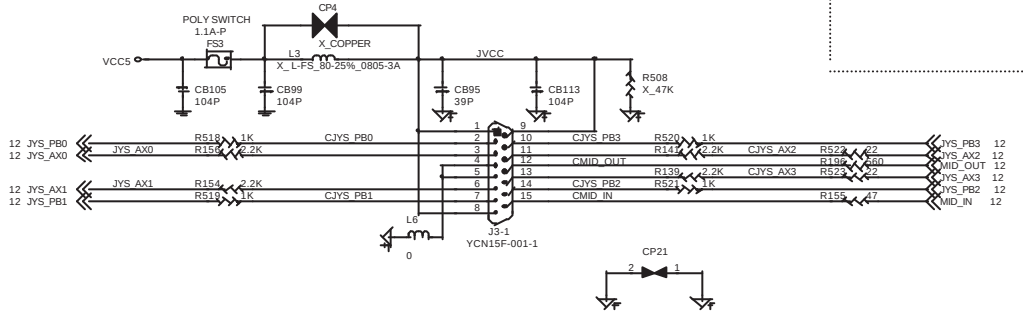




Part	R585	R586	Jaudio1	C281	C282	C283	C284	C285	C302
Stardand	0	0	X	X	X	X	X	X	X
Opt:A	X	X	0	X	X	X	X	X	X

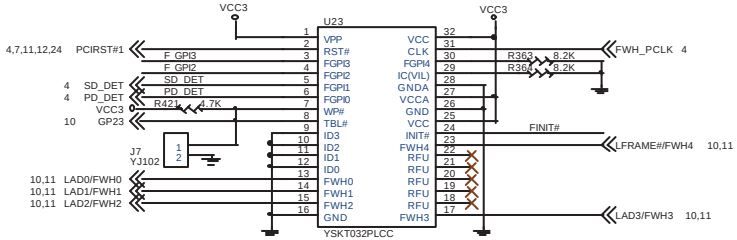
GAME/MIDI CONNECTOR





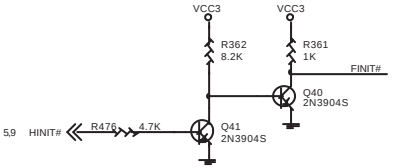
Micro-Star	Title: MS-6527	Rev: 11A
	Document Number: Front Audio & GAME	
Last Revision Date: Friday, October 05, 2001	Sheet 14 of 33	

FirwareHub(FWH)

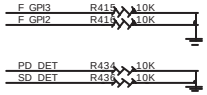


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

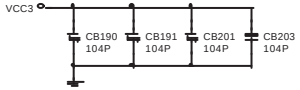
FWH INIT Signal Voltage Translation Block



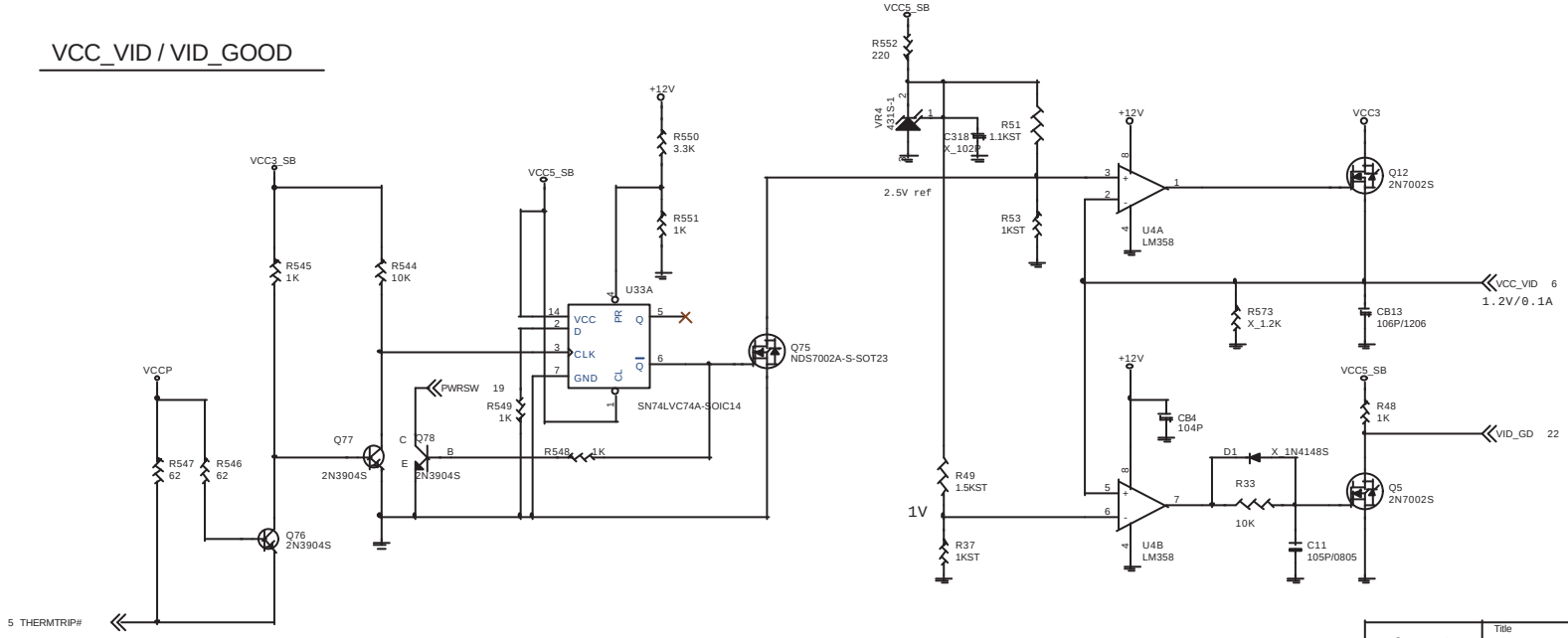
FWH RESISTORS



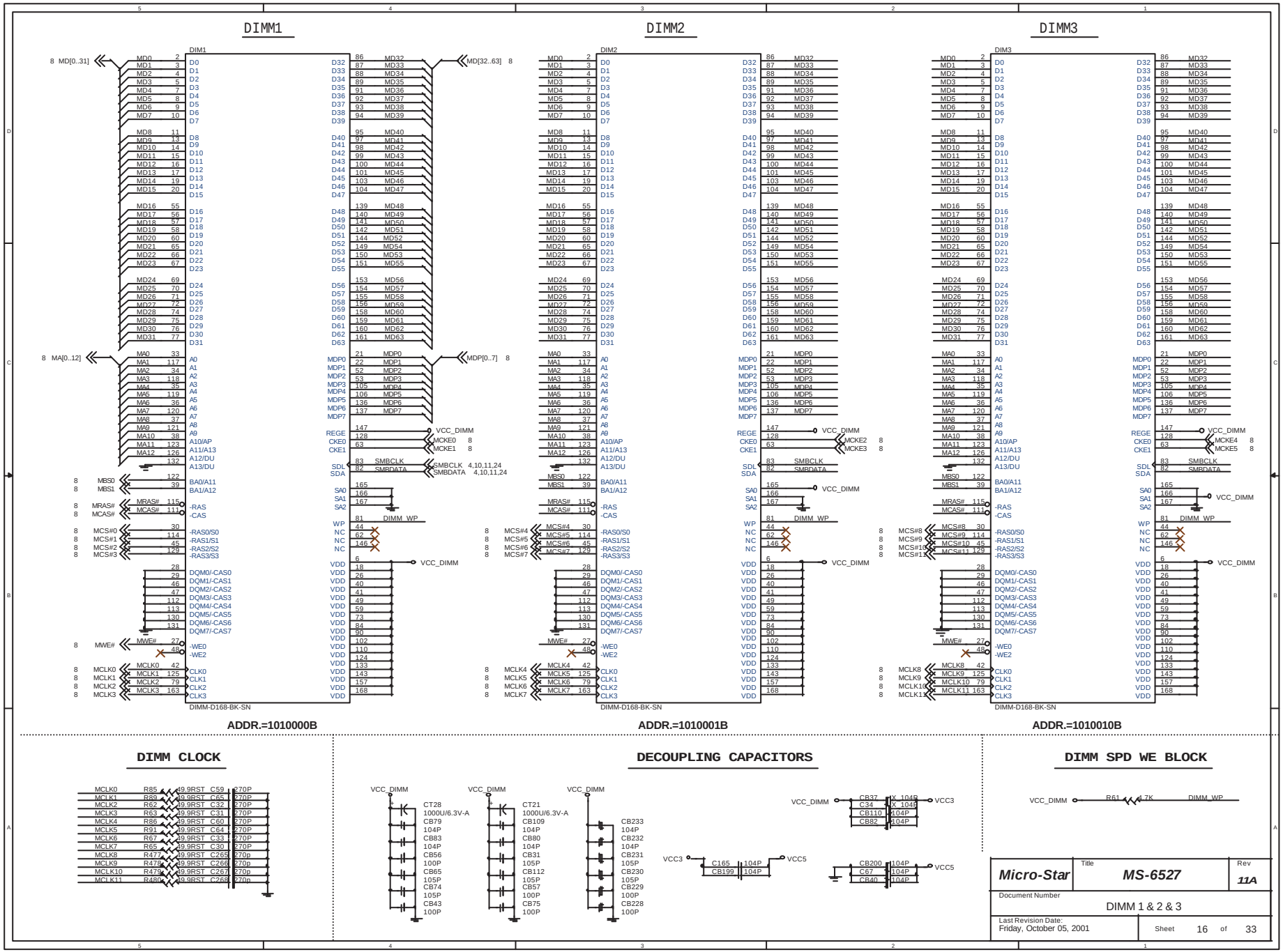
FWH DECOUPLING CAPACITORS



VCC_VID / VID_GOOD

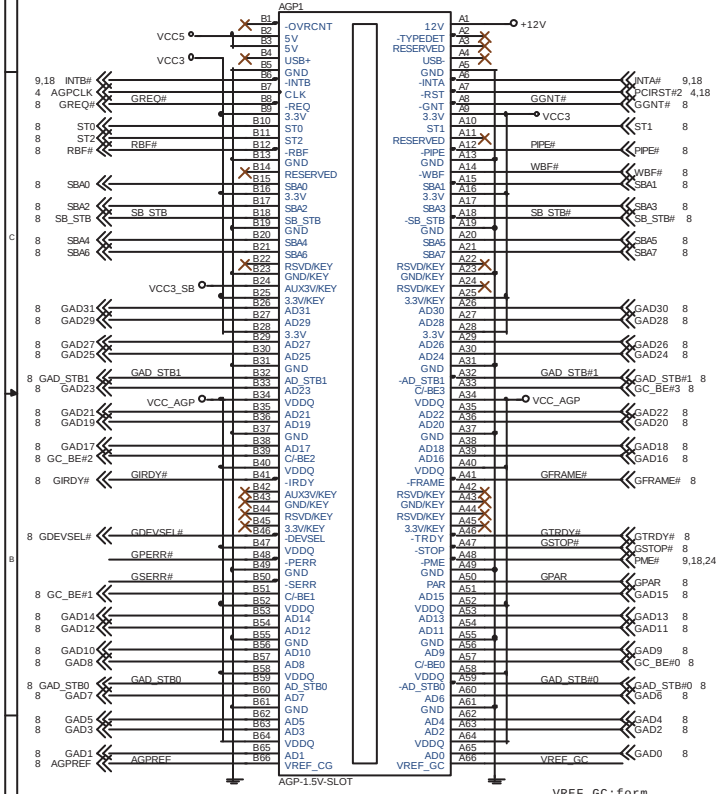


Micro-Star	Title: MS-6527		Rev: 11A
Document Number: FWH & VCC/VID Good			
Last Revision Date: Friday, October 05, 2001		Sheet 15 of 33	


DIMM1
DIMM2
DIMM3
DIMM-D168-BK-SN
ADDR.=1010000B
ADDR.=1010001B
ADDR.=1010010B
DIMM CLOCK
DECOUPLING CAPACITORS
DIMM SPD WE BLOCK
Micro-Star
MS-6527
11A
DIMM 1 & 2 & 3
Friday, October 05, 2001
Sheet 16 of 33

AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

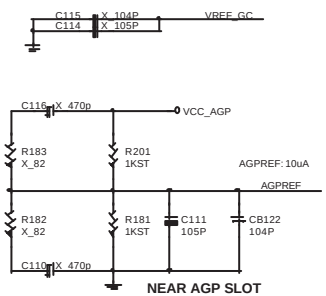
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

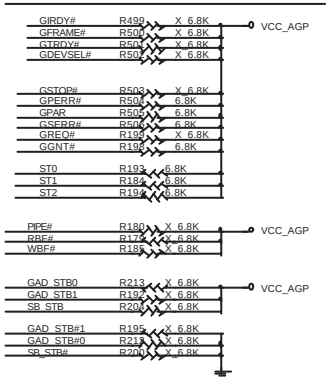
INTA#
INTB#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

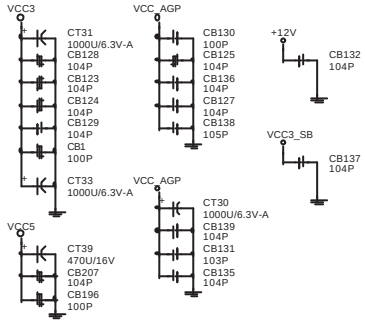
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

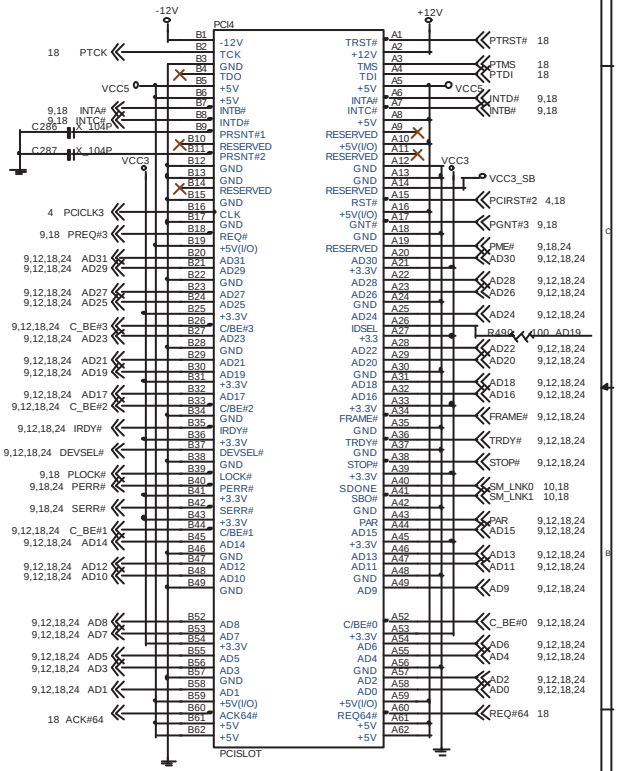
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Part	PCI4	R490
Stardand	0	0
Opt:A	X	X

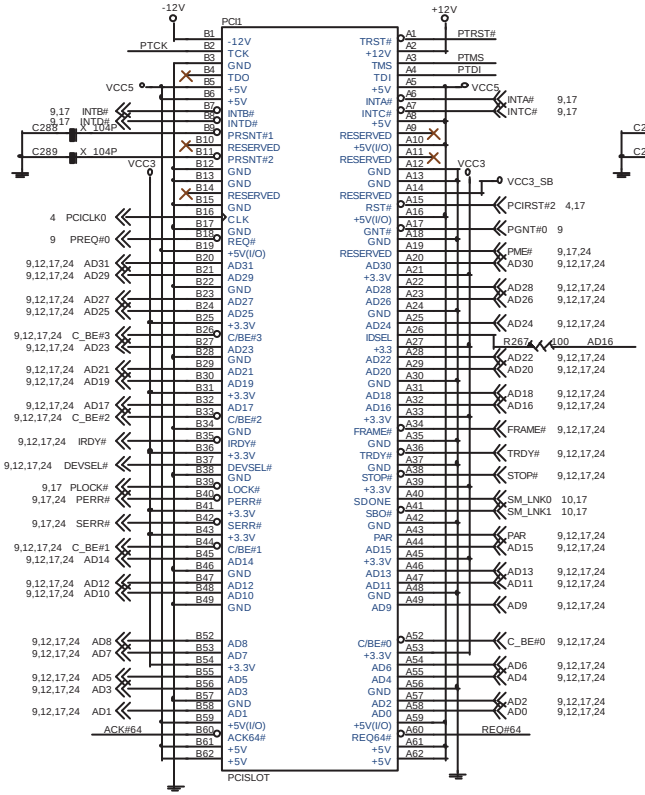
PCI SLOT 4(PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER=PREQ3
INTD#

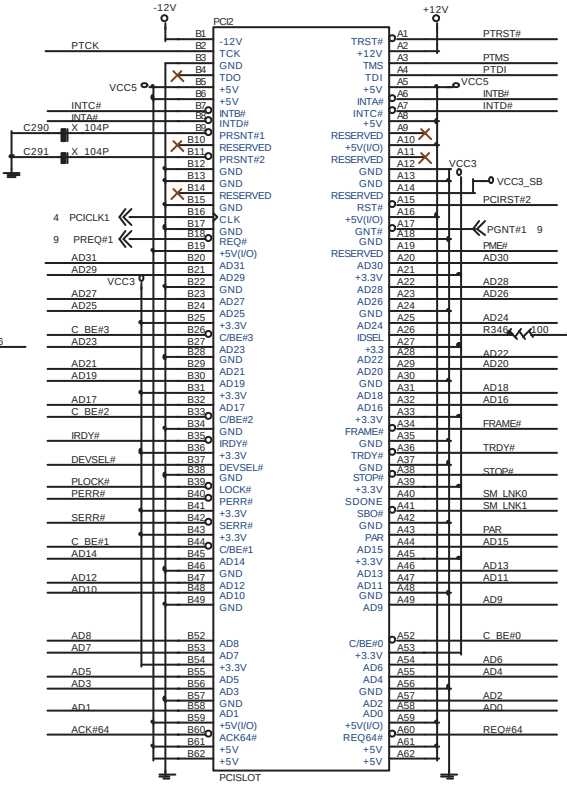
Micro-Star	Title: MS-6527	Rev: 11A
Document Number: AGP Slot & PCI SLOT4		
Last Revision Date: Friday, October 05, 2001	Sheet 17 of 33	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



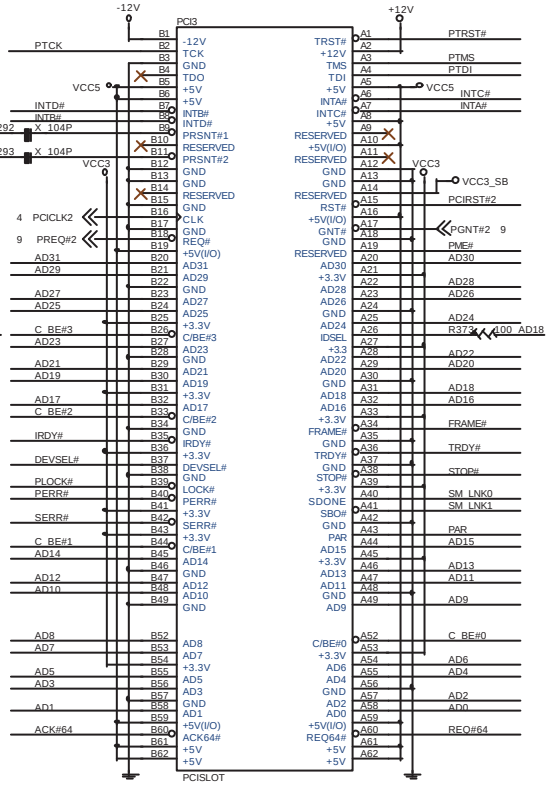
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



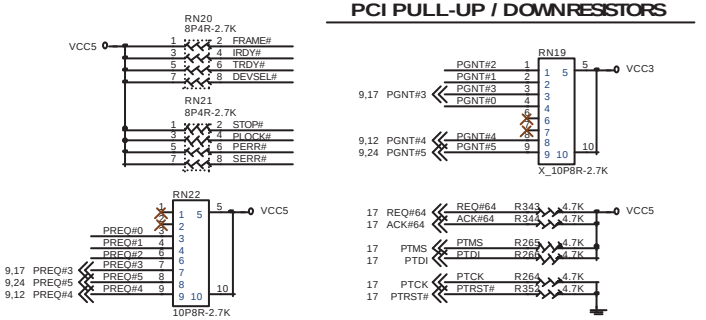
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

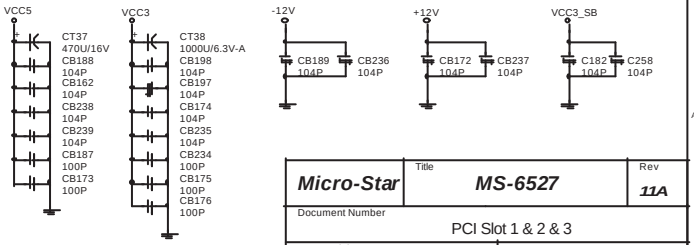


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS

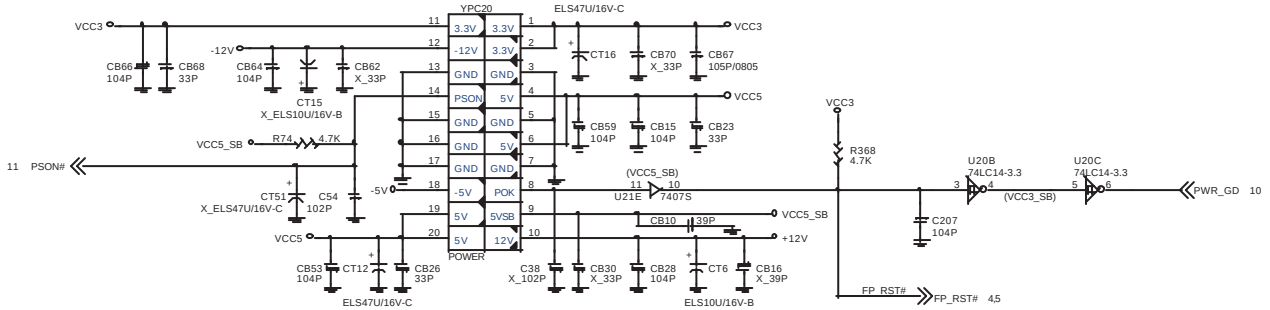


PCI SLOT DECOUPLING CAPACITORS

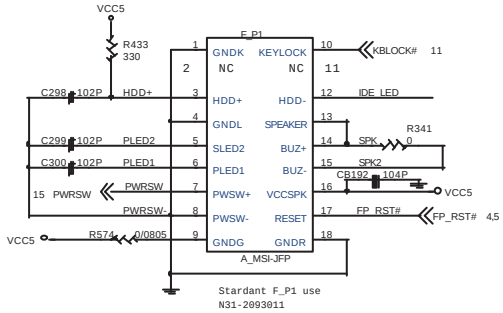


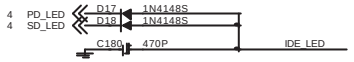
Micro-Star	Title: MS-6527	Rev: 11A
Document Number: PCI Slot 1 & 2 & 3		
Last Revision Date: Friday, October 05, 2001	Sheet 18 of 33	

ATX CONNECTOR

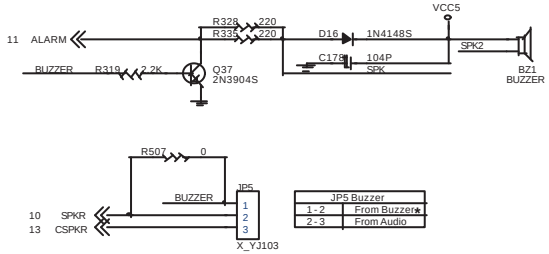


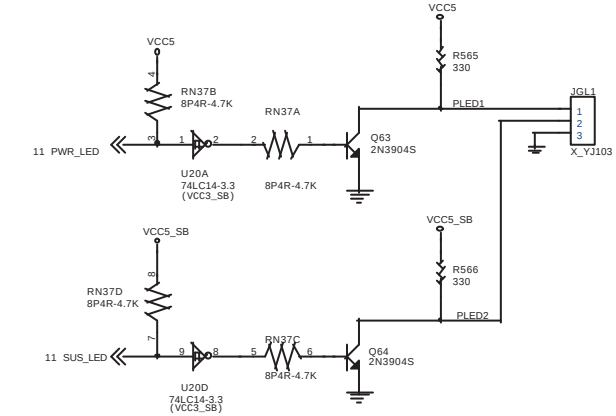
BrookdaleFRONTPANEL-M

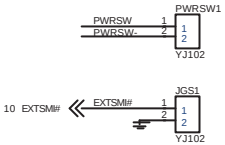




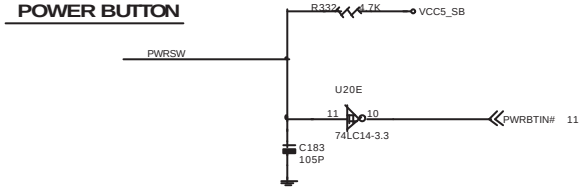
SPEAKER





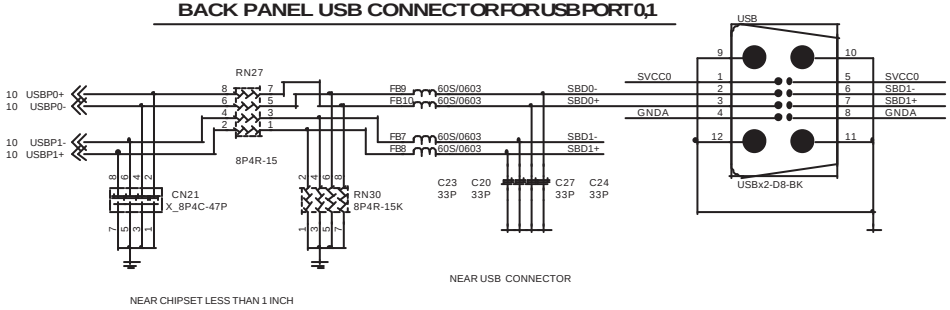


POWER BUTTON

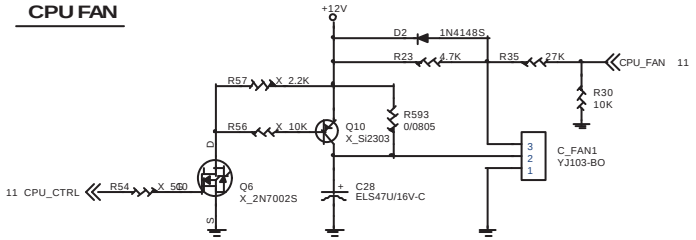


Micro-Star	Title: MS-6527	Rev: 11A
Document Number: Front Panel & Connector		
Last Revision Date: Friday, October 05, 2001	Sheet 19 of 33	

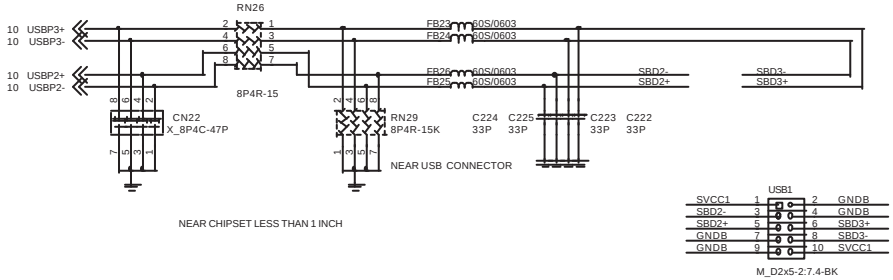
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



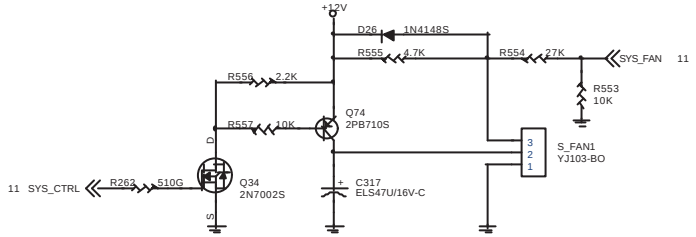
CPU FAN



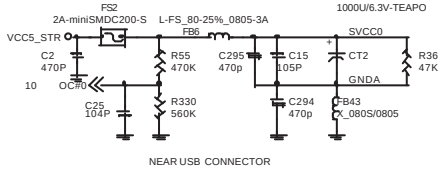
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



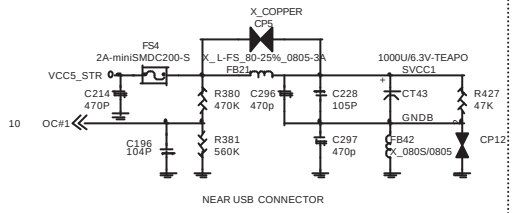
SYSTEM FAN1



POWER CIRCUIT FOR USB PORT 0,1



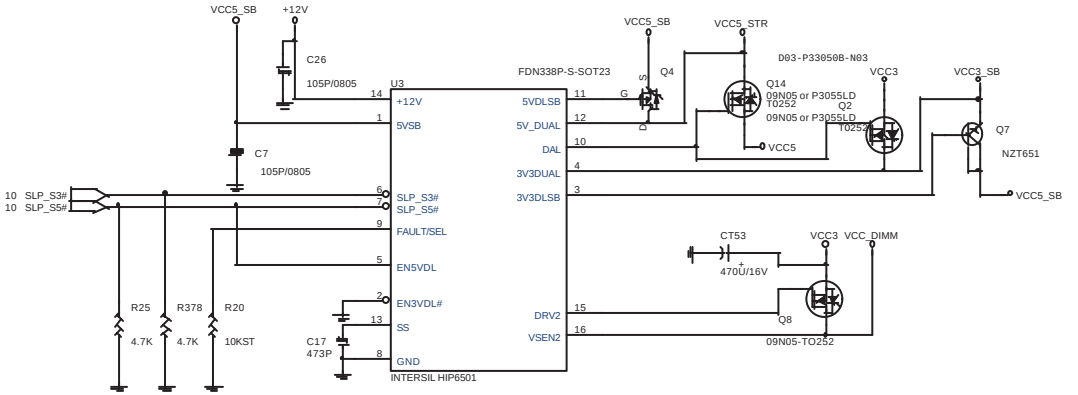
POWER CIRCUIT FOR USB PORT 2,3



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: USB & FAN Connectors		
Last Revision Date: Friday, October 05, 2001	Sheet 20 of 33	

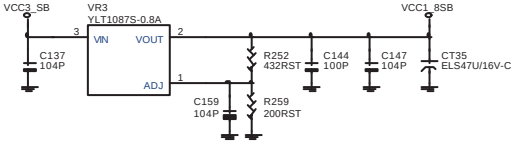
POWER TRANSLATOR

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V



1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH-SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

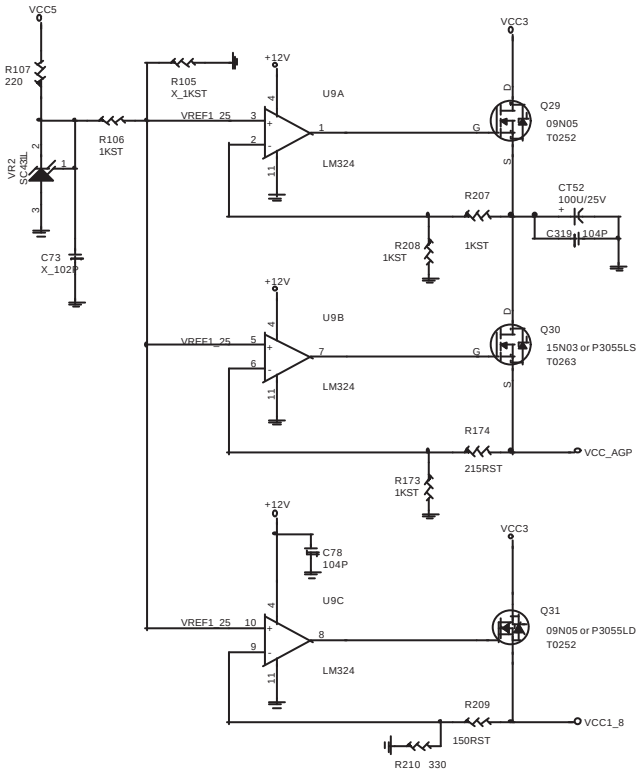
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

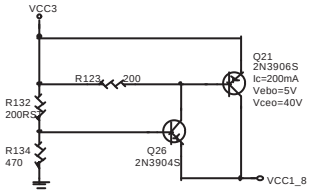
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

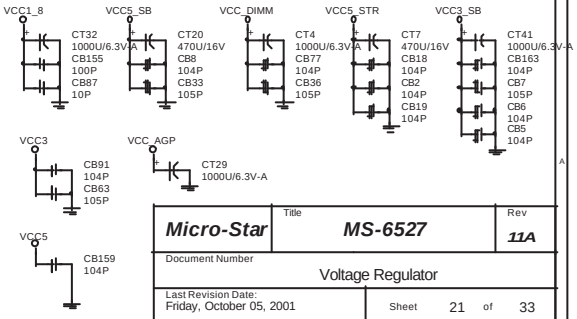
AGP 4X 1.5V POWER TRANSLATOR



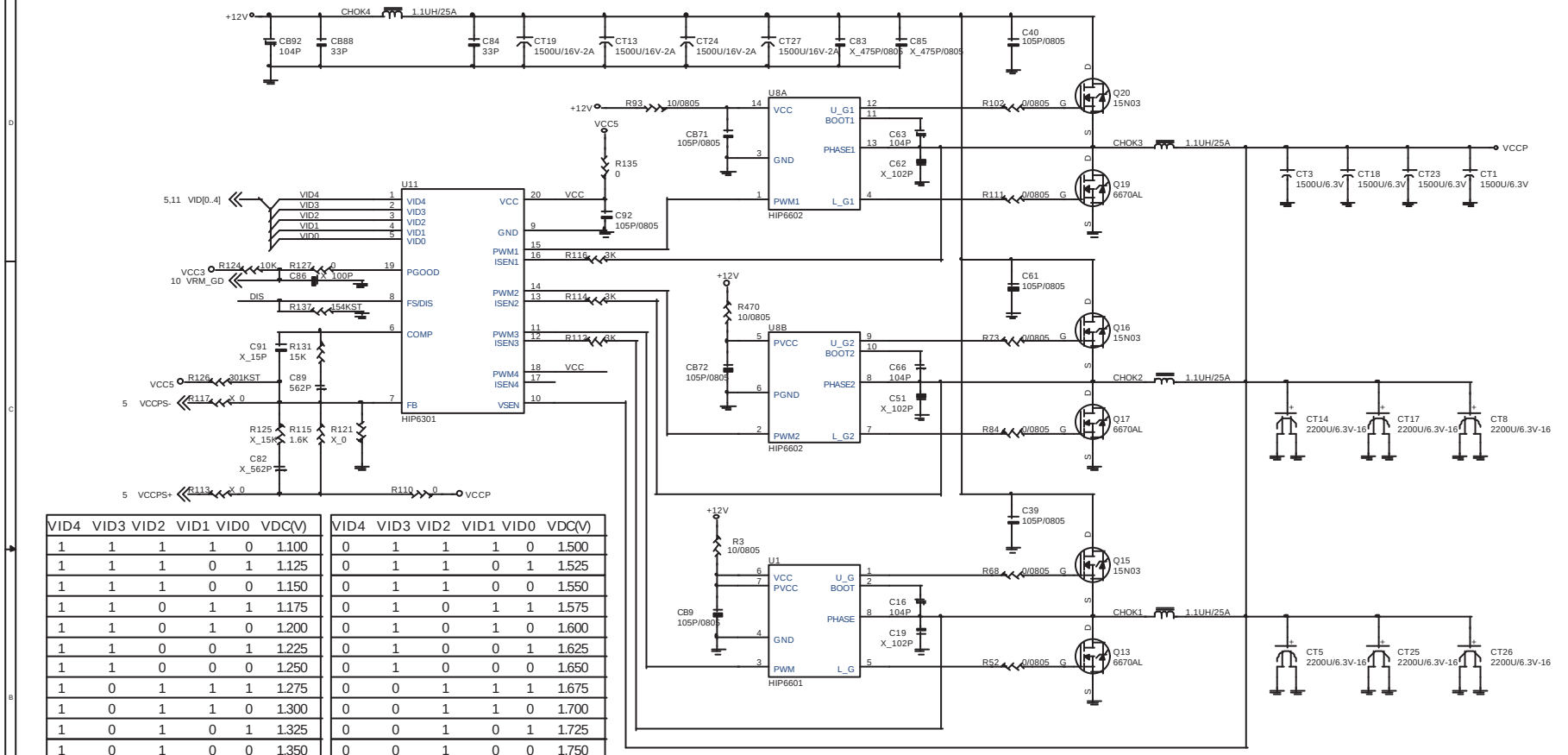
1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: Voltage Regulator		
Last Revision Date: Friday, October 05, 2001	Sheet 21 of 33	

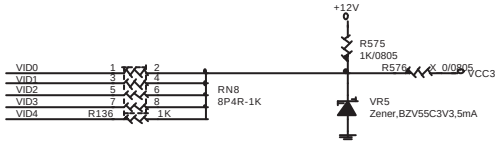


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

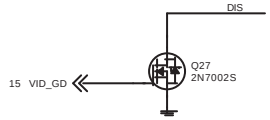
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

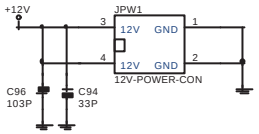
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWMGOOD

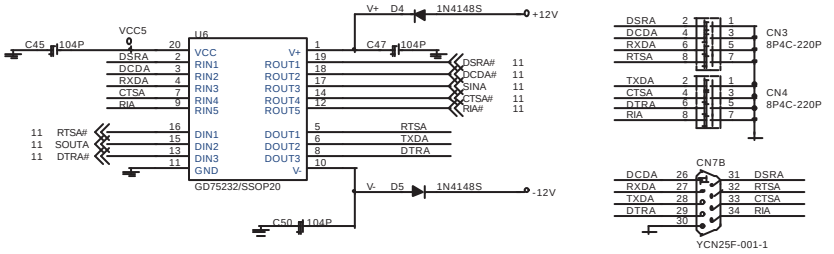


ATX12V POWERCONNECTOR

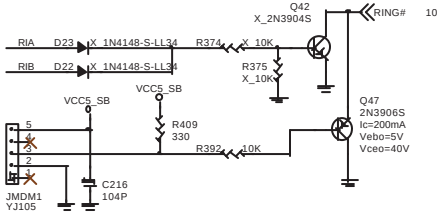


Micro-Star	Title: MS-6527	Rev: 11A
Document Number: VRM 9.2		
Last Revision Date: Friday, October 05, 2001	Sheet 22 of 33	

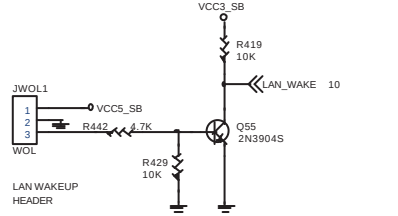
SERIAL PORT1



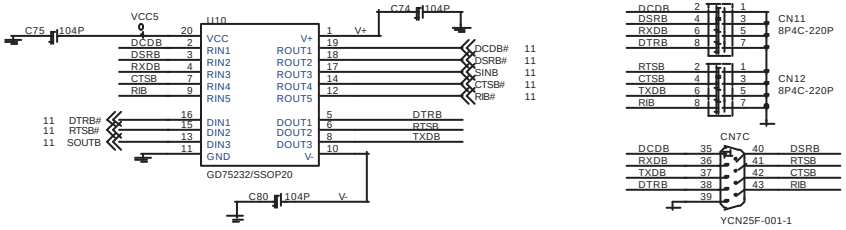
MODEM RING BLOCK



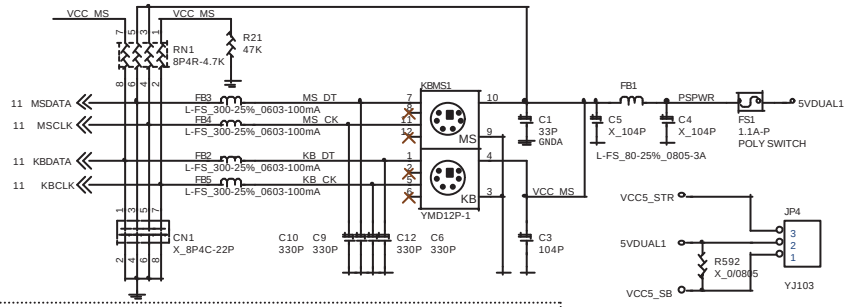
LAN WAKEUP BLOCK



SERIAL PORT2

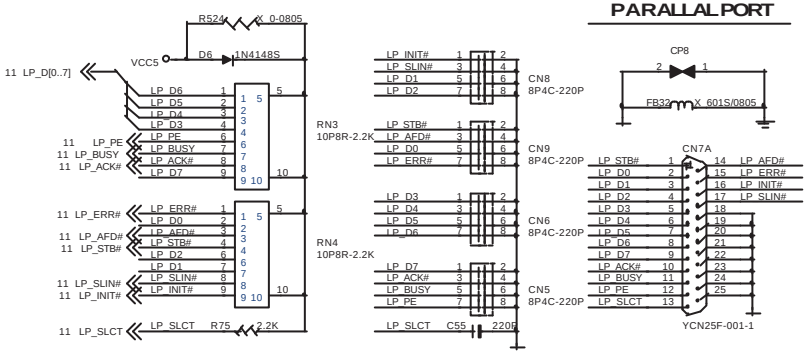


PS2 KEYBOARD & MOUSE CONNECTOR

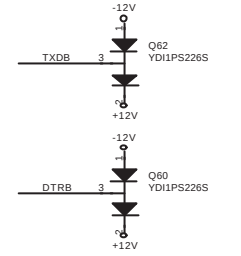


JP4	K/M power on wake up
1-2	S3,S5 both work
2-3	Only S3 work

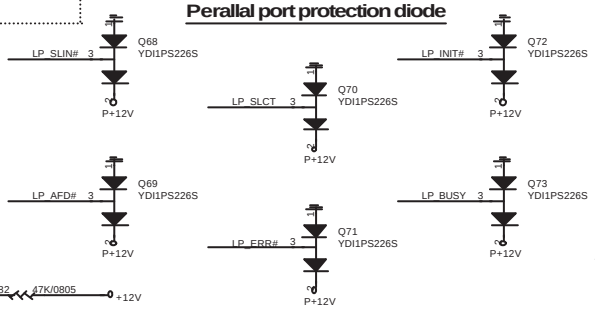
PARALLAL PORT



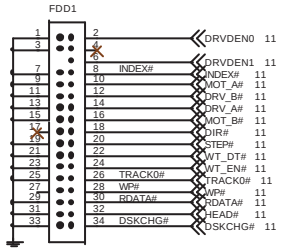
Serial port protection diode



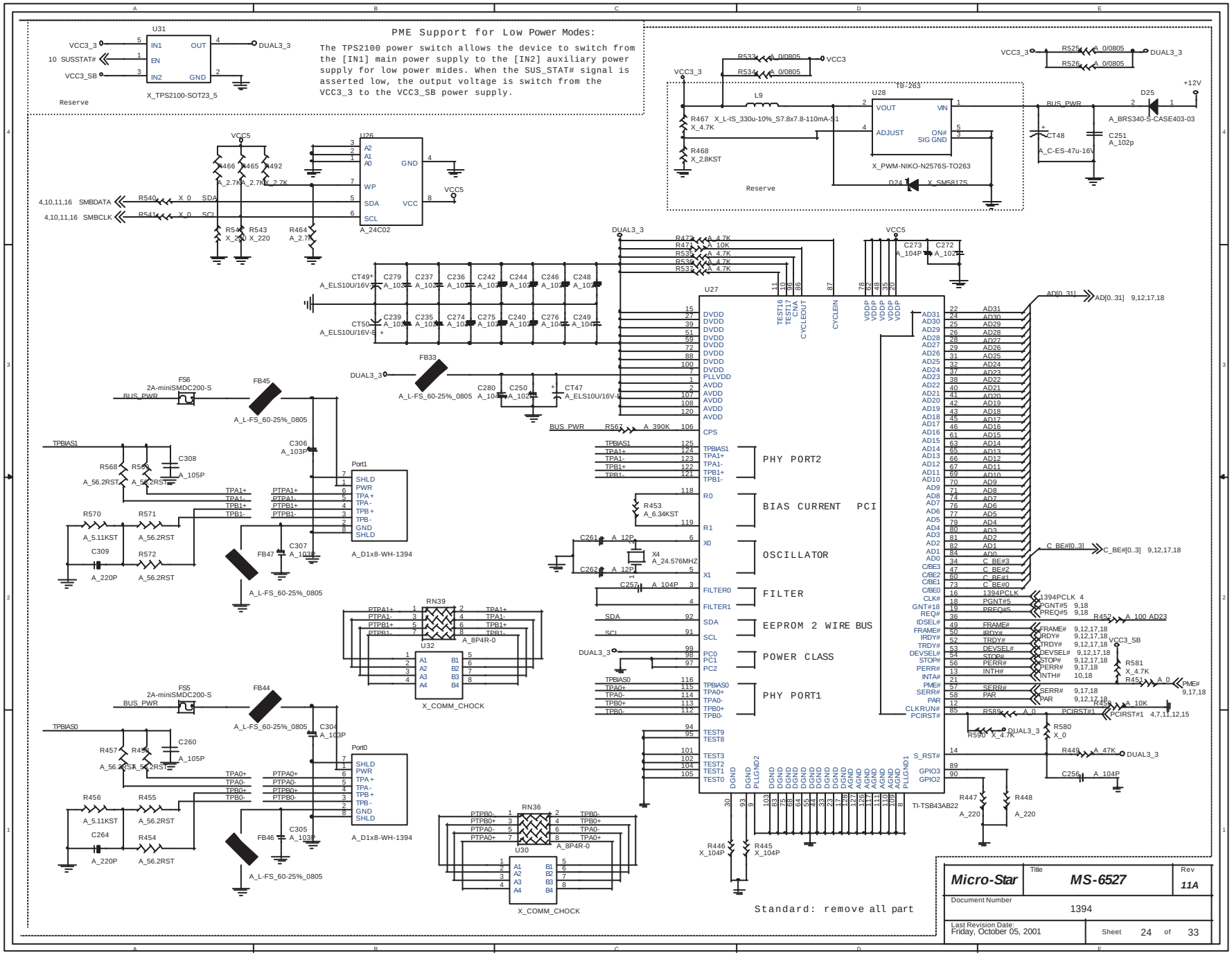
Perallal port protection diode



FLOPPY CONNECTOR



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: IO Connector		
Last Revision Date: Friday, October 05, 2001	Sheet 23 of 33	


PME Support for Low Power Modes:
The TPS2100 power switch allows the device to switch from the [IN1] main power supply to the [IN2] auxiliary power supply for low power mides. When the SUS_STAT# signal is asserted low, the output voltage is switch from the VCC3_3 to the VCC3_SB power supply.
U31
X_TPS2100-SOT23_5
Reserve
U26
A_24C02
U27
PHY PORT2
BIAS CURRENT PCI
OSCILLATOR
FILTER
EEPROM 2 WIRE BUS
POWER CLASS
PHY PORT1
TI-TSB43AB22
U28
X_PWM-NIKO-N2576S-TO263
X_SM5817S
Port1
Port0
A_D1x8-WH-1394
RN39
RN36
U32
U30
X_COMM_CHOCK
Standard: remove all part
Micro-Star
MS-6527
11A
1394
Friday, October 05, 2001
Sheet 24 of 33

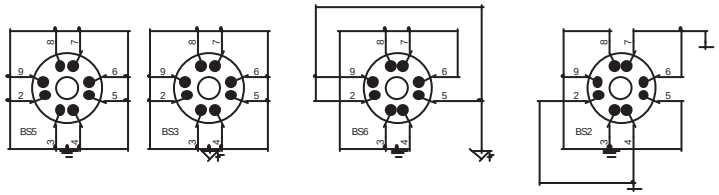
Jumper Setting & Connector Setting

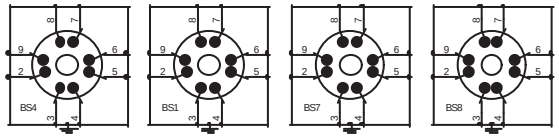
Jumper	Description	
J1	SDR SIMULATION	
J2	AGP SIMULATION	
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	
J4	AC_SDOUT HEADER	
J5	CHASISS INTRUSION HEADER	
J7	BIOS function	
1-2	Normal	(Default)
2-3	Configuration Mode	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
IR1	IR HEADER	
CD_IN1	CDROM HEADER (ATAPI)	
AUX_IN1	AUDIO AUX HEADER (ATAPI)	
MDM_IN1	TELEPHONY HEADER (ATAPI)	
JP2	H/W AUDIO SELECT HEADER	
1-2	Disable	
2-3	Enable	(Default)
JP4	K/M Power on	
1-2	S3,S5 both work	(Default)
2-3	Only S3 work	
JP5	Buzzer	
1-2	From Buzzer	(Default)
2-3	From Audio	

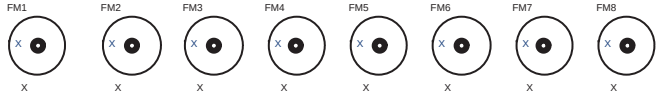
Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
PCI4	PCI Slot4
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
CPU_FAN	CPU FAN HEADER
SYS_FAN	System FAN HEADER
USB	USB REAR CONNECTOR
USB1	USB FRONT HEADER
POWER	ATX Power
F_P1	Front Panel
JPW1	ATX12V Power
JSPDIFO	SPDIF_OUT
JSPDIFI	SPDIF_IN
JAUDIO1	Front AUDIO HEADER

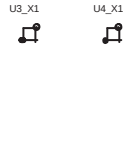
Micro-Star	Title: MS-6527	Rev: 11A
Document Number: JUMPER SETTING		
Last Revision Date: Friday, October 05, 2001	Sheet 25 of 33	

PCB OTHER COMPONENT

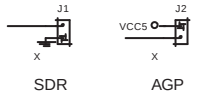








SIMULATION TRACE



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: MANUAL		
Last Revision Date: Friday, October 05, 2001	Sheet 26 of 33	

Norminal 4-layer Board Stackup

1.Board spec.

Description	Target Value	notes
Micro-stripline Er	4.2 - 4.5	
Trace Thickness	1.3 - 1.42 mils	1
Board Thickness	62 mils	
Material	FR4	
Fab Construction	4 layer	

2.Board each layer thickness .

Description	Target Value	Tolerance(+/- mils)
(Layer 1) Top layer	1.4 mil	See notes 1
Perpreg	4.0 mil	0.3
(Layer 2) Power layer	1.4 mil	0.2
Core	48 mil	5
(layer 3) Ground layer	1.4 mil	0.2
Perpreg	4.0 mil	0.3
(layer 4) Bottom layer	1.4 mil	See notes 1

3.Via Stack

Description	Target Value
Via Pad	26 mil
Via Anti-Pad	40 mil
Via Finiched hole	14 mil
Signal Pad(BGA)	20 mil

4.CPU GTL+ bus impedance = 50 Ohm(7mil trace width)

5.CPU asynchronous GTL+,AGP,Memory and Hub-link bus impedance = 60 Ohm(5mil trace width)

CPU Routing Guidelines

1.CPU data synchronous signal groups and the associate strobe

Signals	Associated Strobe
REQ[4:0]#,A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

***All the system bus signals must be referenced to GND**

2.Trace edge to edge spacing greater than 3:1(about 12 mils) versus trace to GND plane height ratio

3.2" - 10" from pin to pin and each data signal group should be routed to same length within +/-100 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

4.A pair data strobe should be routed to the same length within +/- 25mils, if one strobe switch layers, and another switch layer in the same manner.Additional CPU,MCH internal trace length(See Table-1)must be inculded.The calculation trace length follow (Table-2)

5.2" - 10" from pin to pin and each address signal group should be routed to same length within +/-200 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

6.Internal adderss strobe trace length(See Table-1) of CPU,MCH must be inculded.The calculation trace length follow (Table-2)

Table - 1

CPU package length + PCB trace length + MCH package length = Total length
L1 + L2 + L3 = Total L4

7.Keep the voltage divider with in 1.5 inches of GTLREF pin.and do not allow the GTLREF routing to splits or discontinuities power plane.

8.CPU Asynchronous GTL+ bus connect to ICH2 trace length

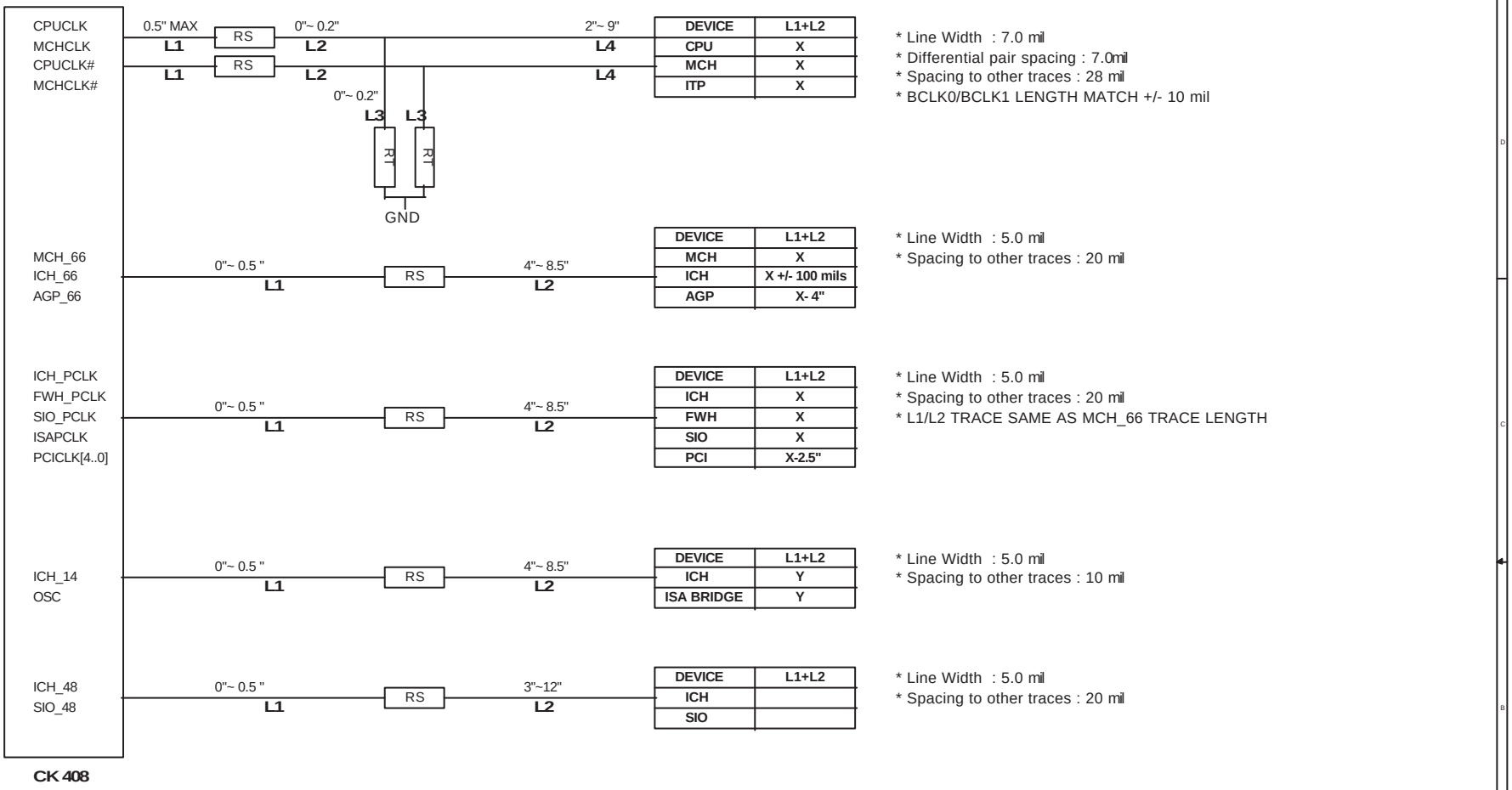
Signal Name	Trace Spacing	Trace Length	Pull-up Resistor
FERR#	7 MIL	1"-12"	62 Ohm +/- 5%
PROCHHOT#	7 MIL	1"-17"	62 Ohm +/- 5%
THERMTRIP#	7 MIL	1"-17"	62 Ohm +/- 5%
A20M#	7 MIL	1"-12"	None
IGNNE#	7 MIL	1"-12"	None
LINT[1:0]	7 MIL	1"-12"	None
SLP#	7 MIL	1"-12"	None
SMI#	7 MIL	1"-12"	None
STPCLK#	7 MIL	1"-12"	None
INIT#	7 MIL	1"-17"	None
PWRGOOD	7 MIL	1"-12"	300 Ohm +/- 5%

9.CPU BCLK,BCLK# should be routed as a differential pair with 7 mil trace and 7 mil spacing between them,2.5" to 10" pin to pin common clock lengths, and 25 mil spacing away form all the signal or clock.

10.DBSY#,DRDY#,TRDY#,ADS#,LOCK#,BNR#,HIT#,HITM#,BPRI#,DEFER#,BR0#,RESET# and RS[2:0]# CPU signal trace length around 2.5" to 10"

11.CPU and MCH package length

Micro-Star	Title: MS-6527	Rev: 11A
Document Number: CPU Bus Layout Guigeline		
Last Revision Date: Friday, October 05, 2001	Sheet 27 of 33	



DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

Micro-Star	Title: MS-6527	Rev: 11A
Document Number: CK-408 Design Guide		
Last Revision Date: Friday, October 05, 2001	Sheet 28 of 33	

MCH Routing Guidelines

1.HVREF,HSWNG and HRCOMP signal layout

Signal	Max. Length	Width	Clearance
HVREF	3"	12 mil	10 mil
HSWNG	3"	12 mil	10 mil
HRCOMP	0.5"	10 mil	7 mil

SDRAM Routing Guidelines

1.SDQ[63:0],SCB[7:0] routing rule

3DIMM Layout Guideline

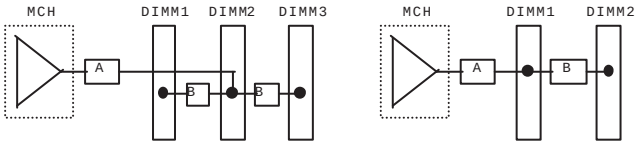
Signal	Length A	Length B	Width	Trace Spacing	Group Spacing
MD[63:0] MDP[7:0]	2.5" - 4.5"	0.4" - 0.6"	5 mil	12 mil	12 mil

2DIMM Layout Guideline

Signal	Length A	Length B	Width	Trace Spacing	Group Spacing
MD[63:0] MDP[7:0]	2.0" - 4.0"	0.4" - 0.6"	5 mil	12 mil	12 mil

Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"
5 mil / 8 mil	1.5"



2.SCS#[11:0],SCKE[5:0] routing rule

3DIMM Layout Guideline

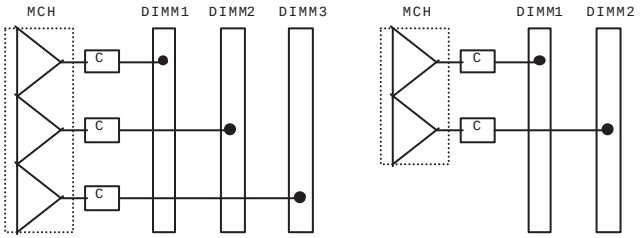
Signal	Length C	Width	Trace Spacing	Group Spacing
MCS#[11:0]	3.0" - 4.0"	5 mil	12 mil	12 mil
MCKE[5:0]	3.0" - 4.4"	10 mil	12 mil	12 mil

2DIMM Layout Guideline

Signal	Length C	Width	Trace Spacing	Group Spacing
MCS#[7:0]	3.0" - 4.0"	5 mil	12 mil	12 mil
MCKE[5:0]	3.0" - 4.0"	10 mil	12 mil	12 mil

Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"



3.SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE# routing rule

3DIMM Layout Guideline

Signal	Length E	Length F	Width	Trace Spacing	Group Spacing
MA[12:0] MBS[1:0] MRAS# MCAS# MWE#	2.5" - 4.0"	0.4" - 0.6"	5 mil	10 mil	12 mil

3DIMM Breakout CHIP routing rule

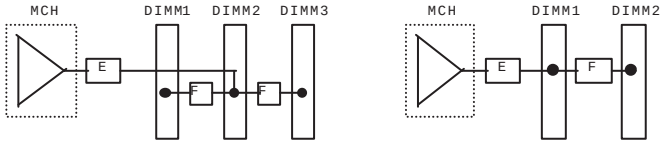
Width/spacing	Max. Length
5 mil / 5 mil	0.5"
5 mil / 8 mil	1.0"

2DIMM Layout Guideline

Signal	Length E	Length F	Width	Trace Spacing	Group Spacing
MA[12:0] MBS[1:0] MRAS# MCAS# MWE#	2.0" - 3.0"	0.4" - 0.6"	5 mil	10 mil	12 mil

2DIMM Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"
5 mil / 8 mil	1.5"



4.SCK[11:0] routing rule

3DIMM Layout Guideline

Signal	Length G	Length H	Length I	Length J	Length K	Width	Trace Spacing	Group Spacing
MCLK[11:0]	See Table-3	0.0" - 1.0"	0.0" - 0.25"	4.0" - 5.0"	0.0" - 1.5"	7 mil	15 mil	15 mil

2DIMM Layout Guideline

Signal	Length G	Length H	Length I	Length J	Length K	Width	Trace Spacing	Group Spacing
MCLK[7:0]	See Table-3	0.0" - 1.0"	0.0" - 0.25"	4.0" - 5.0"	0.0" - 1.5"	7 mil	15 mil	15 mil

3DIMM Total Length Limits

MCH package length G + Length H + Length J = Total length
G + H + J = 5.9"+/- 50mils

2DIMM Total Length Limits

MCH package length G + Length H + Length J = Total length
G + H + J = 5.3"+/- 50mils

Breakout CHIP routing rule

Width/spacing	Max. Length
7 mil / 5 mil	0.5"
7 mil / 10 mil	1.0"

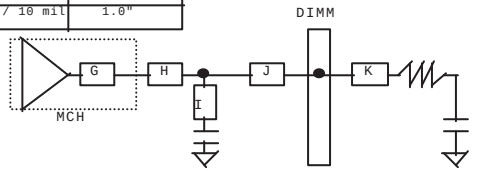
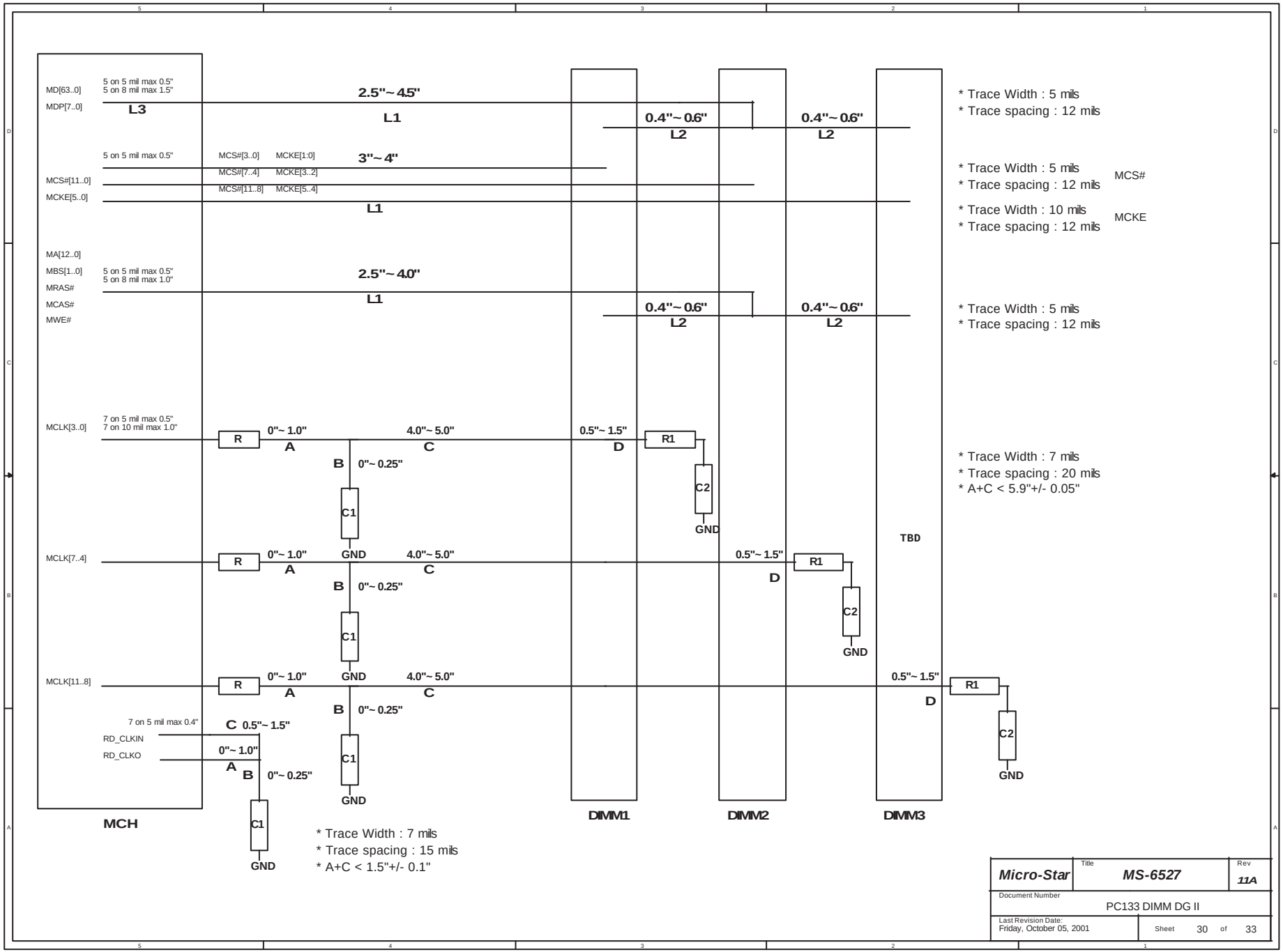


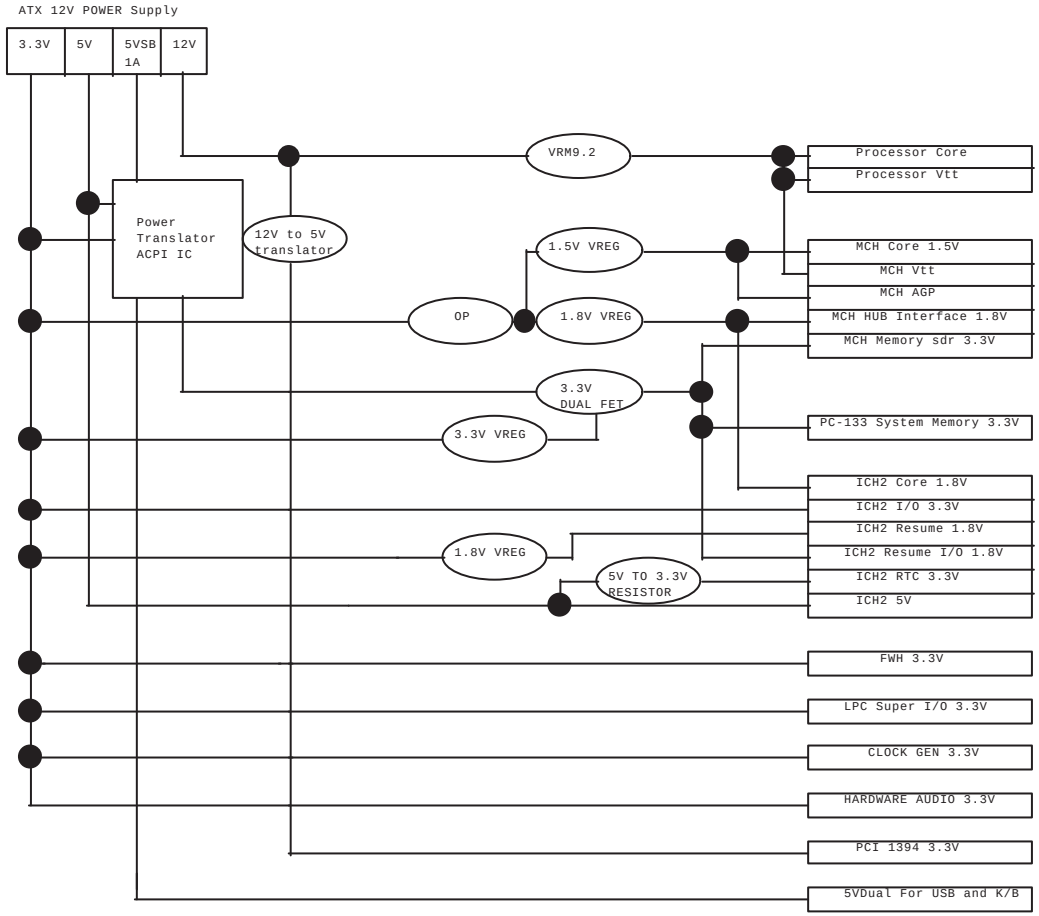
Table - 3

SCK Signal	Package Trace Length(")
MCLK0	0.404
MCLK1	0.353
MCLK2	0.865
MCLK3	0.893
MCLK4	0.371
MCLK5	0.349
MCLK6	0.814
MCLK7	0.821
MCLK8	0.483
MCLK9	0.432
MCLK10	0.589
MCLK11	0.689

Micro-Star	Title: MS-6527	Rev: 11A
Document Number: PC133 DIMM DG I		
Last Revision Date: Friday, October 05, 2001	Sheet 29 of 33	


MD[63..0]
MDP[7..0]
5 on 5 mil max 0.5"
5 on 8 mil max 1.5"
L3
2.5"~4.5"
L1
0.4"~0.6"
L2
0.4"~0.6"
L2
* Trace Width : 5 mils
* Trace spacing : 12 mils
5 on 5 mil max 0.5"
MCS#[3..0] MCKE[1:0]
MCS#[7..4] MCKE[3..2]
MCS#[11..8] MCKE[5..4]
3"~4"
MCS#[11..0]
MCKE[5..0]
L1
* Trace Width : 5 mils
* Trace spacing : 12 mils
MCS#
* Trace Width : 10 mils
* Trace spacing : 12 mils
MCKE
MA[12..0]
MBS[1..0]
MRAS#
MCAS#
MWE#
5 on 5 mil max 0.5"
5 on 8 mil max 1.0"
2.5"~4.0"
L1
0.4"~0.6"
L2
0.4"~0.6"
L2
* Trace Width : 5 mils
* Trace spacing : 12 mils
MCLK[3..0]
7 on 5 mil max 0.5"
7 on 10 mil max 1.0"
R
0"~1.0"
A
4.0"~5.0"
C
0.5"~1.5"
D
R1
B
0"~0.25"
C2
GND
C1
GND
* Trace Width : 7 mils
* Trace spacing : 20 mils
* A+C < 5.9"+/- 0.05"
MCLK[7..4]
R
0"~1.0"
A
GND
4.0"~5.0"
C
0.5"~1.5"
D
R1
TBD
B
0"~0.25"
C2
GND
C1
GND
MCLK[11..8]
R
0"~1.0"
A
GND
4.0"~5.0"
C
0.5"~1.5"
D
R1
B
0"~0.25"
C2
GND
7 on 5 mil max 0.4"
C 0.5"~1.5"
RD_CLKIN
RD_CLKO
0"~1.0"
A
B
0"~0.25"
C1
GND
C1
GND
MCH
DIMM1
DIMM2
DIMM3
* Trace Width : 7 mils
* Trace spacing : 15 mils
* A+C < 1.5"+/- 0.1"
Micro-Star
Title
MS-6527
Rev
11A
Document Number
PC133 DIMM DG II
Last Revision Date:
Friday, October 05, 2001
Sheet 30 of 33

Power Delivery Map



Micro-Star	Title: MS-6527	Rev: 11A
Document Number: Power Delivery Map		
Last Revision Date: Friday, October 05, 2001	Sheet 31 of 33	

Revision History

Revision History (Changes from Rev 0A)

3	Reserve R577,R578,Q79 for power down issue.
12	Change SPDIFI from U19.113 to U19.86.
13	C160,C163 change size from 0805 to 1206.
	C218,C219,C220,C221,C187,C188,C189 change size from0805 to 0603.
	Add R558,R559,R560,R561,R563,R564,C310,C315,C316 for CMI8738 reference circuit.
	To exchange CENTER and BASS signal.
14	C229,C230 change size from SMD 47u to Dip 470u.
	CN23 change size from CM0603 8P4R to CM0603*4.
	Change RN38 from GND to JVCC for game port circuit error.
15	Add R544,R545,R546,R547,R548,R549,R550,R551,R552,R573,Q75,Q76,Q77,Q78,U33,VR4
	for thermtrip circuit.
19	Add R547,CT51 for LG requirement.
	Add R565,R566 for LED circuit modify.
20	Add R553,R554,R555,R556,R557,D26,Q74,C317 for SYS_FAN2 circuit.
22	Add R575,R576,VR5 for change VID power form 3.3V to 12V.
24	Add FS5,FB44,FB46,C304,C305,R567 for changePort0 from 6 pin to 8 pin.
	Add FS6,FB45,Fb47,R568,R569,R570,R571,R572,C306,C307,C308,C309,RN39,U32
	for 1394 PORT1.
	Change R533,R534,R467 from connect L9.1 to connect L9.2 for 1394 circuit error.

Revision History (Changes from Rev 0B)

3	Reserve R591 for P4 133 CPU BSEL.
8	Reserve R587,R588 for P4 133 CPU BSEL.
13	C160,C163 change size from 0805 to 1206.
14	Add R585,R586 for remove JAUDIO1 use.
	Add CP2 for EMI test.
19	Remove R432 for ESD test.
20	Remove R553,R554,R555,R556,R557,D26,Q74,C317,S_FAN2.
	And add one SCREW_HOLE.
22	Add R592 for costdown JP4.
23	Add R582 connect +12V to P+12V for Print issue.
	Change Q65,Q66,Q67,Q68,Q69,Q70,Q71,Q72,Q73 pin1 from -12V to Gnd for Print issue.
	Change Q65,Q66,Q67,Q68,Q69,Q70,Q71,Q72,Q73 pin2 from +12V to P+12V for Print issue.
24	Change U27 pin20,35,48,62,78 from DUAL3_3 to VCC5 for 43AB22.
	And change U26 pin8,R465,R466 from DUAL3_3 to VCC5 for 43AB22.
	Reserve R580,R581,R589,R590 for PCIRST#1 direct connect S_RST.
	Add R565,R566 for LED circuit modify.

Revision History (Changes from Rev 100)

	Layout move RTCRST# signal for to avoid touch APIC_D0 signal.

Revision History (Changes from Rev 110)

20	Add R593 for CPU FAN use.
	Increase X2 crystal wire fixer hole for factory issue.

UUU=JAUDIO1(3-4,5-6)

UUU

JC-D2x2-GN

BAT SOCKET

BAT1[A]

YSKTBT

BIOS

U23[1]

1	VPP	VCC	32
2	RST#	CLK	31
3	FGPI3	FGPI4	30
4	FGPI2	IC(VIL)	29
5	FGPI1	GNDA	28
6	FGPI0	VCCA	27
7	WP#	GND	26
8	TBL#	VCC	25
9	ID3	INIT#	24
10	ID2	FWH4	23
11	ID1	RFU	22
12	ID0	RFU	21
13	FWH0	RFU	20
14	FWH1	RFU	19
15	FWH2	RFU	18
16	GND	FWH3	17

SST49LF002A

JBAT1(1-2)

YJUMPER-MG

JP2(2-3)

YJUMPER-MG

JP4(1-2)

YJUMPER-MG

J7(1)

YJUMPER-MG

JP5(1-2)

X_YJUMPER-MG

AGP1-1

B1		12V	A1
B2	OVRCNT#	TYPEDET#	A2
B3	5V	RESV	A3
B4	5V	USB-	A4
B5	USB+	GND	A5
B6	GND	INTA#	A6
B7	INTB#	RST#	A7
B8	CLK	GNT#	A8
B9	REQ#	VCC3	A9
B10	VCC3	ST1	A10
B11	ST0	RESV	A11
B12	ST2	PIPE#	A12
B13	RBF#	GND	A13
B14	GND	WBF#	A14
B15	RESV	SBA1	A15
B16	SBA0	VCC3	A16
B17	VCC3	SBA3	A17
B18	SBA2	ST_STB#	A18
B19	SB_STB	GND	A19
B20	GND	SBA5	A20
B21	SBA4	SBA7	A21
B22	SBA6	RESV_C	A22
B23	RESV	GND_D	A23
B24	GND N	RESV_D	A24
B25	3_3VAUX1	VCC3_3_C	A25
B26	VCC3	AD30	A26
B27	AD31	AD28	A27
B28	AD29	VCC3	A28
B29	VCC3	AD26	A29
B30	AD27	AD24	A30
B31	AD25	GND	A31
B32	GND	AD_STB1#	A32
B33	AD_STB1	C/BE#3	A33
B34	AD23	VDDQ	A34
B35	VDDQ	AD22	A35
B36	AD21	AD20	A36
B37	AD19	GND	A37
B38	GND	AD18	A38
B39	AD17	AD16	A39
B40	C/BE#2	VDDQ	A40
B41	VDDQ	FRAME#	A41
B42	IRDY#	RESV	A42
B43	3_3VAUX2	GND	A43
B44	GND	RESV	A44
B45	RESV	VCC3	A45
B46	VCC3	TRDY#	A46
B47	DEVSEL#	STOP#	A47
B48	VDDQ	PME#	A48
B49	PERR#	GND	A49
B50	GND	PAR	A50
B51	SERR#	AD15	A51
B52	C/BE#1	VDDQ	A52
B53	VDDQ	AD13	A53
B54	AD14	AD11	A54
B55	AD12	GND	A55
B56	GND	AD9	A56
B57	AD10	C/BE#0	A57
B58	AD8	VDDQ	A58
B59	VDDQ	AD_STB0#	A59
B60	AD_STB0	AD6	A60
B61	AD7	GND	A61
B62	GND	AD4	A62
B63	AD5	AD2	A63
B64	AD3	VDDQ	A64
B65	VDDQ	AD0	A65
B66	AD1	VREF_GC	A66
	VREF_CG		

Retention Module

MS6527PCB

PCB

MS-6527-11A

COM1

YCN9M-1

COM2

YCN9M-1

F900

1	GNDK	KEYLOCK	10
2	NC	NC	11
3	HDD+	HDD-	12
4	GNDL	SPEAKER	13
5	SLED2	BUZ+	14
6	PLED1	BUZ-	15
7	PWSW+	VCCSPK	16
8	PWSW-	RESET	17
9	GNDG	GNDR	18

MSI-JFP

X_U12-A

845-MCH-PIN

X_U12-B

X_845-MCH-PIN

X_U12

845-MCH-H

U7_1

CPU Retention Module

X_U12-C

X_845-MCH-PIN

X_U12-D

845-MCH-PIN

Micro-Star	Title: MS-6527		Rev: 11A
Document Number: PACKING BOM			
Last Revision Date: Friday, October 05, 2001		Sheet 33 of 33	