

MS-6526

Version 00A

INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-G Chipset:

**INTEL GMCH (North Bridge) +
INTEL ICH4 (South Bridge)**

On Board Chipset:

BIOS -- FWH

AC'97 Codec -- ALC201A

LPC Super I/O -- W83627HF-AW

Clock Generation -- ICS950218AF

LAN -- RealTek RTL8101L

Expansion Slots:

PCI2.2 SLOT * 3

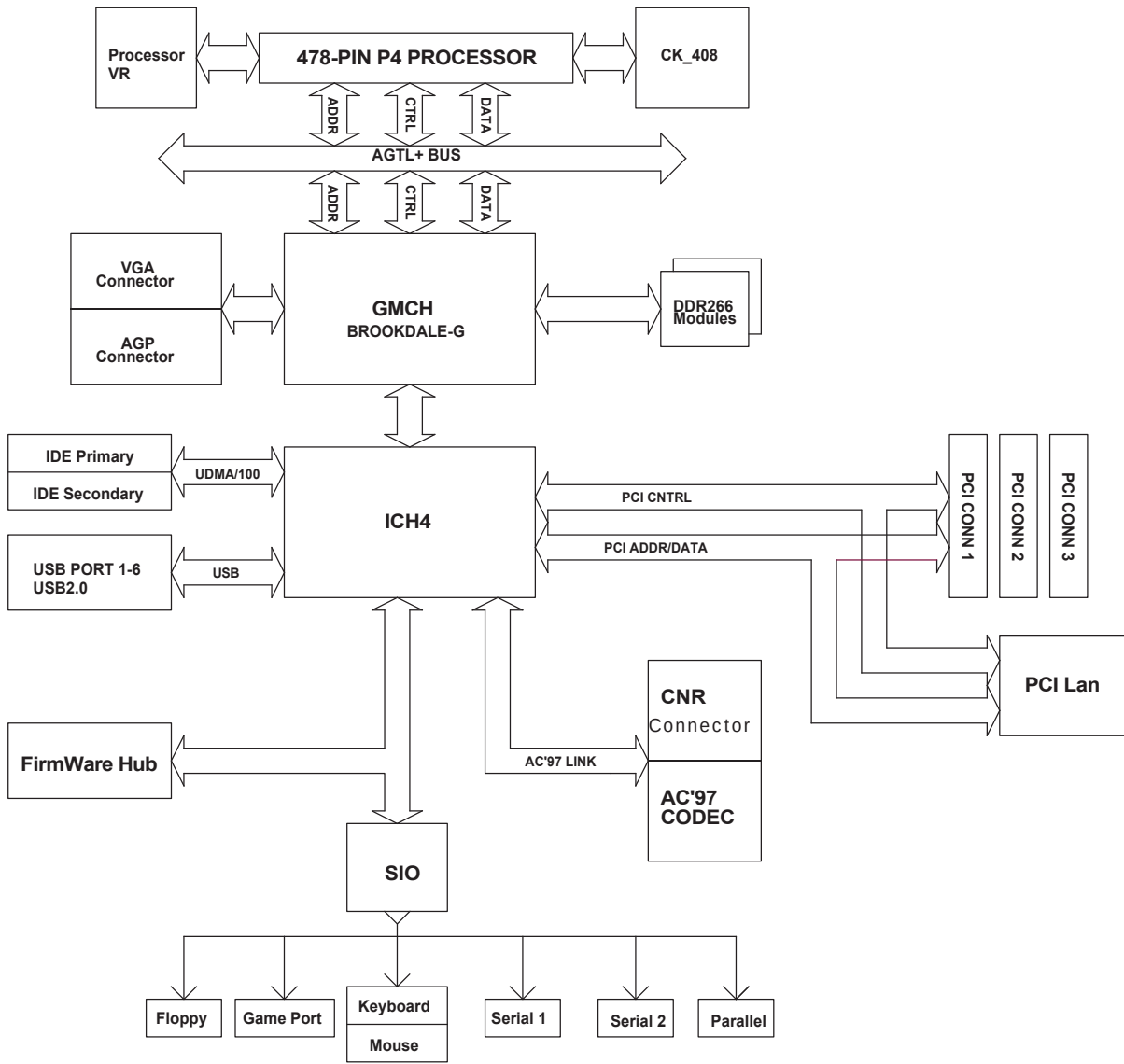
Title

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		MICRO-STAR INT'L CO.,LTD.	
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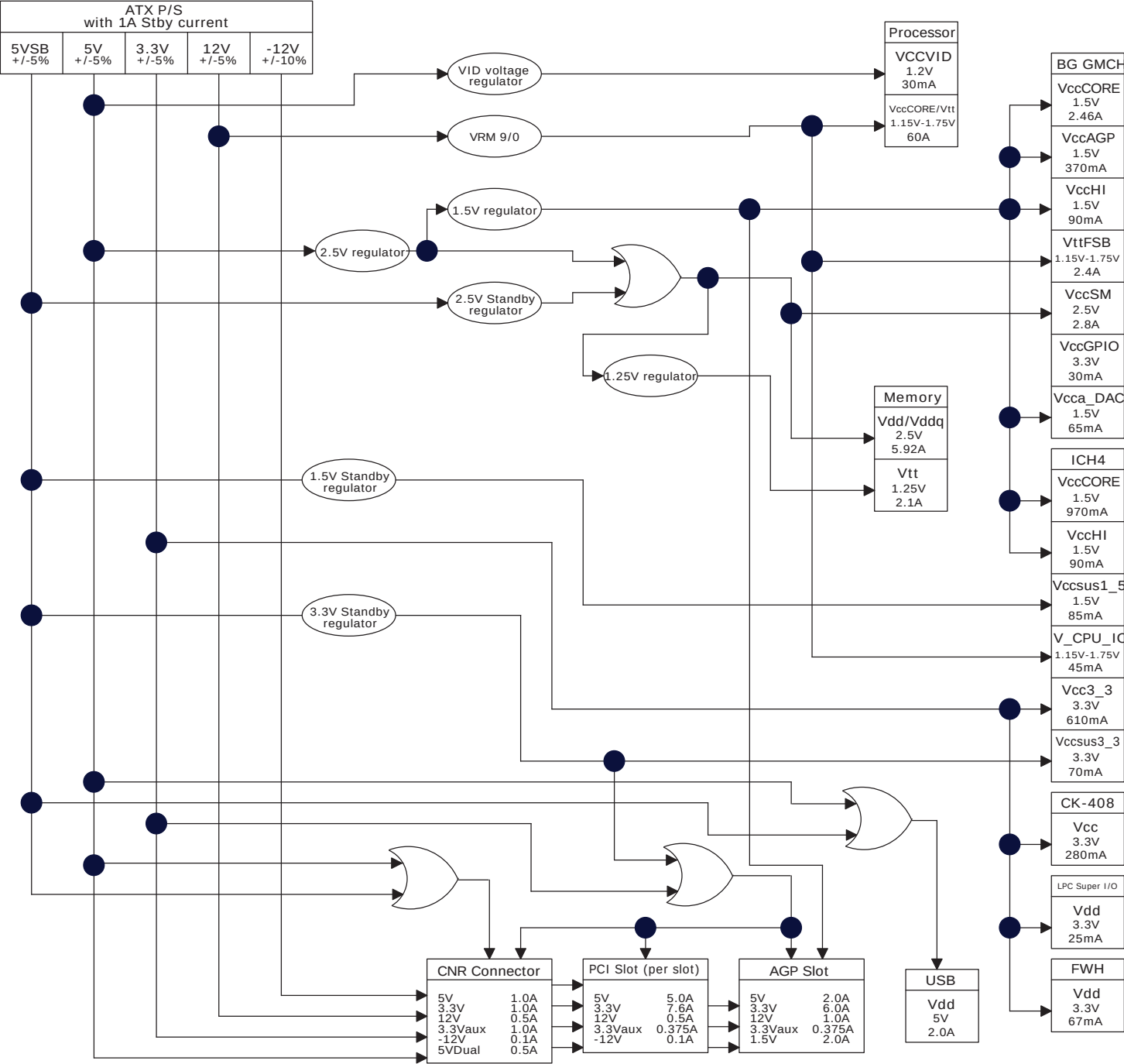
BLOCK DIAGRAM



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Title				Block Diagram			
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Power Delivery Map



General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntion pin)
GPIO 12	I	Pull down through 10K ohms (unused)
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifuntion pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2	12 (PCI5)
PCI LAN	INTG# INTF#	AD29	LAN_PCLK	17 (PCI9)

*ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

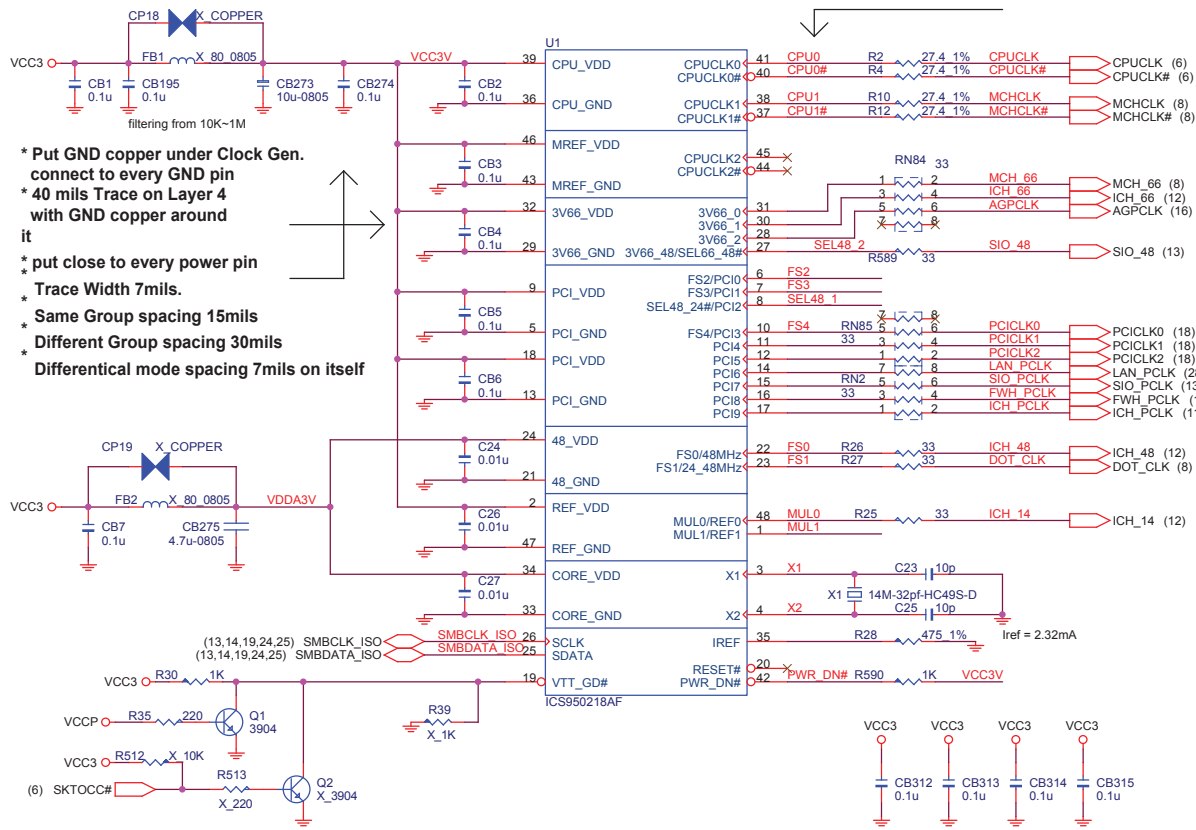


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CLOCK GENERATOR BLOCK

*Trace < 0.5"



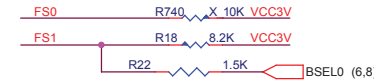
Shut Source Termination Resistors



Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS

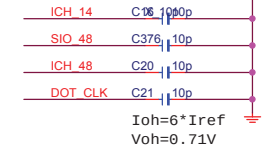
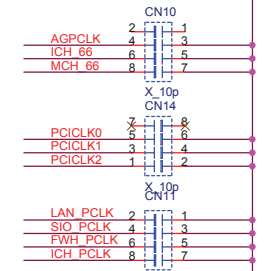
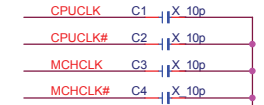


FS4 FS3 FS2 FS1 FS0 FSB (MHz)

1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz



Pull-Down Capacitors



Ioh=6*Iref
Voh=0.71V
used only for EMI issue

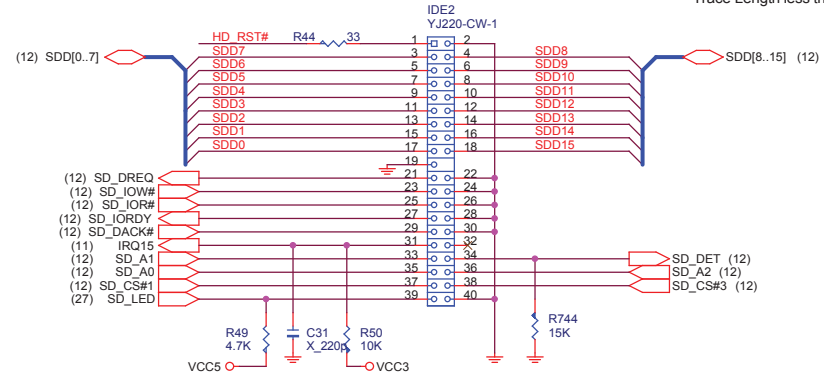
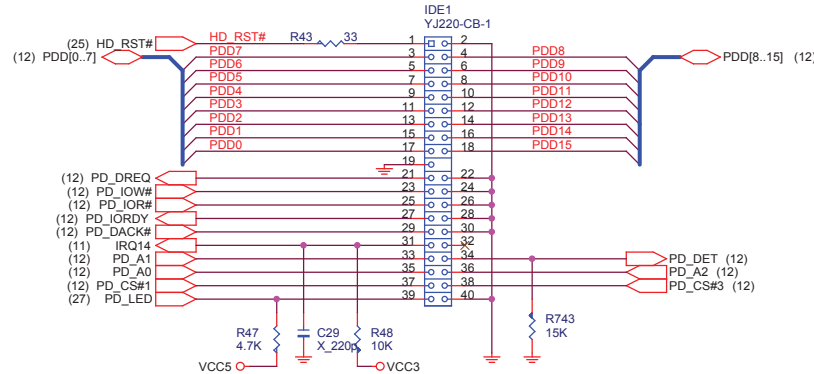
Trace less 0.2"

PRIMARY IDE BLOCK

ATA100 IDE CONNECTORS

SECONDARY IDE BLOCK

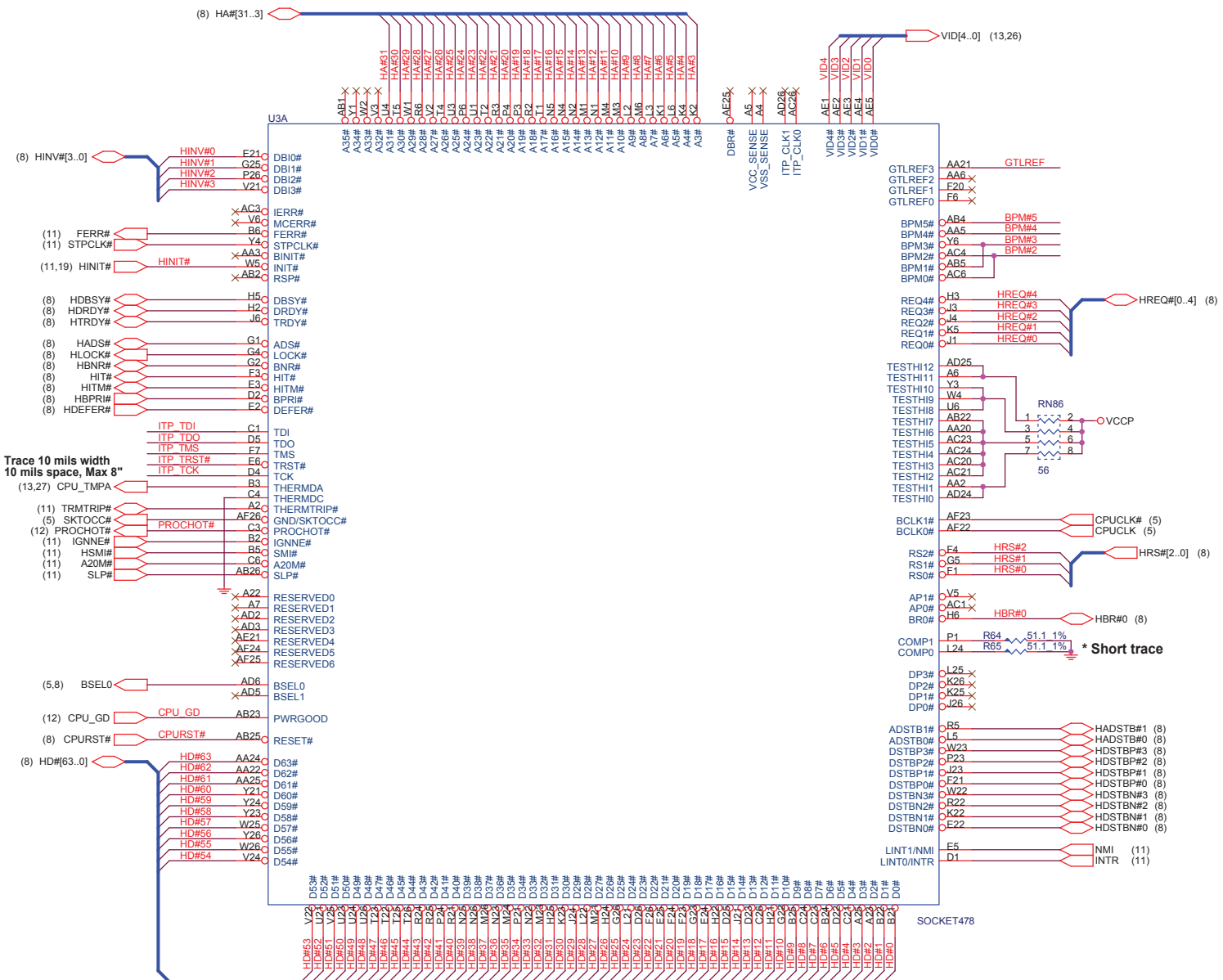
* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than 5"



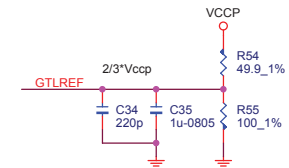
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Title			Clock Gen & ATA100 IDE Connectors
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CPU SIGNAL BLOCK



CPU GTL REFERENCE VOLTAGE BLOCK



Every pin put one 220pF cap near it.
Trace Width 7mils, Space 10mils.
Keep the voltage divider within
1.5" of the GETREF pin.

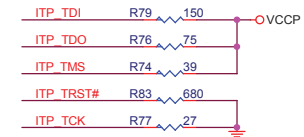
CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU



with in
1"~2"



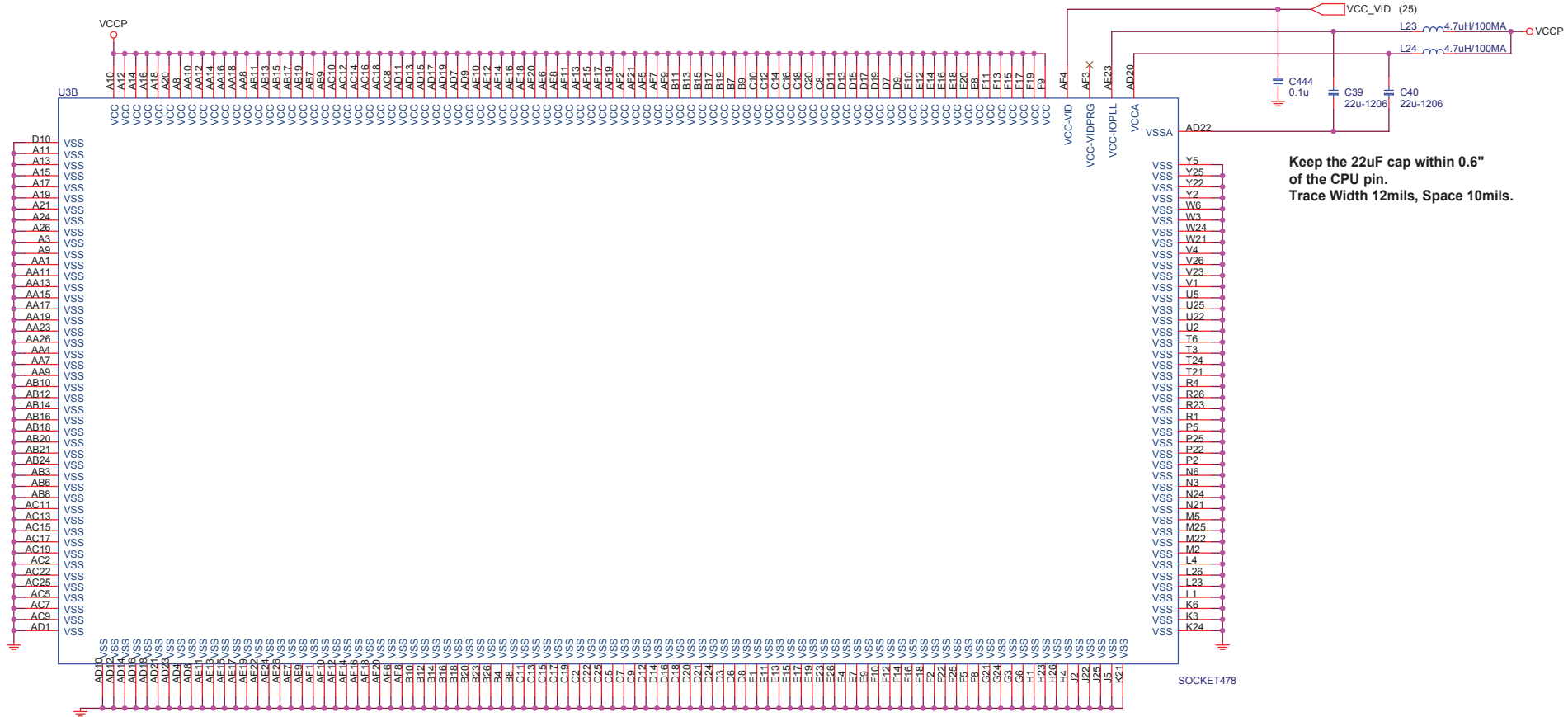
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Title	mPGA478-B INTEL CPU SOCKET Part1
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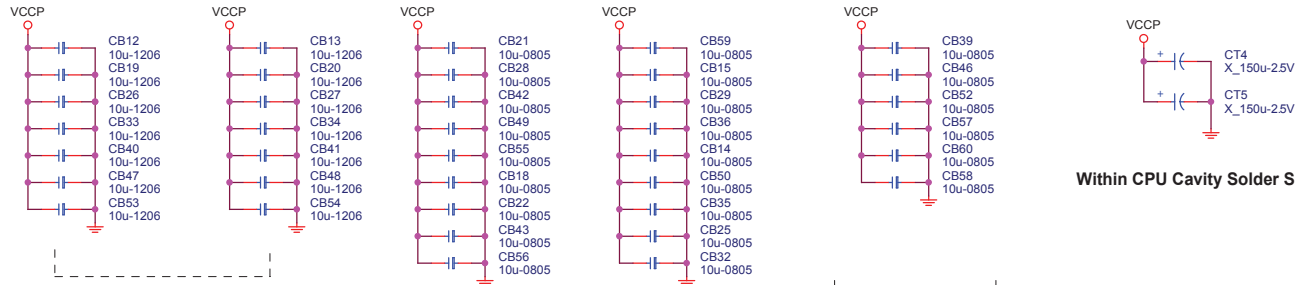
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CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



Place 14 pcs 1206 size cap
north side of processor

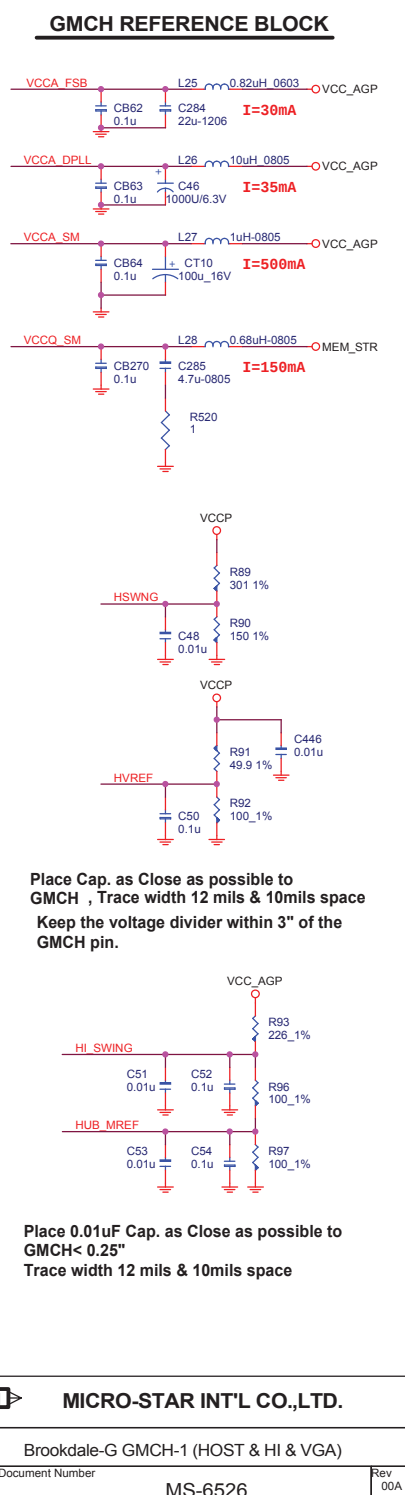
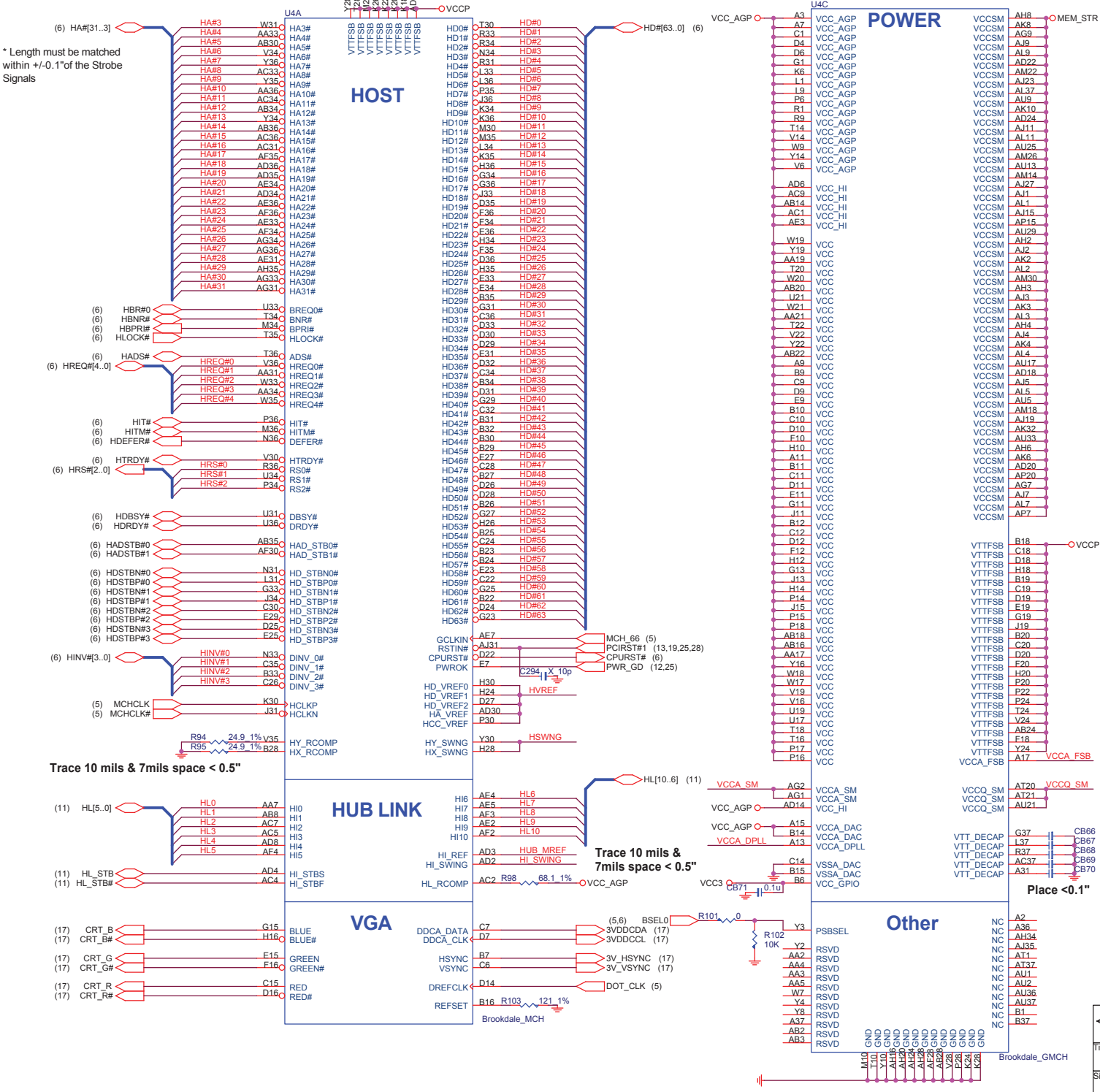
PLACE CAPS WITHIN CPU CAVITY

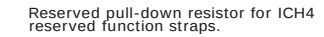
Place these caps on south
side of processor

Within CPU Cavity Solder Side

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* Length must be matched within +/-0.1" of the Strobe Signals





APIC D0 R128 10K
APIC D1 R129 10K
APICCLK

Trace width use 12 mils and 10mils space

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ICH4 PCI & HI & LAN			
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Pin-to-pin comparison diagram for W83627HF and W83627HF-2. The diagram shows two columns of pins, each with a list of functions and pin numbers. Red lines connect corresponding pins between the two columns. Some pins are marked with an 'X' indicating a mismatch or non-connection. The left column is labeled 'U8' and the right column is labeled 'U8'. The diagram is titled 'Pin-to-pin comparison' and includes a note 'W83627HF-2' at the bottom right.

Pin	Function	Pin	Function
1	DRVDEN0	23	DRVDEN0
2	DRVDEN1	23	DRVDEN1
3	INDEX#	23	INDEX#
4	MOA#	23	MOT_A#
5	DSB#	23	DRV_B#
6	DSA#	23	DRV_A#
7	MOB#	23	MOT_B#
8	DIR#	23	DIR#
9	STEP#	23	STEP#
10	WRDATA#	23	WT_DT#
11	WE#	23	WT_EN#
12	TRACK0#	23	TRACK0#
13	WP#	23	FDD_WP#
14	RDDATA#	23	RDATA#
15	HEAD#	23	HEAD#
16	DSKCHG#	23	DSKCHG#
17	PD0	23	LP_D0
18	PD1	23	LP_D1
19	PD2	23	LP_D2
20	PD3	23	LP_D3
21	PD4	23	LP_D4
22	PD5	23	LP_D5
23	PD6	23	LP_D6
24	PD7	23	LP_D7
25	SLCT	23	LP_SLCT
26	PE	23	LP_PE
27	BUSY	23	LP_BUSY
28	ACK#	23	LP_ACK#
29	SUN#	23	LP_SUN#
30	INIT#	23	LP_INIT#
31	ERR#	23	LP_ERR#
32	AFD#	23	LP_AFD#
33	STB#	23	LP_STB#
34	IRRX/GP25	27	IRRX
35	IRTX/GP26	27	IRTX
36	SUSCLKIN	12	SUSCLK
37	DCDA#	23	DCDA#
38	DSRA#	23	DSRA#
39	SINA	23	SINA
40	RTSA#	23	RTSA#
41	SOUTA	23	SOUTA
42	CTSA#	23	CTSA#
43	DTRA#	23	DTRA#
44	RIA#	23	RIA#
45	DCDB#	23	DCDB#
46	DSRB#	23	DSRB#
47	SINB	23	SINB
48	RTSB#	23	RTSB#
49	SOUTB	23	SOUTB
50	CTSB#	23	CTSB#
51	DTRB#	23	DTRB#
52	RIB#	23	RIB#
53	GA20	11	A20GATE#
54	KBST	11	KB_RST#
55	KBDATA	23	KBDATA
56	KBCLK	23	KBCLK
57	MSDATA	23	MSDATA
58	MSCLK	23	MSCLK
59	KBLOCK#	23	KBLOCK#
60	RSMRST#/GP33	23	RSMRST#/GP33
61	PWRK/GP32	23	PWRK/GP32
62	VSS1	20	VSS1
63	VSS2	55	VSS2
64	VSS3	86	VSS3
65	VSS4	117	VSS4

[illegible]

VCC5

CB 0.1

CB 0.1

CB 0.1

CB 0.1

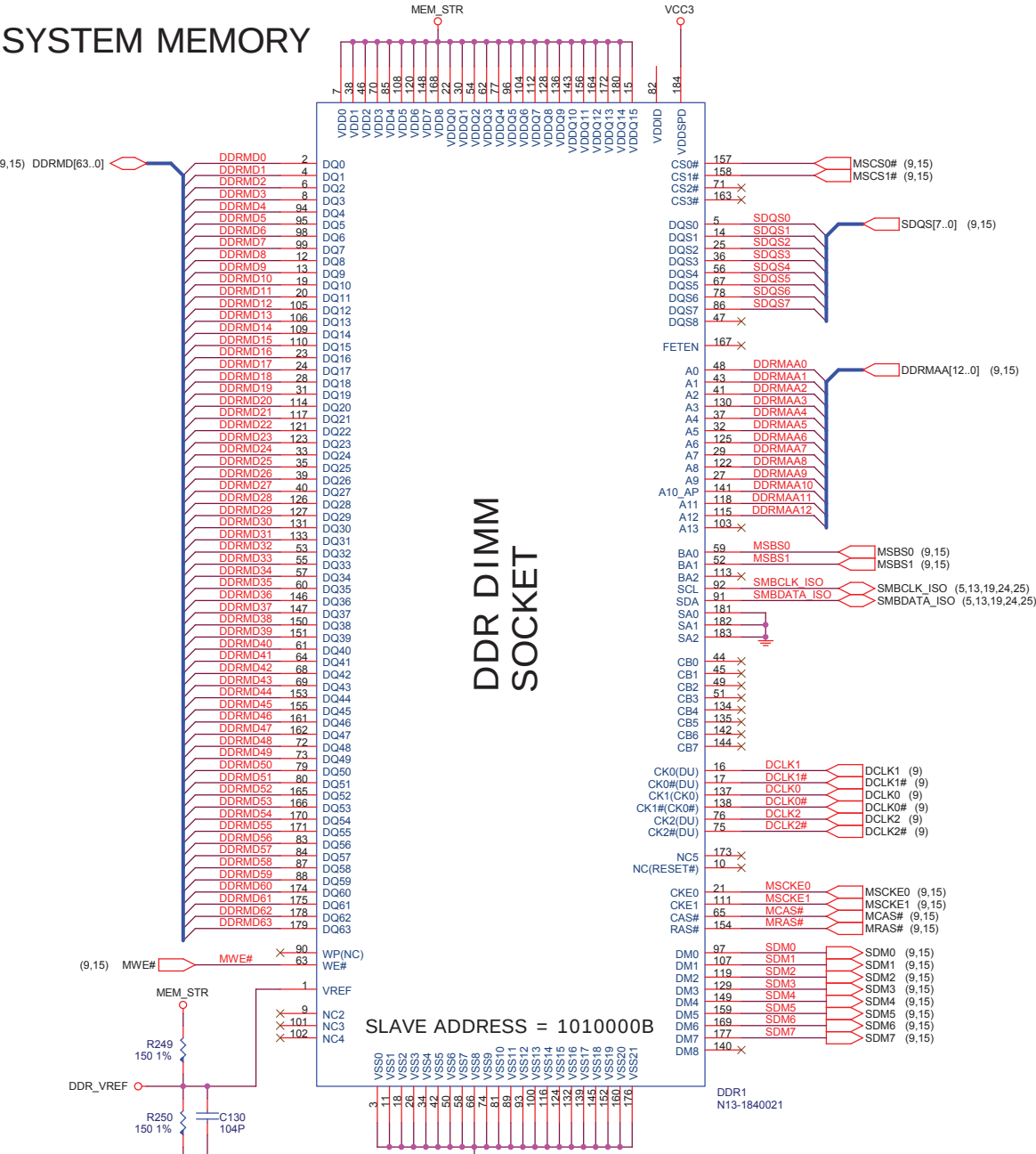
VCC5 ○ R865 4.7K SOUTA
VCC5 ○ R866 4.7K SOUTB
VCC5 ○ R175 X 4.7K RTSA#

SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

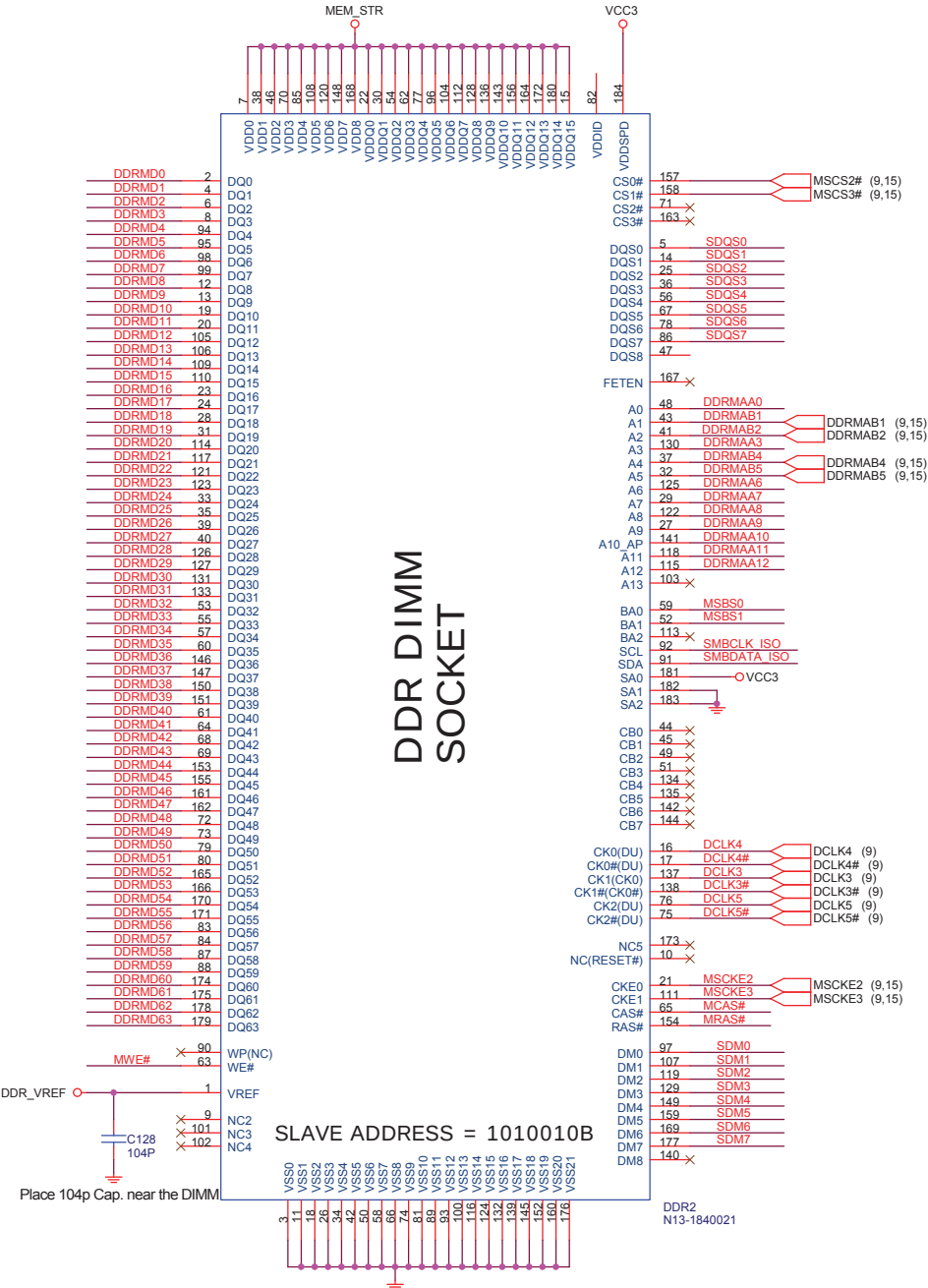
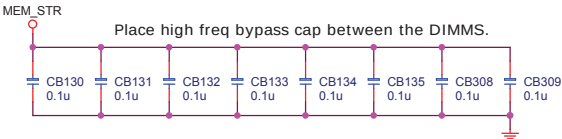


Title			
LPC IO & GAME PORT			
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SYSTEM MEMORY

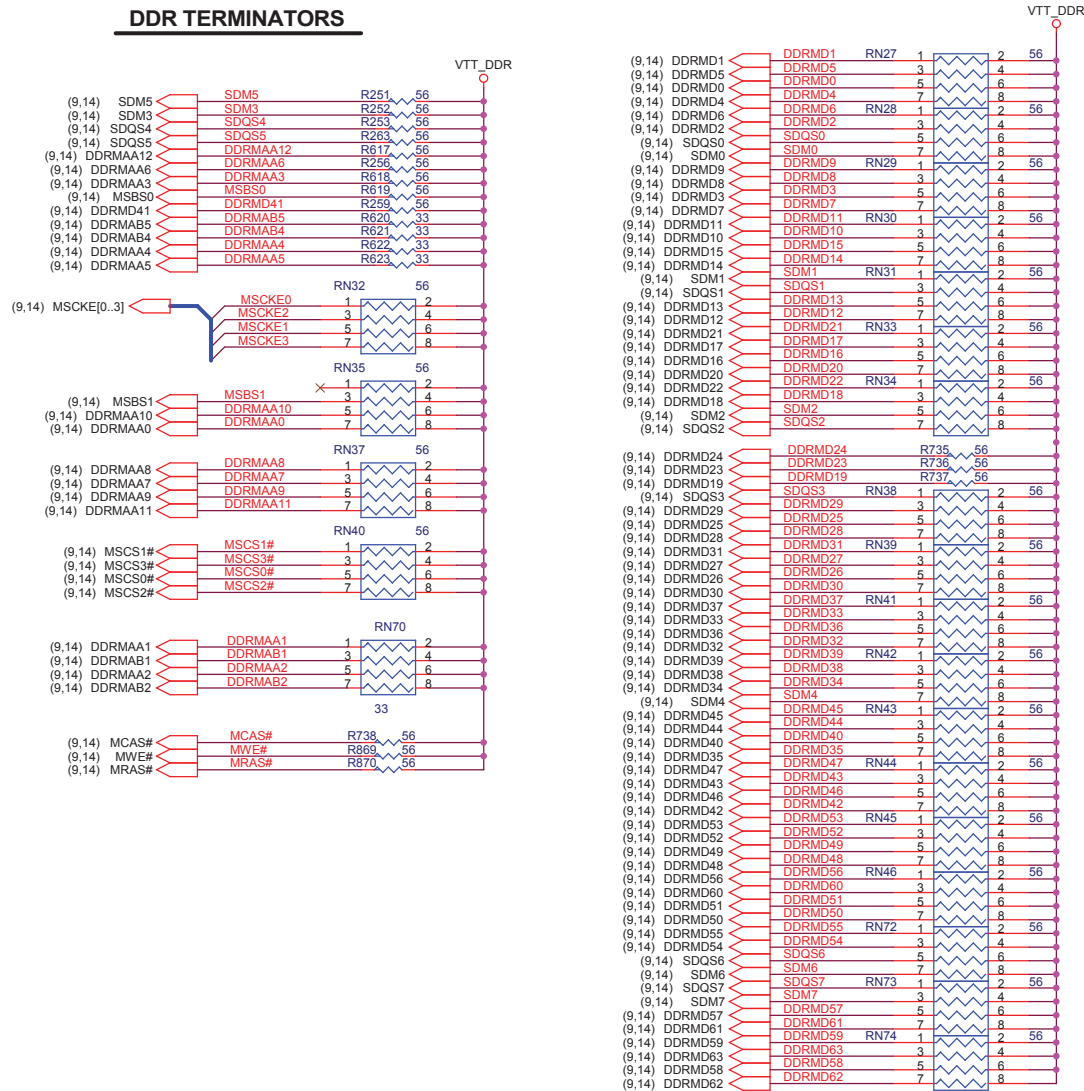


Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DIMM

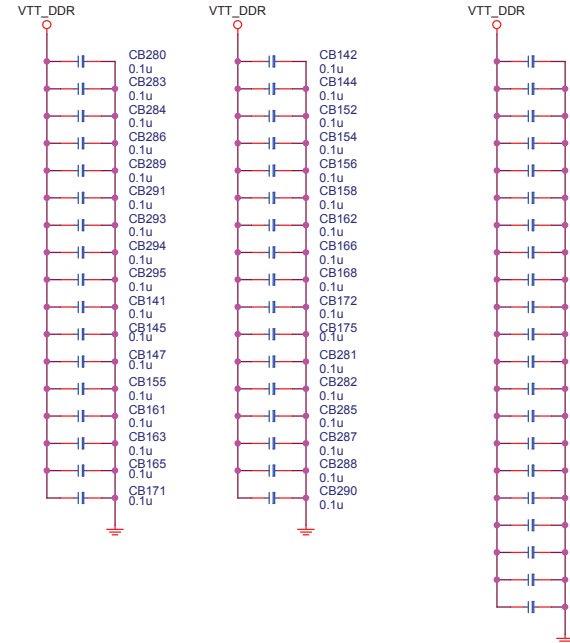


Place 104p Cap. near the DIMM

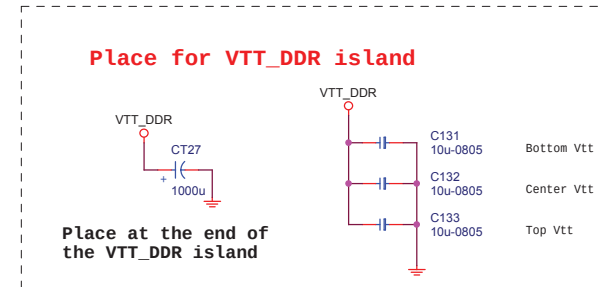
DDR TERMINATORS



DDR Decoupling Caps

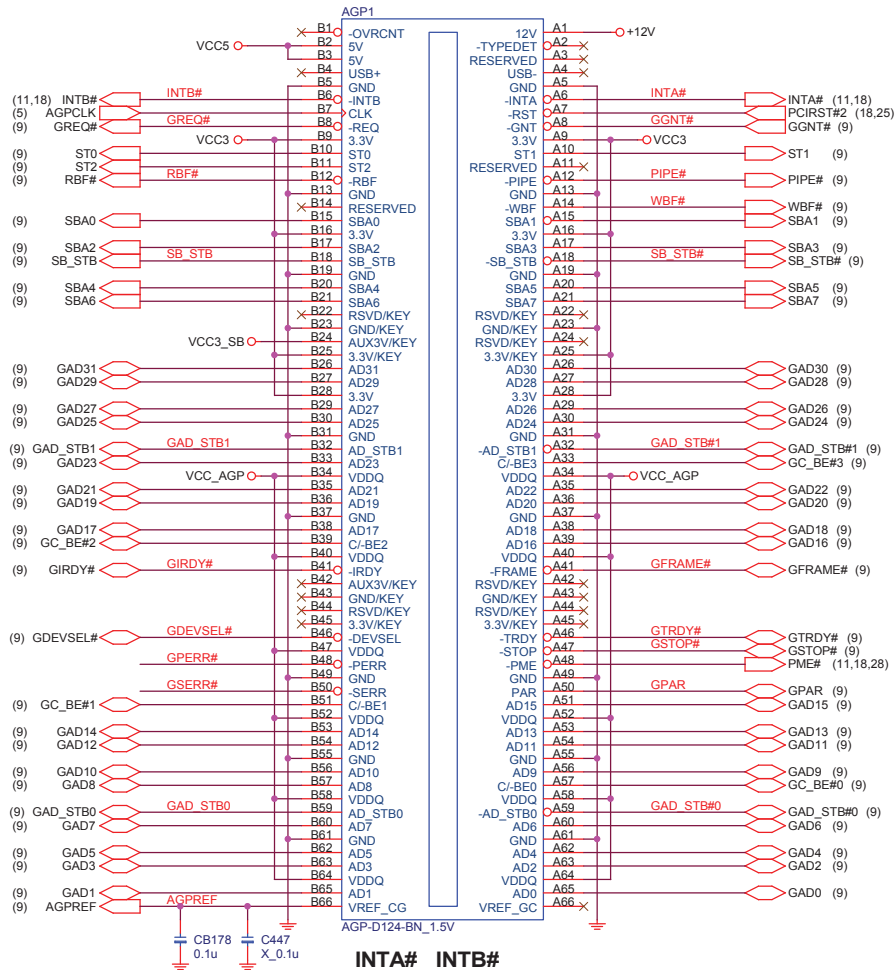


Total 110 signal, need 55 pcs decoupling.

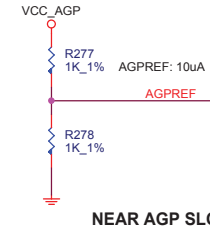


AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

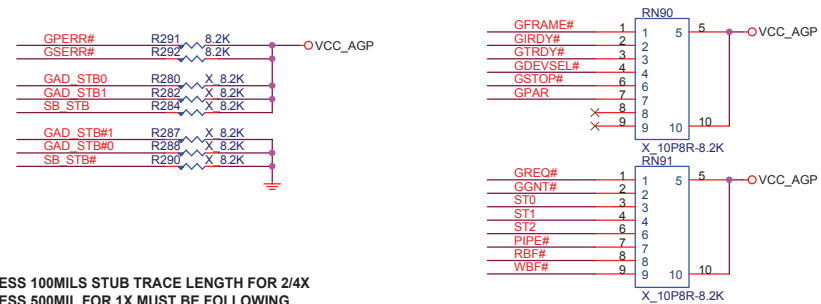
VCC5 = 60mils trace / 15 mils space



AGP SIGNAL REFERENCE CIRCUIT



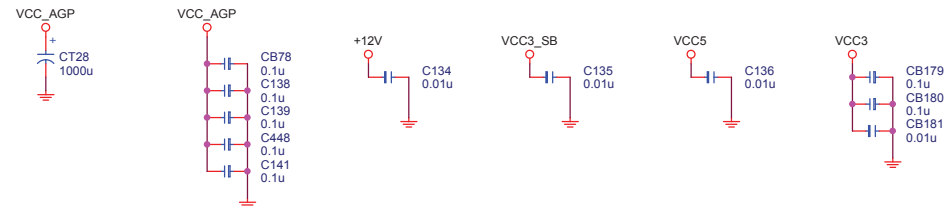
AGP TERMINATION RESISTORS



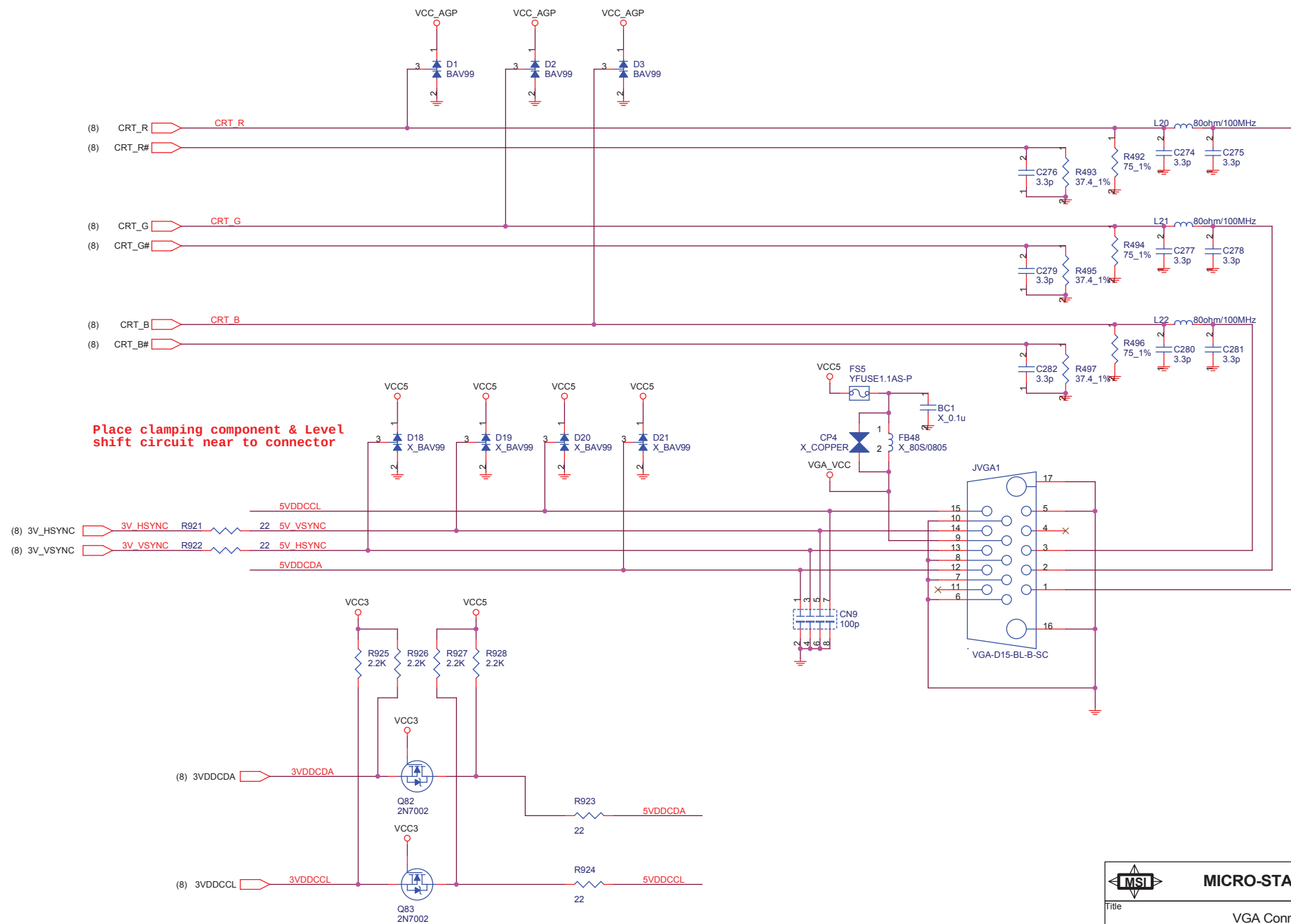
LESS 100MILS STUB TRACE LENGTH FOR 2/4X
LESS 500MIL FOR 1X MUST BE FOLLOWING.

Place these resistors between AGP slot & GMCH

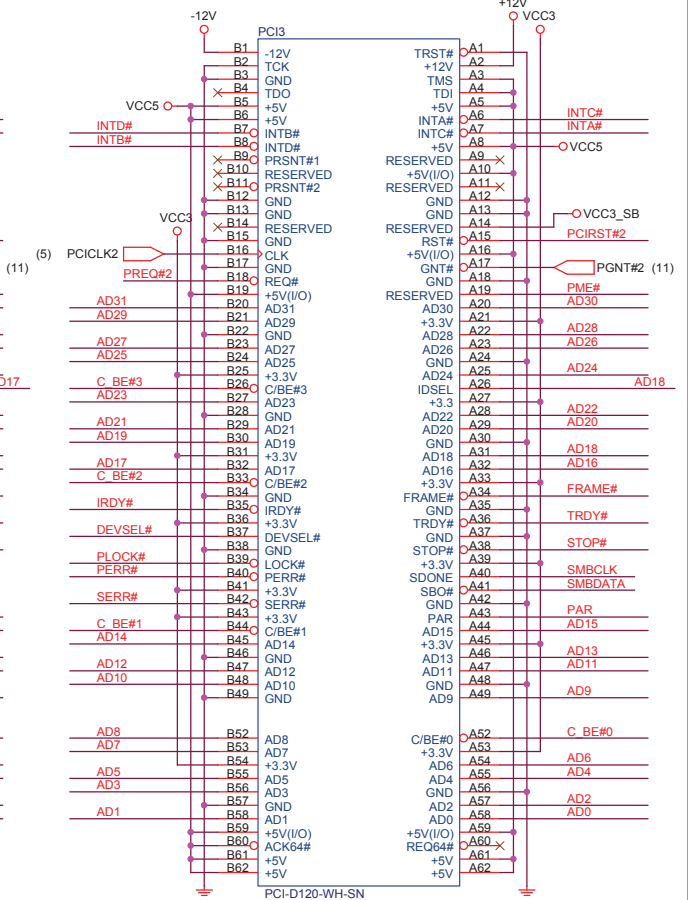
AGP SLOT DECOUPLING CAPACITORS



Video Connector

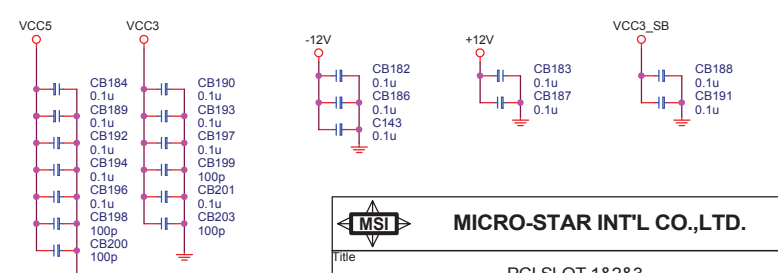


PCI SLOT 3 (PCI VER: 2.2 COMPLY)

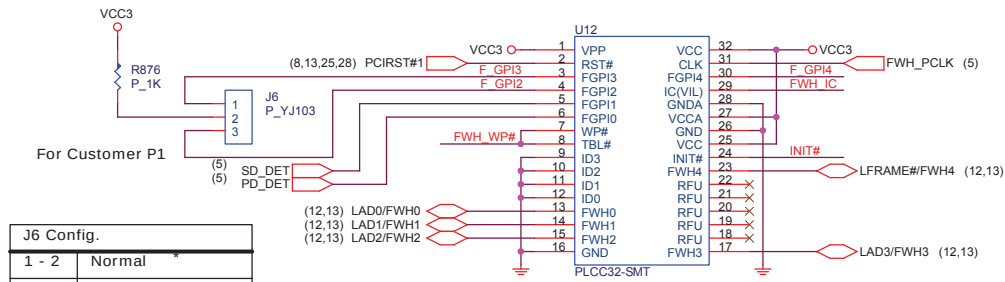


```
IDSEL = AD18
MASTER = PREQ2
INTC#
```

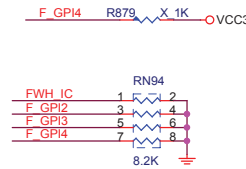
PCI SLOT DECOUPLING CAPACITORS



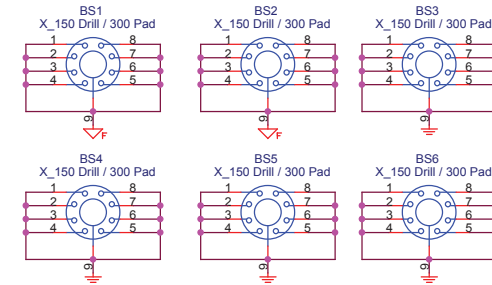
Firware Hub (FWH)



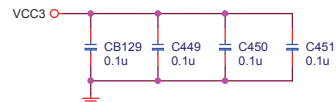
FWH RESISTORS



PCB Mounting Holes

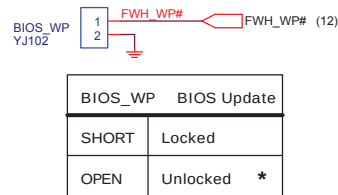


FWH DECOUPLING CAPACITORS

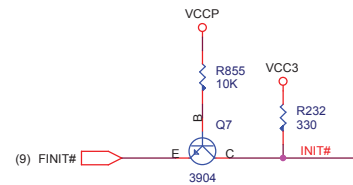


Place Cap. as Close to FWH< 350 mil

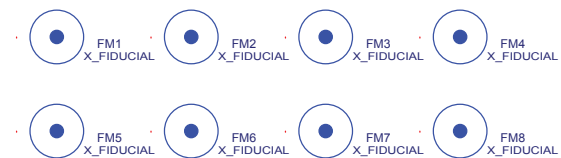
FWH write protect



FWH INIT Signal Voltage Translation Block

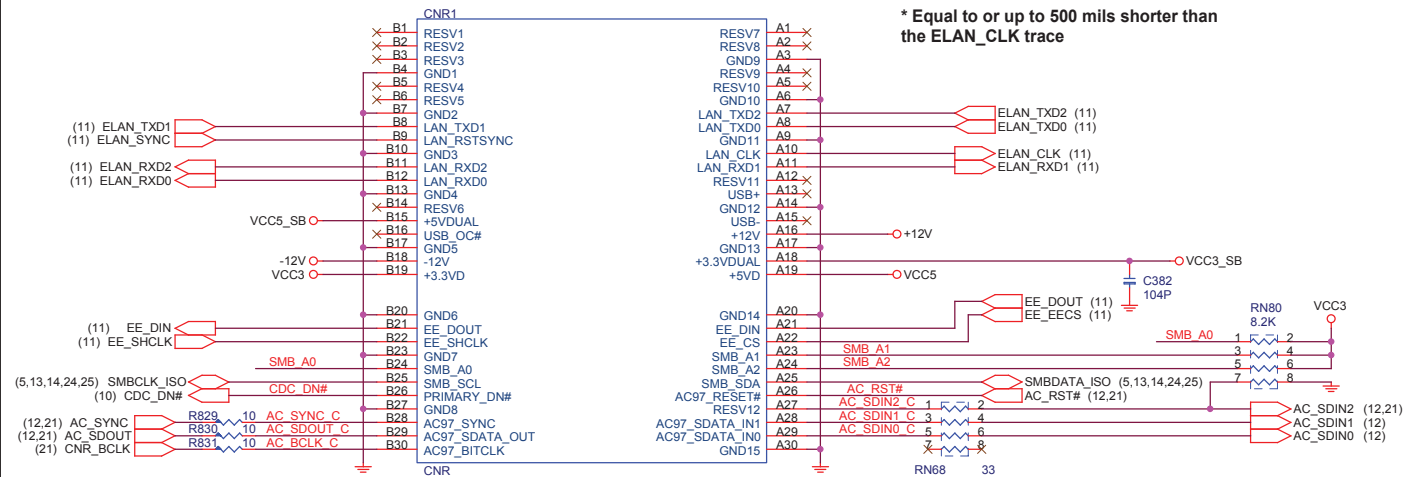


PCB Fiducials

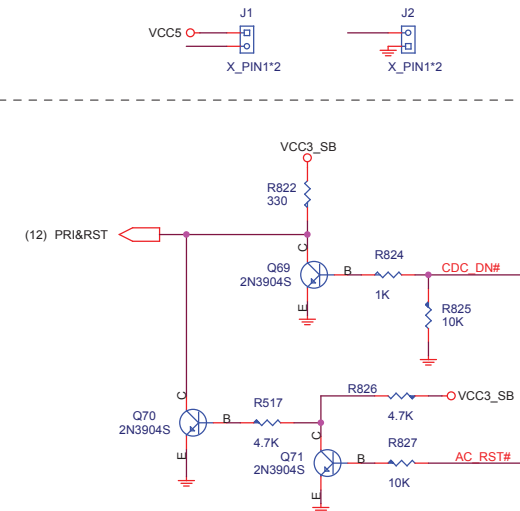


CNR RISER

- * LAN Trace width : 5 mils
- * AC'97 Trace Spacing : 10 mils
- * Maxium trace length < 9.5"
- * Equal to or up to 500 mils shorter than the ELAN_CLK trace

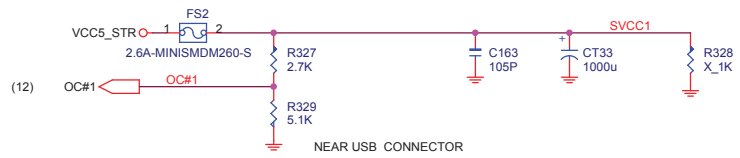


SIMULATION TRACE

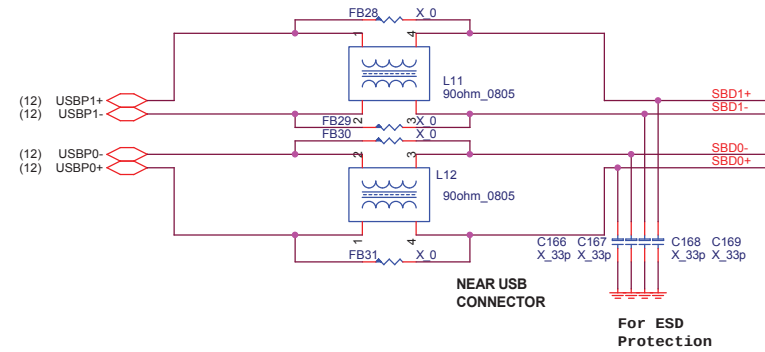


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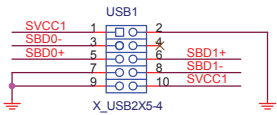
POWER CIRCUIT FOR USB PORT 0,1,2,3



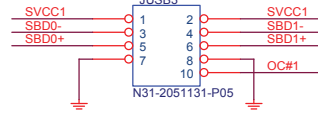
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



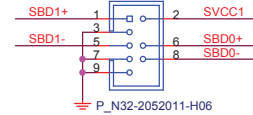
MSI Front USB Header



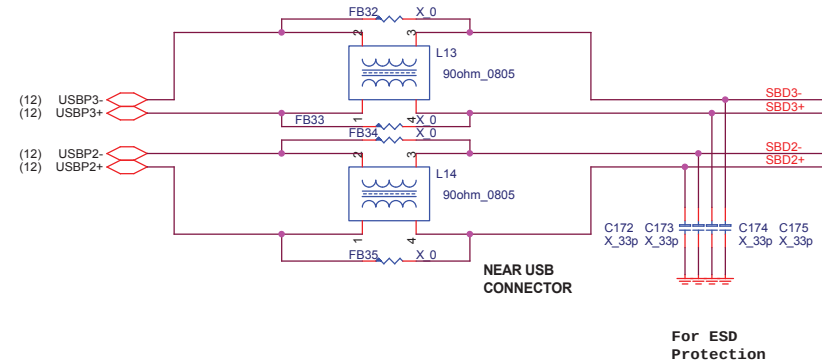
Intel Front USB Header



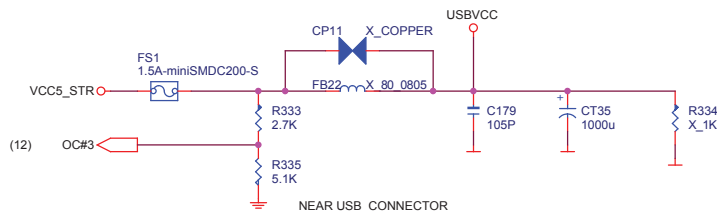
P1 Front USB Header



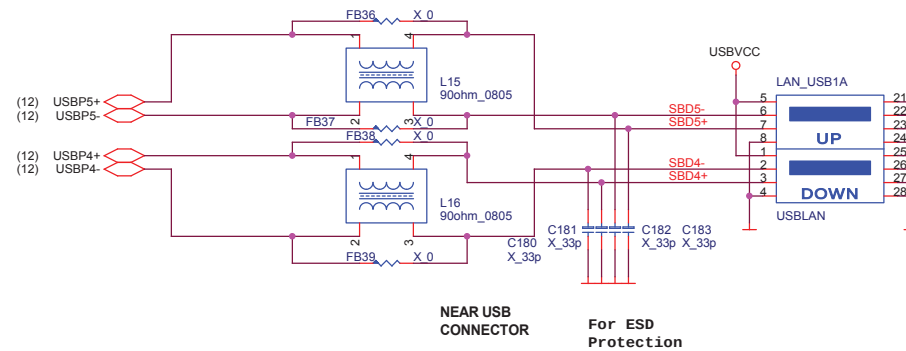
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



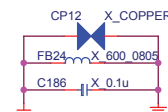
POWER CIRCUIT FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 4,5

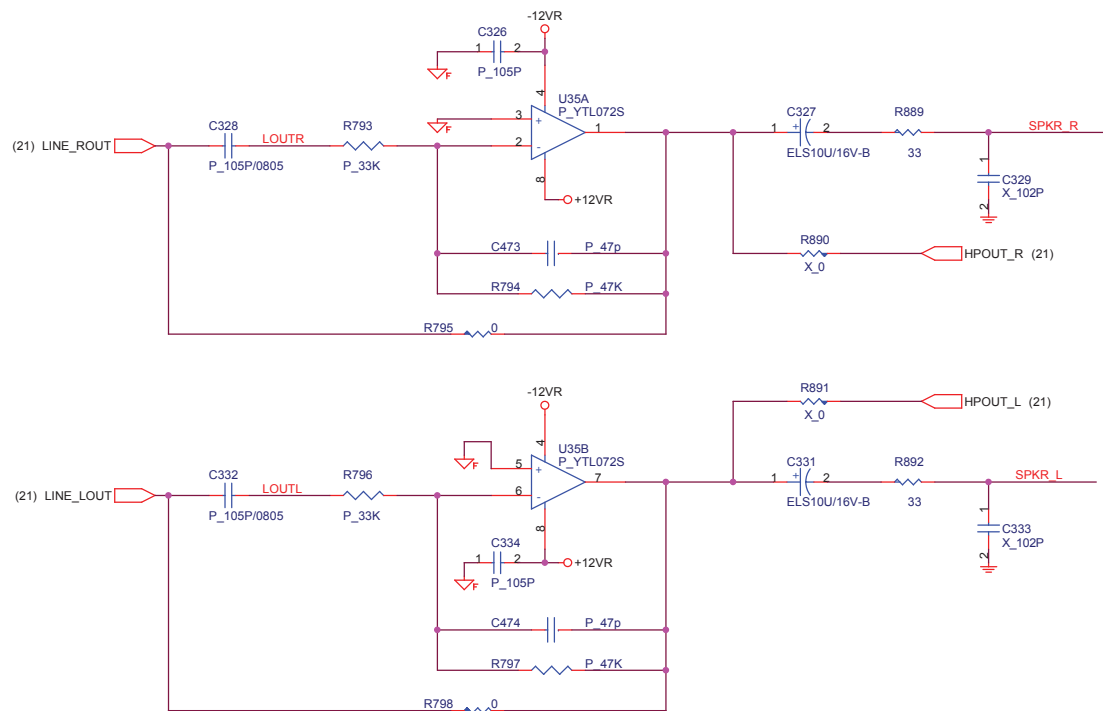


- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signals Trace, Spacing : 18 mils
- * USB Power Trace must be 40mils width

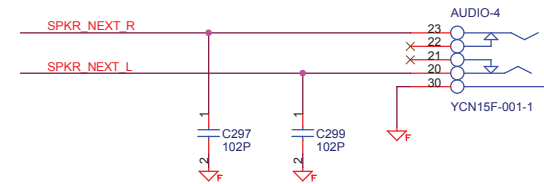


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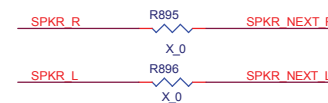
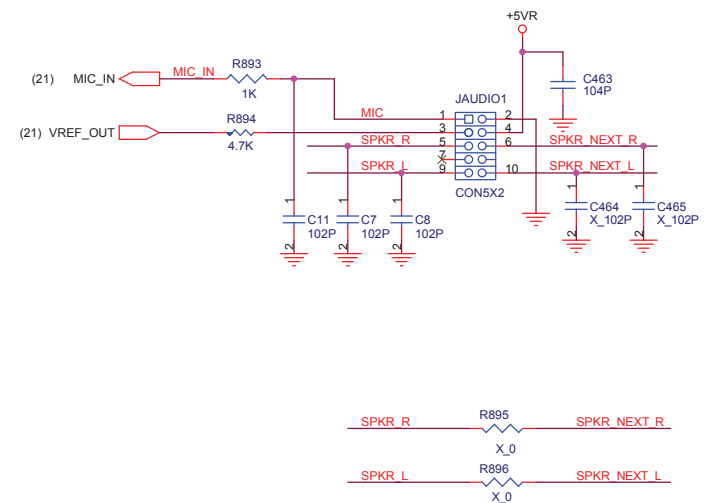
SPEAKER OUT CIRCUIT



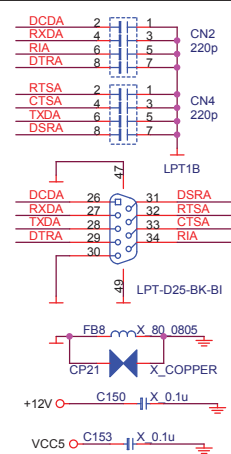
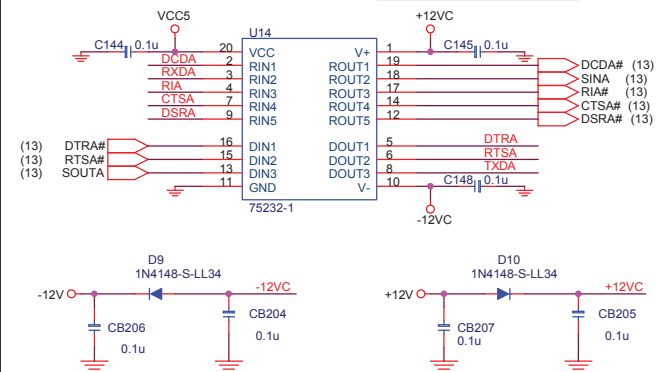
SPEAKER OUT JACK



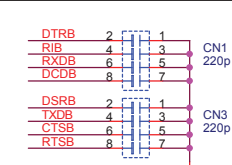
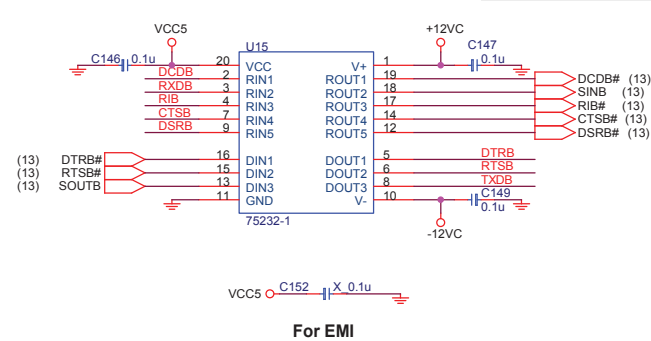
FOR Intel INTERNAL HEADER



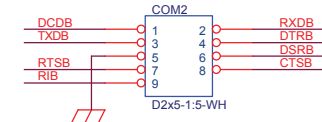
SERIAL PORT 1



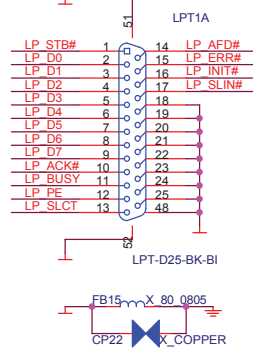
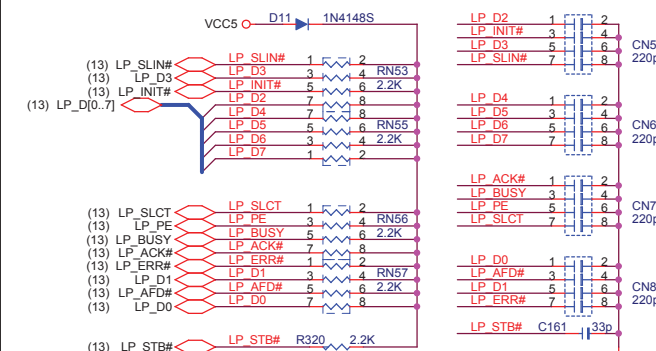
SERIAL PORT 2



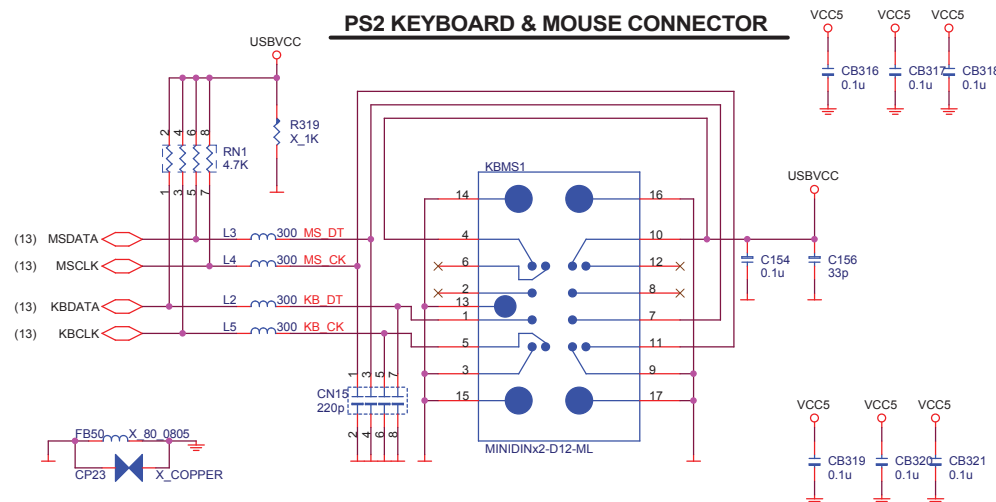
COM2 HEADER



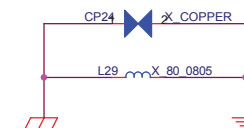
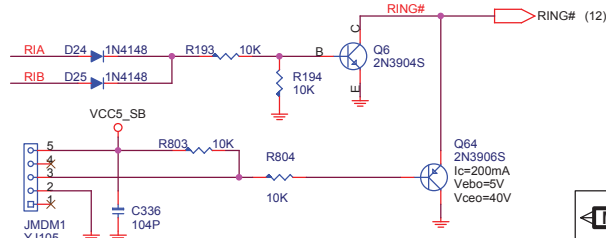
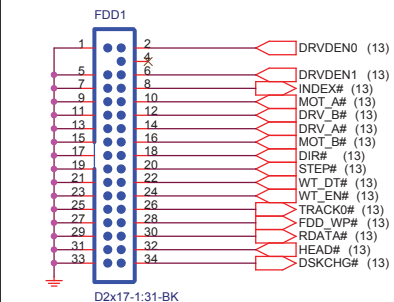
PARALLAL PORT



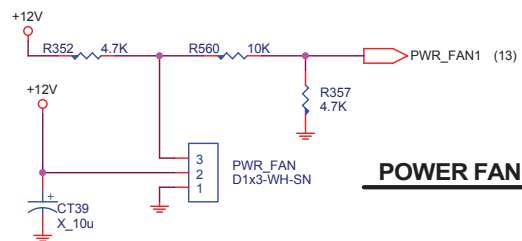
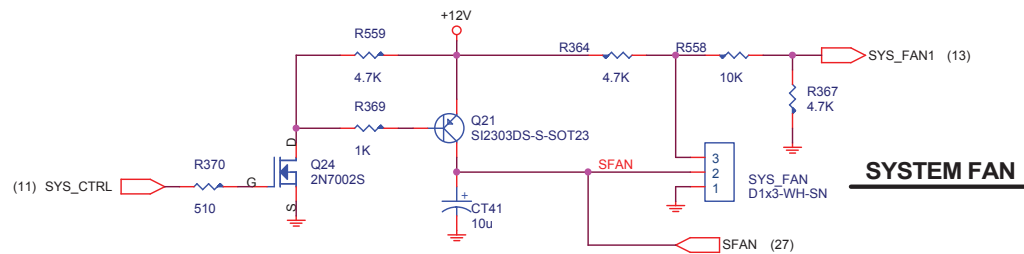
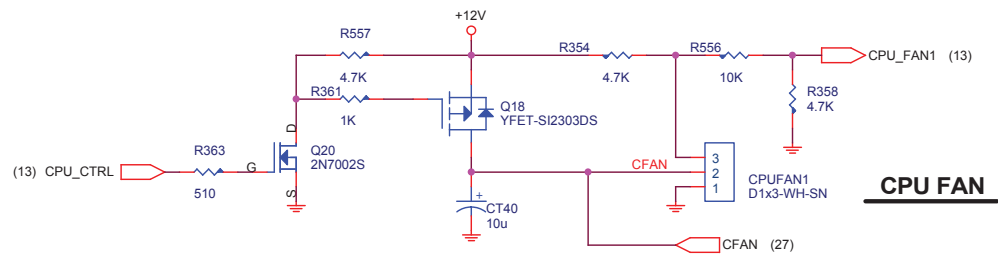
PS2 KEYBOARD & MOUSE CONNECTOR



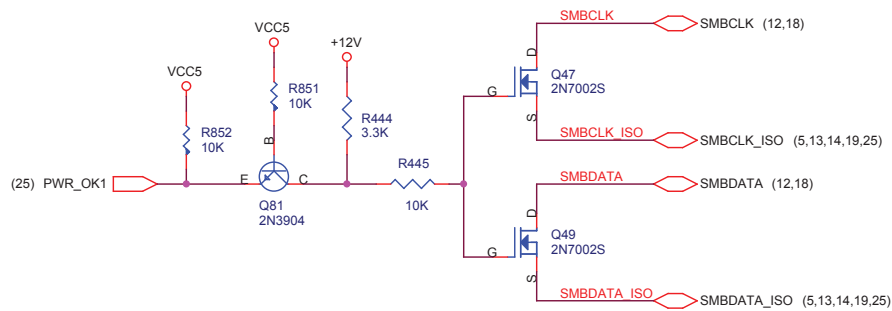
FLOPPY CONNECTOR



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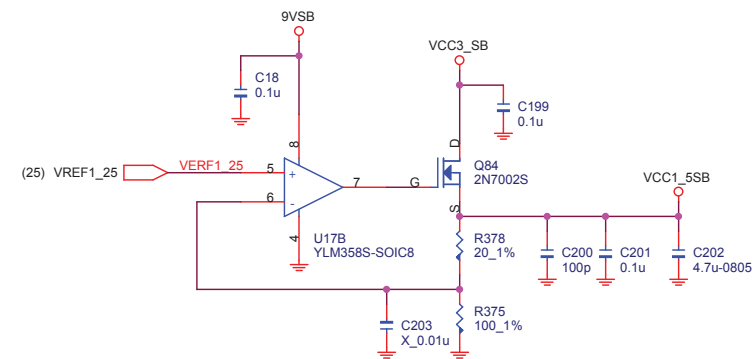


SMBus Isolation

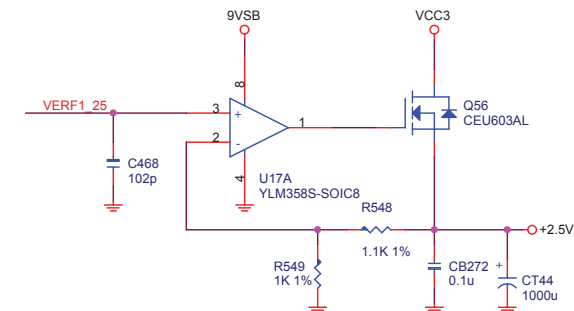


1.5V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



AGP4X & GMCH 1.5V POWER TRANSLATOR



MSI MICRO-STAR INT'L CO.,LTD.			
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	Standby
MEM_STR	Main	Standby	Standby

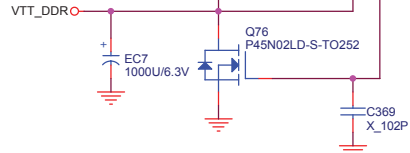
SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

DDR VTT Power

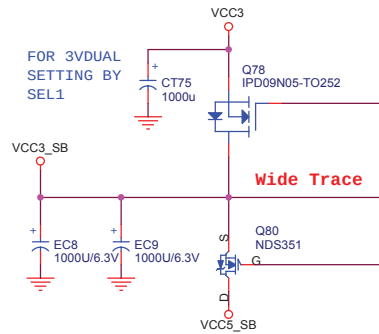
1.25V/2.1A



SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

FOR 3VDUAL
SETTING BY SEL1

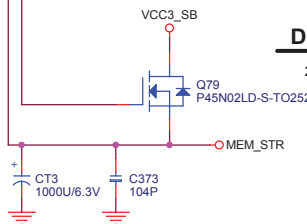


** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

Wide Trace

DDR 2.5V Power

2.5V/2.8A+5.92A



VCC_VID / VID_GOOD

Place MOSFET near CPU

THIS PIN IS OPEN DRAIN OUTPUT

VCC_VID (7)
1.2V/0.1A

VID_GOOD (26)
1.0V

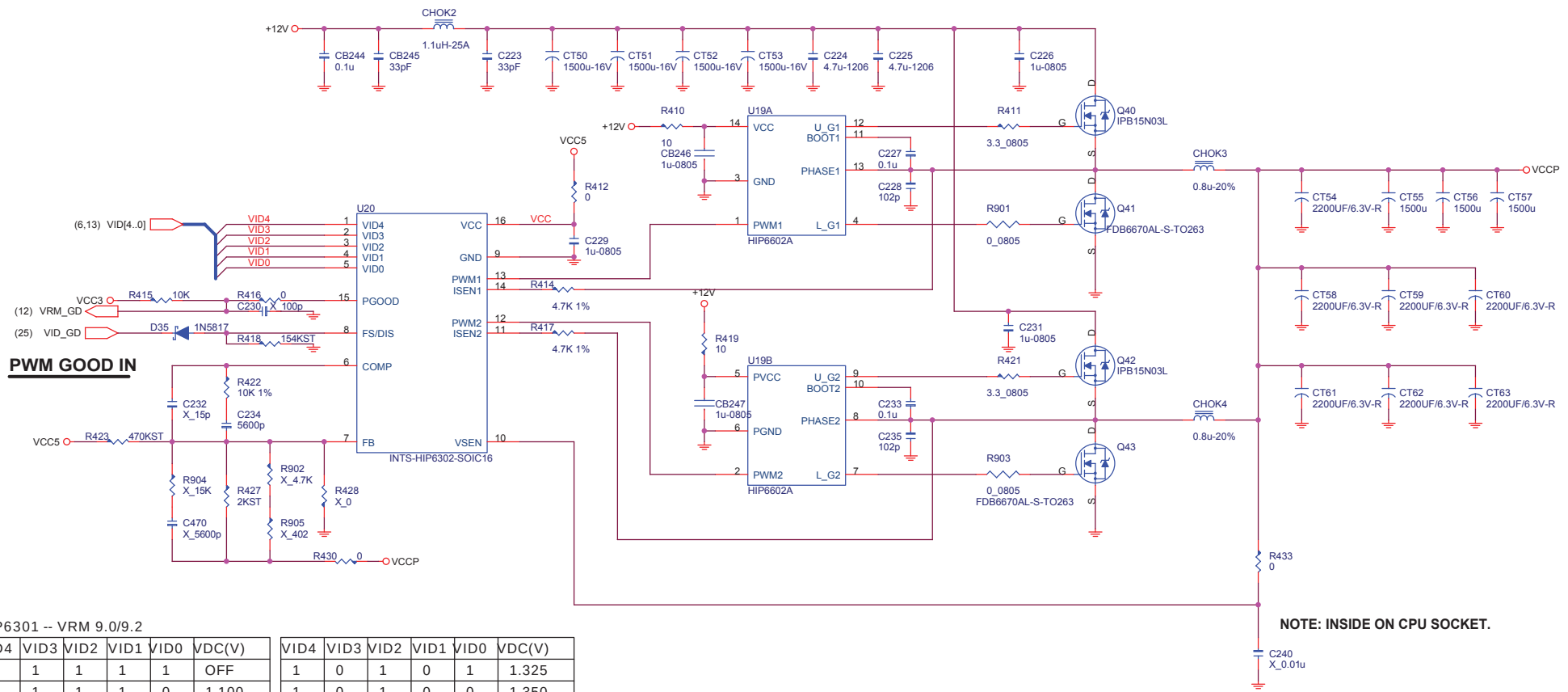
5V DUAL Power

Low RDS ON MOSFET

CHARGE PUMP VOLTAGE OUTPUT



PWM GOOD IN

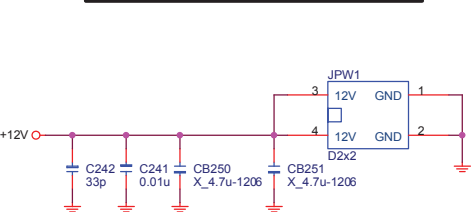


HIP6301 -- VRM 9.0/9.2

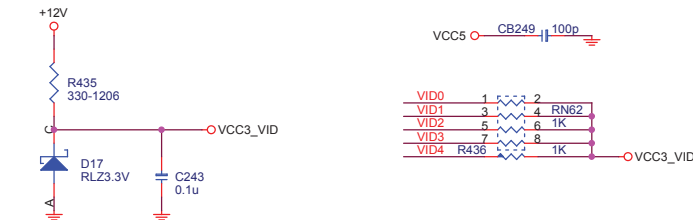
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	1	OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550

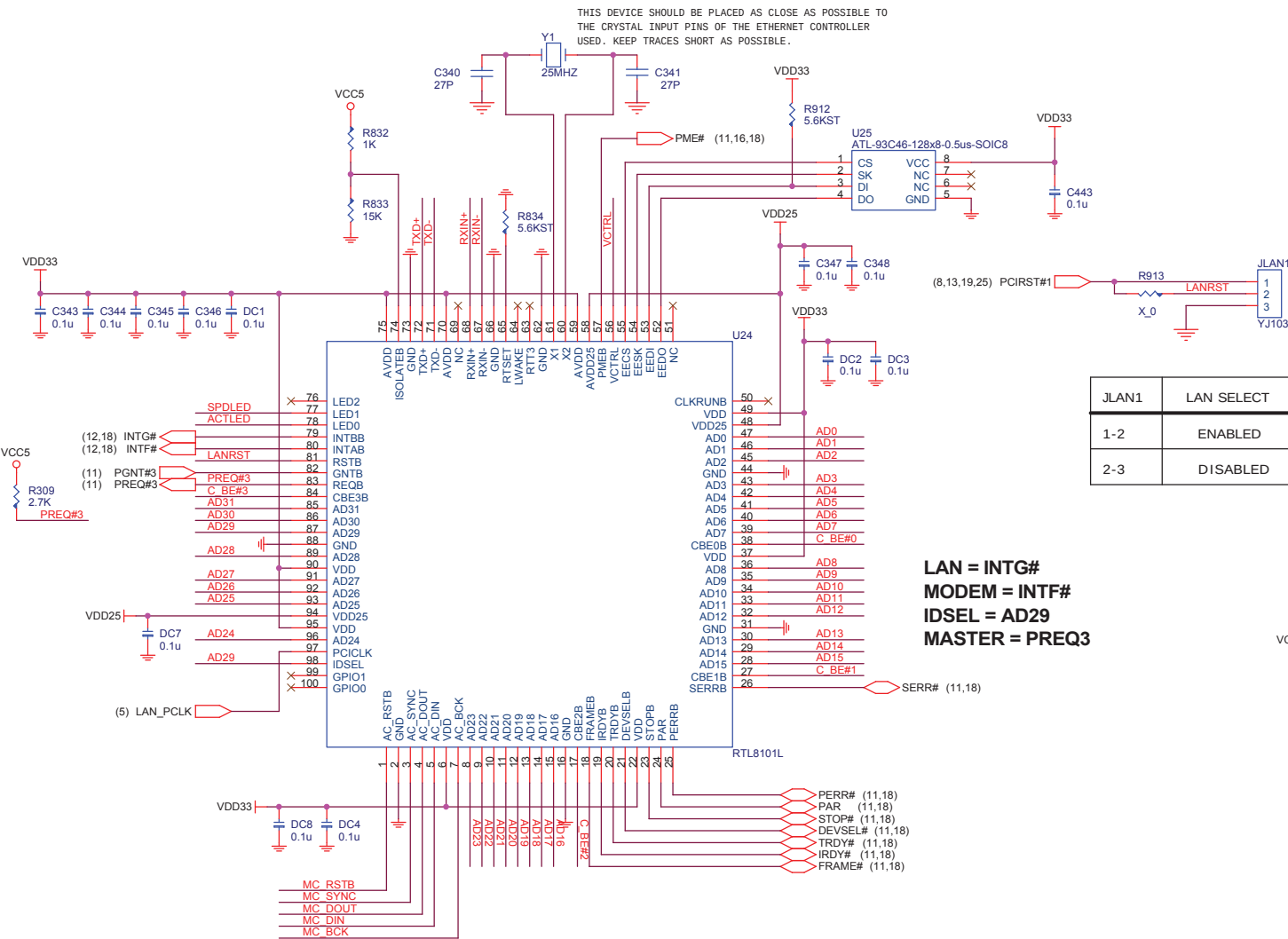
ATX12V POWER CONNECTOR



VID PULL-UP RESISTORS

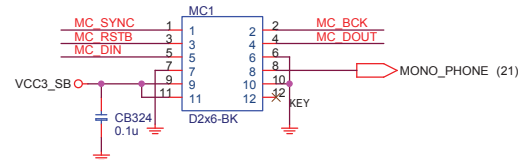
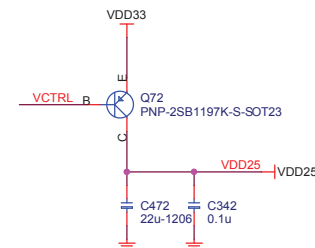
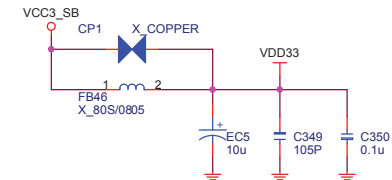


THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.

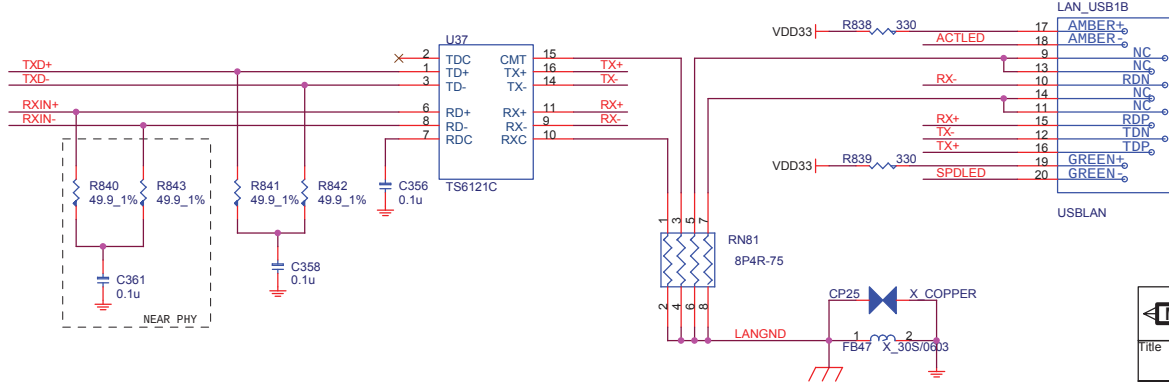


LAN = INTG#
MODEM = INTF#
IDSEL = AD29
MASTER = PREQ3

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

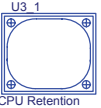
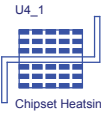


(11,18) AD[31:0] → AD[31:0]
(11,18) C_BE#[3:0] → C_BE#[3:0]





BAT1_X
BATTERY



U4-900
FAN Header



U4-901
FAN Header

JBAT1(1-2)
YJUMPER-MG

JAUDIO1(5-6)
YJUMPER-MG

J6(1-2)
P_YJUMPER-MG

JFP2(4-6)
YJUMPER-MG

JAUDIO1(9-10)
YJUMPER-MG

BIOS_WP(1)
X_YJUMPER-MG

JLAN1(1-2)
YJUMPER-MG

JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

J6 Config. mode	
1 - 2	Normal *
2 - 3	Configuration Mode
OPEN	Recovery

BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED



P_SiGT-STAC9756-S1